BURR-BROWN®

Integrated Circuits Data Book

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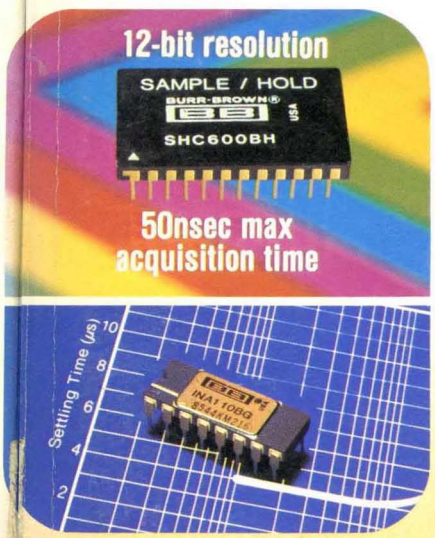
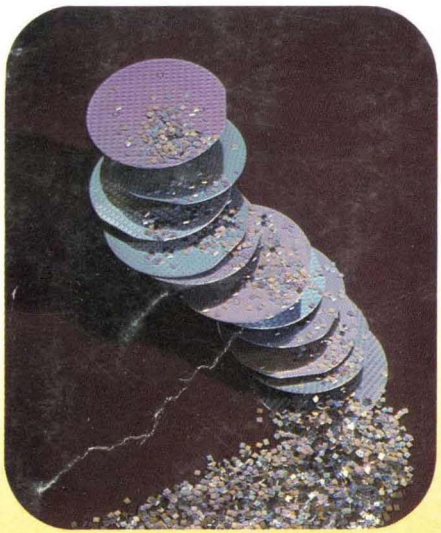
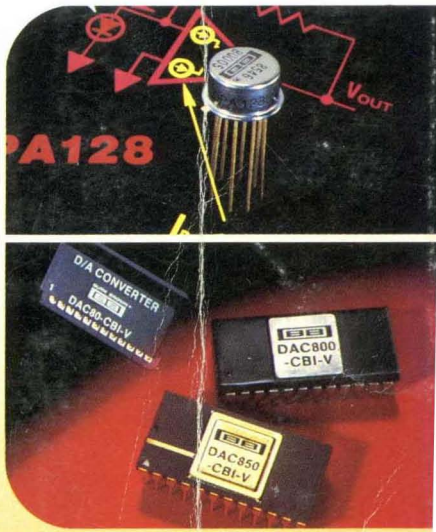






Operational Amplifiers
Instrumentation Amplifiers
Isolation Amplifiers
Analog Circuit Functions
Military Products

A/D Converters
D/A Converters
Sample/Hold Converters
Multiplexers
Power Supplies

BURR-BROWN®

MODEL INDEX

A complete price list for these products is located inside the back cover.

INTEGRATED CIRCUITS DATA BOOK

International Airport Industrial Park - PO Box 11400 - Tucson, Arizona 85734 - Telephone 602-746-1111 - TWX 910-952-1111 - Cable BBRCORP - Telex 66-6491

 LI-335 Printed in U.S.A. June, 1986

Building An Unequalled Reputation, Worldwide, for Quality, Performance, Reliability

Data acquisition, signal conditioning, and computer I/O components and systems from Burr-Brown are recognized and used worldwide. Over the past two decades these products have earned a reputation for superior quality, exceptional performance, and consistent reliability—perhaps the best reputation for workmanship in our industry.

Cost effectiveness of our products has been proven in a host of applications: in industrial and process control, test instrumentation, aerospace systems, environmental monitoring, medical-clinical, and analytical instrumentation.

We have built our credibility by being totally responsive to our customers' requirements. Knowing the problems encountered in the real world, we apply the best, most appropriate, and proven technologies to achieve practical solutions.

Our integrated circuits have become more complex, more sophisticated as we continue to combine and vertically integrate multiple functions into smaller, space-saving packages. When you select these versatile "mini-systems" your design and assembly time is decreased while your products' performance and reliability are increased. And today you pay less, per function, as these microcircuits and subsystems work more efficiently for you.

At Burr-Brown, quality and reliability are built-in by conservative designs, carefully selected components and manufacturing processes, by intensive, thorough testing, and stringent quality control.

Customers also give Burr-Brown high marks for service and support. Our technical literature is among the best in the industry and our global applications and sales force is factory trained—highly qualified to help you in product selection and use. Wherever in the world you contact us, you can be assured of prompt, courteous, efficient service—and superb product performance.

BURR-BROWN INTEGRATED CIRCUITS DATA BOOK

The Burr-Brown Integrated Circuits Data Book contains detailed product data sheets for our broad line of precision integrated circuits for signal processing, data acquisition, and data transmission. In addition, it includes supplementary data for these products, such as screening programs available, a list of other technical literature that you may order, accessories, and information on how to interface with Burr-Brown.

To acquaint you with the full breadth of the Burr-Brown product line, we also include information on the products from our Data Acquisition And Control Systems Division. Additional detailed manuals are available for most of these products upon request. Contact your local Burr-Brown Sales Office listed inside the back cover.

For your convenience the Data Book is separated into 16 major sections: Operational Amplifiers, Instrumentation Amplifiers, Isolation Amplifiers, Analog Circuit Functions, Analog-to-Digital Converters, Digital-to-Analog Converters, Sample/Hold Amplifiers, Data Acquisition Components, CMOS Multiplexers, Voltage-to-Frequency Converters, High Performance Chips, Military Products, BS9000 Products, Modular Power Supplies, Accessories, and System and Subsystem Products. Each right-hand page has a margin tab on the outer edge. The tab index on page V provides a visual guide to the major sections.

At the beginning of each product section, you will find explanatory material and a selection guide to assist you in selecting the product most suitable for your applications. The selection guide also contains page numbers for individual product data sheets.

An index of products in this Data Book, listed in alphanumeric order, is found on the inside of the front cover. A general table of contents appears on page IV.

TABLE OF CONTENTS

TAB INDEX

INTERFACING WITH BURR-BROWN

PLACING AN ORDER

Orders may be placed via mail, telephone, TWX or TELEX with any authorized Burr-Brown field sales office, sales representative, or our headquarters in Tucson. Our offices are listed inside the back cover of this Data Book. When placing your order, please provide complete information, including model number with all option designations, product description or name, quantity desired, and ship-to and bill-to addresses.

TECHNICAL ASSISTANCE

Burr-Brown has a large and competent field sales force, backed-up by an experienced staff of applications specialists. They will be most happy to assist you in selecting the right product for your application. This service is available, without charge, from all sales offices and from our headquarters in Tucson.

DATA SHEETS/LITERATURE

Product data sheets or manuals, similar to those in this Data Book but perhaps containing more recent revisions, are available for most of the products listed in this Data Book. Application Notes and other supporting literature are also available on request. If you wish a copy of any of these items simply contact your nearest Burr-Brown sales office or representative.

PRICES AND TERMS

Prices listed in this catalog, unless otherwise noted, apply only to domestic USA customers; all other customers should contact their local Burr-Brown representative for price information.

All prices are FOB Tucson, Arizona, USA, in U.S. dollars. Applicable federal, state, and local taxes are extra. Terms are net 30 days. Prices and specifications are subject to change without notice.

QUOTATIONS

Price quotations made by Burr-Brown or its authorized field sales representatives are valid for 30 days. Delivery quotations are subject to reconfirmation at the time of order placement.

RETURNS AND WARRANTY SERVICE

When returning products for any reason, it is necessary to contact Burr-Brown, prior to shipping, for authorization and shipping instructions. In the U.S., contact our Tucson headquarters. In other countries, contact your nearest Burr-Brown field sales office or representative. Returned units should be shipped prepaid and must be accompanied by the original purchase order number and date, and an explanation of the malfunction. Upon receipt of the returned unit, Burr-Brown will verify the malfunction and will inform you of the warranty status, cost to repair or replace, credits, and status of replacement units where applicable.

HIGH RELIABILITY PROGRAMS

Burr-Brown is committed to providing products of high quality and reliability. This is manifested by designing for conservative stress levels, careful selection of components and processes, comprehensive testing procedures, thorough quality control practices, and optional programs of military screening. The Burr-Brown Q-Progam, described below, is intended as a reliable enhancement of standard Burr-Brown products by subjecting them to a defined program of environmental stresses.

An even more comprehensive reliability program, aimed particularly at the needs of military customers, is the /MIL program which includes manufacturing procedures per MIL-M-38510 and screening procedures per MIL-STD-883. This program, and the products available under it, are described in section eleven of this Data Book.

THE Q-PROGRAM

The Burr-Brown Q-Program is designed to further enhance the reliability of Burr-Brown microcircuits at a reasonable cost. The Q-Program is appropriate for some military and aerospace applications, industrial control systems, medical patient monitoring instrumentation, and other applications where failure may be expensive or where replacement of parts is difficult and inconvenient. The Q-Program consists of the screening of standard Burr-Brown microcircuits in accordance with applicable test methods of MIL-STD-883. The screening sequences shown below identify the mechanical, electrical, and thermal stresses applied to all Q-Products.

Q-SCREENING SEQUENCE

STEP	SCREEN	PROCEDURE
Routinely performed 100% on all Burr-Brown products	INTERNAL VISUAL INSPECTION (precap)	Burr-Brown QC4118 (copies available on request)
	ELECTRICAL TEST, 100% (postcap)	Per appropriate Burr-Brown product data sheet
①	STABILIZATION BAKE	MIL-STD-883, Method 1008
②	TEMPERATURE CYCLING	MIL-STD-883, Method 1010
③	HERMETICITY, GROSS LEAK	MIL-STD-883, Method 1014
④	HERMETICITY, FINE LEAK	MIL-STD-883, Method 1014
⑤	BURN-IN	MIL-STD-883, Method 1015
⑥	CONSTANT ACCELERATION (centrifuge)	MIL-STD-883, Method 2001
⑦	FINAL ELECTRICAL TEST	Per appropriate Burr-Brown product data sheet

Explanation of Screening Steps...

- **INTERNAL VISUAL INSPECTION**

  This is a microscopic examination of the product performed prior to capping in order to verify conformance to Burr-Brown standards of quality for material, methods of construction, and workmanship. Its purpose is to detect and eliminate devices with internal defects which could lead to failures under the thermal, mechanical, and electrical stresses of extended operation.

- **100% ELECTRICAL TEST**

  Each product is tested in accordance with the appropriate Burr-Brown product data sheet. These tests will normally include static and dynamic tests at +25°C, as well as drift tests over the operating temperature range.

①STABILIZATION BAKE

In this step the product is stored at an elevated temperature without electrical stress applied. The purpose is to stabilize circuit parameters through accelerated aging.

②TEMPERATURE CYCLING

The product is alternately exposed to extremes of high and low temperature such as would be experienced when parts or equipment are transferred to and from heated shelters in arctic areas. The purpose is to check for permanent changes in operating characteristics and physical damage resulting principally from variation in dimensions and other physical properties.

③④HERMETICITY - GROSS AND FINE LEAK

The purpose of these two tests is to verify the hermeticity of the seal of integrated circuits having internal cavities which are evacuated or filled with gas. The test is intended to determine those devices which, when exposed for long periods to atmosphere containing high concentration of water vapor or other gaseous contaminants, would degrade in performance and become latent failures.

⑤BURN-IN

During burn-in the device is subjected to a high temperature for an extended period of time, with power applied. The burn-in screen is performed in order to eliminate marginal devices with inherent defects. In the absence of burn-in, these defective devices would be expected to result in infant mortality or early lifetime failures under use conditions.

⑥CONSTANT ACCELERATION

This test subjects the product to a constant acceleration force in a centrifuge. The purpose is to detect and eliminate devices having structural and mechanical weaknesses that could lead to failure when subjected to mechanical stresses during application.

⑦FINAL ELECTRICAL TEST

This is a repetition of the 100% electrical test above. Devices which pass this test, after successfully passing the above screening test, are qualified as Q-parts.

HANDLING PROCEDURES FOR MICROCIRCUITS

In developing handling procedures for microcircuits it is well to keep in mind that virtually all semiconductor devices are vulnerable in some degree to damage from the discharge of electrostatic energy. This is due to the small dimensions involved. It should be noted that electrostatic damage (ESD) to semiconductor devices can cause effects ranging from a degradation in performance, to latent failure, or immediate failure, of the device involved.

We at Burr-Brown are directly concerned with this subject because our products are designed to achieve the highest performance and precision. Often, this depends upon a high degree of device matching or precision within the microcircuit and any degradation due to ESD is unacceptable. Accordingly, we have developed a set of guidelines that will minimize the exposure of our products to possible electrostatic damage during manufacturing and handling at Burr-Brown. We strongly recommend that our customers adopt similar procedures throughout their handling and utilization of these and other semiconductor products. These guidelines are summarized below:

GUIDELINES

1. Eliminate souces of ESD by removing static generating materials from all areas that handle products, by grounding all operators, equipment, and work stations where products are handled or stored, and by transporting and shipping products in static-free containers.
2. Shield products from potential damage by using a conductive Faraday shield where practical.
3. Shunt electrostatic charges and voltage potentials to zero where practical by connecting together all leads of each device by means of a conductive material.

ELIMINATE SOURCES OF ESD

It is highly desirable to eliminate static-generating materials from close proximity to products. This includes the elimination of all plastics, such as wrapping and packing materials, which have not been properly treated to achieve antistatic properties.

Antistatic is a term used to describe insulators which have been treated to reduce their very high surface resistance from a value in excess of a million meghoms to a value in the vicinity of one megohm.

The human body has been electrically characterized as a capacitor ranging from 100 to 200 picofarads and a resistance ranging from 500 ohms to several thousand ohms. As in electrical applications, the best way to prevent an accumulation of charge, or to drain the accumulation of existing charge on a capacitor, is to short the capacitor terminals together. The body is one plate of the capacitor with earth being the other. The only way to effectively short this capacitor is to connect the body to earth ground. For reasons of safety, this connection should include approximately one megohm of series resistance, or a ground fault interrupter. There should be periodic measurement to assure proper continuity all the way from the wrist strap connection to earth ground, and that the safety protection is operational. The wrist strap must have continuity to the skin in order to drain off the accumulated charge. Work station surfaces should be metallic or conductive plastic and should also be grounded through one megohm of series resistance, or have ground fault interrupters.

Static-free containers are important in storing and transporting product because the product could act as one plate of the capacitor and the container the other plate. Thus, it is possible to induce a charge, and therefore create a voltage, on the product without ohmic contact. Because of area and spacing considerations only unusual situations could cause damage, but it is nevertheless a possibility.

SHIELDING

In even the most optimum environments, there is always the potential for some accumulation of charge. The most positive control is to shield the product from potentially damaging electrostatic fields by use of a highly conductive (Faraday) shield. Antistatic enclosures or wrappers are only low enough in resistance to disperse accumulated charge. The Faraday shield must be low enough in resistance to completely conduct any electrostatic field around the product and prevent any field inside the enclosure. To be totally effective the Faraday shield must completely enclose the product. In addition, only antistatic materials may be used inside the container to assure that internal charge is not developed.

SHUNTING

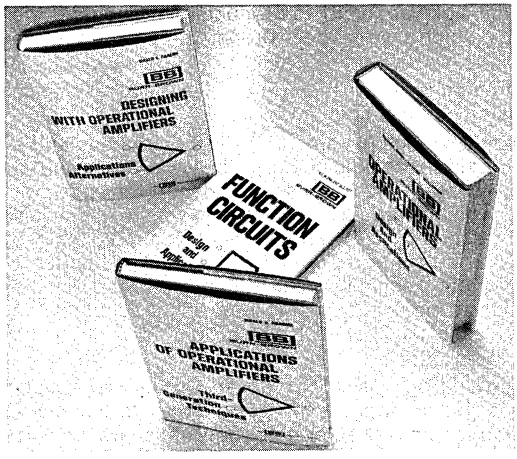
Shunting is one of the most cost-effective ways to protect products during assembly, testing, packing, unpacking, and handling. With a short circuit across sensitive terminals, it is nearly impossible to develop the voltages required for damage to occur. The limitation to this occurs when it is possible to induce large voltages internally in complex microcircuits. We can only shunt or short the exterior connections.

OTHER MEASURES

To help minimize the buildup of electrostatic charge it is desirable to control relative humidity to as high a value as practical (50% is recommended). In addition, where it is not possible to ground all surfaces, or where non-conducting surfaces cannot be completely eliminated, a good alternative may be the use of ionized air blowers.

BURR-BROWN TECHNICAL LIBRARY

The Burr-Brown engineering staff, in cooperation with McGraw-Hill have authored the world's most extensive and authoritative library dealing with the art of analog signal conditioning, conversion, and computation. These books, respected and referenced throughout the international engineering community, are available to you directly from Burr-Brown.



FUNCTION CIRCUITS
Design and Applications

This new volume in the growing Burr-Brown series is the first to deal with the multi-faceted area of analog function circuits. FUNCTION CIRCUITS explores in depth both the design theory and numerous applications for such analog functions as Multipliers, Dividers, Logarithmic Amplifiers, Exponentiators, RMS Converters, and Active Filters. It also shows clearly how to specify and test these functions, which are increasingly becoming available in the form of integrated circuits. As in previous Burr-Brown books, the emphasis is on practicality while maintaining a rigorous treatment of theory. Numerous graphs and formulas are presented to allow the user to obtain optimum circuit performance (over 300 pages and 200 illustrations).

DESIGNING WITH OPERATIONAL AMPLIFIERS
Applications Alternatives

This latest volume in Burr-Brown's well-known series on Operational Amplifiers presents a wealth of new applications and circuit techniques which have evolved since publication of the previous two books. The applications are presented in a manner that will aid the user in developing further circuits. In addition to providing completed designs, the applications include explanations of circuit operation. Practical limitations are discussed and pertinent design equations presented to allow adaptation to specific application requirements.

New applications include amplifier performance improvement techniques, signal analyzers, signal conditioners, absolute-value circuits, signal generators, computing circuits, data transmission circuits, and test an measurement circuits (approximately 270 pages and 200 illustrations).

OPERATIONAL AMPLIFIERS
Design and Applications

Covering basic theory, test methods, amplifier design techniques, and applications, this pioneer work provides *practical* information which can be directly applied to instrumentation design.

The book is divided into two principal parts and two appendices. Part I considers the design of operational amplifiers, offers insight into the factors determining performance characteristics, and outlines the techniques available for their control. Part II presents a wide range of practical operational amplifier applications, and provides sufficient descriptions of operation to permit design adaption from the specific circuits described. In Appendix A the basic theory of operational amplifiers is reviewed to provide an accompanying reference. Appendix B gives concise definitions of the performance parameters used to characterize operational amplifiers, and provides associated test circuits (over 470 pages and 300 illustrations).

APPLICATIONS OF OPERATIONAL AMPLIFIERS

Third Generation Techniques

This is the second volume in the operational amplifier series. More than just a collection of circuit or theoretical analysis, the book presents numerous applications of operational amplifiers in a variety of electronic equipment: specialized amplifiers, signal controls, processors, waveform generators, and special-purpose circuits. It is a storehouse of detailed practical information, featuring numerous circuit diagrams, circuit values, pertinent design equations, error sources, and test-based comments on the efficiency of the arrangements and devices (over 230 pages and 170 illustrations)

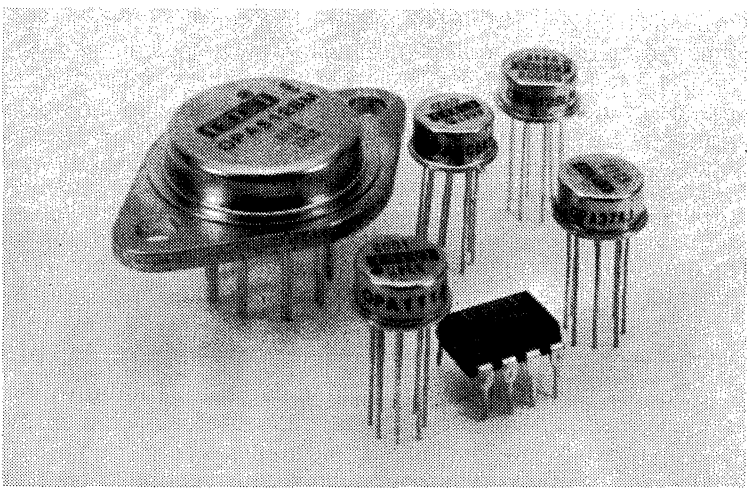
BURR-BROWN *UPDATE*

The Burr-Brown *Update* is published several times per year to keep our customers informed about new product developments, literature, and applications. If you would like to receive this publication on a regular basis, please contact your nearest Burr-Brown sales office or representative and ask to be put on our *Update* mailing list.

APPLICATION NOTES

Burr-Brown engineers have compiled a library of Application Notes to assist you in your designs. These notes are listed below and are available on request.

OPERATIONAL AMPLIFIERS



Burr-Brown operational amplifiers are listed in eight applications groups and are described below. This enables the user to determine and select the best operational amplifier available for a design requirement. Instrumentation amplifiers and isolation amplifiers are described in sections 2 and 3 respectively.

General Purpose—General purpose operational amplifiers are suited for a wide variety of applications. They give moderately good performance over a wide range of parameters at moderate cost. This applications group contains both FET and bipolar input models with frequency responses of 0.5MHz to 1.5MHz and offset voltages as low as 1mV.

Low Drift—Low drift operational amplifiers are best suited for applications where accuracy must be preserved over a substantial temperature range. These amplifiers are optimized to minimize the initial input offset voltage and input offset voltage change with temperature. Input offset drifts from 0.1μV/°C to 5μV/°C are available within this group.

Low Bias Current—Low bias current operational amplifiers consist of FET input designs. This group includes amplifiers with input bias currents from 0.01pA to 1nA. Applications with large feedback resistances or large source resistances (long time constants, integrators, current sources, etc.) and buffer applications will benefit by the use of low bias current amplifiers.

Low Noise—This group contains low noise bipolar and FET input operational amplifiers. Burr-Brown units offer guaranteed noise spectral density, 100% tested. In applications like low noise signal conditioning, light measurements, radiation measurements, photodiode circuits or low noise data acquisition, the fully characterized and tested voltage noise performance of these units allows the designer to truly bound noise errors.

Wideband—Wideband operational amplifiers have bandwidths greater than 10MHz. This group also contains fast settling and high slew rate amplifiers. These amplifiers reduce phase errors at high frequencies and accurately reproduce complex waveforms. These amplifiers are well suited for pulse, video, fast settling, and multiplexing applications.

High Voltage—The amplifiers in this group are designed to provide large output voltage swings and to operate on wide ranges of supply voltage. Output voltages greater than ±10V and up to ±145V are available in this applications group (up to 290V, single supply). These amplifiers provide good frequency response and performance in other parameters. Most models have electrically isolated packages and automatic thermal sensing and shutdown. All units have FET inputs to minimize bias current errors when the amplifier is used with the large resistances usually found with high voltage amplifiers.

High Current—These amplifiers provide output currents from ±10mA to ±10A. They are used with small load resistances, coax cable impedance, and with power booster applications. Many units have self-contained thermal sensing and shutdown to automatically protect the amplifiers from overheating and damage. All of these units have electrically isolated packages.

Unity-Gain Buffer (Power Booster)—Unity-gain buffer amplifiers have a wide variety of applications. They are used to boost the output current capability of another amplifier, buffer an impedance that might load a critical circuit or to be an input impedance converter from an input which must not be loaded. These amplifiers may also be used inside the feedback loop of another operational amplifier to form a current-boosted, composite amplifier.

SELECTION GUIDE

GENERAL PURPOSE

These moderately priced FET and bipolar op amps offer good performance over a wide range of parameters. These are good options when a special function op amp is not required. You can be confident that Burr-Brown's quality and reliability are inherent in their design.

GENERAL PURPOSE												
		Offset Voltage, max		Bias Current	Open Loop	Frequency Response		Rated Output, min				
Description	Model	At 25°C, (±mV)	Temp Drift, (±μV/°C)	(25°C), max (nA)	Gain, min (dB)	Unity Gain (MHz)	Slew Rate (V/μsec)	(±V)	(±mA)	Temp Range[1]	Package	Page
Low Power	OPA21GZ	0.5	5	50	114	0.3	0.2	13.6	1.3	Ind	DIP	1-13
	OPA21EZ	0.1	1	25	120	0.3	0.2	13.7	1.4	Ind	DIP	1-13
Switchable Input	OPA201AG	0.5	5	50	114	0.5	0.1	13.5	5	Com	DIP	1-87
	OPA201BG	0.2	2	40	114	0.5	0.1	13.5	5	Com	DIP	1-87
	OPA201CG	0.1	1	25	120	0.5	0.1	13.5	5	Com	DIP	1-87
	OPA201SG	0.2	2	40	114	0.5	0.1	13.5	5	MIL	DIP	1-87
FET	OPA103AM	0.50	25	−0.002	106	1	1.3	10	5	Ind	TO-99	1-45
	OPA103BM	0.50	15	−0.001	106	1	1.3	10	5	Ind	TO-99	1-45
	OPA103CM	0.25	5	−0.001	106	1	1.3	10	5	Ind	TO-99	1-45
	OPA103DM	0.25	2	−0.001	106	1	1.3	10	5	Ind	TO-99	1-45
Low Cost FET	OPA121KP	3	10	±0.010	106	2	2	10	5	Com	DIP	1-67
	OPA121KM	2	10	±0.005	110	2	2	10	5	Com	TO-99	1-67
Wide Temp Range	OPA11HT	5	5[2]	±25	94	12.0	7.0	10	15	−55°C to +175°C	TO-99	1-9
	OPA27HT	0.05	0.25[2]	1μA	120	6	1.9	12	16[2]	−55°C to +200°C	TO-99	1-29
	OPA37HT	0.05	0.25[2]	1μA	120	36	11.9	12	16[2]	−55°C to +200°C	TO-99	1-29
	OPA111HT	0.5	8[2]	0.002	114	2	2	10	5	−55°C to +200°C	TO-99	1-63

NOTES: (1) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (2) Typical.

LOW DRIFT

Low offset voltage drift vs temperature performance in both FET and bipolar input types is obtained by our sophisticated drift compensation techniques. First, the drift is measured and then special laser trim techniques are used to minimize the drift and the initial offset voltage at 25°C. Finally, "max drift" performance is retested for conformance with specifications.

LOW DRIFT (≤5μV/°C)												
		Offset Voltage, max		Bias Current	Open Loop	Frequency Response		Rated Output, min				
Description	Model	At 25°C (±mV)	Temp Drift (±μV/°C)	(25°C), max (nA)	Gain, min (dB)	Unity Gain (MHz)	Slew Rate (V/μsec)	(±V)	(±mA)	Temp Range[1]	Package	Page
FET	OPA103CM	0.25	5	−0.001	106	1	1.3	10	5	Ind	TO-99	1-45
	OPA103DM	0.25	2	−0.001	106	1	1.3	10	5	Ind	TO-99	1-45
	OPA111AM	0.5	5	±0.002	114	2	2	11	5	Ind	TO-99	1-53
	OPA111BM	0.25	1	±0.001	120	2	2	11	5	Ind	TO-99	1-53
	OPA111SM	0.5	5	±0.002	114	2	2	11	5	MIL	TO-99	1-53
Wideband	OPA156AM	2	5	0.05	94	6	14	10	5	MIL	TO-99	1-81
	OPA356AM	2	5	0.05	94	6	14	10	5	Com	TO-99	1-81
	OPA606LM	0.5	5	±0.01	100	13	35	12	5	Com	TO-99	1-135
Dual FET	OPA2111BM	0.5	2.8	±0.004	114	2	2	11	5	Ind	TO-99	1-143

LOW DRIFT (≤5μV/°C) (Continued)												
		Offset Voltage, max		Bias Current	Open Loop	Frequency Response		Rated Output, min				
Description	Model	At 25°C (±mV)	Temp Drift (±μV/°C)	(25°C), max (nA)	Gain, min (dB)	Unity Gain (MHz)	Slew Rate (V/μsec)	(±V)	(±mA)	Temp Range[1]	Package	Page
Bipolar	OPA27A	0.025	0.6	±40	120	8	1.9	12	16.6	MIL		1-17
	OPA37A	0.025	0.6	±40	120	63[2]	11.9	12	16.6	MIL		1-17
	OPA27B	0.060	1.3	±55	120	8	1.9	12	16.6	MIL		1-17
	OPA37B	0.060	1.3	±55	120	63[2]	11.9	12	16.6	MIL		1-17
	OPA27C	0.100	1.8	±80	117	8	1.9	12	16.6	MIL		1-17
	OPA37C	0.100	1.8	±80	117	63[2]	11.9	12	16.6	MIL	TO-99/	1-17
	OPA27E	0.025	0.6	±40	120	8	1.9	12	16.6	Ind	DIP	1-17
	OPA37E	0.025	0.6	±40	120	63[2]	11.9	12	16.6	Ind		1-17
	OPA27F	0.060	1.3	±55	120	8	1.9	12	16.6	Ind		1-17
	OPA37F	0.060	1.3	±55	120	63[2]	11.9	12	16.6	Ind		1-17
	OPA27G	0.100	1.8	±80	117	8	1.9	12	16.6	Ind		1-17
	OPA37G	0.100	1.8	±80	117	63[2]	11.9	12	16.6	Ind		1-17
	OPA27GP	0.100	1.8	±80	117	8	1.9	12	16.6	Com	DIP	1-17
	OPA37GP	0.100	1.8	±80	117	63[2]	11.9	12	16.6	Com	DIP	1-17
Ultra-Low Bias FET	OPA128LM	0.5	5	±75fA	110	1	3	10	5	Com	TO-99	1-73
Low Power	OPA21EZ	0.1	1	25	120	0.3	0.2	13	5	Ind	DIP	1-13
	OPA21GZ	0.5	5	50	114	0.3	0.2	13	5	Ind	DIP	1-13

NOTES: (1) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (2) Gain-bandwidth product for OPA37. $A_V = 5$ minimum.

LOW BIAS CURRENT

Our many years of experience in designing, manufacturing and testing FET amplifiers gives us unique abilities in providing low and ultra low bias current op amps. These amplifiers offer bias currents as low as 75fA (75×10^{-15} amps) and low voltage drift as low as 1μV/°C. With offset voltage laser-trimmed to as low as 250μV, the need for expensive trim pot adjustments is eliminated.

LOW BIAS CURRENT (≤100pA)												
		Offset Voltage, max		Bias Current	Open Loop	Frequency Response		Rated Output, min				
Description	Model[1]	At 25°C, (±mV)	Temp Drift, (±μV/°C)	(25°C), max (pA)	Gain, min (dB)	Unity Gain (MHz)	Slew Rate (V/μsec)	(±V)	(±mA)	Temp Range[2]	Package	Page
Premium Performance	OPA111AM	0.5	5	±2	114	2	2	11	5	Ind	TO-99	1-53
	OPA111BM	0.25	1	±1	120	2	2	11	5	Ind	TO-99	1-53
	OPA111SM	0.5	5	±2	114	2	2	11	5	MIL	TO-99	1-53
Low Bias Current	OPA103AM	0.50	25	−2	106	1	1.3	10	5	Ind	TO-99	1-45
	OPA103BM	0.50	15	−1	106	1	1.3	10	5	Ind	TO-99	1-45
	OPA103CM	0.25	5	−1	106	1	1.3	10	5	Ind	TO-99	1-45
	OPA103DM	0.25	2	−1	106	1	1.3	10	5	Ind	TO-99	1-45
Low Noise	OPA101AM	0.50	10	−15	94	10	6.5	12	12	Ind	TO-99	1-33
	OPA101BM	0.25	5	−10	94	10	6.5	12	12	Ind	TO-99	1-33
	OPA102AM	0.50	10	−15	94	40	14	12	12	Ind	TO-99	1-33
	OPA102BM	0.25	5	−10	94	40	14	12	12	Ind	TO-99	1-33
Ultra-Low Bias Current	OPA104AM	1.0	25	−0.300	106	1	2.2	10	5	Ind	TO-99	1-49
	OPA104BM	0.50	15	−0.150	106	1	2.2	10	5	Ind	TO-99	1-49
	OPA104CM	0.50	10	−0.075	106	1	2.2	10	5	Ind	TO-99	1-49
	3528AM, (Q)	0.50	15	−0.300	88	0.7	0.3	10	5	Ind	TO-99	1-174
	3528BM, (Q)	0.25	5	−0.150	92	0.7	0.3	10	5	Ind	TO-99	1-174
	3528CM, (Q)	0.50	10	−0.075	90	0.7	0.3	10	5	Ind	TO-99	1-174
	OPA128JM	1	20	±0.300	94	1	3	10	5	Com	TO-99	1-73
	OPA128KM	0.5	10	±0.150	110	1	3	10	5	Com	TO-99	1-73
	OPA128LM	0.5	5	±0.075	110	1	3	10	5	Com	TO-99	1-73
	OPA128SM	0.5	10	±0.150	110	1	3	10	5	MIL	TO-99	1-73
Dual FET	OPA2111AM	0.75	6	±8	110	2	2	11	5	Ind	TO-99	1-143
	OPA2111BM	0.5	2.8	±4	114	2	2	11	5	Ind	TO-99	1-143
	OPA2111SM	0.75	6	±8	110	2	2	11	5	MIL	TO-99	1-143
Quad FET	OPA404AG	1	3[4]	±8	88	6.4	35	11.5	5	Ind	DIP	1-95
	OPA404BG	0.75	3[4]	±4	92	6.4	35	12	5	Ind	DIP	1-95
	OPA404SG	1	3[4]	±8	88	6.4	35	11.5	5	MIL	DIP	1-95
Low Cost	OPA121KM	2	10	±5	110	2	2	11	5	Com	TO-99	1-67
	OPA121KP	3	10	±10	106	2	2	11	5	Com	DIP	1-67

LOW BIAS CURRENT (≤100pA) (Continued)													
		Offset Voltage, max		Bias Current	Open Loop	Frequency Response		Rated Output, min					
Description	Model[1]	At 25°C, (±mV)	Temp Drift, (±μV/°C)	(25°C), max (pA)	Gain, min (dB)	Unity Gain (MHz)	Slew Rate (V/μsec)	(±V)	(±mA)	Temp Range[2]	Package	Page
Wideband	3554AM, (Q)	2	50	−50	100	1000	1000	10	100	Ind	TO-3	1-188
	3554BM, (Q)	1	15	−50	100	1000	1000	10	100	Ind	TO-3	1-188
	3554SM, (Q)	1	25	−50	100	1000	1000	10	100	MIL	TO-3	1-188
	OPA156AM	2	5	50	94	6	14	10	5	MIL	TO-99	1-81
	OPA356AM	2	5	50	94	6	14	10	5	Com	TO-99	1-81
	OPA606KM	1.5	5[4]	±15	95	12.5	33	11	5	Com	TO-99	1-135
	OPA606LM	0.5	5	±10	100	13	35	12	5	Com	TO-99	1-135
	OPA606SM	1.5	5[4]	±15	95	12.5	33	11	5	MIL	TO-99	1-135
	OPA606KP	3	10[4]	±25	90	12	30	11	5	Com	DIP	1-135
High Current	3571AM, (Q)	2	40	−100	94	0.5	3	30	1A	Ind	TO-3	1-196
	3572AM	2	40	−100	94	0.5	3	30	2A	Ind	TO-3	1-196
High Voltage	3580J	10	30	−50	86	5	15	30	60	Com	TO-3	1-206
	3581J	3	25	−20	94	5	20	70	30	Com	TO-3	1-206
	3582J, (Q)	3	25	−20	100	5	20	145	15	Com	TO-3	1-206
	3583AM, (Q)	3	25	−20	105	5	30	140	75	Ind	TO-3	1-210
	3583JM	3	25	−20	94	5	30	140	75	Com	TO-3	1-210
	3584JM, (Q)	3	25	−20	100	20	150	145	15	Com	TO-3	1-214
Fast Settling	OPA600VM	4	20	−100	86	6000[3]	500	10	200	MIL	DIP	12-94
	OPA600UM	5	100	−100	86	6000[3]	500	10	200	MIL	DIP	12-94
Low Cost, Ultra-Low Bias Current	AD515JH	3	50	0.300	86	0.35	1	10	5	Com	TO-99	1-153
	AD515KH	1	15	0.150	92	0.35	1	10	5	Com	TO-99	1-153
	AD515LH	1	25	0.075	88	0.35	1	10	5	Com	TO-99	1-153

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, section 12. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Gain-bandwidth product. (4) Typical.

LOW NOISE

Now both FET and bipolar input op amps are offered with guaranteed low noise specifications. Until now the designer had to rely on "typical" specs for his demanding low noise designs. These fully characterized parts allow a truly complete error budget calculation.

LOW NOISE (Guaranteed e_n)													
		Noise Voltage at 10kHz, max	Bias Current (25°C) max	Offset Voltage, max		Open Loop Gain, min	Frequency Response		Rated Output, min		Temp Range		
Description	Model	(nV/√Hz)	(pA)	At 25°C (±mV)	Temp Drift (±μV/°C)	(dB)	GBW (MHz)	Slew Rate, min (V/μsec)	(±V)	(±mA)	[1]	Package	Page
Bipolar	OPA27A	3.8	±40nA	0.025	0.6	120	8	1.7	12	16.6	MIL		1-17
	OPA37A	3.8	±40nA	0.025	0.6	120	63	11	12	16.6	MIL		1-17
	OPA27B	3.8	±55nA	0.060	1.3	120	8	1.7	12	16.6	MIL		1-17
	OPA37B	3.8	±55nA	0.060	1.3	120	63	11	12	16.6	MIL		1-17
	OPA27C	4.5	±80nA	0.100	1.8	117	8	1.7	12	16.6	MIL		1-17
	OPA37C	4.5	±80nA	0.100	1.8	117	63	11	12	16.6	MIL	TO-99/	1-17
	OPA27E	3.8	±40nA	0.025	0.6	120	8	11	12	16.6	Ind	DIP	1-17
	OPA37E	3.8	±40nA	0.025	0.6	120	63	11	12	16.6	Ind		1-17
	OPA27F	3.8	±55nA	0.060	1.3	120	8	1.7	12	16.6	Ind		1-17
	OPA37F	3.8	±55nA	0.060	1.3	120	63	11	12	16.6	Ind		1-17
	OPA27G	4.5	±80nA	0.100	1.8	117	8	1.7	12	16.6	Ind		1-17
	OPA37G	4.5	±80nA	0.100	1.8	117	63	11	12	16.6	Ind		1-17
FET	OPA101AM	8	−15	0.5	10	94	20	5	12	12	Ind	TO-99	1-33
	OPA101BM	8	−10	0.25	5	94	20	5	12	12	Ind	TO-99	1-33
	OPA102AM	8	−15	0.5	10	94	40	10	12	12	Ind	TO-99	1-33
	OPA102BM	8	−10	0.25	5	94	40	10	12	12	Ind	TO-99	1-33
	OPA111AM	8	±2	0.5	5	114	2	1	11	5	Ind	TO-99	1-53
	OPA111BM	8	±1	0.25	1	120	2	1	11	5	Ind	TO-99	1-53
	OPA111SM	8	±2	0.5	5	114	2	1	11	5	MIL	TO-99	1-53
	OPA606LM	13	±10	0.5	5	100	13	25	12	5	Com	TO-99	1-135
Low Cost	OPA27GP	4.5	±80nA	0.100	1.8	117	8	1.9[2]	10	16.6	Com	DIP	1-17
	OPA37GP	4.5	±80nA	0.100	1.8	117	63	11.9[2]	10	16.6	Com	DIP	1-17
Dual FET	OPA2111AM	8	±8	0.75	6	110	2	1	11	5	Ind	TO-99	1-143
	OPA2111BM	8	±4	0.5	2.8	114	2	1	11	5	Ind	TO-99	1-143
	OPA2111SM	8	±4	0.75	6	110	2	1	11	5	MIL	TO-99	1-143

NOTES: (1) Ind = −25°C to +85°C; MIL = −55°C to +125°C; Com = 0°C to +70°C. (2) Typical.

UNITY-GAIN BUFFER (Power Booster)

These versatile amplifiers: boost the output current capability of another amplifier; buffer an impedance that might load a critical circuit; may be used inside the feedback loop of another op amp to form a current-boosted, composite amplifier. Currents as high as ±100mA are available with speeds of 2000V/μsec.

UNITY-GAIN BUFFER													
		Rated Output, min		Frequency Response					Open Loop				
Description	Model	(±V)	(±mA)	−3dB (MHz)	Full Power BW (MHz)	Slew Rate (V/μsec)	Gain (V/V)	Input Impedance (Ω)	Gain (dB)	.Temp Range[1]	Package	Page
Noninverting	3553AM	10	200	300	32	2000	≈1	10^{11}	NA	Ind	TO-3	1-184

NOTES: (1) Ind = −25°C to +85°C.

WIDE BANDWIDTH

Design expertise in wideband circuits combines with our fullyBurr-Brown high speed amplifiers also offer outstanding DC developed technology to create cost effective wideband op amps. performance specifications.

WIDE BANDWIDTH (≥5MHz)													
		Frequency Response				Rated Output, min		Offset Voltage, max		Open Loop			
Description	Model[1]	GBW (MHz)	Slew Rate, min (V/μsec)	t_s ±0.1% (nsec)	Compensation	(±V)	(±mA)	At 25°C (±mV)	Temp Drift (±μV/°C)	Gain, min (dB)	Temp Range [2]	Package	Page
FET	3554AM, (Q)	1700,	1000	120	ext.	10	100	2	50	100	Ind	TO-3	1-188
	3554BM, (Q)	A=	1000	120	ext.	10	100	1	15	100	Ind	TO-3	1-188
	3554SM, (Q)	1000	1000	120	ext.	10	100	1	25	100	MIL	TO-3	1-188
	3551J	50, A=10	250	400	ext.	10	10	1	50[3]	88	Com	TO-99	1-180
	3551S, (Q)	50, A=10	250	400	ext.	10	10	1	50[3]	88	MIL	TO-99	1-180
	3550J	10, A=10	65	400	int.	10	10	1	50[3]	88	Com	TO-99	1-176
	3550K	20, A=1	100	400	int.	10	10	1	50[3]	88	Com	TO-99	1-176
	3550S, (Q)	10, A=1	65	400	int.	10	10	1	50[3]	88	MIL	TO-99	1-176
Bipolar	3508J	100, A=100	20	—	ext.	10	10	5	30[3]	98	Com	TO-99	1-163
	3507J, (Q)	20, A=10	80	200	ext.	10	10	10	30[3]	83	Com	TO-99	1-161
FET	OPA156AM	6, A = 1	10	1.5μsec	int.	10	5	2	5	94	MIL	TO-99	1-81
	OPA356AM	6, A = 1	10	1.5μsec	int.	10	5	2	5	94	Com	TO-99	1-81
	OPA605H	200, A=1000	300[3]	300	ext.	10	30	1	25	96[3]	Com	DIP	1-129
	OPA605A	200, A=1000	300[3]	300	ext.	10	30	1	25	96[3]	Ind	DIP	1-129
	OPA605K	200, A=1000	300[3]	300	ext.	10	30	0.5	5	96[3]	Com	DIP	1-129
	OPA605C	200, A=1000	300[3]	300	ext.	10	30	0.5	5	96[3]	Ind	DIP	1-129
	OPA606KM	12.5	22	1μsec	int.	11	5	1.5	5[3]	95	Com	TO-99	1-135
	OPA606LM	13	25	1μsec	int.	12	5	0.5	5	100	Com	TO-99	1-135
	OPA606SM	12.5	22	1μsec	int.	11	5	1.5	5[3]	95	MIL	TO-99	1-135
	OPA606KP	12	20	1μsec	int.	11	5	3	10[3]	90	Com	TO-99	1-135
Quad FET	OPA404AG	6.4	24	600	int.	11.5	5	1	3[3]	88	Ind	DIP	1-95
	OPA404BG	6.4	28	600	int.	12	5	0.75	3[3]	92	Ind	DIP	1-95
	OPA404SG	6.4	24	600	int.	11.5	5	1	3[3]	88	MIL	DIP	1-95
Low Noise Bipolar	OPA27A	8, A = 1	1.7	—	int.[4]	12	16.6	0.025	0.6	120	MIL		1-17
	OPA37A	63, A = 5	11	—	int.[4]	12	16.6	0.025	0.6	120	MIL		1-17
	OPA27B	8, A = 1	1.7	—	int.[4]	12	16.6	0.060	1.3	120	MIL		1-17
	OPA37B	63, A = 5	11	—	int.[4]	12	16.6	0.060	1.3	120	MIL		1-17
	OPA27C	8, A = 1	1.7	—	int.[4]	12	16.6	0.100	1.8	117	MIL		1-17
	OPA37C	63, A = 5	11	—	int.[4]	12	16.6	0.100	1.8	117	MIL	TO-99/	1-17
	OPA27E	8, A = 1	1.7	—	int.[4]	12	16.6	0.025	0.6	120	Ind	DIP	1-17
	OPA37E	63, A = 5	11	—	int.[4]	12	16.6	0.025	0.6	120	Ind		1-17
	OPA27F	8, A = 1	1.7	—	int.[4]	12	16.6	0.060	1.3	120	Ind		1-17
	OPA37F	63, A = 5	11	—	int.[4]	12	16.6	0.060	1.3	120	Ind		1-17
	OPA27G	8, A = 1	1.7	—	int.[4]	12	16.6	0.100	1.8	117	Ind		1-17
	OPA37G	63, A = 5	11	—	int.[4]	12	16.6	0.100	1.8	117	Ind		1-17
Low Noise FET	OPA101AM	20, A=100	5	2.5μsec	int.	12	12	0.5	10	94	Ind	TO-99	1-33
	OPA101BM	20, A=100	5	2.5μsec	int.	12	12	0.25	5	94	Ind	TO-99	1-33
	OPA102AM	40, A=100	10	1.5μsec	int.	12	12	0.5	10	94	Ind	TO-99	1-33
	OPA102BM	40, A=100	10	1.5μsec	int.	12	12	0.25	5	94	Ind	TO-99	1-33
Fast Settling	OPA600UM	6000, A=1000	500	80	ext.	9	180	5	100	86	MIL	DIP	12-94
	OPA600VM	6000, A=1000	500	80	ext.	9	180	4	20	86	MIL	DIP	12-94
	OPA600BM	5000, A=1000	500	80	ext.	9	180	±5	±80	86	Ind	DIP	1-121
	OPA600CM	5000, A=1000	500	80	ext.	9	180	±4	±40	86	Ind	DIP	1-121
	OPA600SM	5000, A=1000	500	80	ext.	9	180	±5	±100	86	MIL	DIP	1-121
	OPA600TM	5000, A=1000	500	80	ext.	9	180	±4	±80	86	MIL	DIP	1-121
Unity-Gain Buffer	3553AM, (Q)	32	2000	—	—	10	200	50	300[3]	NA	Ind	TO-3	1-184

WIDE BANDWIDTH (≥5MHz) (Continued)													
		Frequency Response				Rated Output, min		Offset Voltage, max		Open Loop Gain, min (dB)	Temp Range [2]		
Description	Model[1]	GBW (MHz)	Slew Rate, min (V/μsec)	t_s ±0.1% (nsec)	Compensation	(±V)	(±mA)	At 25°C (±mV)	Temp Drift (±μV/°C)			Package	Page
Low Cost	OPA27GP	8, A = 1	1.9[3]	—	int.	12	16.6	0.100	1.8	117	Com	DIP	1-17
	OPA37GP	63, A = 5	11.9[3]	—	int.[4]	12	16.6	0.100	1.8	117	Com	DIP	1-17
Wide Temp Range	OPA27HT	6, A = 1	1.9	—	int.	12	16.6[3]	0.050	0.25[3]	120	−55°C to +200°C	TO-99	1-29
	OPA37HT	36, A = 5	11.9	—	int.[4]	12	16.6[3]	0.050	0.25[3]	120		TO-99	1-29
	OPA11HT	12, A=1	4	1.5μsec	ext.	10	15	5[3]	5	98	−55°C to +200°C	TO-99	1-9

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, section 12. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Typical. (4) G = 5 min for OPA37.

HIGH VOLTAGE—HIGH CURRENT

These IC op amp designs set the pace for the industry and are a product of our extensive hybrid circuit technology. Output currents up to ±10A peak and voltages up to ±145V are available.

Output voltages > ±30V to ±145V.

HIGH VOLTAGE													
		Rated Output, min		Offset Voltage, max		Bias Current (25°C), max (pA)	Frequency Response		Open Loop Gain (dB)	Temp Range [2]			
Description	Model[1]	(±V)	(±mA)	At 25°C (±mV)	Temp Drift (±μV/°C)		Unity Gain (MHz)	Slew Rate (V/μsec)			Package	Page
FET	3584JM, (Q)	145	15	3	25	−20	20[3]	150	120	Com	TO-3	1-214
	3583AM, (Q)	140	75	3	25	−20	5	30	118	Ind	TO-3	1-210
	3583JM	140	75	3	25	−20	5	30	118	Com	TO-3	1-210
	3582J	145	15	3	25	−20	5	20	118	Com	TO-3	1-206
	3581J	70	30	3	25	−20	5	20	112	Com	TO-3	1-206
	3580J	30	60	10	30	−50	5	15	106	Com	TO-3	1-206
	3571AM, (Q)	30	1A[4]	2	40	−100	0.5	3	94	Ind	TO-3	1-196
	3572AM	30	2A[5]	2	40	−100	0.5	3	94	Ind	TO-3	1-196

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, section 12. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Gain-bandwidth product. (4) 2A peak. (5) 5A peak.

Output currents > ±15mA to ±10A.

HIGH CURRENT												
		Rated Output, min		Offset Voltage, max		Bias Current (25°C), max (pA)	Frequency Response		Open Loop Gain (dB)	Temp Range [2]		
Description	Model[1]	(±V)	(±mA)	At 25°C, (±mV)	Temp Drift, (±μV/°C)		Unity Gain (MHz)	Slew Rate (V/μsec)			Package	Page
High Power	OPA501AM	20	10A	10	65	40nA	1	1.35	94	Ind	TO-3	1-103
	OPA501BM	26	10A	5	40	20nA	1	1.35	98	Ind	TO-3	1-103
	OPA501RM	20	10A	10	65	40nA	1	1.35	94	MIL	TO-3	1-103
	OPA501SM	26	10A	5	40	20nA	1	1.35	98	MIL	TO-3	1-103
	OPA511AM	22	5A	10	65	40	1	1	91	Ind	TO-3	1-111
	OPA512BM	35	10A	6	65	30	4	2.5	110	Ind	TO-3	1-116
	OPA512SM	35	15A	3	40	20	4	2.5	110	MIL	TO-3	1-116
	3573AM	20	2A[5]	10	65	40nA	1	2.6	94	Ind	TO-3	1-202
	3572AM	30	2A[5]	2	40	−100	0.5	3	94	Ind	TO-3	1-196
	3571AM, (Q)	30	1A[4]	2	40	−100	0.5	3	94	Ind	TO-3	1-196
Wideband	3554AM, (Q)	10	100	2	50	−50	1700[3]	1200	100	Ind	TO-3	1-188
	3554BM, (Q)	10	100	1	15	−50	1700[3]	1200	100	Ind	TO-3	1-188
	3554SM, (Q)	10	100	1	25	−50	1700[3]	1200	100	MIL	TO-3	1-188
High Voltage	3584JM, (Q)	145	15	3	25	−20	20[3]	150	126	Com	TO-3	1-214
	3583AM	140	75	3	25	−20	5	30	118	Ind	TO-3	1-210
	3583JM	140	75	3	25	−20	5	30	118	Com	TO-3	1-210
	3582J	145	15	3	25	−20	5	20	118	Com	TO-3	1-206
	3581J	70	30	3	25	−20	5	20	112	Com	TO-3	1-206
	3580J	30	60	10	30	−50	5	15	106	Com	TO-3	1-206
Booster (Buffer)	3553AM, (Q)	10	200	50	300[6]	−200	300	2000	NA	Ind	TO-3	1-184
	3329/03	10	100	50	—	Bipolar	5	—	NA	Ind	DIP	1-157

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, section 12. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Gain-bandwidth product. (4) 2A peak. (5) 5A peak. (6) Typical.

GLOSSARY OF TERMS AND DEFINITIONS
Operational Amplifiers

COMMON-MODE INPUT IMPEDANCE
The effective impedance (resistance in parallel with capacitance) between either input of an amplifier and its common, or ground terminal.

COMMON-MODE REJECTION (CMR)
When both inputs of a differential amplifier experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) which produces the same output change.

$$\text{CMR (in dB)} = 20 \log_{10} \text{CMV/Error Voltage}$$

Thus a CMR of 80dB means that 1V of common-mode voltage will cause an error of 100μV (referred to input).

COMMON-MODE VOLTAGE (CMV)
That portion of an input signal which is common to both inputs of a differential amplifier. Mathematically it is defined as the average of the signals at the two inputs:

$$\text{CMV} = (e_1 + e_2)/2$$

COMMON-MODE VOLTAGE GAIN
The ratio of the output signal voltage (ideally zero) to the common-mode input signal voltage.

COMMON-MODE VOLTAGE RANGE
The range of input voltage for linear, nonsaturated operation.

DIFFERENTIAL INPUT IMPEDANCE
The apparent impedance, resistance in parallel with capacitance, between the two input terminals.

FULL POWER FREQUENCY RESPONSE
The maximum frequency at which a device can supply its peak-to-peak rated output voltage and current, without introducing significant distortion.

GAIN-BANDWIDTH PRODUCT
A product of small signal, open-loop gain and frequency at that gain.

INPUT BIAS CURRENT
The DC input current required at each input of an amplifier to provide zero output voltage when the input signal and input offset voltage are zero. The specified maximum is for each input.

INPUT BIAS CURRENT VS SUPPLY VOLTAGE
The sensitivity of input bias current to the power supply voltages.

INPUT BIAS CURRENT VS TEMPERATURE
The sensitivity of input bias current to temperature.

INPUT CURRENT NOISE
The input current which would produce, at the output of a noiseless amplifier, the same output as that produced by the inherent noise generated internally in the amplifier when the source resistances are large.

INPUT OFFSET CURRENT
The difference of the two input bias currents of a differential amplifier.

INPUT OFFSET VOLTAGE
The DC input voltage required to provide zero voltage at the output of an amplifier when the input signal and input bias currents are zero.

INPUT OFFSET VOLTAGE VS SUPPLY VOLTAGE I/PSRR
The sensitivity of input offset voltage to the power supply voltages. Both power supply magnitudes are changed in the same direction and over the operating voltage range.

INPUT OFFSET VOLTAGE VS TEMPERATURE (DRIFT)
The rate of change of input offset voltage with temperature. At Burr-Brown, this is the change in input offset voltage from 25°C to the maximum specification temperature, plus the change in input offset voltage from 25°C to the minimum specification temperature, this quantity divided by the specification temperature range.

INPUT OFFSET VOLTAGE VS TIME
The sensitivity of input offset voltage to time.

INPUT VOLTAGE NOISE
The differential input voltage which would produce, at the output of a noiseless amplifier, the same output as that produced by the inherent noise generated internally in the amplifier when the source resistances are small.

MAXIMUM SAFE INPUT VOLTAGE
The maximum, peak value, continuous voltage that may be applied at, or between, the inputs without damage.

OPEN-LOOP GAIN
The ratio of the output signal voltage to the differential input signal voltage.

OPERATING TEMPERATURE RANGE
The temperature range, ambient unless otherwise indicated, over which the amplifier may be safely operated.

OUTPUT RESISTANCE
The open-loop output source resistance with respect to ground.

POWER SUPPLY RATED VOLTAGE
The normal value of power supply voltage at which the amplifier is designed to operate.

POWER SUPPLY VOLTAGE RANGE
The range of power supply voltage over which the amplifier may be safely operated.

QUIESCENT CURRENT
The current required from the power supply to operate the amplfiier with no load and with the output at zero.

RATED OUTPUT
The peak output voltage and current which can be continuously, simultaneously supplied.

SETTLING TIME
The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE
The maximum rate of charge of the output voltage when supplying rated output.

SPECIFICATION TEMPERATURE RANGE
The temperature range over which the "versus temperature" specifications are specified.

STORAGE TEMPERATURE RANGE
The temperature range over which the amplifier may be safely stored, unpowered.

UNITY-GAIN FREQUENCY RESPONSE
The frequency at which the open-loop becomes unity.

BURR-BROWN®

OPA11HT

Wide Temperature-Range General Purpose OPERATIONAL AMPLIFIER

FEATURES

- −55°C TO +175°C SPECIFICATIONS
- 30nA MAX, INPUT BIAS CURRENT AT +175°C
- ±6mV, MAX, INPUT OFFSET VOLTAGE AT +175°C
- ±5μV/°C TYP, INPUT OFFSET VOLTAGE COEFFICIENT
- 12MHz BANDWIDTH, TYPICAL
- HERMETIC PACKAGE WITH STANDARD PINOUT (741-TYPE)

DESCRIPTION

These specifications give you a versatile operational amplifier that will work in circuits that are subjected to extremely wide temperature ranges. Typical applications for OPA11HT include general purpose gain blocks, high-speed pulse amplifiers, audio amplifiers, high-frequency active filters, high-speed integrators, and photodiode amplifiers.

You're assured of this product's performance over the -55°C to +175°C range because we conduct 100% screening procedures in accordance with MIL-STD-883, method 5004, class B. Burn-in is performed at 200°C. Our sample and inspection procedures include both destructive and nondestructive bonding wire pull tests in accordance with Method 2011 of MIL-STD-883. The product is assembled in a clean-room environment.

Model OPA11HT is internally compensated for stability at all gains. Pins are available for special tailoring of the bandwidth compensation. Significant advantages in high gain, wide bandwidth, low-bias current, high output current and high common-mode rejection are provided by OPA11HT. Inputs are protected against common-mode voltages up to the value of the power supplies while the output is current limited to offer short circuited protection. TO-99 hermetic package has standard 741-type pinout arrangement.

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PDS-476

SPECIFICATIONS

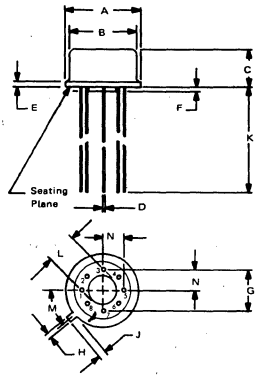
ELECTRICAL

Specifications at ±15VDC and T_A = +175°C unless otherwise noted.

MODEL		OPA11HT			
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
OPEN LOOP GAIN, DC, single-ended	A_V				
No load			103		dB
R_L= 2kΩ		94	100		dB
RATED OUTPUT					
Voltage, R_L= 2kΩ	V_{om}	±10	±12		V
Current (T_A = 25°C)	I_{om}	±15	±23		mA
DYNAMIC RESPONSE (T_A = 25°C)					
Small-Signal Bandwidth (0dB)			12		MHz
Full-Power Bandwidth, V_{OUT} = ±10V	BW_{fp}	50	75		kHz
Slew Rate, R_L = 2kΩ	SR	4	7		V/μsec
Settling Time (0.1%)			1.5		μsec
Rise Time (10% to 90%, small-signal)			30		nsec
INPUT OFFSET VOLTAGE	V_{io}				
Initial (without adj. at 25°C)			±1	±5	mV
Over Temperature					
T_A = +175°C				±6	mV
T_A = −55°C				±7	mV
Average V_{io} coefficient			±5		μV/°C
Average V_{io} coefficient vs supply voltage (T_A = 25°C)			±10	±200	μV/V
INPUT BIAS CURRENT	I_{ib}				
Initial at +25°C			±10	±25	nA
Over Temperature					
T_A = +175°C				±30	nA
T_A = −55°C				±40	nA
Average I_{ib} coefficient			±0.1		nA/°C
INPUT DIFFERENCE CURRENT	I_{io}				
Initial at +25°C			±10	±25	nA
Over Temperature					
T_A = +175°C				±30	nA
T_A = −55°C				±40	nA
Average I_{io} coefficient			±0.1		nA/°C
INPUT IMPEDANCE (T_A = 25°C)					
Differential	r_i	100	300		MΩ
	c_i		3		pF
Common Mode	r_i(CM)		1000		MΩ
	c_i(CM)		3		pF
INPUT VOLTAGE RANGE					
Common Mode				±11	V
Differential Mode				±12	V
Common-Mode Rejection	CMR	80	100		dB
Over Temperature (-55°C ≤ T_A ≤ +175°C)			100		dB
POWER SUPPLY (T_A = 25°C)					
Rated Voltage	V_{CC}			±15	V
Voltage Range, derated			±8 to ±22		V
Current, quiescent	I_q		±3	±3.7	mA
Over Temperature (-55°C ≤ T_A ≤ +175°C)			±3		mA
Power Supply Rejection Ratio (T_A = +175°C)	PS_{rr}	80	100		dB
TEMPERATURE RANGE					
Specification		−55°C ≤ T_A ≤ +175°C			
Operating		−55°C ≤ T_A ≤ +200°C			
Storage		−65°C ≤ T_A ≤ +250°C			

MECHANICAL

TO-99 PACKAGE

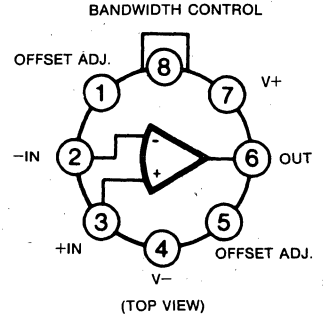


NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM



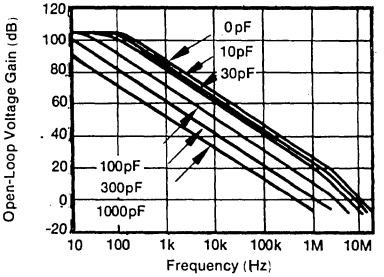
(TOP VIEW)

PIN 4 IS CONNECTED TO CASE

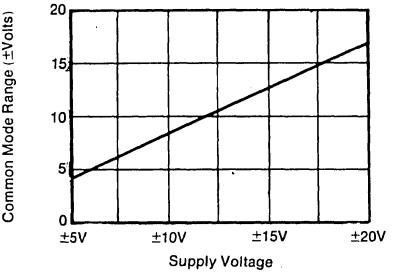
TYPICAL PERFORMANCE CURVES

(at ±15VDC and T_A = +25°C unless otherwise specified)

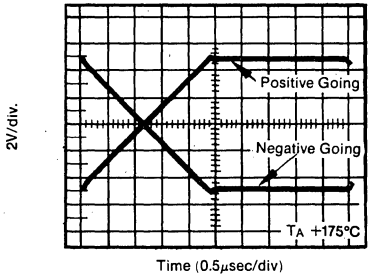
OPEN LOOP FREQUENCY RESPONSE[1]



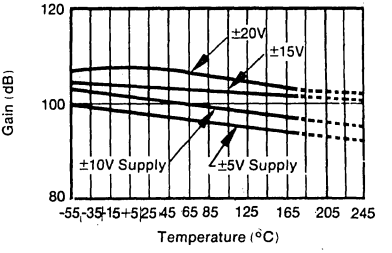
COMMON MODE VOLTAGE RANGE vs. SUPPLY VOLTAGE



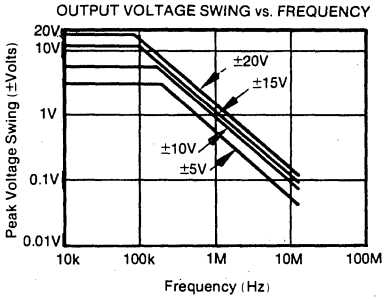
STEP RESPONSE IN FOLLOWER CONFIGURATION[2]



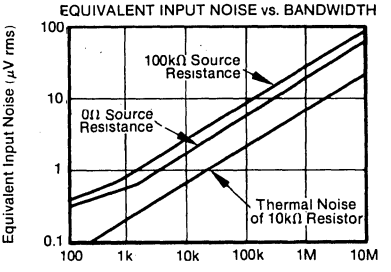
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



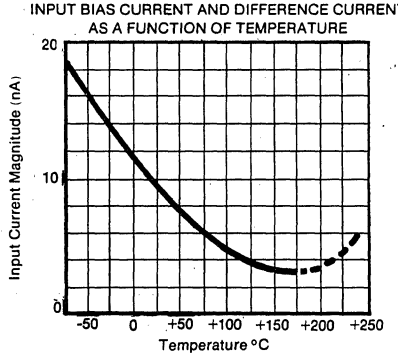
OUTPUT VOLTAGE SWING vs. FREQUENCY



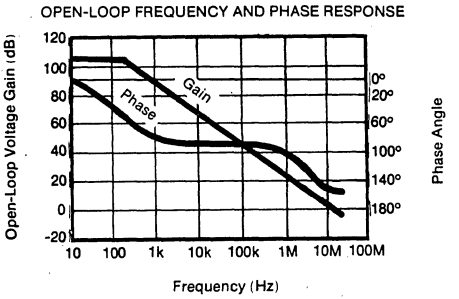
EQUIVALENT INPUT NOISE vs. BANDWIDTH



INPUT BIAS CURRENT AND DIFFERENCE CURRENT AS A FUNCTION OF TEMPERATURE



OPEN-LOOP FREQUENCY AND PHASE RESPONSE



1. Capacitance values shown are compensation from pin 8 to common. Not required for stability. See Figure 1. 2. See Figure 3.

APPLICATIONS

BANDWIDTH COMPENSATION

The frequency response of the OPA11HT can be adjusted by use of an external compensation capacitor from pin 8 to common as shown in Figure 1. The open-loop frequency response curves illustrate the effect of various values of capacitance. The OPA11HT is stable at any gain level without the use of compensation, provided that stray wiring capacitance and/or load capacitance are not excessive, and that moderate values of feedback resistance are used ($R_{FB} \leq 10k\Omega$). A load capacitance of ≈50pF is desirable in all feedback configurations.

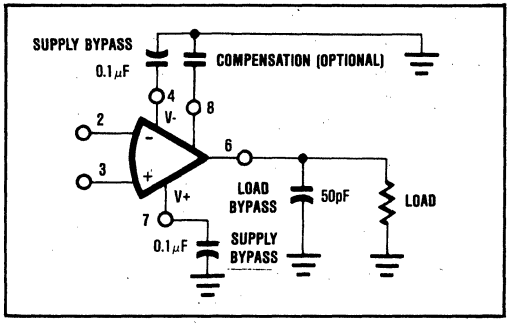


FIGURE 1. Compensated Amplifier with Supply Load Bypassing.

STABILITY

Because the OPA11HT is an extremely-fast amplifier with high gain, stray wiring capacitance and inductance in power supply leads can cause circuit oscillation. This can be prevented by proper circuit layout (all leads or patterns as short as possible) and by properly by passing the power supply lines to common at points close to the amplifier. In addition, it is recommended that the load be bypassed by a 50pF capacitor, see Figure 1.

OFFSET VOLTAGE AND ADJUSTMENT

Although the offset voltage of these amplifiers is only a few millivolts, it may in some cases be desirable to null this offset. This is done by use of a 100kΩ potentiometer as shown in Figure 2.

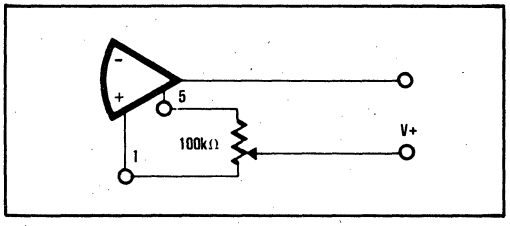


FIGURE 2. External Adjustment of Offset Voltage.

TEST CIRCUIT - DYNAMIC RESPONSE

The test circuit of Figure 3 is used for measurement of slew rate, settling time, rise time and overshoot. Both rise time and overshoot are measured for a small output signal (V_{OUT} = ±100mV). Slew rate and settling time are measured for a 10V, p-p, square wave.

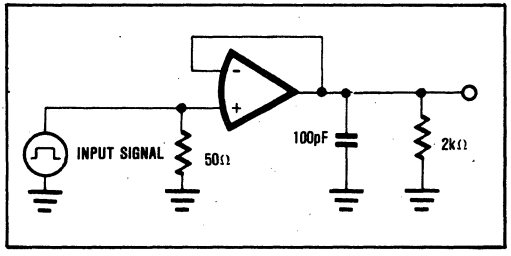


FIGURE 3. Dynamic Response Test Circuit.

VOLTAGE REGULATOR AT 200°C

In many applications, a regulated source of ±15V is needed. A voltage regulator that typically will operate up to +175°C is shown in Figure 4. This regulator accepts +16V to +30V at its input and provides +15V at 20mA at its output. A complementary version may be constructed to provide -15V by using the OPA11HT with a 2N1711 transistor. Short-circuit protection should be added if required.

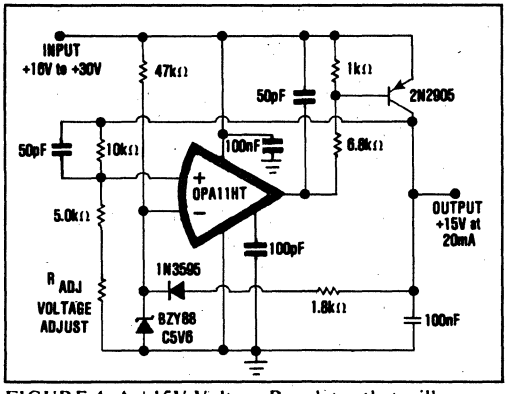


FIGURE 4. A +15V Voltage Regulator that will Operate at +175°C.

BURR-BROWN®

OPA21

Low-Power Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW SUPPLY CURRENT
  230μA max at $V_{CC} = \pm 15V$
- WIDE SUPPLY RANGE
  $\pm 2.5V$ to $\pm 18V$
- LOW OFFSET VOLTAGE
  100μV max
- LOW OFFSET VOLTAGE DRIFT
  1.0μV/°C max

APPLICATIONS

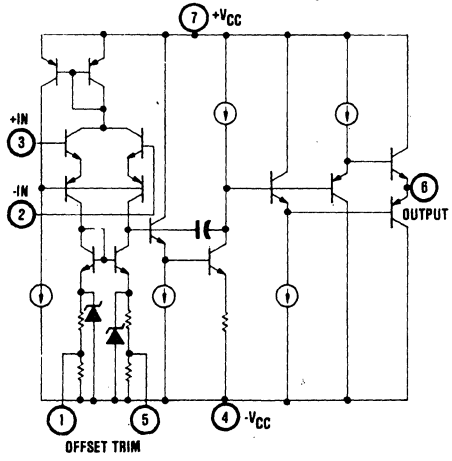
- PORTABLE EQUIPMENT
- BATERY OPERATION
- IMPROVED REPLACEMENT FOR OP-21

DESCRIPTION

A unique circuit design, state-of-the-art monolithic processing and advanced laser-trimming techniques are used to provide a low power amplifier with outstanding parameters—truly "instrumentation grade" performance over a wide voltage supply range.

The OPA21 consumes only 6.9mW of power at $V_{CC} = \pm 15V$ and 1.1mW at $V_{CC} = \pm 2.5V$ but offers far higher performance than MOS op-amps.

The OPA21 is internally compensated for unity-gain stability.



SIMPLIFIED CIRCUIT

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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 2.5VDC to 15VDC, unless otherwise noted.

PARAMETERS	CONDITIONS	OPA21E			OPA21G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT OFFSET VOLTAGE								
OFFSET VOLTAGE[1]			40	100		300	500	µV
	−25°C to +85°C		75	200		500	1000	µV
Drift	−25°C to +85°C		0.5	1.0		2.5	5.0	µV/°C
Offset Adjustment Range			±4			*		mV
INPUT OFFSET CURRENT								
Offset Current			0.3	1		1.2	4	nA
	−25°C to +85°C		0.5	2		2	6	nA
INPUT BIAS CURRENT								
Bias Current			7	25		15	50	nA
	−25°C to +85°C		9	40		18	75	nA
INPUT NOISE								
Voltage	0.1Hz to 10Hz		1.0			*		µV p-p
Voltage Density	f_o = 1Hz		60			*		$nV/\sqrt{Hz}$
	f_o = 10Hz		20			*		$nV/\sqrt{Hz}$
	f_o = 100Hz		20			*		$nV/\sqrt{Hz}$
Current Density	f_o = 1Hz		0.7			*		$pA/\sqrt{Hz}$
	f_o = 10Hz		0.25			*		$pA/\sqrt{Hz}$
	f_o = 100Hz		0.07			*		$pA/\sqrt{Hz}$
INPUT RESISTANCE								
Differential			6			4		MΩ
Common-Mode			$10^{10}\|\|2$			*		Ω||pF
INPUT VOLTAGE RANGE								
Input Voltage Range		−12.5			*			V
		+14.3			*			V
	−25°C to +85°C	−12.0			*			V
		+14.0			*			V
COMMON-MODE REJECTION RATIO								
CMRR	V_{CM} = −12V to +14V, R_L = 100kΩ	100	110		84	100		dB
	−25°C to +85°C	96	105		80	95		dB
POWER SUPPLY REJECTION RATIO								
PSRR	$\pm V_{CC}$ = 2.5V to 18V, R_L = 100kΩ	104	114		90	100		dB
	−25°C to +85°C	100	108		85	95		dB
LARGE SIGNAL VOLTAGE GAIN								
Open-Loop Voltage Gain	R_L = 10kΩ	1000	2000		500	1000		V/mV
		120	126		114	120		dB
	−25°C to +85°C	500	1500		250	1000		V/mV
		114	124		108	120		dB
RATED OUTPUT								
Output Voltage Swing	R_L = 10kΩ	−13.7	−14.2		−13.6	*		V
		+14.0	+14.1		+13.8	*		V
Output Current	R_L = 2kΩ		5			*		mA
	−25°C to +85°C, R_L = 10kΩ	−13.5			*			V
		+13.8			+13.6			V
Output Resistance	Open-Loop		500			*		Ω
DYNAMIC RESPONSE								
Slew Rate	C_L = 100pF, R_L = 25kΩ		0.2			*		V/µsec
Closed-Loop Bandwidth	A_{CL} = +1, R_L = 10kΩ		300			*		kHz
POWER SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range	Derated	±2.5		±18	*		*	VDC
Current Quiescent	I_o = 0MA							
	$\pm V_{CC}$ = 2.5V		170	210		*	250	µA
	$\pm V_{CC}$ = 15V		200	230		*	325	µA
	$\pm V_{CC}$ = 2.5V, −25°C to +85°C		210	275		*	325	µA
	$\pm V_{CC}$ = 15V, −25°C to +85°C		230	325		*	375	µA
TEMPERATURE RANGE								
Specification	Ambient	−25		+85	*		*	°C
Operating	Ambient	−55		+125	*		*	°C

NOTE: (1) Guaranteed fully warmed-up.

*Specification same as OPA21E.

ABSOLUTE MAXIMUM RATINGS

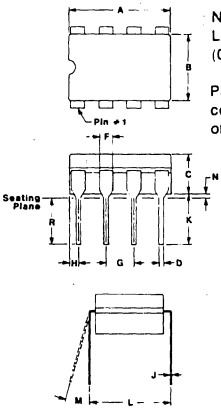
Supply Voltage	±18V
Internal Power Dissipation[1]	500mW
Input Voltage	Supply Voltage
Differential Input Voltage	±30V
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature Range (soldering, 60sec)	+300°C

NOTE: (1) Maximum package power dissipation vs ambient temperature:

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
8-Pin Hermetic DIP (Z)	+75°C	6.7mW/°C

MECHANICAL

8-PIN HERMETIC DIP
("Z" SUFFIX)



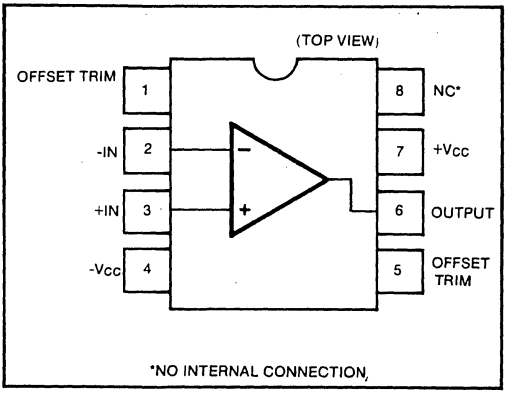
NOTE:
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

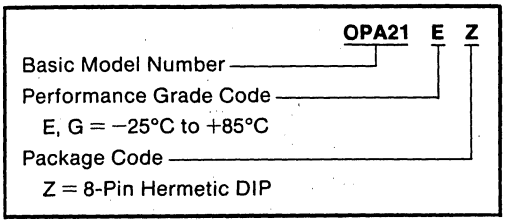
Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.375	.405	9.53	10.28
B	.245	.261	6.22	6.38
C	.140	.170	3.56	4.32
D	.016	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	–	.099	–	2.40
J	.008	.012	0.20	0.30
K	.150	–	3.80	–
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

PIN CONFIGURATION

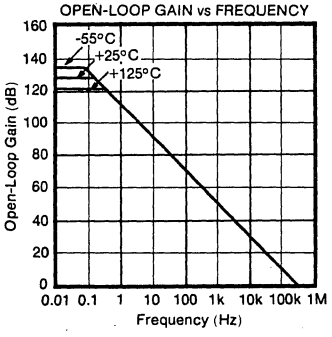


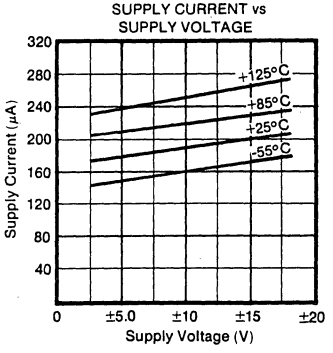
ORDERING INFORMATION

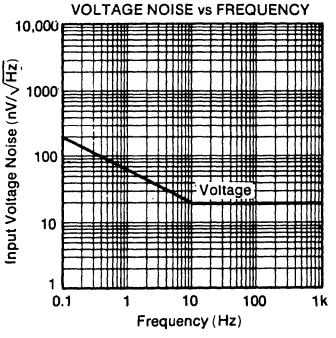


TYPICAL PERFORMANCE CURVES

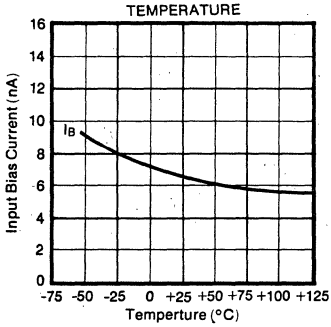
(T_A = +25°C, ±V_{CC} = 15VDC unless otherwise noted)



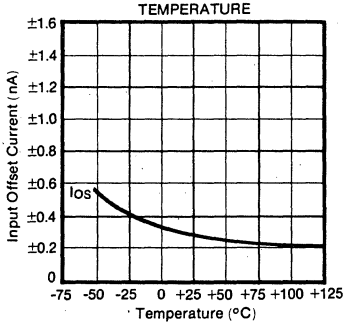




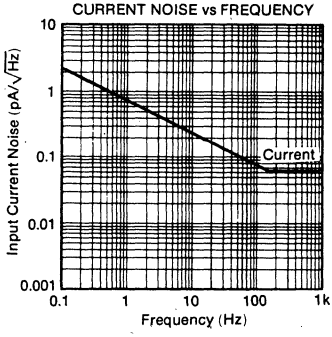
INPUT BIAS CURRENT vs TEMPERATURE



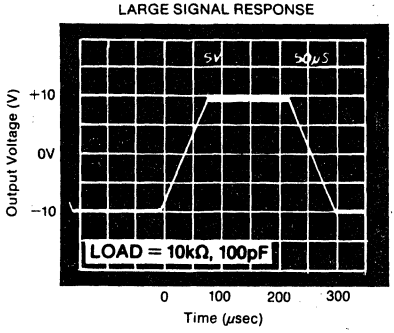
INPUT OFFSET CURRENT vs TEMPERATURE



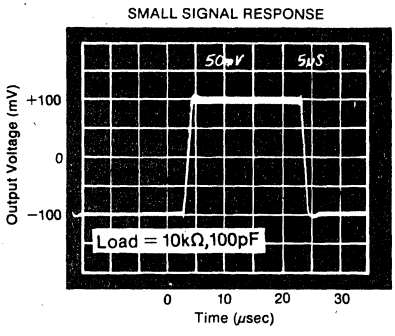
CURRENT NOISE vs FREQUENCY



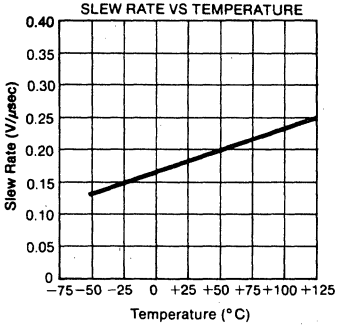
LARGE SIGNAL RESPONSE



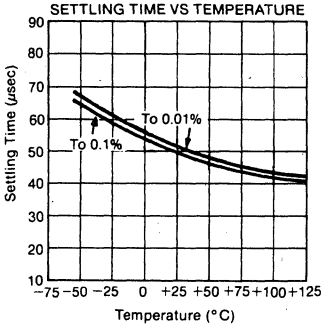
SMALL SIGNAL RESPONSE



SLEW RATE VS TEMPERATURE



SETTLING TIME VS TEMPERATURE



BURR-BROWN®

OPA27
OPA37

Ultra-Low Noise Precision OPERATIONAL AMPLIFIERS

FEATURES

- LOW NOISE: 100% tested, 3.8nV/$\sqrt{Hz}$ max at 1kHz
- LOW OFFSET: 25μV max
- LOW DRIFT: 0.6μV/°C max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 114dB min
- HIGH POWER SUPPLY REJECTION: 100dB min
- FITS OP-07, OP-05, AD510, AD517 SOCKETS

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- TRANSDUCER AMPLIFIER
- RADIATION HARD EQUIPMENT

DESCRIPTION

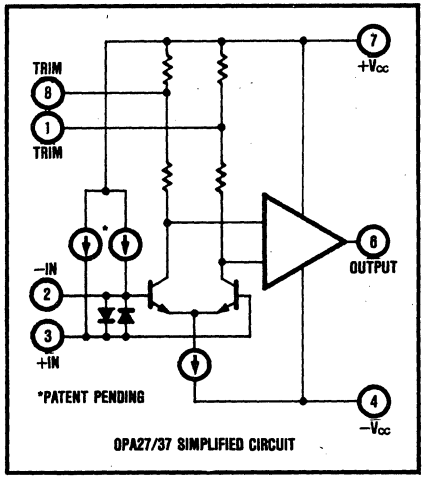
The OPA27/37 is an ultra-low noise, high precision monolithic operational amplifier.

Laser-trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset compared to common zener-zap techniques.

A unique bias current cancellation circuit (patent pending) allows bias and offset current specifications to be met over the full −55°C to +125°C temperature range.

The OPA27 is internally compensated for unity-gain stability. The decompensated OPA37 requires a closed-loop gain ≥ 5.

The Burr-Brown OPA27/37 is an improved replacement for the industry-standard OP-27/OP-37.



OPA27/37 SIMPLIFIED CIRCUIT

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = P15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
NOISE											
Voltage, f_O = 10Hz	100% tested, (A, E)		3.1	5.5		3.5	5.5		3.8	8.0	nV/√Hz
f_O = 30Hz	100% tested, (A, E)		2.9	4.5		3.1	4.5		3.3	5.6	nV/√Hz
f_O = 1kHz	100% tested, (A, E)		2.7	3.8		3.0	3.8		3.2	4.5	nV/√Hz
f_B = 0.1Hz to 10Hz			0.07	0.18		0.08	0.18		0.09	0.25	µV, p-p
Current,[1] f_O = 10Hz	100% tested, (A, E)		1.7	4.0		1.7	4.0		1.7		pA/√Hz
f_O = 30Hz	100% tested, (A, E)		1.0	2.3		1.0	2.3		1.0		pA/√Hz
f_O = 1kHz	100% tested, (A, E)		0.4	0.6		0.4	0.6		0.4	0.6	pA/√Hz
OFFSET VOLTAGE[2]											
Input Offset Voltage			±6	±25		±12	±60		±25	±100	µV
Average Drift[3]	$T_{A\ MIN}$ to $T_{A\ MAX}$		±0.2	±0.6		±0.3	±1.3		±0.4	±1.8	µV/°C
Long Term Stability[4]			0.2	1		0.3	1.5		0.4	2.0	µV/mo
Supply Rejection	±V_{CC} = 4 to 18V	100	134		100	125		94	120		dB
	±V_{CC} = 4 to 18V		±0.2	±10		±0.6	±10		±1	±20	µV/V
BIAS CURRENT											
Input Bias Current			±11	±40		±13	±55		±15	±80	nA
OFFSET CURRENT											
Input Offset Current			6	35		8	50		10	75	nA
IMPEDANCE											
Common-Mode			3			2.5			2		GΩ
VOLTAGE RANGE											
Common-Mode Input Range		±11	±12.3		±11	±12.3		±11	±12.3		V
Common-Mode Rejection	V_{IN} = ±11VDC	114	128		106	125		100	122		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	120	126		120	125		117	124		dB
	$R_L \geq 1k\Omega$	118	125		118	125			124		dB
FREQUENCY RESPONSE											
Gain-Bandwidth Product[5]	OPA27	5	8		5	8		5	8		MHz
	OPA37	45	63		45	63		45	63		MHz
Slew Rate[5]	V_o = ±10V, R_L = 2kΩ										
	OPA27, G = +1	1.7	1.9		1.7	1.9		1.7	1.9		V/µsec
	OPA37, G = +5	11	11.9		11	11.9		11	11.9		V/µsec
Settling Time, 0.01%	OPA27, G = +1		25			25			25		µsec
	OPA37, G = +5		25			25			25		µsec
RATED OUTPUT											
Voltage Output	$R_L \geq 2k\Omega$	±12	±13.8		±12	±13.8		±12	±13.8		V
	$R_L \geq 600\Omega$	±10	±12.8		±10	±12.8		±10	±12.8		V
Output Resistance	DC, open loop		70			70			70		Ω
Short Circuit Current	R_L = 0Ω		25	60		25	60		25	60	mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±4		±22	±4		±22	±4		±22	VDC
Current, Quiescent	I_O = 0mADC		3	4.7		3	4.7		3.3	5.7	mA
TEMPERATURE RANGE											
Specification											
A, B, C (J, Z)		−55		+125	−55		+125	−55		+125	°C
E, F, G (J, Z)		−25		+85	−25		+85	−25		+85	°C
G (P)							0			+70	°C
Operating: J, Z		−55		+125	−55		+125	−55		+125	°C
P								−25		+85	°C

NOTES: (1) Measured with industry-standard noise test circuit (Figures 1 and 2). Due to errors introduced by this method, these current noise specifications should be used for comparison purposes only. (2) Offset voltage specifications on grades A and E are also guaranteed with units fully warmed up. Grades B, C, F, and G are measured with automatic test equipment after approximately 0.5 second from power turn-on. (3) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (4) Long-term voltage offset vs time trend line does not include warm-up drift. (5) Typical specification only on plastic package units. Slew rate varies on all units due to differing test methods. Minimum specification applies to open-loop test.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range											
A, B, C (J, Z)		−55		+125	−55		+125	−55		+125	°C
E, F, G (J, Z)		−25		+85	−25		+85	−25		+85	°C
G (P)								0		+70	°C
INPUT											
OFFSET VOLTAGE[1]											
Input Offset Voltage											
A, B, C			±24	±60		±45	±200		±60	±300	µV
E, F, G			±17	±50		±33	±140		±48	±220	µV
Average Drift[2]	$T_{A\ MIN}$ to $T_{A\ MAX}$		±0.2	±0.6		±0.3	±1.3		±0.4	±1.8	µV/°C
Supply Rejection											
A, B, C	±V_{CC} = 4.5 to 18V	96	130		94	127		86	122		dB
E, F, G	±V_{CC} = 4.5 to 18V	97	130		96	127		90	122		dB
BIAS CURRENT											
Input Bias Current											
A, B, C			±16	±60		±22	±95		±29	±150	nA
E, F, G			±13	±60		±16	±95		±21	±150	nA
OFFSET CURRENT											
Input Offset Current											
A, B, C			23	50		25	85		35	135	nA
E, F, G			12	50		14	85		20	135	nA
VOLTAGE RANGE											
Common-Mode Input Range											
A, B, C		±10.3	±11.5		±10.3	±11.5		±10.3	±11.5		V
E, F, G		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8		V
Common-Mode Rejection	V_{IN} = ±11VDC										
A, B, C		108	124		100	122		94	120		dB
E, F, G		110	126		102	124		96	122		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$										
A, B, C		116	121		114	120		110	118		dB
E, F, G		118	123		117	122		113	120		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ										
A, B, C		±11.5	±13.7		±11.0	±13.5		±10.5	±13.3		V
E, F, G		±11.7	±13.8		±11.4	±13.6		±11.0	±13.4		V
Short Circuit Current	V_O = 0VDC		25			25			25		mA

NOTES: (1) Offset voltage specifications on grades A and E are also guaranteed with the units fully warmed up. Grades B, C, F, and G are measured with automatic equipment after approximately 0.5 second. (2) Unnulled or nulled with 8kΩ to 20kΩ potentiometer.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation[1] 500mW
Input Voltage[2] ..... ±22V
Output Short Circuit Duration[3] ..... Indefinite
Differential Input Voltage[4] ..... ±0.7V
Differential Input Current[4] ..... ±25mA
Storage Temperature Range:
J, Z ..... −65°C to +150°C
P ..... −55°C to +125°C
Operating Temperature Range:
A, B, C, E, F, G (J, Z) ..... −55°C to +125°C
G (P) ..... −25°C to +85°C
Lead Temperature Range (Soldering, 60sec) ..... +300°C

NOTES:

1. Maximum package power dissipation vs ambient temperature:

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C

2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. To common with ±V_{CC} = 15V.
4. The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

ORDERING INFORMATION

OPAXX Y Z

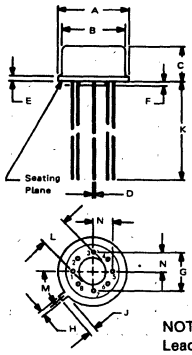
Basic Model Number

Performance Grade Code:
- A, B, C = −55°C to +125°C
- E, F, G = −25°C to +85°C
- GP = 0°C to +70°C

Package Code:
- J = TO-99
- Z = 8-Pin Hermetic DIP
- P = 8-Pin Plastic DIP

MECHANICAL

"J" PACKAGE, TO-99



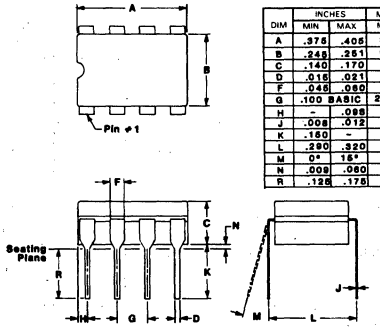
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE:
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD—883 (except paragraph 3.2).

"Z" PACKAGE, 8-PIN HERMETIC



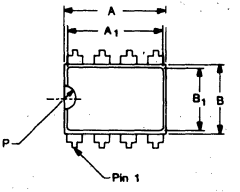
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.375	.405	9.53	10.28
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	–	.098	–	2.49
J	.008	.012	0.20	0.30
K	.150	–	3.80	–
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

NOTE:
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

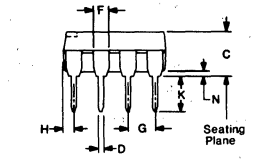
Pin numbers shown for reference only. Numbers may not be marked on package.

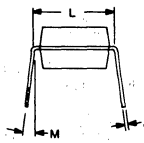
Pin material and plating composition conform to method 2003 (solderability) of MIL-STD—883 (except paragraph 3.2).

"P" PACKAGE, 8-PIN PLASTIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.355	.400	9.03	10.16
A_1	.340	.385	8.65	9.80
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27



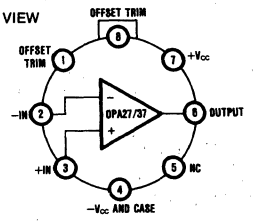


NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

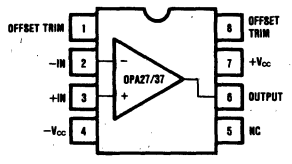
Pin numbers shown for reference only. Numbers may not be marked on package.

CONNECTION DIAGRAMS

TOP VIEW



TOP VIEW



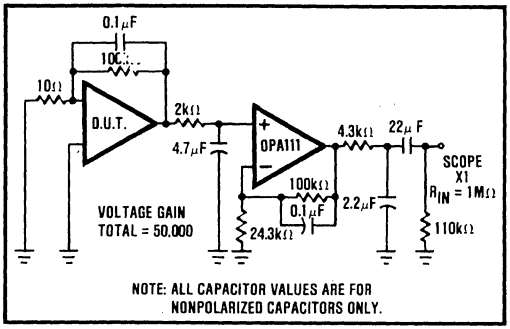


FIGURE 1. 0.1Hz to 10Hz Noise Test Circuit.

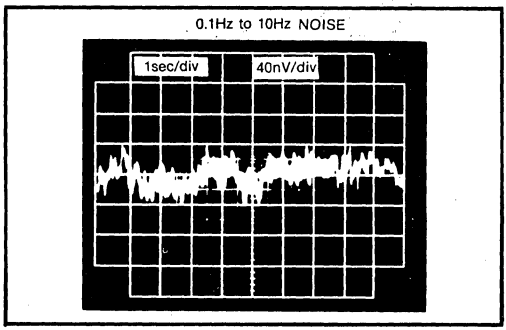
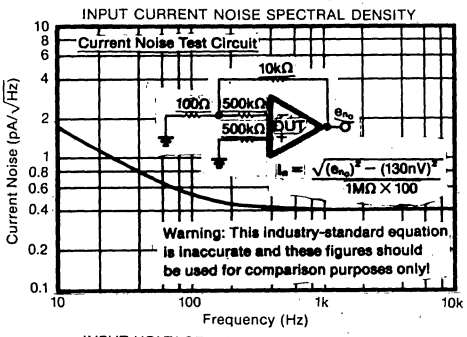
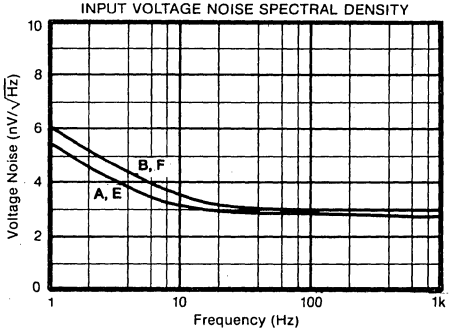


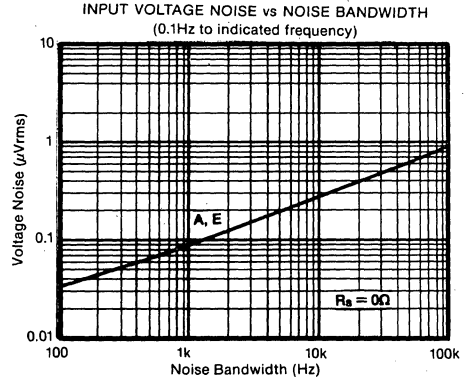
FIGURE 2. Low Frequency Noise.

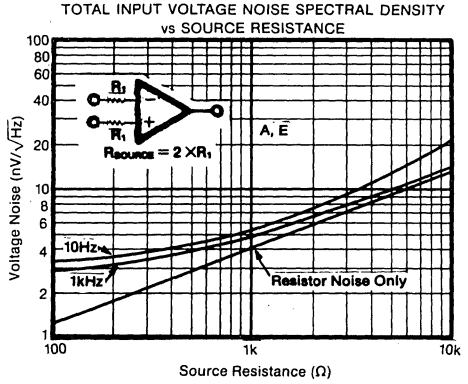
TYPICAL PERFORMANCE CURVES

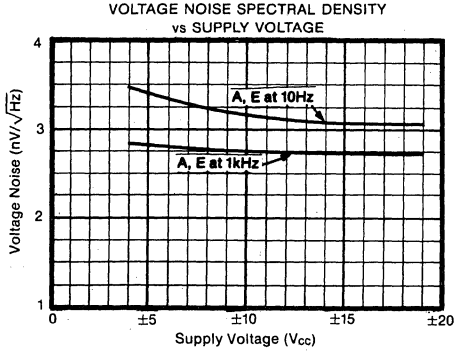
T_A = +25°C, $\pm V_{CC}$ = ±15VDC unless otherwise noted.

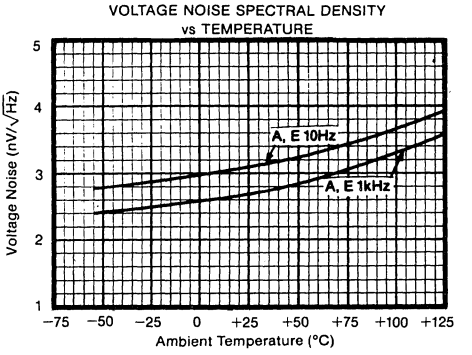








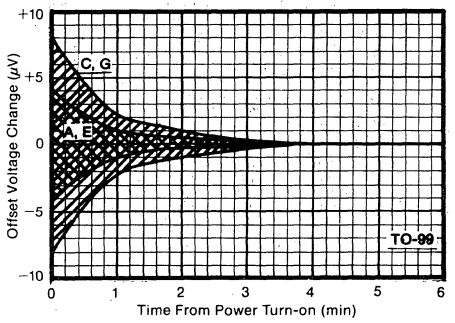




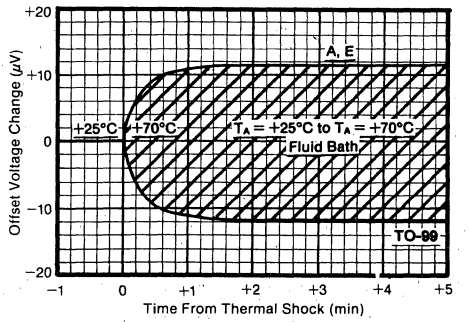
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, $\pm V_{CC}$ = ±15VDC unless otherwise noted.

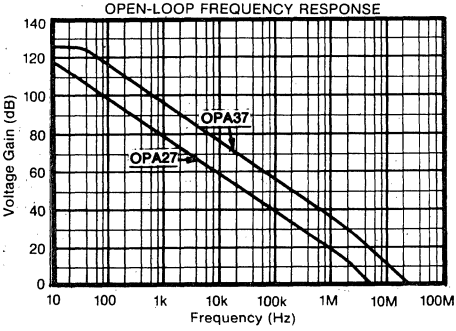
INPUT OFFSET VOLTAGE WARM-UP DRIFT



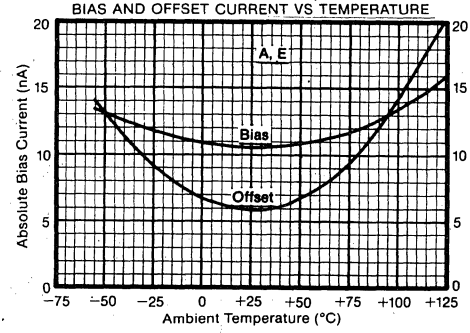
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



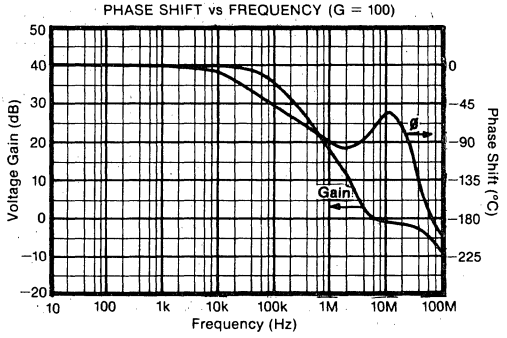
OPEN-LOOP FREQUENCY RESPONSE



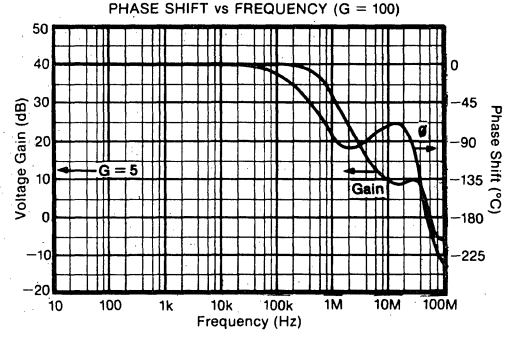
BIAS AND OFFSET CURRENT VS TEMPERATURE



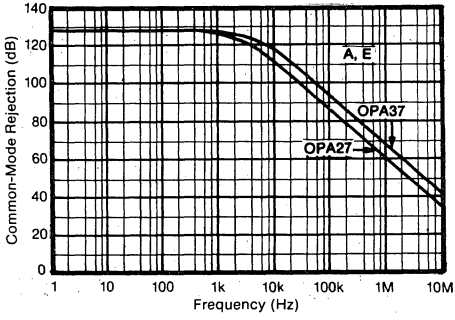
OPA27 CLOSED-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY (G = 100)



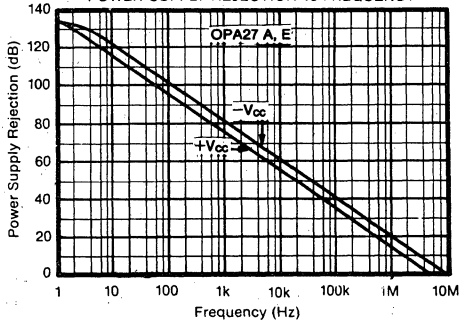
OPA37 CLOSED-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY (G = 100)



COMMON-MODE REJECTION vs FREQUENCY



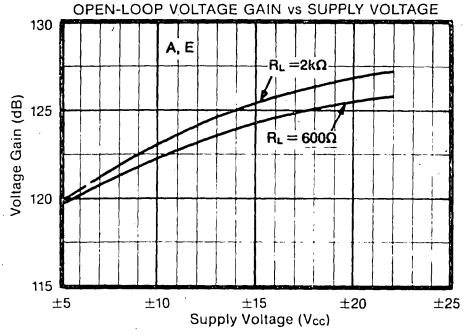
POWER SUPPLY REJECTION vs FREQUENCY



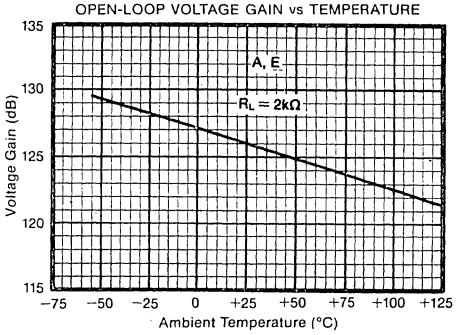
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, $\pm V_{CC}$ = ±15VDC unless otherwise noted.

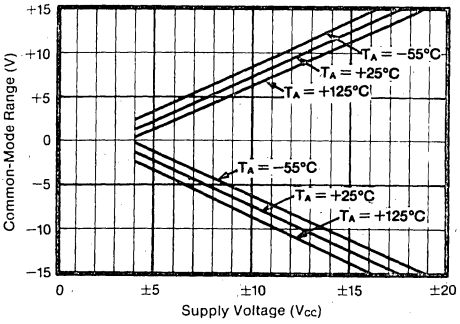
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



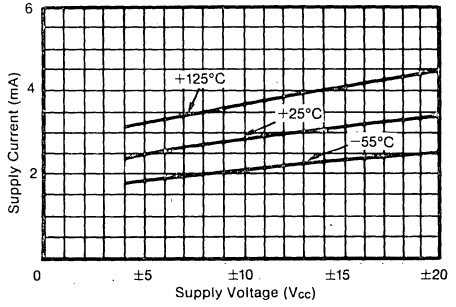
OPEN-LOOP VOLTAGE GAIN vs TEMPERATURE



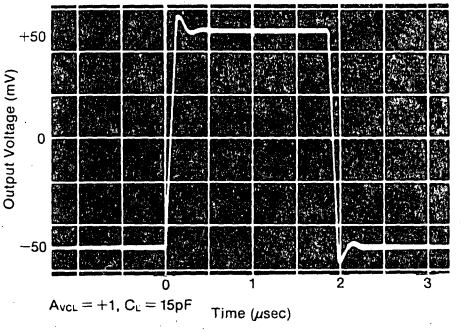
COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



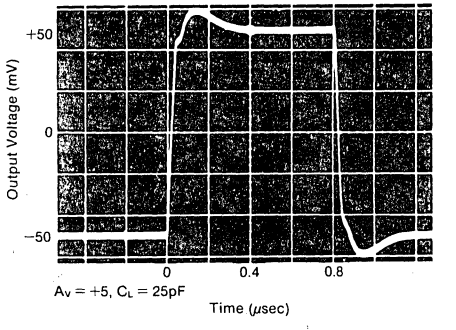
SUPPLY CURRENT vs SUPPLY VOLTAGE



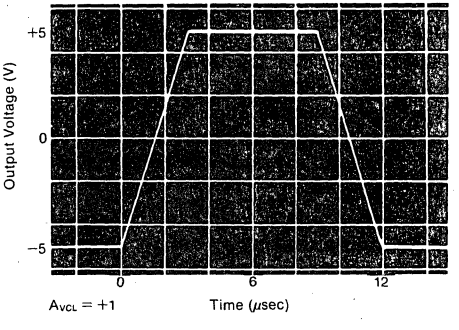
OPA27 SMALL SIGNAL TRANSIENT RESPONSE



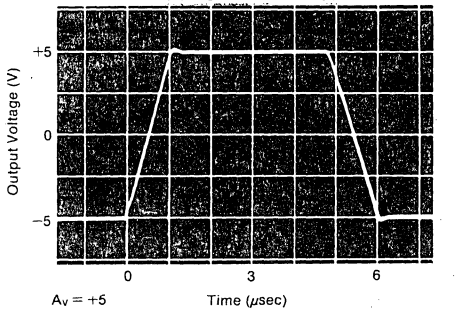
OPA37 SMALL SIGNAL TRANSIENT RESPONSE



OPA27 LARGE SIGNAL TRANSIENT RESPONSE



OPA37 LARGE SIGNAL TRANSIENT RESPONSE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA27/37 offset voltage is laser-trimmed and will require no further trim for most applications. Offset voltage drift will not be degraded when the input offset is nulled with a 10kΩ trim potentiometer. Other potentiometer values from 1kΩ to 1MΩ can be used but V_{OS} drift will be degraded by an additional 0.1 to 0.2μV/°C.

Nulling large system offsets by use of the offset trim adjust will degrade drift performance by approximately 0.3μV/°C per millivolt of offset. Large system offsets can be nulled without drift degradation by input summing.

The conventional offset voltage trim circuit is shown in Figure 3. For trimming very-small offsets, the higher resolution circuit shown in Figure 4 is recommended.

The OPA27/37 can replace 741-type operational amplifiers by removing or modifying the trim circuit.

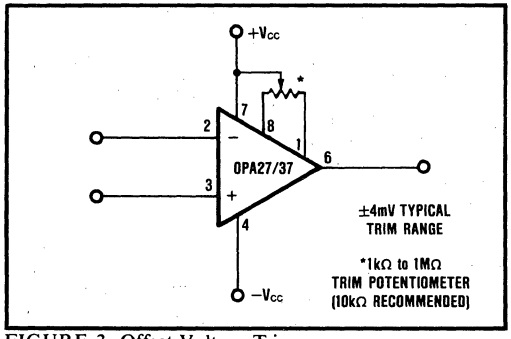


FIGURE 3. Offset Voltage Trim.

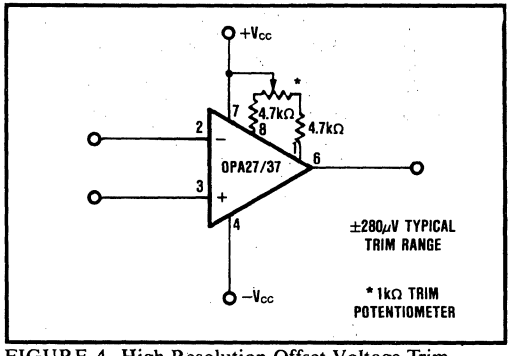


FIGURE 4. High Resolution Offset Voltage Trim.

THERMOELECTRIC POTENTIALS

The OPA27/37 is laser-trimmed to microvolt-level input offset voltage and for very-low input offset voltage drift.

Careful layout and circuit design techniques are necessary to prevent offset and drift errors from external thermoelectric potentials. Dissimilar metal junctions can generate small EMF's if care is not taken to eliminate either their sources (lead-to-PC, wiring, etc.) or their temperature difference. See Figure 7.

Short, direct mounting of the OPA27/37 with close spacing of the input pins is highly recommended. Poor layout can result in circuit drifts and offsets which are an order of magnitude greater than the operational amplifier alone.

NOISE: BIPOLAR VERSUS FET

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the Burr-Brown OPA111 low-noise FET operational amplifier is recommended for lower total noise than the OPA27 (see Figure 5).

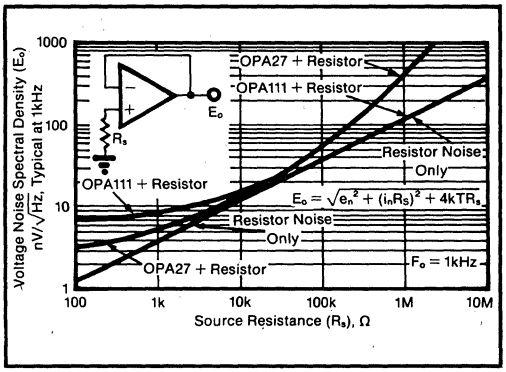


FIGURE 5. Voltage Noise Spectral Density Versus Source Resistance.

COMPENSATION

Although internally compensated for unity-gain stability, the OPA27 may require a small capacitor in parallel with a feedback resistor (R_f) which is greater than 2kΩ. This capacitor will compensate the pole generated by R_f and C_{IN} and eliminate peaking or oscillation.

INPUT PROTECTION

Back-to-back diodes are used for input protection on the OPA27/37. Exceeding a few hundred millivolts differential input signal will cause current to flow and without external current limiting resistors the input will be destroyed.

Accidental static discharge as well as high current can damage the amplifier's input circuit. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may be permanently damaged if any precision operational amplifier is subjected to abuse.

Transient conditions can cause feedthrough due to the amplifier's finite slew-rate. When using the OP-27 as a unity-gain buffer (follower) a feedback resistor of 1kΩ is recommended (see Figure 6).

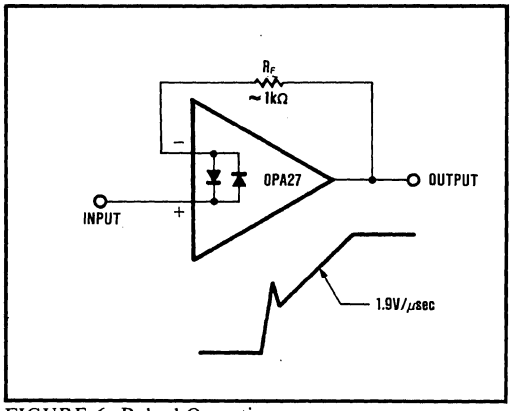


FIGURE 6. Pulsed Operation.

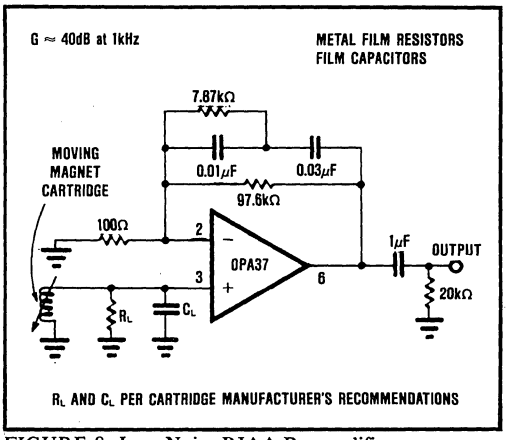


FIGURE 8. Low-Noise RIAA Preamplifier.

APPLICATIONS CIRCUITS

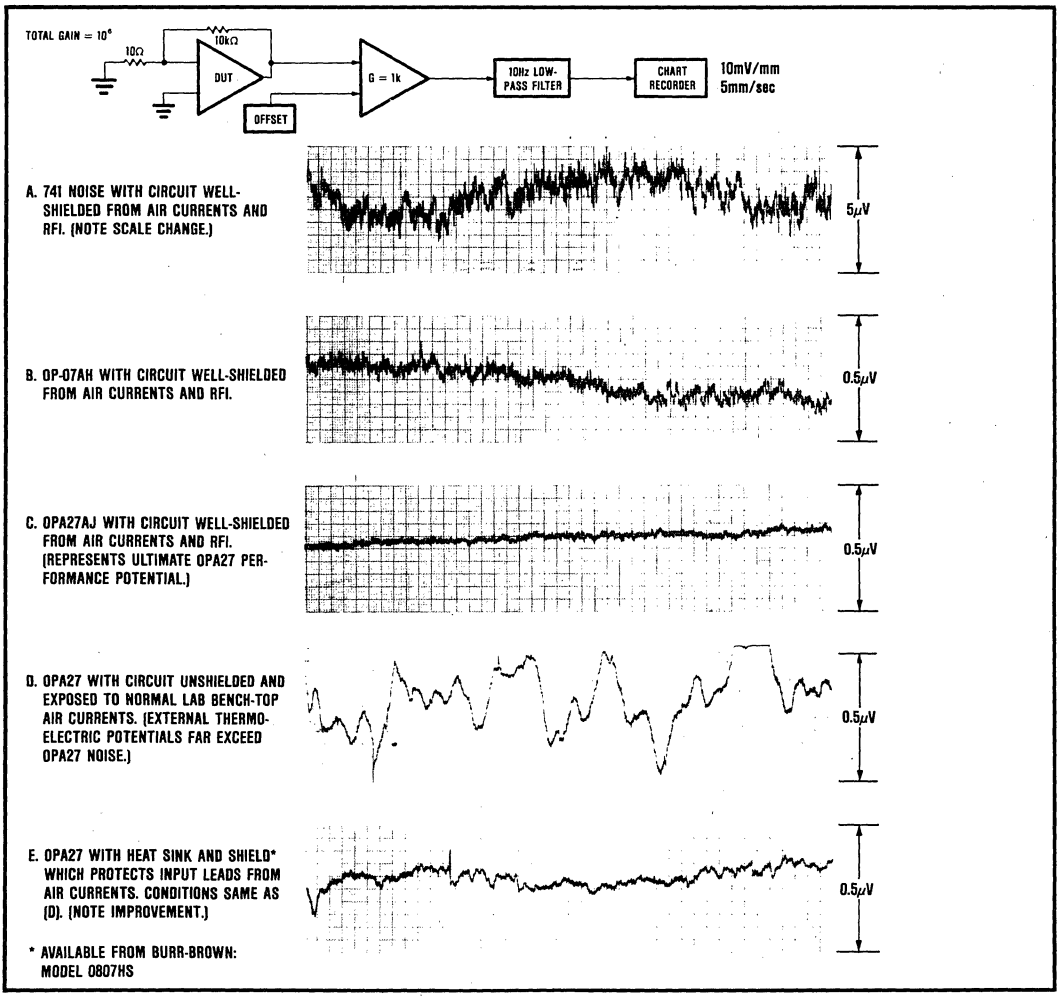


FIGURE 7. Low Frequency Noise Comparison.

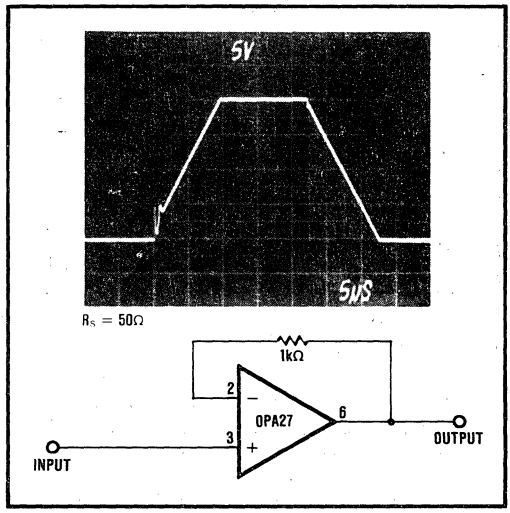


FIGURE 9. Unity-Gain Buffer.

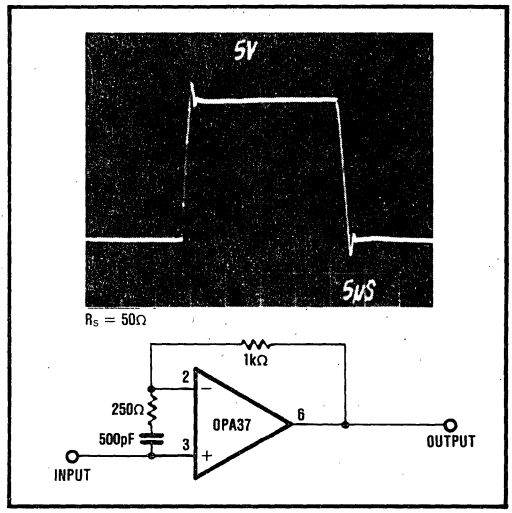


FIGURE 10. High Slew Rate Unity-Gain Buffer.

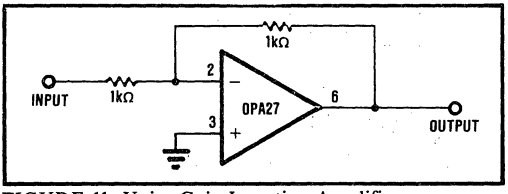


FIGURE 11. Unity-Gain Inverting Amplifier.

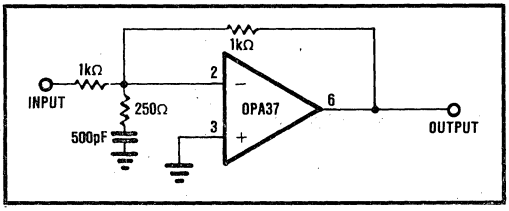


FIGURE 12. High Slew Rate Unity-Gain Inverting Amplifier.

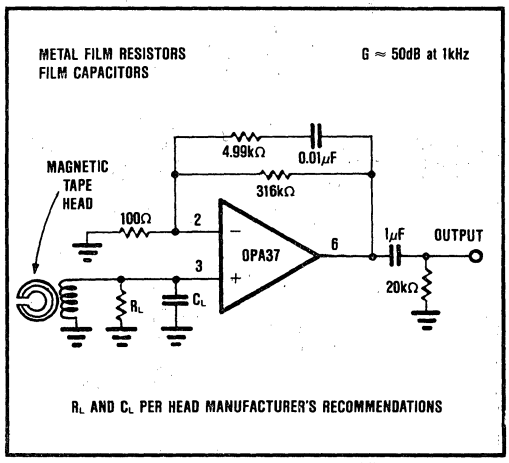


FIGURE 13. NAB Tape Head Preamplifier.

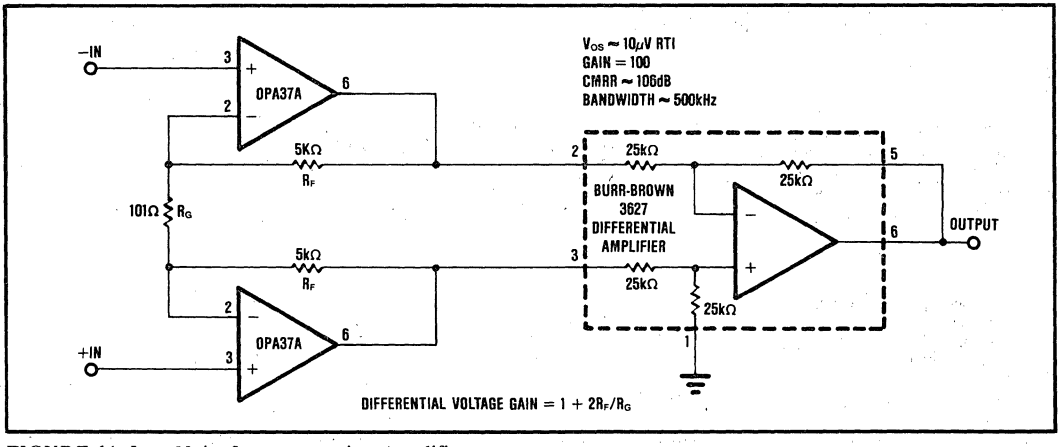


FIGURE 14. Low Noise Instrumentation Amplifier.

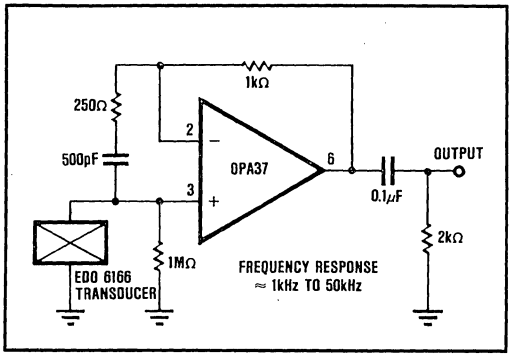


FIGURE 15. Hydrophone Preamplifier.

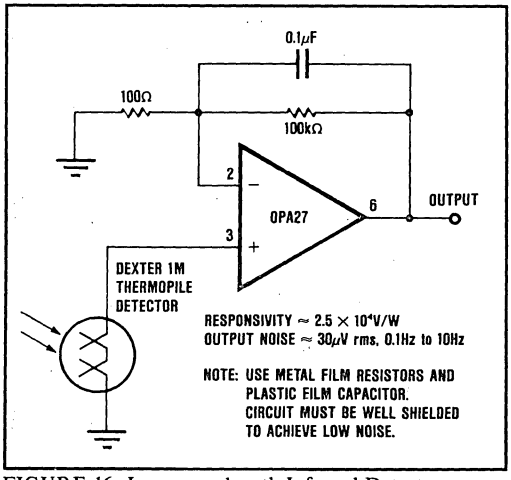


FIGURE 16. Long-wavelength Infrared Detector Amplifier.

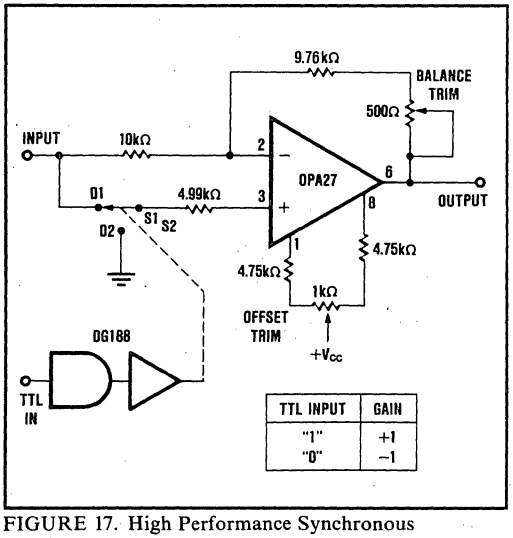


FIGURE 17. High Performance Synchronous Demodulator.

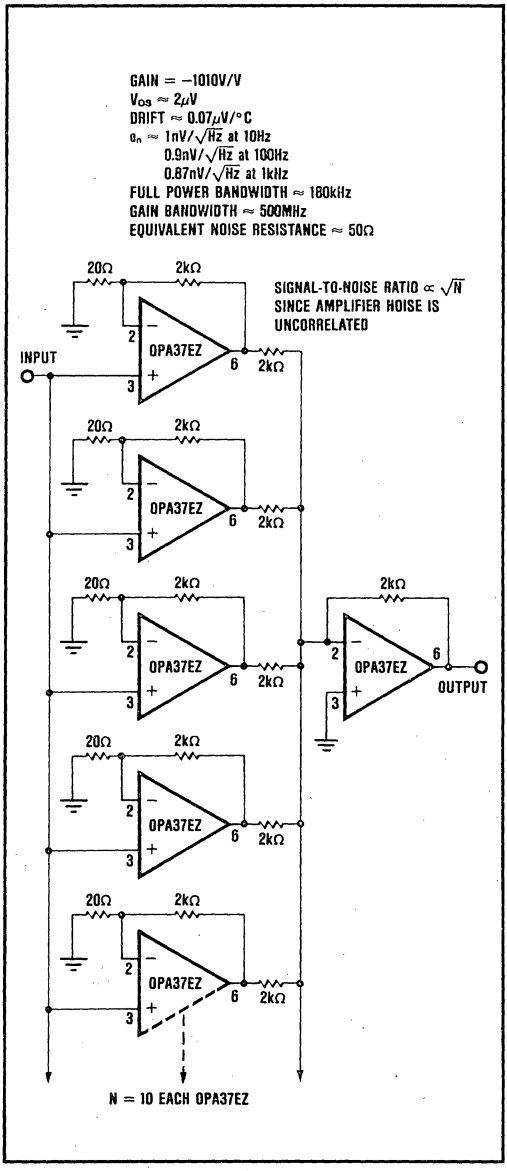


FIGURE 18. Ultra-low Noise "N" Stage Parallel Amplifier.

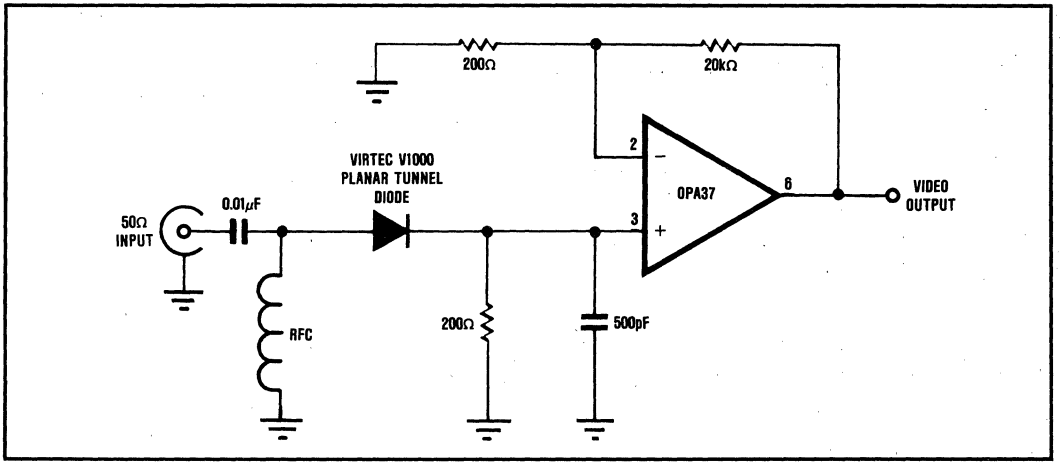


FIGURE 19. RF Detector and Video Amplifier.

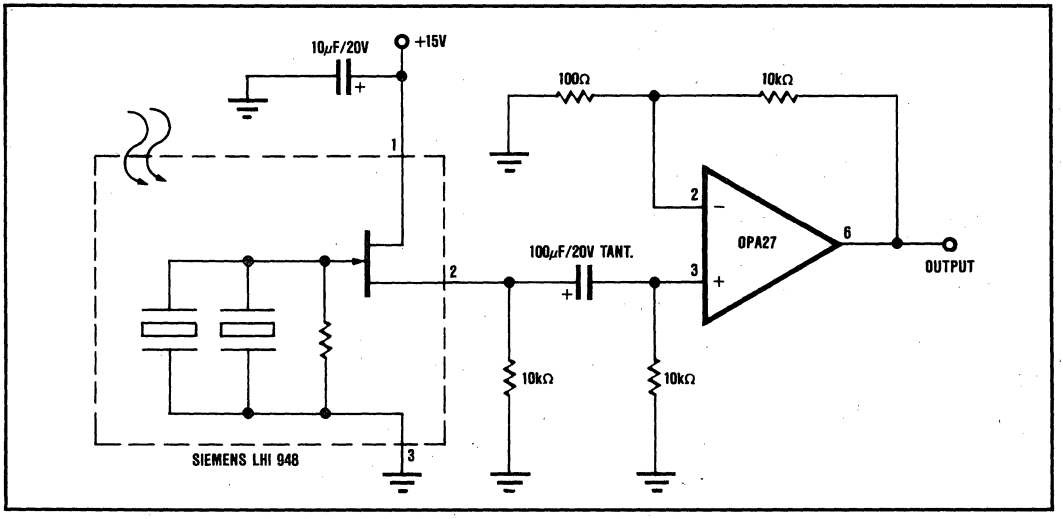


FIGURE 20. Balanced Pyroelectric Infrared Detector.

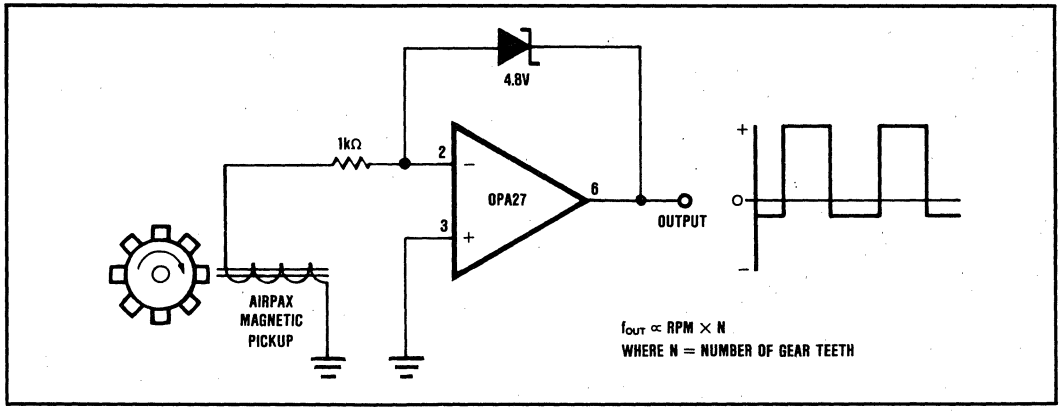


FIGURE 21. Magnetic Tachometer.

BURR-BROWN®

OPA27HT
OPA37HT

Wide Temperature Range Precision OPERATIONAL AMPLIFIERS

FEATURES

- FULLY SPECIFIED OVER −55°C to +200°C
- LOW OFFSET: ±400μV max at +200°C
- LOW DRIFT: ±0.4μV/°C
- ULTRA-LOW NOISE
- MONOLITHIC
- HERMETIC TO-99 PACKAGE
- 100% BURN-IN AT +200°C

APPLICATIONS

- DOWN-HOLE INSTRUMENTATION
- WELL LOGGING
- ENGINE CONTROLS
- EXTREMELY SEVERE ENVIRONMENT
- TRANSDUCER AMPLIFIER
- RADIATION HARD EQUIPMENT

DESCRIPTION

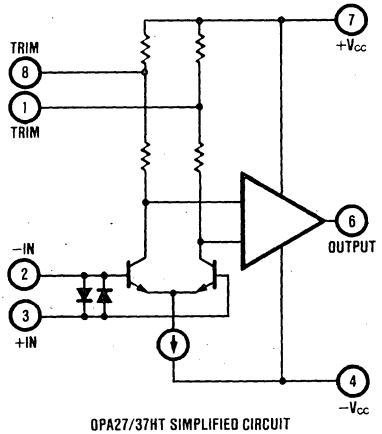
The OPA27/37HT is an ultra-low noise, high precision monolithic operational amplifier.

Laser trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset and drift performance.

The OPA27/37HT are tested and guaranteed over an extremely wide temperature range: −55°C to +200°C. In addition, they have demonstrated an ability to withstand a total dose of 2×10^6 RAD (Si) gamma and a neutron fluence of 1×10^{13}, 1MEV equivalent n/cm^2.

The OPA27HT is internally compensated for unity-gain stability. The decompensated OPA37HT requires a closed-loop gain ≥ 5.

The Burr-Brown OPA27/37HT use an industry-standard OP27/37 pinout and they can replace many existing amplifiers in low-source-impedance applications.



OPA27/37HT SIMPLIFIED CIRCUIT

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = 15VDC, T_A = indicated temperature.

PARAMETER	CONDITIONS	+25°C MIN	+25°C TYP	+25°C MAX	−55°C TO +125°C MIN	−55°C TO +125°C TYP	−55°C TO +125°C MAX	+200°C MIN	+200°C TYP	+200°C MAX	UNITS
INPUT											
NOISE											
Voltage, f_O = 10Hz	(1)		3.1			8.5			5.6		nV/√Hz
f_O = 30Hz	(1)		2.9			4.0			4.5		nV/√Hz
f_O = 1kHz	(1)		2.7			3.6			4.0		nV/√Hz
f_B = 0.1Hz to 10Hz			0.07								μV, p-p
Current, f_O = 1kHz			0.4			0.5			0.8		pA/√Hz
OFFSET VOLTAGE[2]											
Input Offset Voltage			±25	±75		±37	±200		±150	±400	μV
Average Drift[3]	$T_{A\ MIN}$ to $T_{A\ MAX}$								±0.4		μV/°C
Long Term Stability[4]	T_A = +125°C		8								μV/kHrs
Supply Rejection[7]	$\pm V_{CC}$ = 4V to 18V	100	134		94	127		94	127		dB
	$\pm V_{CC}$ = 4V to 18V		±0.2	±10		±0.45	±20		±0.45	±20	μV/V
BIAS CURRENT											
Input Bias Current			430	1μA		600	2μA		3.4μA	5μA	nA
OFFSET CURRENT											
Input Offset Current			±40	±180		±50	±200		±300	±550	nA
IMPEDANCE											
Common-Mode			3								GΩ
VOLTAGE RANGE											
Common-Mode Input Range		±11	±12.3		±10.3	±11.5		±9.0	±11.0		V
Common-Mode Rejection	V_{IN} = ±10VDC[5]	106	128		100	122		96	119		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	120	126		±109	120		104	113		dB
	$R_L \geq 1k\Omega$	±116	125								dB
FREQUENCY RESPONSE											
Gain-Bandwidth Product	OPA27HT		6			7			6		MHz
A_V = 1000V/V	OPA37HT		36			38			41		MHz
Slew Rate	V_O = ±10V, R_L = 2kΩ										
	OPA27HT, G = +1		1.9			1.7			3.5		V/μs
	OPA37HT, G = +5		11.9			10			16		V/μs
Settling Time, 0.01%	OPA27HT, G = +1		25								μs
	OPA37HT, G = +5		25								μs
RATED OUTPUT											
Voltage Output	$R_L \geq 2k\Omega$	±12	±13.9		±11	±13.8		±10.5	±13.7		V
Output Resistance	DC, open loop		70								Ω
Short Circuit Current	R_L = 0Ω		35	60		25			15		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range,											
Derated Performance		±4		±18							VDC
Current, Quiescent	I_O = 0mADC		3.6	4.7		4.3	6		6.1	8	mA
TEMPERATURE RANGE											
Specification[6]	Ambient temp.	−55		+200							°C
Operating (Typical)	Ambient temp.	−65		+225							°C
Storage	Ambient temp.	−65		+225							°C
θ Junction-Ambient			175								°C

NOTES: (1) Noise testing available—inquire. (2) Offset voltage specifications on grade HT are also guaranteed with units fully warmed up. (3) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (4) Long-term voltage offset vs time trend line does not include warm-up drift. (5) Common-mode rejection specified at +200°C with V_{IN} = ±9VDC. (6) 100% tested at −55°C, +25°C and +200°C using forced-air environment. +125°C specification is guaranteed by design. (7) $\pm V_{CC}$ = 6V to 18V at +200°C.

ABSOLUTE MAXIMUM RATINGS

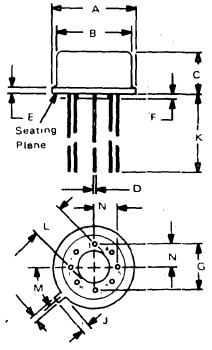
Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage[2]	±0.7VDC
Input Voltage Range[3]	±18VDC
Storage Temperature Range	−65°C to +225°C
Operating Temperature Range	−65°C to +225°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[4]	Continuous
Junction Temperature	+250°C

NOTES: (1) Packages must be derated based on θ_{JC} = 45°C/W or θ_{JA} = 175°C/W. (2) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA. (3) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to the supply voltage. (4) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

MECHANICAL

"M" PACKAGE TO-99 (Hermetic)

NOTE:
Leads in true position within .010" (.25mmR) at MMC at seating plane.



Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8.51	9.40
B	305	335	7.75	8.51
C	165	185	4.19	4.70
D	016	021	0.41	0.53
E	010	040	0.25	1.02
F	010	040	0.25	1.02
G	200 BASIC		5.08 BASIC	
H	028	034	0.71	0.86
J	029	045	0.74	1.14
K	500		12.7	
L	110	160	2.79	4.06
M	45° BASIC		45° BASIC	
N	095	105	2.41	2.67

ORDERING INFORMATION

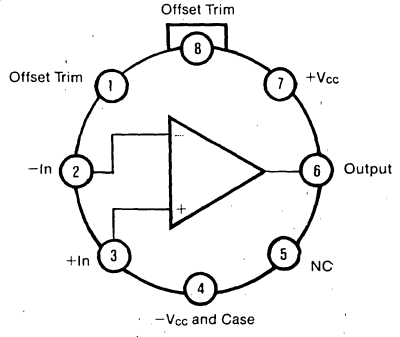
OPAXX HT

Basic Model Number

Performance Grade
HT = −55°C to +200°C

CONNECTION DIAGRAM

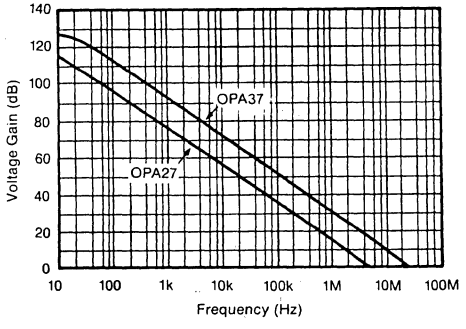
TOP VIEW



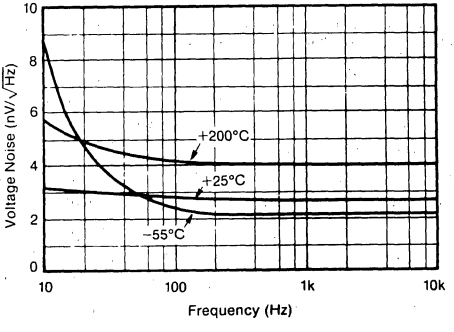
TYPICAL PERFORMANCE CURVES

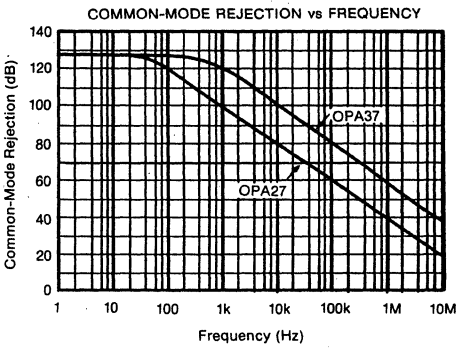
T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

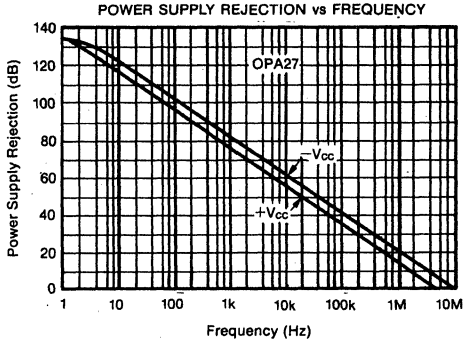
OPEN-LOOP FREQUENCY RESPONSE

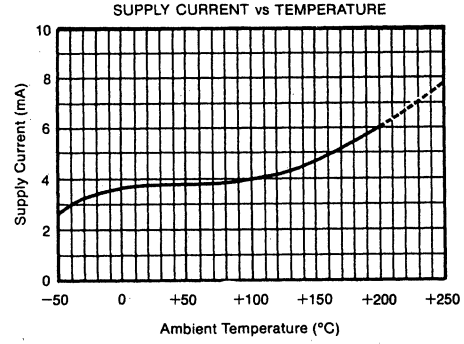


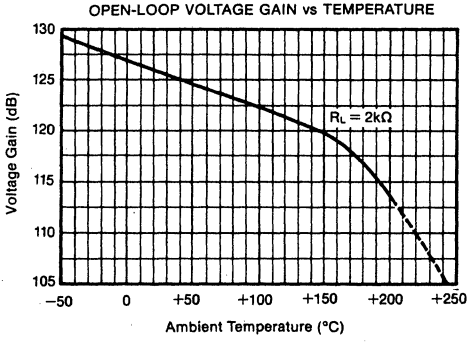
INPUT VOLTAGE NOISE SPECTRAL DENSITY

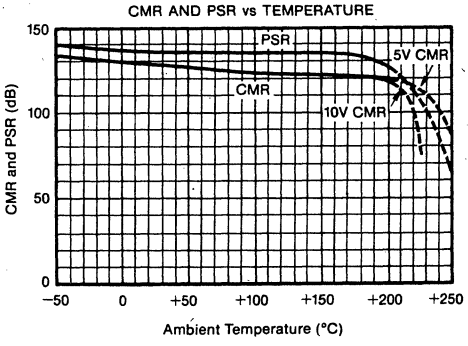


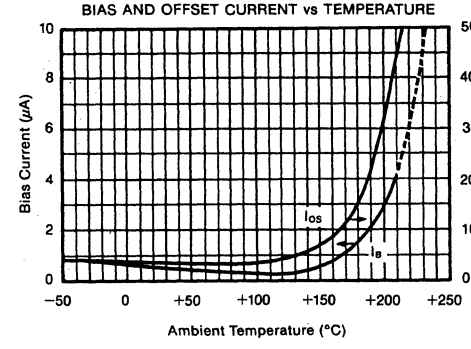










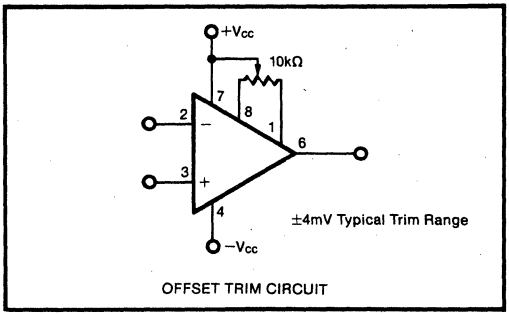


APPLICATIONS INFORMATION

These amplifiers are capable of unusually low voltage offset and drift and to achieve this ultimate capability, attention must be paid to externally generated thermal EMF contributions. Dissimilar metal junctions together with temperature gradients can generate thermocouple voltages that exceed the OPA27/37HT amplifier drift.

The OPA27/37HT are extremely wide-temperature range versions of the standard Burr-Brown OPA27 and OPA37. These high-temperature amplifiers do not employ bias current cancellation but note that their noise current performance has not been degraded.

Eutectic die attach is used exclusively for the OPA27HT and OPA37HT. Hermeticity is assured by 100% fine leak testing. Units are 100% burned-in for 28 hours at +200°C for increased reliability.



BURR-BROWN®

OPA101
OPA102

Low Noise - Wideband
PRECISION JFET INPUT OPERATIONAL AMPLIFIER

FEATURES

- GUARANTEED NOISE SPECTRAL DENSITY - 100% Tested
- LOW VOLTAGE NOISE - 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW VOLTAGE DRIFT - 5μV/°C max (B grade)
- LOW OFFSET VOLTAGE - 250μV max (B grade)
- LOW BIAS CURRENTS - 10pA max at 25°C Ambient (B Grade)
- HIGH SPEED - 10V/μsec min (OPA102)
- GAIN BANDWIDTH PRODUCT - 40MHz (OPA102)

APPLICATIONS

- LOW NOISE SIGNAL CONDITIONING
- LIGHT MEASURMENTS
- RADIATION MEASUREMENTS
- PIN DIODE APPLICATIONS
- DENSITOMETERS
- PHOTODIODE/PHOTOMULTIPLIER CIRCUITS
- LOW NOISE DATA ACQUISITION

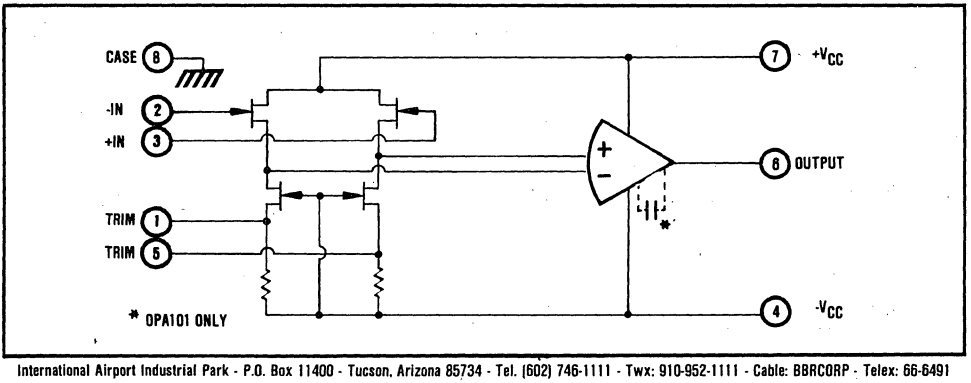
DESCRIPTION

The OPA101 and OPA102 are the first FET operational amplifiers available with noise characteristics (voltage spectral density) guaranteed and 100% tested.

The amplifiers have a complementary set of specifications permitting low errors in signal conditioning applications; low noise, low bias current, high open-loop gain, high common-mode rejection, low offset voltage, low offset voltage drift, etc.

In addition, the amplifiers have moderately high speed. The OPA101 is compensated for unity gain stability and has a slew rate of 5V/μsec, min. The OPA102 is compensated for gains of 3V/V and above and has a slew rate of 10V/μsec, min.

Each unit is laser-trimmed for low offset voltage and low offset voltage drift versus temperature. Bias currents are specified with the units fully warmed up at +25°C ambient temperature.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL		OPA101/102AM			OPA101/102BM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT NOISE								
Voltage Noise Density	f_O = 1Hz(1)		100	200		80	100	$nV/\sqrt{Hz}$
	f_O = 10Hz		32	60		25	30	$nV/\sqrt{Hz}$
	f_O = 100Hz		14	30		11	15	$nV/\sqrt{Hz}$
	f_O = 1kHz		9	15		8	12	$nV/\sqrt{Hz}$
	f_O = 10kHz		7	8		7	8	$nV/\sqrt{Hz}$
	f_O = 100kHz		6.5	8		6.5	8	$nV/\sqrt{Hz}$
f_C; 1/f Corner Frequency			125			100		Hz
Voltage Noise	f_B = 0.1Hz to 10Hz(1)		1.3	2.6		1.0	1.3	µV, p-p
	f_B = 10Hz to 10kHz		1.0	1.2		0.8	1.0	µV, rms
	f_B = 10Hz to 100kHz		2.1	2.6		2.1	2.6	µV, rms
Current Noise Density	f_O = 0.1Hz thru 10kHz		2.0			1.4		$fA/\sqrt{Hz}$
Current Noise	f_B = 0.1Hz to 10Hz		38			26		fA, p-p
	f_B = 10Hz to 10kHz		200			140		fA, rms
DYNAMIC RESPONSE								
Bandwidth, Unity Gain	Small Signal							
OPA101			10			*		MHz
OPA102			Note 2			*		
Gain-Bandwidth Product	A_{CL} = 100							
OPA101			20			*		MHz
OPA102			40			*		MHz
Full Power Bandwidth	V_O = 20V, p-p; R_L = 1kΩ							
OPA101		80	100		*	*		kHz
OPA102		160	210		*	*		kHz
Slew Rate	V_O = ±10V; R_L = 1kΩ							
OPA101	A_{CL} = -1	5	6.5		*	*		V/µsec
OPA102	A_{CL} = -3	10	14		*	*		V/µsec
Settling Time (OPA101)	V_O = ±5V; A_{CL} = -1; R_L = 1kΩ							
ε = 1%			2			*		µsec
ε = 0.1%			2.5			*		µsec
ε = 0.01%			10			*		µsec
Settling Time (OPA102)	V_O = ±5V; A_{CL} = -3; R_L = 1kΩ							
ε = 1%			1			*		µsec
ε = 0.1%			1.5			*		µsec
ε = 0.01%			8			*		µsec
Small-Signal Overshoot	R_L = 1kΩ; C_L = 100pF							
OPA101	A_{CL} = +1		15			*		%
OPA102	A_{CL} = +3		20			*		%
Rise Time	10% to 90%, Small Signal							
OPA101			40			*		nsec
OPA102			30			*		nsec
Phase Margin	R_L = 1kΩ							
OPA101	A_{CL} = +1		60			*		Degrees
OPA102	A_{CL} = +3		45			*		Degrees
Overload Recovery(3)								
OPA101	A_{CL} = -1, 50% overdrive		1			*		µsec
OPA102	A_{CL} = -3, 50% overdrive		0.8			*		µsec
OPEN-LOOP GAIN, DC								
Full Load	V_O = ±10V; R_L = 1kΩ	94	105		*	*		dB
No Load	V_O = ±10V; R_L ≥ 10kΩ	96	108		*	*		dB
RATED OUTPUT								
Voltage	I_O = ±12mA	±12	±13		*	*		V
Current	V_O = ±12V	±12	±30		*	*		mA
Output Resistance	Open-Loop, f = DC		500			*		Ω
Short-Circuit Current			±45			*		mA
Capacitive Load Range	Phase Margin ≥ 25°							
OPA101	A_{CL} = +1		500			*		pF
OPA102	A_{CL} = +3		300			*		pF
INPUT OFFSET VOLTAGE								
Initial Offset	T_A = +25°C		±100	±500		±50	±250	µV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±6	±10		±3	±5	µV/°C
vs Supply Voltage	±5VDC ≤ | V_{CC} | ≤ ±20VDC		±10	±50		*	*	µV/V
vs Time			±10			*		µV/mo.
Adjustment Range	Circuit in "Connection Diagram"		±1			*		mV
INPUT BIAS CURRENT								
Initial Bias	T_A = +25°C		-12	-15		-6	-10	pA
vs Temperature			Note 4			*		
vs Supply Voltage			Note 5			*		

ELECTRICAL (CONT)

MODEL		OPA101/102AM			OPA101/102BM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT DIFFERENCE CURRENT								
Initial Difference	T_A = +25°C		±3	±6		±1.5	±4	pA
vs Temperature			Note 4			•		
vs Supply Voltage			Note 5			•		
INPUT IMPEDANCE								
Differential								
Resistance			10^{12}			•		Ω
Capacitance			1			•		pF
Common-mode								
Resistance			10^{13}			•		Ω
Capacitance			3			•		pF
INPUT VOLTAGE RANGE								
Common-mode Voltage Range	Linear Operation		±(| V_{CC} | -3)			•		V
Common-mode Rejection	f_o = DC, V_{CM} = ±10V	80	105		•	•		dB
POWER SUPPLY								
Rated Voltage			±15			•		VDC
Voltage Range	Derated Performance	±5		±20	•		•	VDC
Current, Quiescent			5.8	8		•	•	mA
TEMPERATURE RANGE								
Specification		-25		+85	•		•	°C
Operating	Derated Performance	-55		+125	•		•	°C
Storage		-65		+150	•		•	°C

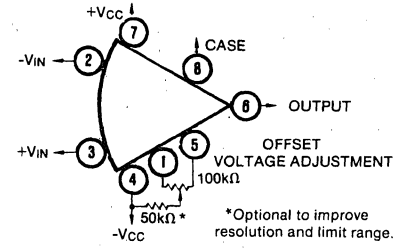
NOTES: *Specifications same as for OPA101/102AM.
1. Parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.
2. Minimum stable gain for the OPA102 is 3V/V.
3. Time required for output to return from saturation to linear operation following the removal of an input overdrive signal.
4. Doubles approximately every 8.5°C.
5. See Typical Performance Curves.

ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	750mW
Differential Input Voltage(2)	±20VDC
Input Voltage, Either Input(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-Circuit Duration(3)	60 seconds
Junction Temperature	+175°C

NOTES:
1. Package must be derated according to the details in the Application Information section.
2. For supply voltages less than ±20VDC, the absolute maximum input is equal to the supply voltage.
3. Short-circuit may be to ground only. See discussion of Thermal Model in the Application Information section.

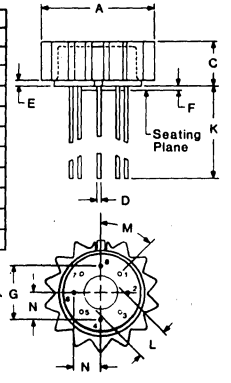
CONNECTION DIAGRAM



NOTE: Offset voltage adjustment affects voltage drift vs temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted.

MECHANICAL SPECIFICATIONS

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.489	.522	12.42	13.26
C	.243	.307	6.17	7.80
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67



NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

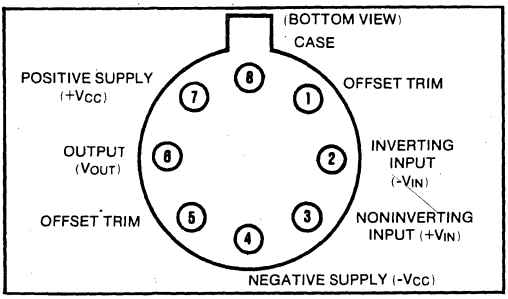
Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

Weight: 2 grams

Order Number:
OPA101AM OPA101BM
OPA102AM OPA102BM

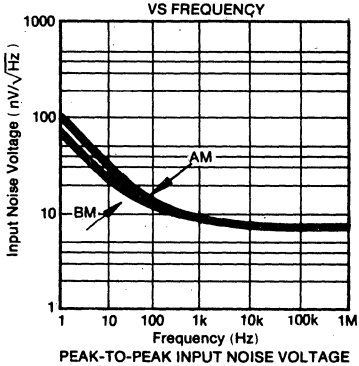
PIN CONFIGURATION



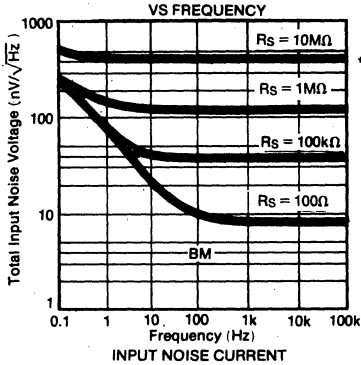
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = ±15VDC, unless otherwise noted. Performance curves apply to both OPA101 and OPA102 unless otherwise noted.)

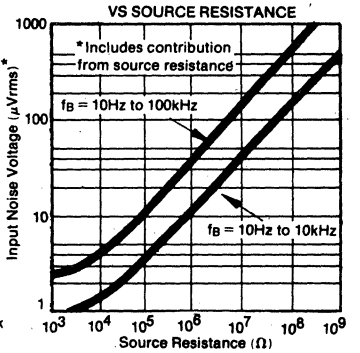
INPUT NOISE VOLTAGE VS FREQUENCY



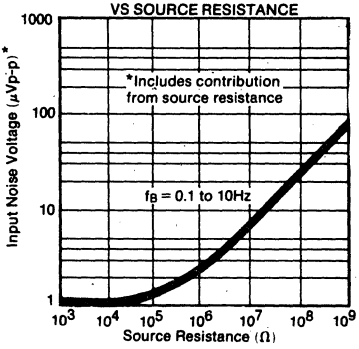
TOTAL INPUT NOISE VOLTAGE VS FREQUENCY



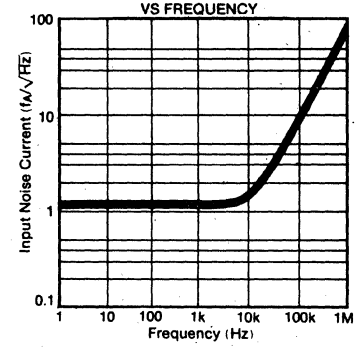
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



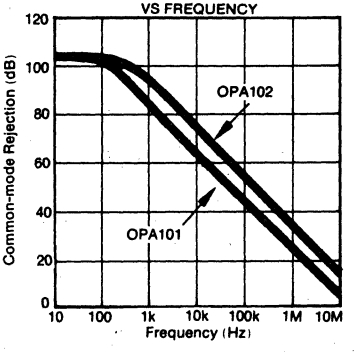
PEAK-TO-PEAK INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



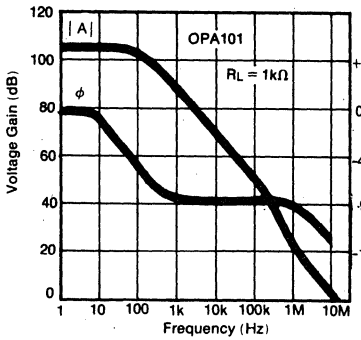
INPUT NOISE CURRENT VS FREQUENCY



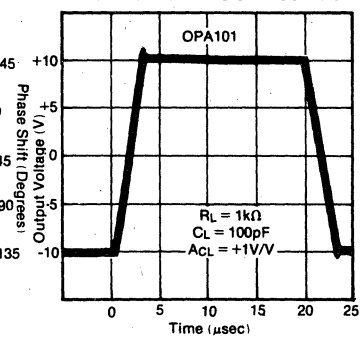
COMMON-MODE REJECTION VS FREQUENCY



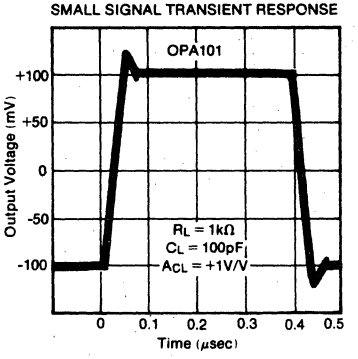
OPEN-LOOP FREQUENCY RESPONSE



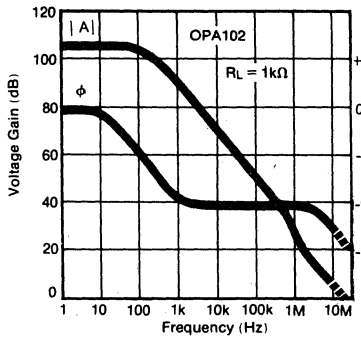
LARGE SIGNAL TRANSIENT RESPONSE



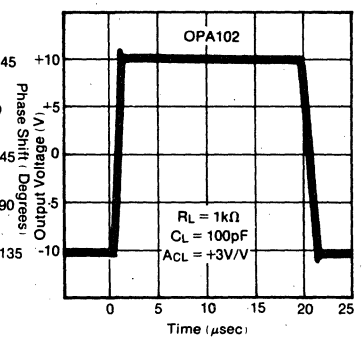
SMALL SIGNAL TRANSIENT RESPONSE



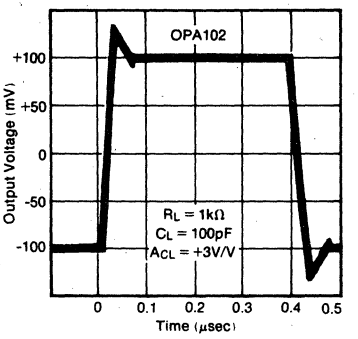
OPEN-LOOP FREQUENCY RESPONSE



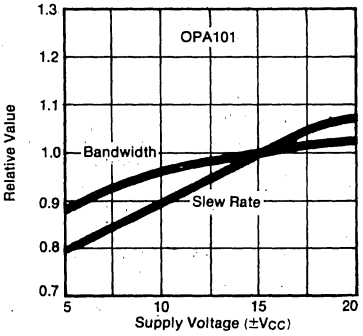
LARGE SIGNAL TRANSIENT RESPONSE



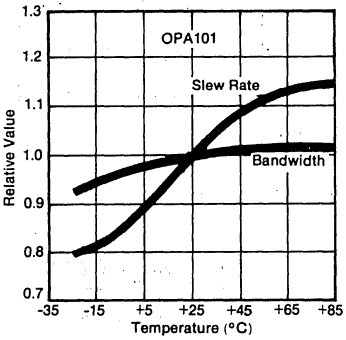
SMALL SIGNAL TRANSIENT RESPONSE



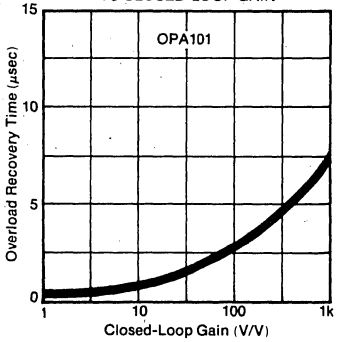
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



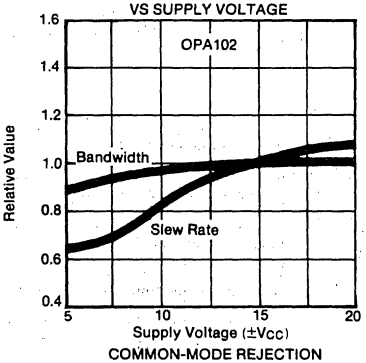
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



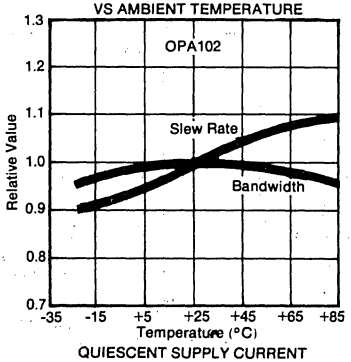
OVERLOAD RECOVERY TIME VS CLOSED-LOOP GAIN



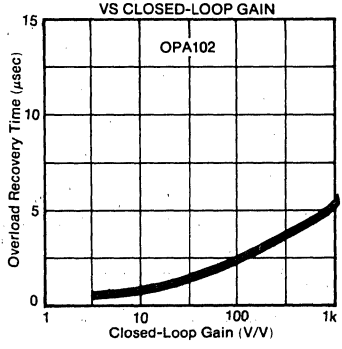
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



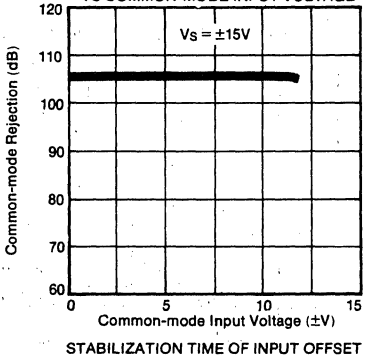
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



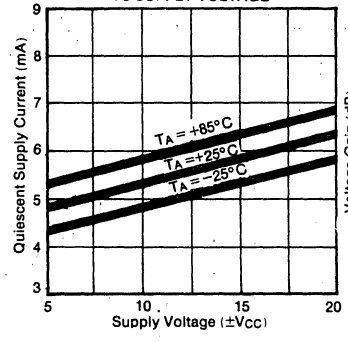
OVERLOAD RECOVERY TIME VS CLOSED-LOOP GAIN



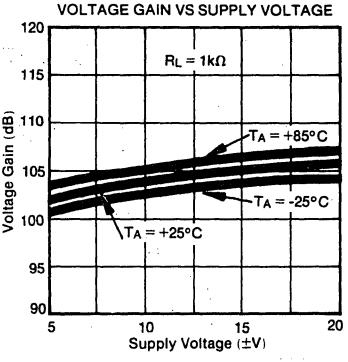
COMMON-MODE REJECTION VS COMMON-MODE INPUT VOLTAGE



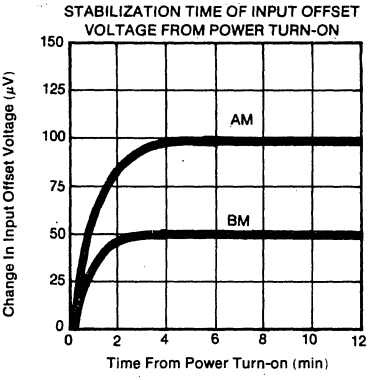
QUIESCENT SUPPLY CURRENT VS SUPPLY VOLTAGE



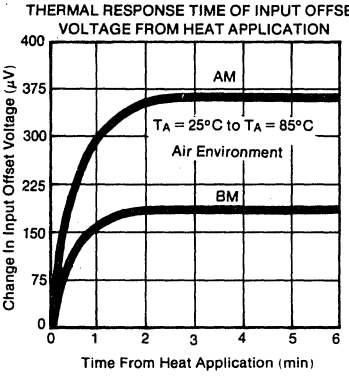
VOLTAGE GAIN VS SUPPLY VOLTAGE



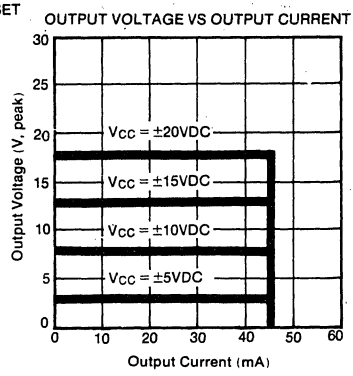
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



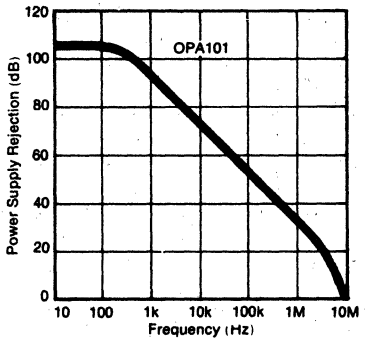
THERMAL RESPONSE TIME OF INPUT OFFSET VOLTAGE FROM HEAT APPLICATION



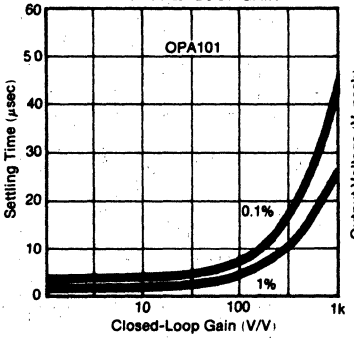
OUTPUT VOLTAGE VS OUTPUT CURRENT



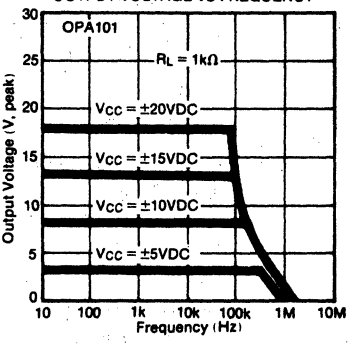
POWER SUPPLY REJECTION VS FREQUENCY



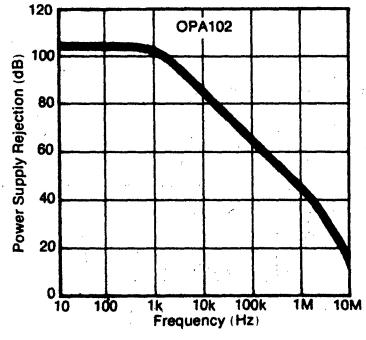
SETTLING TIME VS CLOSED-LOOP GAIN



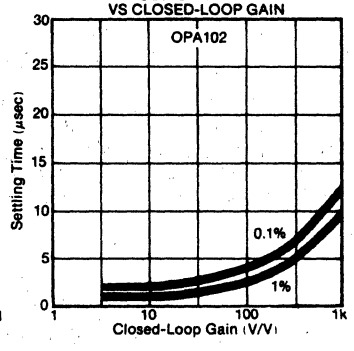
OUTPUT VOLTAGE VS FREQUENCY



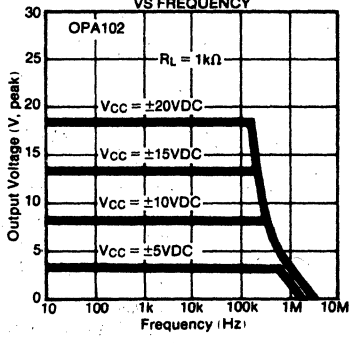
POWER SUPPLY REJECTION VS FREQUENCY



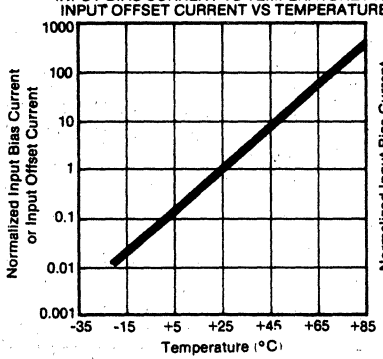
SETTLING TIME VS CLOSED-LOOP GAIN



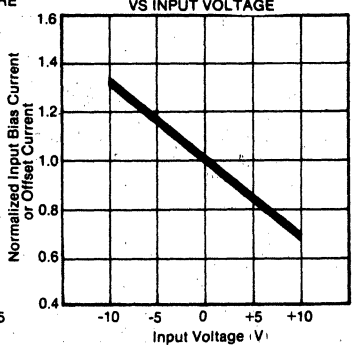
OUTPUT VOLTAGE VS FREQUENCY



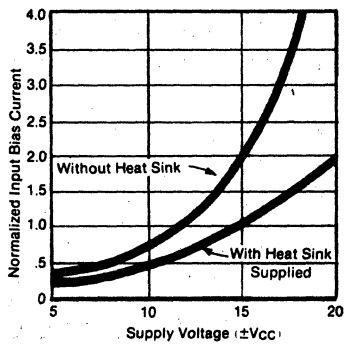
INPUT BIAS CURRENT VS TEMPERATURE AND INPUT OFFSET CURRENT VS TEMPERATURE



INPUT BIAS CURRENT VS INPUT VOLTAGE AND INPUT OFFSET CURRENT VS INPUT VOLTAGE



INPUT BIAS CURRENT VS SUPPLY VOLTAGE



APPLICATION INFORMATION

INTRODUCTION

The availability of detailed noise spectral density characteristics for the OPA101/102 amplifiers allows an accurate noise error analysis in a variety of different circuit configurations. The fact that the spectral characteristics are guaranteed maximums allows absolute noise errors to be truly bounded. Other FET amplifiers normally use simpler specifications of rms noise in a given bandwidth (typically 10Hz to 10kHz) and peak-to-peak noise (typically specified in the band 0.1Hz to 10Hz). These specifications do not contain enough information to allow accurate analysis of noise behavior in any but the simplest of circuit configurations.

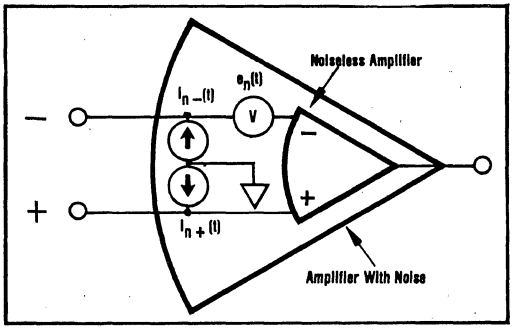


FIGURE 1. Noise Model of OPA101/102.

Noise in the OPA101/102 can be modeled as shown in Figure 1. This model is the same form as the DC model for offset voltage (E_{OS}) and bias currents (I_B). In fact, if the voltage $e_n(t)$ and currents $i_n(t)$ are thought of as general instantaneous error sources, then they could represent either noise or DC offsets. The error equations for the general instantaneous model are shown in Figure 2 below.

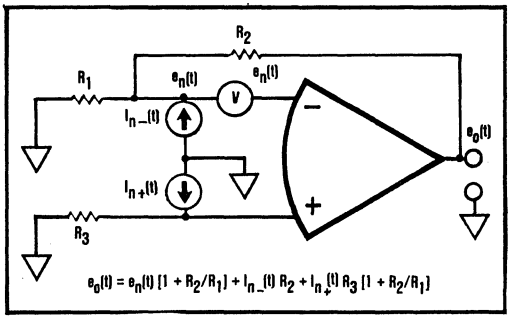


FIGURE 2. Circuit With Error Sources.

If the instantaneous terms represent DC errors (i.e., offset voltage and bias currents) the equation is a useful tool to compute actual errors. It is not, however, useful in the same direct way to compute noise errors. The basic problem is that noise cannot be predicted as a function of time. It is a random variable and must be described in probabilistic terms. It is normally described by some type of average - most commonly the rms value.

$$N_{rms} \triangleq \sqrt{1/T \int_0^T n^2(t)\, dt} \qquad (1)$$

where N_{rms} is the rms value of some random variable n(t). In the case of amplifier noise, n(t) represents either $e_n(t)$ or $i_n(t)$.

The internal noise sources in operational amplifiers are normally uncorrelated. That is, they are randomly related to each other in time and there is no systematic phase relationship. Uncorrelated noise quantities are combined as root-sum-squares. Thus, if $n_1(t)$, $n_2(t)$, and $n_3(t)$ are uncorrelated then their combined value is

$$N_{TOTAL_{rms}} = \sqrt{N_1^2{}_{rms} + N_2^2{}_{rms} + N_3^2{}_{rms}} \qquad (2)$$

The basic approach in noise error calculations then is to identify the noise sources, segment them into conveniently handled groups (in terms of the shape of their noise spectral densities), compute the rms value of each group, and then combine them by root-sum-squares to get the total noise.

TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. It will be used to demonstrate the above noise calculation method.

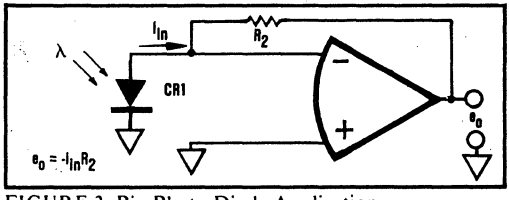


FIGURE 3. Pin Photo Diode Application.

CR1 is a PIN photo diode connected in the photovoltaic mode (no bias voltage) which produces an output current i_{in} when exposed to the light, λ.

A more complete circuit is shown in Figure 4. The values shown for C_1 and R_1 are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of C_2 is what would be expected from stray capacitance with moderately careful layout (0.5pF to 2pF). A larger value of C_2 would normally be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

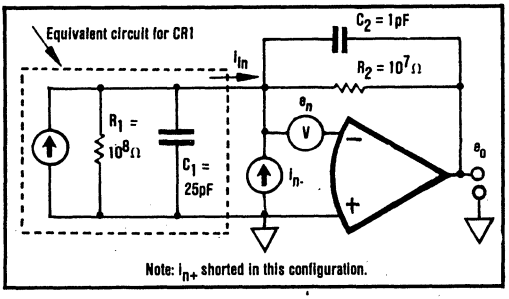


FIGURE 4. Noise Model of Photo Diode Application.

In Figure 4, e_n and i_n represent the amplifier's voltage and current spectral densities, $e_n(\omega)$ and $i_n(\omega)$ respectively. These are shown in Figure 5.

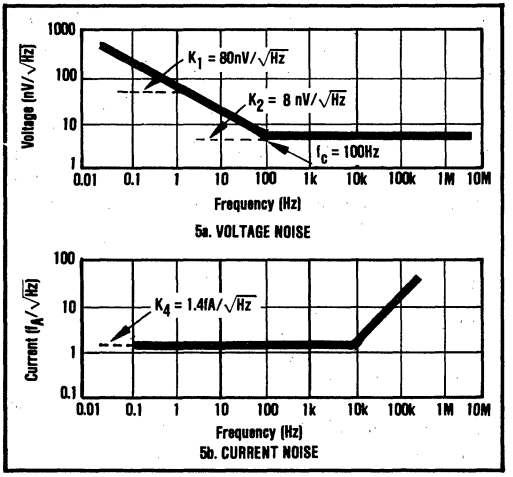


FIGURE 5. Noise Voltage and Current Spectral Density.

Figure 6 shows the desired "gain" of the circuit (transimpedance of $e_o/i_{in} = Z_2(s)$). It has a single-pole rolloff at $f_2 = 1/(2\pi R_2C_2) = \omega_2/2\pi$. Output noise is minimized if f_2 is made smaller. Normally R_2 is chosen for the desired DC transimpedance based on the full scale input current (i_{in} full scale) and maximum output (e_o max). Then C_2 is chosen to make f_2 as small as possible consistent with the necessary signal frequency response.

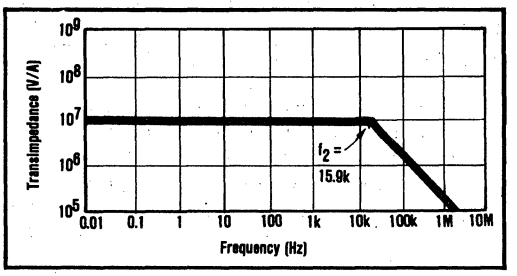


FIGURE 6. Transimpedance.

Voltage Noise

Figure 7 shows the noise voltage gain for the circuit in Figure 4. It is derived from the equation

$$e_o = e_n\left[\frac{A}{1+A\beta}\right] = e_n\,\frac{1}{\beta}\left[\frac{1}{1+\frac{1}{A\beta}}\right] \qquad (3)$$

where:

$A = A(\omega)$ is the open-loop gain

$\beta = \beta(\omega)$ is the feedback factor. It is the amount of output voltage feedback to the input of the op amp.

$A\beta = A(\omega)\,\beta(\omega)$ is the loop gain. It is the amount of the output voltage feedback to the input and then amplified and returned to the output.

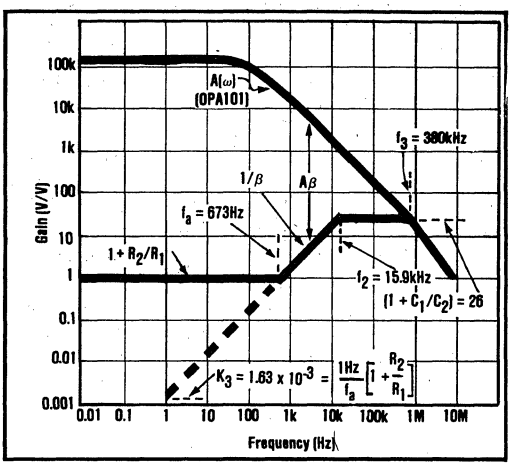


FIGURE 7. Noise Voltage Gain.

Note that for large loop gain ($A\beta >> 1$)

$$e_o \cong e_n\,\frac{1}{\beta} \qquad (4)$$

For the circuit in Figure 4 it can be shown that

$$\frac{1}{\beta} = 1 + \frac{R_2(R_1C_1s+1)}{R_1(R_2C_2s+1)} \qquad (5)$$

This may be rearranged to

$$\frac{1}{\beta} = \frac{R_2+R_1}{R_1}\left[\frac{\tau_a s+1}{\tau_2 s+1}\right] \qquad (5a)$$

where $\tau_a = (R_1 \parallel R_2)(C_1 \parallel C_2)$ (5b)

$$= \left[\frac{R_1R_2}{R_1+R_2}\right](C_1+C_2)$$

and $\tau_2 = R_2C_2$ (5c)

Then, $f_a = \dfrac{1}{2\pi\tau_a}$ and $f_2 = \dfrac{1}{2\pi\tau_2}$ (5d)

For very low frequencies ($f << f_a$), s approaches zero and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1} \qquad (6)$$

For very high frequencies ($f >> f_2$), s approaches infinity and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{C_1}{C_2} \qquad (7)$$

The noise voltage spectral density at the output is obtained by multiplying the amplifier's noise voltage spectral density (Figure 5a) times the circuits noise gain (Figure 7). Since both curves are plotted on log-log scales the multiplication can be performed by the addition of the two curves. The result is shown in Figure 8.

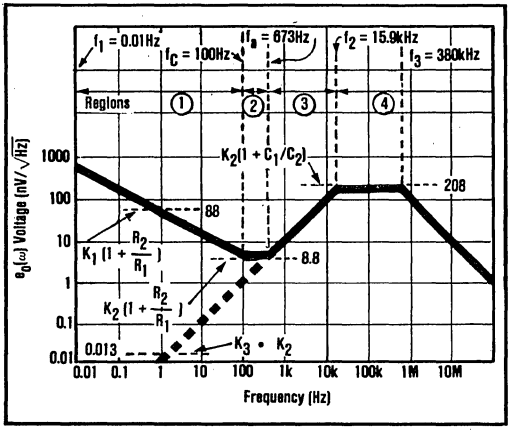


FIGURE 8. Output Noise Voltage Spectral Density.

The total rms noise at the amplifier's output due to the amplifier's internal voltage noise is derived from the $e_o(\omega)$ function in Figure 8 with the following expression:

$$E_{o\ rms} = \sqrt{\int_{-\infty}^{+\infty} e_o^2(\omega)\, d\omega} \qquad (8)$$

It is both convenient and informative to calculate the rms noise using a piecewise approach (region-by-region) for each of the four regions indicated in Figure 8.

Region 1; $f_l = 0.01Hz$ to $f_c = 100Hz$

$$E_{n1\ rms} = K_1 \left(1 + \frac{R_2}{R_1}\right) \sqrt{\ln(f_c/f_l)} \qquad (9)$$

$$= 80nV/\sqrt{Hz} \left(1 + \frac{10^7}{10^8}\right) \sqrt{\ln \frac{100}{0.01}} \qquad (9a)$$

$$= 2.67\mu V$$

This region has the characteristic of $1/f$ or "pink" noise (slope of -10dB per decade on the log-log plot of $e_n(\omega)$). The selection of 0.01Hz is somewhat arbitrary but it can be shown that for this example there would be only negligible additional contribution by extending f_l several decades lower. Note that $K_1(1 + R_2/R_1)$ is the value of e_o at $f = 1Hz$.

Region 2; $f_c = 100Hz$ to $f_a = 673Hz$

$$E_{n2\ rms} = K_2 \left(1 + \frac{R_2}{R_1}\right) \sqrt{f_a - f_c} \qquad (10)$$

$$= 8nV/\sqrt{Hz} \left(1 + \frac{10^7}{10^8}\right) \sqrt{673 - 100} \qquad (10a)$$

$$= 0.21\mu V$$

This is a region of "white" noise which leads to the form of equation (10).

Region 3; $f_a = 673Hz$ to $f_2 = 15.9kHz$

$$E_{n3\ rms} = K_2 \cdot K_3 \sqrt{\frac{f_2^3}{3} - \frac{f_a^3}{3}} \qquad (11)$$

$$= 8nV/\sqrt{Hz}\,(1.63 \times 10^{-3}) \sqrt{\frac{(15.9k)^3}{3} - \frac{(673)^3}{3}} \qquad (11a)$$

$$= 15.1\mu V$$

This is the region of increasing noise gain (slope of +20dB/decade on the log-log plot) caused by the lead network formed by the resistance $R_1 \| R_2$ and the capacitance $(C_1 + C_2)$. Note that $K_3 \cdot K_2$ is the value of the $e_o(\omega)$ function for this segment projected back to 1Hz.

Region 4; $f > 15.9kHz$

$$E_{n4\ rms} = K_2 \left(1 + \frac{C_1}{C_2}\right) \sqrt{\left[\frac{\pi}{2}\right] f_3 - f_2} \qquad (12)$$

$$= 8nV/\sqrt{Hz} \left(1 + \frac{25}{1}\right) \sqrt{\left[\frac{\pi}{2}\right] 380k - 15.9k} \qquad (12a)$$

$$= 158.5\mu V$$

This is a region of white noise with a single order rolloff at $f_3 = 380kHz$ caused by the intersection of the $1/\beta$ curve and the open-loop gain curve. The value of 380kHz is obtained from observing the intersection point of Figure 7. The $\pi/2$ applied to f_3 is to convert from a 3dB corner frequency to an effective noise bandwidth.

Current Noise

The output voltage component due to current noise is equal to:

$$E_{ni} = i_n \times Z_2(s) \qquad (13)$$

where $Z_2(s) = R_2 \| X_{C_2}$ (13a)

This voltage may be obtained by combining the information from figures 5 (b) and 6 together with the open loop gain curve of Figure 7. The result is shown in Figure 9 below.

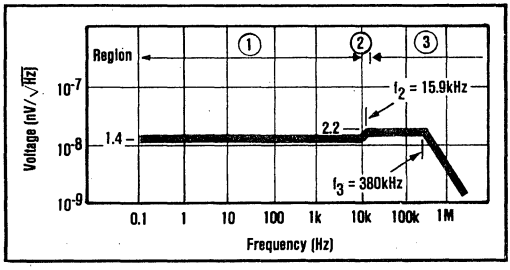


FIGURE 9. Output Voltage Due to Noise Current.

Using the same techniques that were used for the voltage noise:

Region 1; 0.1Hz to 10kHz

$$E_{ni1} = 1.4 \times 10^{-8} \sqrt{10k - 0.1} \quad (14)$$

$$= 1.4\mu V$$

Region 2; 10kHz to 15.9kHz

$$E_{ni2} = 1.4 \times 10^{-12} \sqrt{\frac{(15.9k)^3}{3} - \frac{(10k)^3}{3}} \quad (14a)$$

$$= 1.4\mu V$$

Region 3; f > 15.9kHz

$$E_{ni3} = 2.2 \times 10^{-8} \sqrt{\frac{\pi}{2} 380k - 15.9k} \quad (14b)$$

$$= 16.8\mu V$$

$$E_{ni\ total} = 10^{-6} \sqrt{(1.4)^2 + (1.4)^2 + (16.8)^2} \quad (14c)$$

$$= 16.9\mu V_{rms}$$

Resistor Noise

For a complete noise analysis of the circuit in Figure 4, the noise of the feedback resistor, R_2, must also be included. The thermal noise of the resistor is given by:

$$E_{R\ rms} = \sqrt{4kTRB} \quad (15)$$

K = Boltzmann's constant = 1.38×10^{-23} Joules/°Kelvin
T = Absolute temperature (degrees Kelvin)
R = Resistance (ohms)
B = Effective noise bandwidth (Hz) (ideal filter assumed)

At 25°C this becomes
E_R rms $\cong 0.13 \sqrt{RB}$
E_R rms in μV
R in MΩ
B in Hz

For the circuit in Figure 4
$R_2 = 10^7\Omega = 10M\Omega$

$$B = \frac{\pi}{2}(f_2) = \frac{\pi}{2} 15.9k$$

Then

$$E_R\ rms = (411nV/\sqrt{Hz}) \sqrt{B}$$

$$= (411nV/\sqrt{Hz}) \sqrt{\frac{\pi}{2} 15.9kHz}$$

$$= 64.9\mu V\ rms$$

Total Noise

The total noise may now be computed from

$$E_{n\ total} = \sqrt{E_{n1}^2 + E_{n2}^2 + E_{n3}^2 + E_{n4}^2 + E_{nR}^2 + E_{ni}^2} \quad (16)$$

$$= \sqrt{2.67^2 + 0.21^2 + 15.1^2 + 158.5^2 + 64.9^2 + 16.9^2} \quad (16a)$$

$$= \sqrt{7.1 + 0.04 + 228 + 25122 + 4212 + 286} \quad (16b)$$

$$= 173\mu V\ rms$$

Conclusions

Examination of the results in equation (16b) together with the curves in Figure 8 leads to some interesting conclusions. In this example 84% of the noise comes from E_{n4}. From Figure 8 it is seen that this is the area beyond the pole formed by R_2 and C_2.

The E_{n4} contribution could be reduced several ways. The most common method is to increase C_2. This reduces f_2 and the value of K2(1 + C1/C2) (see Figure 8). It also reduces the signal bandwidth (see Figure 6) and the final value of C_2 is normally a compromise between noise gain and necessary signal bandwidth.

It should be noted that increasing C_2 will also affect f_a since f_a is determined by $(C_1 + C_2)$ (see equation (5b)). Normally C_2 is larger than C_1 and f_2 will change more than f_a for a given change in C_2.

The other means of reducing the noise in region 4 involves changing amplifier parameters. For example, the use of a slower amplifier would move the open-loop gain curve to the left and decrease f_3. Of course, reducing the value of K_2, the noise floor, would also reduce the noise in this region.

The second largest component is the resistor noise E_{nR} (14% of the total noise). A lower resistor value decreases resistor noise as a function of $\sqrt{R}$, but it also lowers the desired signal gain as a direct function of R. Thus, lowering R reduces the signal-to-noise ratio at the output which shows that the feedback resistor should be as large as possible. The noise contribution due to R_2 can be decreased by raising the value of C_2 (lowering f_2) but this reduces signal bandwidth.

It is interesting to note that the current noise of the amplifier accounted for only 1% of the total E_n. This is different than would be expected when comparing the current and voltage spectral densities with the size of the feedback resistor. For example, if we define a characteristic value of resistance as

$$R_{characteristic} = \frac{e_n(\omega)}{i_n(\omega)} \text{ at } f = 10kHz \quad (17)$$

$$= \frac{8nV/\sqrt{Hz}}{1.4fA/\sqrt{Hz}}$$

$$= 5.7M\Omega$$

Thus, in simple transimpedance circuits with feedback resistors greater than the characteristic value, the amplifier's current noise would cause more output noise than the amplifier's voltage noise. Based on this and the 10MΩ feedback resistor in the example, the amplifier noise current would be expected to have a higher contribution than the noise voltage. The reason it does not in the example of Figure 4 is that the noise voltage has high gain at higher frequencies (Figure 7) and the noise current does not (Figure 6).

The fourth largest component of total noise comes from E_{n3} (0.8%). Decreasing C_1 will also lower the term $K_2(1 + C_1/C_2)$. In this case, f_2 will stay fixed and f_a will move to the right (i.e., the +20dB/decade slope segment will move

to the right). This can have a significant reduction on noise without lowering the signal bandwidth. This points out the importance of maintaining low capacitance at the amplifier's input in low noise applications.

Shielding and Guarding

The low noise, low bias current and high input impedance of the OPA101/102 are well suited to a number of precision applications. In order to fully benefit from the outstanding specifications of this unit, careful layout, shielding, and guarding are required. Careless signal wiring or printed circuit board layout can easily degrade circuit performance several orders of magnitude below the capability of the OPA101/102.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. The metal case of the OPA101/102 is connected to pin 8 and is not connected to any internal amplifier circuitry. Thus it is possible to use the case as a shield to reduce noise pickup.

Unless care is used, leakage currents across printed circuit boards can easily exceed the bias current of the OPA101/102. To avoid leakage problems, it is recommended that a Teflon IC socket be used or that at least the signal input lead of the amplifier be wired to a Teflon standoff. If this is not done and instead the OPA101/102 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 10). The amplifier case, pin 8, should also be connected to the guard. This insures that the entire amplifier circuitry is fully surrounded by the guard potential. This minimizes the voltage placed across any leakage paths and thus reduces leakage currents. In addition, noise pickup is also reduced.

Figures 11, 12, and 13 show typical applications using the guard and case shielding.

Cleanliness is also a prime concern in low bias current circuits. It is recommended that after installation is complete the assembly be washed with a low residue solvent such as TMC Freon followed by rinsing with deionized water. The use of some form of high dielectric conformal coating such as a good two-part urathane should be considered if the assembly will be used in air environment which could deposit contaminants on the low current circuitry.

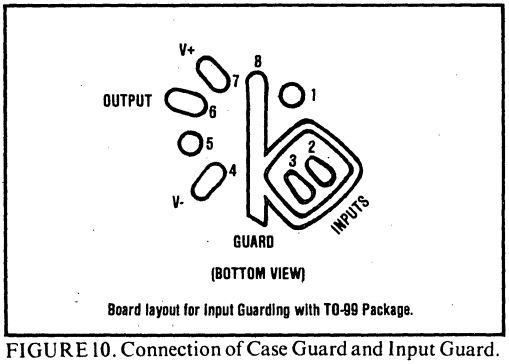


FIGURE 10. Connection of Case Guard and Input Guard.

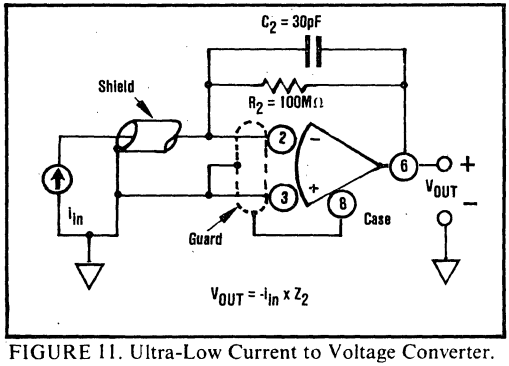


FIGURE 11. Ultra-Low Current to Voltage Converter.

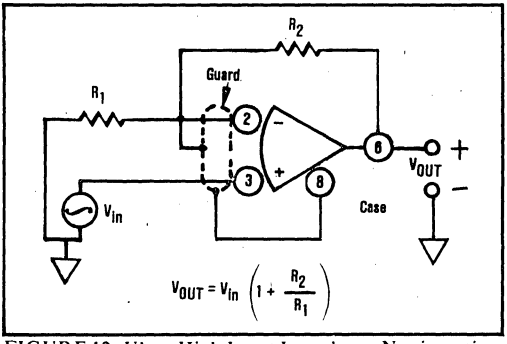


FIGURE 12. Ultra-High Input Impedance Noninverting Circuit.

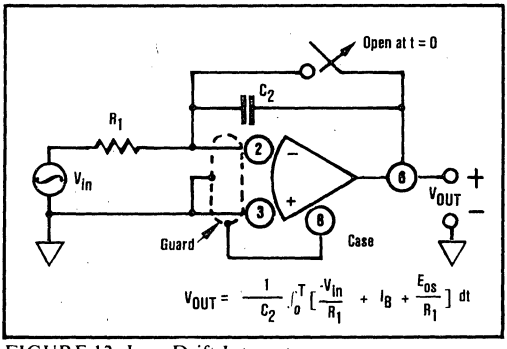


FIGURE 13. Low Drift Integrator.

Thermal Model

Figure 14 is the thermal model for the OPA101/102 where:

T_J = Junction temperature (output load)
T_J* = Junction temperature (no load)
T_C = Case temperature
T_A = Ambient temperature
θ_{CA} = Thermal resistance, case-to-ambient

θ_{HS} = Effective thermal resistance of the heat sink
P_{DQ} = Quiescent power dissipation
$= |+V_{CC}| I_{+QUIESCENT} + |-V_{CC}| I_{-QUIESCENT}$
P_{DX} = Power dissipation in the output transistor
$= (V_{OUT} - V_{CC}) I_{OUT}$

(In a complementary output stage only one output transistor is conducting current at a time.)

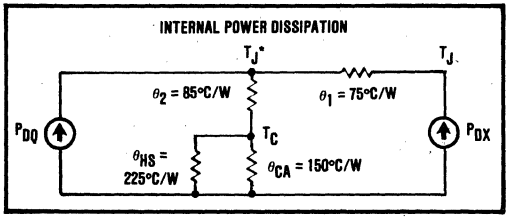


FIGURE 14. OPA101/102 Thermal Model

This model is obviously not the simple one-power source model used with most linear integrated circuits. It is, however, a more accurate model for multichip hybrid integrated circuits where the quiescent power is dissipated in the input stage and the internal power dissipation due to the load is dissipated in a somewhat physically separated output stage.

The model in Figure 14 must be used in conjunction with the OPA101/102's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

As an example of how to use this model, consider this problem: Determine the output transistor junction temperature when the output has its maximum load resistance and is operated at the worst-case output voltage conditions. Assume $V_{CC} = \pm 15$VDC and $T_A = 25°C$.

Maximum P_{DX} occurs where $V_{OUT} = 1/2 V_{CC}$. Then

$$P_{DX\ max} = \frac{(V_{CC})^2}{4R_{load}} \qquad (18)$$

$$T_j = T_A + P_{DQ}[\theta_2 + (\theta_{HS} \parallel \theta_{CA})] + P_{DX}[\theta_1 + \theta_2 + (\theta_{HS} \parallel \theta_{CA})] \qquad (19)$$

where $(\theta_{HS} \parallel \theta_{CA}) = \frac{\theta_{HS}\theta_{CA}}{\theta_{HS} + \theta_{CA}} = 90°C/W$

Substituting appropriate values yields

$$T_j = 25° + (30V \times 8mA)[85°C/W + 90°C/W] + \frac{(15V)^2}{4 \times 1k\Omega}[75°C/W + 85°C/W + 90°C/W]$$

$$= 25°C + 42°C + 14°C = T_A + 56°C$$

$$= 81°C$$

The conclusion is that under a worst-case output voltage condition and with a 1kΩ load the junction temperature rise is 56°C above ambient. Thus, under these conditions, the device could be operated in an ambient up to 119°C without exceeding the 175°C junction temperature rating.

A similar analysis for conditions of the output short-circuited to ground where

$$P_{DX\ SS} = V_{CC} I_{(output\ limit)} \qquad (20)$$

shows that the maximum junction temperature rating of 175°C is exceeded. Thus, the output should not be shorted to ground for sustained periods of time.

HEAT SINK

The heat sink used on the OPA101/102 should not be removed. It has the effect of reducing the package thermal resistance from 150°C/W to about 90°C per watt. Removing the heat sink would naturally increase the junction temperature of the amplifier which would in turn raise the input bias current. The change in thermal resistance also affects the noise performance. Removing the heat sink would increase the noise in the 1/f region.

BURR-BROWN®

OPA103

For a /883B version of this product see OPA105/883B in the Military Products section.

Low Drift - Low Bias Current FET Input OPERATIONAL AMPLIFIER

FEATURES

- LOW BIAS CURRENT, 1pA, max
- HIGH INPUT IMPEDANCE, $10^{15}\Omega$
- ULTRA-LOW DRIFT, $2\mu V/°C$, max
- LOW OFFSET VOLTAGE, 0.25mV, max
- LOW QUIESCENT CURRENT, 1.5mA, max
- HERMETICALLY SEALED TO-99 PACKAGE

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS SUCH AS:
  - photo current detectors
  - pH electrodes
  - biological probes/transducers

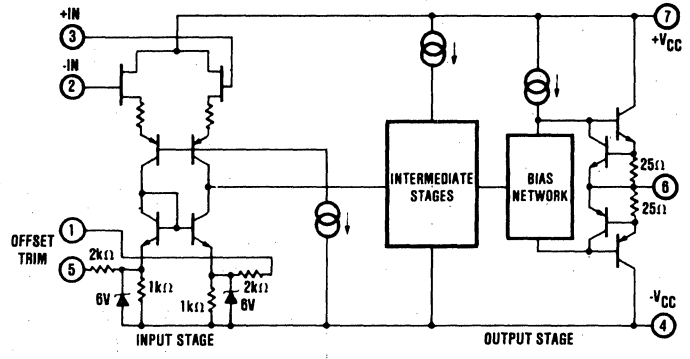
DESCRIPTION

The OPA103 is a precision low bias current operational amplifier. Guaranteed low initial offset voltage (0.25mV, max) and associated drift versus temperature ($2\mu V/°C$, max) is achieved by laser-adjusting the amplifier during manufacturing. This feature, and guaranteed low bias current (1pA, max), allow greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristics of the OPA103 include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidentally shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA103 allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL	OPA103AM			OPA103BM			OPA103CM			OPA103DM			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OPEN-LOOP GAIN, DC, V_{OUT} + ±10V													
Rated Load, $R_L \geq 2k\Omega$	100	106		*	*		*	*		*	*		dB
$R_L \geq 10k\Omega$		112			*			*			*		dB
T_A = -25°C to +85°C, $R_L \geq 2k\Omega$	94	100		*	*		*	*		*	*		dB
RATED OUTPUT													
Voltage at R_L = 2kΩ, T_A = -25°C to +85°C	±10	±12		*	*		*	*		*	*		V
R_L = 10kΩ, T_A = -25°C to +85°C	±12	±13		*	*		*	*		*	*		V
Current, T_A = -25°C to +85°C; V_O = ±10V	±5	±10		*	*		*	*		*	*		mA
Output Impedance		3			*			*			*		kΩ
Load Capacitance(1)	500	1000		*	*		*	*		*	*		pF
Short Circuit Current	10	25		*	*		*	*		*	*		mA
FREQUENCY RESPONSE													
Unity Gain, Small Signal		1			*			*			*		MHz
Full Power Response	14	20		*	*		*	*		*	*		kHz
Slew Rate	0.9	1.3		*	*		*	*		*	*		V/µsec
Settling Time (0.1%)		9			*			*			*		µsec
Settling Time (0.01%)		20			*			*			*		µsec
Overload Recovery(2), 50% overdrive		4	15		*	*		*	*		*	*	µsec
INPUT OFFSET VOLTAGE													
Initial Offset, T_A = +25°C		±200	±500		*	*		±100	±250		±100	±250	µV
vs Temperature, T_A = -25°C to +85°C		±15	±25		±10	±15		±3	±5		±1	±2	µV/°C
vs Supply Voltage, T_A = -25°C to +85°C		±20	±200		*	*		*	*		*	*	µV/V
INPUT BIAS CURRENT(3)													
Initial Bias, T_A = +25°C			−2			-1			-1			-1	pA
vs Supply Voltage		0.005			*			*			*		pA
INPUT DIFFERENCE CURRENT													
Initial Difference, T_A = +25°C		±0.3			±0.2			±0.2			±0.2		pA
INPUT IMPEDANCE													
Differential		10^{13}||0.8			*			*			*		Ω || pF
Common-mode		10^{15}||1.6			*			*			*		Ω || pF
INPUT NOISE													
Voltage, f_O = 10Hz		55			*			*			*		nV/√Hz
f_O = 100Hz		35			*			*			*		nV/√Hz
f_O = 1kHz		30			*			*			*		nV/√Hz
f_O = 10kHz		25			*			*			*		nV/√Hz
f_B = 0.1Hz to 10Hz		3.0			*			*			*		µV (p-p)
Current, f_B = 0.1Hz to 10Hz		0.01			*			*			*		pA (p-p)
f_B = 10Hz to 10kHz		0.003			*			*			*		pA, rms
f_O = 1kHz		0.6			*			*			*		fA/√Hz
INPUT VOLTAGE RANGE													
Differential	±20			*			*			*			V
Common-mode, T_A = -25°C to +85°C	±10	±12		*	*		*	*		*	*		V
Common-mode Rejection, V_{IN} = ±10V	76	86		*	*		*	*		*	*		dB
Maximum Safe Input Voltage		$\pm V_{CC}$			*			*			*		V
POWER SUPPLY													
Rated Voltage		±15			*			*			*		VDC
Voltage Range, derated performance	±5		±20	*		*	*		*	*		*	VDC
Current, quiescent T_A = -25°C to +85°C		1.0	1.5		*	*		*	*		*	*	mA
TEMPERATURE RANGE (ambient)													
Specification	-25		+85	*		*	*		*	*		*	°C
Operating	-55		+125	*		*	*		*	*		*	°C
Storage	-65		+150	*		*	*		*	*		*	°C
θ junction - ambient		235			*			*			*		°C/W

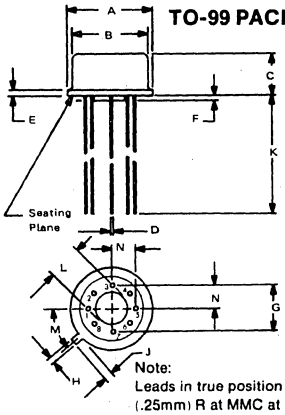
*Specifications same as for OPA103AM.

NOTES:

1. Stability guaranteed with load capacitance ≤ 500pF.
2. Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.
3. Bias current is tested and guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperature the bias current doubles every +10°C.

MECHANICAL

TO-99 PACKAGE



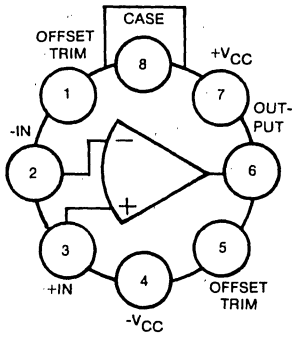
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	---	12.7	---
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Weight: 1 gram

Note:
Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.

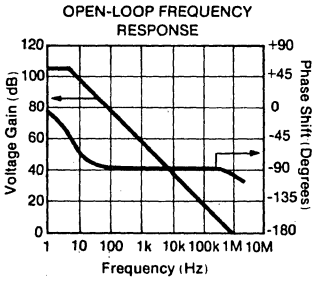
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

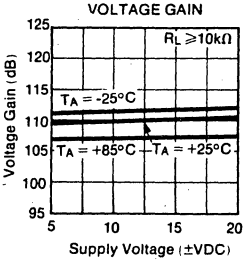
CONNECTION DIAGRAM

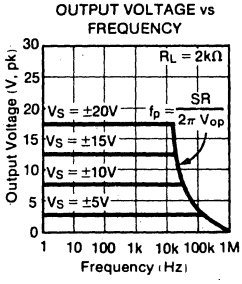


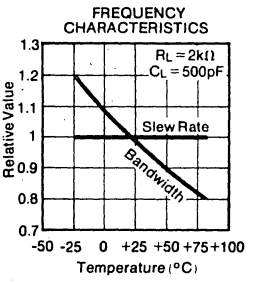
(TOP VIEW)

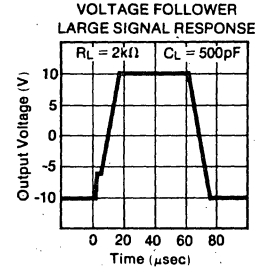
TYPICAL PERFORMANCE CURVES

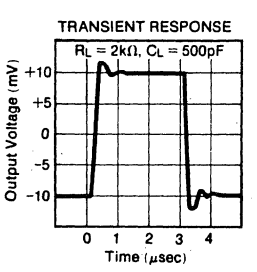


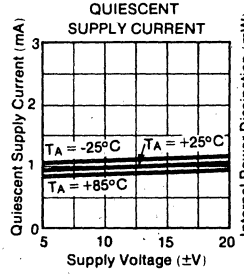


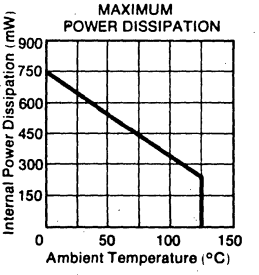


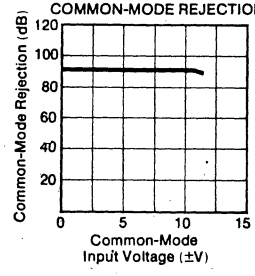


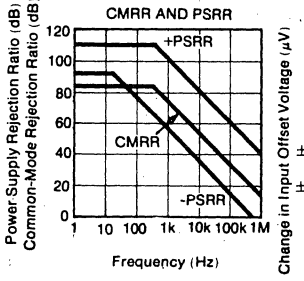


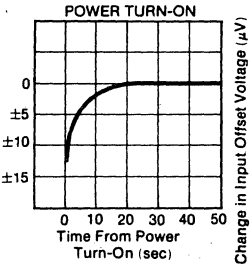


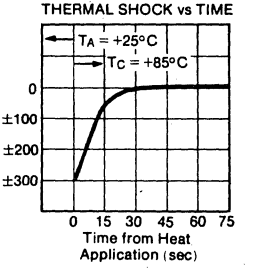












APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the OPA103. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA103 is approximately 20 seconds (see Typical Performance Curves).

GUARDING AND SHIELDING

The ultra-low bias current and high input impedance of the OPA103 are well-suited to a number of stringent applications. However, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA103.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA103. To avoid leakage problems, it is recommended that the signal input lead of the OPA103 be wired to a Teflon standoff. If the OPA103 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 1 illustrates the use of the guard. The resistor R_3 shown in Figure 1 is optional. It may be used to compensate effects of very large source resistances. However, note that its use would also increase the noise due to the thermal noise of R_3.

OFFSET VOLTAGE ADJUSTMENT

Although the OPA103 has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. Figure 2 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C, for every 100μV of offset adjustment.

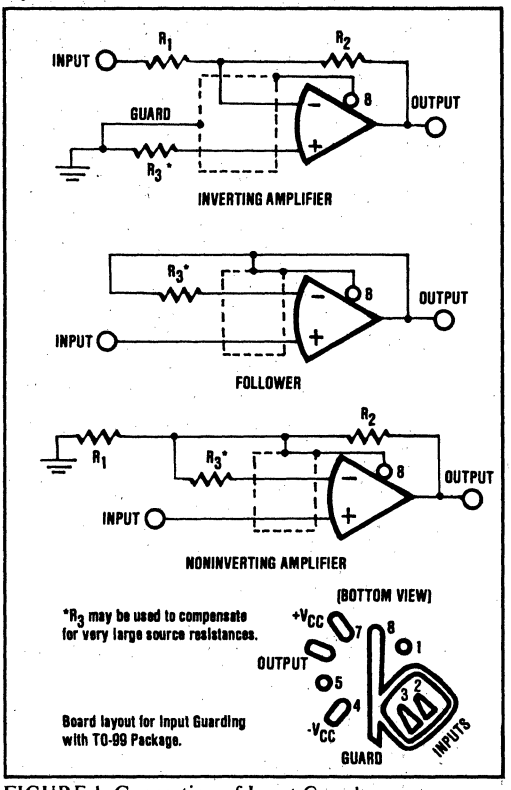


FIGURE 1. Connection of Input Guard.

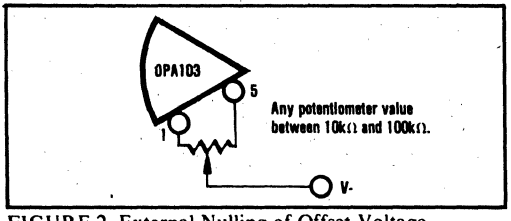


FIGURE 2. External Nulling of Offset Voltage.

BURR-BROWN®

OPA104

For a /883B version of this product, see OPA106/883B in the Military Products section.

Ultra-Low Bias Current Low Drift FET Input OPERATIONAL AMPLIFIER

FEATURES

- SPECIFICATIONS GUARANTEED OVER TEMPERATURE
- ULTRA-LOW BIAS CURRRENT, 75fA, max
- HIGH INPUT IMPEDANCE, $10^{15}\Omega$
- LOW DRIFT, $10\mu V/°C$, max
- LOW OFFSET VOLTAGE, 0.5mV, max
- LOW QUIESCENT CURRENT, 1.5mA, max

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS SUCH AS:
  - photo current detectors
  - pH electrodes
  - biological probes/transducers

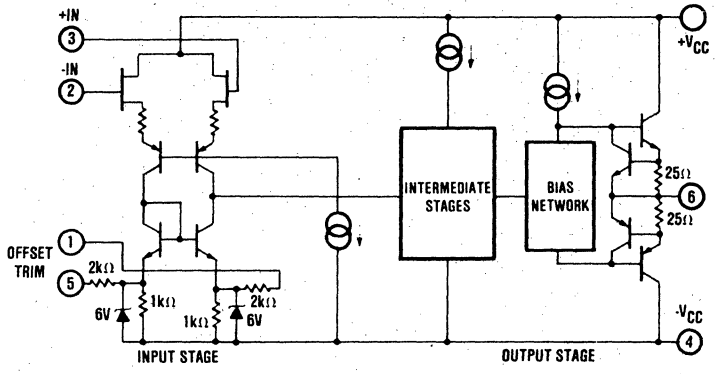
DESCRIPTION

The OPA104 is a precision low bias current operational amplifier. Guaranteed low initial offset voltage (0.5mV, max) and associated drift versus temperature ($10\mu V/°C$, max) is achieved by laser-adjusting the amplifier during manufacturing. The low offset, in addition to the guaranteed low bias current (75fA, max), allows greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristics of the OPA104 include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or ambient temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidently shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA104 allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL	OPA104AM			OPA104BM			OPA104CM			
PARAMETERS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OPEN-LOOP GAIN, DC, V_{OUT} = ±10V										
Rated Load, $R_L \geq 2k\Omega$	100	106		•	•		•	•		dB
$R_L \geq 10k\Omega$	106	112		•	•		•	•		dB
T_A = -25°C to +85°C, $R_L \geq 2k\Omega$	92	100		•	•		•	•		dB
RATED OUTPUT										
Voltage at R_L = 2kΩ, T_A = -25°C to +85°C	±10	±12		•	•		•	•		V
R_L = 10kΩ, T_A = -25°C to +85°C	±12	±13		•	•		•	•		V
Current T_A = -25°C to +85°C	±5	±10		•	•		•	•		mA
Output Impedance		3			•			•		kΩ
Load Capacitance(1)	500	1000		•	•		•	•		pF
Short Circuit Current	10	25		•	•		•	•		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			•			•		MHz
Full Power Response	25	35		•	•		•	•		kHz
Slew Rate	1.6	2.2		•	•		•	•		V/µsec
Settling Time (0.1%), Av = -1, V_O = 0 to ±10V		6			•			•		µsec
Settling Time (0.01%), Av = -1, V_O = 0 to ±10V		18			•			•		µsec
Overload Recovery(2), 50% overdrive		4	15		•	•		•	•	µsec
INPUT OFFSET VOLTAGE										
Initial Offset, T_A = +25°C		±200	±1000		±200	±500		±200	±500	µV
vs Temperature, T_A = -25°C to +85°C		±15	±25		±10	±15		±5	±10	µV/°C
vs Supply Voltage, T_A = +25°C		±10	±100		•	•		•	•	µV/V
vs Supply Voltage, T_A = -25°C to +85°C		±20	±150		•	•		•	•	µV/V
INPUT BIAS CURRENT(3)										
Initial Bias, T_A = +25°C			-300			-150			-75	fA
vs Supply Voltage		1				•			•	fA/V
INPUT DIFFERENCE CURRENT										
Initial Difference, T_A = +25°C		±80			±80			±40		fA
INPUT IMPEDANCE										
Differential		10^{14} || 0.5			•			•		Ω || pF
Common-mode		10^{15} || 1.0			•			•		Ω || pF
INPUT NOISE										
Voltage, f_o = 10Hz		75			•			•		nV/√Hz
f_o = 100Hz		55			•			•		nV/√Hz
f_o = 1kHz		35			•			•		nV/√Hz
f_o = 10kHz		35			•			•		nV/√Hz
f_B = 0.1Hz to 10Hz		6			•			•		µV, p-p
Current, f_B = 0.1Hz to 10Hz		3			•			•		fA, p-p
f_B = 10Hz to 10kHz		10			•			•		fA, rms
f_o = 1kHz		0.25			•			•		fA/√Hz
INPUT VOLTAGE RANGE										
Differential	±20			•			•			V
Common-mode, T_A = -25°C to +85°C	±10	±12		•	•		•	•		V
Common-mode Rejection at V_{IN} = ±10V	66	76		•	•		80	90		dB
Maximum Safe Input Voltage		±Vs			•			•		V
POWER SUPPLY										
Rated Voltage		±15			•			•		VDC
Voltage Range, derated performance	±5		±20	•		•	•		•	VDC
Current, quiescent T_A = -25°C to +85°C		1.0	1.5		•	•		•	•	mA
TEMPERATURE RANGE (ambient)										
Specification	-25		+85	•		•	•		•	°C
Operating	-55		+125	•		•	•		•	°C
Storage	-65		+150	•		•	•		•	°C
θ junction - ambient		235			•			•		°C/W

*Specifications same as for OPA104AM.

NOTES:

1. Stability guaranteed with load capacitance ≤ 500pF
2. Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.
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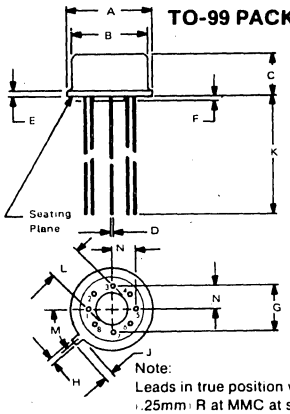
MECHANICAL

TO-99 PACKAGE



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N	.095	.105	2.41	2.67

Weight: 1 gram

Note:
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Pin numbers shown for reference only. Numbers may not be marked on package

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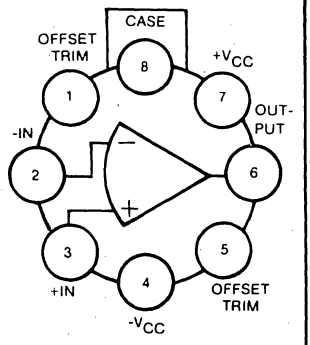
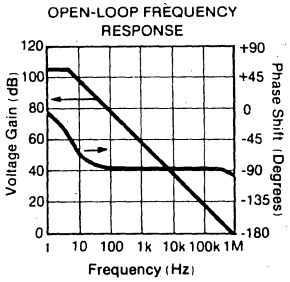
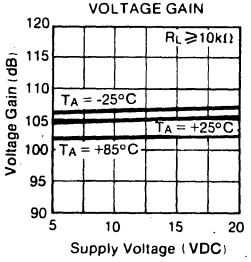
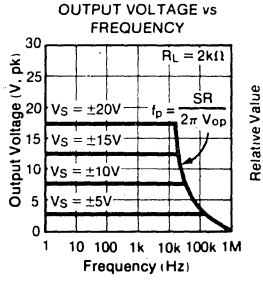


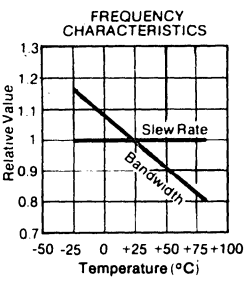
(TOP VIEW)

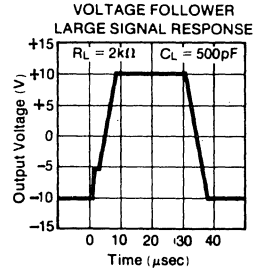
TYPICAL PERFORMANCE CURVES

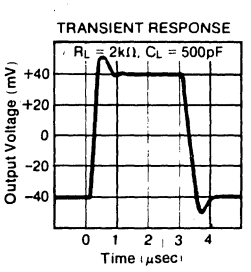


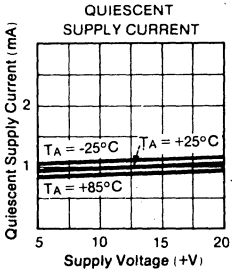


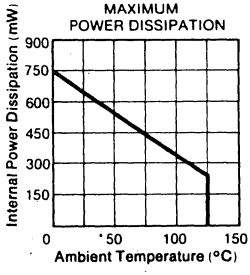


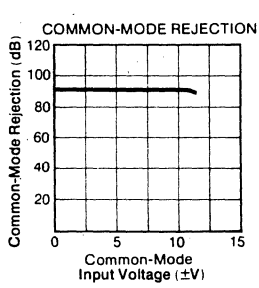


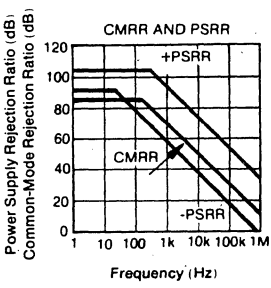


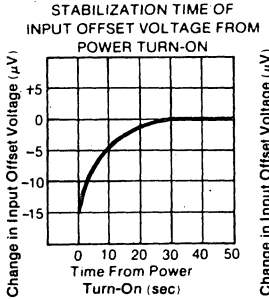


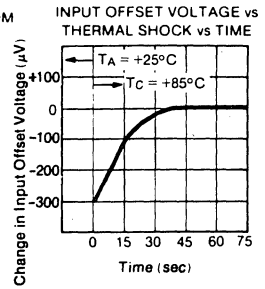












APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the OPA104. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA104 is approximately 20 seconds (see Typical Performance Curves).

GUARDING AND SHIELDING

The ultra-low bias current and high input impedance of the OPA104 are well-suited to a number of stringent applications. However, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA104.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA104. To avoid leakage problems, it is recommended that the signal input lead of the OPA104 be wired to a Teflon standoff. If the OPA104 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 1 illustrates the use of the guard.

OFFSET VOLTAGE ADJUSTMENT

Although the OPA104 has a low initial offset voltage (500μV), some applications may require external nulling of this small offset. Figure 2 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C, for every 100μV of offset adjustment.

TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. Noise calculations are often important when using low current photodiodes.

CR1 is a PIN photodiode connected in the photovoltaic mode (no bias voltage) which produces an output current i_{in} when exposed to the light, λ.

A more complete circuit is shown in Figure 4. The values shown for C_1 and R_1 are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of C_2 (0.5pF to 2pF) is what would be typically required to compensate for the pole generated by the capacitance at the input node. A larger value of C_2 could be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

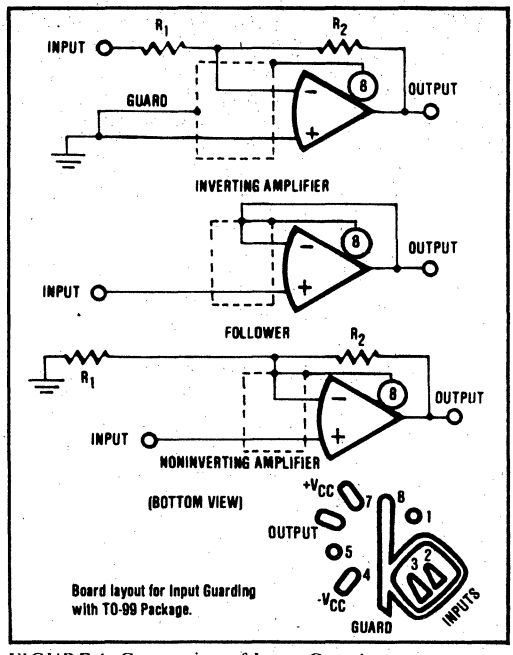


FIGURE 1. Connection of Input Guard.

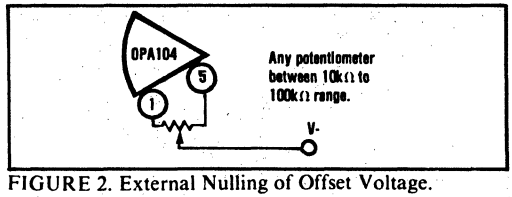


FIGURE 2. External Nulling of Offset Voltage.

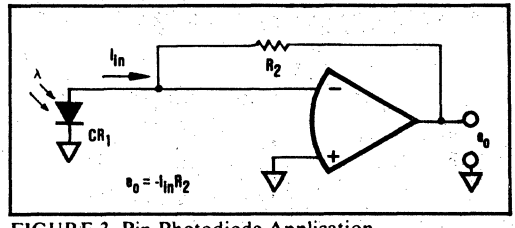


FIGURE 3. Pin Photodiode Application.

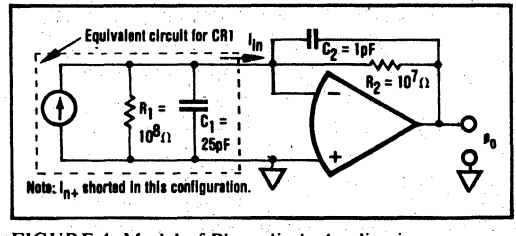


FIGURE 4. Model of Photodiode Application.

BURR-BROWN®

OPA111

Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 100% tested, 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW BIAS CURRENT: 1pA max
- LOW OFFSET: 250μV max
- LOW DRIFT: 1μV/°C max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 100dB min

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- OPTOELECTRONICS
- MEDICAL EQUIPMENT—CAT SCANNER
- RADIATION HARD EQUIPMENT

DESCRIPTION

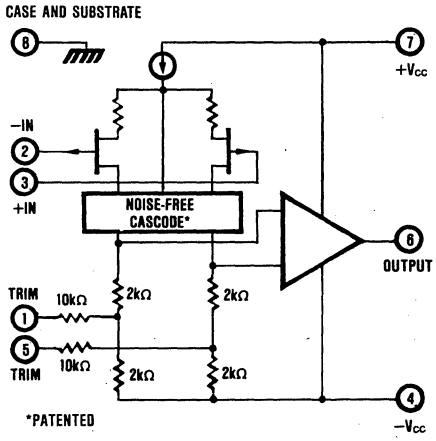
The OPA111 is a precision monolithic dielectrically-isolated FET (*Difet*®) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.



OPA111 SIMPLIFIED CIRCUIT

BIFET®National Semiconductor Corp., *Difet*® Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA111AM MIN	OPA111AM TYP	OPA111AM MAX	OPA111BM MIN	OPA111BM TYP	OPA111BM MAX	OPA111SM MIN	OPA111SM TYP	OPA111SM MAX	UNITS
INPUT											
NOISE											
Voltage, f_o = 10Hz	100% tested		40	80		30	60		40	80	nV/√Hz
f_o = 100Hz	100% tested		15	40		11	30		15	40	nV/√Hz
f_o = 1kHz	100% tested		8	15		7	12		8	15	nV/√Hz
f_o = 10kHz	100% tested		6	8		6	8		6	8	nV/√Hz
f_B = 10Hz to 10kHz	100% tested		0.7	1.2		0.6	1.0		0.7	1.2	µV, rms
f_B = 0.1Hz to 10Hz	(1)		1.6	3.3		1.2	2.5		1.6	3.3	µV, p-p
Current, f_B = 0.1Hz to 10Hz	(1)		9.5	15		7.5	12		9.5	15	fA, p-p
f_o = 0.1Hz thru 20kHz	(1)		0.5	0.8		0.4	0.6		0.5	0.8	fA/√Hz
OFFSET VOLTAGE[2]											
Input Offset Voltage	V_{cm} = 0VDC		±100	±500		±50	±250		±100	±500	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±2	±5		±0.5	±1		±2	±5	µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	90	110		100	110		90	110		dB
			±3	±31		±3	±10		±3	±31	µV/V
BIAS CURRENT[2]											
Input Bias Current	V_{cm} = 0VDC		±0.8	±2		±0.5	±1		±0.8	±2	pA
OFFSET CURRENT[2]											
Input Offset Current	V_{cm} = 0VDC		±0.5	±1.5		±0.25	±0.75		±0.5	±1.5	pA
IMPEDANCE											
Differential			10^{13} ‖ 1			10^{13} ‖ 1			10^{13} ‖ 1		Ω ‖ pF
Common-Mode			10^{14} ‖ 3			10^{14} ‖ 3			10^{14} ‖ 3		Ω ‖ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		100	110		90	110		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	114	125		120	125		114	125		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			2			2			2		MHz
Full Power Response	20V p-p, R_L = 2k	16	32		16	32		16	32		kHz
Slew Rate	V_o = ±10V, R_L = 2k	1	2		1	2		1	2		V/µsec
Settling Time, 0.1%	Gain = −1, R_L = 2k		6			6			6		µsec
0.01%	10V step		10			10			10		µsec
Overload Recovery, 50% Overdrive[3]	Gain = −1		5			5			5		µsec
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11	±12		±11	±12		±11	±12		V
Current Output	V_o = ±10VDC	±5.5	±10		±5.5	±10		±5.5	±10		mA
Output Resistance	DC, open loop		100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_o = 0mADC		2.5	3.5		2.5	3.5		2.5	3.5	mA
TEMPERATURE RANGE											
Specification	Ambient temp.	−25		+85	−25		+85	−55		+125	°C
Operating	Ambient temp.	−55		+125	−55		+125	−55		+125	°C
Storage	Ambient temp.	−65		+150	−65		+150	−65		+150	°C
θ Junction-Ambient			200			200			200		°C/W

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

ELECTRICAL [FULL TEMPERATURE RANGE SPECIFICATIONS]

At V_{CC} = ±15VDC and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA111AM MIN	OPA111AM TYP	OPA111AM MAX	OPA111BM MIN	OPA111BM TYP	OPA111BM MAX	OPA111SM MIN	OPA111SM TYP	OPA111SM MAX	UNITS
TEMPERATURE RANGE											
Specification Range	Ambient temp.	−25		+85	−25		+85	−55		+125	°C
INPUT											
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{cm} = 0VDC		±220	±1000		±110	±500		±300	±1500	µV
Average Drift			±2	±5		±0.5	±1		±2	±5	µV/°C
Supply Rejection	V_{CC} − ±10V to ±18V	86	100		90	100		86	100		dB
			±10	±50		±10	±32		±10	±50	µV/V
BIAS CURRENT[1]											
Input Bias Current	V_{cm} = 0VDC		±50	±250		±30	±130		±820	±4100	pA
OFFSET CURRENT[1]											
Input Offset Current	V_{cm} = 0VDC		±30	±200		±15	±100		±510	±3100	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	100		90	100		86	100		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	110	120		114	120		110	120		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±10.5	±11		±11	±11		±11	±11		V
Current Output	V_o = ±10VDC	±5.25	±10		±5.25	±10		±5.25	±10		mA
Short Circuit Current	V_o = 0VDC	10	40		10	40		10	40		mA
POWER SUPPLY											
Current, Quiescent	I_o = 0mADC		2.5	3.5		2.5	3.5		2.5	3.5	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES:
(1) Packages must be derated based on θ_{JC} = 150°C/W or θ_{JA} = 200°C/W.
(2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to +18V > V_{IN} > $-V_{CC}$ −6V. See Figure 2.
(3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ORDERING INFORMATION

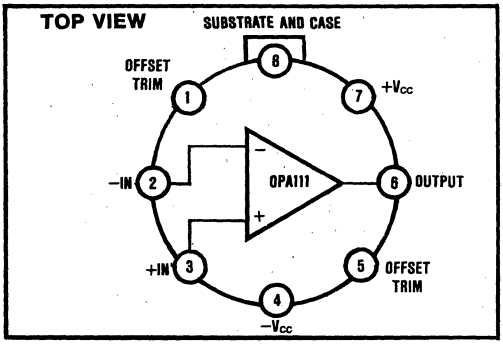
OPA111 X M

Basic model number

Performance grade
A, B = −25°C to +85°C
S = −55°C to +125°C

Package code
M = TO-99 metal can

CONNECTION DIAGRAM

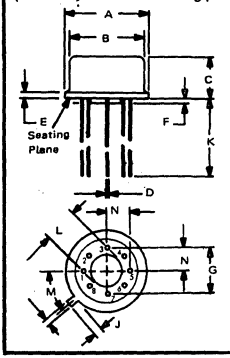


MECHANICAL "M" PACKAGE TO-99 (Hermetic)

NOTE:
Leads in true position within .010" (.25mmR) at MMC at seating plate.

Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

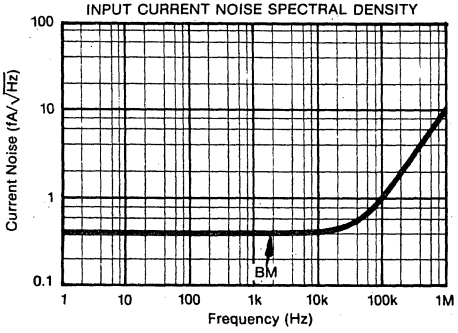


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

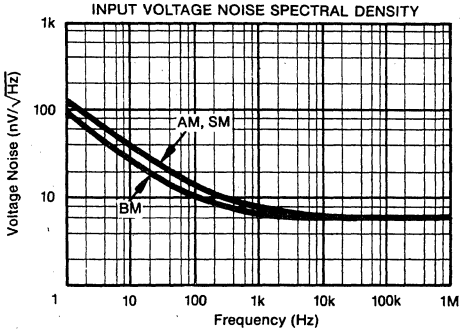
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

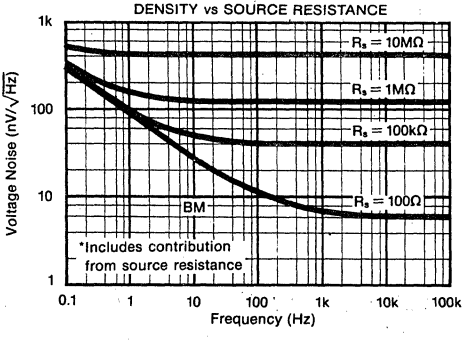
INPUT CURRENT NOISE SPECTRAL DENSITY



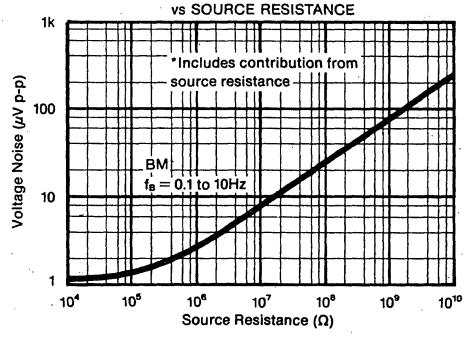
INPUT VOLTAGE NOISE SPECTRAL DENSITY



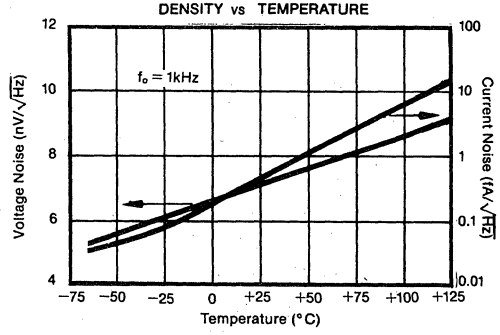
TOTAL* INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



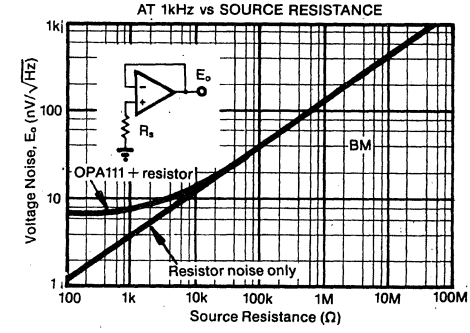
TOTAL* INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



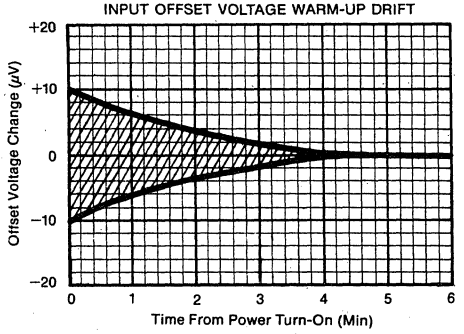
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



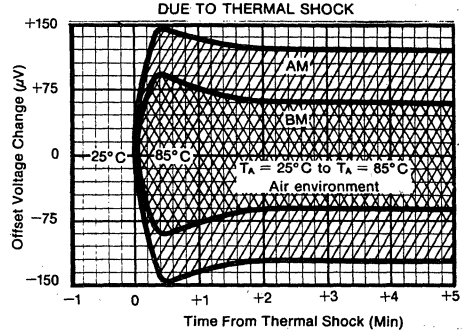
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



INPUT OFFSET VOLTAGE WARM-UP DRIFT



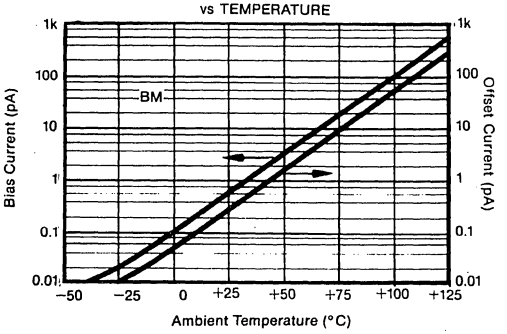
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



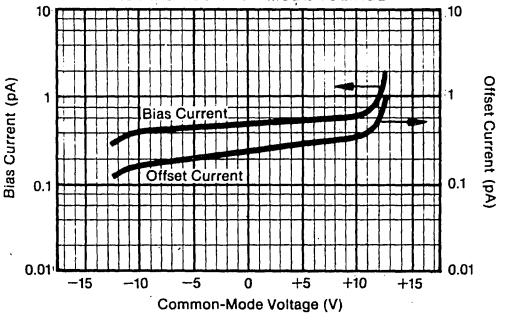
TYPICAL PERFORMANCE CURVES [CONT]

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

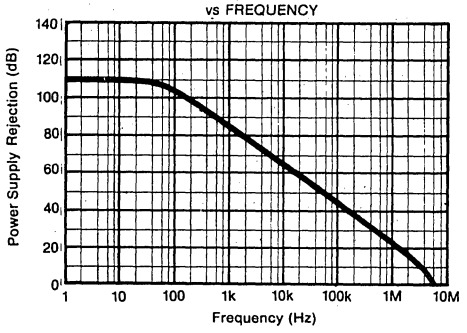
BIAS AND OFFSET CURRENT vs TEMPERATURE



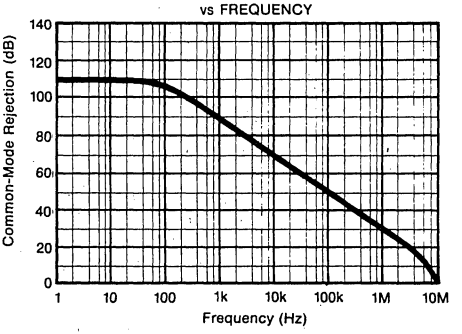
BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



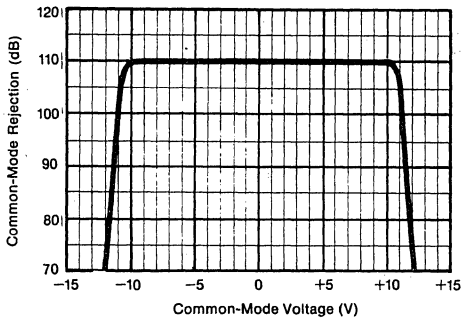
POWER SUPPLY REJECTION vs FREQUENCY



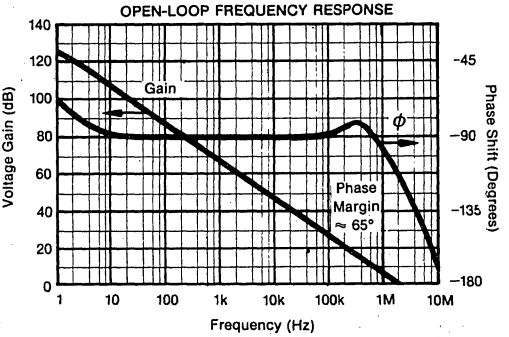
COMMON-MODE REJECTION vs FREQUENCY



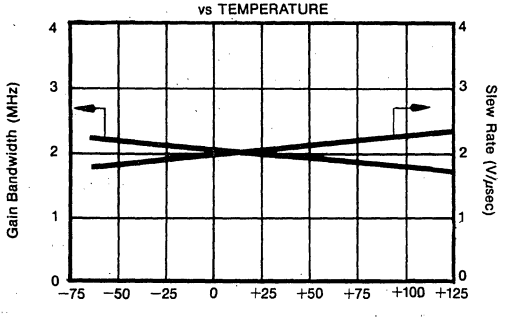
COMMON-MODE REJECTION vs INPUT COMMON MODE VOLTAGE



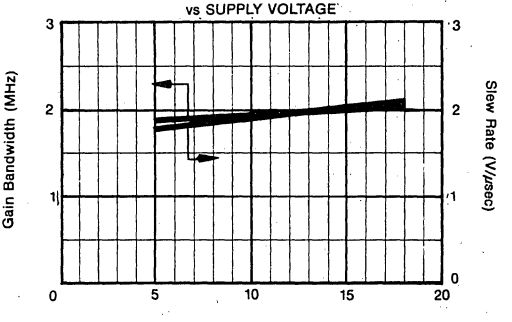
OPEN-LOOP FREQUENCY RESPONSE



GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



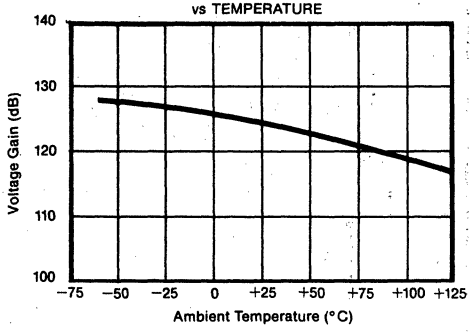
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



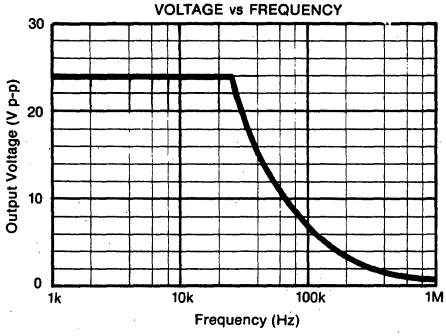
TYPICAL PERFORMANCE CURVES [CONT]

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

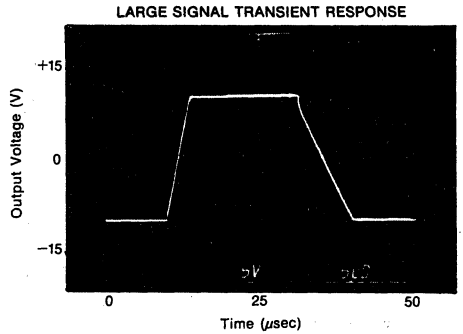
OPEN-LOOP GAIN vs TEMPERATURE



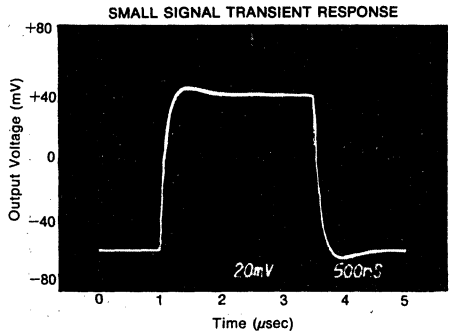
MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY



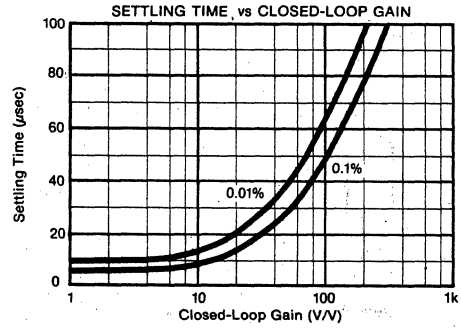
LARGE SIGNAL TRANSIENT RESPONSE



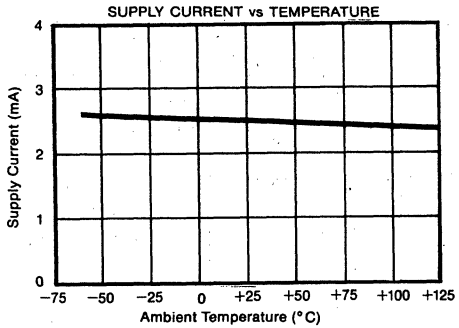
SMALL SIGNAL TRANSIENT RESPONSE



SETTLING TIME vs CLOSED-LOOP GAIN



SUPPLY CURRENT vs TEMPERATURE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA111 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3μV/°C for each 100μV of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA111 can replace most other amplifiers by leaving the external null circuit unconnected.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their

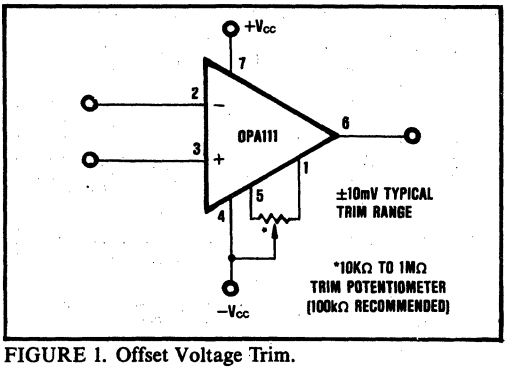


FIGURE 1. Offset Voltage Trim.

inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the ***Difet*** OPA111 requires input current limiting resistors only if its input voltage is greater than 6 volts more negative than $=V_{CC}$. A 10kΩ series resistor will limit input current to a safe level with up to ±15V input levels even if both supply voltages are lost.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

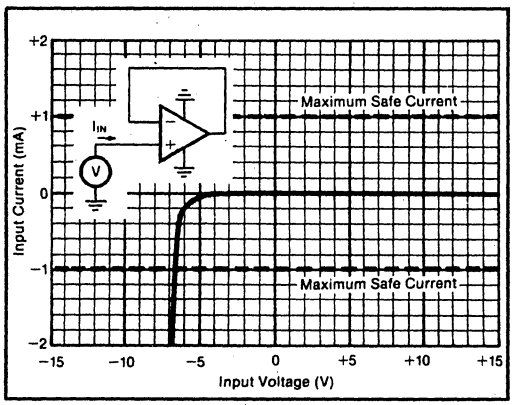


FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is rquired to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias curent of the OPA111. To avoid leakage problems, it is recommended that the signal input lead of the OPA111 be wired to a Teflon standoff. If the OPA111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 3).

If guarding is not required, pin 8 (case) should be connected to ground.

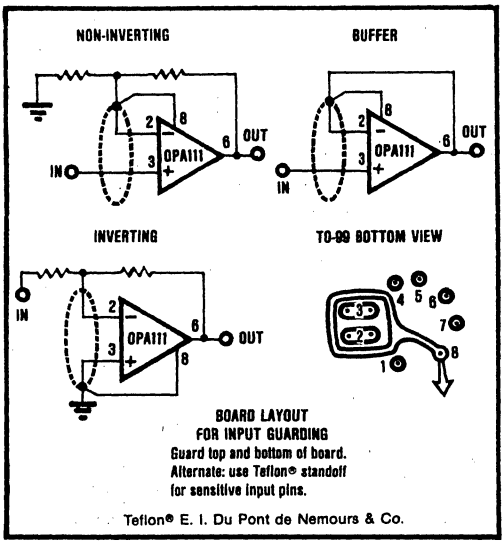


FIGURE 3. Connection of Input Guard.

NOISE: FET VERSUS BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the OPA111 will have lower total noise than an OP-27 (see Figure 4).

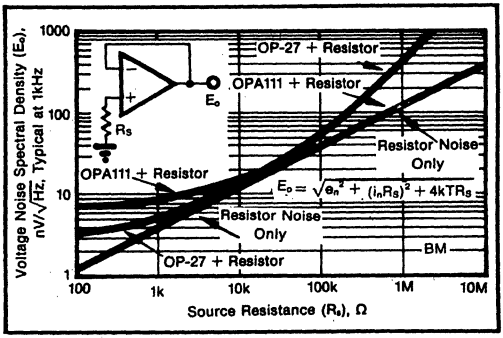


FIGURE 4. Voltage Noise Spectral Density Versus Source Resistance.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 5). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA111 is not compromised by common-mode voltage.

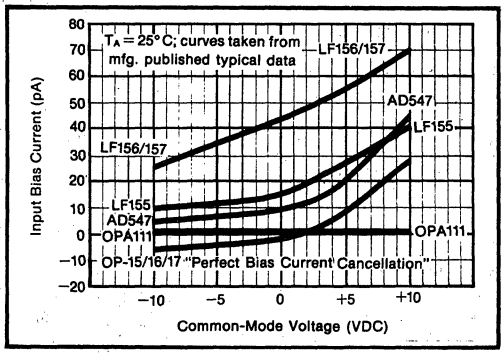


FIGURE 5. Input Bias Current Versus Common-Mode Voltage.

APPLICATIONS CIRCUITS

Figures 6 through 18 are circuit diagrams of various applications for the OPA111.

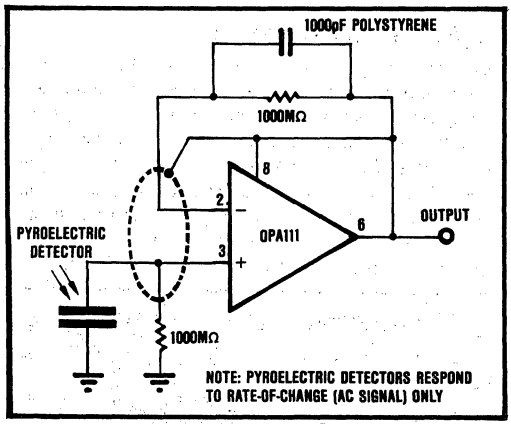


FIGURE 6. Pyroelectric Infrared Detector.

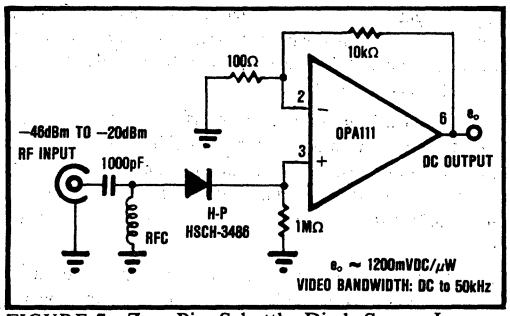


FIGURE 7. Zero-Bias Schottky Diode Square-Law RF Detector.

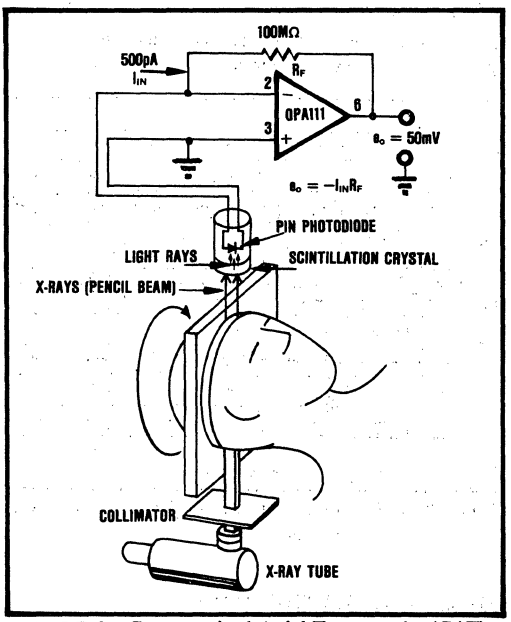


FIGURE 8. Computerized Axial Tomography (CAT) Scanner Channel Amplifier.

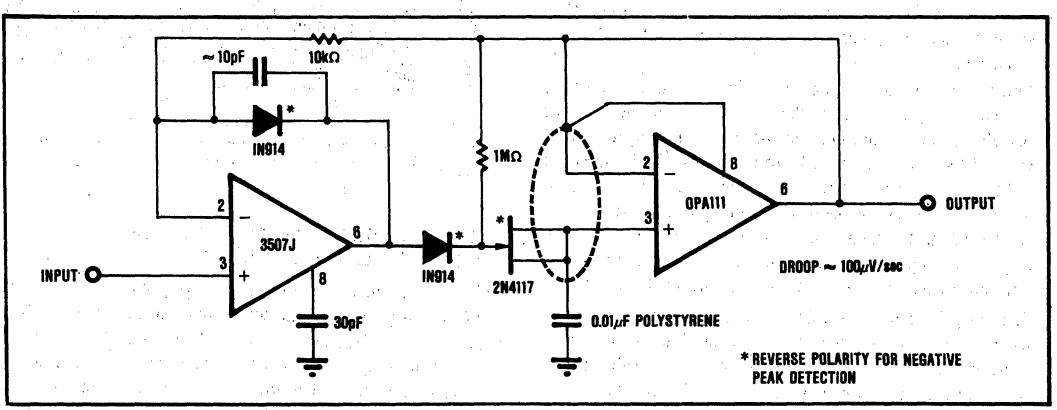


FIGURE 9. Low-Droop Positive Peak Detector.

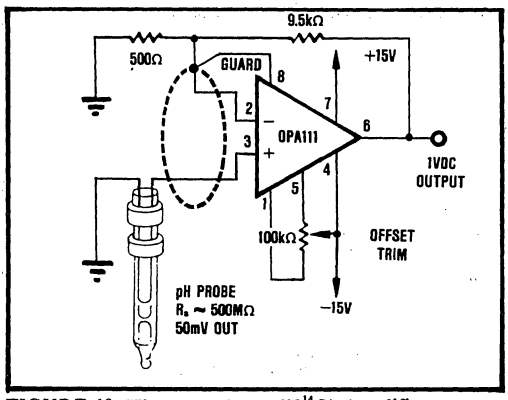


FIGURE 10. High Impedance ($10^{14}\Omega$) Amplifier.

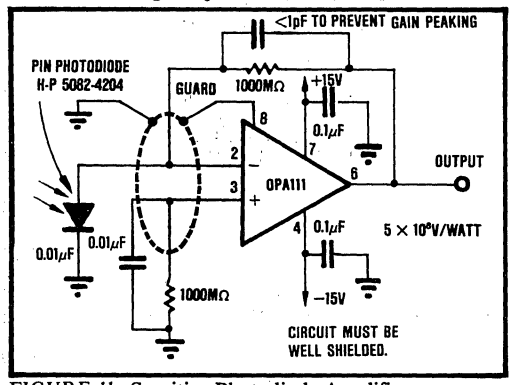


FIGURE 11. Sensitive Photodiode Amplifier.

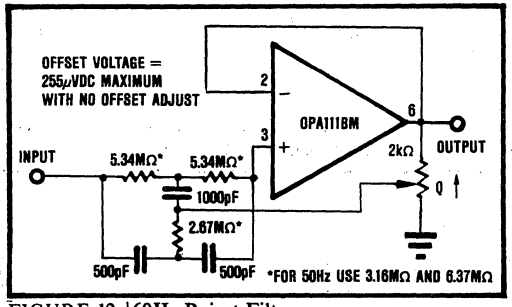


FIGURE 12. 60Hz Reject Filter.

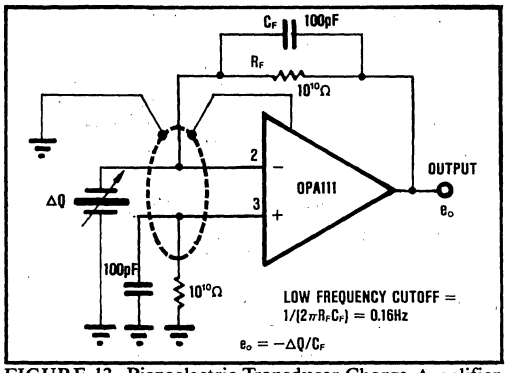


FIGURE 13. Piezoelectric Transducer Charge Amplifier.

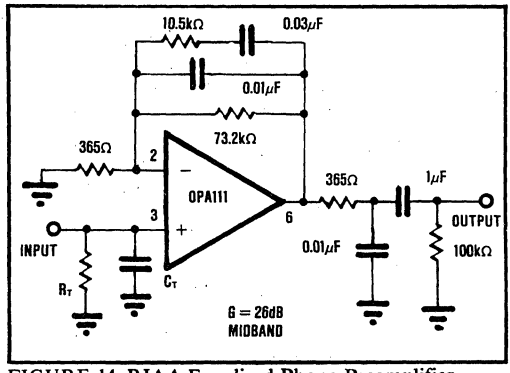


FIGURE 14. RIAA Equalized Phono Preamplifier.

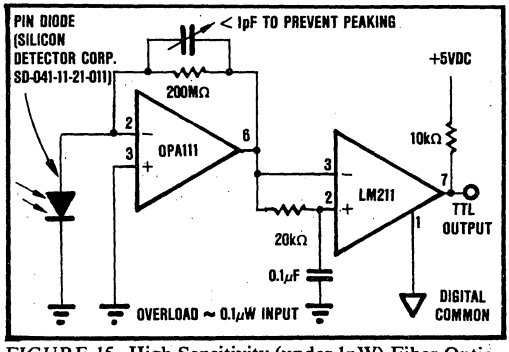


FIGURE 15. High Sensitivity (under 1nW) Fiber Optic Receiver for 9600 Baud Manchester Data.

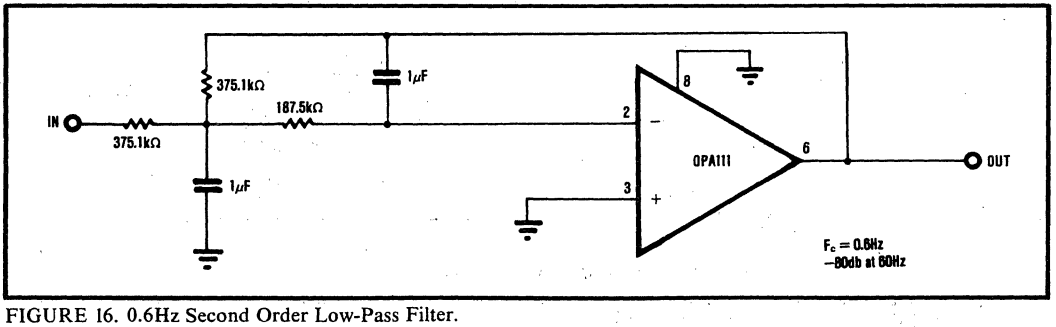


FIGURE 16. 0.6Hz Second Order Low-Pass Filter.

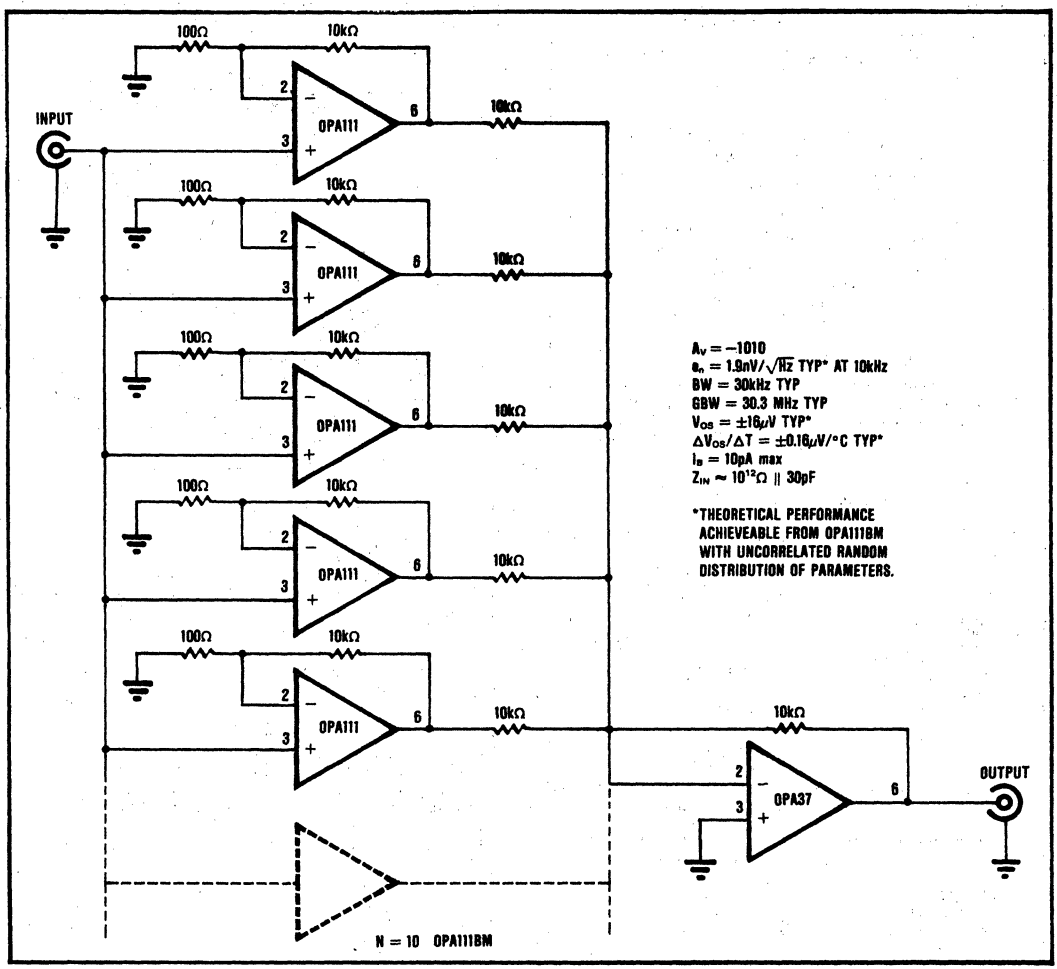


FIGURE 17. 'N' Stage Parallel-Input Amplifier For Reduced Relative Amplifier Noise At The Output.

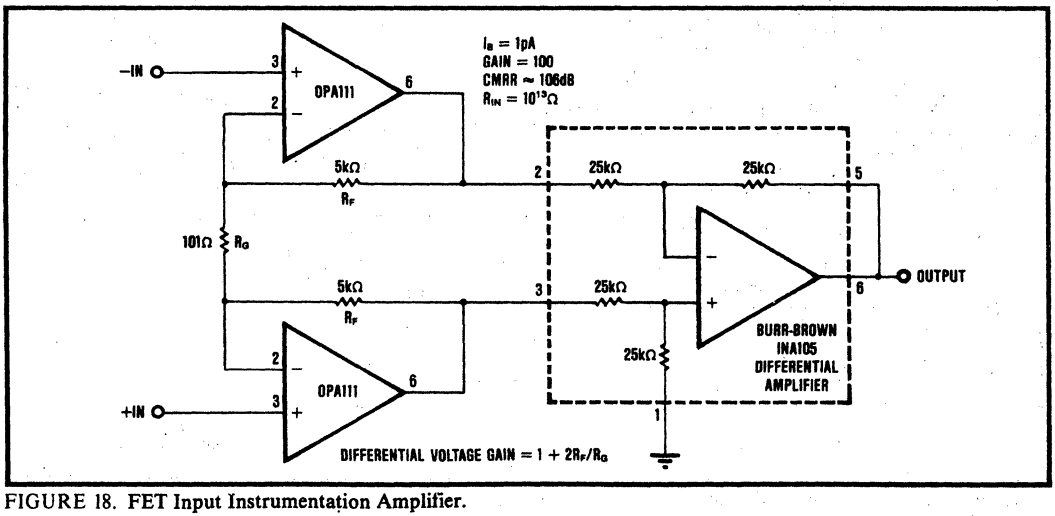


FIGURE 18. FET Input Instrumentation Amplifier.

BURR-BROWN®

OPA111HT

Wide Temperature Range *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- FULLY SPECIFIED OVER −55°C to +200°C
- LOW BIAS CURRENT
- LOW NOISE
- MONOLITHIC
- HERMETIC TO-99 PACKAGE
- 100% BURN-IN AT +200°C

APPLICATIONS

- WELL LOGGING
- DOWN-HOLE INSTRUMENTATION
- ENGINE CONTROLS
- EMISSIONS CONTROLS
- EXTREMELY SEVERE ENVIRONMENT
- RADIATION HARD EQUIPMENT

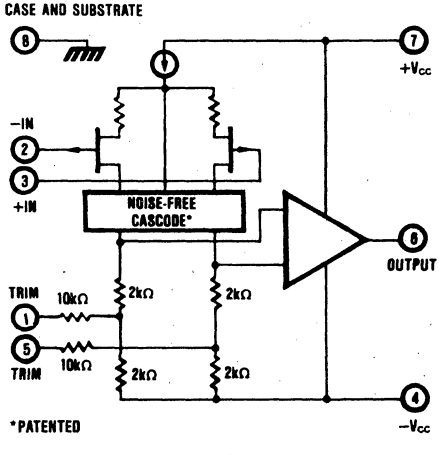
DESCRIPTION

The OPA111HT is a precision monolithic dielectrically-isolated FET (*Difet*®) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

The OPA111HT is tested and guaranteed over an extremely wide temperature range: −55°C to +200°C. In addition, it has demonstrated an ability to withstand a total dose of 10×10^6 RAD (Si) of 2.5MeV electrons, and a neutron fluence of 1×10^{13}, 1MeV equivalent n/cm^2.

Laser trimmed thin-film resistors give very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.



OPA111HT SIMPLIFIED CIRCUIT

Difet® Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC, T_A = indicated temperature, Pin 8 connected to ground.

PARAMETER	CONDITIONS	+25°C			−55°C TO +125°C			+200°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE											
Voltage, f_O = 10Hz	(1)		40			50			65		nV/√Hz
f_O = 100Hz	(1)		15			17			19		nV/√Hz
f_O = 1kHz	(1)		8			9			9.5		nV/√Hz
f_O = 10kHz			6			7			8		nV/√Hz
f_B = 10Hz to 10kHz	(1)		0.7			0.8			0.9		μV, rms
f_B = 0.1Hz to 10Hz			1.6								μV, p-p
Current, f_B = 0.1Hz to 10Hz			9.5								fA, p-p
f_O = 0.1Hz thru 20kHz			0.5								fA/√Hz
OFFSET VOLTAGE[2]											
Input Offset Voltage	V_{CM} = 0VDC		±100	±500		±300	±2mV		±1.8mV	±5mV	μV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}					±2			±8		μV/°C
Supply Rejection	V_{CC} = ±9V to ±15V	90	110		86	100		80	97		dB
			±3	±31		±10	±50		±14	±100	μV/V
BIAS CURRENT[2][3]											
Input Bias Current	V_{CM} = 0VDC		0.8	2		820	2.1nA		65nA	150nA	pA
OFFSET CURRENT[2][3]											
Input Offset Current	V_{CM} = 0VDC		±0.5	±1.5		±510	±1.6nA		±5nA	±50nA	pA
IMPEDANCE											
Differential			10^{13} ‖ 1								Ω ‖ pF
Common-Mode			10^{14} ‖ 3								Ω ‖ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		86	100		80	95		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	114	125		108	120		90	99		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			2			1.5			0.6		MHz
Full Power Response	20V p-p, R_L = 2kΩ		32			17			11		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	2			1.1			0.7		V/μs
Settling Time, 0.1%	Gain = −1, R_L = 2kΩ		6								μs
0.01%	10V step		10								μs
Overload Recovery, 50% Overdrive[4]	Gain = −1		5								μs
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±10	±13		±10	±12.9		±10	±12.7		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, open loop		100								Ω
Load Capacitance Stability	Gain = +1		1000								pF
Short Circuit Current		10	40								mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18							VDC
Current, Quiescent	I_O = 0mADC		2.3	3.5		2.4	3.5		2.4	3.7	mA
TEMPERATURE RANGE											
Specification[5]	Ambient temp.	−55		+200							°C
Operating	Ambient temp.	−65		+225							°C
Storage	Ambient temp.	−65		+225							°C
θ Junction-Ambient			175								°C/W

NOTES: (1) Noise testing available—inquire. (2) Offset voltage, offset current, and bias current on grade HT are also guaranteed with the units fully warmed up. (3) Bias current and offset current double approximately every 10°C up to about 130°C. (4) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (5) 100% tested at −55°C, +25°C, and +200°C using forced-air environment. +125°C specification is guaranteed by design.

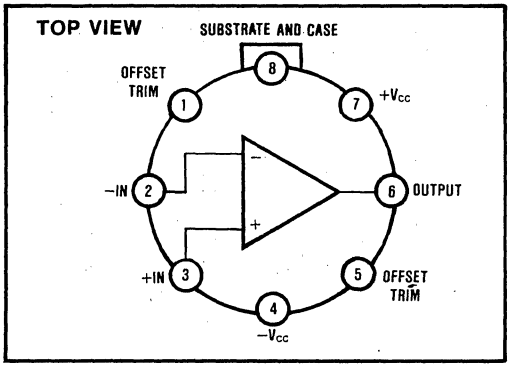
ORDERING INFORMATION

OPA111 HT

Basic Model Number

Performance Grade
HT = −55°C to +200°C

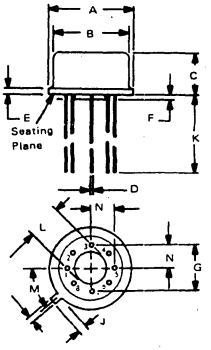
CONNECTION DIAGRAM



MECHANICAL

"M" PACKAGE TO-99 (Hermetic)

NOTE:
Leads in true position within .010" (.25mmR) at MMC at seating plane.



Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

ABSOLUTE MAXIMUM RATINGS

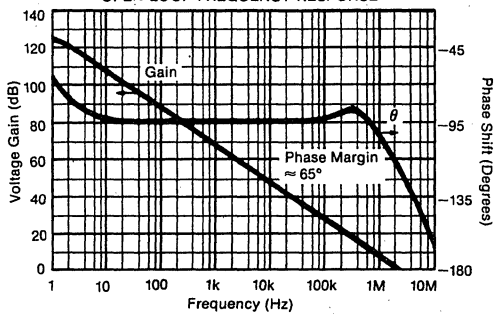
Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	−65°C to +225°C
Operating Temperature Range	−65°C to +225°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[2]	Continuous
Junction Temperature	+250°C

NOTES: (1) Packages must be derated based on θ_{JC} = 45°C/W or θ_{JA} = 175°C/W. (2) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

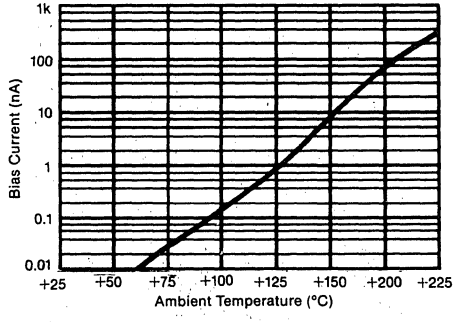
TYPICAL PERFORMANCE CURVES

T_A = +25° C, V_{CC} = ±15VDC unless otherwise noted.

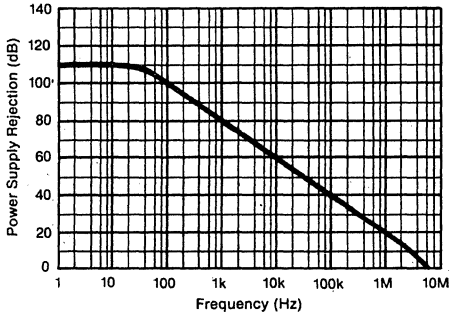
OPEN-LOOP FREQUENCY RESPONSE



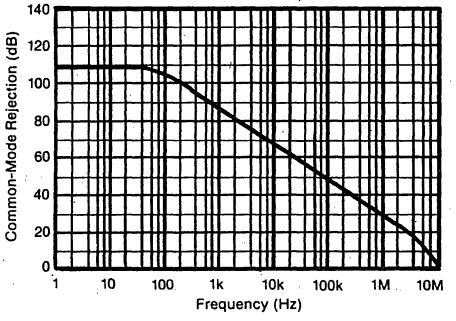
BIAS AND OFFSET CURRENT vs TEMPERATURE

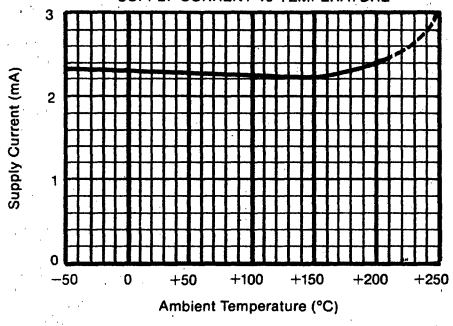


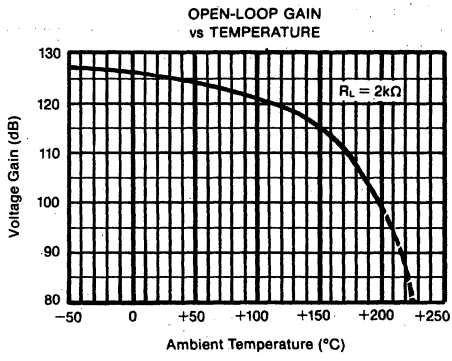
POWER SUPPLY REJECTION vs FREQUENCY

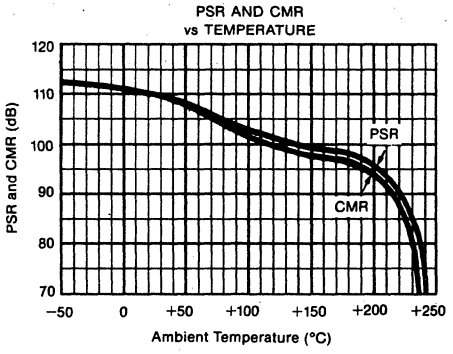


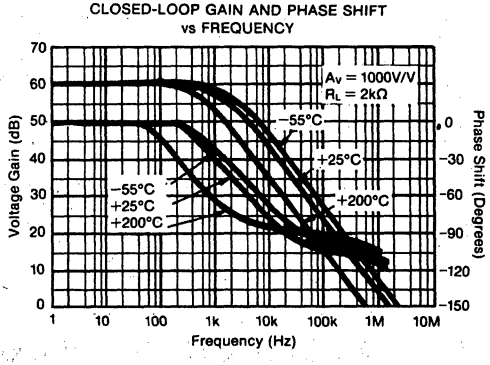
COMMON-MODE REJECTION vs FREQUENCY

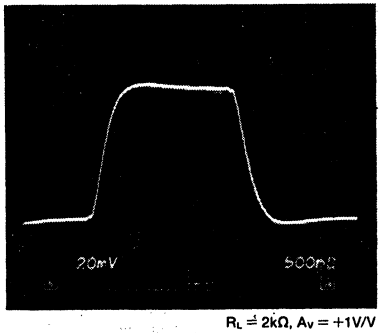




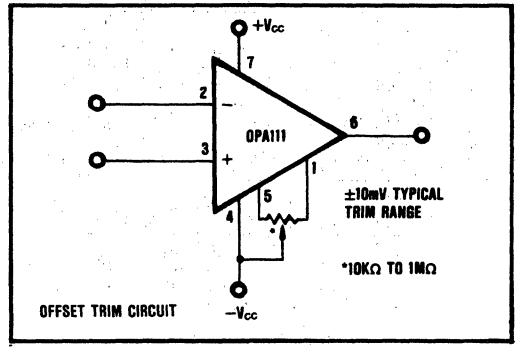








$R_L \doteq 2k\Omega$, $A_V = +1V/V$



APPLICATIONS INFORMATION

To preserve this amplifier's low bias current, pin 8 (case connection) should be driven in a guard mode or it should be connected to common. Recommended guard circuits are shown in the standard OPA111 data sheet.

The OPA111HT is unity-gain stable over its full −55°C to +200°C temperature range. The OPA111HT is an extremely wide temperature version of the standard Burr-Brown model OPA111. It is built and tested for severe service applications.

Eutectic die attach is used exclusively for the OPA111HT. Hermeticity is assured by 100% fine leak testing.

Units are 100% burned-in for 28 hours at +200°C for increased reliability.

BURR-BROWN®

OPA121

Low Cost Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 6nV/$\sqrt{Hz}$ typ at 10kHz
- LOW BIAS CURRENT: 5pA max
- LOW OFFSET: 2mV max
- LOW DRIFT: 3μV/°C typ
- HIGH OPEN-LOOP GAIN: 110dB min
- HIGH COMMON-MODE REJECTION: 86dB min

APPLICATIONS

- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- MEDICAL EQUIPMENT
- RADIATION HARD EQUIPMENT

DESCRIPTION

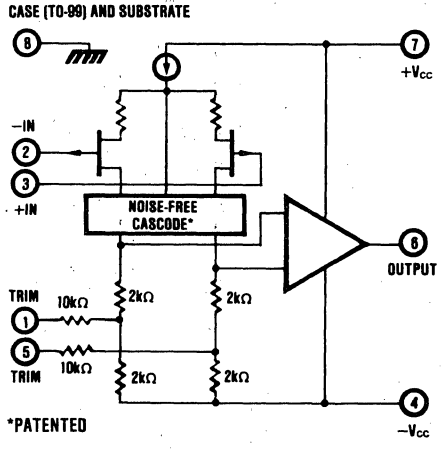
The OPA121 is a precision monolithic dielectrically-isolated FET (*Difet*®) operational amplifier. Outstanding performance characteristics are now available for low-cost applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise. noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.



OPA121 SIMPLIFIED CIRCUIT

BIFET® National Semiconductor Corp., *Difet*® Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA121KM			OPA121KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
NOISE								
Voltage, f_o = 10Hz	[1]		40			50		nV/√Hz
f_o = 100Hz	[1]		15			18		nV/√Hz
f_o = 1kHz	[1]		8			10		nV/√Hz
f_o = 10kHz	[1]		6			7		nV/√Hz
f_B = 10Hz to 10kHz	[1]		0.7			0.8		μV, rms
f_B = 0.1Hz to 10Hz	[1]		1.6			2		μV, p-p
Current, f_B = 0.1Hz to 10Hz	[1]		15			21		fA, p-p
f_o = 0.1Hz thru 20kHz	[1]		0.8			1.1		fA/√Hz
OFFSET VOLTAGE[2]								
Input Offset Voltage	V_{cm} = 0VDC		±0.5	±2		±0.5	±3	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±10		±3	±10	μV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	86	104		86	104		dB
			±6	±50		±6	±50	μV/V
BIAS CURRENT[2]								
Input Bias Current	V_{cm} = 0VDC		±1	±5		±1	±10	pA
OFFSET CURRENT[2]								
Input Offset Current	V_{cm} = 0VDC		±0.7	±4		±0.7	±8	pA
IMPEDANCE								
Differential			10^{13} ‖ 1			10^{13} ‖ 1		Ω ‖ pF
Common-Mode			10^{14} ‖ 3			10^{14} ‖ 3		Ω ‖ pF
VOLTAGE RANGE								
Common-Mode Input Range		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	104		82	100		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	110	120		106	114		dB
FREQUENCY RESPONSE								
Unity Gain, Small Signal			2			2		MHz
Full Power Response	20V p-p, R_L = 2kΩ		32			32		kHz
Slew Rate	V_o = ±10V, R_L = 2kΩ		2			2		V/μsec
Settling Time, 0.1%	Gain = −1, R_L = 2kΩ		6			6		μsec
0.01%	10V step		10			10		μsec
Overload Recovery, 50% Overdrive[3]	Gain = −1		5			5		μsec
RATED OUTPUT								
Voltage Output	R_L = 2kΩ	±11	±12		±11	±12		V
Current Output	V_o = ±10VDC	±5.5	±10		±5.5	±10		mA
Output Resistance	DC, open loop		100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000		pF
Short Circuit Current		10	40		10	40		mA
POWER SUPPLY								
Rated Voltage			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	VDC
Current, Quiescent	I_o = 0mADC		2.5	4.0		2.5	4.5	mA
TEMPERATURE RANGE								
Specification	Ambient temp.	0		+70	0		+70	°C
Operating	Ambient temp.	−40		+85	−25		+85	°C
Storage	Ambient temp.	−65		+150	−55		+125	°C
θ Junction-Ambient			200			150		°C/W

NOTES: (1) Sample tested. (2) Offset voltage, offset current, and bias current are also specified with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

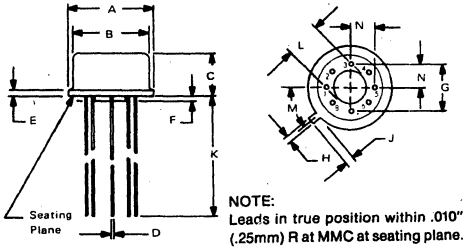
At V_{CC} = ±15VDC and $T_A = +T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA121KM MIN	OPA121KM TYP	OPA121KM MAX	OPA121KP MIN	OPA121KP TYP	OPA121KP MAX	UNITS
TEMPERATURE RANGE								
Specification Range	Ambient temp.	0		+70	0		+70	°C
INPUT								
OFFSET VOLTAGE[1]								
Input Offset Voltage	V_{cm} = 0VDC		±1	±3		±1	±5	mV
Average Drift			±3	±10		±3	±10	µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	82	94		82	94		dB
			±20	±80		±20	±80	µV/V
BIAS CURRENT[1]								
Input Bias Current	V_{cm} = 0VDC Device operating		±23	±115		±23	±250	pA
OFFSET CURRENT[1]								
Input Offset Current	V_{cm} = 0VDC Device operating		±16	±100		±16	±200	pA
VOLTAGE RANGE								
Common-Mode Input Range		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	82	98		80	96		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	106	116		100	110		dB
RATED OUTPUT								
Voltage Output	R_L = 2kΩ	±10.5	±11		±10.5	±11		V
Current Output	V_o = ±10VDC	±5.25	±10		±5.25	±10		mA
Short Circuit Current	V_o = 0VDC	10	40		10	40		mA
POWER SUPPLY								
Current, Quiescent	I_o = 0mADC		2.5	4.5		2.5	5.0	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

MECHANICAL

"M" PACKAGE TO-99 (Hermetic)



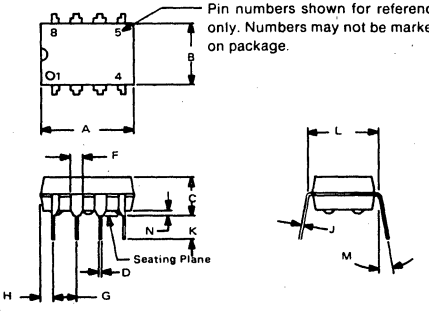
NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

"P" PACKAGE 8-pin Plastic

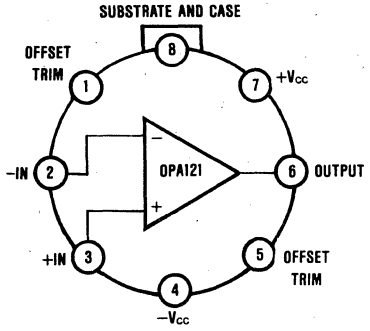


NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.370	.400	9.40	10.16
B	.230	.290	5.84	7.37
C	.120	.200	3.05	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.050	0.76	1.27
J	.008	.015	0.20	0.38
K	.070	.135	1.78	3.43
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.010	.030	0.25	0.76

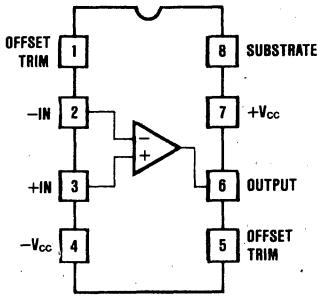
CONNECTION DIAGRAMS

"M" PACKAGE TO-99 (Hermetic)



TOP VIEW

"P" PACKAGE Plastic Mini-DIP



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	−65°C to +150°C (KM)
	−55°C to +125°C (KP)
Operating Temperature Range	−40°C to +85°C (KM)
	−25°C to +85°C (KP)
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[2]	Continuous
Junction Temperature	+175°C

NOTES:
1. Packages must be derated based on θ_{JA} = 150°C/W (KP) or θ_{JA} = 200°C/W (KM).
2. For supply voltages less than ±18VDC the absolute maximum input voltage is equal to +18V > V_{IN} > $-V_{CC}$ −6V. See typical curves.
3. Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ORDERING INFORMATION

OPA121 K X

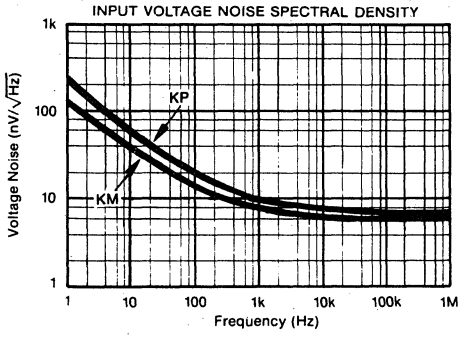
Basic model number

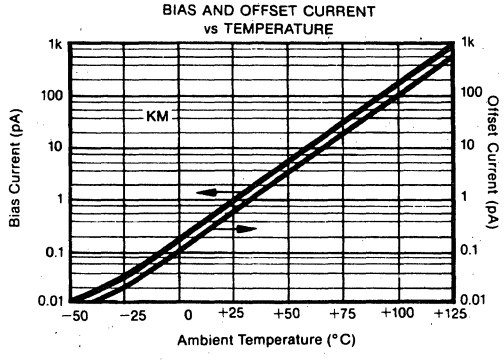
Performance grade
K = 0°C to +70°C

Package code
M = TO-99 metal can
P = Plastic mini-DIP

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

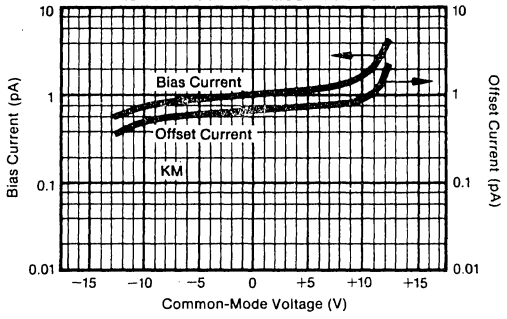




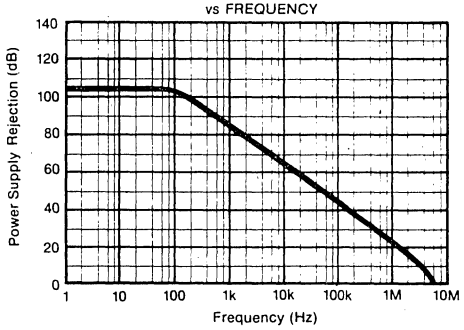
TYPICAL PERFORMANCE CURVES [CONT]

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

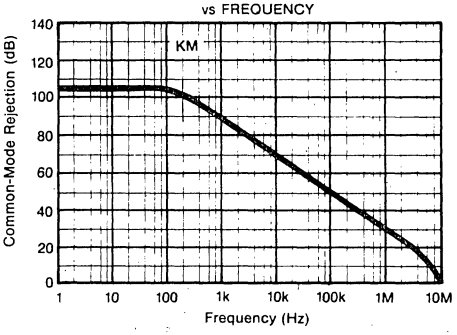
BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



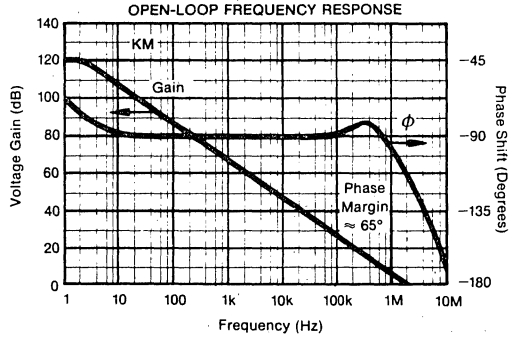
POWER SUPPLY REJECTION vs FREQUENCY



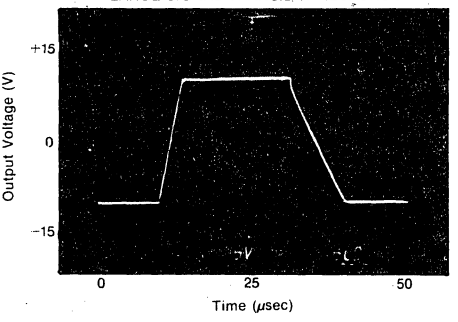
COMMON-MODE REJECTION vs FREQUENCY



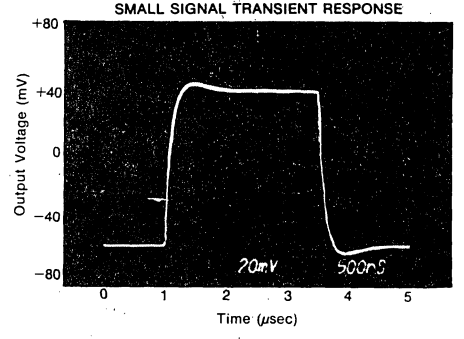
OPEN-LOOP FREQUENCY RESPONSE



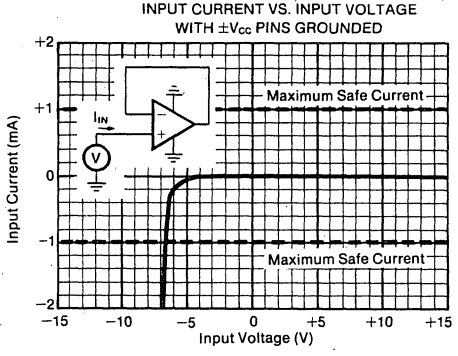
LARGE SIGNAL TRANSIENT RESPONSE



SMALL SIGNAL TRANSIENT RESPONSE



INPUT CURRENT VS. INPUT VOLTAGE WITH ±V_{CC} PINS GROUNDED



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA121 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3μV/°C for each 100μV of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA121 can replace most BIFET amplifiers by leaving the external null circuit unconnected.

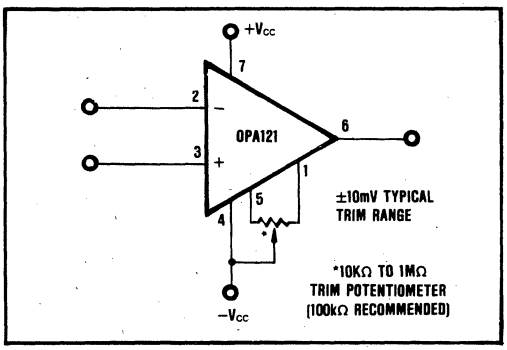


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the ***Difet*** OPA111 requires input current limiting resistors only if its input voltage is greater than 6 volts more negative than $-V_{CC}$. A 10kΩ series resistor will limit input current to a safe level with up to ±15V input levels even if both supply voltages are lost.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias curent of the OPA121. To avoid leakage problems, it is recommended that the signal input lead of the OPA121 be wired to a Teflon standoff. If the OPA121 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 2).

If guarding is not required, pin 8 (case) should be connected to ground.

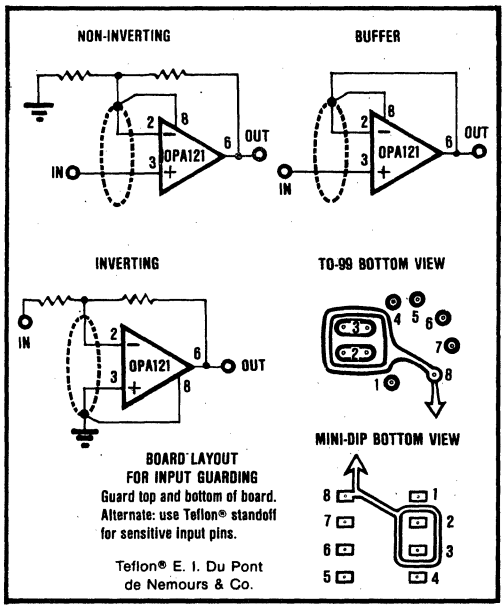


FIGURE 2. Connection of Input Guard.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 3). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA121 is not compromised by common-mode voltage.

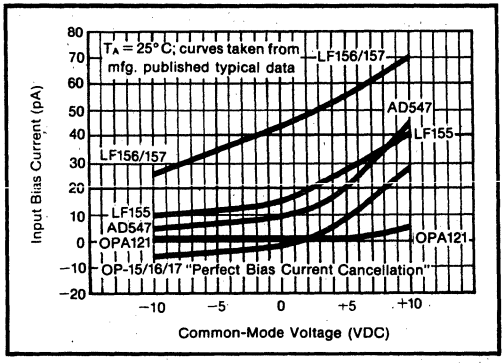


FIGURE 3. Input Bias Current Versus Common-Mode Voltage.

BURR-BROWN®

OPA128

Difet® Electrometer-Grade OPERATIONAL AMPLIFIER

FEATURES

- ULTRA-LOW BIAS CURRENT: 75fA max
- LOW OFFSET: 500μV max
- LOW DRIFT: 5μV/°C max
- HIGH OPEN-LOOP GAIN: 110dB min
- HIGH COMMON-MODE REJECTION: 90dB min
- IMPROVED REPLACEMENT FOR AD515 AND AD549

APPLICATIONS

- ELECTROMETER
- MASS SPECTROMETER
- CHROMATOGRAPH
- ION GAUGE
- PHOTODETECTOR
- RADIATION-HARD EQUIPMENT

DESCRIPTION

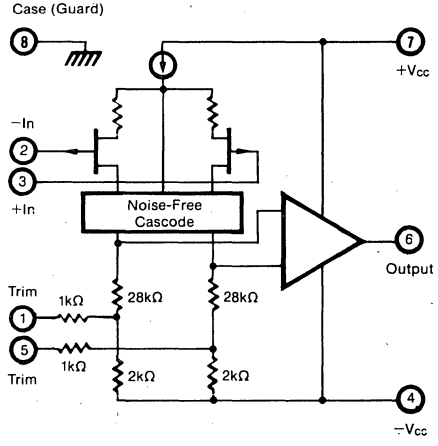
The OPA128 is an ultra-low bias current monolithic operational amplifier. Using advanced geometry dielectrically-isolated FET (*Difet*®) inputs, this monolithic amplifier achieves a performance level exceeding even the best hybrid electrometer amplifiers.

Laser-trimmed thin-film resistors give outstanding voltage offset and drift performance.

A noise-free cascode and low-noise processing give the OPA128 excellent low-level signal handling capabilities. Flicker noise is very low.

The OPA128 is an improved pin-for-pin replacement for the AD515.

Difet® Burr-Brown Corp.



OPA128 Simplified Circuit

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = +15VDC and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA128JM			OPA128KM			OPA128LM			OPA128SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT														
BIAS CURRENT[1]														
Input Bias Current	V_{CM} = 0VDC, R_L > 10kΩ		±150	±300		±75	±150		±40	±75		±75	±150	fA
OFFSET CURRENT[1]														
Input Offset Current	V_{CM} = 0VDC, R_L = 10kΩ		65			30			30			30		fA
OFFSET VOLTAGE[1]														
Input Offset Voltage	V_{CM} = 0VDC		±260	±1000		±140	±500		±140	±500		±140	±500	μV
Average Drift	T_A = T_{MIN} to T_{MAX}			±20			±10			±5			±10	μV/°C
Supply Rejection		80	120		90	120		90	120		90	120		dB
			±1	±100		±1	±32		±1	±32		±1	±32	μV/V
NOISE[4]														
Voltage, f_O = 10Hz			92			92			92			92		nV/√Hz
f_O = 100Hz			78			78			78			78		nV/√Hz
f_O = 1kHz			27			27			27			27		nV/√Hz
f_O = 10kHz			15			15			15			15		nV/√Hz
f_B = 10Hz to 10kHz			2.4			2.4			2.4			2.4		μV, rms
f_B = 0.1Hz to 10Hz			4			4			4			4		μV, p-p
Current, f_B = 0.1Hz to 10Hz			4.2			3			2.3			3		fA, p-p
f_O = 0.1Hz thru 20kHz			0.22			0.16			0.12			0.16		fA/√Hz
IMPEDANCE														
Differential			10^{13} || 1			10^{13} || 1			10^{13} || 1			10^{13} || 1		Ω || pF
Common-Mode			10^{15} || 2			10^{15} || 2			10^{15} || 2			10^{15} || 2		Ω || pF
VOLTAGE RANGE														
Common-Mode Input Range		±10	±12		±10	±12		±10	±12		±10	±12		V
Common-Mode Rejection	V_{IN} = ±10VDC	80	118		90	118		90	118		90	118		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	R_L ≥ 2kΩ	94	128		110	128		110	128		110	128		dB
FREQUENCY RESPONSE														
Unity Gain, Small Signal	[2]	0.5	1		0.5	1		0.5	1		0.5	1		MHz
Full Power Response	20V p-p, R_L = 2kΩ		47			47			47			47		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	0.5	3		1	3		1	3		1	3		V/μs
Settling Time, 0.1%	Gain = −1, R_L = 2kΩ		5			5			5			5		μs
0.01%	10V step		10			10			10			10		μs
Overload Recovery, 50% Overdrive[3]	Gain = −1		5			5			5			5		μs
RATED OUTPUT														
Voltage Output	R_L = 2kΩ	±10.5	±13		±10.5	±13		±10.5	±13		±10.5	±13		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, open loop		100			100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000			1000		pF
Short Circuit Current		10	29	40	10	29	40	10	29	40	10	29	40	mA
POWER SUPPLY														
Rated Voltage			±15			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		0.9	1.5		0.9	1.5		0.9	1.5		0.9	1.5	mA
TEMPERATURE RANGE														
Specification	Ambient temp.	0		+70	0		+70	0		+70	−55		+125	°C
Operating	Ambient temp.	−55		+125	−55		+125	−55		+125	−55		+125	°C
Storage	Ambient temp.	−65		+150	−65		+150	−65		+150	−65		+150	°C
θ Junction-Ambient			200			200			200			200		°C/W

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. Bias current doubles approximately every 11°C. (2) Sample tested. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) Noise test available—inquire.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA128JM			OPA128KM			OPA128LM			OPA128SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE														
Specification Range	Ambient temp.	0		+70	0		+70	0		+70	−55		+125	°C
INPUT														
BIAS CURRENT[1]														
Input Bias Current	V_{CM} = 0VDC		±2.5	±8		±1.3	±4		±0.7	±2		±43	±170	pA
OFFSET CURRENT[1]														
Input Offset Current	V_{CM} = 0VDC		1.1			0.6			0.6			18		pA
OFFSET VOLTAGE[1]														
Input Offset Voltage	V_{CM} = 0VDC			±2.2mV			±1mV			±750			±1.5mV	µV
Average Drift				±20			±10			±5			±10	µV/°C
Supply Rejection		74	114		80	114		80	114		80	106		dB
			±2	±200		±2	±100		±2	±100		±5	±100	µV/V
VOLTAGE RANGE														
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	74	112		80	112		80	112		74	104		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	90	125		104	125		104	125		90	122		dB
RATED OUTPUT														
Voltage Output	R_L = 2kΩ	±10.5			±10.5			±10.5			±10.5			V
Current Output	V_O = ±10VDC	±5			±5			±5			±5			mA
Short Circuit Current	V_O = 0VDC	10	22		10	22		10	22		10	18		mA
POWER SUPPLY														
Current, Quiescent	I = 0mADC		0.9	1.8		0.9	1.8		0.9	1.8		0.9	2	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[2]	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on θ_{CA} = 150°C/W or θ_{JA} = 200°C/W. (2) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

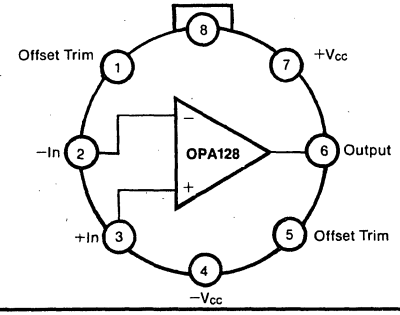
ORDERING INFORMATION

OPA128 X M

- Basic Model Number
- Performance Grade
  - J, K, L = 0°C to +70°C
  - S = −55°C to +125°C
- Package Code
  - M = TO-99 metal can

CONNECTION DIAGRAM

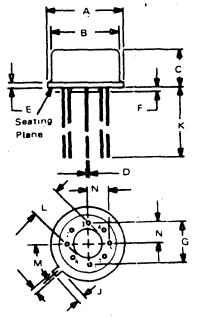
Top View Substrate and Case



MECHANICAL

"M" PACKAGE TO-99 (Hermetic)

NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

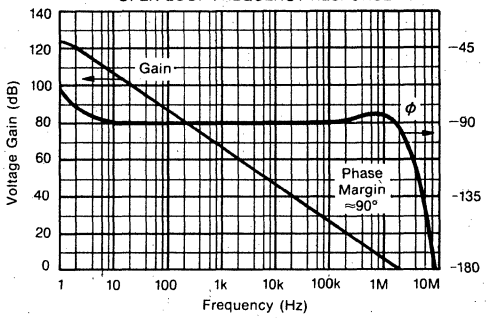


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	–	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

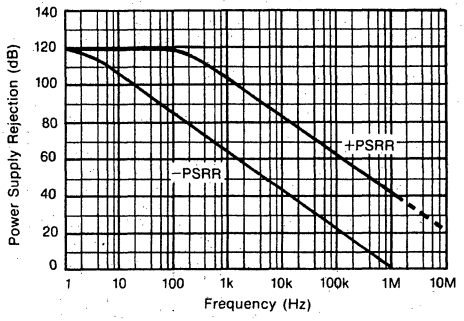
TYPICAL PERFORMANCE CURVES

T_A = +25°C, ±15VDC unless otherwise noted.

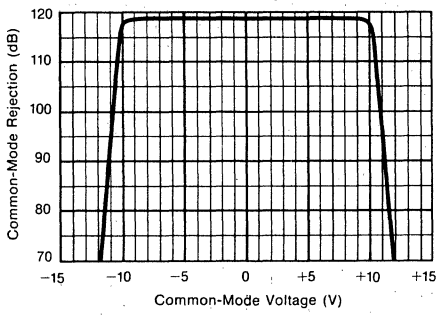
OPEN-LOOP FREQUENCY RESPONSE



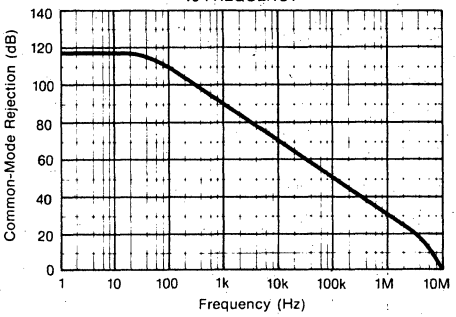
POWER SUPPLY REJECTION vs FREQUENCY



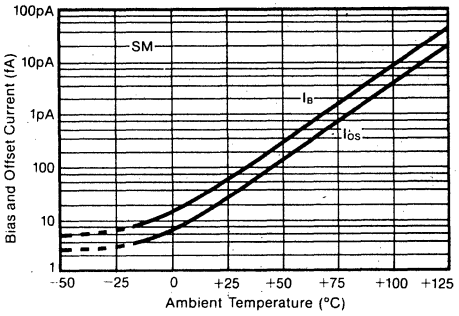
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



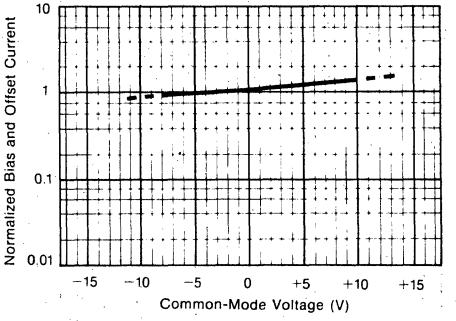
COMMON-MODE REJECTION vs FREQUENCY



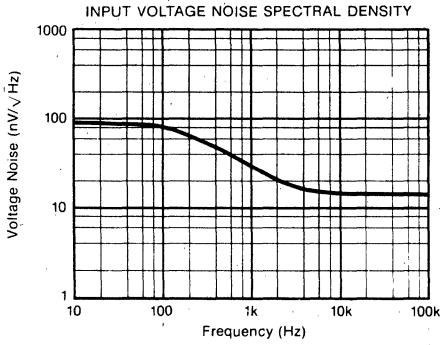
BIAS AND OFFSET CURRENT vs TEMPERATURE



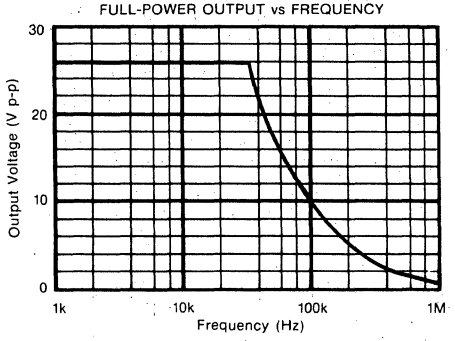
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



INPUT VOLTAGE NOISE SPECTRAL DENSITY



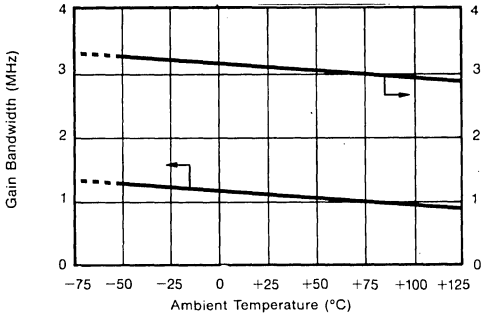
FULL-POWER OUTPUT vs FREQUENCY



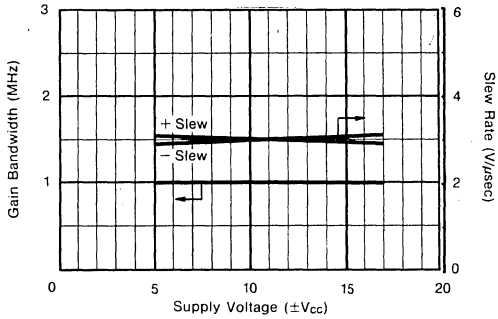
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, ±15VDC unless otherwise noted.

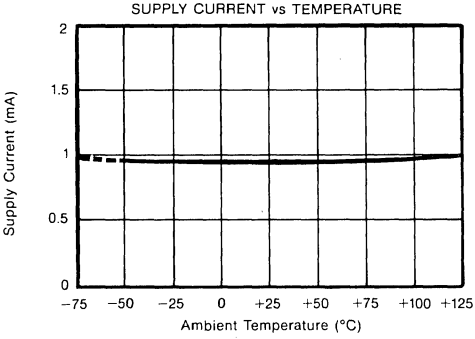
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



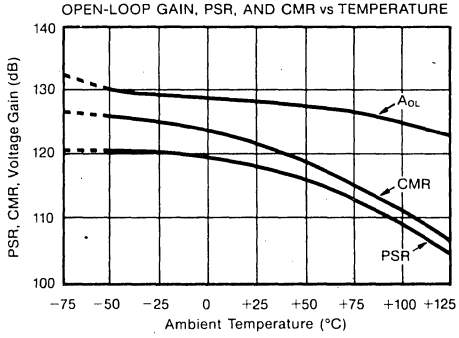
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



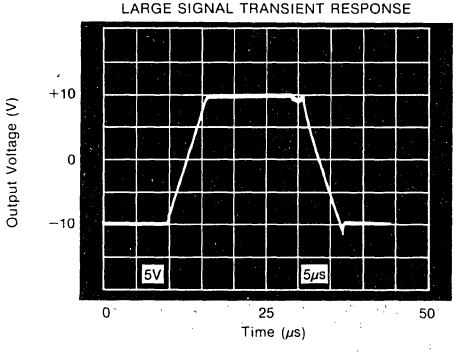
SUPPLY CURRENT vs TEMPERATURE



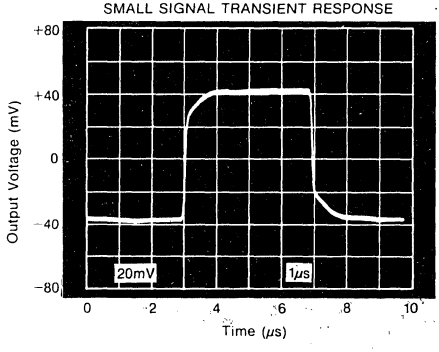
OPEN-LOOP GAIN, PSR, AND CMR vs TEMPERATURE



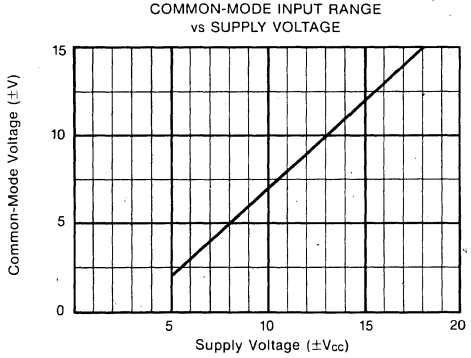
LARGE SIGNAL TRANSIENT RESPONSE



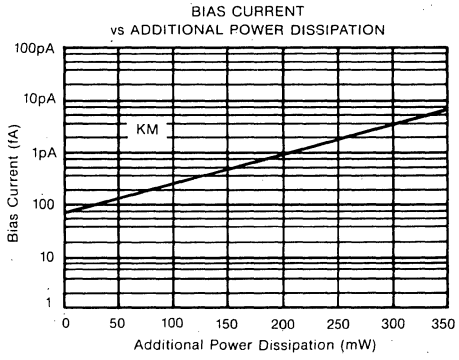
SMALL SIGNAL TRANSIENT RESPONSE



COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE



BIAS CURRENT vs ADDITIONAL POWER DISSIPATION



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA128 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplfiers, externally trimming the remaining offset can change drift performance by about 0.3μV/°C for each 100μV of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as HA-5180 and AD515. The OPA128 can replace many other amplifiers by leaving the external null circuit unconnected.

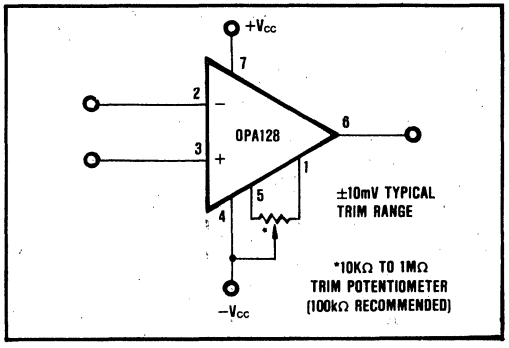


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers' inputs must be protected against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET® amplifiers can be destroyed by the loss of $-V_{CC}$.

Because of its dielectric isolation, no special protection is needed on the OPA128. Of course, the differential and common-mode voltage limits should be observed.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. Leakage currents across printed circuit boards can easily exceed the bias current of the OPA128. To avoid leakage problems, it is recommended that the signal input lead of the OPA128 be wired to a Teflon standoff. If the input is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 2).

Triboelectric charge (static electricity generated by friction) can be a troublesome noise source from cables connected to the input of an electrometer amplifier. Special low-noise cable will minimize this effect but the optimum solution is to mount the signal source directly at the electrometer input with short, rigid, wiring to preclude microphonic noise generation.

TESTING

Accurately testing the OPA128 is extremely difficult due to its high level of performance. Ordinary test equipment may not be able to resolve the amplifier's extremely low bias current.

Inaccurate bias current measurements can be due to:

1. Test socket leakage
2. Unclean package
3. Humidity or dew point condensation
4. Circuit contamination from fingerprints or anti-static treatment chemicals
5. Test ambient temperature
6. Load power dissipation.

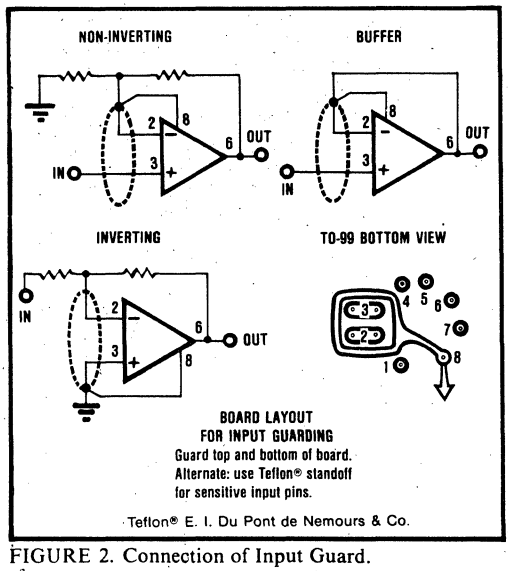


FIGURE 2. Connection of Input Guard.

BIFET® National Semiconductor Corp.

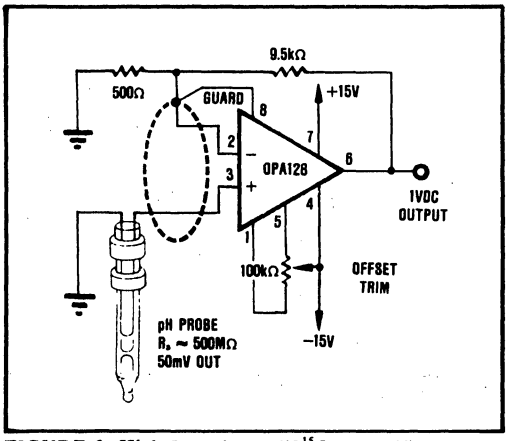


FIGURE 3. High Impedance ($10^{15}\Omega$) Amplifier.

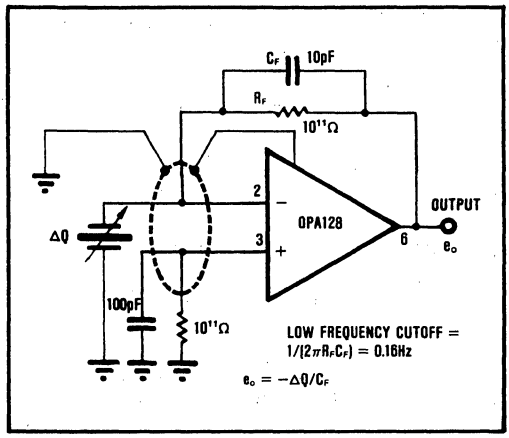


FIGURE 4. Piezoelectric Transducer Charge Amplifier.

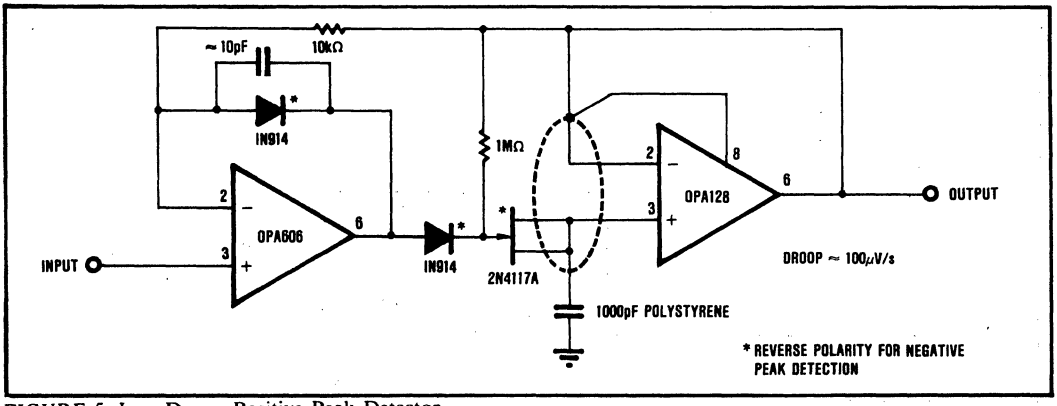


FIGURE 5. Low-Droop Positive Peak Detector.

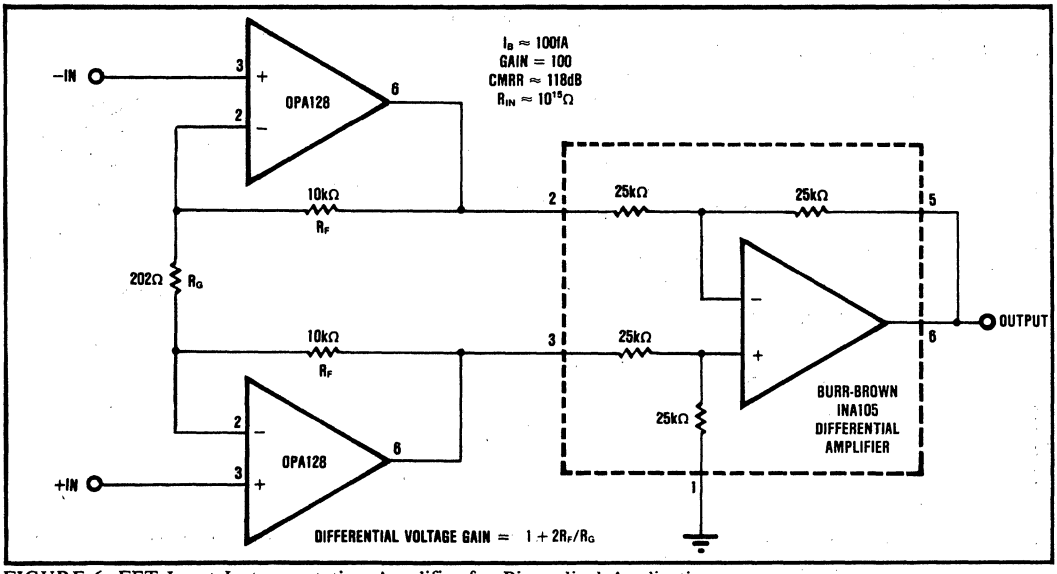


FIGURE 6. FET Input Instrumentation Amplifier for Biomedical Applications.

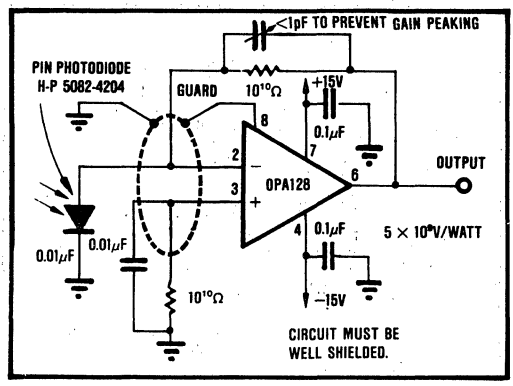


FIGURE 7. Sensitive Photodiode Amplifier.

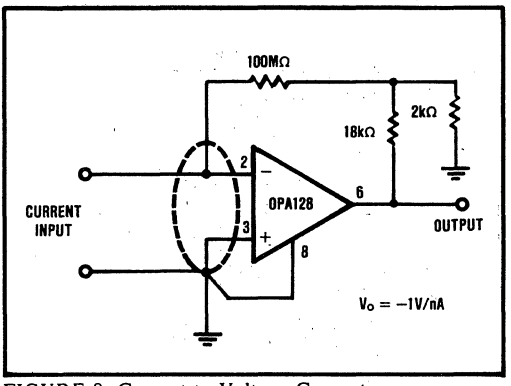


FIGURE 8. Current-to-Voltage Converter.

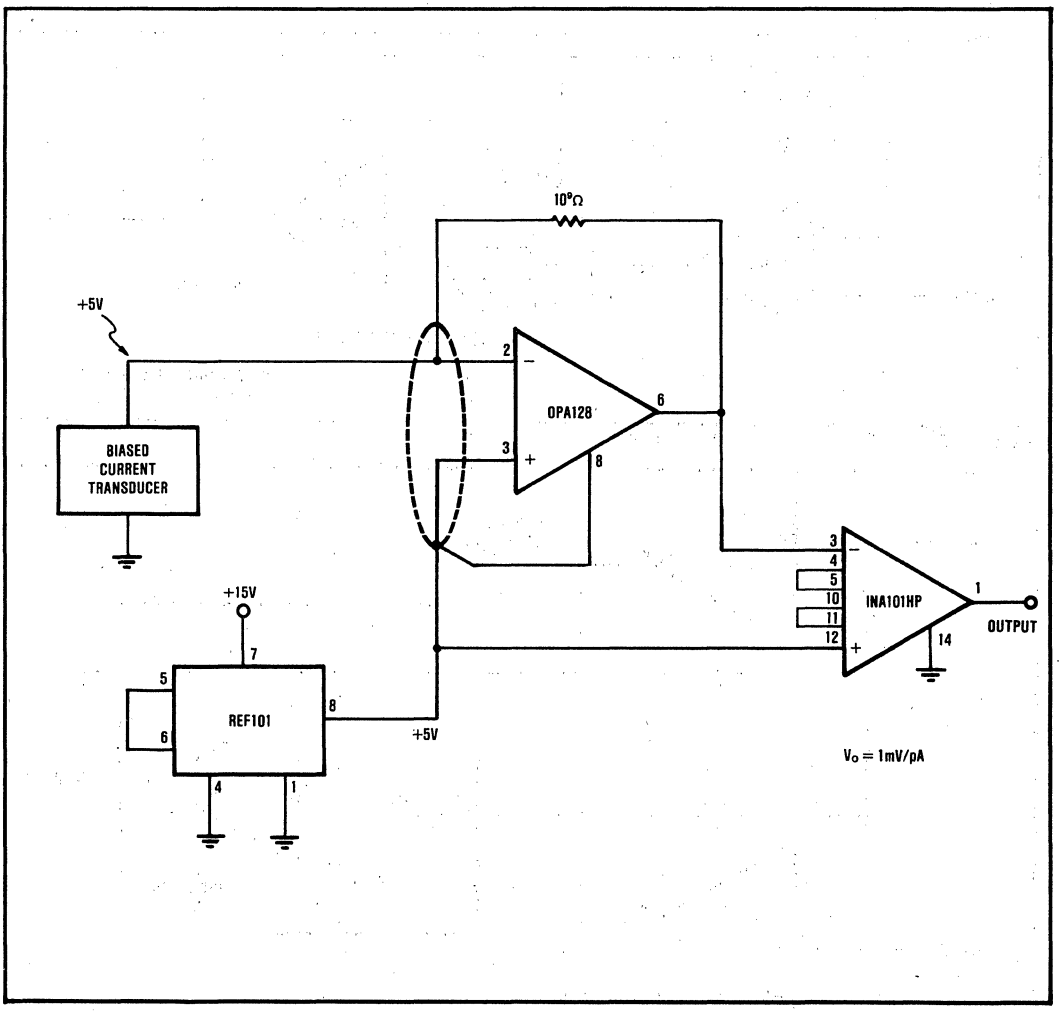


FIGURE 9. Biased Current-to-Voltage Converter.

BURR-BROWN®

OPA156A
OPA356A

Wide-Bandwidth *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH, 4MHz min
- HIGH SLEW RATE, 10V/μsec min
- LOW BIAS CURRENT, 50pA max at $T_A = +25°C$
- LOW OFFSET VOLTAGE, 2mV max
- LOW DRIFT, 5μV/°C max

APPLICATIONS

- OPTOELECTRONICS
- DATA ACQUISITION
- IMPROVED REPLACEMENT FOR INDUSTRY-STANDARD LF156A BIFET® OPERATIONAL AMPLIFIER

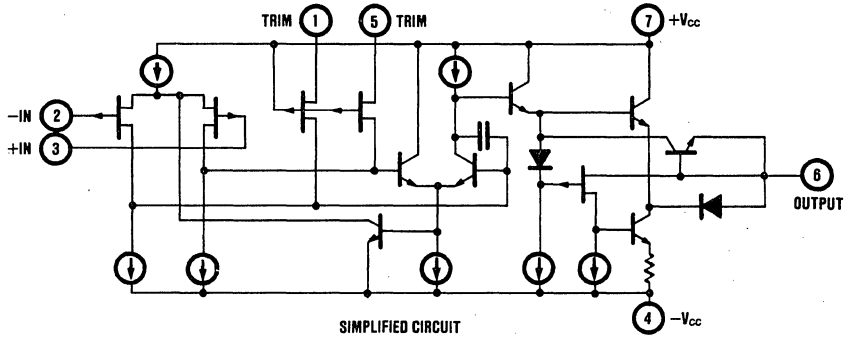
DESCRIPTION

The OPA156A/356A is a wide-bandwidth monolithic dielectrically-isolated FET (*Difet*) operational amplifier. Improved circuit design and dielectric isolation allow lower bias current than BIFET LF156A amplifiers. Bias current is specified under warmed-up and operating conditions, not at a JUNCTION temperature of +25°C.

Laser-trimmed thin-film resistors offer improved offset voltage and noise performance.

The OPA156A is internally compensated for unity-gain stability.

BIFET® National Semiconductor Corp., *Difet*® Burr-Brown Corp.



SIMPLIFIED CIRCUIT

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At $\pm V_{CC}$ = 15VDC and T_A = +25°C unless otherwise specified.

PARAMETER	CONDITIONS	OPA156A MIN	OPA156A TYP	OPA156A MAX	OPA356A MIN	OPA356A TYP	OPA356A MAX	UNITS
FREQUENCY RESPONSE								
Slew Rate	V_o = ±10V, R_L = 2kΩ							
	G = +1	10	14		10	14		V/µsec
Settling Time, 0.01%[1]	10V Step, R_L = 2kΩ		4			4		µsec
Gain Bandwidth		4	6		4	6		MHz
INPUT								
NOISE								
Voltage: f_o = 100Hz	R_s = 100Ω		25			25		nV/√Hz
f_o = 1kHz	R_s = 100Ω		15			15		nV/√Hz
Current: f_o = 100Hz			0.005			0.005		pA/√Hz
f_o = 1kHz			0.005			0.005		pA/√Hz
OFFSET VOLTAGE[2]								
Input Offset Voltage	R_s = 50Ω		±1	±2		±1	±2	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±5		±3	±5	µV/°C
Supply Rejection	$\Delta+V_{CC} = \Delta-V_{CC}$	85	100		85	100		dB
			±10	±57		±10	±57	µV/V
BIAS CURRENT[2]								
Input Bias Current	V_{cm} = 0VDC		30	50		30	50	pA
OFFSET CURRENT[2]								
Input Offset Current	V_{cm} = 0VDC		3	10		3	10	pA
INPUT IMPEDANCE								
Resistance || Capacitance			10^{12} || 3			10^{12} || 3		Ω || pF
VOLTAGE RANGE								
Common-Mode Input Range		±11	±12		±11	±12		V
Common-Mode Rejection	V_{IN} = ±10VDC	85	100		85	100		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq$ 2kΩ	94	106		94	106		dB
		50	200		50	200		V/mV
RATED OUTPUT								
Voltage Output	R_L = 10kΩ	±12	±13		±12	±13		V
	R_L = 2kΩ	±10	±12		±10	±12		V
POWER SUPPLY								
Rated Voltage			±15			±15		VDC
Voltage Range, Derated Performance		±5		±20	±5		±18	VDC
Current, Quiescent	I_o = 0mADC		5	7		5	10	mA
TEMPERATURE RANGE								
Specification	Ambient temp.	−55		+125	0		+70	°C
Storage	Ambient temp.	−65		+150	−65		+150	°C
θ Junction-Ambient			150			150		°C/W

NOTES: (1) Sample tested—this parameter is not guaranteed. See settling time test circuit (Figure 2). (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $\pm V_{CC}$ = 15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA156A MIN	OPA156A TYP	OPA156A MAX	OPA356A MIN	OPA356A TYP	OPA356A MAX	UNITS
TEMPERATURE RANGE								
Specification Range	Ambient temp.	−55		+125	0		+70	°C
INPUT								
OFFSET VOLTAGE[1]								
Input Offset Voltage	R_s = 50Ω		±1	±2.5		±1	±2.3	mV
Average Drift	R_s = 50Ω		±3	±5		±3	±5	µV/°C
Supply Rejection	$\Delta+V_{CC} = \Delta-V_{CC}$	85	100		85	100		dB
			±10	±57		±10	±57	µV/V
BIAS CURRENT[1]								
Input Bias Current	V_{cm} = 0VDC		15	25		3	5	nA
OFFSET CURRENT[1]								
Input Offset Current	V_{cm} = 0VDC		6	10		0.6	1	nA
VOLTAGE RANGE								
Common-Mode Input Range		±11	±12		±11	±12		V
Common-Mode Rejection	V_{IN} = ±10VDC	85	100		85	100		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	88	92		88	92		dB
		25	40		25	40		V/mV
RATED OUTPUT								
Voltage Output	R_L = 10kΩ	±12	±13		±12	±13		V
	R_L = 2kΩ	±10	±12		±10	±12		V

NOTE: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply: OPA156A ..... ±22VDC
OPA356A ..... ±18VDC
Internal Power Dissipation[1] 670mW
Differential Input Voltage[2] ..... ±40VDC
Input Voltage Range[2] ..... ±20VDC
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range ..... −55°C to +125°C
Lead Temperature (soldering, 10 seconds) ..... +300°C
Output Short Circuit Duration[3] ..... Continuous
Junction Temperature ..... +150°C

NOTES: (1) Packages must be derated based on θ_{JC} = 45°C/W or θ_{JA} = 150°C/W. (2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ORDERING INFORMATION

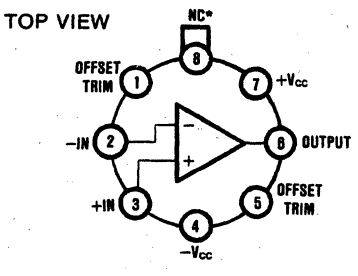
OPA X 56A X

Basic model number

Temperature range
1 = −55°C to +125°C
3 = 0°C to +70°C

Package code
M = TO-99

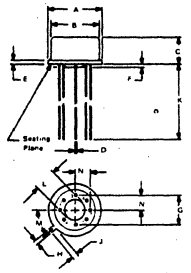
CONNECTION DIAGRAMS



* NO INTERNAL CONNECTION
CASE IS INTERNALLY CONNECTED TO V_{CC}

MECHANICAL

"M" PACKAGE: TO-99



NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

The TO-99 can and leads are bright acid tin plated.

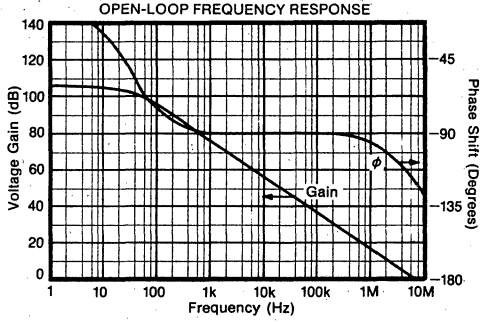
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

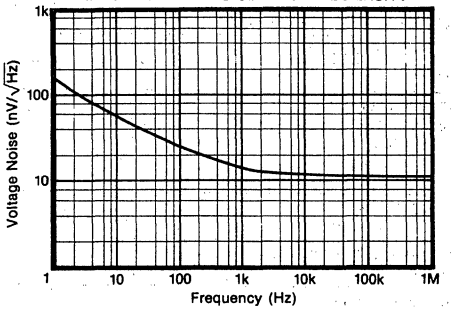
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

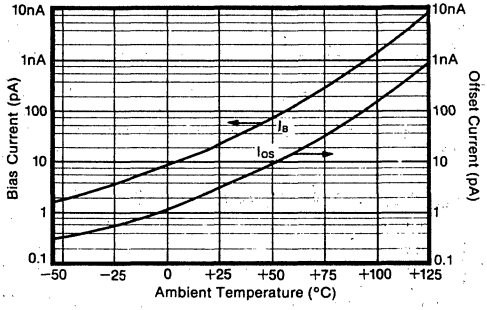
OPEN-LOOP FREQUENCY RESPONSE



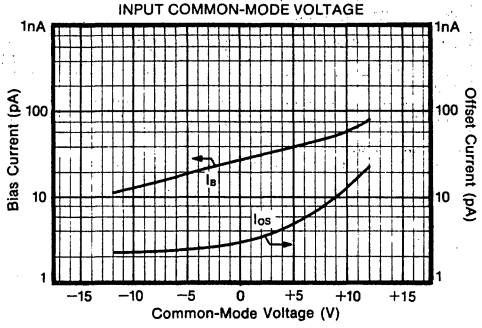
INPUT VOLTAGE NOISE SPECTRAL DENSITY



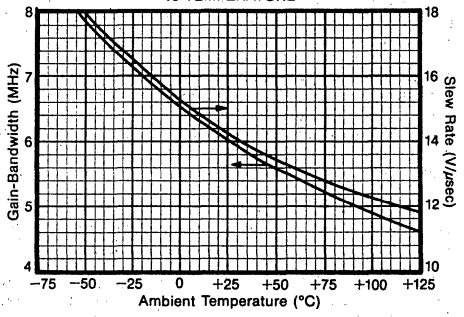
BIAS AND OFFSET CURRENT vs TEMPERATURE



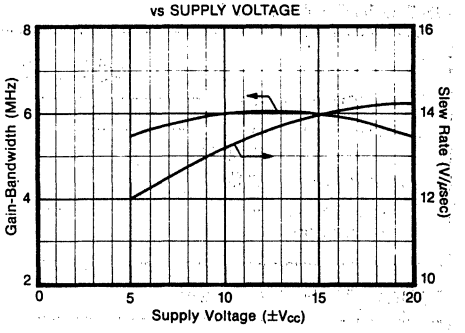
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



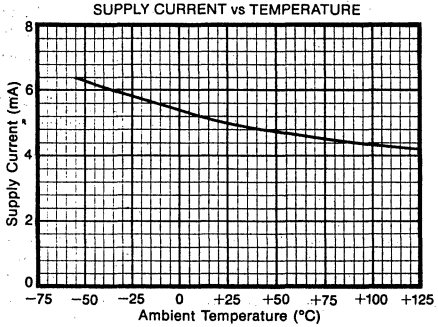
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



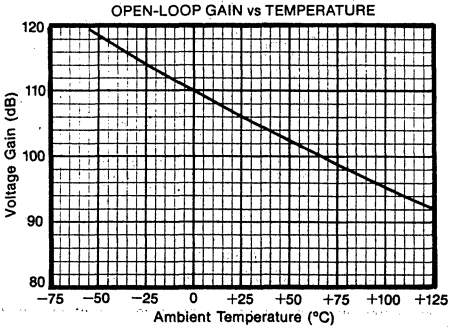
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



SUPPLY CURRENT vs TEMPERATURE



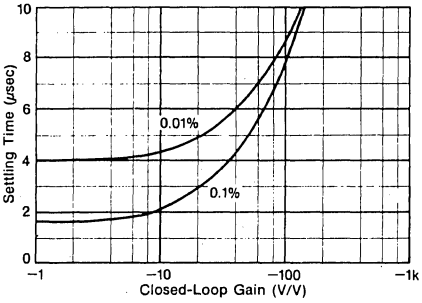
OPEN-LOOP GAIN vs TEMPERATURE



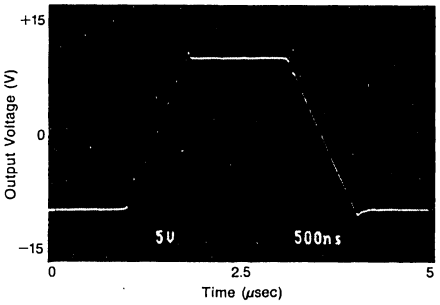
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

SETTLING TIME vs CLOSED-LOOP GAIN



LARGE SIGNAL TRANSIENT RESPONSE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA156A offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.5µV/°C for each millivolt of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as LF156 and OP-16. The OPA156A can replace most other amplifiers by leaving the external null circuit unconnected.

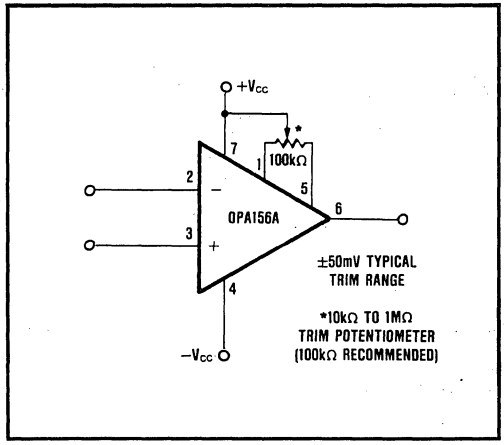


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

If the input voltage exceeds the supply voltage, current must be limited to 1mA to prevent damage.

CIRCUIT LAYOUT

Wideband amplifiers require good circuit layout techniques and adequate power supply bypassing. Short, direct connections and good high frequency bypass capacitors (ceramic or tantalum) will help avoid noise pickup or oscillation.

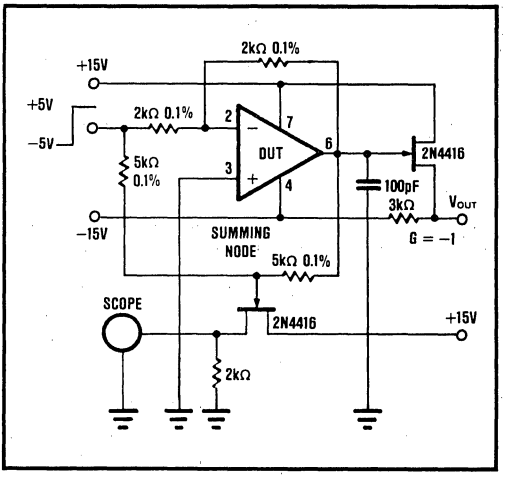


FIGURE 2. Settling Time Test Circuit.

APPLICATIONS CIRCUITS

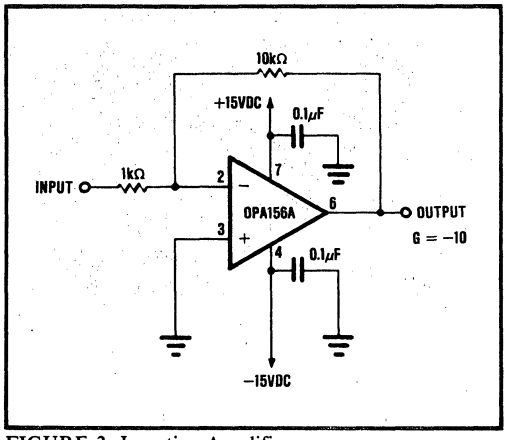


FIGURE 3. Inverting Amplifier.

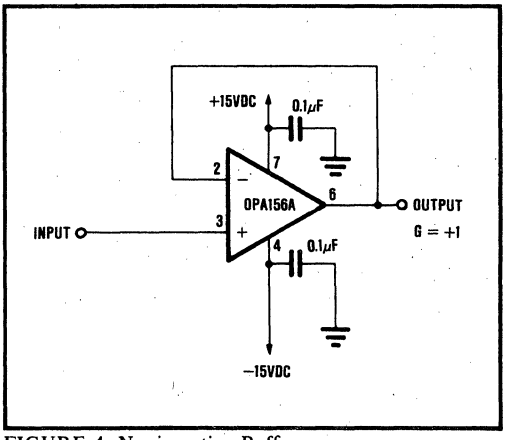


FIGURE 4. Noninverting Buffer.

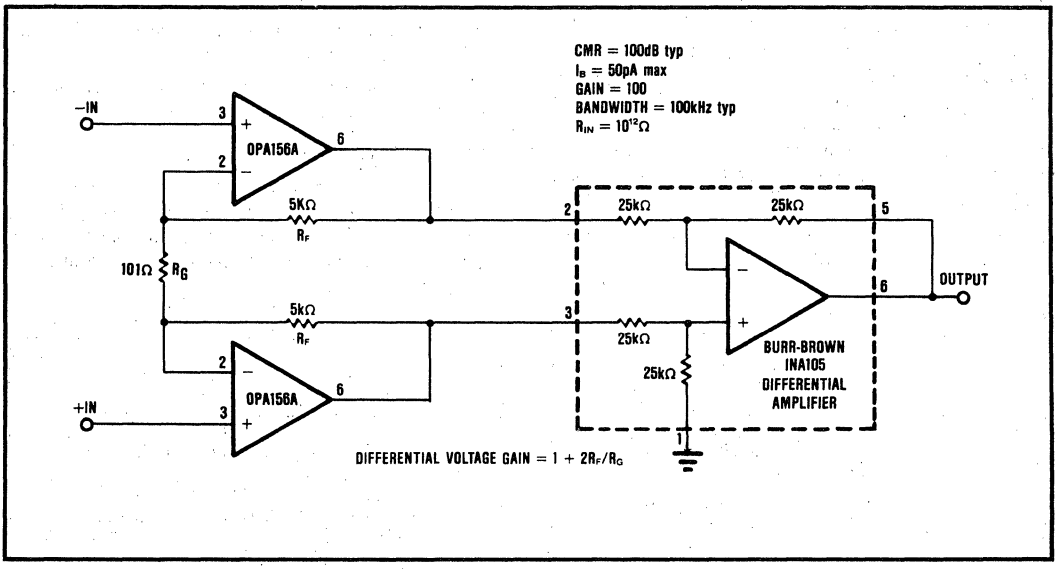


FIGURE 5. Wideband FET Input Instrumentation Amplifier.

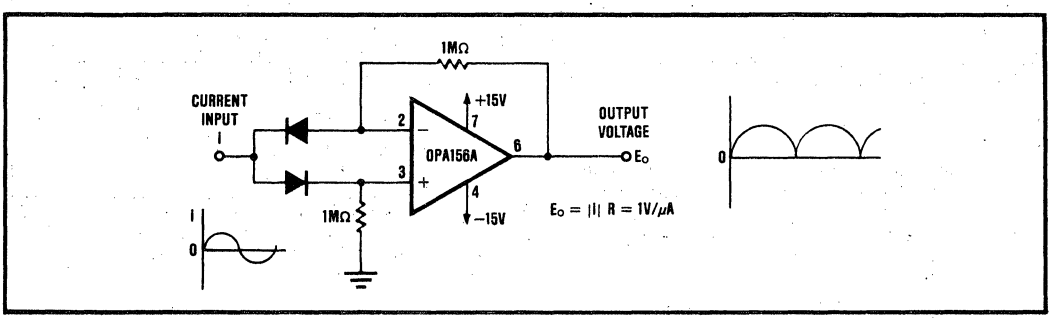


FIGURE 6. Absolute Value Current-to-Voltage Converter.

BURR-BROWN®

OPA201

PAT. PEND.

Switchable-Input Operational Amplifier
SWOP AMP™

FEATURES

- TWO PRECISION INPUT STAGES SELECTABLE BY DIGITAL SIGNAL
- EXCELLENT INPUT SPECIFICATIONS
  - V_{OS} 100μV max
  - DRIFT: 0.5μV/°C typ
  - I_B 25nA max
- LOW POWER
  - $\pm V_{CC}$ 2.5V to 18V
  - I_Q 500μA max

APPLICATIONS

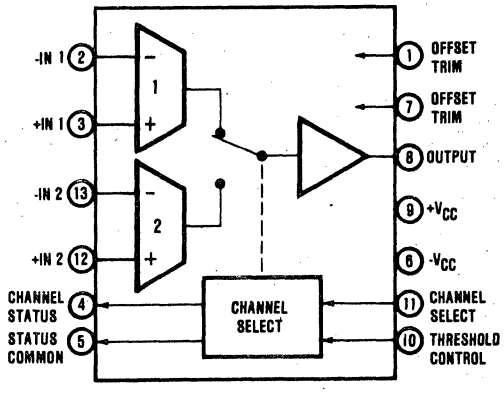
- AUTO-ZERO SYSTEMS
- TWO-CHANNEL MULTIPLEXER WITH GAIN
- SWITCHABLE-GAIN CIRCUITS
- SWITCHABLE-BANDWIDTH CIRCUITS
- SYNCHRONOUS MODULATOR/DEMODULATOR
- BATTERY OPERATED SYSTEMS

DESCRIPTION

The OPA201 is a switchable-input operational amplifier (Swop Amp™). It contains two independent differential input stages and one output stage. Either of the input stages may be connected to the output stage under the control of the Channel Select digital input signal which is TTL-compatible or user-programmable. The OPA201 is easy to use and functions as an operational amplifier that can switch between two sets of inputs.

Each input stage provides excellent input characteristics: low offset voltage (100μV, max), low offset voltage drift versus temperature (1μV/°C, max), and low bias current (25nA, max).

Additionally, the Swop Amp is a low power device. It draws less than 500μA (max) over the supply range $\pm$2.5V to $\pm$18V. It is well suited for portable, remote, and other battery powered applications. Also, its low power consumption and excellent specifications make it well suited for isolation circuit applications. Burr-Brown's state-of-the-art monolithic design and processing, compatible thin-film resistors, and active laser trimming produce a truly unique highly versatile circuit. The unique switchable input stage design allows solutions to very demanding analog circuit design problems.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted. Specifications are for either channel 1 or 2 unless otherwise noted.

PARAMETER	CONDITIONS	OPA201AG/RG MIN	OPA201AG/RG TYP	OPA201AG/RG MAX	OPA201BG/SG MIN	OPA201BG/SG TYP	OPA201BG/SG MAX	OPA201CG MIN	OPA201CG TYP	OPA201CG MAX	UNITS
OPEN-LOOP GAIN, DC	$V_{OUT} = \pm 10V$										
Rated Load	$R_L = 10k\Omega$	114	130		114	130		120	130		dB
	$T_A = T_{MIN}$ to T_{MAX}		120			120			120		dB
RATED OUTPUT											
Voltage	$R_L = 10k\Omega$	±13.5	±14		±13.5	±14		±13.5	±14		V
Current	$V_{OUT} = \pm 10V$		5			5			5		mA
Output Impedance			0.5			0.5			0.5		kΩ
Short Circuit Current			10			10			10		mA
INPUT OFFSET VOLTAGE											
Either Channel											
Voltage Offset[1]			120	500		70	200		35	100	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		1.4			0.9			0.5		µV/°C
vs Supply	$\pm V_{CC} = \pm 2.5V$ to ±18V		8	32		5	18		4	10	µV/V
			10			6			5		µV/V
Match Between											
Channels 1 and 2											
Initial			150	500		65	100		25	50	µV
INPUT BIAS CURRENT											
Initial Bias Current			15	50		13	40		12	25	nA
Over Temperature			22			18			17		nA
INPUT OFFSET CURRENT											
Initial Offset Current			1.4	4		0.75	2		0.7	1	nA
Over Temperature			2.4			1.3			1.2		nA
FREQUENCY RESPONSE											
Gain Bandwidth	G = 100V/V		500			500			500		kHz
Full Power Response	20V, p-p, $R_L = 10k\Omega$		4			4			4		kHz
Slew Rate	$V_{OUT} = \pm 10V$, $R_L = 10k\Omega$	0.1	0.18		0.1	0.18		0.1	0.18		V/µsec
Settling Time 0.1%	G = 1V/V, $R_L = 10k\Omega$		49			49			49		µsec
0.01%	10V Step		52			52			52		µsec
INPUT IMPEDANCE											
Differential			6			6			6		MΩ
Common-Mode			$10^{10} \parallel 2$			$10^{10} \parallel 2$			$10^{10} \parallel 2$		Ω ‖ pF
INPUT NOISE											
Voltage	f_B = 0.1 to 10Hz		1			1			1		µV, p-p
Voltage Density	f_o = 1Hz		85			85			85		$nV/\sqrt{Hz}$
	f_o = 10Hz		27			27			27		$nV/\sqrt{Hz}$
	f_o = 100Hz		27			27			27		$nV/\sqrt{Hz}$
	f_o = 1kHz		27			27			27		$nV/\sqrt{Hz}$
Current	f_B = 0.1 to 10Hz		1.5			1.5			1.5		pA, p-p
Current Density	f_o = 1Hz		1000			1000			1000		$fA/\sqrt{Hz}$
	f_o = 10Hz		300			300			300		$fA/\sqrt{Hz}$
	f_o = 100Hz		100			100			100		$fA/\sqrt{Hz}$
	f_o = 1kHz		100			100			100		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE											
Common-Mode		−12.5		+12.5	−12.5		+12.5	−12.5		+12.5	V
	$T_A = T_{MIN}$ to T_{MAX}		±12			±12			±12		V
Common-Mode Rejection	$V_{IN} = \pm 10V$	85	94		90	98		95	98		dB
	$T_A = T_{MIN}$ to T_{MAX}		92			95			97		dB
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range,											
derated performance		±2.5		±18	±2.5		±18	±2.5		±18	VDC
Current, quiescent			425	500		425	500		425	500	µA
DIGITAL SIGNALS											
Threshold control											
(TC) Voltage Range		$-V_{CC}$		$+V_{CC} - 5$	$-V_{CC}$		$+V_{CC} - 5$	$-V_{CC}$		$+V_{CC} - 5$	V
Channel Select (CSEL)[2]											
Voltage Range		$-V_{CC}$		$+V_{CC}$	$-V_{CC}$		$+V_{CC}$	$-V_{CC}$		$+V_{CC}$	V
V_{IH} (selects ch. 1)		$V_{TC} + 2$		$+V_{CC}$	$+V_{CC} + 2$		$+V_{CC}$	$+V_{CC} + 2$		$+V_{CC}$	V
V_{IL} (selects ch. 2)		$-V_{CC}$	$V_{TC} + 0.6$	$V_{TC} + 0.8$	$-V_{CC}$	$V_{TC} + 0.6$	$-V_{CC} + 0.8$	$-V_{CC}$	$V_{CC} + 0.6$	$V_{TC} + 0.6$	V
	$T_A = T_{MIN}$ to T_{MAX}		$-V_{CC}$			$-V_{CC}$			$-V_{CC}$		V
I_{IH}	$V_{CSEL} = +V_{CC}$		<1	50		<1	50		<1	50	µA
I_{IL}	$V_{CSEL} = V_{TC} = 0V$		25	60		25	60		25	60	µA
Status Common (SC)											
Voltage Range		$-V_{CC}$		[3]	$-V_{CC}$		[3]	$-V_{CC}$		[3]	V
Channel Status											
(CSTA = CSEL)[2]											
V_{OL}	I_{OL} = 1mA, $V_{SC} = 0V$			0.4			0.4			0.4	V
V_{OH}	$V_{pullup} = 15V$, $V_{SC} = 0V$	2.0	15		2.0	15		2.0	15		V

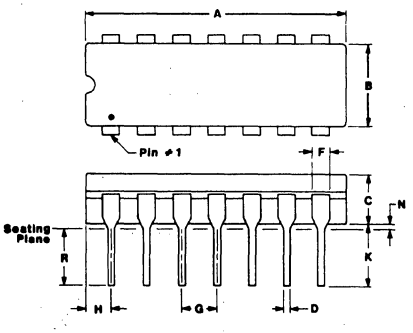
ELECTRICAL (CONT)

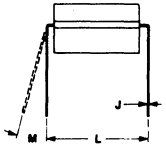
PARAMETER	CONDITIONS	OPA201AG/RG			OPA201BG/SG			OPA201CG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL SIGNALS											
I_{OH} (OFF)			<1	20		<1	20		<1	20	µA
Switching Time											
Between Channels	$T_{MIN} \leq T_A \leq T_{MAX}$		5			5			5		µsec
CROSSTALK											
DC	V_{IN} to OFF	−100	−130		−120	−130		−120	−130		dB
60Hz	Channel = ±12V		−108			−108			−108		dB
TEMPERATURE RANGE (ambient)											
Specification											
A, B, C Grades		−25		+85	−25		+85	−25		+85	°C
S Grade					−55		+125				°C
Operating		−55		+125	−55		+125	−55		+125	°C
Storage		−65		+150	−65		+150	−65		+150	°C

NOTES:
1. Voltage offset is also guaranteed fully warmed-up.
2. V_{TC} = Voltage on threshold control, pin 10. V_{IH}, V_{IL}, V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{OH}, I_{OL}, refers to voltage and current, input and output, high and low logic states.
3. Maximum voltage at Status Common must not be more positive than the Channel Select voltage (pin 11) or Threshold Control voltage (pin 10).

MECHANICAL

NOTES: 1. Leads in true position within 0.01" (0.25mm) R at seating plane.





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.753	.767	19.13	19.48
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.065	—	2.16
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	0.3 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

ORDERING INFORMATION

OPA201 X G

Basic Model Number

Performance Grade Code
- A, B, C −25°C to +85°C
- S −55°C to +125°C

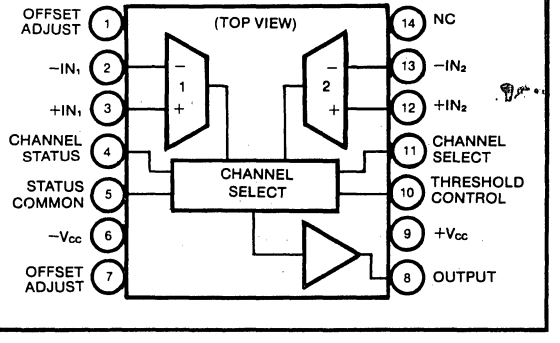
Package Code
- G 14-pin Hermetic DIP

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES:
1. θ_{JA} = 100°C/W
2. For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to power supply common or $\pm V_{CC}$.

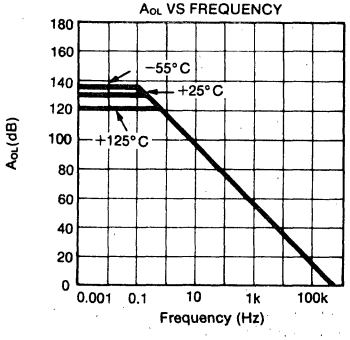
PIN CONFIGURATION



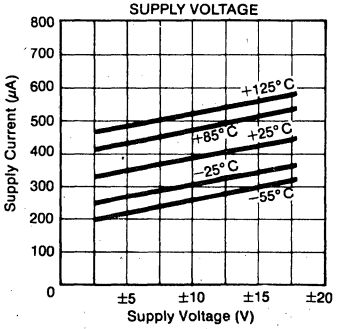
TYPICAL PERFORMANCE CURVES

T_A = +25°C, $\pm V_{CC}$ = 15VDC, specifications are for both channels unless otherwise noted.

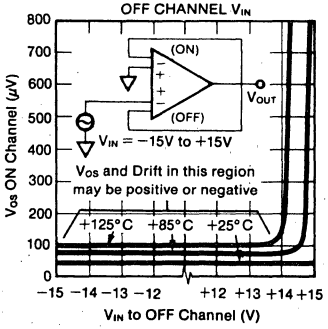
A_{OL} VS FREQUENCY



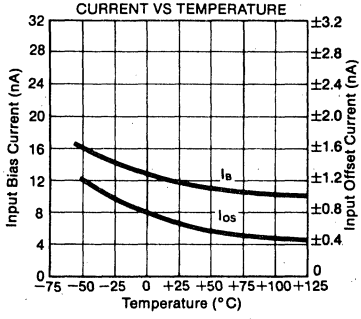
SUPPLY CURRENT VS SUPPLY VOLTAGE



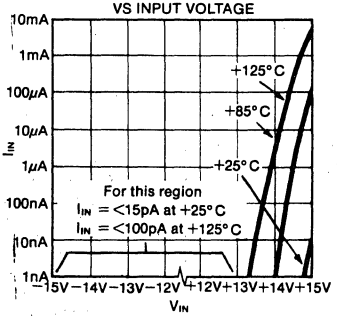
ON CHANNEL V_{OS} VS OFF CHANNEL V_{IN}



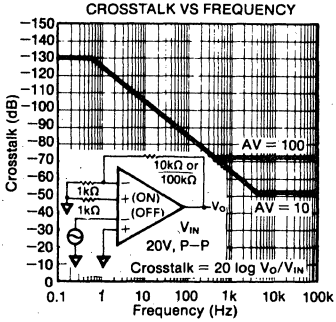
INPUT BIAS AND OFFSET CURRENT VS TEMPERATURE



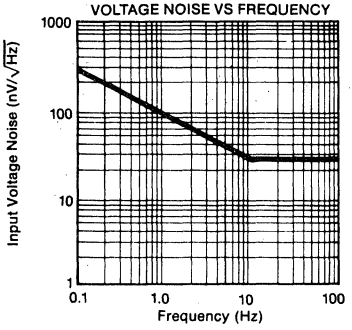
OFF CHANNEL INPUT CURRENT VS INPUT VOLTAGE



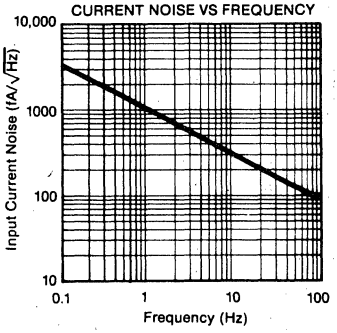
CROSSTALK VS FREQUENCY



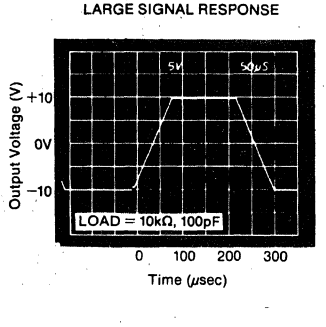
VOLTAGE NOISE VS FREQUENCY



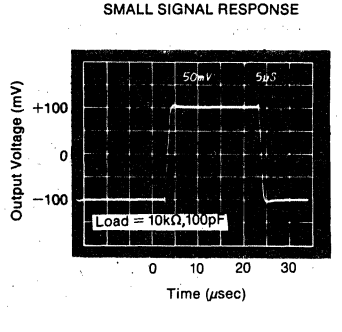
CURRENT NOISE VS FREQUENCY



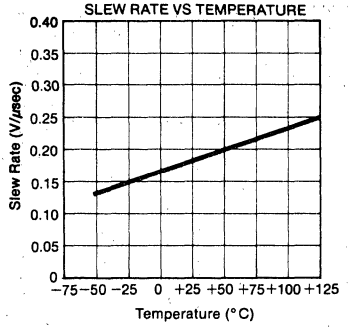
LARGE SIGNAL RESPONSE



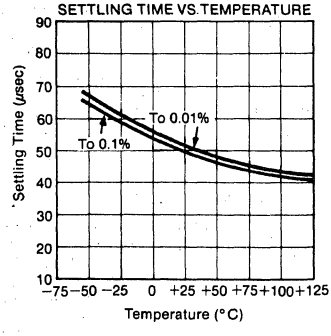
SMALL SIGNAL RESPONSE



SLEW RATE VS TEMPERATURE



SETTLING TIME VS TEMPERATURE



THEORY OF OPERATION

A simplfied schematic of the OPA201 Swop Amp is shown in Figure 1. The circuit has four main parts: (A) input stage 1, (B) input stage 2, (C) active load and output amplifier, and (D) channel select circuit. The two precision differential input stages are identical, with offset and drift laser-trimmed for very-tight matching. The input stages share a balanced, high precision active load and external offset adjust pins, so offset trim affects both channels (see "Using the Swop Amp" section for independent trim techniques). The input stages also share a gain stage and complementary output stage. The biasing circuits for the two input stages are well matched, so the characteristics of the two amplifiers are very nearly identical.

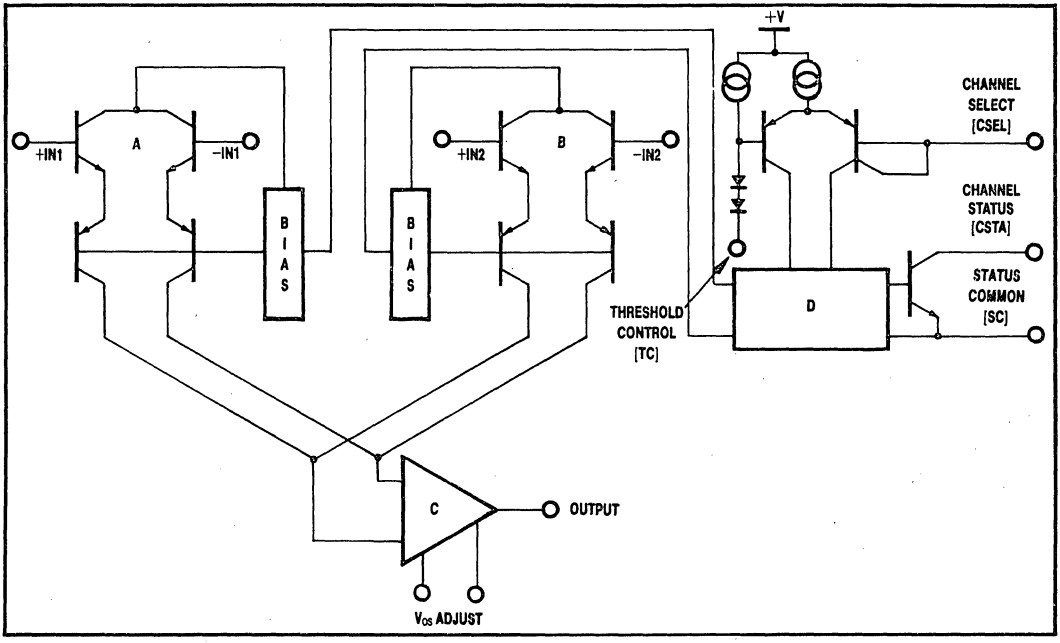


FIGURE 1. OPA 201 Simplified Schematic.

Under control of the channel select circuitry, only one input stage at a time is active. The selected input stage controls the output amplifier, while the unselected input stage is turned off by deactivating its bias circuitry. With no current in the unselected stage, it has negligible input bias current, and the OFF channel cannot send signals to the output amplifier (see Crosstalk specifications and Typical Performance Curves).

The channel select circuitry is simple but versatile, and its use is fully described in the "Using the Swop Amp" section. The trip point for changing channels is set by the threshold control, pin 10. This provides TTL-compatible levels for the channel select voltage on pin 11 when pin 10 is grounded. An open collector output transistor provides the logic inverse of the channel select voltage at the channel status pin. The emitter of this transistor, status common, is also brought out to a pin so the channel status can be referenced to ground or −V.

The complete circuit functions as a high precision operational amplifier which can switch between two sets of inputs under control of a 1-bit logic signal.

USING THE SWOP AMP

Designing with the Swop Amp is basically the same as designing with any precision operational amplifer, with the added versatility of switchable inputs. Feedback is connected from the output to each differential input to configure each channel as an inverting or noninverting amplifier, integrator, or other analog circuit function. The transfer functions for channels 1 and 2 may be identical to the point of sharing feedback elements, or they may be completely independent. Feedback resistors for the off channel are driven by the output as part of the load resistance. Error analysis involving E_{os}, I_B, I_{os}, and V_{cm} is the same as for any operational amplifier.

The OFF channel may be modeled as an open circuit in most applications, with input currents typically under 15pA for input voltages within the specified common-mode range (see Typical Performance Curves). Although crosstalk is specified for OFF channel input voltages equal to the common-mode input range extremes, the same crosstalk characteristics are typically observed for all input voltages between $-V_{CC}$ and $(+V_{CC} - 1VDC)$. Rejection of signals applied to the OFF channel's inputs is outstanding, as shown by the −120dB Crosstalk specifications and Typical Performance Curves for cross-talk versus frequency.

CHANNEL SELECTION

Four pins are involved in the channel select logic,

providing programmable input logic levels for channel select and an output status indicating which channel has been selected. Programmable logic levels allow the logic to be referenced to ground or virtually any voltage. Referencing the logic to −V is especially useful in applications where the supply voltage is low, for example ±3V. The pin-by-pin description and recommended connections describe the versatile but simple channel select techniques (refer to Figures 2 and 3).

Pin 10 - Threshold Control

Pin 10 sets the threshold voltage for channel switching, such that the switching point is two diode drops (≈1.3V) more positive than the Threshold Control voltage. This results in TTL compatibility when pin 10 is grounded. Pin 10 must be at least 5V more negative than $+V_{CC}$, and should be tied to $-V_{CC}$ when the minimum supply voltages are used (±2.5V or +5V). This results in TTL compatibility for logic referenced to $-V_{CC}$.

Pin 11 - Channel Select

The voltage on pin 11 determines which input stage is active. A logic high selects channel 1, logic low selects channel 2. Logic voltages are referenced to the Threshold Control, pin 10, and are TTL-, CMOS-, and open collector-compatible.

Pin 4 - Channel Status

Channel Status is an open collector output indicating which channel has been selected. It is the logic inverse of the Channel Select input referenced to Status Common, pin 5. This function is not required in many applications, and pin 4 should be left unconnected if not used. When using Channel Status, a pullup resistor is connected between pin 4 and a potential more positive than pin 5 (usually +V or ground). The logic low (indicating channel 1 selected) will be less than 0.4V more positive than pin 5 if the pullup resistor sets a current of 1mA or less. Logic high will be the voltage connected to the pullup resistor.

Pin 5 - Status Common

Status Common sets the reference point for Channel Status, and is usually connected to the same potential as the Threshold Control. Pin 5 must be more negative than pins 10 and 11 at all times, and should be connected to $-V_{CC}$ if the Channel Status function is not used. Status Common must be at least 5V more negative than $+V_{CC}$.

OFFSET ADJUSTMENT

The input offset voltage is laser-trimmed and will not require user-adjustment for most applications. Pins 1 and 7 may be used to adjust the offset of the active channel to zero (see Figure 4). This will also affect the offset of the inactive channel (both offsets move in the same direction as the pot is adjusted). This technique may be used to make the offset for each channel equal in magnitude and opposite in polarity, which is desirable in many applications. Besides the complementary nature of the adjusted offsets, their magnitudes will now be less than one-half of the V_{os} match specification.

An inexpensive CMOS IC, CD4007 (dual-Complementary Pair Plus Inverter), may be used to alternately connect dual-offset adjust potentiometers (see Figure 5) allowing independent V_{os} adjustment. In this circuit, the channel status output from the Swop Amp is used to drive the CMOS logic, which connects one wiper or the

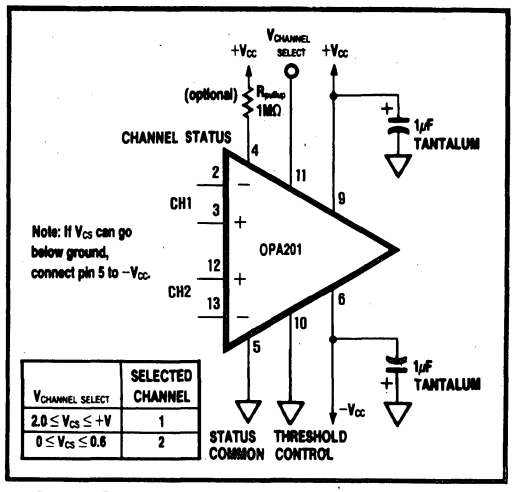


FIGURE 2. Channel Selection for Ground-Referenced Channel Select Signals.

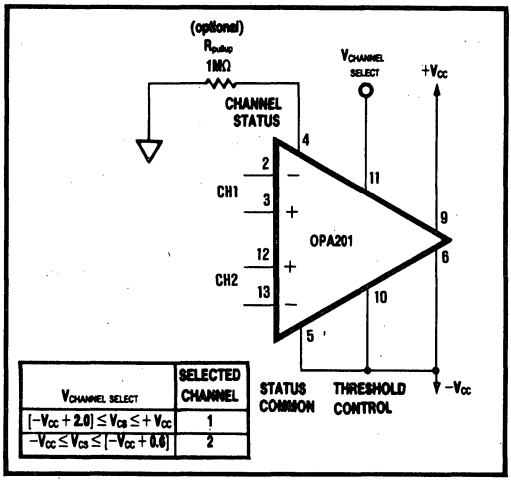


FIGURE 3. Channel Selection for $-V_{CC}$ Referenced Logic Signals.

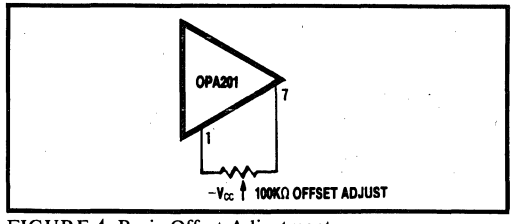


FIGURE 4. Basic Offset Adjustment.

other to $-V_{CC}$. Thus R_1 adjusts the offset of channel 1 while R_2 affects the offset only when channel 2 is selected.

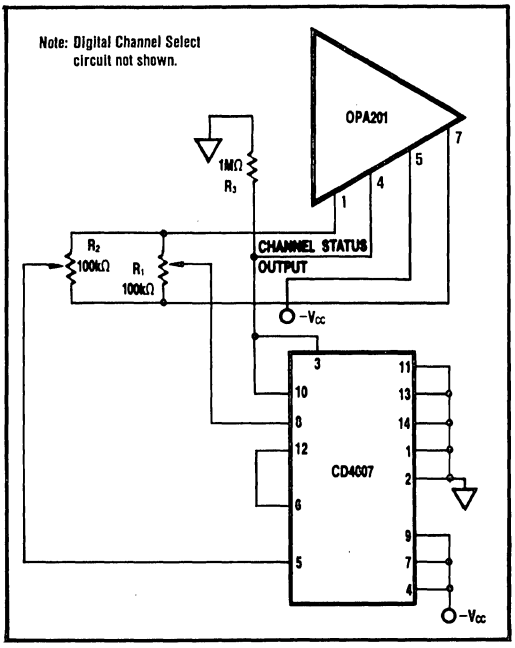


FIGURE 5. Independent Dual-Offset Adjustment.

Note: The CMOS logic requires $-V_{CC}$ (3V minimum) and common. The Status Common (pin 5) must be connected to $-V_{CC}$.

APPLICATIONS

The OPA201 is ideal for a variety of applications where a precision amplifier and switch are needed. Since the two input stages are contained on the same IC and are precision laser-trimmed, their offsets match very closely. Therefore, the OPA201 can be used as an auto-zeroing circuit as well as a dual-channel or switchable-gain amplifier. It can also be extended to become a low power 4-channel Swop Amp or dual-channel instrumentation amplifier under control of TTL level logic. General purpose and unique applications are only limited by the user's imagination.

Software auto-zeroing using the Swop Amp is easy to perform (Figure 6). One channel processes signals and the other channel has the input grounded (both channels have the same gain). The system generating the error signal may be a VFC, Iso Amp, ADC, Modulator, etc. When the zero-input channel is selected,

$$V_{out} = V_{error} + A_V V_{os2}$$

V_{error} = system error voltage
V_{os2} = Channel 2 V_{os}
A_V = Swop Amp voltage gain $= 1 + (R_2/R_1)$

When the signal channel is selected,

$$V_{out} = V_{error} + A_V V_{os1} + A_V V_{IN}$$

Subtracting the "zero" V_o from signal V_o leaves a corrected output voltage

$$V_{0ut} = A_V V_{IN} + A_V (V_{os1} - V_{os2})$$
$$= A_V (V_{IN} + \Delta V_{os})$$

Using this technique, system errors may be reduced to the V_{os} match error (50μV untrimmed for CG grade) of the Swop Amp. Obviously the channel used for zeroing could have a voltage reference or AC waveform for gain calibration for an input, instead of ground.

Auto-zeroing may be free-running, with the Swop Amp functioning as a chopper, by connecting an oscillator to the channel select. Figure 6 shows pin 10 grounded, which allows TTL level interfacing. By programming this pin with a voltage level, other logic levels can be accommodated.

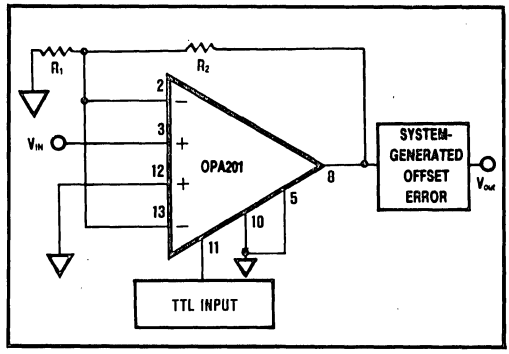


FIGURE 6. Input Amplifier for Auto-Zeroing Systems.

The OPA201 requires only external resistors to make a dual-channel amplifier (2-channel multiplexer with gain). Gain for either channel may be noninverting (Figure 7) or inverting (Figure 8) with the usual operational amplifier gain equations applying in each case. In the noninverting case, feedback is connected from the output to each input, with a common feedback resistor for equal gains. The advantage, in inverting gain circuits, is that the signal does not produce a common-mode voltage which can introduce error or input swing limitations. This is especially important in low supply voltage applications where common-mode range becomes limited. Also one channel can be noninverting and the other inverting, which is particularly useful in absolute value circuits. Note that in order to achieve the specified open-loop gain and maximum output voltage swing, the total output load including both feedback networks should not be less than 10kΩ (see Figures 7 and 8).

Amplifiers with switchable transfer functions are designed much like dual-channel amplifiers, except both inputs are connected in parallel, with each channel configured for a different transfer function. Figure 9 shows a circuit that has a gain of 10 for Channel Select HIGH (channel 1 selected) and a gain of 1000 for Channel Select LOW (channel 2 selected). In this case, the channel select may be thought of as a gain select.

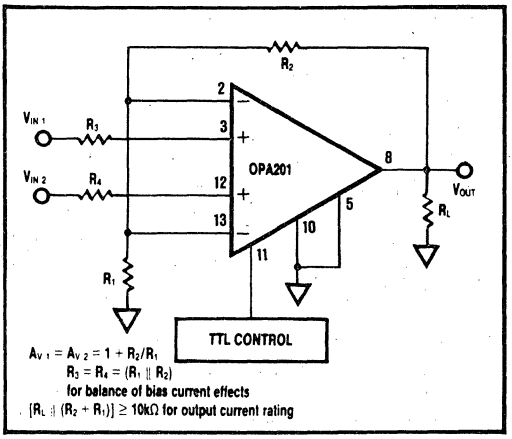


FIGURE 7. Selectable Input Amplifier, Noninverting.

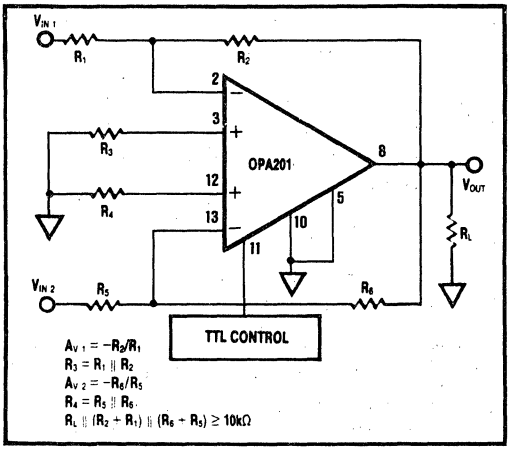


FIGURE 8. Selectable Input Amplifier, Inverting.

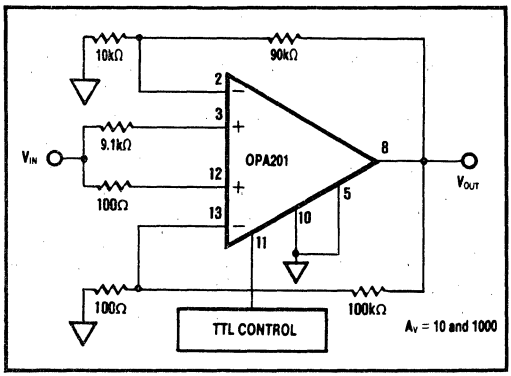


FIGURE 9. Switchable Gain Amplifier.

This concept also applies to switchable bandwidth circuits, where AC coupling (high-pass) or smoothing (low-pass) characteristics need to be switched in under digital control. A wide variety of operational amplifier function circuits may be made selectable or switchable using these techniques.

Figure 10 shows a two-channel differential amplifier. This concept can be expanded to a full high input impedance instrumentation amplifier by adding four input buffer amplifiers or by using two front end Swop Amps followed by an operational amp (Figure 11).

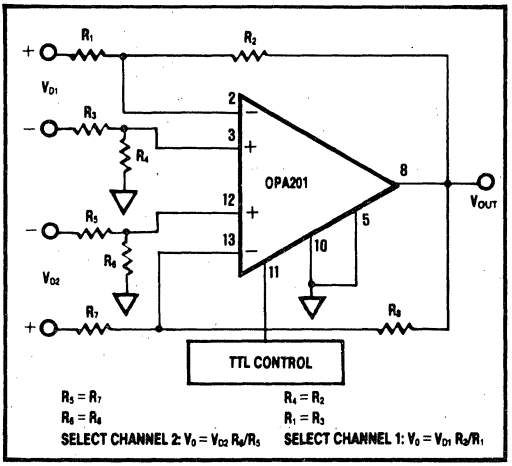


FIGURE 10. Low Power Dual-Channel Differential Amplifier.

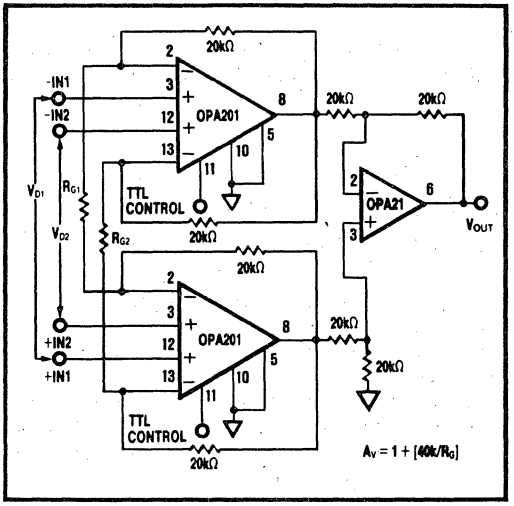


FIGURE 11. Low Power Dual-Channel Instrumentation Amplifier.

BURR-BROWN®

OPA404

Quad High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.4MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: $\pm$750μV max
- LOW BIAS CURRENT: $\pm$4pA max
- FAST SETTLING: 1.5μs to 0.01%
- STANDAD QUAD PINOUT

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

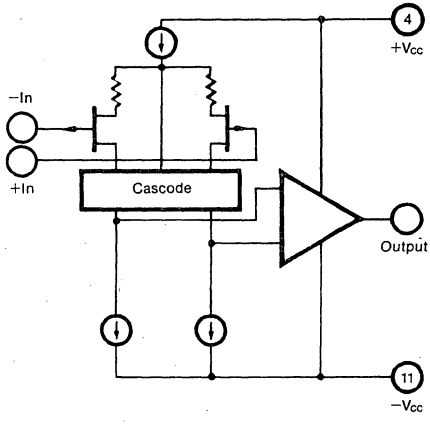
The OPA404 is a high performance monolithic *Difet*® (dielectrically-isolated FET) quad operational amplifier. It offers an unusual combination of very-low bias current together with wide bandwidth and fast slew rate.

Noise, bias current, voltage offset, drift, and speed are superior to BIFET® amplifiers.

Laser trimming of thin-film resistors gives very-low offset and drift—the best available in a quad FET op amp.

The OPA404's input cascode design allows high precision input specifications and uncompromised high-speed performance.

Standard quad op amp pin configuration allows upgrading of existing designs to higher performance levels. The OPA404 is unity-gain stable.



OPA404 Simplified Circuit
(Each Amplifier)

Difet® Burr-Brown Corp., BIFET® National Semiconductor Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG MIN	OPA404AG TYP	OPA404AG MAX	OPA404BG MIN	OPA404BG TYP	OPA404BG MAX	OPA404SG MIN	OPA404SG TYP	OPA404SG MAX	UNITS
INPUT											
NOISE[1]											
Voltage: f_O = 10Hz			32			32			32		nV/√Hz
f_O = 100Hz			19			19			19		nV/√Hz
f_O = 1kHz			15			15			15		nV/√Hz
f_O = 10kHz			12			12			12		nV/√Hz
f_B = 10Hz to 10kHz			1.4			1.4			1.4		μV, rms
f_B = 0.1Hz to 10Hz			0.95			0.95			0.95		μV, p-p
Current: f_B = 0.1Hz to 10Hz			12			12			12		fA, p-p
f_O = 0.1Hz thru 20kHz			0.6			0.6			0.6		fA/√Hz
OFFSET VOLTAGE[2]											
Input Offset Voltage	V_{CM} = 0VDC		±260	±1mV		±260	±750		±260	±1mV	μV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3			±3			±3		μV/°C
Supply Rejection	±V_{CC} = 12V to 18V	80	100		86	100		80	100		dB
			10	100		10	50		10	100	μV/V
Channel Separation	100Hz, R_L = 2kΩ		125			125			125		dB
BIAS CURRENT[2]											
Input Bias Current	V_{CM} = 0VDC		±1	±8		±1	±4		±1	±8	pA
OFFSET CURRENT[2]											
Input Offset Current	V_{CM} = 0VDC		0.5	8		0.5	4		0.5	8	pA
IMPEDANCE											
Differential			10^{13} ‖ 1			10^{13} ‖ 1			10^{13} ‖ 1		Ω ‖ pF
Common-Mode			10^{14} ‖ 3			10^{14} ‖ 3			10^{14} ‖ 3		Ω ‖ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10.5	+13, −11		±10.5	+13, −11		±10.5	+13, −11		V
Common-Mode Rejection	V_{IN} = ±10VDC	88	100		92	100		88	100		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	88	100		92	100		88	100		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Gain = 100	4	6.4		5	6.4		4	6.4		MHz
Full Power Response	20V p-p, R_L = 2kΩ		570			570			570		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	24	35		28	35		24	35		V/μs
Settling Time: 0.1%	Gain = −1, R_L = 2kΩ		0.6			0.6			0.6		μs
0.01%	C_L = 100pF, 10V step		1.5			1.5			1.5		μs
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11.5	+13.2, −13.8		±11.5	+13.2, −13.8		±11.5	+13.2, −13.8		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
Output Resistance	1MHz, open loop		80			80			80		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		±10	±18		±10	±18		±10	±18		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		9	10		9	10		9	10	mA
TEMPERATURE RANGE											
Specification	Ambient temp.	−25		+85	−25		+85	−55		+125	°C
Operating	Ambient temp.	−55		+125	−55		+125	−55		+125	°C
Storage	Ambient temp.	−65		+150	−65		+150	−65		+150	°C
θ Junction-Ambient			85			85			85		°C/W

NOTES: (1) Noise testing available—inquire. (2) Offset voltage, offset current, and bias current are also guaranteed with the units fully warmed up.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG MIN	OPA404AG TYP	OPA404AG MAX	OPA404BG MIN	OPA404BG TYP	OPA404BG MAX	OPA404SG MIN	OPA404SG TYP	OPA404SG MAX	UNITS
TEMPERATURE RANGE											
Specification Range	Ambient temp.	−25		+85	−25		+85	−55		+125	°C
INPUT											
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC		±450	±2mV		±450	±1.5mV		±550	±2.5mV	µV
Average Drift			±3			±3			±3		µV/°C
Supply Rejection		75	96		80	96		70	93		dB
			16	178		16	100		22	316	µV/V
BIAS CURRENT[1]											
Input Bias Current	V_{CM} = 0VDC		±32	±200		±32	±100		±500	±5nA	pA
OFFSET CURRENT[1]											
Input Offset Current	V_{CM} = 0VDC		17	100		17	50		260	2.5nA	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10.2	+12.7, −10.6		±10.2	+12.7 −10.6		±10.0	+12.6 −10.5		V
Common-Mode Rejection	V_{IN} = ±10VDC	82	99		86	99		80	98		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	82	94		86	94		80	88		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11.5	+12.9, −13.8		±11.5	+12.9, −13.8		±11	+12.7, −13.8		V
Current Output	V_O = ±10VDC	±5	±9		±5	±9		±5	±8		mA
Short Circuit Current	V_O = 0VDC	±10	±12		±10	±12		±8	±10		mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		9.3	10.5		9.3	10.5		9.4	11	mA

NOTES: (1) Offset voltage, offset current, and bias current are also guaranteed with the units fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	1000mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES:
(1) Packages must be derated based on θ_{JC} = 15°C/W or θ_{JA} = 85°C/W.
(2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to: 18V > V_{IN} > −V_{CC} − 8V. See Figure 2.
(3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ORDERING INFORMATION

OPA404 X X

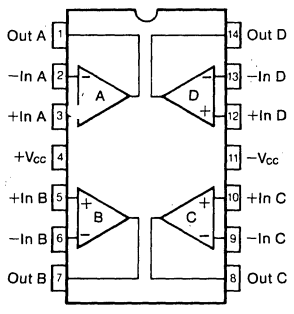
Basic model number

Performance grade
A, B = −25°C to +85°C
S = −55°C to +125°C

Package code
G = 14-pin ceramic DIP

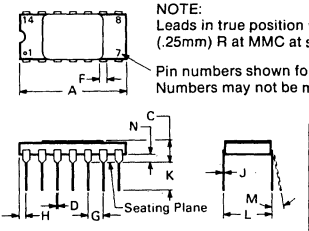
CONNECTION DIAGRAM

Top View



MECHANICAL

"G" Package



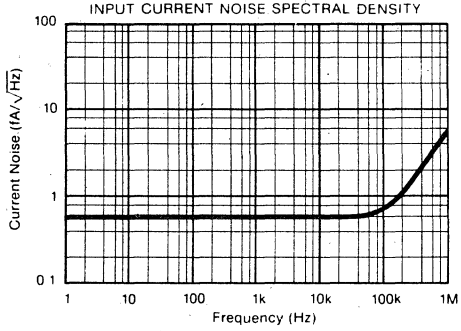
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M		10°		10°
N	.009	.060	0.23	1.52

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

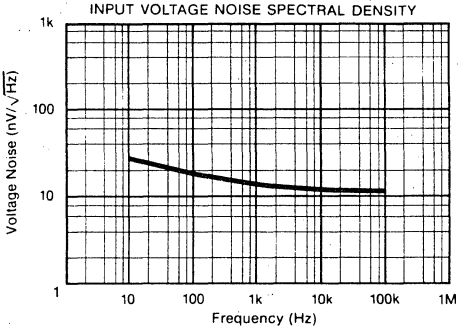
TYPICAL PERFORMANCE CURVES

T_A – +25°C, V_{CC} = ±15VDC unless otherwise noted.

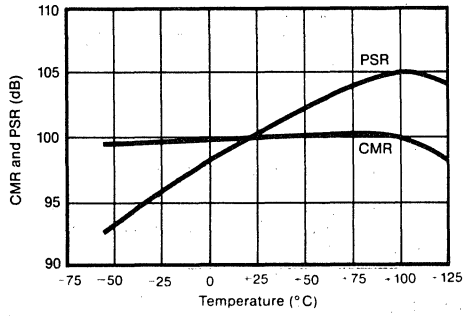
INPUT CURRENT NOISE SPECTRAL DENSITY



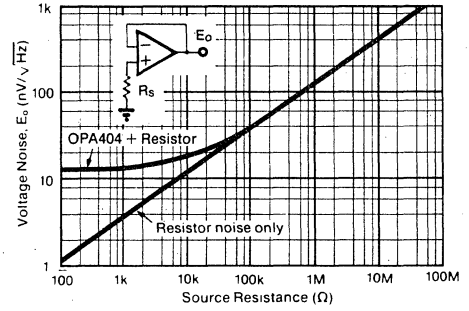
INPUT VOLTAGE NOISE SPECTRAL DENSITY



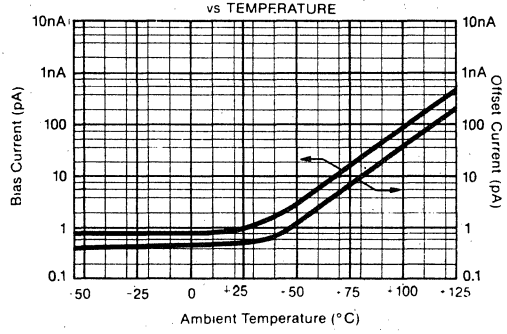
POWER SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



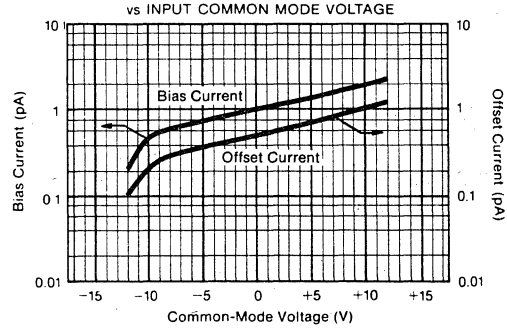
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



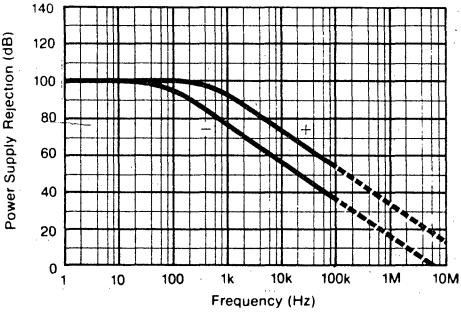
BIAS AND OFFSET CURRENT vs TEMPERATURE



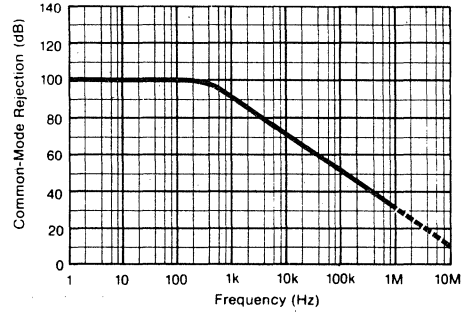
BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



POWER SUPPLY REJECTION vs FREQUENCY



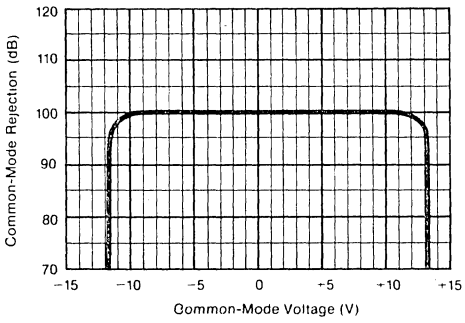
COMMON-MODE REJECTION vs FREQUENCY



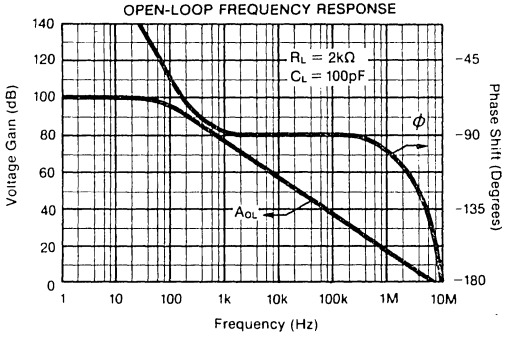
TYPICAL PERFORMANCE CURVES [CONT]

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

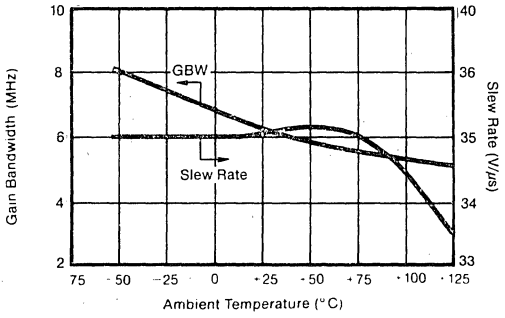
COMMON-MODE REJECTION
vs INPUT COMMON MODE VOLTAGE



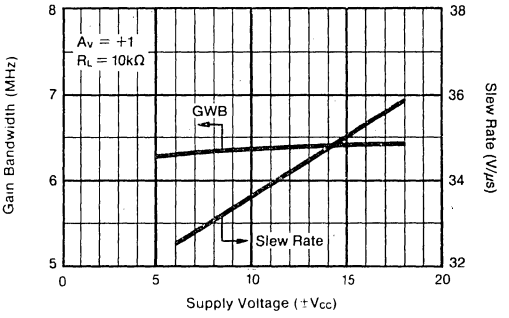
OPEN-LOOP FREQUENCY RESPONSE



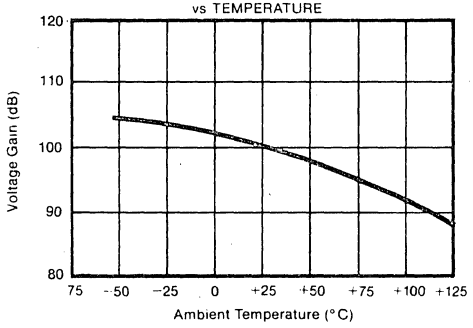
GAIN-BANDWIDTH AND SLEW RATE
vs TEMPERATURE



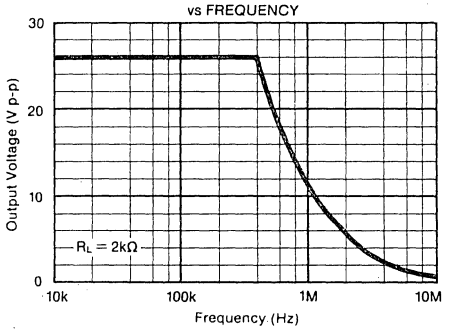
GAIN-BANDWIDTH AND SLEW RATE
vs SUPPLY VOLTAGE



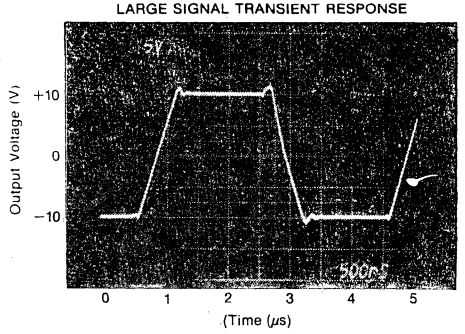
OPEN-LOOP GAIN
vs TEMPERATURE



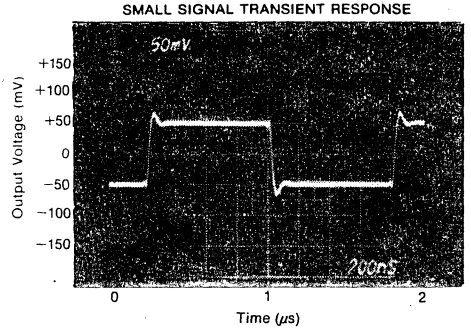
MAXIMUM OUTPUT VOLTAGE SWING
vs FREQUENCY



LARGE SIGNAL TRANSIENT RESPONSE

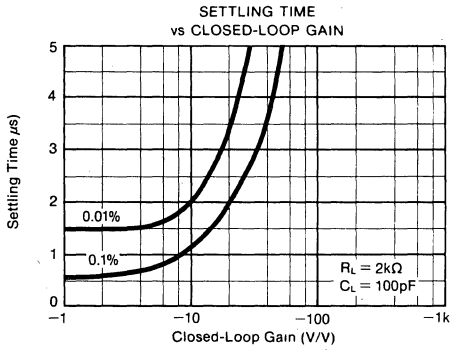


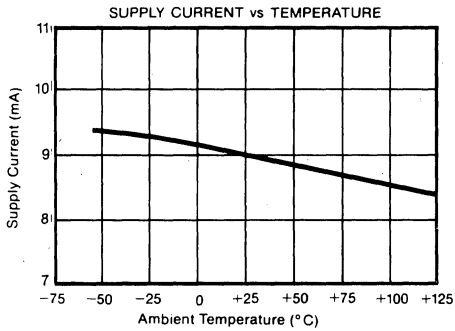
SMALL SIGNAL TRANSIENT RESPONSE

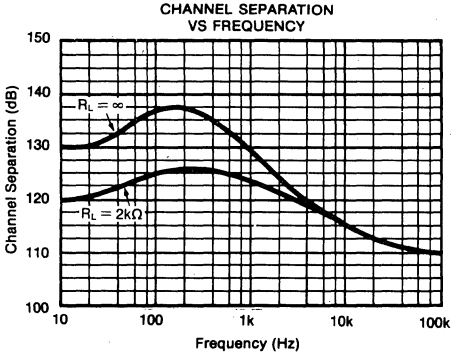


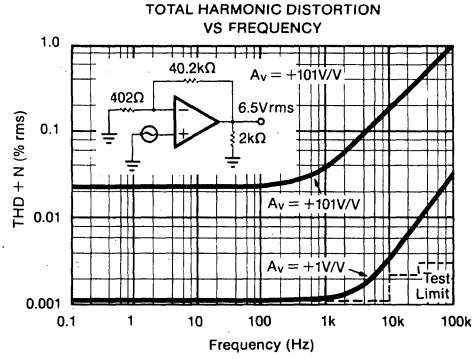
TYPICAL PERFORMANCE CURVES [CONT]

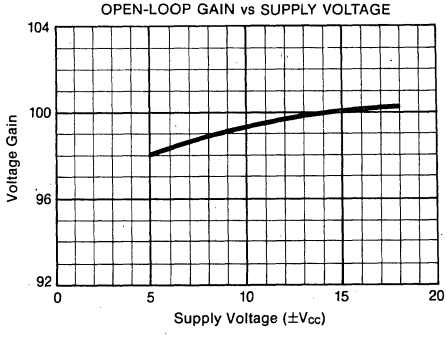
T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted











APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA404 offset voltage is laser-trimmed and will require no further trim for most applications. If desired, offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

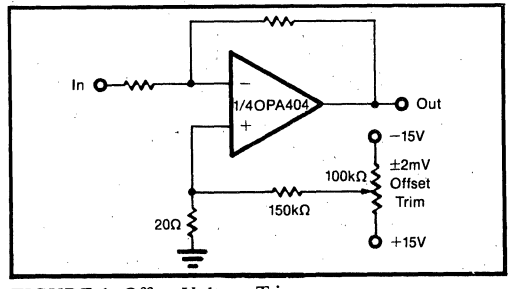


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET® amplifiers can be destroyed by the loss of $-V_{CC}$

Unlike BIFET® amplifiers, the ***Difet®*** OPA404 requires input current limiting resistors only if its input voltage can exceed −8V. A 10kΩ series resistor will limit the input current to a safe value with up to ±15V input levels even if both supply voltages are lost. (See Figure 2 and Absolute Maximum Ratings).

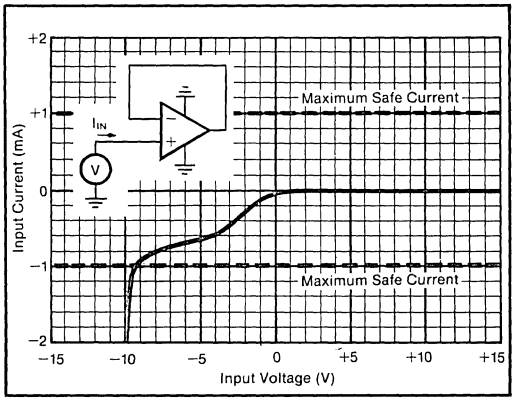


FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA404. To avoid leakage, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input ptotential (see Figure 3).

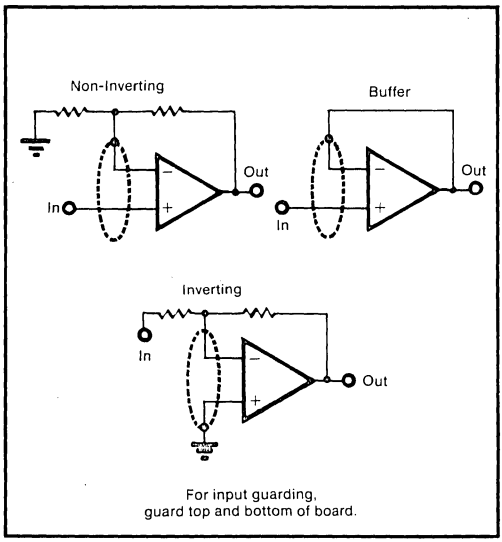


FIGURE 3. Connection of Input Guard.

HANDLING AND TESTING

Measuring the unusually low bias current of the OPA404 is difficult without specialized test equipment; most commercial benchtop testers cannot accurately measure the OPA404 bias current. Low-leakage test sockets and special test fixtures are recommended if incoming inspection of bias current is to be performed.

To prevent surface leakage between pins, the DIP package should not be handled by bare fingers. Oils and salts from fingerprints or careless handling can create leakage currents that exceed the specified OPA404 bias currents.

If necessary, DIP packages and PC board assemblies can be cleaned with Freon TF®, baked for 30 minutes at 85°C, rinsed with de-ionized water, and baked again for 30 minutes at 85°C. Surface contamination can be prevented by the application of a high-quality conformal coating to the cleaned PC board assembly.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET® operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA404 is not compromised by common-mode voltage.

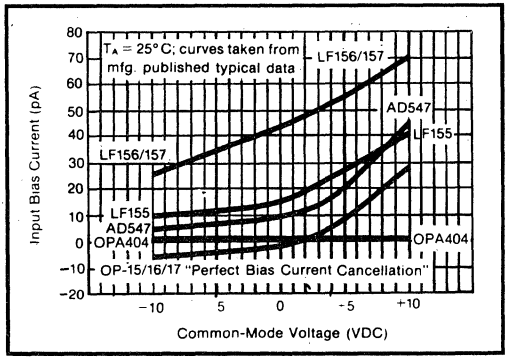


FIGURE 4. Input Bias Current Versus Common-Mode Voltage.

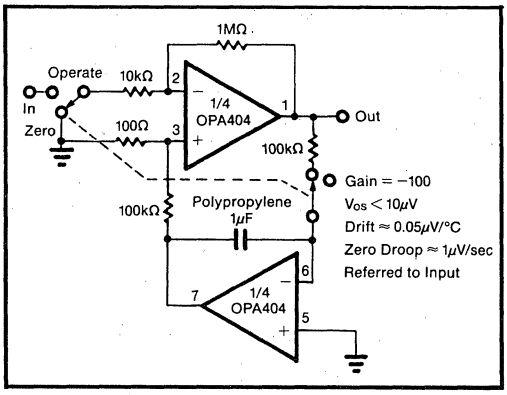


FIGURE 5. Auto-Zero Amplifier.

APPLICATIONS CIRCUITS

Figures 5 through 7 are circuit diagrams of various applications for the OPA404.

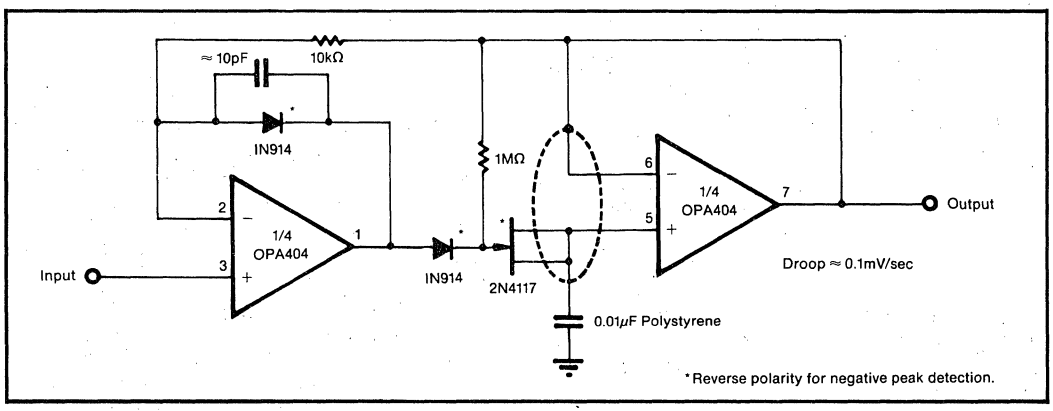


FIGURE 6. Low-Droop Positive Peak Detector.

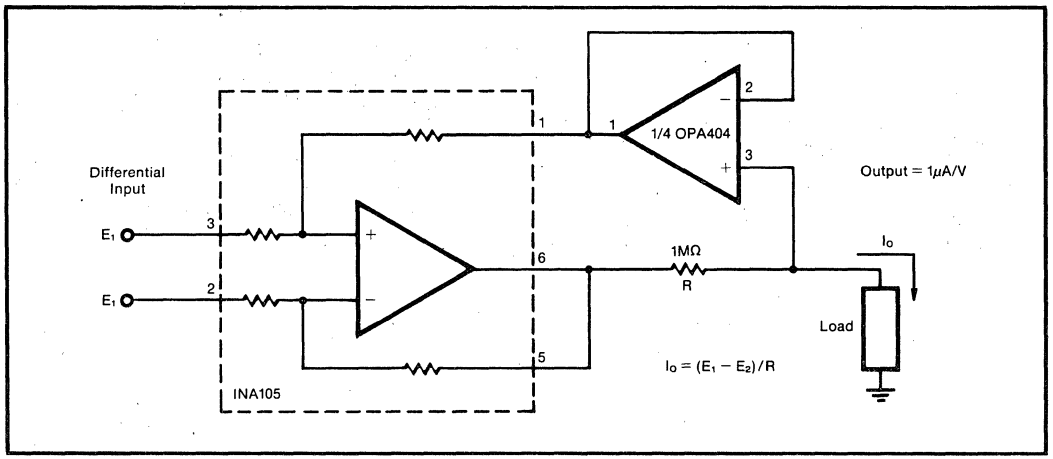


FIGURE 7. Voltage-Controlled Microamp Currrent Source.

BURR-BROWN®

OPA501

For a /883B version of this product, see OPA8785/883B in the Military Products section.

High Current - High Power OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE
  ±10 to ±40 Volts
- HIGH OUTPUT CURRENT
  ±10 Amps Peak
- HIGH OUTPUT POWER
  260 Watts Peak
- SMALL SIZE: TO-3 PACKAGE

APPLICATIONS

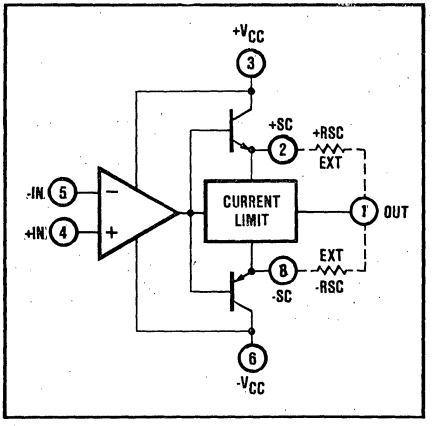
- SERVO AMPLIFIER
- MOTOR DRIVER
- ACTUATOR CONTROL
- AUDIO AMPLIFIER
- SYNCRO DRIVER
- POWER SUPPLY REGULATOR

DESCRIPTION

The OPA501 is a high power operational amplifier. Its high current output stage delivers ±10A yet the amplifier is unity-gain stable and it can be used in any operational amplifier configuration. The 260W peak output capability allows the OPA501 to drive loads (such as motors) with a greater safety margin.

Safe operating area is fully specified and output current limiting is provided to protect both the amplifier and the load from excessive current.

This hybrid IC is housed in an 8-pin hermetic TO-3 package. The electrically-isolated package allows direct mounting to chassis or heat sink without an insulating washer or spacer which would increase thermal resistance.



SIMPLIFIED CIRCUIT

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_C = +25°C and $\pm V_{CC}$ = 28VDC (OPA501RM/AM); $\pm V_{CC}$ = 34VDC (OPA501SM/BM) unless otherwise noted.

PARAMETER	CONDITIONS	OPA501RM/AM			OPA501SM/BM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RATED OUTPUT(1)(2)								
Output Current,	R_L = 2Ω (RM/AM)	±10			*			A
Continuous(3)	R_L = 2.6Ω (SM/BM)	±10			*			A
Output Voltage(3)	I_O = 10A peak	±20	23		±26	±29		V
DYNAMIC RESPONSE								
Bandwidth, Unity Gain	Small Signal		1			*		MHz
Full Power Bandwidth	V_O = 40Vp-p, R_L = 8Ω	10	16		*	*		kHz
Slew Rate	R_L = 5Ω (RM/AM)	1.35			*			V/µs
	R_L = 6.5Ω (SM/BM)	1.35			*			V/µs
INPUT OFFSET VOLTAGE								
Initial Offset			±5	±10		±2	±5	mV
vs Temperature	−25°C < T< +85°C (AM/BM)		±10	±65				µV/°C
	−55°C < T< +125°C (RM/SM)					±10	±40	µV/°C
vs Supply Voltage			±35			*		µV/V
INPUT BIAS CURRENT								
Initial	T_{case} = +25°C		15	40		*	20	nA
vs Temperature			±0.05			*		nA/°C
vs Supply Voltage			±0.02			*		nA/V
INPUT DIFFERENCE CURRENT								
Initial	T_{case} = +25°C		±5	±10		±2	±3	nA
vs Temperature	−25°C < T < +85°C (AM/BM)		±0.01					nA/°C
	−55°C < T < +125°C (RM/SM)					±0.01		nA/°C
OPEN-LOOP GAIN, DC	R_L = 5Ω (RM/AM)	94	115					dB
	R_L = 6.5Ω (SM/BM)				98	115		dB
INPUT IMPEDANCE								
Differential			10			*		MΩ
Common-mode			250			*		MΩ
INPUT NOISE								
Voltage Noise	f_n = 0.3Hz to 10Hz		3			*		µV, p-p
	f_n = 10Hz to 10kHz		5			*		µV, rms
Current Noise	f_n = 0.3Hz to 10Hz		20			*		pA, p-p
	f_n = 10Hz to 10kHz		4.5			*		pA, rms
INPUT VOLTAGE RANGE								
Common-mode Voltage(4)	Linear Operation	±(|V_{CC}|-6)	±(|V_{CC}|-3)		*	*	*	V
Common-mode Rejection	F = DC, V_{CM} = ±(|V_{CC}|-6)	70	110		80	*		dB
POWER SUPPLY								
Rated Voltage			±28			±34		V
Operating Voltage Range		±10		±36	*		±40	V
Current, quiescent			±2.6	±10		*	*	mA
TEMPERATURE RANGE	case							
Specification, RM/SM		-55		+125	*		*	°C
AM/BM		-25		+85	*		*	°C
Operating, derated performance, AM/BM		-55		+125	*		*	°C
Storage		-65		+150	*		*	°C
THERMAL RESISTANCE	Steady State θ_{JC}		2.0	2.2		*	*	°C/W

*Specification same as for OPA501RM/AM.

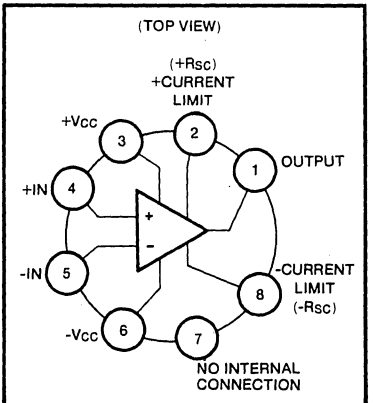
NOTES:
1. Package must be derated based on a junction to case thermal resistance of 2.2° C/W or a junction to ambient thermal resistance of 30° C/W.
2. Safe Operating Area and Power Derating Curves must be observed.
3. With $\pm R_{SC}$ = 0. Peak output current is typically greater than 10A if duty cycle and pulse width limitations are observed. Output current greater than 10A is not guaranteed.
4. The absolute maximum voltage is 3V less than supply voltage.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage (V_{CC})	±40VDC
Power dissipation at +25°C[1][2]	79W
Differential input voltage	±V_{CC}-3V
Common-mode input voltage	±V_{CC}
Operating temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10sec)	+300°C
Junction temperature	+200°C
Output short-circuit duration[3]	continuous

NOTES:
1. At case temperature of +25°C. Derate at 2.2° C/W above case temperature of +25°C.
2. Average dissipation.
3. Within safe operating area and with appropriate derating.

CONNECTION DIAGRAM



ORDERING INFORMATION

OPA501 X M

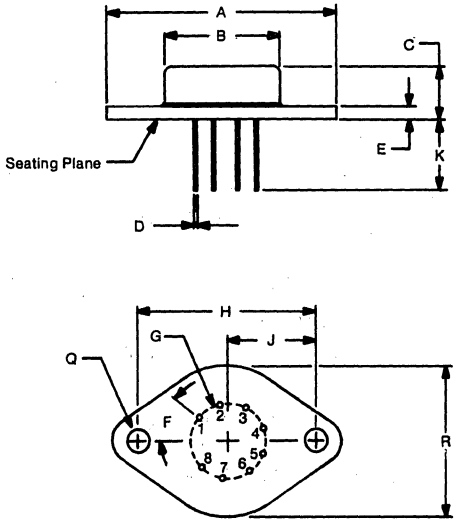
Basic Model Number

Performance Grade Code
- A, B = -25°C to +85°C
- R, S = -55°C to +125°C

Package Code
- TO-3

OPA501AM	
OPA501BM	
OPA501RM	
OPA501SM	

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

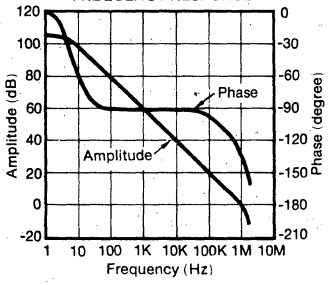
Pin numbers shown for reference only.
Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.240	.290	6.10	7.37
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.583 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

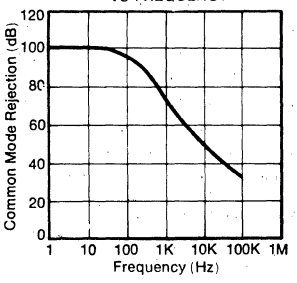
TYPICAL PERFORMANCE CURVES

(Typical at +25° case and ±Vcc = 28VDC unless otherwise noted.)

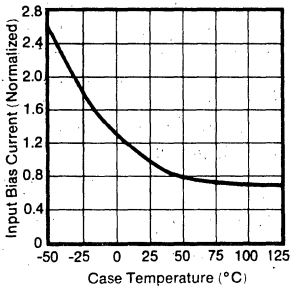
OPEN-LOOP FREQUENCY RESPONSE



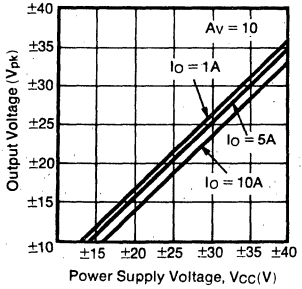
COMMON-MODE REJECTION VS FREQUENCY



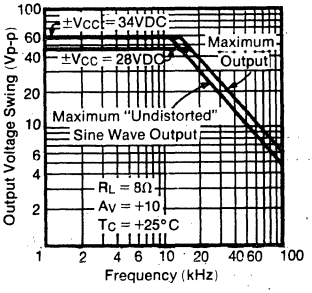
INPUT BIAS CURRENT VS TEMPERATURE



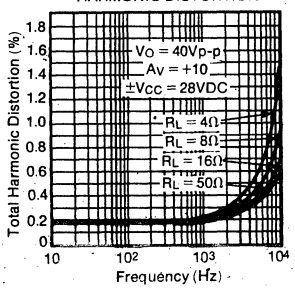
OUTPUT VOLTAGE SWING VS POWER SUPPLY VOLTAGE



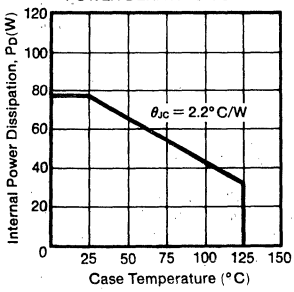
FULL POWER RESPONSE



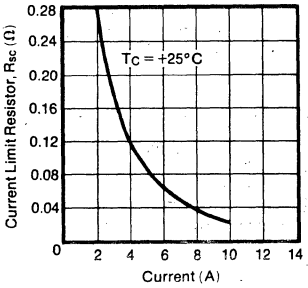
HARMONIC DISTORTION



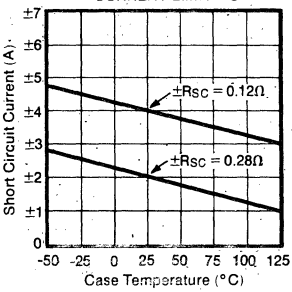
POWER DERATING CURVE



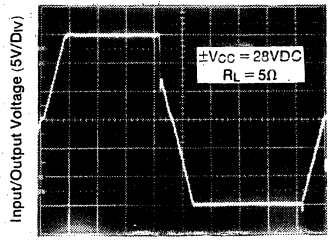
CURRENT LIMITING



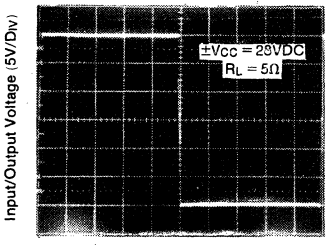
CURRENT LIMITING



PULSE RESPONSE, Av = +1



PULSE RESPONSE, AV = +1



INSTALLATION AND OPERATING INSTRUCTIONS

PROPER GROUNDING AND POWER SUPPLY BYPASSING

Particular attention should be given to proper grounding practices because the large output currents can cause significant ground-loop errors. Figure 1 illustrates proper connections.

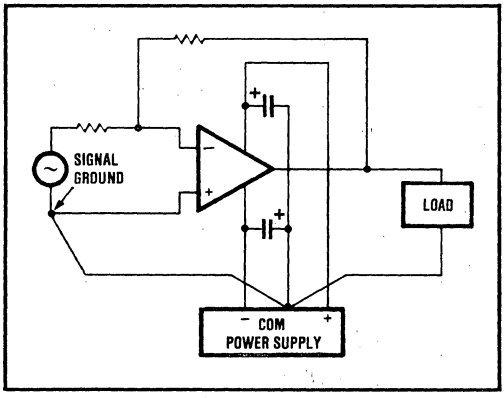


FIGURE 1. Proper Power Supply Connections.

Note that the connections are such that the load curent does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

The amplifier should be power-supply-bypassed with 10μF tantalum capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground..

CURRENT LIMITS

The OPA501 amplifier is designed so that both the positive and negative load current limits can be set independently with external resistors R_{+SC} and R_{-SC} respectively. The approximate value of these resistors is given by the equation:

$$R_{SC} = \left(\frac{0.65}{I_{LIMIT}} - 0.0437\right) \text{ ohms}$$

I_{LIMIT} is the desired maximum current in amperes. The power dissipation of the current limit resistor is:

$$P_{max} = R_{SC} (I_{LIMIT})^2 \text{ watts}$$

R_{SC} is in ohms and I_{LIMIT} is in amperes.

Current limit resistors carry the full amplifier output current so lead lengths should be minimized. Highly inductive resistors can cause loop instability. Variation in I_{LIMIT} with case temperature is shown in the Typical Performance Curves.

The amplifier should be used with as low a current limit as possible for its particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and will increase reliability by limiting internal power dissipation.

The current limits may be used to generate other functions such as constant current supplies and torque or stall current limits for servomotor applications.

HEAT SINKING

The OPA501 requires a heat sink to limit output transistor junction temperature (T_J) to an absolute maximum of +200°C. The steady-state thermal circuit is illustrated in Figure 2.

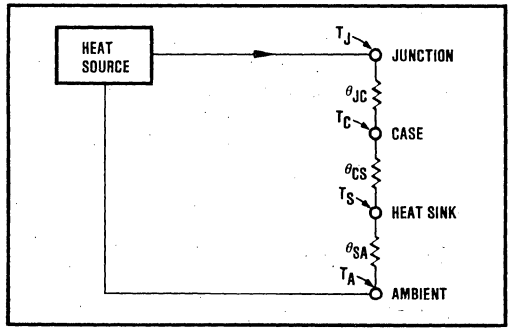


FIGURE 2. Simplified Steady-State Heat Flow Model.

Junction temperature (T_J) is found from the equation:

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$

Where P_D = average amplifier power dissipation (W)
θ_{JC} = junction to case thermal resistance (°C/W)
θ_{CS} = device mounting thermal resistance (°C/W)
θ_{SA} = heat sink thermal resistance (°C/W)
T_A = ambient temperature (°C)

For most heat sink calculations the quiescent power dissipation is very low (<1 watt) and can be disregarded with only a small error.

The minimum size heat sink can be found from the equation:

$$\theta_{SA} = \frac{T_J - T_A}{P_D} - \theta_{CS} - \theta_{JC}$$

Example: Find the maximum thermal resistance (smallest heat sink) that can be used for an OPA501 with $\pm V_{CC}$ = 28VDC. Output voltage is +10VDC across a 10Ω resistor and ambient temperature is +50°C:

$$P_D = [(+28\text{VDC}) - (+10\text{VDC})] \times \frac{+10\text{VDC}}{10\Omega} = 18\text{W}$$

$$\theta_{SA} = \frac{200°\text{C} - 50°\text{C}}{18\text{W}} - 0.1°\text{C/W} - 2.2°\text{C/W}$$

θ_{SA}= 6.03°C/W maximum

As large a heat sink as possible should be used. θ_{CS} depends on the flatness of the heat sink, the thermal compound used, and the roughness of the mating surfaces. Typical values are between 0.1°C/W and 0.3°C/W for a TO-3 package properly mounted on a heat sink.

The OPA501 mounting flange is electrically-isolated and can be mounted directly to a heat sink without insulating washers or spacers. Screws with Bellville spring washers are recommended to maintain positive clamping pressure on heat sink mounting surfaces. Long periods of thermal cycling can loosen mounting screws and increase θ_{CS}.

The output transistor thermal resistance (θ_{JC}) is a function of output current pulse width, pulse shape, and duty cycle. Long duration pulses allow the junction temperature to approach its steady state value while shorter pulses cause a lower peak junction temperature due to the junction's thermal time constant. Heat is conducted rapidly away from the junction so that as duty cycle decreases, junction temperature decreases.

Steady state θ_{JC} is rated at 2.2°C/W maximum. In applications where the amplifier's output current alternates between output transistors–for example, an AC amplifier–the transistor θ_{JC} will depend on frequency as shown in Figure 3.

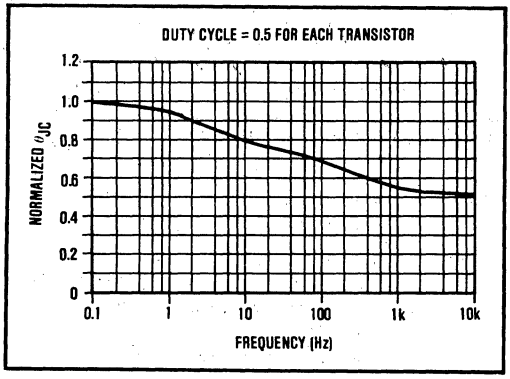


FIGURE 3. Effective θ_{JC} for Applications Where Output Current Alternates Between Output Transistors.

Example: OPA501SM with $\pm V_{CC}$ = 28VDC; heat sink θ_{SA} = 0.4°C/W; output = 11.2VAC, rms 400Hz (sine) at 5A, rms; Power Factor = 1.0; assume a mounting resistance of 0.1°C/W and an ambient temperature of +25°C.

The power dissipated by the OPA501, P_D, is equal to the power delivered by the power supplies, P_S, minus the power delivered to the load, P_L.

Peak output current is $(5A)(\sqrt{2}) = 7.07A$ peak.
$P_S = (V_{CC})(I_{AVG}) = (28V)(2/\pi)(7.07A) = 126W$.

Note that the power delivered by the power supply is equal to its voltage times the *average* current (not rms). Average is equal to $2/\pi$ times peak for a sine wave.

$P_L = (11.2VAC)(5A) = 56W$.

Average power dissipation of the amplifier is 126W − 56W = 70W. From Figure 3, the effective value of θ_{JC} at 400Hz is 0.6 × the rated θ_{JC}, threrfore, θ_{JC} = 1.32°C/W. This accounts for the fact that each output transistor is "resting" during alternate half cycles.

The junction temperature will be:

$$T_J = (70W)(1.32 + 0.1 + 0.4°C/W) + 25°C = 152°C.$$

This is well below the maximum junction temperature limit of 200°C. Best circuit reliability can be achieved, however, by keeping junction temperature to a minimum. In this case, a lower $\pm V_{CC}$ could be used to further reduce amplifier power dissipation.

At frequencies of 50Hz or less the junction temperature will change in response to the instantaneous dissipation—the product of the instantaneous voltage and current across the power transistors. Under approximately 50Hz the junction will heat in response to the peak dissipation condition which occurs at an output of one-half the power supply voltage. In the previous example, the peak dissipation can be found as follows:

Peak dissipation occurs at half of 28V = 14V output.
The load impedance Z_{LOAD} = 11.2V/5A = 2.24Ω.
The load current at peak dissipation = 14V/2.24Ω = 6.25A.
The peak dissipation = (14V)(6.25A) = 87.5W.

Furthermore, the θ_{JC} at this low frequency is equal to its specified value of 2.2°C/W (see Figure 3). In this case, the junction temperature would be:

$$T_J = (87.5W)(2.2 + 0.1 + 0.4°C/W) + 25°C = 261°C.$$

This exceeds the maximum specified junction temperature and is clearly unacceptable. More examples of this type of calculation can be found in Burr-Brown Application Note AN-123.

SAFE OPERATING AREA (SOA)

In addition to the limits imposed by power dissipation, the amplifier's output transistors are also limited by a

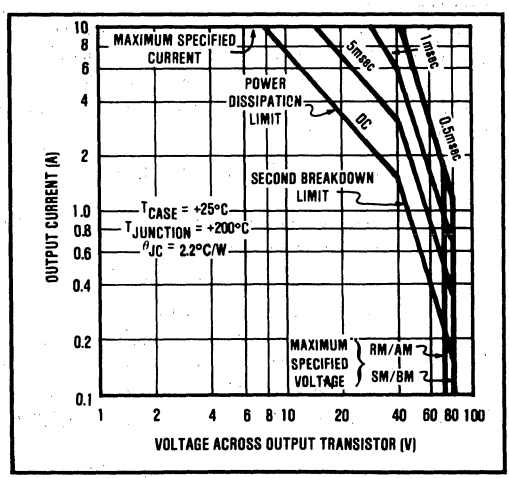


FIGURE 4. Transistor Safe Operating Area at +25°C Case Temperature.

second breakdown region. This occurs because of increased emitter current density due to current crowding at higher operating voltages. Both the dissipation and second breakdown limits depend on time and temperature. Figure 4 shows each output transistor's SOA at a case temperature of +25°C.

Limits for short pulse widths are substantially greater than for steady state (DC). At a case temperature of +125°C the SOA limits are reduced (see Figure 5). The SOA shown in these curves is based on a conservative linear derating of both the power dissipation and the second breakdown region.

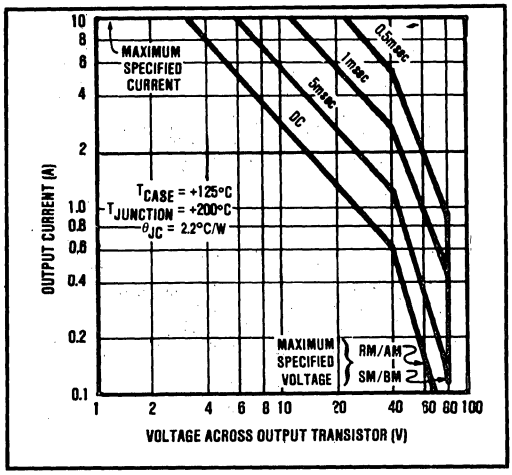


FIGURE 5. Transistor Safe Operating Area at +125°C Case Temperature.

Resistive loads are easy to analyze by simply plotting load lines on the SOA curve. If the curve representing the load line stays within the OPA501 output transistor SOA curve and all other parameters are observed, such as case temperature, etc., the amplifier will be safe. The load line can swing through the larger SOA limits if their time duration constraints are strictly observed.

Reactive loads present a more complex problem since the output voltage and current are not in phase. This results in the reactive load line becoming elliptical (when plotted on linear axes) which requires a larger SOA for safe operation.

Although detailed analysis is beyond the scope of this data sheet, the load line can be viewed on an oscilloscope as shown in Figure 6. The X-Y display is driven by the voltage across the load and by the current into the load.

This set up can also display voltage and current stress across the OPA501 output transistors as shown in Figure 7. This data can then be compared to the SOA limits.

The amplifier is designed to operate with electromotive-force-generating loads such as servomotors, relays, and actuators. Careful attention must be paid to both the load characteristics and the amplifier's SOA to ensure safe operation.

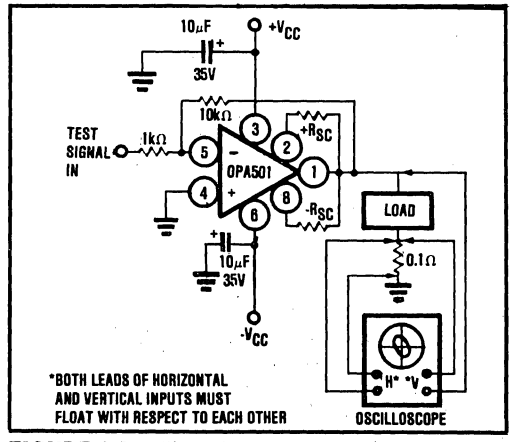


FIGURE 6. Loadline Display.

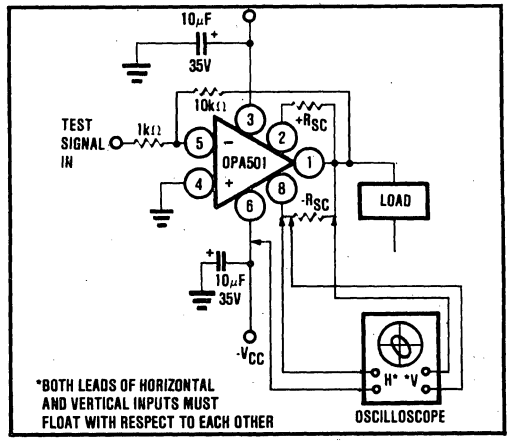


FIGURE 7. Output Transistor Safe Operating Area Stress Display.

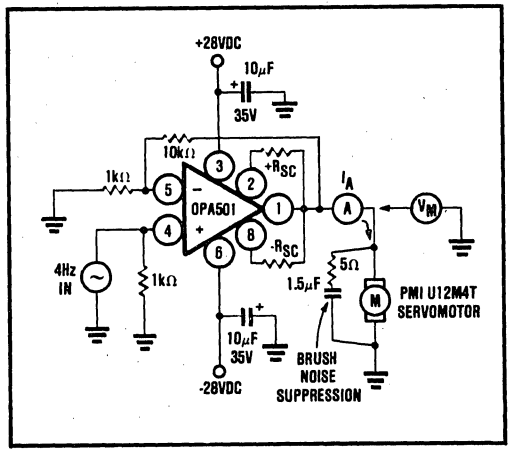


FIGURE 8. Servomotor Amplifier.

Figure 8 shows the OPA501 configured as a DC permanent magnet motor driver. The armature current (I_A) and motor voltage (V_m) are monitored within an oscilloscope in the X-Y mode displaying I_A and V_m respectively. Slewing the motor with a 4Hz sine wave results in the motor power ellipse of Figure 9. The input level has been adjusted to give ±20V, pk, across the motor. An examination of the power ellipse indicates that the instan-

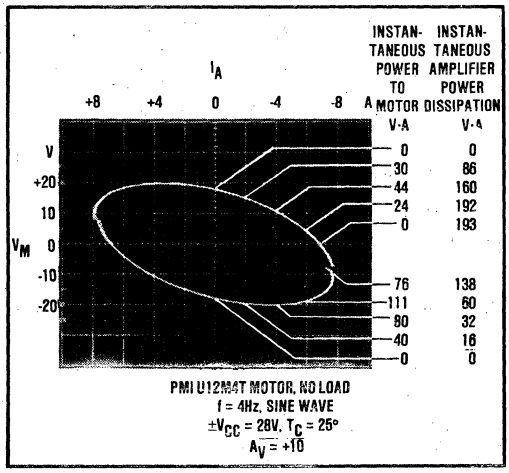


FIGURE 9. D.C. Servomotor Load Line.

taneous power delivered to the motor exceeds the amplifier output transistor's safe operating area at a case temperature of +25°C. The point at which the motor shows 0V at -6.9A is a problem. The voltage across the output transistor is 28V - 0V = 28V. Checking the SOA curve shows that the amplifier can safely withstand this condition for slightly under 5msec. At 4Hz this transient swing outside the DC SOA region is exceeded for much longer than 5msec. Continued operation under these conditions will result in failure. Peak junction temperatures should not exceed +200°C. Perhaps a motor with a higher impedance winding should be considered for this application. Current limiting and lower supply voltage can also reduce dissipation.

Motors used in servo applications often required a surprisingly large current to accelerate quickly. Worst case conditions occur when the motor is operating at full speed and is suddenly slammed into reverse ("plugging"). This condition is illustrated in Figure 10 when a DC servomotor is driven by a bipolar square wave. As the motor reverses direction a large surge current flows, causing very high peak power dissipation in the amplifier. After several time constants (determined by the inertia moment) the current drops to a lower steady-state value. Loading the motor increases the motor average power and amplifier dissipation. SOA curves should be checked for safe operation under these surge conditions.

The OPA501 current limits may be set to clip the high surge currents to a safe level. This is shown in Figure 11. Note that the current limit does limit the servo motor peak acceleration.

Inductive loads should be investigated for high peak transients generated by a collapsing magnetic field. Resistive damping can reduce this problem and although the amplifier has substrate diodes as part of the Darlington output transistor structure, external diodes are recommended for heavy clamping.

Fast diodes such as those normally used as rectifiers in switching power supplies are suitable.

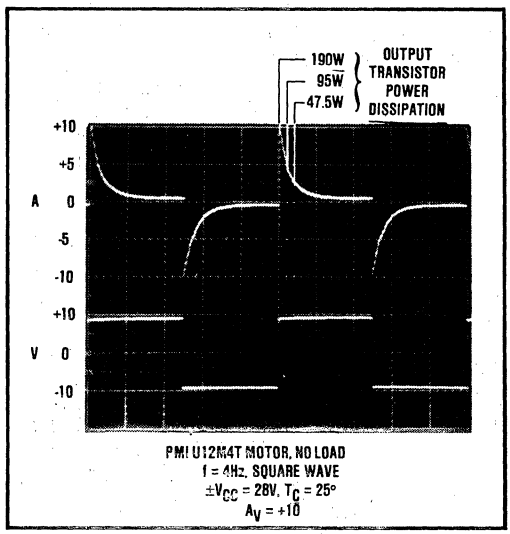


FIGURE 10. Servomotor Drive – "Plugging"

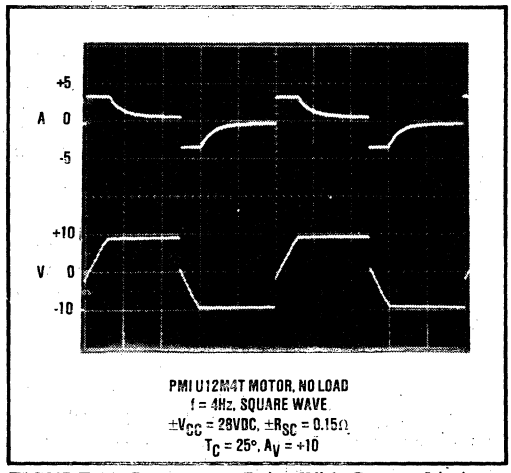


FIGURE 11. Servomotor Drive With Current Limit.

BURR-BROWN®

OPA511

High Current—High Power OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE: ±10V to ±30V
- HIGH OUTPUT CURRENT: 5A peak
- CLASS A/B OUTPUT STAGE: Low distortion
- SMALL TO-3 PACKAGE

APPLICATIONS

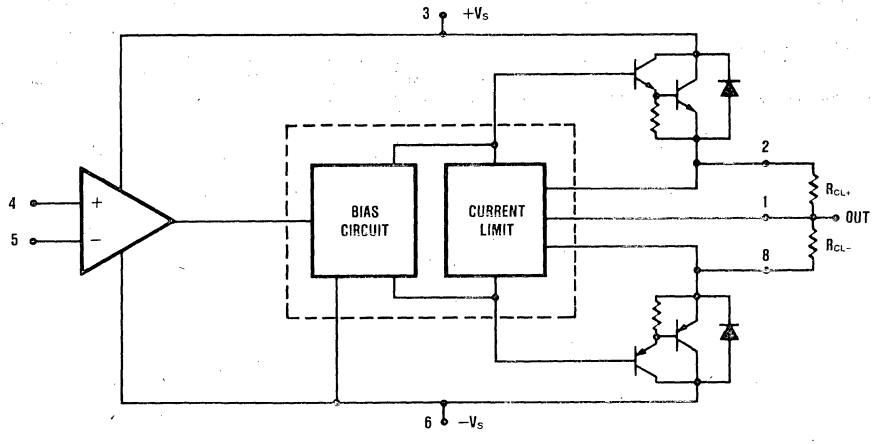
- SERVO AMPLIFIER
- MOTOR DRIVER
- SYNCRO EXCITATION
- AUDIO AMPLIFIER
- TEST PIN DRIVER

DESCRIPTION

The OPA511 is a high voltage, high current operational amplifier designed to drive a wide variety of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from cross-over distortion. User-set current limit circuitry provides protection to the amplifier and load in fault conditions.

The OPA511 employs a laser-trimmed monolithic integrated circuit to bias the output transistors, providing excellent low-level signal fidelity and high output voltage swing. The reduced internal parts count made possible with this bias IC improves performance and reliability.

This hybrid integrated circuit is housed in a hermetically sealed TO-3 package and all circuitry is electrically isolated from the case. This allows direct mounting to a chassis or heat sink without cumbersome insulating hardware and provides optimum heat transfer.



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SPECIFICATIONS

ELECTRICAL

At T_C = +25°C and V_S = ±28VDC unless otherwise noted.

PARAMETER	CONDITIONS	OPA511AM MIN	OPA511AM TYP	OPA511AM MAX	UNITS
INPUT					
OFFSET VOLTAGE					
Initial Offset			±5	±10	mV
vs Temperature	Full temperature range		±10	±65	µV/°C
vs Supply Voltage			±35	±200	µV/V
vs Power			±20		µV/W
BIAS CURRENT					
Initial			±15	±40	nA
vs Temperature	Full temperature range		±0.05	±0.4	nA/°C
vs Supply Voltage			±0.02		nA/V
OFFSET CURRENT					
Initial			±5	±10	nA
vs Temperature	Full temperature range		±0.01		nA/°C
INPUT IMPEDANCE					
Common-Mode			200		MΩ
Differential			10		MΩ
VOLTAGE RANGE[1]					
Common-Mode Voltage	Full temperature range	±(|V_S| − 6)	±(|V_S| − 3)		V
Common-Mode Rejection	V_{CM} = V_S − 6V	70	110		dB
GAIN					
Open-Loop Gain at 10Hz	Full temperature range, full load	91	113		dB
Gain-Bandwidth Product at 1MHz	T_C = +25°C, full load		1		MHz
Power Bandwidth	T_C = +25°C, I_O = 4A, V_O = 40V p-p	15	23		kHz
Phase Margin	Full temperature range		45		Degrees
OUTPUT					
Voltage Swing	I_O = 5A	±(|V_S| − 8)	±(|V_S| − 5)		V
	Full temperature range, I_O = 2A	±(|V_S| − 6)	±(|V_S| − 5)		V
	Full temperature range, I_O = 56mA	±(|V_S| − 5)			V
Current, Peak		±5			A
Settling Time to 0.1%	2V step		2		µs
Slew Rate	R_L = 2.5Ω	±1.0	1.8		V/µs
Capacitive Load: Unity Gain	Full temperature range			3.3	nF
Gain > 4	Full temperature range			SOA[2]	
POWER SUPPLY					
Voltage	Full temperature range	±10	±28	±30	V
Current, Quiescent			20	30	mA
THERMAL					
RESISTANCE					
AC Junction to Case[3]	f > 60Hz		1.9	2.1	°C/W
DC Junction to Case	f > 60Hz		2.4	2.6	°C/W
Junction to Air			30		°C/W
TEMPERATURE RANGE, case		−25		+85	°C

NOTES: (1) +V_S and −V_S denote the positive and negative supply voltage respectively. Total V_S is measured from +V_S to −V_S. (2) SOA = Safe Operating Area. (3) Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$	68V
Output Current: source	5A
sink	see SOA
Power Dissipation, internal[1]	67W
Input Voltage: differential	$\pm(\|V_S\| - 3V)$
common-mode	$\pm V_S$
Temperature: junction[1]	+200°C
pin solder, 10sec	+300°C
Temperature Range: storage	−65°C to +150°C
operating (case)	−25°C to +85°C

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

ORDERING INFORMATION

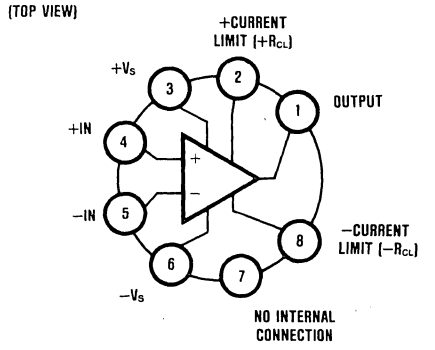
OPA511 A M

Basic Model Number

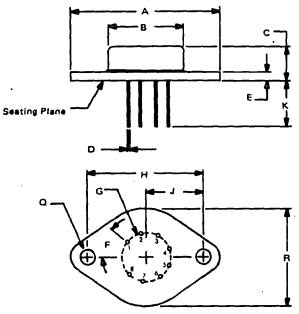
Grade Code

Package Code (TO-3)

CONNECTION DIAGRAM



MECHANICAL



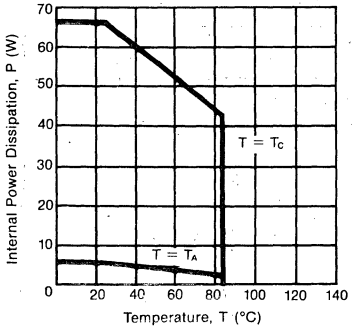
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.240	.290	6.10	7.37
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.583 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

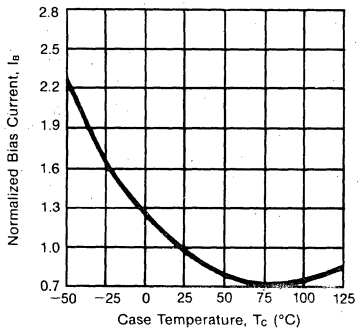
TYPICAL PERFORMANCE CURVES

T_A = 25°C. V_S = ±28VDC unless otherwise noted.

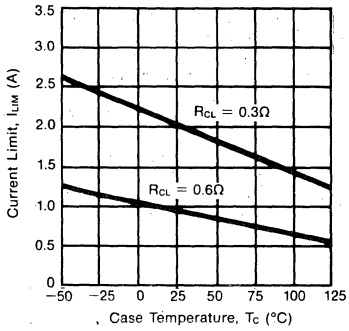
POWER DERATING



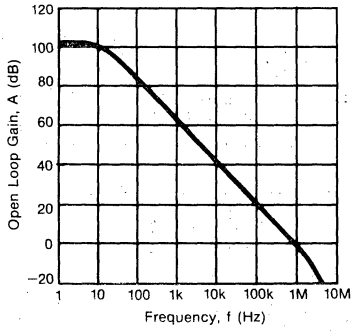
BIAS CURRENT



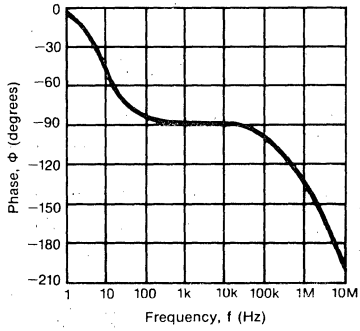
CURRENT LIMIT



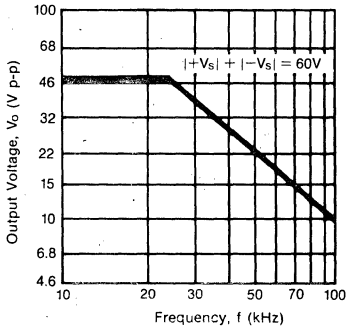
SMALL SIGNAL RESPONSE



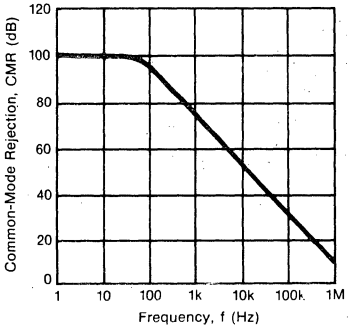
PHASE RESPONSE



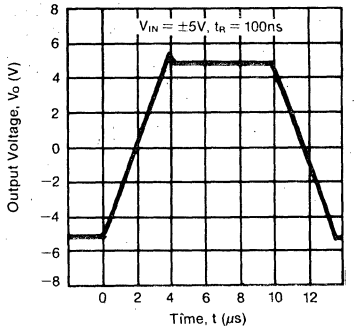
POWER RESPONSE



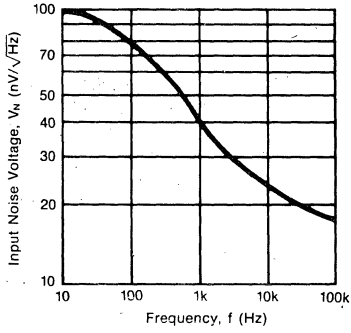
COMMON-MODE REJECTION



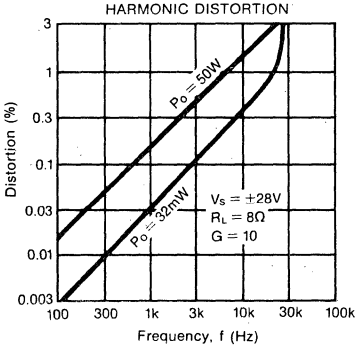
PULSE RESPONSE



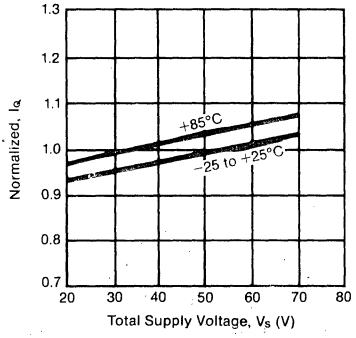
INPUT NOISE



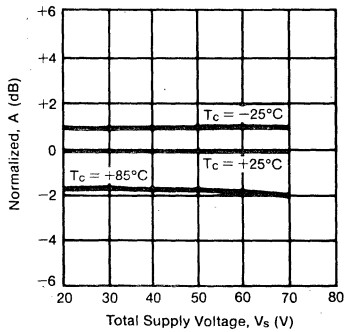
HARMONIC DISTORTION



QUIESCENT CURRENT



OPEN LOOP GAIN



APPLICATIONS INFORMATION

POWER SUPPLIES

Specifications for the OPA511 are based on a nominal operating voltage of ±28V. A single power supply or unbalanced supplies may be used so long as the maximum total operating voltage (total of $+V_S$ and $-V_S$) is not greater than 68V.

CURRENT LIMITS

Current limit resistors must be provided for proper operation. Independent positive and negative current limit values may be selected by choice of R_{CL+} and R_{CL-} respectively. Resistor values are calculated by:

$$R_{CL} = 0.65 / I_{LIM} \text{ (amps)} - 0.01$$

This is the nominal current limit value at room temperature. The maximum output current decreases at high temperature as shown in the typical performance curve. Most wire-wound resistors are satisfactory, but some highly inductive types may cause loop stability problems. Be sure to evaluate performance with the actual resistors to be used in production.

HEAT SINKING

Power amplifiers are rated by case temperature (not ambient temperature). The maximum allowable power dissipation is a function of the case temperature as shown in the power derating curve. Load characteristics, signal conditions, and power supply voltage determine the power dissipated by the amplifier. The case temperature will be determined by the heat sinking conditions. Sufficient heat sinking must be provided to keep the case temperature within safe bounds given the power dissipated and ambient temperature. See Applications Note AN-83 for further details.

SAFE OPERATING AREA (SOA)

The safe area plot provides a comprehensive summary of the power handling limitations of a power amplifier, including maximum current, voltage and power as well as the secondary breakdown region (see Figure 1). It shows the allowable output current as a function of the power supply to output voltage differential (voltage across the conducting power device). See Applications Note AN-123 for details on SOA.

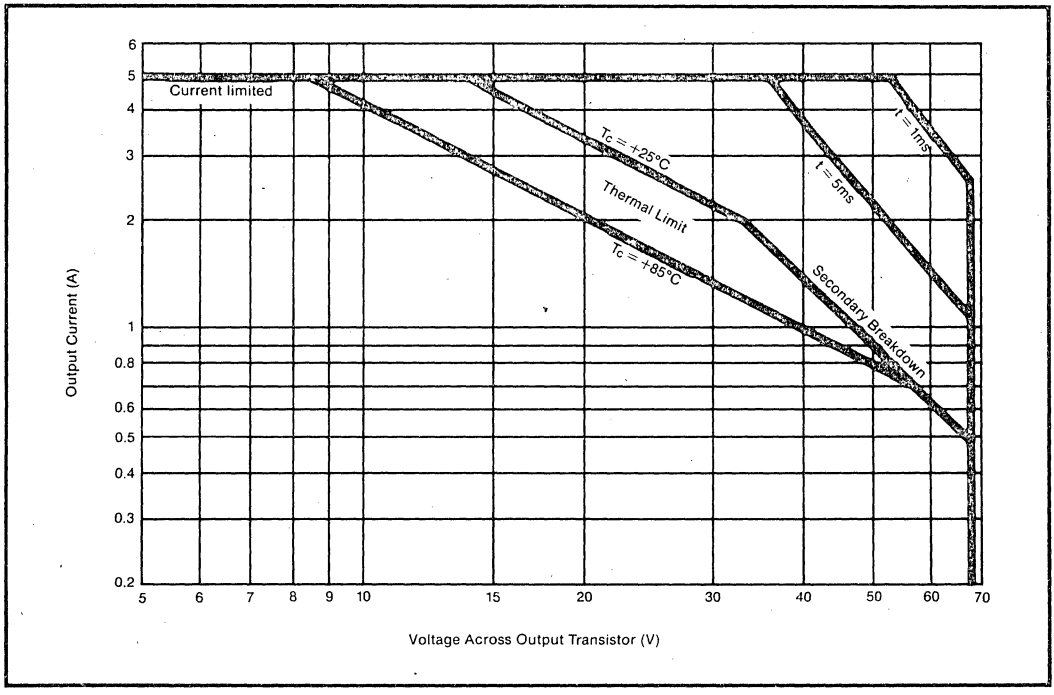


FIGURE 1. Safe Operating Area.

BURR-BROWN®

OPA512

Very-High Current—High Power OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE: ±10V to ±50V
- HIGH OUTPUT CURRENT: 15A peak
- CLASS A/B OUTPUT STAGE: Low distortion
- VOLTAGE-CURRENT LIMIT PROTECTION CIRCUIT
- SMALL TO-3 PACKAGE

APPLICATIONS

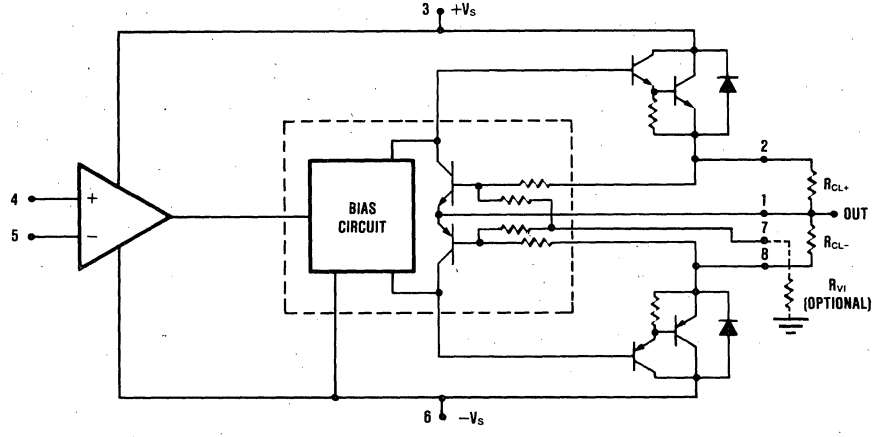
- SERVO AMPLIFIER
- MOTOR DRIVER
- SYNCRO EXCITATION
- AUDIO AMPLIFIER
- TEST PIN DRIVER

DESCRIPTION

The OPA512 is a high voltage, very-high current operational amplifier designed to drive a wide variety of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from cross-over distortion. User-set current limit circuitry provides protection to the amplifier and load in fault conditions. A resistor-programmable voltage-current limiter circuit may be used to further protect the amplifier from damaging conditions.

The OPA512 employs a laser-trimmed monolithic integrated circuit to bias the output transistors, providing excellent low-level signal fidelity and high output voltage swing. The reduced internal parts count made possible with this monolithic IC improves performance and reliability.

This hybrid integrated circuit is housed in a hermetically-sealed TO-3 package and all circuitry is electrically-isolated from the case. This allows direct mounting to a chassis or heat sink without cumbersome insulating hardware and provides optimum heat transfer.



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SPECIFICATIONS

ELECTRICAL

At T_C = +25°C and V_S = ±40VDC unless otherwise noted.

PARAMETER	CONDITIONS	OPA512BM MIN	OPA512BM TYP	OPA512BM MAX	OPA512SM MIN	OPA512SM TYP	OPA512SM MAX	UNITS
INPUT								
OFFSET VOLTAGE								
Initial Offset			±2	±6		±1	±3	mV
vs Temperature	Specified temp. range		±10	±65		*	±40	µV/°C
vs Supply Voltage			±30	±200		*	*	µV/V
vs Power			±20			*		µV/W
BIAS CURRENT								
Initial			12	30		10	20	nA
vs Temperature	Specified temp. range		±50	400		*	*	pA/°C
vs Supply Voltage			±10			*		pA/V
OFFSET CURRENT								
Initial			±12	±30		±5	±10	nA
vs Temperature	Specified temp. range		±50			*		pA/°C
INPUT IMPEDANCE, DC			200			*		MΩ
INPUT CAPACITANCE			3			*		pF
VOLTAGE RANGE								
Common-Mode Voltage	Specified temp. range	±(|V_S| − 5)	±(|V_S| − 3)		*	*		V
Common-Mode Rejection	Specified temp. range	74	100		*	*		dB
GAIN								
Open-Loop Gain at 10Hz	1kΩ load		110			*		dB
	Specified temp. range, 8Ω load	96	108		*	*		dB
Gain-Bandwidth Product, 1MHz	8Ω load		4			*		MHz
Power Bandwidth	8Ω load	13	20		*	*		kHz
Phase Margin	Specified temp. range, 8Ω load		20			*		Degrees
OUTPUT								
Voltage Swing[1]	BM at 10A, SM at 15A	±(|V_S| − 6)			±(|V_S| − 7)			V
	Specified temp. range, I_O = 80mA	±(|V_S| − 5)			*			V
	I_O = 5A	±(|V_S| − 5)			*			V
Current, Peak		10			15			A
Settling Time to 0.1%	2V step		2			*		µs
Slew Rate		2.5	4		*	*		V/µs
Capacitive Load	Specified temp. range, G = 1			1.5			*	nF
	Specified temp. range, G > 10			SOA[2]			*	
POWER SUPPLY								
Voltage	Specified temp. range	±10	±40	±45	*	*	±50	V
Current, Quiescent			25	50		*	35	mA
THERMAL								
RESISTANCE								
AC Junction to Case[3]	T_C = −55°C to +125°C, f > 60Hz		0.8	0.9		*	*	°C/W
DC Junction to Case	T_C = −55°C to +125°C		1.25	1.4		*	*	°C/W
Junction to Air	T_C = −55°C to +125°C		30			*		°C/W
TEMPERATURE RANGE, specified	T_C	−25		+85	−55		+125	°C

*Specification same as OPA512BM.

NOTES: (1) +V_S and −V_S denote the positive and negative supply voltage respectively. Total V_S is measured from +V_S to −V_S. (2) SOA = Safe Operating Area. (3) Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$	100V
Output Current: source	15A
sink	see SOA
Power Dissipation, internal[1]	125W
Input Voltage: differential	$\pm(\|V_S\| - 3V)$
common-mode	$\pm V_S$
Temperature: pin solder, 10s	+300°C
junction[1]	+200°C
Temperature Range: storage[2]	−65°C to +150°C
operating (case)	−55°C to +125°C

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. (2) OPA512BM, −55°C to +100°C.

ORDERING INFORMATION

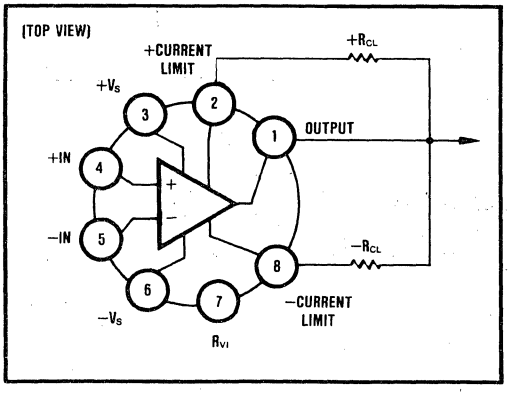
OPA512 X M

Basic Model Number

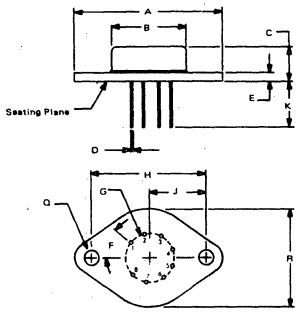
Performance Grade Code
B = −25°C to +85°C
S = −55°C to +125°C

Package Code (TO-3)
M = TO-3

CONNECTION DIAGRAM



MECHANICAL



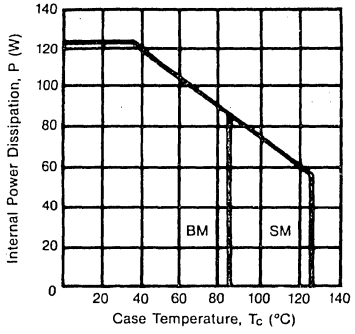
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.240	.290	6.10	7.37
D	.038	.042	.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

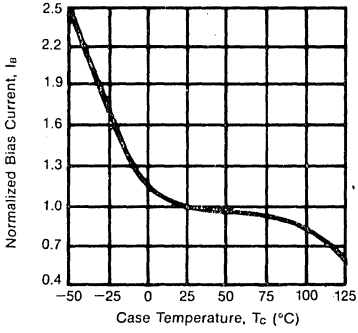
TYPICAL PERFORMANCE CURVES

T_A = 25°C, V_S = ±40VDC unless otherwise noted.

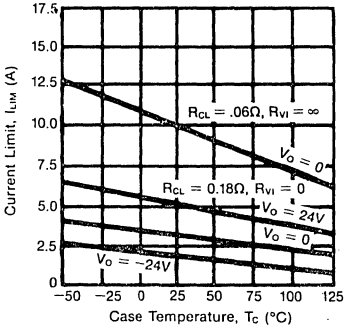
POWER DERATING



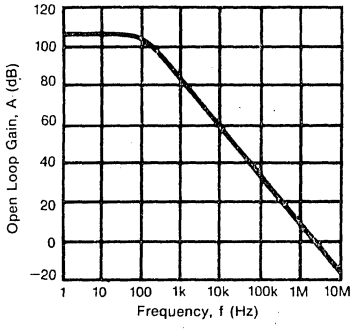
BIAS CURRENT



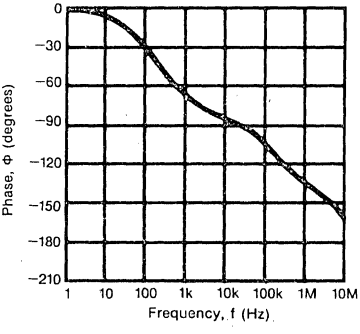
CURRENT LIMIT



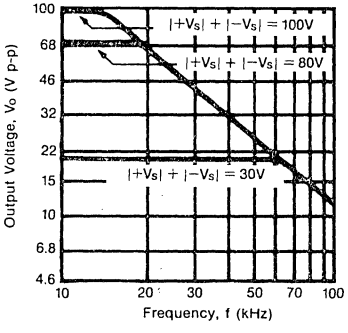
SMALL SIGNAL RESPONSE



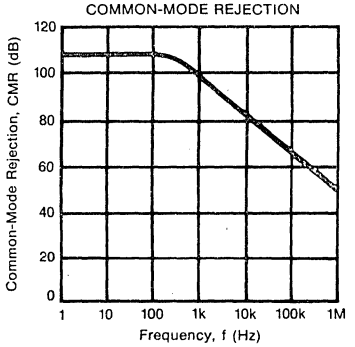
PHASE RESPONSE



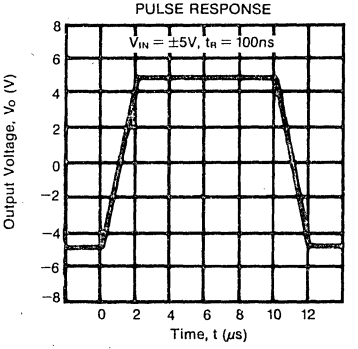
POWER RESPONSE



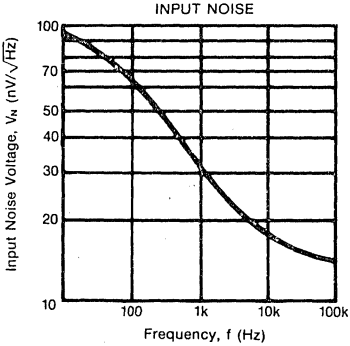
COMMON-MODE REJECTION



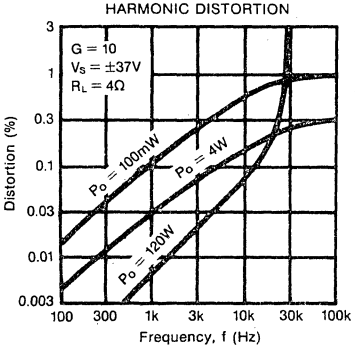
PULSE RESPONSE



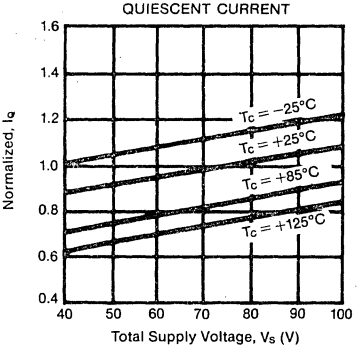
INPUT NOISE



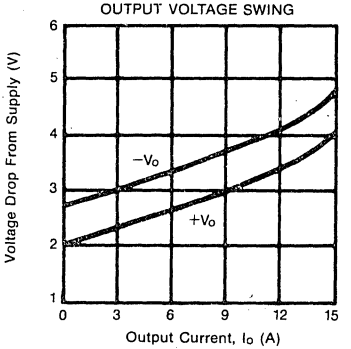
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



APPLICATIONS INFORMATION

POWER SUPPLIES

Specifications for the OPA512 are based on a nominal operating voltage of ±40V. A single power supply or unbalanced supplies may be used as long as the maximum total operating voltage (total of $+V_S$ and $-V_S$) is not greater than 90V (100V for "S" grade version).

CURRENT LIMITS

Current limit resistors must be provided for proper operation. Independent positive and negative current limit values may be selected by choice of R_{CL+} and R_{CL-} respectively. Resistor values are calculated by:

$$R_{CL} = 0.65/I_{LIM} \text{ (amps)} - 0.007$$

This is the nominal current limit value at room temperature. The maximum output current decreases at high temperature as shown in the typical performance curve. Most wire-wound resistors are satisfactory, but some highly inductive types may cause loop stability problems. Be sure to evaluate performance with the actual resistors to be used in production.

HEAT SINKING

Power amplifiers are rated by case temperature (not ambient temperature). The maximum allowable power dissipation is a function of the case temperature as shown in the power derating curve. Load characteristics, signal conditions, and power supply voltage determine the power dissipated by the amplifier. The case temperature will be determined by the heat sinking conditions. Sufficient heat sinking must be provided to keep the case temperature within safe bounds given the power dissipated and ambient temperature. See Applications Note AN-83 for further details.

SAFE OPERATING AREA (SOA)

The safe area plot provides a comprehensive summary of the power handling limitations of a power amplifier, including maximum current, voltage and power as well as the secondary breakdown region (see Figure 1). It shows the allowable output current as a function of the power supply to output voltage differential (voltage across the conducting power device). See Applications Note AN-123 for details on SOA.

VOLTAGE-CURRENT LIMITER CIRCUITRY

The voltage-current (V-I) limiter circuit provides a means to protect the amplifier from SOA damage such as a short circuit to ground, yet allows high output currents to flow under normal load conditions. Sensing both the output current and the output voltage, this limiter circuit increases the current limit value as the output voltage approaches the power supply voltage (where power dissipation is low). This type of limiting is achieved by connecting pin 7 through a programming resistor to ground. The V-I limiter circuit is governed by the equation:

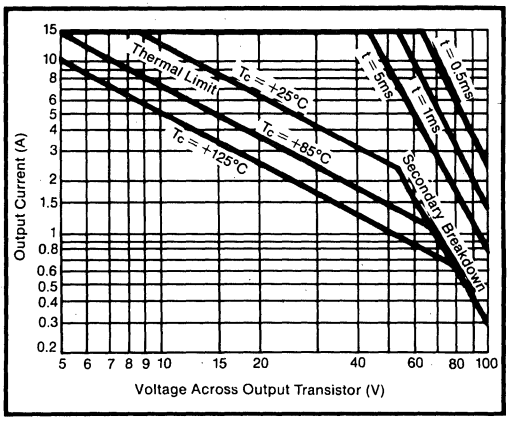


FIGURE 1. Safe Operating Area.

$$I_{LIMIT} = \frac{0.65 + \dfrac{0.28\ V_O}{20 + R_{VI}}}{R_{CL} + 0.007}$$

where:

I_{LIMIT} is the maximum current available at a given output voltage.

R_{VI} is the value (kΩ) of the resistor from pin 7 to ground.

R_{CL} is the current limit resistor in ohms.

V_O is the instantaneous output voltage in volts.

Reactive or EMF generating loads may produce unusual (perhaps undesirable) waveforms with the V-I limit circuit driven into limit. Since current peaks in a reactive load do not align with the output voltage peaks, the output waveform will not appear as a simple voltage-limited waveform. Response of the load to the limiter, in fact, may produce a "backfire" reaction producing unusual output waveforms.

BURR-BROWN®

OPA600

Fast-Settling Wideband OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 80ns to ±0.1%
  115ns to ±0.01%
- FULL DIFFERENTIAL FET INPUT
- −25°C to +85°C AND
  −55°C to +125°C TEMPERATURE RANGES
- ±10V OUTPUT; 200mA
- GAIN BANDWIDTH PRODUCT: 5GHz

APPLICATIONS

- VOLTAGE CONTROLLED OSCILLATOR DRIVER
- LARGE SIGNAL, WIDEBAND DRIVERS
- HIGH SPEED D/A CONVERTER OUTPUT AMPLIFIER
- VIDEO PULSE AMPLIFIER

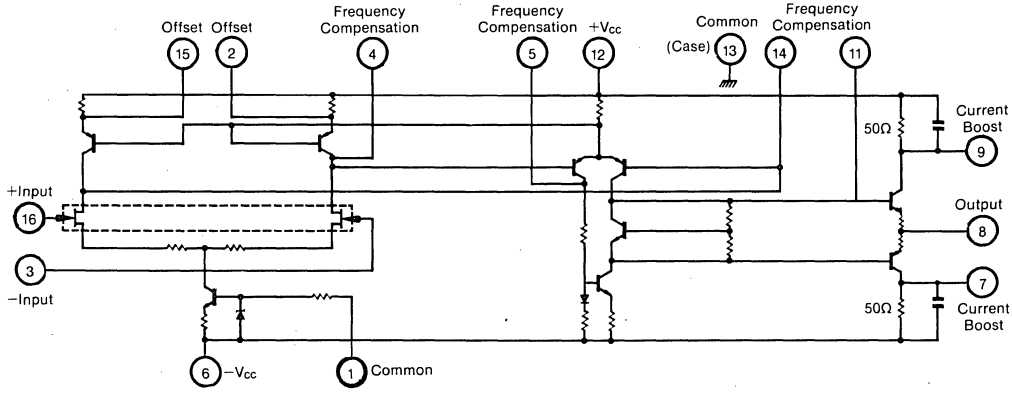
DESCRIPTION

The OPA600 is a wideband operational amplifier specifically designed for fast settling to ±0.01% accuracy. It is stable, easy to use, has good phase margin with minimum overshoot, and it has excellent DC performance. It utilizes an FET input stage to give low input bias current. Its DC stability over temperature is outstanding. The slew rate exceeds 400V/μs. All of this combines to form an outstanding amplifier for large and small signals.
form an outstanding amplifier for large and small signals.

High accuracy with fast settling time is achieved by using a high open-loop gain which provides the accuracy at high frequencies. The thermally balanced design maintains this accuracy without droop or thermal tail. External frequency compensation allows the user to optimize the settling time for various gains and load conditions.

The OPA600 is useful in a broad range of video, high speed test circuits and ECM applications. It is particularly well suited to operate as a voltage controlled oscillator (VCO) driver. It makes an excellent digital-to-analog converter output amplifier. It is a workhorse in test equipment where fast pulses, large signals, and 50Ω drive are important. It is a good choice for sample/holds, integrators, fast waveform generators, and multiplexers.

The OPA600 is specified over the industrial temperature range (OPA600BM, CM) and military temperature range (OPA600SM, TM). The OPA600 is housed in a welded, hermetic metal package.



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SPECIFICATIONS

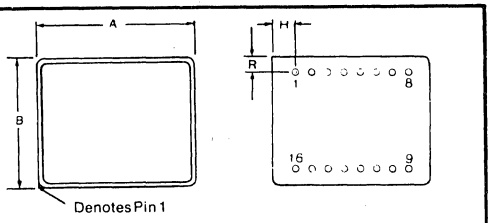
ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise specified.

		OPA600CM, TM[1]			OPA600BM, SM			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OUTPUT								
Voltage	R_L = 2kΩ	±10			*	*		V
	R_L = 50Ω[2]	±9			*	*		V
Current	R_L = 50Ω[2]	±180	±200		*	*		mA
Current Pulse	R_L = 50Ω[3]	±180	±200		*	*		mA
Resistance	Open loop DC		75			*	*	Ω
Short-Circuit Current	To COMMON only, t_{MAX} = 1s[4]		250	300		*	*	mA
DYNAMIC RESPONSE								
Settling Time[5]: to ±0.01% (±1mV)	ΔV_{OUT} = 10V		100	125		*	*	ns
to ±0.1% (±10mV)	ΔV_{OUT} = 10V		80	105		*	*	ns
to ±1% (±100mV)	ΔV_{OUT} = 10V		70	95		*	*	ns
Gain-Bandwidth Product (open-loop)	C_C = 0pF, G = 1V/V		150			*		MHz
	C_C = 0pF, G = 10V/V		500			*		MHz
	C_C = 0pF, G = 100V/V		1.5			*		GHz
	C_C = 0pF, G = 1000V/V		5			*		GHz
	C_C = 0pF, G = 10,000V/V		10			*		GHz
Bandwidth (−3dB small signal)[6]	G = +1V/V		125			*		MHz
	G = −1V/V		90			*		MHz
	G = −10V/V		95			*		MHz
	G = −100V/V		20			*		MHz
	G = −1000V/V		6			*		MHz
	Over Temperature		?			*		MHz
Full Power Bandwidth	V_{OUT} = ±5V, G = −1V/V, C_C = 3.3pF, R_L = 100Ω		16			*		MHz
Slew Rate	V_{OUT} = ±5V, G = −1000V/V, C_C = 0pF, R_L = 100Ω		500			*		V/μs
	V_{OUT} = ±5V, G = −1V/V[4]	400	440			*		V/μs
Phase Margin	G = −1V/V, C_C = 3.3pF		40			*		Degrees
GAIN								
Open-Loop Voltage Gain	f = DC, R_L = 2kΩ, T_A = +25°C	86	94		*	*		dB
INPUT								
Offset Voltage[7]	T_A = +25°C		±1	±4		±2	±5	mV
	T_A = −25°C to +85°C			±5			±10	mV
	T_A = −55°C to +125°C			±6			±15	mV
Offset Voltage Drift	T_A = −25°C to +85°C			±20			±80	μV/°C
	T_A = −55°C to +125°C			±20			±100	μV/°C
Bias Current	T_A = +25°C		−20	−100		*	*	pA
	T_A = +25°C to +125°C		−20	−100		*	*	nA
Offset Current	T_A = +25°C		20			*		pA
	T_A = +55°C to +125°C		20			*		nA
Power Supply Rejection Ratio	V_{CC} = ±15V, ±1V		200	500		*	*	μV/V
Common-Mode Voltage Range		−10		+7	*		*	V
Common-Mode Rejection Ratio	V_{CM} = −5V to +5V	60	80		*	*		dB
Impedance	Differential and Common-Mode		10^{11}‖2			*		Ω‖pF
Voltage Noise	10kHz Bandwidth		20			*		nV/√Hz
POWER SUPPLY								
Rated (V_{CC})			±15			*		VDC
Operating Range		±9		±16	*		*	VDC
Quiescent Current			±30	±38		*	*	mA
TEMPERATURE RANGE (Ambient)								
Operating: BM, CM		−25		+85	*		*	°C
SM, TM		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C
θ_{JC}, (junction to case)			30			*		°C/W
θ_{CA}, (case to ambient			35			*		°C/W

*Specification same as OPA600CM, TM.

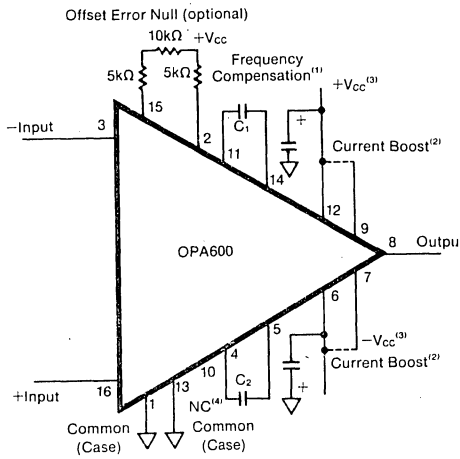
NOTES: (1) BM, CM grades: −25°C to +85°C. SM, TM grades: −55°C to +125°C. (2) Pin 9 connected to +V_{CC}, pin 7 connected to −V_{CC}. Observe power dissipation ratings. (3) Pin 9 and pin 7 open. Single pulse t = 100ns. Observe power dissipation ratings. (4) Pin 9 and pin 7 open. See section on Current Boost. (5) G = −1V/V. Optimum settling time and slew rate achieved by individually compensating each device. Refer to section on Compensation. (6) Frequency compensation as discussed in section on Compensation. (7) Adjustable to zero.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.963	.980	24.46	24.59
B	.760	.805	19.30	20.45
C	.175	.190	4.45	4.83
D	.014	.022	0.36	0.56
G	.100 BASIC		2.54 BASIC	
H	.135	.155	3.43	3.94
K	.230	.270	5.84	6.86
L	.600 BASIC		15.24 BASIC	
R	.096	.116	2.41	2.92

NOTES:
1. Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
2. Pin numbers shown for reference only.

CONNECTION DIAGRAM



NOTES: (1) Refer to Figure 4 for recommended frequency compensation. (2) Connect pin 9 to pin 12 and connect pin 7 to pin 6 for maximum output current. See Application Information for further information. (3) Bypass each power supply lead as close as possible to the amplifier pins. A 1μF CS13 tantalum capacitor is recommended. (4) There is no internal connection. An external connection may be made. (5) It is recommended that the amplifier be mounted with the case in contact with a ground plane for good thermal transfer and optimum AC performance.

ORDERING INFORMATION

Model	Temperature Range (°C)	Voltage Offset Drift (μV/°C)
OPA600BM	−25 to +85	±80
OPA600CM	−25 to +85	±20
OPA600SM	−55 to +125	±10
OPA600TM	−25 to +125	±20

ABSOLUTE MAXIMUM RATINGS(1)

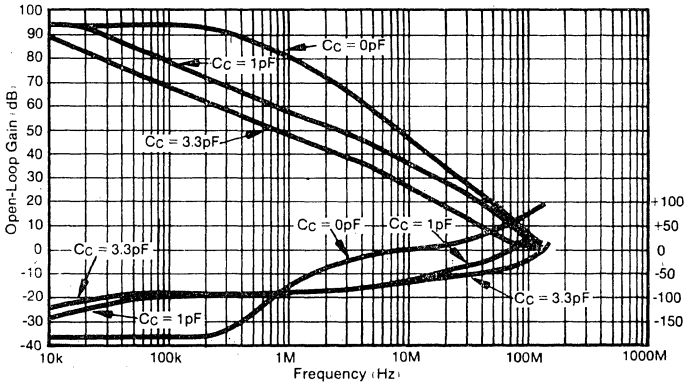
Supply Voltage, $+V_{CC}$ to $-V_{CC}$	±17
Power Dissipation, At T_{CASE} +125°C(2)	1.6W
Input Voltage: Differential	$\pm V_{CC}$
Common-Mode	$\pm V_{CC}$
Output Short Circuit Duration to Common	<5sec
Temperature: Pin (soldering, 20sec)	+300°C
Junction(1), T_J	+175°C
Temperature Range: Storage	−65°C to +150°C
Operating (case)	−55°C to +125°C

NOTES: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability. (2) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

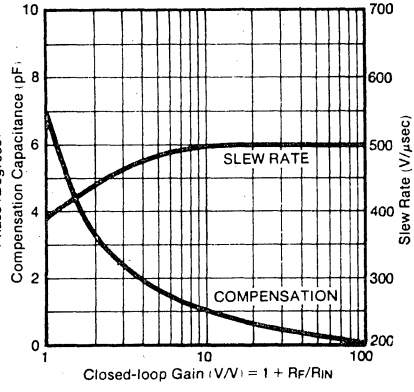
TYPICAL PERFORMANCE CURVES

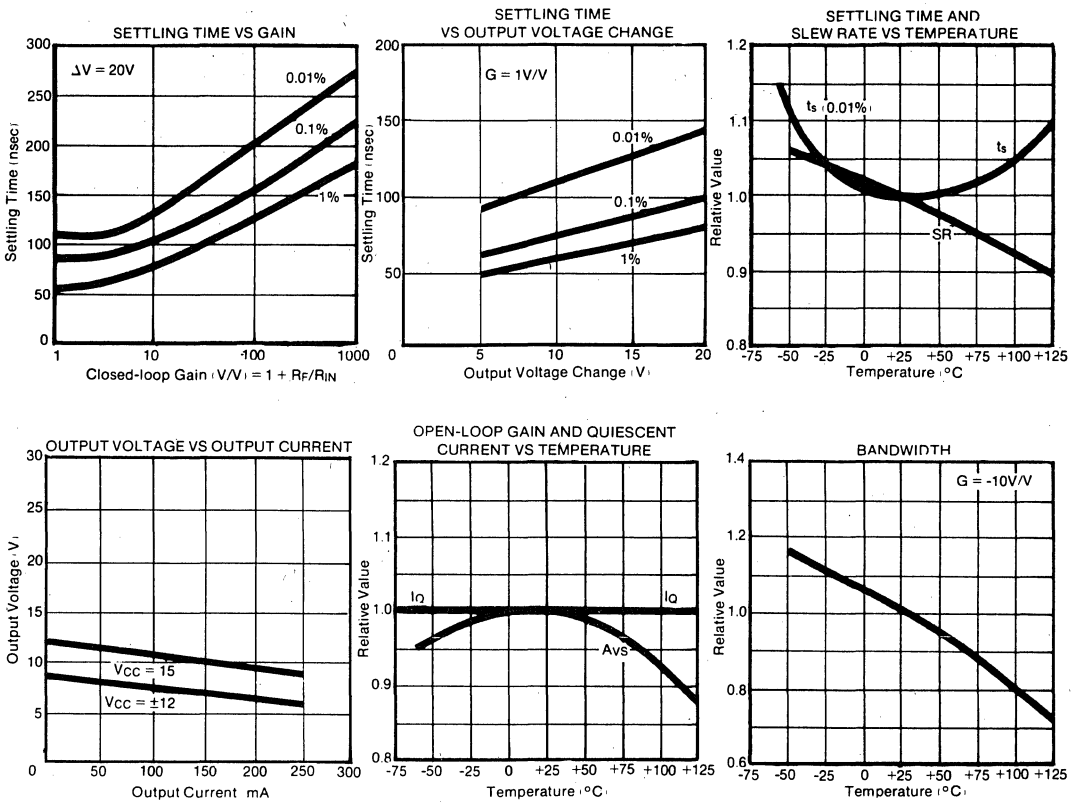
Typical at T_A = +25°C and $\pm V_{CC}$ = 15VDC, unless otherwise specified.

BODE PLOT



COMPENSATION AND SLEW RATE VS GAIN





INSTALLATION AND OPERATION

WIRING PRECAUTIONS

The OPA600 is a wideband, high frequency operational amplifier with a gain-bandwidth product exceeding 5GHz. This capability can be realized by observing a few wiring precautions and using high frequency layout techniques. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths and should be as short as possible. The entire physical circuit should be as small as is practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the input terminals of the amplifier and compensation pins. Stray signal coupling from the output to the input should be minimized. All circuit element leads should be as short as possible and low values of resistance should be used. This will give the best circuit performance as it will minimize the time constants formed with the circuit capacitances and will eliminate stray, unwanted tuned circuits.

Grounding is the most important application consideration for the OPA600, as it is with all high frequency circuits. Ultra-high frequency transistors are used in the design of the OPA600 and oscillations at frequencies of 500MHz and above can be stimulated if good grounding techniques are not used. A ground plane is highly recommended. It should connect all areas of the pattern side of the printed circuit that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pickup.

Point-to-point wiring is not recommended. However, if point-to-point wiring is used, a single-point ground should be used. The input signal return, the load signal return and the power supply common should all be connected at the same physical point. This eliminates common current paths or ground loops which can cause unwanted feedback.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A 1μF CS13 tantalum capacitor is recommended. A parallel 0.01μF ceramic may be added if desired. This is especially important when driving high current loads. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

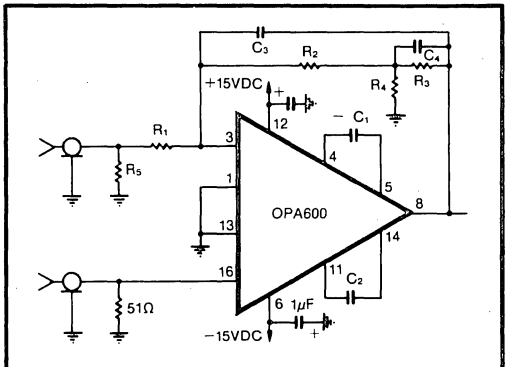
OPA600 circuit common is connected to pins 1 and 13; these pins should be connected to the ground plane. The input signal return, load return, and power supply commmon should also be connected to the ground plane.

The case of the OPA600 is internally connected to circuit common, and as indicated above, pins 1 and 13 should be connected to the ground plane. Ideally, the case should be mechanically connected to the ground plane for good thermal transfer, but because this is difficult in practice, the OPA600 should be fully inserted into the printed circuit board with the case very close to the ground plane to make the best possible thermal connection. If the case and ground plane are physically connected or are in close thermal proximity, the ground plane will provide heat sinking which will reduce the case temperature rise. The minimum OPA600 pin length will minimize lead inductance, thereby maximizing performance.

COMPENSATION

The OPA600 uses external frequency compensation so that the user may optimize the bandwidth or settling time for his particular application. Several performance curves aid in the selection of the correct compensations capacitance value. The Bode plot shows amplitude and phase versus frequency for several values of compensation. A related curve shows the recommended compensation capacitance versus closed-loop gain.

Figure 1 shows a recommended circuit schematic. Component values and compensation for amplifiers with several different closed-loop gains are shown. This circuit will yield the specified settling time. Because each device is unique and slightly different, as is each user's circuit, optimum settling time will be achieved by individually compensating each device in its own circuit, if desired. A 10% to 20% improvement in settling time has been experienced from the values indicated in the Electrical Specifications table.



Closed Loop Gain	R_1	R_2	R_3	R_4	C_1, C_2	C_3	C_4	R_5
+1	open	100	short	open	6.8	0	0	--
-1	620	620	short	open	3.3	4.7	0	56.
-10	100	1k	short	open	1	2.2	0	100
-100	100	3.3k	3.3k	3.2k	0	1	0	100
-1000	100	3.3k	3.3k	116	0	0	4.7	100

FIGURE 1. Recommended Amplifier Circuits and Frequency Compensation.

The primary compensation capacitors are C_1 and C_2 (see Figure 1). They are connected between pins 4 and 5 and between pins 11 and 14. Both C_1 and C_2 should be the same value. As Figure 1 and the performance curves show, larger closed-loop configurations require less capacitance and improved gain-bandwidth product can be realized. Note that no compensation capacitor is required for closed-loop gains equal to or above 100V/V. If upon initial application the user's circuit is unstable, and remains so after checking for proper bypassing, grounding, etc., it may be necessary to increase the compensation slightly to eliminate oscillations. Do not over compensate. It should not be necesary to increase C_1 and C_2 beyond 10pF to 15pF. It may also be necessary to individually optimize C_1 and C_2 for improved performance.

The flat high frequency response of the OPA600 is preserved and high frequency peaking is minimized by connecting a small capacitor in parallel with the feedback resistor (see Figure 1). This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. It will typically be 2pF for a clean layout using low resistances (1kΩ) and up to 10pF for circuits using larger resitances. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator is recommended to avoid using a large value resistor with its long time constant.

CAPACITIVE LOADS

The OPA600 will drive large capacitive loads (up to 100pF) when properly compensated and settling times of under 150ns are achievable. The effect of a capacitive load is to decrease the phase margin of the amplifier, which may cause high frequency peaking or oscillations. A solution is to increase the compensation capacitance, somewhat slowing the amplifier's ability to respond. The recommended compensation capacitance value as a function of load capacitance is shown in Figure 2. (Use two capcitors, each with the value indicated.) Alternately, without increasing the OPA600's compensation capacitance, the capacitive load may be buffered by connecting a small resistance, usually 5Ω to 50Ω, in series with the Output, pin 8.

For very-large capacitive loads, greater than 100pF, it will be necessary to use doublet compensation. Refer to Figure 3 and discussion on slew rate. This places the dominant pole at the input stage. Settling time will be approximately 50% slower; slew rate should increase. Load capacitance should be minimized for optimum high frequency performance.

Because of its large output capability, the OPA600 is particularly well suited for driving loads via coaxial

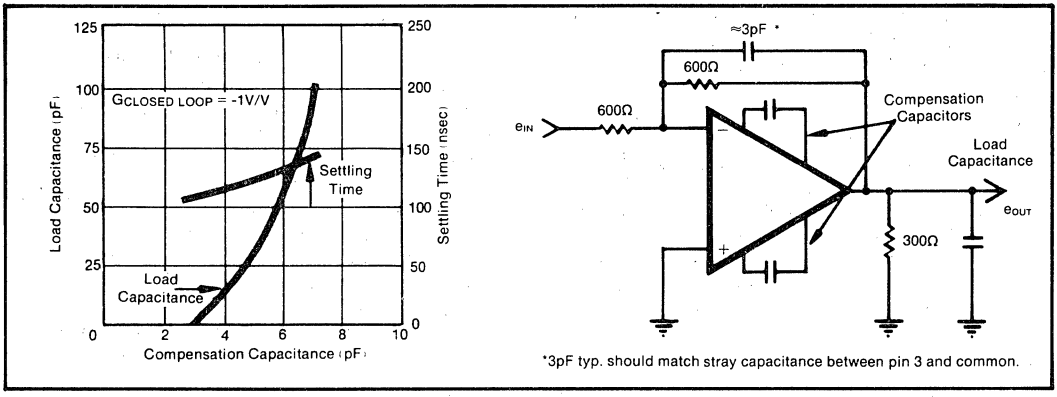


FIGURE 2. Capacitive Load Compensation and Response.

cables. Note that the capacitance of coaxial cable (29pF/foot of length for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition, a 10V step.

Settling time is a complete dynamic measure of the OPA600's total performance. It includes the slew rate time, a large signal dynamic parameter, and the time to accurately reach the final value, a small signal parameter that is a function of bandwidth and open-loop gain. Performance curves show the OPA600 settling time to ±1%, ±0.1%, and ±0.01%. The best settling time is achieved in low closed-loop gain circuits.

Settling time is dependent upon compensation. Under-compensation will result in small phase margin, overshoot or instability. Over-compensation will result in poor settling time.

Figure 1 shows the recommended compensation to yield the specified settling time. Improved or optimum settling time may be achieved by individually compensating each device in the user's circuit since individual devices vary slightly from one to another, as do user's circuits.

SLEW RATE

Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed-loop gain or small signal bandwidth. Slew rate is dependent upon compensation and decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve.

The OPA600 slew rate may be increased by using an alternate compensation as shown in Figure 3. The slew rate will increase between 700 and 800V/μs typical, with 0.01% settling time increasing to between 175 and 190ns typical, and 0.1% settling time increasing to between 110 and 120ns typical.

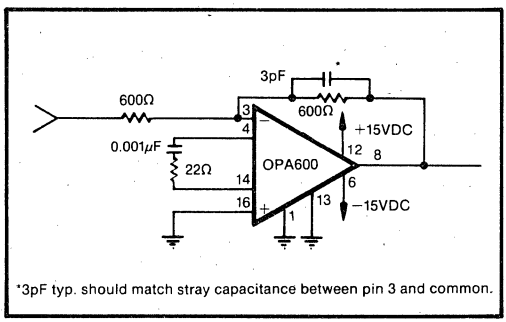


FIGURE 3. Amplifier Circuit for Increased Slew Rate.

For alternate doublet compensation refer to Figure 3. For a closed-loop gain equal to −1, delete C_1 and C_2 and add a series RC circuit (R = 22Ω, C = 0.01μF) between pins 14 and 4. Make no connections to pins 11 and 5. Absolutely minimze the capacitance to these pins. If a connector is used for the OPA600, it is recommended that sockets for pins 11 and 5 be removed. For a PC board mount, it is recommended that the PC board holes be overdrilled for pins 11 and 5 and adjacent ground plane copper be removed. Effectively this compensation places the dominant pole at the input stage, allowing the output stage to have no compensation and to slew as fast as possible. Bandwidth and settling time are impaired only slightly. For closed-loop gains other than −1, different values of R and C may be required.

OFFSET ADJUSTMENT

The offset voltage of the OPA600 may be adjusted to zero by connecting a 5kΩ resistor in series with a 10kΩ linear potentiometer in series with another 5kΩ resistor between pins 2 and 15, as shown in Figure 4. It is important that one end of each of the two resistors be located very close to pins 2 and 15 to isolate and avoid loading these sensitive terminals. The potentiometer should be a small noninductive type with the wiper connected to the positive supply. The leads connecting these components should be short, no longer than 0.5-inch, to avoid stray capacitance and stray signal pick-up. If the potentiometer must be located away from the immediate vicin-

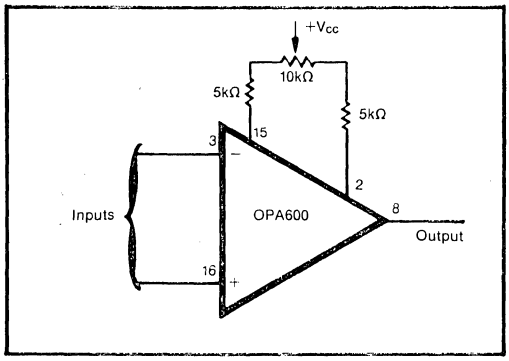


FIGURE 4. Offset Null Circuit.

ity of the OPA600, extreme care must be observed with the sensitive leads. Locate the two 5kΩ resistors very close to pins 2 and 15.

Never connect $+V_{CC}$ directly to pin 2 or 15. Do not attempt to eliminate the 5kΩ resistors because at extreme rotation, the potentiometer will directly connect $+V_{CC}$ to pin 2 or 15 and permanent damage will result.

Offset voltage adjustment is optional. The potentiometer and two resistors are omitted when the offset voltage is considered sufficiently low for the particular application. For each microvolt of offset voltage adjusted, the offset voltage temperature sensitivity will change by $\pm 0.004\mu V/°C$.

CURRENT BOOST

External ability to bypass the internal current limiting resistors has been provided in the OPA600. This is referred to as current boost. Current boost enables the OPA600 to deliver large currents into heavy loads (±200mA at ±10V). To bypass the resistors and activate the current boost, connect pin 7 to $-V_{CC}$ at pin 6 with a short lead to minimize lead inductance and connect pin 9 to $+V_{CC}$ at pin 12 with a short lead.

CAUTION—Activating current boost by bypassing the internal current limiting resistors can permanently damage the OPA600 under fault conditions. See section on short circuit protection.

Not activating current boost is especially useful for initial breadboarding. The 50Ω (±5%) current limiting resistor in the collector circuit of each of the output transistors causes the output transistors to saturate; this limits the power dissipation in the output stage in case of a fault. Operating with the current boost not activated may also be desirable with small-signal outputs (i.e., ±1V) or when the load current is small.

Each resistor is internally capacitively-bypassed (0.01μF, ±20%) to allow the amplifier to deliver large pulses of current, such as to charge diode junctions or circuit capacitance and still respond quickly. The length of time that the OPA600 can deliver these current pulses is limited by the RC time constant.

The internal voltage drops, output voltage available, power dissipation, and maximum output current can be determined for the user's application by knowing the load resistance and computing:

$$V_{OUT} = 14\,[R_{LOAD} \div (50 + R_{LOAD})]$$

This applies for R_{LOAD} less than 100Ω and the current boost not activated. When R_{LOAD} is large, the peak output voltage is typically ±11V, which is determined by other factors within the OPA600.

SHORT-CIRCUIT PROTECTION

The OPA600 is short-circuit-protected for momentary short to common (<5s), typical of those enountered when probing a circuit during experimental breadboarding or troubleshooting. This is true only if pins 7 and 9 are open (current boost not activated). An internal 50Ω resistor is in series with the collector of each of the output transistors, which under fault conditions will cause the output transistors to saturate and limit the power dissipation in the output stage. Extended application of an output short can damage the amplifier due to excessive power dissipation.

The OPA600 is not short-circuit-protected when the current boost is activated. The large output current capability of the OPA600 will cause excessive power dissipation and permanent damage will result even for momentary shorts to ground.

Output shorts to either supply will destroy the OPA600 whether the current boost is activated or not.

HEAT SINKING AND POWER DISSIPATION

The OPA600 is intended as a printed circuit board mounted device, and as such does not require a heat sink. It is specified for ambient temperature operation from −55°C to +125°C. However, the power dissipation must be kept within safe limits. At extreme temperature and under full load conditions, some form of heat sinking will be necessary. The use of a heat sink, or other heat dissipating means such as proximity to the ground plane, will result in cooler operating temperatures, better temperature performance, and improved reliability.

It may be necessary to physically connect the OPA600 to the printed circuit board ground plane, attach fins, tabs, etc., to dissipate the generated heat. Because of the wide variety of possibilities, this task is left to the user. For all applications it is recommended that the OPA600 be fully inserted into the printed circuit board and that the pin length be short. Heat will be dissipated through the ground plane and the AC performance will be its best.

With a maximum case temperature of +125°C and not exceeding the maximum junction of +175°C, a maximum power dissipation of 600mW is allowed in either output transistor.

TESTING

For static and low frequency dynamic measurements, the OPA600 may be tested in conventional operational amplifier test circuits, provided proper ground techniques are observed, excessive lead lengths are avoided, and care is maintained to avoid parasitic oscillations. The circuit in Figure 3 is recommended for low frequency functional testing, incoming inspection, etc. This circuit is less susceptible to stray capacitance, excessive lead length, parasitic tuned circuits, changing capacitive loads, etc. It does not yield optimum settling time. We recommend placing a resistor (approximately 300Ω) in series with each piece of test equipment, such as a DVM, to isolate loading effects on the OPA600.

To realize the full performance capabilities of the OPA600, high frequency techniques must be employed and the test fixture must not limit the amplifier. Settling time is the most critical dynamic test and Figure 5 shows a recommended OPA600 settling time test circuit schematic. Good grounding, truly square drive signals, minimum stray coupling, and small physical size are important.

The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. A circuit that generates a ±5V flat topped pulse is shown in Figure 6.

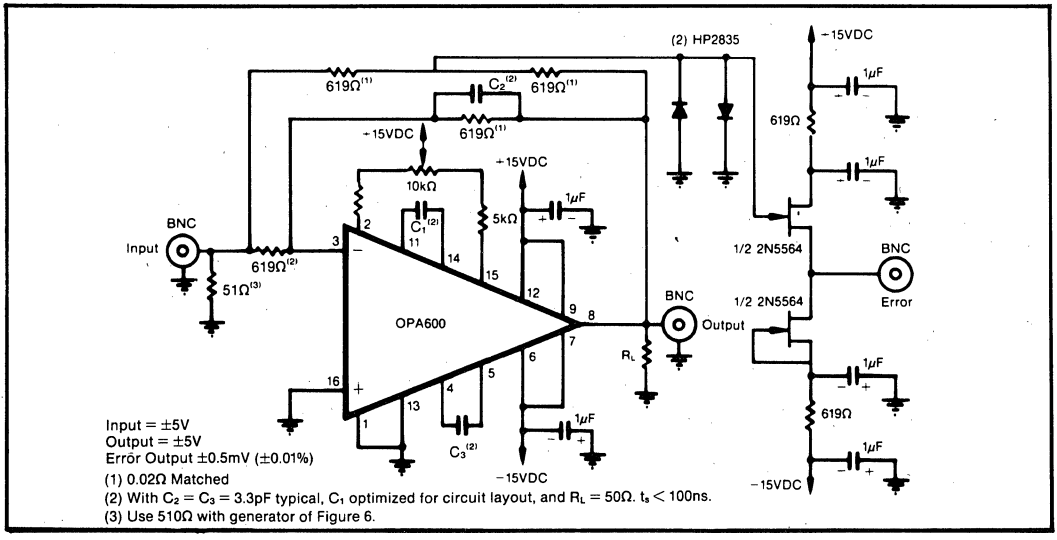


FIGURE 5. Settling Time and Slew Rate Test Circuit.

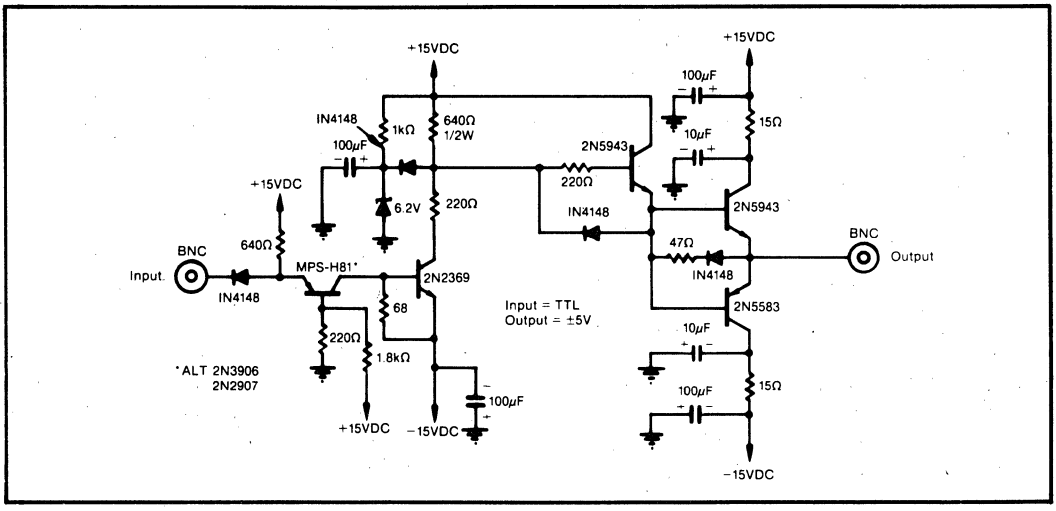


FIGURE 6. Flat Top Pulse Generator.

BURR-BROWN®

OPA605

Wideband - Fast Settling OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING - 500nsec max to 0.1%
- WIDE BANDWIDTH - 200MHz Gain - Bandwidth Product
- FAST SLEWING - 300V/μsec slew rate, $A_{CL} \geq 50$
- LARGE OUTPUT CURRENT - ±30mA min at ±10V
- HIGH GAIN - 80dB min at ±30mA output
- LOW VOLTAGE OFFSET AND DRIFT - 500μV max, 5μV/°C max

APPLICATIONS

- PULSE AMPLIFIERS
- FAST D/A CONVERTERS
- LINE DRIVERS
- WAVEFORM GENERATORS
- HIGH SPEED TEST EQUIPMENT

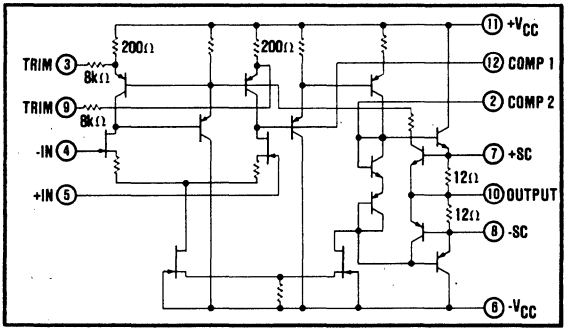
DESCRIPTION

The OPA605 is designed to offer a well balanced set of both AC and DC specifications. Versatility in fast settling, wideband and steady state AC applications is provided by the use of a single external compensation capacitor. This allows the user to optimize speed and stability for any particular application.

The full ±30mA guaranteed minimum output current (at ±10V) allows the user to realize the high speed features of the OPA605. Unlike most integrated circuit wideband amplifiers additional current booster circuitry is not needed for most applications.

The 500nsec max to 0.1% settling time specification is guaranteed with a load of 500Ω and 100pF. Also the open-loop gain is guaranteed at the full ±30mA output.

In addition to the excellent wideband and fast settling characteristics, the OPA605 also offers outstanding DC performance. Offset voltages are as low as 500μV max and offset voltage drift versus temperature of only 5μV °C max is available.



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SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL		OPA605GH/OPA605AM			OPA605KG/OPA605CM			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OPEN-LOOP GAIN, DC								
Full Load	V_O = ±10V; R_L = 330Ω	80	96		*	*		dB
No Load	V_O = ±10V; $R_L \geq$ 10kΩ		102			*		dB
RATED OUTPUT								
Voltage	I_O = ±30mA	±10	±12		*	*		V
Current	V_O = ±10V	±30	±50		*	*		mA
Output Resistance	Open Loop		200			*		Ω
Short Circuit Current	Internal Limits(1)	±30	±50	±80	*	*	*	mA
Capacitive Load(2)	A_{CL} = -1, C_C = 20pF	500			*			pF
DYNAMIC RESPONSE								
Gain-Bandwidth Product								
A_{CL} = 1000, C_C = 0			200			*		MHz
A_{CL} = -1, C_C = 20pF			20			*		MHz
Slew Rate	R_L = 330Ω, V_O = 0 to +10V,							
$A_{CL} \geq$ 50, C_C = 0	0 to -10V		300			*		V/μsec
A_{CL} = -1, C_C = 20pF		80	94		*	*		V/μsec
Full Power Bandwidth	R_L = 330Ω, V_O = ±10V,	1.3	1.5		*	*		MHz
	A_{CL} = -1, C_C = 20pF							
Settling Time, A_V = -1(3)	C_C = 20pF, R_L = 500Ω,							
	C_L = 100pF, V_O = 0 to +10V,							
	0 to -10V							
ε = 1%			200			*		nsec
ε = 0.1%			300	500		*	*	nsec
ε = 0.01%			400			*		nsec
Small-Signal Overshoot	A_V = -1, C_C = 20pF, R_L = 500Ω		0	20		*	*	%
	C_L = 100pF							
INPUT OFFSET VOLTAGE								
Initial Offset	T_A = +25°C		±0.25	±1.0		*	±0.5	mV
vs Temperature	T_L to T_H, V_{CM} = 0			±25			±5	μV/°C
vs Supply Voltage			±30	±200		*	*	μV/V
Adjustment Range(4)	Circuit in		±9			*		mV
	"Connection Diagram"							
INPUT BIAS CURRENT								
Initial Bias	T_A = +25°C, V_{CM} = 0		-10	-35		*	*	pA
vs Temperature	T_L to T_H		Note 5			*		
vs Supply Voltage			0.2			*		pA/V
vs V_{CM}			Note 6			*		
INPUT DIFFERRENCE CURRENT								
Initial Difference	T_A = +25°C, V_{CM} = 0		±2			*		pA
vs Temperature			Note 5			*		
vs Supply Voltage			0.05			*		pA/V
VOLTAGE NOISE DENSITY $R_S \leq$ 100Ω								
	f_O = 10Hz		80			*		nV/√Hz
	f_O = 100Hz		30			*		nV/√Hz
	f_O = 1kHz		20			*		nV/√Hz
	f_O = 10kHz		12			*		nV/√Hz
	f_O = 100kHz		12			*		nV√Hz
INPUT IMPEDANCE								
Differential								
Resistance			10^{11}			*		Ω
Capacitance			3			*		pF
Common-Mode								
Resistance			10^{11}			*		Ω
Capacitance			3			*		pF
INPUT VOLTAGE RANGE								
Common-Mode Voltage	Linear Operation							
Range		±10	±12		*	*		V
Common-Mode Rejection		70	90		80	90		dB
POWER SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range	Derated Performance	±5		±18	*		*	VDC
Current, Quiescent			±7.2	±9		*	*	mA
TEMPERATURE RANGE								
Specification								
GH, KG Grades	T_L to T_H	0		+70	*		*	°C
AM, CM Grades	T_L to T_H	-25		+85	*		*	°C
Operating	Derated Performance	-55		+125	*		*	°C
Storage		-65		+150	*		*	°C

NOTES: *Specifications same as for OPA605H/OPA605A. (1) Current limit may be increased with external resistors. (2) Allowable capacitive load depends on several factors. See Compensation section. (3) Settling Time measured in circuit of Figure 4. (4) Adjustment affects voltage drift vs temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted. (5) Doubles approximately every 8.5°C. (6) See Typical Performance Curves.

ABSOLUTE MAXIMUM RATINGS

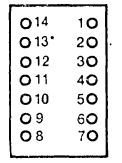
Supply	±20VDC
Internal Power Dissipation	(1)
Differential Input Voltage(2)	±20VDC
Input Voltage, Either Input(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration(3)	Continuous
Junction Temperature	+175°C

NOTES:
1. Package must be derated according to details in the Applications Information section.
2. For supply voltages less than ±20VDC, the absolute maximum input is equal to the supply voltage.
3. Short circuit to ground only. See Short Circuit Protection discussion in the Application Information section.

PIN CONFIGURATION

1. No Internal Connection.
2. Optional Frequency Compensation.
3. Offset Adjust.
4. Inverting Input.
5. Noninverting Input.
6. -Vcc.
7. Optional Short Circuit Adjust.
8. Optional Short Circuit Adjust.
9. Offset Adjust.
10. Output
11. +Vcc.
12. Frequency Compensation.
13. No Internal Connection*.
14. No Internal Connection.

*Case on metal package

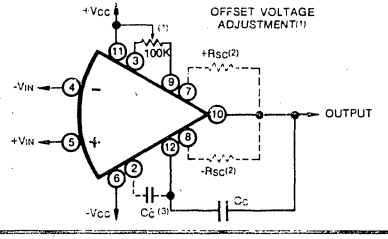


Bottom View

Pin numbers shown for reference only. Numbers are not marked on package.

Pin 13 is case on metal unit.

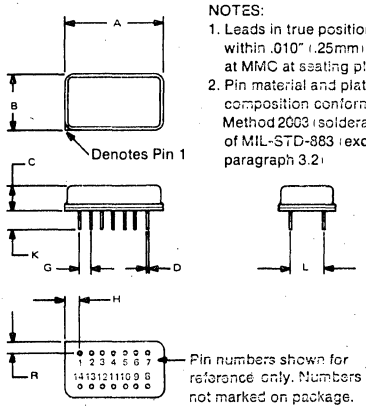
CONNECTION DIAGRAM



NOTES:
1. Offset voltage adjustment affects voltage drift vs temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted.
2. Optional resistors to increase current limits. See Application Information.
3. Optional frequency compensation. See Applications Information.

MECHANICAL

METAL PACKAGE—"M"

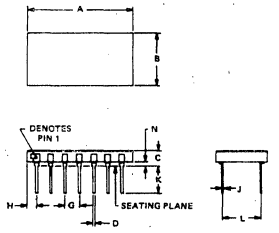


NOTES:
1. Leads in true position within .010" (.25mm) R at MMC at seating plane.
2. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

Pin numbers shown for reference only. Numbers are not marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

CERAMIC PACKAGE—"G"



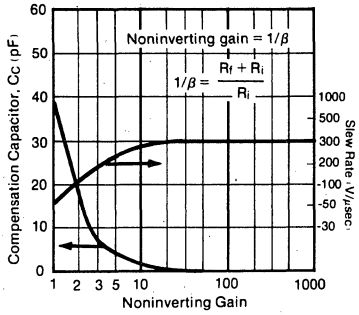
NOTES:
1. Leads in true position within .010" (.25mm) R at MMC at seating plane
2. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.770	.810	19.56	20.57
B	.480	.500	12.19	12.70
C	.155	.215	3.94	5.46
D	.016	.020	.41	.51
G	.100 BASIC		2.54 BASIC	
H	.080	.110	2.03	2.79
J	.009	.012	.23	.30
K	.150	.210	3.81	5.33
L	.300 BASIC		7.62 BASIC	
N	.015	.035	.38	.89

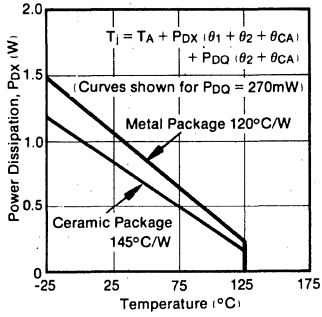
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted)

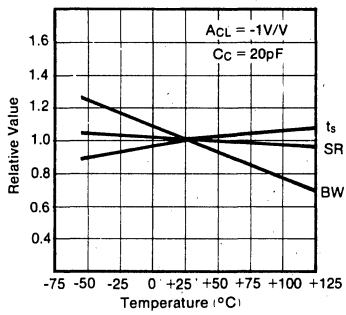
COMPENSATION CAPACITANCE AND SLEW RATE VS NONINVERTING GAIN



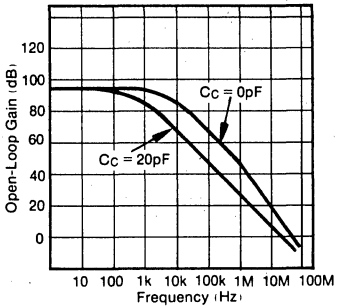
POWER DERATING



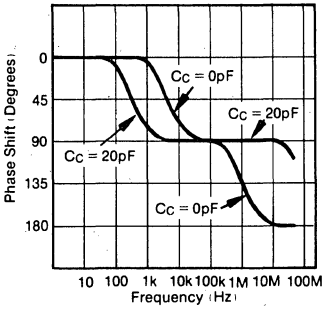
AC PARAMETERS VS TEMPERATURE



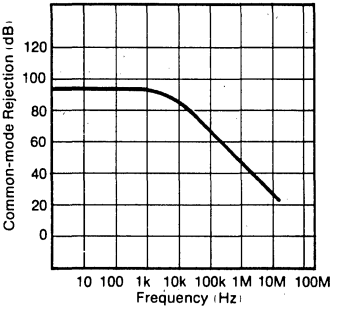
OPEN-LOOP GAIN VS FREQUENCY



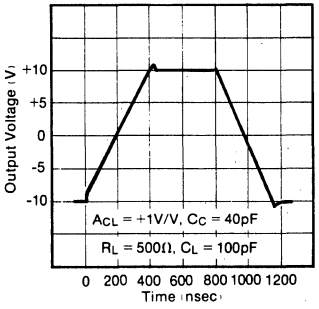
OPEN-LOOP PHASE SHIFT VS FREQUENCY



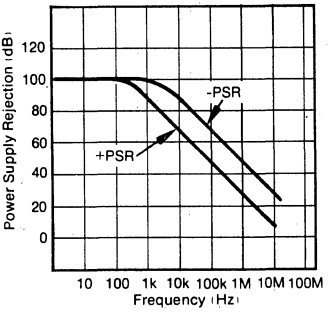
COMMON-MODE REJECTION VS FREQUENCY



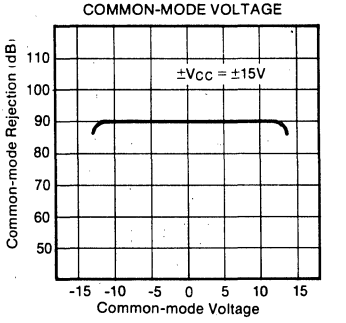
LARGE SIGNAL TRANSIENT RESPONSE



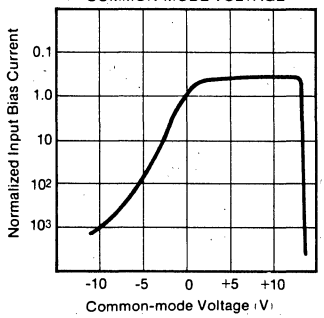
POWER SUPPLY REJECTION VS FREQUENCY



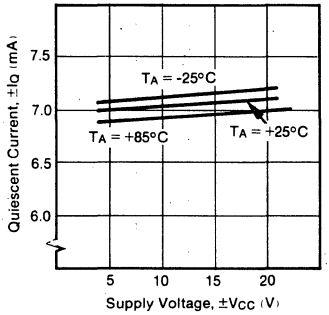
COMMON-MODE REJECTION VS COMMON-MODE VOLTAGE



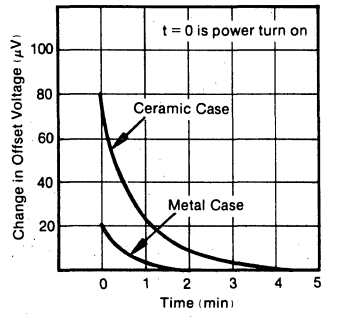
BIAS CURRENT VS COMMON-MODE VOLTAGE



QUIESCENT CURRENT VS SUPPLY VOLTAGE



OFFSET VOLTAGE VS TIME



APPLICATION INFORMATION

SLEW RATE

Slew rate is a large signal output parameter. It is primarily dependent on the compensation capacitor value (C_C) and has almost no dependence on changes in the closed loop gain or bandwidth. Typical values of slew rate versus compensation capacitor value are shown in the Typical Performance Curves. Decreasing the compensation capacitance increases the slew rate but reduces the frequency stability of the closed-loop circuit. Stray circuit capacitances may appear as added compensation to the amplifier. Therefore, stray capacitances should be minimized to avoid limiting slew rate performance.

BANDWIDTH

The closed-loop bandwidth is a small signal parameter. It is dependent on the open-loop frequency response of the op amp (which is determined by the value of the compensation capacitor, C_C) and the external closed-loop circuitry applied to the amplifier. Requirements for increased bandwidth and more frequency stability result in opposing constraints on the circuitry and generally the final selection of circuit values represents a compromise between the two needs.

SETTLING TIME

Settling time is defined as the total time required, measured from the input signal step, for the output to settle to within the specified error band around the final value. The error band is expressed as a percent of the full scale output voltage (10V) and the output transition is from 0V to +10V or 0V to -10V.

Settling time depends on slew rate (discussed above) and the time to reach the final value after the slew portion of the transition is complete. The latter is a function of the closed-loop bandwidth (discussed above) and the closed-loop gain. Thus, settling time is a function of both the open-loop frequency compensation (value of C_C) and the particular closed-loop circuit configuration. The best settling time is generally obtained at low gains.

COMPENSATION

The OPA605 uses external frequency compensation which allows the user to optimize slew rate, bandwidth and settling time for a particular application. As mentioned previously, compensation is normally a compromise between the desired speed and the necessary frequency stability - the higher the speed the lower the value of C_C and the less stable the circuit. Several of the Typical Performance Curves provide information to aid in the selection of the correct value of compensation capacitor. In addition, several typical circuits show recommended compensation in different applications.

The value of compensation capacitor required for stability is a function of the amount of negative feedback used in the particular application.

This is characterized as $1/\beta$, where β is the "feedback factor". $1/\beta$ is also equal to the gain in noninverting configurations (see figures 2 and 3).

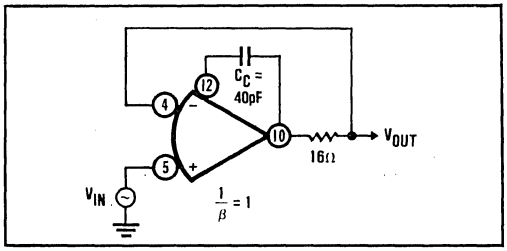


FIGURE 1. Unity Gain Follower.

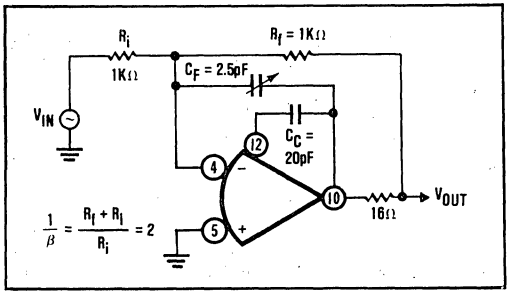


FIGURE 2. Unity Gain Inverting.

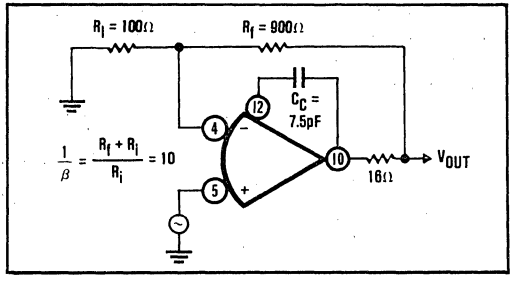


FIGURE 3. Gain of +10V.

The OPA605 may be compensated in either one of two ways. In the primary compensation method, C_C is connected between pins 10 and 12. Alternately the amplifier may be compensated with C_C' between pins 12 and 2 (see Connection Diagram). Normally the use of C_C is recommended. The use of C_C' will give lower output impedance at higher frequencies. This can be an advantage in some applications, but the effects are subtle and must be determined empirically.

Improved stability with larger capacitive loads may be obtained by connecting a small resistor (a value of 16Ω is recommended) in series with the output (see figures 2 through 4).

Flat high frequency closed-loop frequency response may be preserved and any high frequency peaking reduced by connecting a small capacitor (C_f in the examples) in parallel with the feedback resistor. This capacitor will compensate for the high frequency closed-loop transfer function zero formed by the capacitance at the amplifier's input and the input and feedback resistors. C_f may be a trimmer capacitor, a fixed capacitor or a planned printed circuit board capacitance. Typical values range from 0pF to 5pF.

WIRING PRECAUTIONS

Of all the wiring precautions, grounding is the most important. A good ground plane and good grounding practices should be used. The ground plane should connect all areas of the pattern side of the printed circuit board that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns.

If point-to-point wiring is used (no ground plane), single point grounding should be used. The input signal return, the load signal return and the power supply common should all be connected at the same physical point. This will eliminate any common current paths or ground loops which could cause signal modulation or unwanted feedback.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins.

All printed circuit board conductors should be wide to provide low resistance, low inductance connections, and should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitance should be minimized especially at high impedance nodes. Pin 4, the inverting input is especially sensitive to capacitance and all connections to that point must be short.

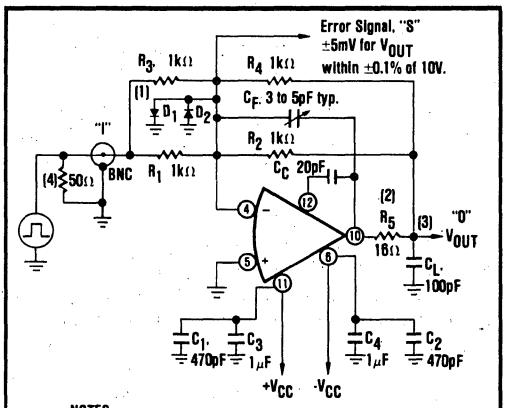


FIGURE 4. Dynamic Test Circuit.

Input and feedback resistors should be kept as small in value as practical; values less than 5.6kΩ are recommended. This will minimize performance limitations caused by the time constants formed by these resistors and circuit capacitances.

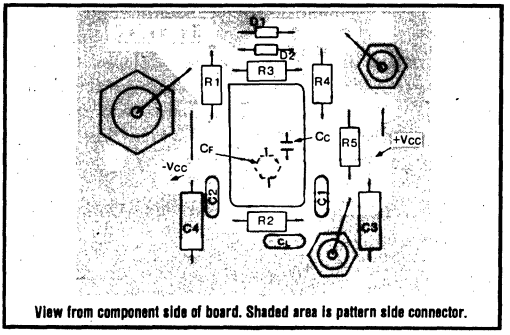


FIGURE 5. Dynamic Test Circuit Layout.

SHORT CIRCUIT PROTECTION

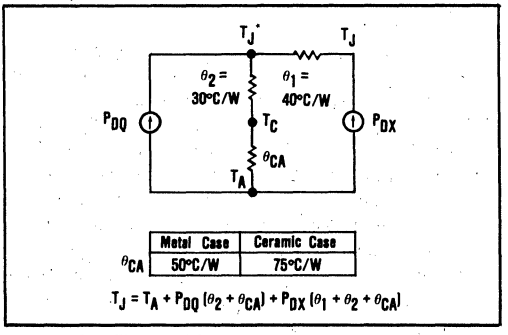
Short circuit protection to common is provided by internal current limiting resistors. (Output shorts to either supply can destroy the device.) The current limits may be increased by paralleling the internal resistors with external resistors, R_{EXT} connected between pins 7 and 10 and pins 8 and 10. The short-circuit current is then $I_{SC} \approx 0.05 + 0.6/R_{EXT}$ (in amps). The power derating constraints must be observed when modifying the current limits. Details are given by the thermal model.

THERMAL MODEL

Figure 6 is the thermal model for the OPA605 where:

T_J = Junction temperature (output load)
T_J* = Junction temperature (no load)
T_C = Case temperature
T_A = Ambient temperature
θ_{CA} = Thermal resistance, case-to-ambient
P_{DQ} = Quiescent power dissipation
$|+V_{CC}|I_{QUIESCENT}| + |-V_{CC}|I_{QUIESCENT}|$
P_{DX} = Power dissipation in the output transistor
$= (V_{OUT} - V_{CC})\, I_{OUT}$

(In a complementary output stage only one output transistor is conducting current at a time.)



	Metal Case	Ceramic Case
θ_{CA}	50°C/W	75°C/W

$T_J = T_A + P_{DQ}(\theta_2 + \theta_{CA}) + P_{DX}(\theta_1 + \theta_2 + \theta_{CA})$

FIGURE 6. Thermal Model.

This model yields a Power Derating curve which is a function of P_{DQ}. See Typical Performance Curves.

BURR-BROWN®

OPA606

Wide-Bandwidth *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH, 13MHz typ
- HIGH SLEW RATE, 35V/μsec typ
- LOW BIAS CURRENT, 10pA max at $T_A = +25°C$
- LOW OFFSET VOLTAGE, 500μV max
- LOW DISTORTION, 0.0035% typ at 10kHz

APPLICATIONS

- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- AUDIO AMPLIFIERS

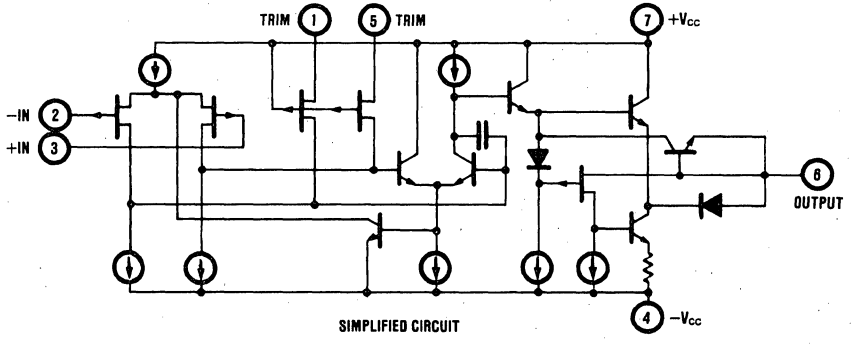
DESCRIPTION

The OPA606 is a wide-bandwidth monolithic dielectrically-isolated FET (*Difet*®) operational amplifier featuring a wider bandwidth and lower bias current than BIFET® LF156A amplifiers. Bias current is specified under warmed-up and operating conditions, not at a JUNCTION temperature of +25°C.

Laser-trimmed thin-film resistors offer improved offset voltage and noise performance.

The OPA606 is internally compensated for unity-gain stability.

Difet® Burr-Brown Corp., Bifet® National Semiconductor Corp.



SIMPLIFIED CIRCUIT

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = + 25°C unless otherwise specified.

PARAMETER	CONDITIONS	OPA606KM/SM			OPA606LM			OPA606KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE											
Gain Bandwidth	Small signal	10	12.5		11	13		9	12		MHz
Full Power Response	20V p-p, R_L = 2kΩ		515			550			470		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	22	33		25	35		20	30		V/µsec
Settling Time[1]: 0.1%	Gain = −1, R_L = 2kΩ		1.0			1.0			1.0		µsec
0.01%	10V step		2.1			2.1			2.1		µsec
Total Harmonic Distortion	G = +1, 20V p-p R_L = 2kΩ, f = 10kHz		0.0035			0.0035			0.0035		%
INPUT											
OFFSET VOLTAGE[2]											
Input Offset Voltage	V_{CM} = 0VDC		±180	±1.5mV		±100	±500		±300	±3mV	µV
Average Drift	T_A = T_{MIN} to T_{MAX}		±5			±3	±5		±10		µV/°C
Supply Rejection	V_{cc} = ±10V to ±18V	82	100		90	104		80	90		dB
			±10	±79		±6	±32		±32	±100	µV/V
BIAS CURRENT[2]											
Input Bias Current	V_{CM} = 0VDC		±7	±15		±5	±10		±8	±25	pA
OFFSET CURRENT[2]											
Input Offset Current	V_{CM} = 0VDC		±0.6	±10		±0.4	±5		±1	±15	pA
NOISE											
Voltage, f_O = 10Hz	100% tested (L)		37			30	40		37		$nV/\sqrt{Hz}$
100Hz	100% tested (L)		21			20	28		21		$nV/\sqrt{Hz}$
1kHz	100% tested (L)		14			13	16		14		$nV/\sqrt{Hz}$
10kHz	[3]		12			11	13		12		$nV/\sqrt{Hz}$
20kHz	[3]		11			10.5	13		11		$nV/\sqrt{Hz}$
f_B = 10Hz to 10kHz	[3]		1.3			1.2	1.5		1.3		µV rms
Current, f_O = 0.1Hz thru 20kHz	[3]		1.5			1.3	2		1.7		$fA/\sqrt{Hz}$
IMPEDANCE											
Differential			10^{13} ‖ 1			10^{13} ‖ 1			10^{13} ‖ 1		Ω ‖ pF
Common-Mode			10^{14} ‖ 3			10^{14} ‖ 3			10^{14} ‖ 3		Ω ‖ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10.5	±11.5		±11	±11.6		±10.2	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	80	95		85	96		78	90		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	95	115		100	118		90	110		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11	±12.2		±12	±12.6		±11	±12		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, open loop		40			40			40		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	20		10	20		10	20		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		6.5	9.5		6.2	9		6.5	10	mA
TEMPERATURE RANGE											
Specification	Ambient temp.										
	KM, KP, LM	0		+70	0		+70	0		+70	°C
	SM	−55		+125							°C
Operating	Ambient Temp.	−55		+125	−55		+125	−25		+85	°C
θ Junction-Ambient			200			200			155		°C/W

NOTES: (1) See settling time test circuit in Figure 2. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Sample tested—this parameter is guaranteed on L grade only.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA606KM/SM MIN	OPA606KM/SM TYP	OPA606KM/SM MAX	OPA606LM MIN	OPA606LM TYP	OPA606LM MAX	OPA606KP MIN	OPA606KP TYP	OPA606KP MAX	UNITS
TEMPERATURE RANGE											
Specification Range	Ambient temp. KM	0		+70	0		+70	0		+70	°C
	SM	−55		+125							°C
INPUT											
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC KM		±400	±2mV		±335	±750		±750	±3.5mV	µV
	SM		±680	±3mV							µV
Average Drift			±5			±3	±5		±10		µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	80	98		85	100		78	95		dB
			±13	±100		±10	±56		±18	±126	µV/V
BIAS CURRENT[1]											
Input Bias Current	V_{CM} = 0VDC KM		±158	±339		±113	±226		±181	±566	pA
	SM		±7.2	±15.4							nA
OFFSET CURRENT[1]											
Input Offset Current	V_{CM} = 0VDC KM		±14	±226		±9	±113		±23	±339	pA
	SM		±614	±10.2nA							pA
VOLTAGE RANGE											
Common-Mode Input Range		±10.4	±11.4		±10.9	±11.5		±10	±10.9		V
Common-Mode Rejection	V_{IN} = ±10VDC	78	92		82	95		75	88		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	90	106		95	112		88	104		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±10.5	±12		±11.5	±12.4		±10.4	±11.8		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		6.6	10		6.4	9.5		6.6	10.5	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ORDERING INFORMATION

OPA606 X X

Basic model number

Performance grade
- K, L = 0°C to +70°C
- S = −55°C to +125°C

Package code
- M = TO-99 metal can
- P = 8-pin plastic DIP (K grade only)

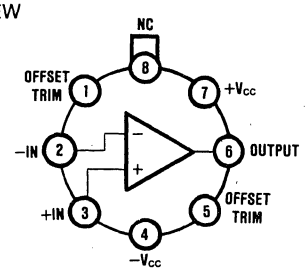
ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	M = −65°C to +150°C, P = −40°C to +85°C
Operating Temperature Range	M = −55°C to +125°C, P = −40°C to +85°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on θ_{JC} = 15°C/W or θ_{JA}. (2) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to the negative supply voltage. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

CONNECTION DIAGRAMS

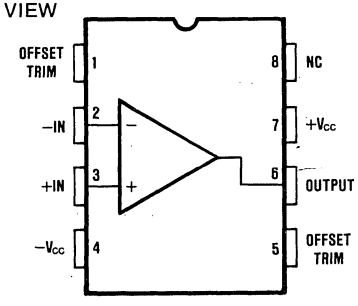
TOP VIEW — TO-99



CASE IS CONNECTED TO V_{CC}

MECHANICAL

TOP VIEW — DIP



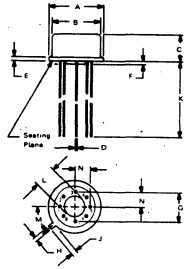
MECHANICAL

"M" PACKAGE — TO-99 (Hermetic)

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	-	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

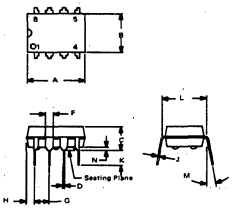
MECHANICAL

"P" PACKAGE — Plastic DIP

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

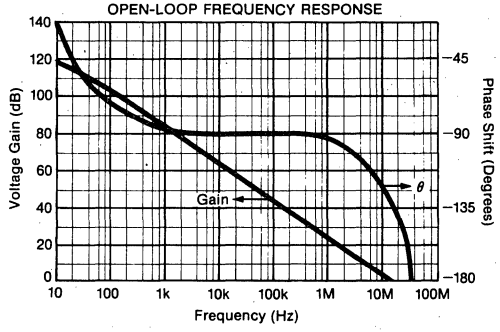


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.370	.400	9.40	10.16
B	.230	.290	5.84	7.37
C	.120	.200	3.05	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.060	0.76	1.27
J	.008	.015	0.20	0.38
K	.070	.135	1.78	3.43
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.010	.030	0.25	0.76

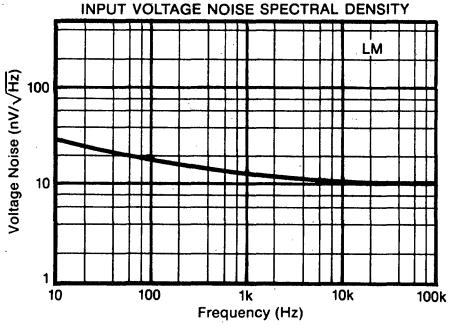
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_{CC} = \pm 15VDC$ unless otherwise noted.

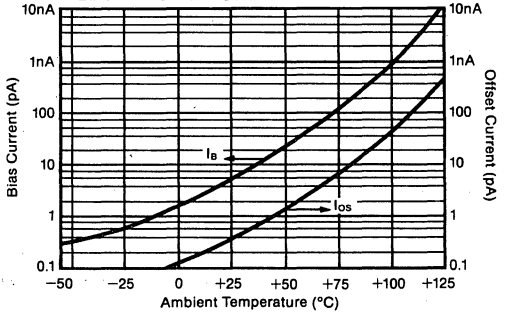
OPEN-LOOP FREQUENCY RESPONSE



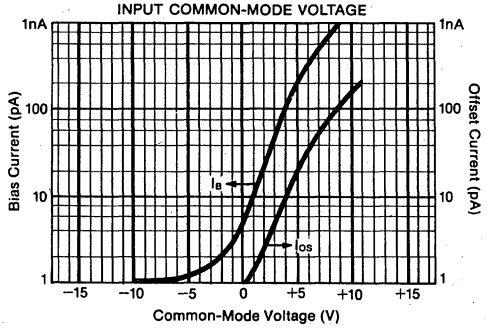
INPUT VOLTAGE NOISE SPECTRAL DENSITY



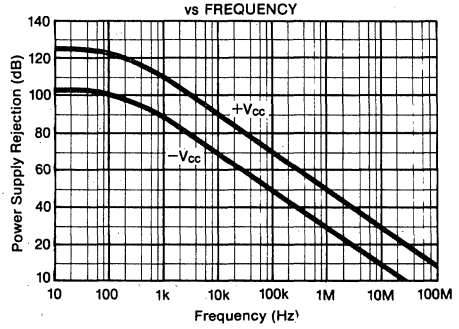
BIAS AND OFFSET CURRENT vs TEMPERATURE



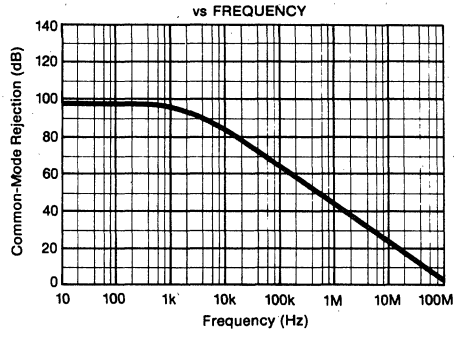
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



POWER SUPPLY REJECTION vs FREQUENCY



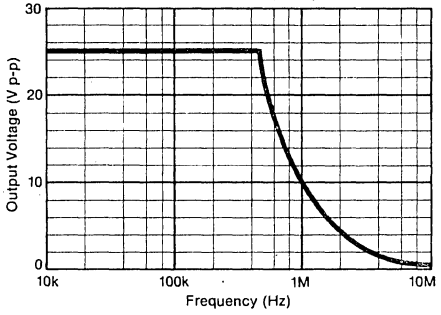
COMMON-MODE REJECTION vs FREQUENCY



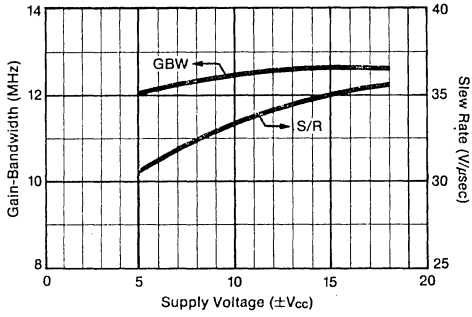
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

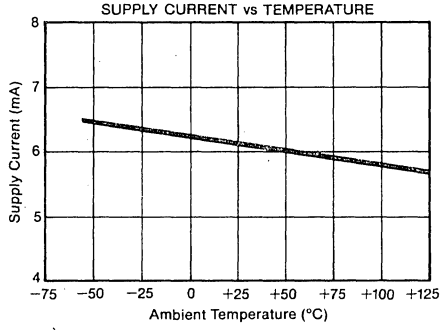
MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY



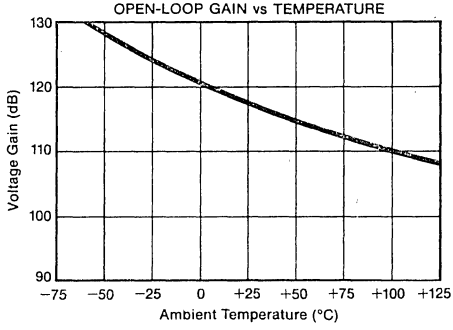
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



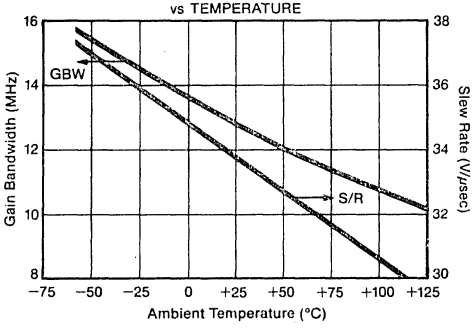
SUPPLY CURRENT vs TEMPERATURE



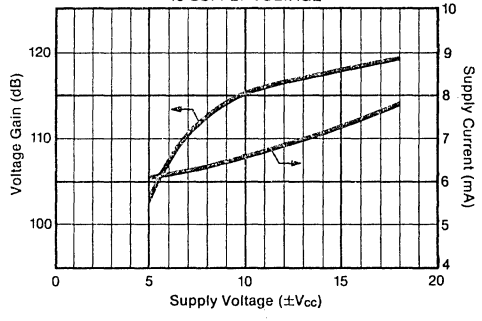
OPEN-LOOP GAIN vs TEMPERATURE



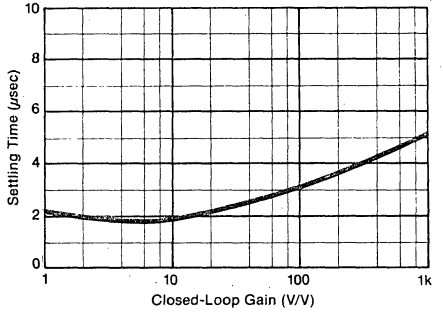
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



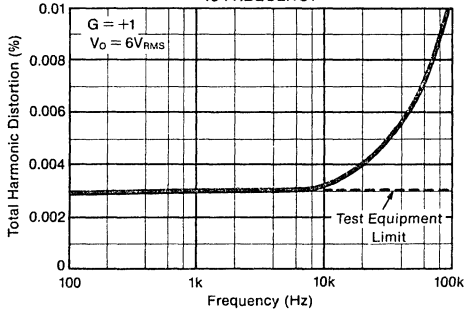
OPEN-LOOP GAIN AND SUPPLY CURRENT vs SUPPLY VOLTAGE



SETTLING TIME vs CLOSED-LOOP GAIN



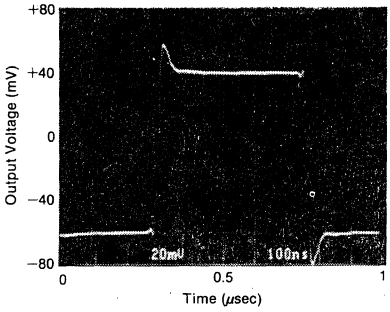
TOTAL HARMONIC DISTORTION vs FREQUENCY



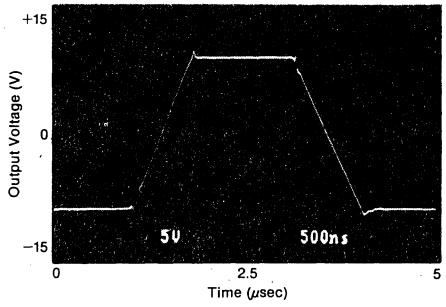
TYPICAL PERFORMANCE CURVES (CONT)

T_a = +25°C, V_{CC} = ±15VDC unless otherwise noted.

SMALL SIGNAL TRANSIENT RESPONSE



LARGE SIGNAL TRANSIENT RESPONSE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA606 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.5μV/°C for each millivolt of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as LF156 and OP-16. The OPA606 can replace most other amplifiers by leaving the external null circuit unconnected.

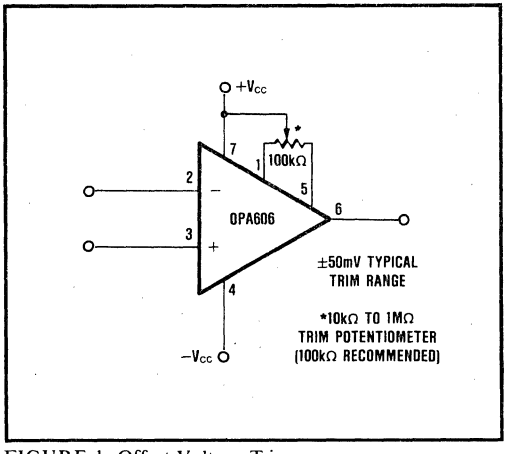


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

If the input voltage exceeds the amplifier's negative supply voltage, input current limiting must be used to prevent damage.

CIRCUIT LAYOUT

Wideband amplifiers require good circuit layout techniques and adequate power supply bypassing. Short, direct connections and good high frequency bypass capacitors (ceramic or tantalum) will help avoid noise pickup or oscillation.

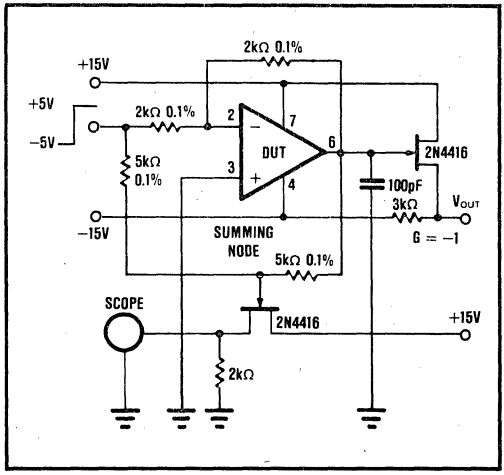


FIGURE 2. Settling Time Test Circuit.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA606. To avoid leakage problems, it is recommended that the signal input lead of the OPA606 be wired to a Teflon® standoff. If the OPA606 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout.

A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 3).

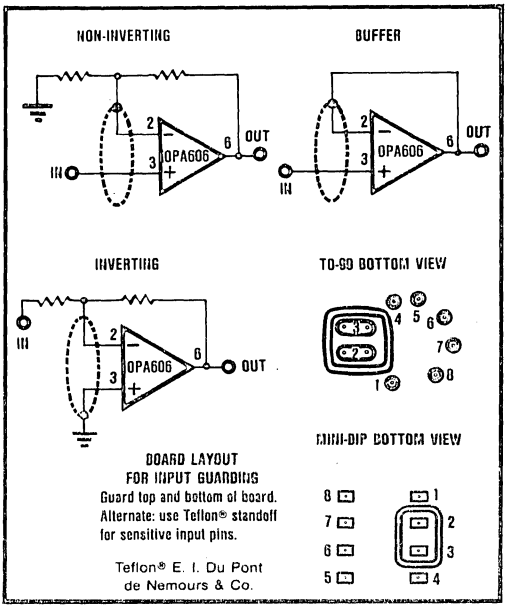


FIGURE 3. Connection of Input Guard.

APPLICATIONS CIRCUITS

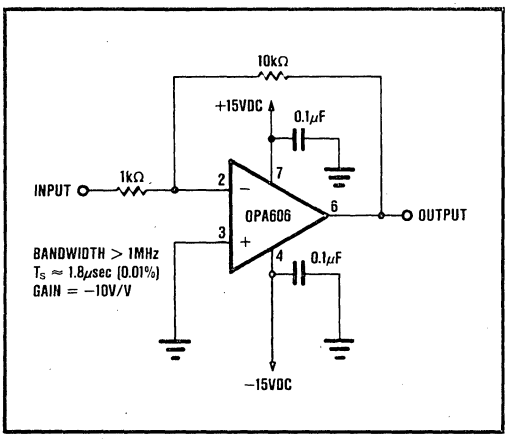


FIGURE 4. Inverting Amplifier.

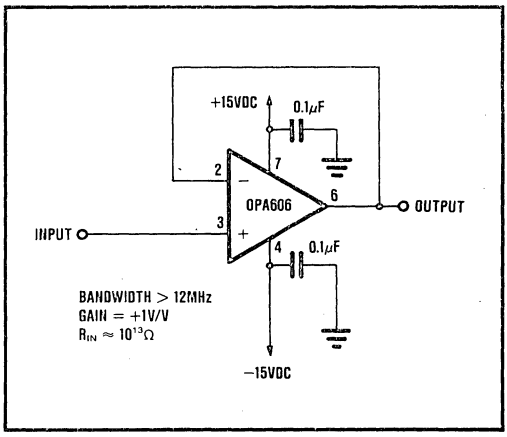


FIGURE 5. Noninverting Buffer.

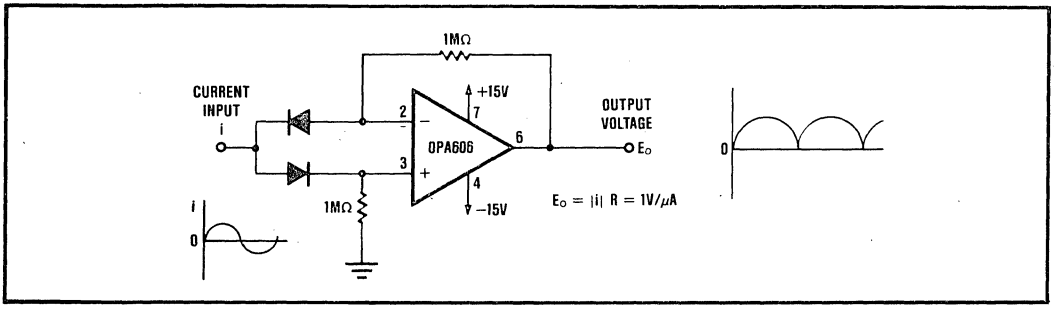


FIGURE 6. Absolute Value Current-to-Voltage Converter.

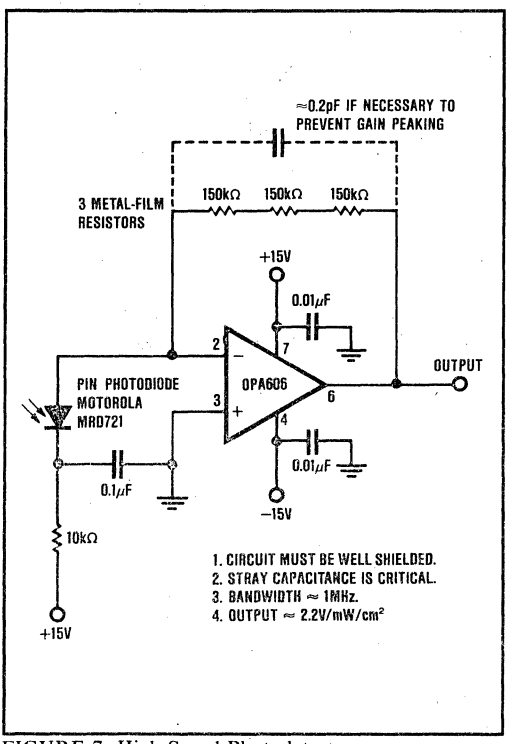


FIGURE 7. High-Speed Photodetector.

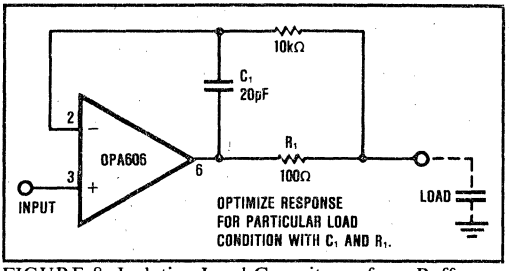


FIGURE 8. Isolating Load Capacitance from Buffer.

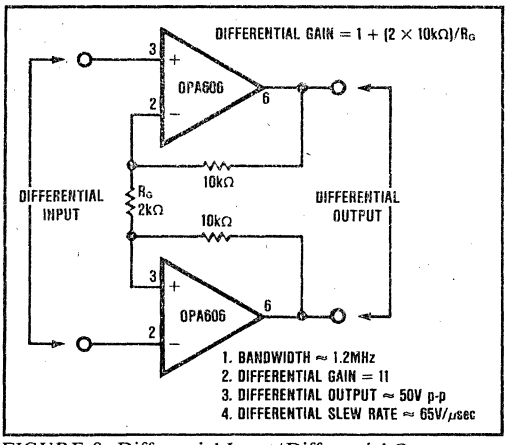


FIGURE 9. Differential Input/Differential Output Amplifier.

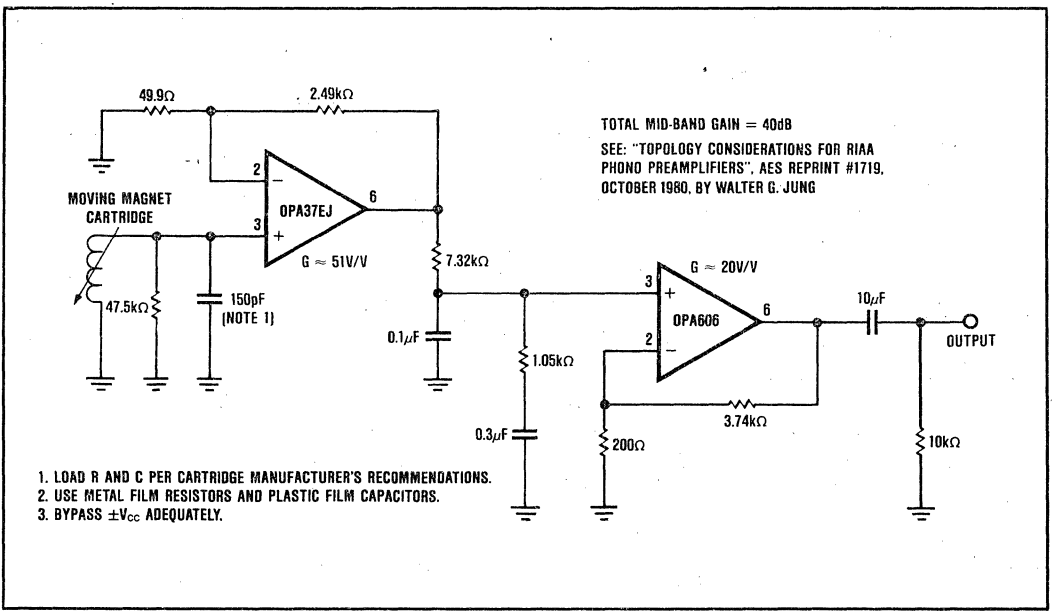


FIGURE 10. Low Noise/Low Distortion RIAA Preamplifier.

BURR-BROWN®

OPA2111

Dual Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 100% tested: 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW BIAS CURRENT: 4pA max
- LOW OFFSET: 500μV max
- LOW DRIFT: 2.8μV/°C
- HIGH OPEN LOOP GAIN: 114dB min
- HIGH COMMON-MODE REJECTION: 96dB min

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

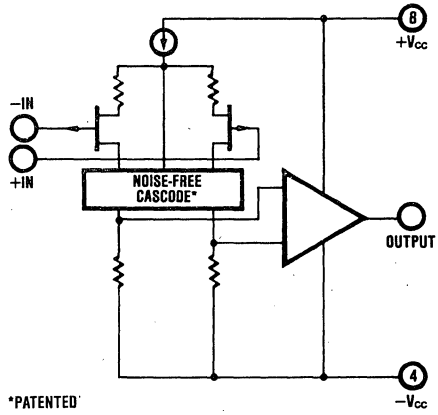
The OPA2111 is a high precision monolithic *Difet*® (dielectrically-isolated FET) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser-trimming of thin film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard dual op-amp pin configuration allows upgrading of existing designs to higher performance levels.



OPA2111 SIMPLIFIED CIRCUIT (EACH AMPLIFIER)

BIFET® National Semiconductor Corp., *Difet*® Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA2111AM			OPA2111BM			OPA2111SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
NOISE											
Voltage, f_o = 10Hz	100% tested		40	80		30	60		40	80	nV/√Hz
f_o = 100Hz	100% tested		15	40		11	30		15	40	nV/√Hz
f_o = 1kHz	100% tested		8	15		7	12		8	15	nV/√Hz
f_o = 10kHz	100% tested		6	8		6	8		6	8	nV/√Hz
f_B = 10Hz to 10kHz	100% tested		0.7	1.2		0.6	1.0		0.7	1.2	µV, rms
f_B = 0.1Hz to 10Hz	(1)		1.6	3.3		1.2	2.5		1.6	3.3	µV, p-p
Current, f_B = 0.1Hz to 10Hz	(1)		15	24		12	19		15	24	fA, p-p
f_o = 0.1Hz thru 20kHz	(1)		0.8	1.3		0.6	1.0		0.8	1.0	fA/√Hz
OFFSET VOLTAGE[2]											
Input Offset Voltage	V_{CM} = 0VDC		±0.1	±0.75		±0.05	±0.5		±0.1	±0.75	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±2	±6		±0.5	±2.8		±2	±6	µV/°C
Match			1			0.5			2		µV/°C
Supply Rejection		90	110		96	110		90	110		dB
			±3	±31		±3	±16		±3	±31	µV/V
Channel Separation	100Hz, R_L = 2kΩ		136			136			136		dB
BIAS CURRENT[2]											
Initial Bias Current	V_{CM} = 0VDC		±2	±8		±1.2	±4		±2	±8	pA
Match			1			0.5			1		pA
OFFSET CURRENT[2]											
Input Offset Current	V_{CM} = 0VDC		±1.2	±6		±0.6	±3		±1.2	±6	pA
IMPEDANCE											
Differential			10^{13} ‖ 1			10^{13} ‖ 1			10^{13} ‖ 1		Ω ‖ pF
Common-Mode			10^{14} ‖ 3			10^{14} ‖ 3			10^{14} ‖ 3		Ω ‖ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		96	110		90	110		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq$ 2kΩ	110	125		114	125		110	125		dB
Match			3			2			3		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			2			2			2		MHz
Full Power Response	20V p-p, R_L = 2kΩ	16	32		16	32		16	32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	2		1	2		1	2		V/µsec
Settling Time, 0.1%	Gain = −1, R_L = 2kΩ		6			6			6		µsec
0.01%	10V step		10			10			10		µsec
Overload Recovery, 50% Overdrive[3]	Gain = −1		5			5			5		µsec
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11	±12		±11	±12		±11	±12		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, open loop		100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		5	7		5	7		5	7	mA
TEMPERATURE RANGE											
Specification	Ambient temp.	−25		+85	−25		+85	−55		+125	°C
Operating	Ambient temp.	−55		+125	−55		+125	−55		+125	°C
Storage	Ambient temp.	−65		+150	−65		+150	−65		+150	°C
θ Junction-Ambient			200			200			200		°C/W

NOTES: (1) Sample tested—parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA2111AM			OPA2111BM			OPA2111SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range	Ambient temp.	−25		+85	−25		+85	−55		+125	°C
INPUT											
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC		±0.22	±1.2		±0.08	±0.75		±0.3	±1.5	mV
Average Drift			±2	±6		±0.5	±2.8		±2	±6	µV/°C
Match			1			0.5			2		µV/°C
Supply Rejection		86	100		90	100		86	100		dB
			±10	±50		±10	±32		±10	±50	µV/V
BIAS CURRENT[1]											
Initial Bias Current	V_{CM} = 0VDC		±125	±1nA		±75	±500		±2.0nA	±16.3nA	pA
Match			60			30			1nA		pA
OFFSET CURRENT[1]											
Input Offset Current	V_{CM} = 0VDC		±75	±750		±38	±375		±1.3nA	±12nA	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	100		90	100		86	100		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	106	120		110	120		106	120		dB
Match			5			3			5		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±10.5	±11		±10.5	±11		±10.5	±11		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
Short Circuit Current	V_O = 0VDC	10	40		10	40		10	40		mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		5	8		5	8		5	8	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage	±36VDC
Input Voltage Range (See OPA111)	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[2]	Continuous
Junction Temperature	+175°C

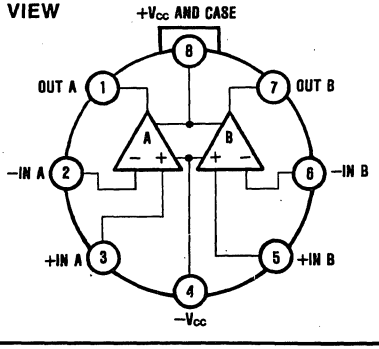
NOTES:
(1) Packages must be derated based on θ_{JC} = 150°C/W or θ_{JA} = 200°C/W.
(2) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ORDERING INFORMATION

OPA2111 X M

- Basic model number
- Performance grade
  - A, B = −25°C to +85°C
  - S = −55°C to +125°C
- Package code
  - M = TO-99 metal can

CONNECTION DIAGRAM

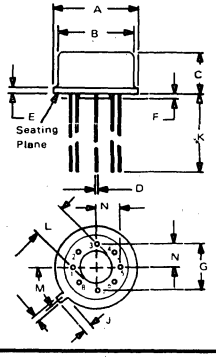


MECHANICAL "M" PACKAGE TO-99 (Hermetic)

NOTE:
Leads in true position within .010" (.25mmR) at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

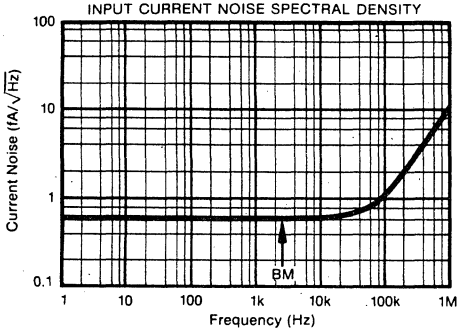


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

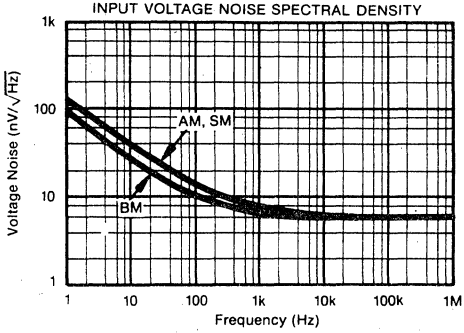
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

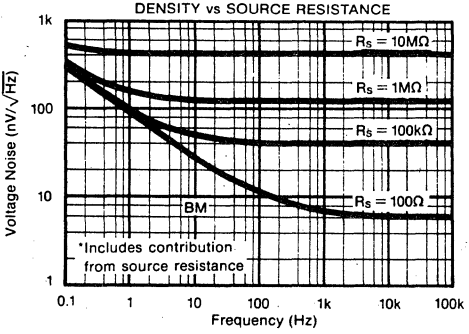
INPUT CURRENT NOISE SPECTRAL DENSITY



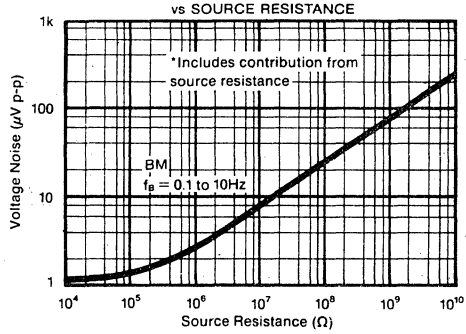
INPUT VOLTAGE NOISE SPECTRAL DENSITY



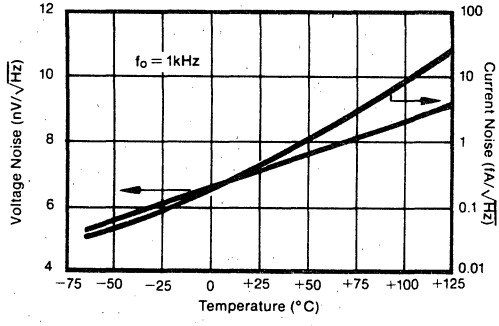
TOTAL* INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



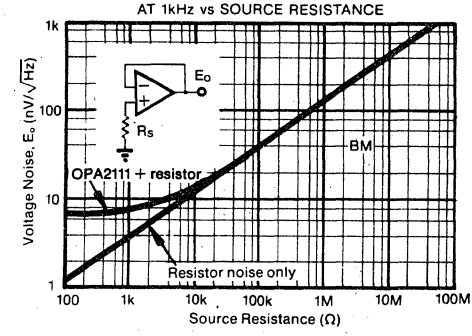
TOTAL* INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



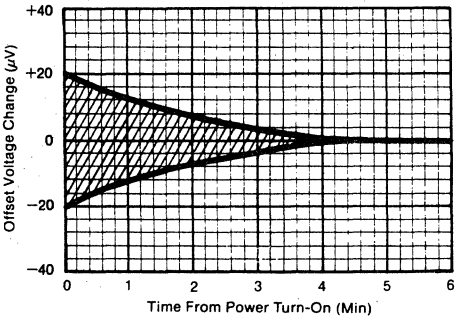
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



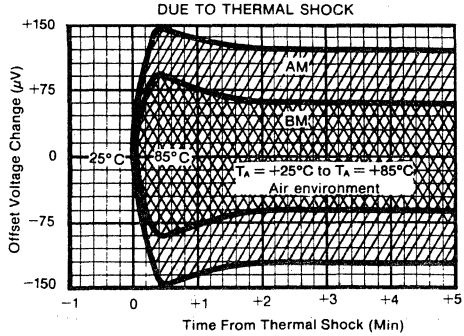
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



INPUT OFFSET VOLTAGE WARM-UP DRIFT



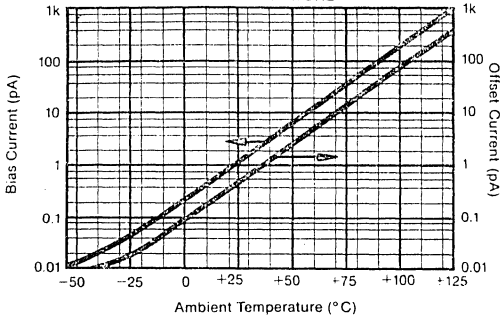
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



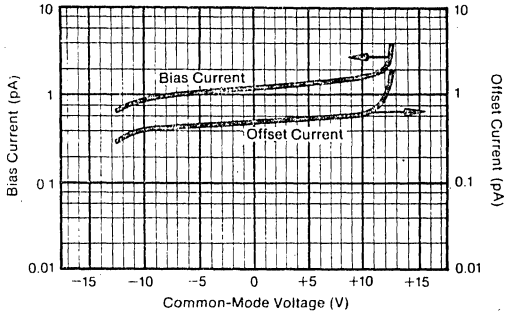
TYPICAL PERFORMANCE CURVES [CONT]

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

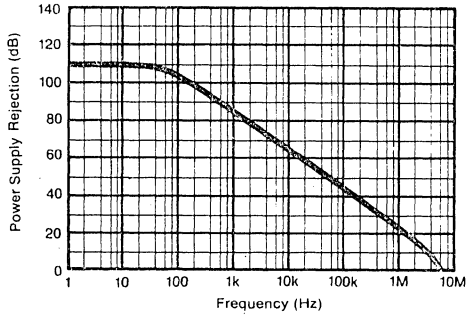
BIAS AND OFFSET CURRENT vs TEMPERATURE



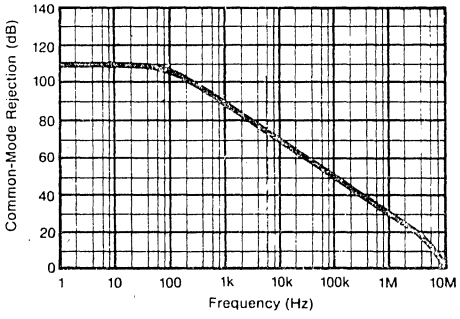
BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



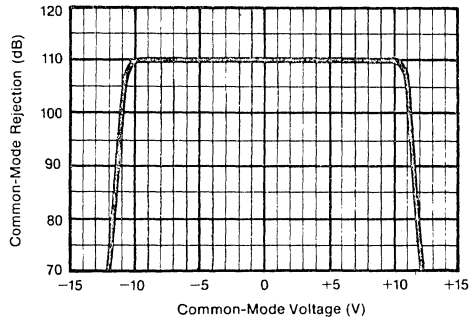
POWER SUPPLY REJECTION vs FREQUENCY



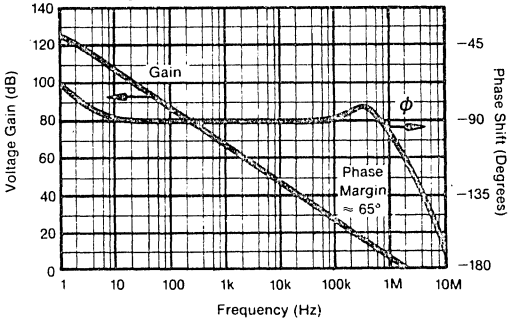
COMMON-MODE REJECTION vs FREQUENCY



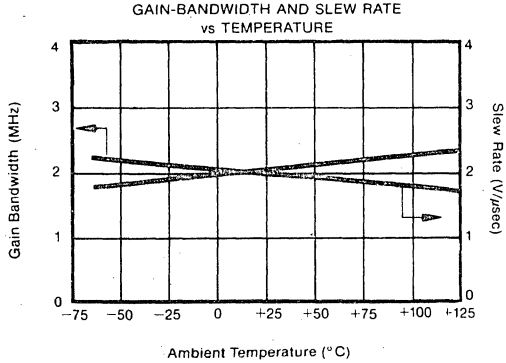
COMMON-MODE REJECTION vs INPUT COMMON MODE VOLTAGE



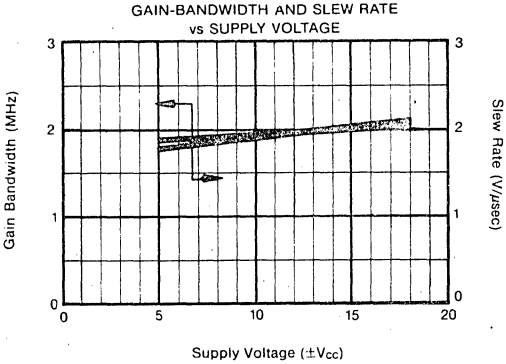
OPEN-LOOP FREQUENCY RESPONSE



GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



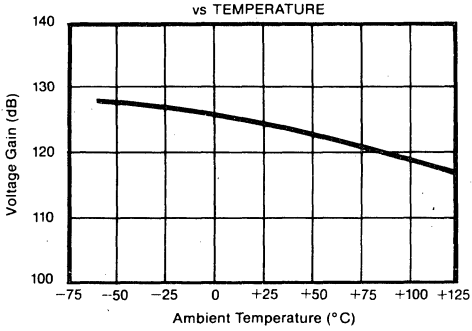
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



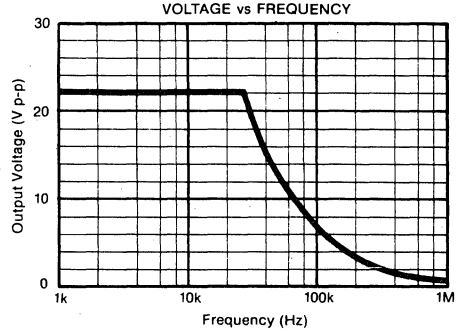
TYPICAL PERFORMANCE CURVES [CONT]

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

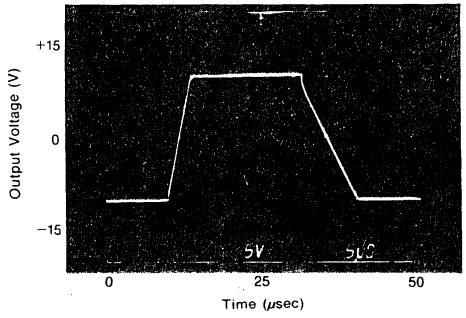
OPEN-LOOP GAIN vs TEMPERATURE



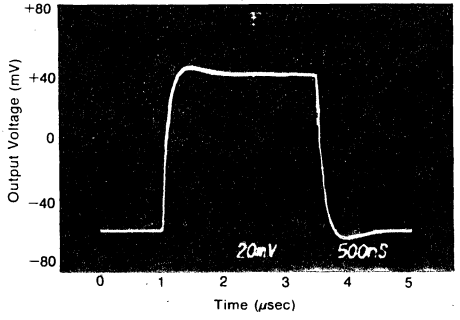
MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY



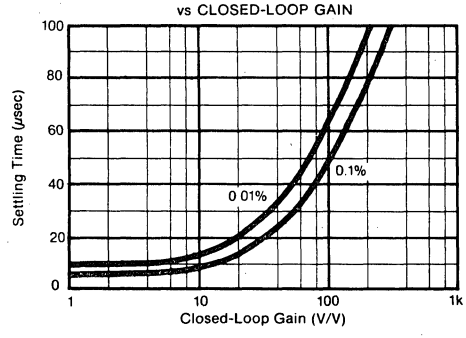
LARGE SIGNAL TRANSIENT RESPONSE



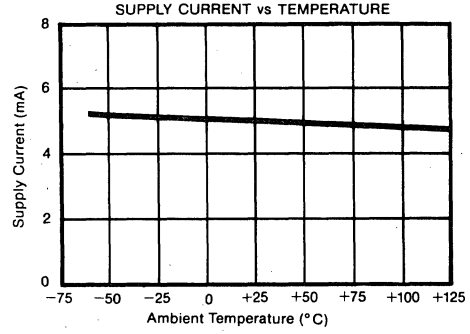
SMALL SIGNAL TRANSIENT RESPONSE



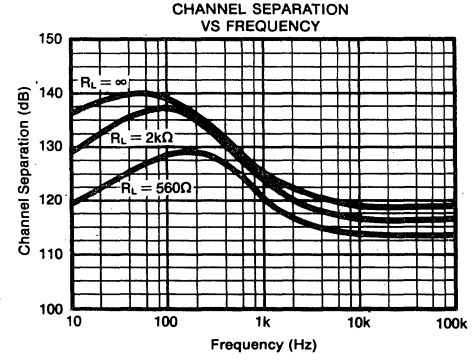
SETTLING TIME vs CLOSED-LOOP GAIN



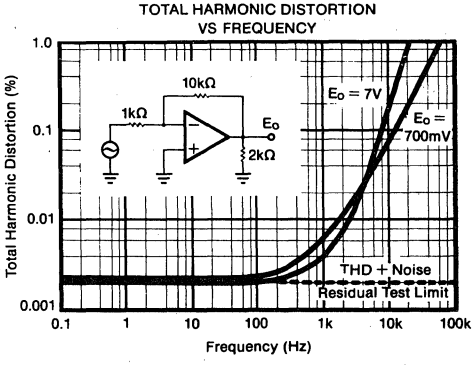
SUPPLY CURRENT vs TEMPERATURE



CHANNEL SEPARATION VS FREQUENCY



TOTAL HARMONIC DISTORTION VS FREQUENCY



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA2111 offset voltage is laser-trimmed and will require no further trim for most applications.

Offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

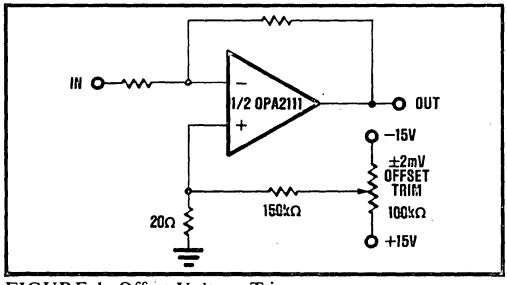


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA2111. To avoid leakage problems, it is recommended that the signal input lead of the OPA2111 be wired to a Teflon standoff. If the OPA2111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 2).

NOISE: FET VERSUS BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the low voltage noise of a bipolar operational amplifier is superior, but at higher impedances

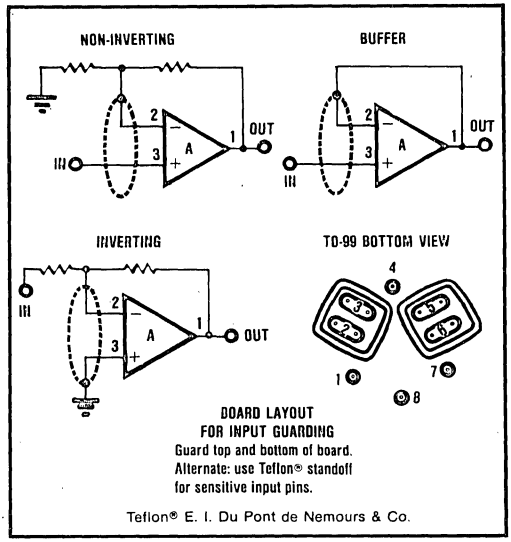


FIGURE 2. Connection of Input Guard.

the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the OPA2111 will have lower total noise than an OP-27 (see Figure 3).

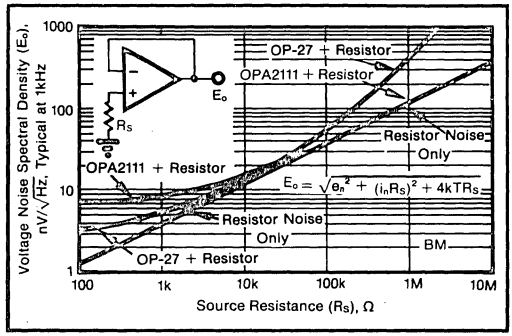


FIGURE 3. Voltage Noise Spectral Density Versus Source Resistance.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET® operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA2111 is not compromised by common-mode voltage.

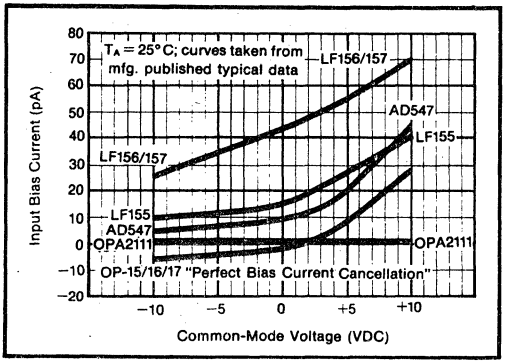


FIGURE 4. Input Bias Current Versus Common-Mode Voltage.

APPLICATIONS CIRCUITS

Figures 5 through 15 are circuit diagrams of various applications for the OPA2111.

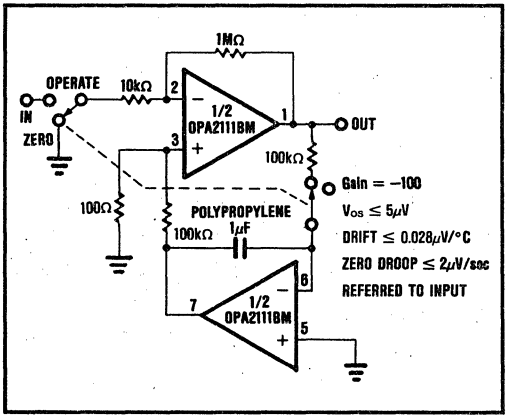


FIGURE 5. Auto-Zero Amplifier.

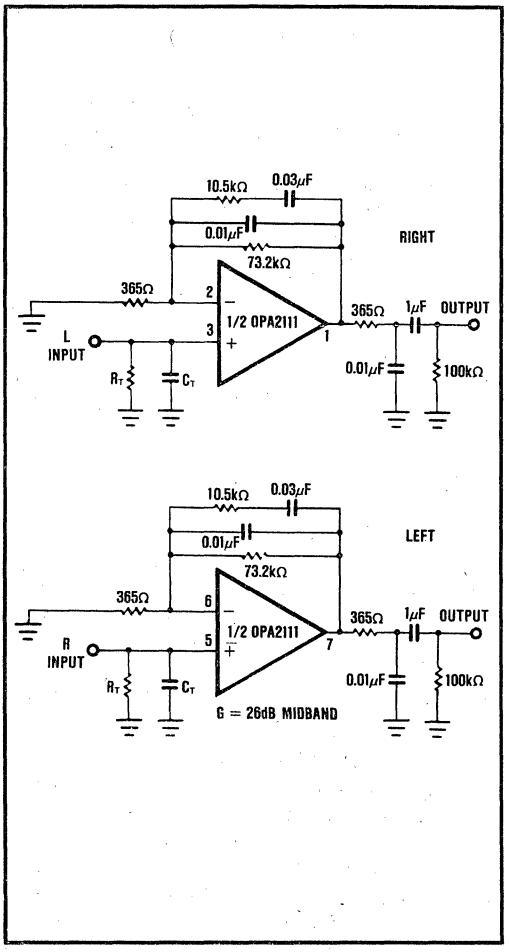


FIGURE 6. RIAA Equalized Stereo Preamplifier.

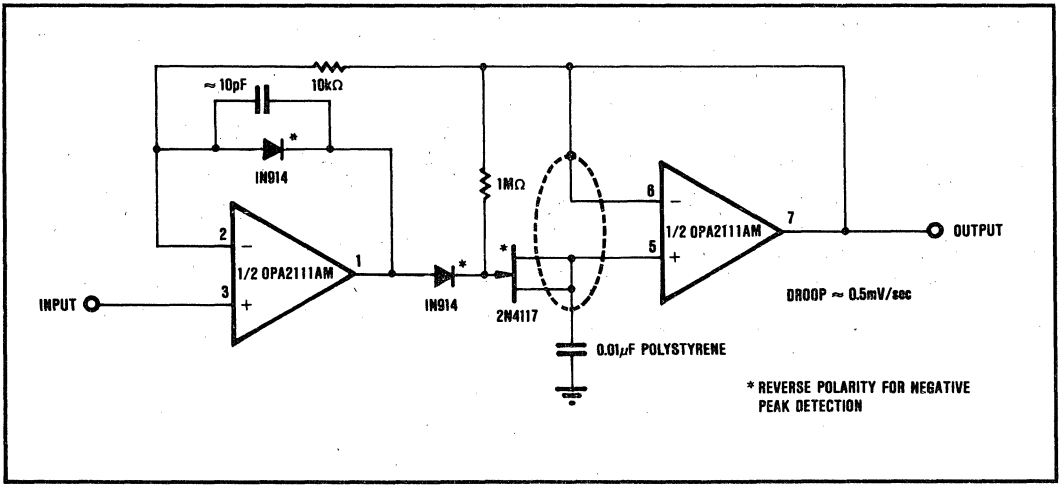


FIGURE 7. Low-Droop Positive Peak Detector.

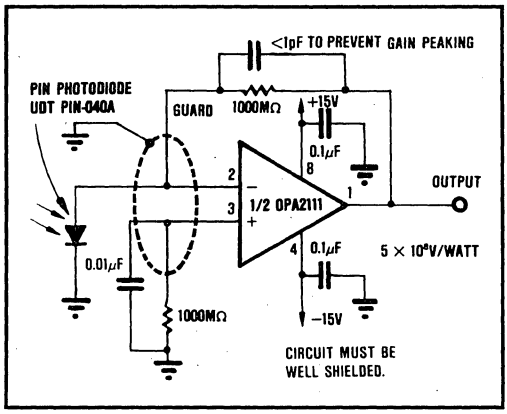


FIGURE 8. Sensitive Photodiode Amplifier.

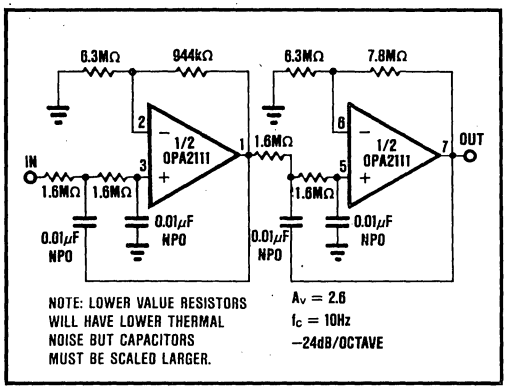


FIGURE 9. 10Hz Fourth-Order Butterworth Low-Pass Filter.

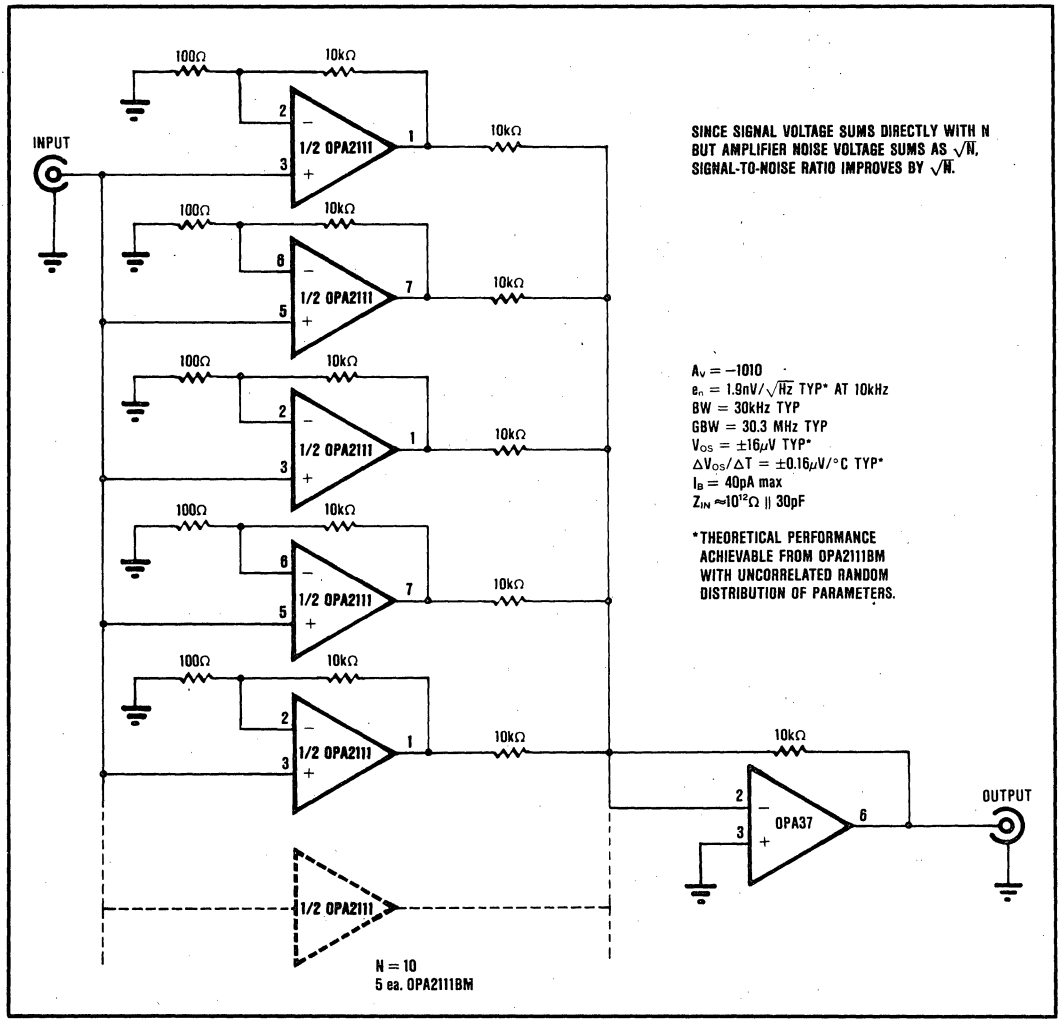


FIGURE 10. 'N' Stage Parallel-Input Amplifier.

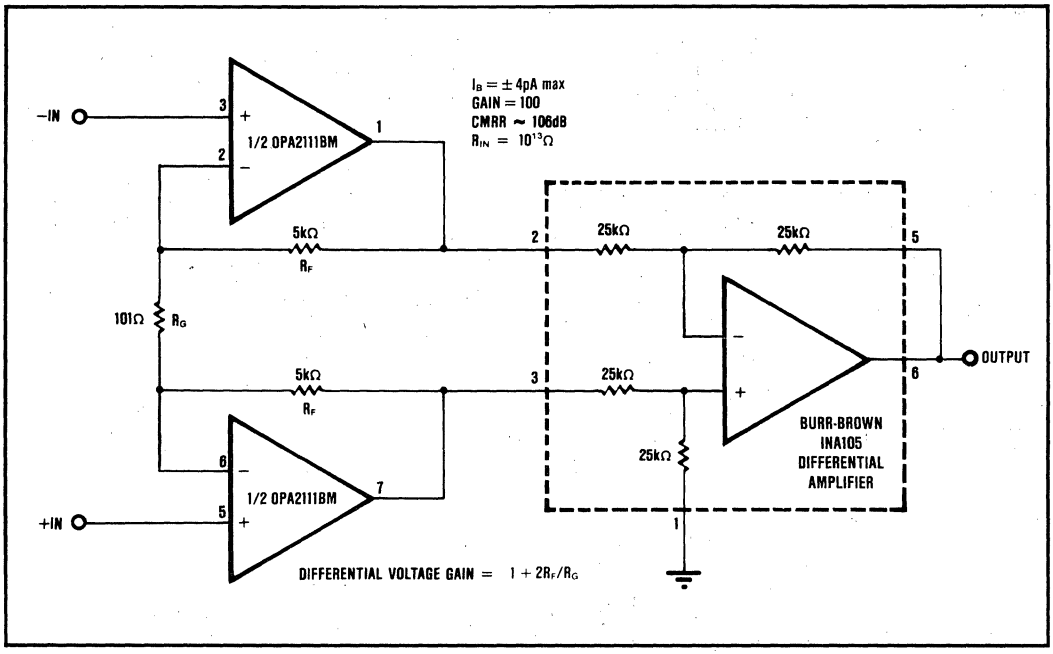


FIGURE 11. FET Input Instrumentation Amplifier.

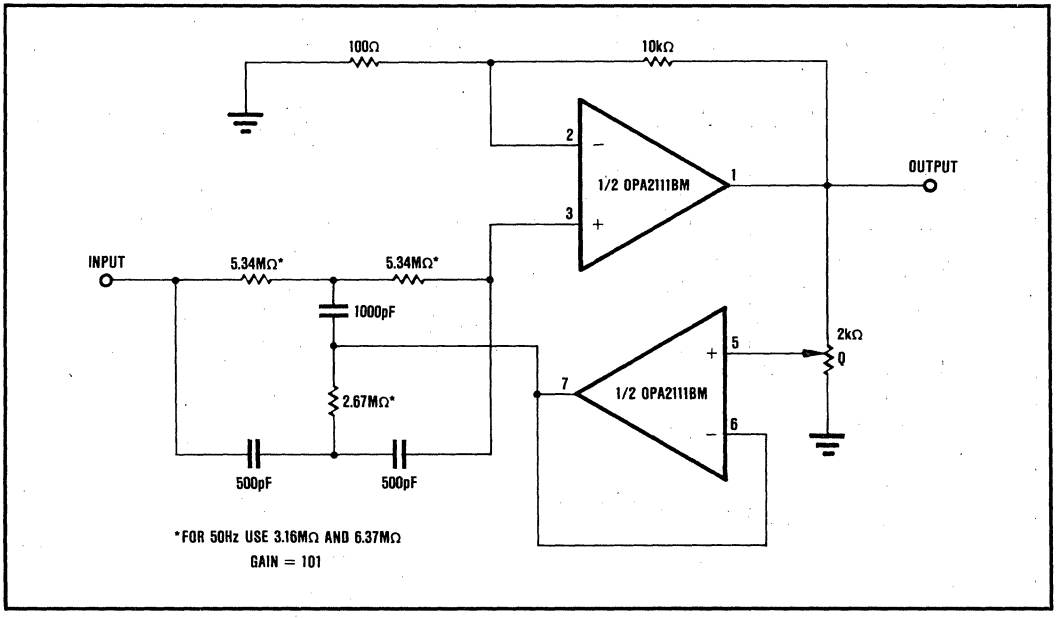


FIGURE 12. High-Impedance 60Hz Reject Filter with Gain.

BURR-BROWN®

AD515

FET-Input Electrometer OPERATIONAL AMPLIFIER

FEATURES

- ULTRA-LOW BIAS CURRENT: 0.075pA max
- LOW POWER: 1.5mA max
- LOW OFFSET: 1mV max
- LOW DRIFT: 15μV/°C max
- LOW COST
- REPLACES ANALOG DEVICES AD515

APPLICATIONS

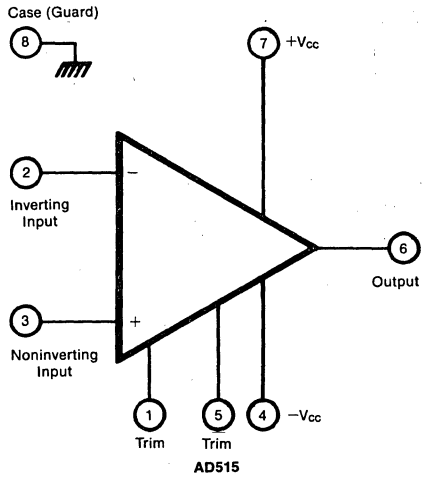
- pH SENSORS
- INTEGRATORS
- TEST EQUIPMENT
- ELECTRO-OPTICS
- CHARGE AMPLIFIERS
- GAS DETECTORS

DESCRIPTION

The Burr-Brown AD515 is a monolithic pin-for-pin replacement for the hybrid Analog Devices AD515 ultra-low bias current operational amplifier.

Laser-trimmed offset voltage and very-low bias current are important features of this popular amplifier. Monolithic construction allows lower cost and higher reliability than hybrid designs.

The AD515 is available in three electrical grades; all are specified over 0°C to +70°C and supplied in a TO-99 hermetic package.



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SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	AD515J MIN	AD515J TYP	AD515J MAX	AD515K MIN	AD515K TYP	AD515K MAX	AD515L MIN	AD515L TYP	AD515L MAX	UNITS
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain[1]	$R_L \geq 2k\Omega$	20k			40k			25k			V/V
	$R_L \geq 10k\Omega$	40k			100k			50k			V/V
	T_{MIN} to T_{MAX}, R_L = 2k	15k			40k			25k			V/V
RATED OUTPUT											
Voltage Output: R_L = 2kΩ	T_{MIN} to T_{MAX}	±10	±12		*	*		*	*		V
R_L = 10kΩ	T_{MIN} to T_{MAX}	±12	±13		*	*		*	*		V
Load Capacitance Stability	Gain = +1		1000			*			*		pF
Short Circuit Current		10	25	50	*	*	*	*	*	*	mA
FREQUENCY RESPONSE											
Unity Gain, Small Signal			350			*			*		kHz
Full Power Response	20V p-p, R_L = 2k	5	16		*	*		*	*		kHz
Slew Rate	V_O = ±10V, R_L = 2k, Gain = −1	0.3	1.0		*	*		*	*		V/μs
Overload Recovery	Gain = −1		16	100		*	*		*	*	μs
INPUT											
OFFSET VOLTAGE[2]											
Input Offset Voltage	V_{CM} = 0VDC		0.4	3.0		*	1.0		*	1.0	mV
Average Drift	T_{MIN} to T_{MAX}			50			15			25	μV/°C
Supply Rejection	T_{MIN} to T_{MAX}	68	86		80			74			dB
			50	400			100			200	μV/V
BIAS CURRENT[2]											
Input Bias Current Either Input	V_{CM} = 0VDC			300			150			75	fA
IMPEDANCE											
Differential			10^{13} ‖ 1.6			*			*		Ω ‖ pF
Common-Mode			10^{15} ‖ 0.8			*			*		Ω ‖ pF
VOLTAGE RANGE[3]											
Differential Input Range		±20			*			*			V
Common-Mode Input Range		±10	±11		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	66	94		80			70			dB
NOISE											
Voltage: 0.1Hz to 10Hz			4.0			*			*		μV p-p
f_O = 10Hz			75			*			*		nV/√Hz
f_O = 100Hz			55			*			*		nV/√Hz
f_O = 1kHz			50			*			*		nV/√Hz
Current: 0.1Hz to 10Hz			0.003			*			*		pA p-p
f_O = 10Hz to 10kHz			0.01			*			*		pA rms
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range, Derated Performance		±5		±18	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		0.8	1.5		*	*		*	*	mA
TEMPERATURE RANGE											
Specification Range	Ambient temp.	0		+70	*		*	*		*	°C
Storage	Ambient temp.	−65		+150	*		*	*		*	°C

* Specification same as AD515J.

NOTES: (1) With or without nulling of V_{OS}. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can withstand overload currents of 0.3mA indefinitely without damage.

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on θ_{JC} = 150°C/W or θ_{JA} = 200°C/W. (2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

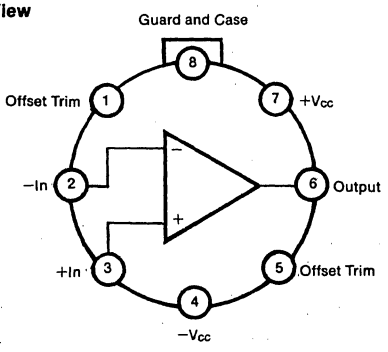
ORDERING INFORMATION

AD515 X H

- Basic model number
- Performance grade
  J, K, L = 0°C to +70°C
- Package code
  H = TO-99 metal can

CONNECTION DIAGRAM

Top View

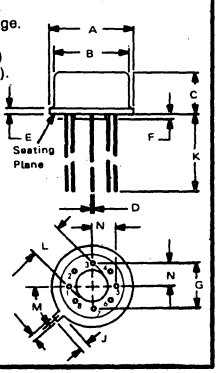


MECHANICAL

"H" PACKAGE TO-99 (Hermetic)

NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only.
Numbers may not be marked on package.
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

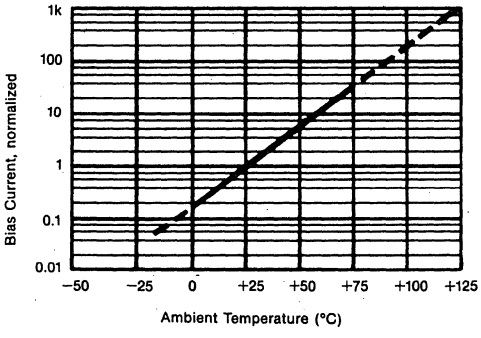
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67



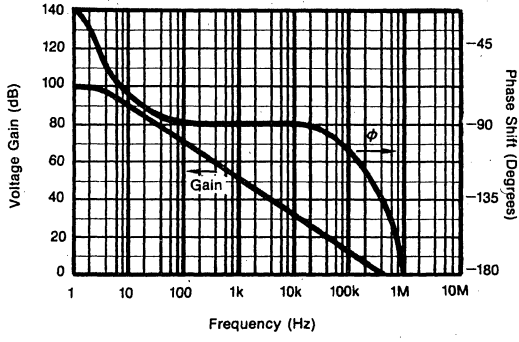
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

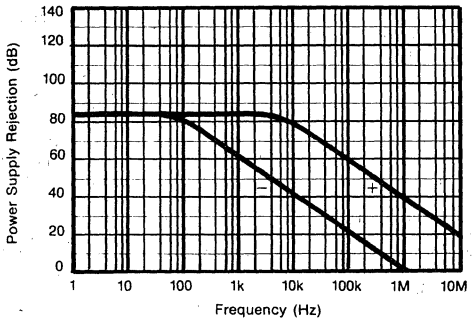
NORMALIZED BIAS CURRENT vs TEMPERATURE



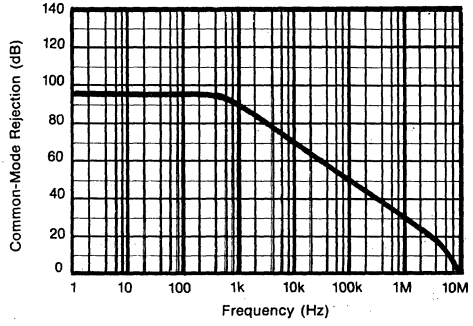
OPEN-LOOP FREQUENCY RESPONSE



POWER SUPPLY REJECTION vs FREQUENCY



COMMON-MODE REJECTION vs FREQUENCY



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

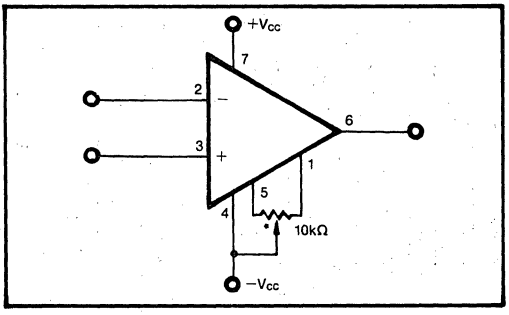


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

The AD515 requires input protection only if the source is not current limited. Limiting input current to 0.5mA with a series resistor is recommended when input voltage exceeds supply voltage.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the AD515. To avoid leakage problems, it is recommended that the signal input lead of the AD515 be wired to a Teflon standoff. If the lead is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout.

A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential. The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 2).

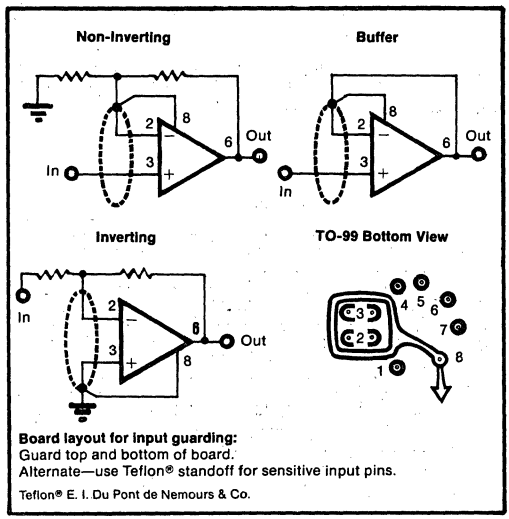


FIGURE 2. Connection of Input Guard.

BURR-BROWN®

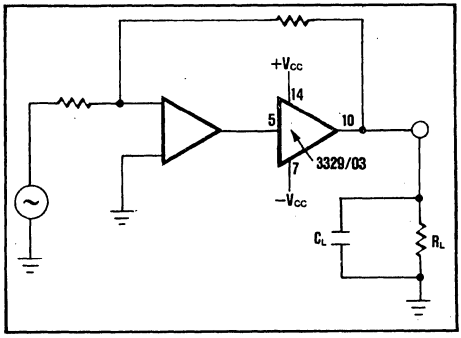
3329/03

NOT RECOMMENDED FOR NEW DESIGNS

HYBRID IC POWER BOOSTER

FEATURES

- ±100mA OUTPUT
- SHORT CIRCUIT PROTECTED
- NO HEAT SINK REQUIRED
- DUAL-IN-LINE PACKAGE



DESCRIPTION

The Model 3329/03 is a power booster amplifier designed for use in cascade with IC or discrete component operational amplifiers inside the feedback loop. Current output of up to ±100mA at ±10VDC is provided without the need for a heat sink. The unit is short circuit protected over the full temperature range or -40°C to +85°C. Output current is limited to ±15mA by internal circuitry. No external components are required. The high full power frequency (1MHz) and small signal bandwidth of 5MHz insure that the unit will not degrade the frequency response of the operational amplifier used.

The class B output stage provides high output current with a minimum of quiescent power supply drain. The low open loop output impedance (10Ω) insures stable operation with large capacitive loads, and virtually eliminates the closed loop gain loading effect of low impedance loads such as 50Ω terminated lines. Because of the 10kΩ input impedance of the booster, the current output requirements of the operational amplifier are minimal.

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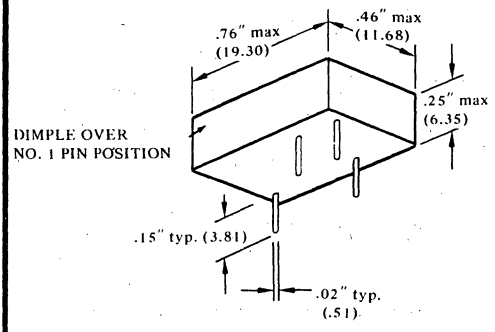
PDS-225E

MECHANICAL SPECIFICATIONS

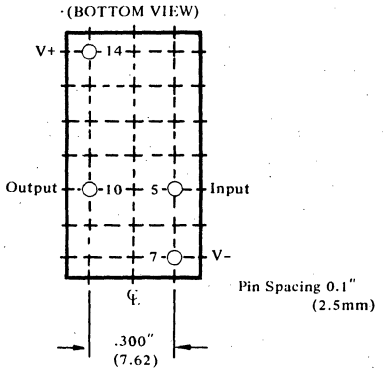
Dimensions in millimeters are shown in parentheses.

PHYSICAL DIMENSIONS



Weight: 0.12 Oz. (3.40 grams) max.
Material: Black Epoxy
Pins: Tin plated nickel
Connector: Fits any commercial dual-in-line connector

CONNECTION DIAGRAM



APPLICATIONS INFORMATION

Power Supply Requirements

The Model 3329/03 is designed to operate over a power supply range of ±12 VDC to ±18 VDC. Output voltage swing is guaranteed to be in excess of ±10 volts at full load, when operating on supplies of ±15 VDC. For other values of supply voltage, the output swing varies in proportion.

Gain and Stability

The voltage gain of the 3329/03 is approximately 1.0. The accuracy of this gain is relatively unimportant, since the booster is used inside the feedback loop of an operational amplifier. The booster by itself is completely stable under all conditions of capacitive loading. Because of it's very low output impedance, the 3329/03 tends to isolate the associated operational amplifier from the effects of capacitive load.

The input impedance of the booster is approximately equal to 100 x (load impedance). Thus, for a 100 ohm load, the input impedance is approximately 10 k ohms. The effective output impedance of the booster is approximately equal to the output impedance of the operational amplifier, divided by 100.

For most general purpose operational amplifiers the dynamic output impedance is on the order of 1 kΩ. When a low impedance load (e.g. 50Ω) is being driven, a severe loading effect occurs which greatly reduces the effective open loop gain and bandwidth. Effectively, the unloaded gain and bandwidth of the operational amplifier would be multipled by the loading factor $\frac{50}{1050} \approx .05$, if the load is 50Ω.

When the 3329/03 booster is used, however, the effective open loop output impedance is 10Ω. The loading factor now is $\frac{50}{60} = .866$, and the gain and bandwidth are reduced only slightly by this loading.

Input and Output Protection

The output stage of the 3329/03 is current limited to insure survival of the booster if the output is shunted to ground. The unit is safe even under continuous short circuit at +85°C. No heat sink is required.

The input circuitry will withstand overvoltage up to the value of supply voltage.

Temperature Range

The 3329/03 will operate over the -40°C to +85°C temperature range. Storage temperature range may vary from -55°C to +100°C.

3329/03 POWER BOOSTER SPECIFICATIONS

Rated Output		Full Power Response	-3dB Response	Input Signal Range	Input Offset Voltage	Input Impedance	Output Impedance	Power Supply Requirements		
V_O Volts (min)	I_O mA (min)	kHz (min)	MHz (min)	Volts (min)	mVolts (max)	kΩ (typ.)	Ω (typ.)	Nom. Rated Volts	Range Volts	Quies. Current mA (max)
±10	±100	1000	5	±10	±50	10	10	±15	±12 to ±18	±15

BURR-BROWN®

3500 SERIES

For a /883B version of this product, see 3500/883B in the Military Products section.

NOT RECOMMENDED FOR NEW DESIGNS

Low Bias Current OPERATIONAL AMPLIFIERS

FEATURES

- LOW BIAS CURRENT, ±15nA, max
- LOW DRIFT, ±1μV/°C, max
- LOW NOISE, 1.4μV, p-p
- WIDE SUPPLY RANGE, ±3VDC to ±20VDC
- INTERNAL COMPENSATION
- REPLACES 741 TYPE AMPLIFIERS

APPLICATIONS

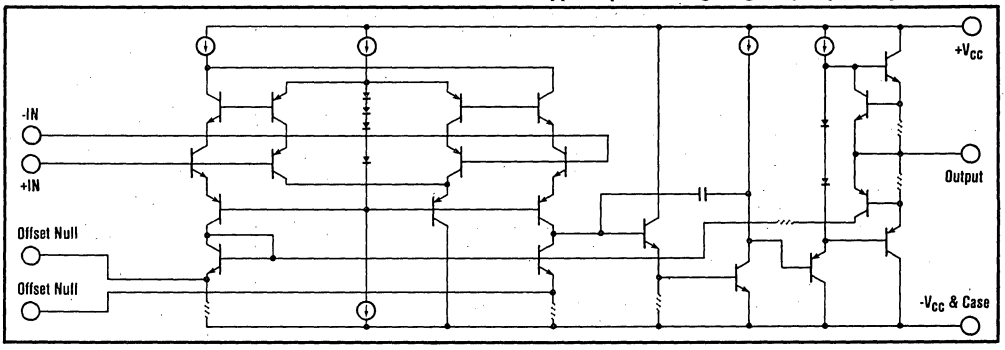
- GENERAL PURPOSE AMPLIFIER
- ANALOG COMPUTATION
- PRECISION BUFFER
- LOW DRIFT INTEGRATOR
- BRIDGE AMPLIFIER
- STABLE REFERENCE CIRCUITS

DESCRIPTION

The 3500 IC op amps are designed for low input current while maintaining slew rate and bandwidth adequate for most applications. The low input bias current is achieved by a unique bias current cancelling circuit. This method insures that the bias current remains low over the full temperature and common-mode voltage ranges. The same circuitry gives the amplifier high impedance, both differential and common-mode. The amplifier maintains internal current levels essentially constant over the full range of power supply voltages. Thus the offset voltage and drift remain low for all combinations of supply voltage.

Both military and industrial temperature range versions are offered. Drift selected units are offered at ±1, ±3, ±5, ±10, and ±20μV/°C, max. The 3500 is also a low noise IC op amp, as illustrated by the typical performance curves. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually prevent the use of IC op amps for low-level signal processing.

The 3500 is internally compensated for unconditional stability for all feedback configurations, even with capacitive loads. The slew rate is independent of supply voltage level. The input stage of the 3500 series exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high with differential inputs as high as ±30 volts, thus the amplifier can be used as a sensitive comparator. The output stage is internally current-limited to provide protection against continuous short circuits. The 3500 is interchangeable with 741 type amplifiers but gives greatly improved performance.



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SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

MODEL	3500 SERIES			
	3500A 3500R	3500B 3500S	3500C 3500T	3500E
OPEN-LOOP GAIN, DC, no load, min	93dB	*	*	100dB**
RATED OUTPUT				
Voltage, min	±10V	*	*	*
Current, min	±10mA	*	*	*
Output Impedance	2kΩ	*	*	1kΩ
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1.5MHz	*	*	*
Full Power Sine Wave, min	10kHz	12kHz	15kHz	12kHz
Slew Rate, min	0.6V/μsec	0.8V/μsec	1.0V/μsec	0.8V/μsec
INPUT OFFSET VOLTAGE				
Initial Offset at 25°C, max	±5mV	±2mV	±1mV±500μV	±500μV
Avg. vs Temp. (-25°C to +85°C) max	±20μV/°C (A)	±5μV/°C (B)	±3μV/°C (C)	+1μV/°C
(-55°C to +125°C) max	±20μV/°C (R)	±10μV/°C (S)	±5μV/°C (T)	--
vs Supply Voltage	±40μV/V	*	*	*
vs Time	±2μV/day	*	*	±5μV/mo
INPUT BIAS CURRENT				
At 25°C (either input), max	±30nA	±20nA	±15nA	±50nA
Avg. vs Temp. (-25°C to +85°C) max	±1.0nA/°C (A)	±0.5nA/°C (B)	±0.3nA/°C (C)	±0.5nA/°C
(-55°C to +125°C) max	±1.5nA/°C (R)	±1.0nA/°C (S)	±0.5nA/°C (T)	--
vs Supply Voltage	±0.2nA/V	*	*	*
INPUT DIFFERENCE CURRENT				
At 25°C	±15nA	±10nA	±7nA	±30nA, max
Avg. vs Temp. (-25°C to +85°C)	±0.5nA/°C (A)	±0.2nA/°C (B)	±0.1nA/°C (C)	±0.3nA/°C, max
(-55°C to +125°C)	±0.7nA/°C (R)	±0.5nA/°C (S)	±0.2nA/°C (T)	--
vs Supply Voltage	±0.1nA/V	*	*	*
INPUT IMPEDANCE				
Differential	$10^7\Omega$ || 3pF	*	*	*
Common Mode	$5 \times 10^9\Omega$ || 3pF	*	*	*
INPUT NOISE				
Voltage, 0.01Hz to 10Hz, p-p	2.0μV	*	*	*
10Hz to 10kHz, rms	1.4μV	*	*	*
Current, 0.01Hz, p-p	200pA	*	*	*
10Hz to 10kHz, rms	35pA	*	*	*
INPUT VOLTAGE RANGE				
Common-mode Voltage, min	±11V	*	*	*
Common-mode Rejection at ±10V	100dB	*	*	*
Maximum Safe Input Voltage***	±Vcc	*	*	*
POWER SUPPLY				
Voltage, rated specification	±15V	*	*	*
Operating Range	±3V to ±20V	*	*	*
Current, quiescent, max	±3.5mA	*	*	*
TEMPERATURE				
Operating, Rated Specs A, B, C	-25°C to +85°C	*	*	*
R, S, T	-55°C to +125°C	*	*	--
Storage	-65°C to +150°C	*	*	*

*Specifications the same as the 3500A or 3500R.

**Typical.

***If signal voltage is applied to the input in the absence of power supply voltage, series resistance should be used to limit input current to 20mA.

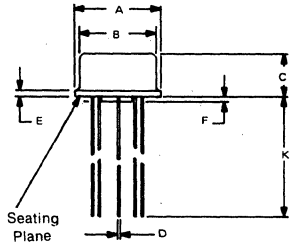
ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	500mW
Differential Input Voltage(2)	±40VDC
Input Voltage Range(2)	±20VDC
Storage Temperature Range	-65° C to +150° C
Operating Temperature Range	-55° C to +125° C
Lead Temperature (Soldering, 10 seconds)	+300° C
Output Short Circuit Duration(3)	Continuous
Junction Temperature	+150° C

NOTES:
1. Package must be derated based on: θ_{JC} = 45°C/W or θ_{JA} = 150°C/W.
2. For supply voltages less than ±20VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to power supply common only. Rating applies to +85°C ambient.

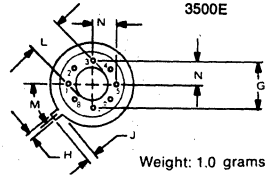
MECHANICAL

TO-99



Order Number:

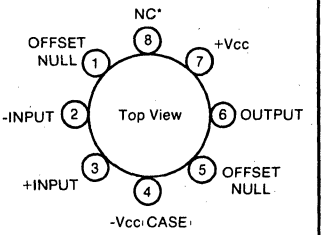
3500A
3500B
3500C
3500R
3500S
3500T
3500E



Weight: 1.0 grams

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

PIN CONFIGURATION



*No Internal Connection

BURR-BROWN®

3507J

Fast-Slewing OPERATIONAL AMPLIFIER

FEATURES

- 120V/μsec SLEW RATE
- 20MHz GAIN-BANDWIDTH PRODUCT
- INTERCHANGEABLE WITH 741 TYPES

DESCRIPTION

Burr-Brown model 3507J is intended for use in circuits requiring fast transient response-pulse amplifiers, D/A converters, comparators, fast followers, etc. Key parameters such as slew rate, settling time and bandwidth are orders of magnitude better than for most other IC op amps.

The 3507J is compensated to allow faster slewing and greater bandwidth for gains of 3 or more. For gains greater than 3, the gain rolloff is 6dB/octave. By use of a single external 20pF compensation capacitor the 3507J can be stabilized at all gains including unity. In addition, by use of an alternate compensation technique, it is possible to stabilize the 3507J at unity gain without sacrificing its faster slew rate.

The 3507J is pin-compatible with other standard IC op amps while offering greater speed and higher output current. It also is input- and output-protected to prevent damage if the output is shorted to common, or the input is shorted to supply voltage.

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PDS-297B

SPECIFICATIONS

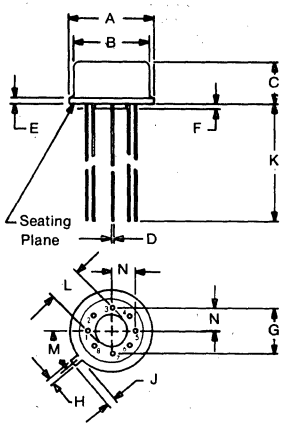
ELECTRICAL

Typical at ±15VDC and +25°C unless otherwise noted.

MODEL	3507J	
	TYPICAL	GUARANTEED
OPEN-LOOP GAIN, DC		
No Load	90dB	
2kΩLoad	83dB	77dB
RATED OUTPUT		
Voltage (1kΩ load)	±12V	±10V
Current	±20mA	±10mA
DYNAMIC RESPONSE		
Small Signal Bandwidth (0dB)	--	
Gain-Bandwidth Product (A_{CL} = 10)	20MHz	
Full Power Bandwidth	1.6MHz	1.2MHz
Slew Rate	120V/μsec	80V/μsec
Settling Time (0.1%)	200nsec	
Rise Time (10-90%, small signal)	25nsec	50nsec
Overshoot	--	--
INPUT OFFSET VOLTAGE		
Initial (without adjust) at +25°C	±5mV	±10mV
Over Temperature		±14mV
(avg. 0°C to +70°C)	±30μV/°C	
vs Supply Voltage	±30μV/V	200μV/V
vs Time	±50μV/mo	
INPUT BIAS CURRENT		
Initial at +25°C	+50nA	+250nA
Over Temperature		+500nA
(avg. 0°C to +70°C)	±0.5nA/°C	
INPUT DIFFERENCE CURRENT		
Initial at +25°C	±20nA	±50nA
Over Temperature		±100nA
(avg. 0°C to +70°C)	±0.1nA/°C	
INPUT IMPEDANCE		
Differential	100MΩ || 3pF	40MΩ
Common-Mode	1000MΩ || 3pF	
INPUT VOLTAGE RANGE		
Common-Mode (linear operation)	±12V	±10V
Differential (between inputs)		±15V
Absolute Max (either input)		±Supply
Common-Mode Rejection	90dB	74dB
POWER SUPPLY		
Rated Voltage		±15VDC
Voltage Range, derated	±8V to ±20V	
Current, quiecscent	±4mA	±6mA
TEMPERATURE RANGE		
Specifications		0°C to +70°C
Operating		-25°C to +85°C
Storage		-65°C to +150°C

MECHANICAL

TO-99 PACKAGE



NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
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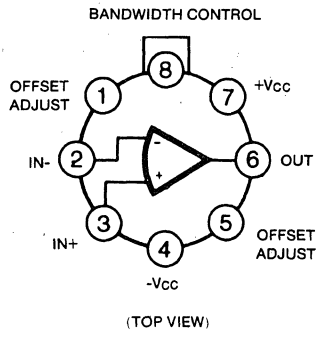
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM



(TOP VIEW)

BURR-BROWN®

3508J

Wideband OPERATIONAL AMPLIFIER

FEATURES

- 100mHz GAIN BANDWIDTH PRODUCT
- 5nA INPUT BIAS CURENT
- 103dB OPEN-LOOP GAIN

DESCRIPTION

Burr-Brown model 3508J is a wideband operational amplifier intended for use in circuits requiring extended bandwidth and high gain. Typical examples of applications are: RF signal amplifiers, fast recovery voltage references, high speed integrators, high frequency active filters, and photodiode amplifiers.

Model 3508J is internally compensated for stability at gains greater than five and thus has a high gain-bandwidth product and fast slew rate. The 3508J can be externally compensated by use of a single capacitor, and can thus be stabilized at any value of gain. By use of an alternate compensation scheme the 3508J can be stabilized at unity gain without sacrificing slew rate.

In addition to its wide bandwidth and high gain the amplifier has a number of other significant advantages over other IC op amps; low bias current, high output current, and high common-mode rejection. Inputs are protected against voltages up to the value of the power supplies. The output is current-limited to provide short-circuit protection.

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SPECIFICATIONS

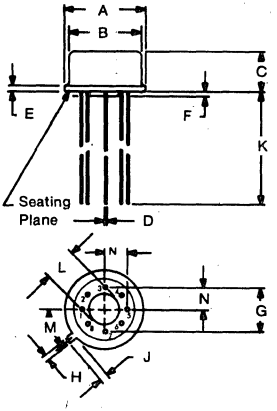
ELECTRICAL

Typical at ±15V and +25°C unless otherwise noted.

MODEL	3508J	
	TYPICAL	GUARANTEED
OPEN-LOOP GAIN, DC		
No Load	106dB	
2kΩ Load	103dB	98dB
RATED OUTPUT		
Voltage	±12V	±10V
Current	±18mA	±10mA
DYNAMIC RESPONSE		
Gain-Bandwidth Product (A_{CL} = 10)	100MHz	
Full Power Bandwidth	600kHz	320kHz
Slew Rate	35V/μsec	20V/μsec
Rise Time (10-90%, small signal)	17nsec	45nsec
INPUT OFFSET VOLTAGE		
Initial (without adjust) at +25°C	±3mV	±5mV
Over Temperature		±7mV
(avg. 0°C to +70°C)	±30μV/°C	
vs Supply Voltage	±30μV/V	±200μV/V
vs Time	±50μV/mo	
INPUT BIAS CURRENT		
Initial at +25°C	±15nA	±25nA
Over Temperature		±40nA
(avg. 0°C to +70°C)	±0.5nA/°C	
INPUT DIFFERENCE CURRENT		
Initial at +25°C	±5nA	±25nA
Over Temperature		±40nA
(avg. 0°C to +70°C)	±0.2nA/°C	
INPUT IMPEDANCE		
Differential	300MΩ ‖ 3pF	40MΩ
Common-Mode	1000MΩ ‖ 3pF	
INPUT VOLTAGE RANGE		
Common-Mode (linear operation)	±13V	±11V
Differential-Mode (between inputs)		±12V
Absolute Max (either input)		± Supply
Common-Mode Rejection	100dB	74dB
POWER SUPPLY		
Rated Voltage		±15VDC
Voltage Range, derated	±8V to ±22V	
Current, quiescent	±3mA	±4mA
TEMPERATURE RANGE		
Specification		0°C to +70°C
Operating		−25°C to +85°C
Storage		−65°C to +150°C

MECHANICAL

TO-99 PACKAGE

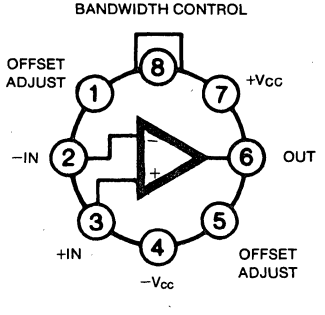


NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM



(TOP VIEW)

BURR-BROWN®

3510

For a /883B version of this product, see 3510/883B in the Military Products section.

NOT RECOMMENDED FOR NEW DESIGNS

Very-Low Drift - Precision OPERATIONAL AMPLIFIER

FEATURES

- VERY-LOW DRIFT - ±0.5µV/°C max
- VERY-LOW OFFSET - ±60µV max
- LOW BIAS CURRENT - ±15nA max
- HIGH OPEN-LOOP GAIN - 120dB min
- HIGH CMR - 110dB min
- VERY-LOW THERMAL FEEDBACK - ±0.1µV/V

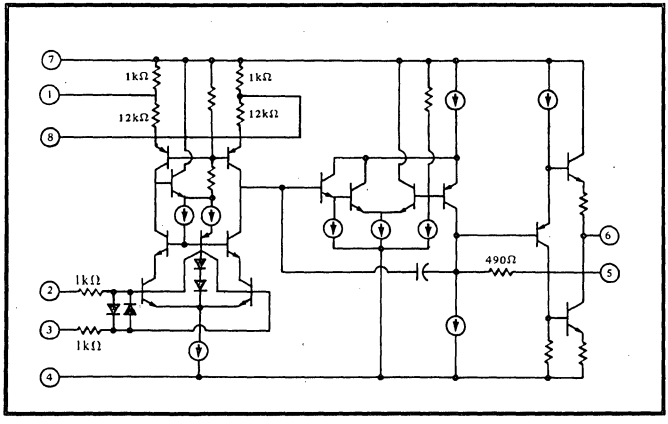
DESCRIPTION

High overall accuracy is offered by Burr-Brown's 3510 Operational Amplifier. It's designed expressly for use in high gain analog circuits where very-low drift and high accuracy are essential requirements.

This precision instrumentation grade op amp provides an economical method to maintain high circuit accuracy and reliability over temperature ranges from -25°C to +85°C, surpassing competitive units rated for only 0°C to +70°C.

Additional performance features of the 3510 include high open-loop gain, extremely-low initial offset voltage, high CMR, very-low thermal feedback, low input bias current and very-low voltage drift vs temperature.

Burr-Brown's rigid control of monolithic processing and its rigid quality control standards result in very-low voltage and current noise in the 3510. It's specifically designed for use in low level analog signal processing. Performance specifications are met exactly by precision trimming at the wafer level with complete testing before shipment. Performance of the 3510 significantly exceeds that of Burr-Brown's popular 3500 op amp.



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ELECTRICAL SPECIFICATIONS

Specifications at T_A = 25°C and ±15VDC, unless otherwise noted. Standard specifications after warm-up.

MODELS	3510AM			3510BM/3510SM			3510CM			UNITS
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN, DC										
2kΩ Load	120			*			*			dB
RATED OUTPUT										
Voltage	±10			*			*			V
Current	±10			*			*			mA
Output Resistance		300			*			*		Ω
Load Capacitance		1000			*			*		pF
FREQUENCY RESPONSE										
Unity Gain, Open Loop, Small Signal C_c = 4700pF		0.4			*			*		MHz
Closed-Loop Gain, C_c = 0, Stable Operation		≥10			*			*		V/V
Full Power Response, C_c = 0, A_{CL} = 10	7	12		*	*		*	*		kHz
Slew Rate, C_c = 0, A_{CL} = 10	0.5	0.8		*	*		*	*		V/μsec
INPUT OFFSET VOLTAGE										
Initial Offset, 25°C			150			120			60	μV
vs Temp(1) - unnulled V_{os}			2.0			1.0			0.5	μV/°C
vs Temp(1) - nulled V_{os}			2.5			1.4			0.7	μV/°C
vs Time		0.2			*			*		μV/mo
Power Supply Rejection	110	130		*	*		*	*		dB
Thermal Feedback, R_L = 2kΩ, f = 1Hz		±0.1			*			*		μV/V
INPUT BIAS CURRENT										
Initial Bias, 25°C			±35			±25			±15	nA
vs Temp(1)			±0.6			±0.4			±0.25	nA/°C
vs Supply Voltage		±0.1			*			*		nA/V
INPUT DIFFERENCE CURRENT										
Initial Difference, 25°C			±20			±15			±10	nA
vs Temp(1)			±0.4			±0.25			±0.15	nA/°C
vs Supply Voltage		±10			*			*		pA/V
INPUT IMPEDANCE										
Differential		1 ‖ 3			*			*		MΩ ‖ pF
Common-mode		10 ‖ 3			*			*		GΩ ‖ pF
INPUT NOISE										
Voltage, 0.1Hz to 10Hz		0.8			*			*		μV, p-p
f_o = 10Hz		14			*			*		nV/√Hz
f_o = 100Hz		12			*			*		nV/√Hz
f_o = 1kHz		12			*			*		nV/√Hz
Current, 0.1Hz to 10Hz		50			*			*		pA, p-p
f_o = 10Hz		0.8			*			*		pA/√Hz
f_o = 100Hz		0.46			*			*		pA/√Hz
f_o = 1kHz		0.35			*			*		pA/√Hz
INPUT VOLTAGE RANGE										
Common-mode Voltage Range, linear operation		±(|V_{cc}|-3)		*			*			V
Common-mode Rejection at ±10V	110			*			*			dB
Maximum Safe Input Voltage		±V_{cc}			*			*		V
POWER SUPPLY										
Rated Voltage		±15			*			*		VDC
Voltage Range, derated performance	±3		±20	*		*	*		*	VDC
Quiescent Current		±2.5	±3.5		*	*		*	*	mA
TEMPERATURE RANGE										
Specification, (A, B, C)	-25		+85	*		*	*		*	°C
, (S)				-55		+125				°C
Operating, derated performance	-55		+125	*		*	*		*	
Storage	-65		+150	*		*	*		*	°C
θ junction-case		40			*			*		°C/W
θ junction-ambient		190			*			*		°C/W

*Specification limits same as 3510A

(1) Temperature coefficient specifications: -25°C to +85°C for AM, BM, CM
-55°C to +125°C for SM

BURR-BROWN®

3521 SERIES
3522 SERIES

NOT RECOMMENDED FOR NEW DESIGNS

Ultra-Low Drift - FET Input OPERATIONAL AMPLIFIERS

FEATURES

- ULTRA-LOW DRIFT, 1μV/°C max
- LOW INITIAL OFFSET VOLTAGE, 250μV, max
- LOW BIAS CURRENT, 1pA, max
- LOW NOISE
- HIGH COMMON-MODE REJECTION, 90dB, typ
- WIDE POWER SUPPLY RANGE, ±5VDC to ±20VDC

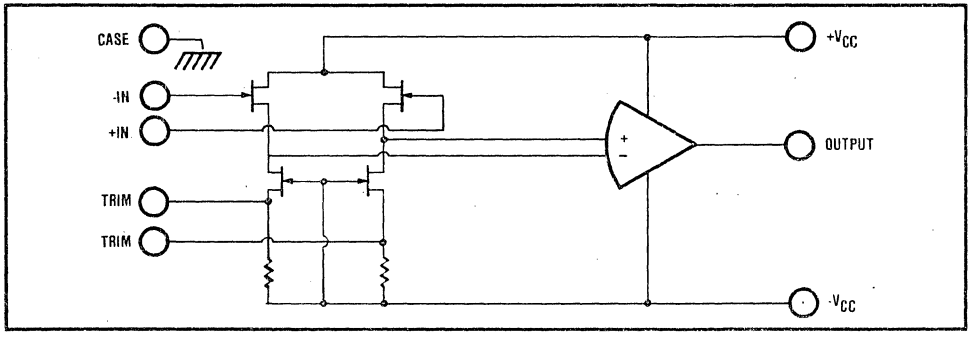
DESCRIPTION

With input offset voltage drifts as low as 1μV/°C, the Burr-Brown 3521 IC Operational Amplifier provides FET input performance combined with drift equal to the best bipolar IC's (e.g., BB3500E). The spectacular performance is achieved through truly state-of-the-art hybrid design and manufacturing, including monolithic FET pairs and active laser-trimming.

The 3521 and 3522 have an exceptionally fast thermal response. This fast warm-up is achieved without any heat-sinking.

While low drift and FET input impedance are the outstanding features of the 3521 and 3522 other specifications have not been compromised. They are internally compensated for unity-gain configuration and the initial voltage offset is guaranteed less than 250μV so for most applications the 3521 is ready to "plug-in and go." Like other low drift IC's from Burr-Brown the 3521 and 3522 have ample speed and bandwidth for most any application. (Slew rate = 0.6V/μsec). The high common-mode rejection ratio (90dB, typ.) enables them to be used as a 0.01% accurate buffer with low drift and extremely-high input impedance. The 3521/3522 also have very-low input noise to complement the low drift. The output is current limited to provide protection for continuous output shorts to common.

The 3521/3522 are pin-compatible with 741-type amplifiers, but provide FET input performance with ultra-low drift while exceeding all other specifications for general purpose operational amplifiers of the 741-type. Burr-Brown tests and guarantees all units to meet all max/min specifications.



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SPECIFICATIONS

ELECTRICAL

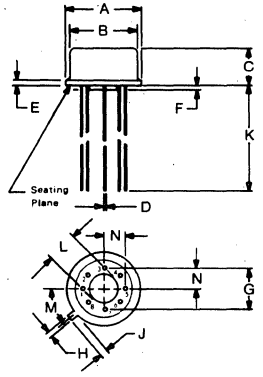
Typical at +25°C and ±15VDC power supply unless otherwise noted.

MODELS	3521H	3521J	3521K	3521L	3521R
OPEN-LOOP GAIN, DC					
Rated Load, min	94dB	*	*	*	*
RATED OUTPUT					
Voltage, min	+10V	*	*	*	*
Current, min	±10mA	*	*	*	*
Output Impedance	100Ω	*	*	*	*
FREQUENCY RESPONSE					
Unity Gain, Open-Loop	1.5MHz	*	*	*	*
Full Power Response, min	10kHz	*	*	*	*
Slew Rate, min	0.6V/μsec	*	*	*	*
INPUT OFFSET VOLTAGE					
Initial Offset, 25°C, max	±500μV	250μV	250μV	250μV	250μV
vs Temp (0°C to +70°C), **max	±10μV/°C	±5μV/°C	2μV/°C	±1μV/°C	±5μV/°C
vs Temp (-25°C to +85°C)	±15μV/°C	±8μV/°C	±4μV/°C	±2μV/°C	±2μV/°C
vs Supply Voltage	±25μV/V	*	*	*	*
vs Time	5μV/mo	*	*	*	*
INPUT BIAS CURRENT					
Initial Bias, 25°C, max	-20pA	*	-15pA	-10pA	*
(doubles every +10°C)					
vs Supply Voltage	1pA/V	*	*	*	*
INPUT DIFFERENCE CURRENT					
Initial difference, 25°C	±2pA	*	*	*	*
INPUT IMPEDANCE					
Differential	$10^{11}\Omega$	*	*	*	*
Common-mode	$10^{12}\Omega$	*	*	*	*
INPUT NOISE					
Voltage, 0.01Hz - 10Hz, p-p	4μV	*	*	*	*
Voltage, 10Hz - 1kHz, rms	2μV	*	*	*	*
Current, 0.01Hz - 10Hz, p-p	0.3pA	*	*	*	*
Current, 10Hz - 1kHz, rms	0.6pA	*	*	*	*
INPUT VOLTAGE RANGE					
Common-mode Voltage	±10V	*	*	*	*
Common-mode Rejection	90dB	*	*	*	*
Max. Safe Input Voltage	±Supply	*	*	*	*
POWER SUPPLY					
Rated Voltage	±15VDC	*	*	*	*
Voltage Range, derated	±5 to ±20VDC	*	*	*	*
Current, quiescent	±4mA	*	*	*	*
TEMPERATURE RANGE					
Specification	0°C to +70°C	*	*	*	-55°C to +125°C
Operating	-25°C to +85°C	*	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*	*

*Specification same as for 3521H.
**-55°C to +125°C for 3521R.

MECHANICAL

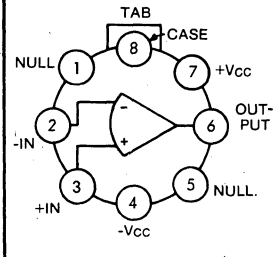
(TO-99 PACKAGE)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53"
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM

(TOP VIEW)



ELECTRICAL (CONT)

Typical at +25°C and ±15VDC power supply unless otherwise noted.

MODELS	3522J	3522K	3522L	3522S
OPEN-LOOP GAIN, DC				
Rated Load, min	94dB	•	•	•
RATED OUTPUT				
Voltage, min	±10V	•	•	•
Current, min	±10mA	•	•	•
Output Impedance	100Ω	•	•	•
FREQUENCY RESPONSE				
Unity Gain, Open-loop	1MHz	•	•	•
Full Power Response, min	10kHz	•	•	•
Slew Rate, min	0.6V/μsec	•	•	•
INPUT OFFSET VOLTAGE				
Initial Offset, 25°C, max	±1mV	±500μV	±500μV	±500μV
vs Temp (0°C to +70°C), max	±50μV/°C	±10μV/°C	±10μV/°C	
(-55°C to +125°C), max				±25μV/°C
vs Supply Voltage	±25μV/mo	•	•	•
vs Time	±10μV/mo	•	•	•
INPUT BIAS CURRENT**				
Input Bias, 25°C, max	-10pA	-5pA	-1pA	-5pA
(doubles every +10°C)				
vs Supply Voltage	±0.1pA/V	•	•	•
INPUT DIFFERENCE CURRENT				
Initial Difference, +25°C	±2pA	±1pA	±0.5pA	±1pA
INPUT IMPEDANCE				
Differential	$10^{11}\Omega$	•	•	•
Common-mode	$10^{12}\Omega$	•	•	•
INPUT NOISE				
Voltage, 0.01Hz to 10Hz, p-p	4μV	•	•	•
Voltage, 10Hz to 1kHz, rms	2μV	•	•	•
Current, 0.01Hz to 10Hz, p-p	0.3pA	•	•	•
Current, 10Hz to 1kHz, rms	0.6pA	•	•	•
INPUT VOLTAGE RANGE				
Common-mode Voltage	±10V	•	•	•
Common-mode Rejection	90dB	•	•	•
Max. Safe Input Voltage	±Supply	•	•	•
POWER SUPPLY				
Rated Voltage	±15VDC	•	•	•
Voltage Range, derated	±5VDC to ±20VDC	•	•	•
Current, quiescent	±4mA	•	•	•
TEMPERATURE RANGE				
Specification	0°C to +70°C	•	•	-55°C to +125°C
Operating	-25°C to +85°C	•	•	-55°C to +125°C
Storage	-65°C to +150°C	•	•	•

*Specification same as for 3522J.
**After Warm-Up.

BURR-BROWN®

3523 SERIES

NOT RECOMMENDED FOR NEW DESIGNS

Ultra-Low Bias Current FET OPERATIONAL AMPLIFIERS

FEATURES

- BIAS CURRENT, 0.1pA, max
- OFFSET VOLTAGE, 500μV, max
- VOLTAGE DRIFT, 25μV/°C, max
- INPUT IMPEDANCE, $10^{13}\Omega$
- Noise (10Hz), 0.003pA, p-p

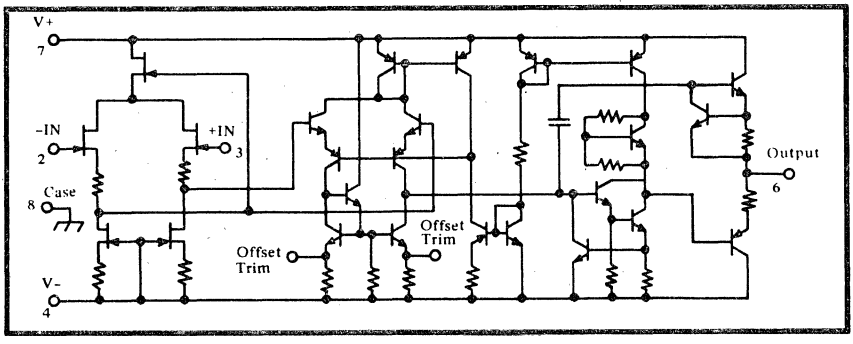
DESCRIPTION

The Burr-Brown 3523 Series amplifiers are the first IC operational amplifiers to achieve sub-picoampere input currents without exhibiting excessive offset voltage, voltage drift and voltage noise. The high common-mode rejection, ultra-low bias current, and $10^{13}\Omega$ input impedance of the 3523 make it the best choice for a variety of buffer and electrometer applications. These include pH measurement, photocurrent amplification, long term integration, and low droop sample/hold or track/hold applications. Because its input offset voltage is laser-trimmed to less than 500μV, the 3523 can usually be used without offset nulling. This is a distinct advantage in applications where it is desired to locate the 3523 near the signal source (e.g., in a signal probe).

The package of the 3523 is designed to preserve its ability to measure ultra-low currents and to avoid noise pickup. The case guard (pin no. 8) may be connected to a point which is at signal potential. This minimizes leakage current input from pins to case. Also, it shields the amplifier's sensitive input circuitry from power line frequency "hum", switching transients, and other sources of electrical noise.

Bias current specifications of the 3523 are guaranteed after warm-up in ambient air with no heat sink. Thus, the ultra-low bias current specifications become even more significant since internal power dissipation can easily raise case temperature by 20°C in many applications.

The bias current on many FET amplifiers is a strong function of applied common-mode voltage. This is not the case with the 3523. The input stage design of the 3523 make the input bias current virtually independent of the common-mode voltage over its full range.



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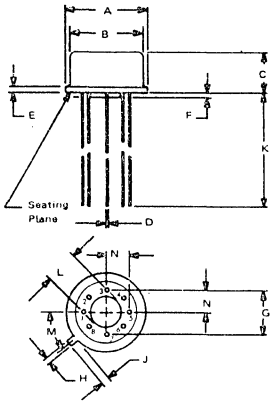
ELECTRICAL SPECIFICATIONS

Specifications typical at 25°C and ±15VDC power supply unless otherwise noted.

MODELS	3523J	3523K	3523L
OPEN-LOOP GAIN, DC no load		100dB	
1kΩ, load, min		94dB	
RATED OUTPUT			
Voltage, min		±10V	
Current min		±10mA	
Output Impedance		100Ω	
FREQUENCY RESPONSE			
Unity Gain, Open-Loop		1MHz	
Full Power Response, min		10kHz	
Slew Rate, min		0.6V/μsec	
INPUT OFFSET VOLTAGE			
Initial Offset, 25°C, max	±1mV	±500μV	±500μV
vs. Temp (0°C to 70°C), max	±50μV/°C	±25μV/°C	±25μV/°C
vs. Supply Voltage		±25μV/V	
vs. Time		±5μV/mo	
INPUT BIAS CURRENT			
Initial bias, 25°C, max	-0.5pA	-0.25pA	-0.1pA
(doubles every +10°C)			
vs. Supply Voltage		±0.01pA/V	
INPUT DIFFERENCE CURRENT			
Initial difference, 25°C	±0.2pA	±0.1pA	±0.05pA
INPUT IMPEDANCE			
Differential		$10^{12}\Omega$	
Common-mode		$10^{11}\Omega$	
INPUT NOISE			
Voltage, .01Hz to 10Hz, p-p		4μV	
10Hz to 10kHz, rms		2μV	
Current, .01Hz to 10Hz, p-p		.003pA	
10Hz to 10kHz, rms		0.01pA	
INPUT VOLTAGE RANGE			
Common-mode Voltage		±(V$\sqrt{}$-2)V	
Common-mode Rejection at 10V		80dB	
Max. Safe Input Voltage		±Supply	
POWER SUPPLY			
Rated Voltage		±15VDC	
Voltage Range, derated		±5VDC to ±20VDC	
Current, quiescent		±4mA	
TEMPERATURE RANGE			
Specification		0°C to +70°C	
Operating		-55°C to +125°C	
Storage		-65°C to +150°C	

MECHANICAL



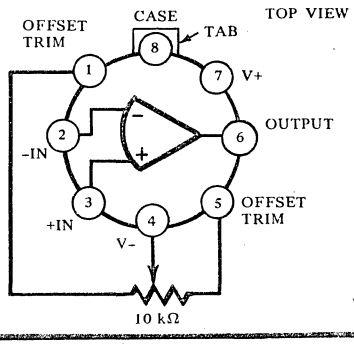
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Dimensions in inches are in parentheses. Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

CONNECTION DIAGRAM



BURR-BROWN®

3527

NOT RECOMMENDED FOR NEW DESIGNS

Low Drift - Low Bias Current FET Input OPERATIONAL AMPLIFIER

FEATURES

- LOWER PRICED
- ULTRA-LOW DRIFT, 2μV/°C, max
- LOW INITIAL OFFSET VOLTAGE, 250μV, max
- LOW BIAS CURRENT, 2pA, max
- LOW NOISE

APPLICATIONS

- CURRENT-TO-VOLTAGE CONVERSION
- LONG TERM INTEGRATION
- LOW DROOP SAMPLE/HOLD CIRCUITS
- PRECISION VOLTAGE AMPLIFICATION
- HIGH INPUT RESISTANCE BUFFER

DESCRIPTION

The Burr-Brown 3527 is a precision operational amplifier. It offers excellent performance at moderate cost through the use of hybrid construction, monolithic ICs, matched FETs, thin-film resistors, and active laser trimming.

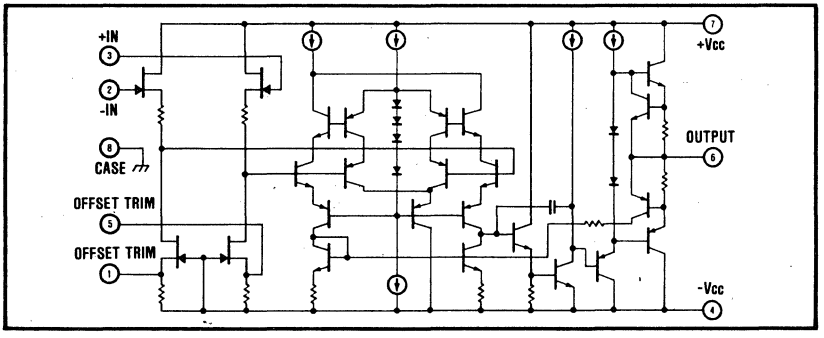
The 3527 low, initial offset voltage (250μV max) allows higher design accuracy at lower installed cost. Costly pots and external nulling of the offset voltage are not required for most applications. Also, higher system reliability is achieved by using fewer parts.

The offset voltage temperature drift of the 3527 is exceptionally low (2μV/°C max) and is compatible with the best bipolar amplifiers (BB3500E). It is achieved by laser adjusting the offset during manufacture and means that high system accuracy is maintained over the temperature range.

The low bias current (guaranteed 2pA max) allows the use of larger feedback resistor values, and smaller bias current errors are realizable.

Of course, all the other desirable features of high quality op amps are engineered into the 3527. It has low input noise, is free from latch up, is short circuit protected for continuous output shorts to common, is internally compensated for unity gain stability, and is pin compatible with 741 amplifiers. Guarding is achieved by the pin 8 case connection.

For increased reliability screening, consult Burr-Brown.



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SPECIFICATIONS

ELECTRICAL

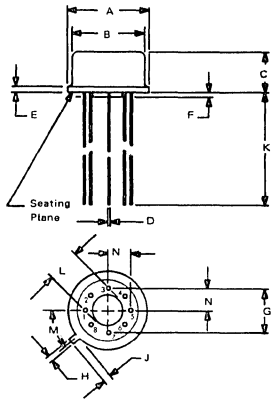
Specifications typical at T_A = 25°C and ±15VDC supplies, unless otherwise noted.

MODELS	3527AM			3527BM			3527CM			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN, DC										
No Load		112			•			•		dB
R_L = 2kΩ	100	108		•	•		•	•		dB
RATED OUTPUT										
Voltage	±10	±12		•	•		•	•		V
Current	±10	±20		•	•		•	•		mA
Output Impedance		600			•			•		Ω
Load Capacitance		1000			•			•		pF
FREQUENCY RESPONSE										
Unity Gain, Open Loop		1			•			•		MHz
Full Power Response	10	14		•	•		•	•		kHz
Slew Rate	0.6	0.9		•	•		•	•		V/μsec
Settling Time (0.01%)		45			•			•		μsec
INPUT OFFSET VOLTAGE										
Initial Offset, 25°C		±200	±500		±100	±250		±100	±250	μV
vs. Temp. (-25°C to +85°C)		±5	±10		±2	±5		±1	±2	μV/°C
vs. Supply Voltage		±75			•			•		μV/V
vs. Time		±20			•			•		μV/mo
INPUT BIAS CURRENT										
Initial Bias, 25°C		-2	-5		-0.7	-2		-2	-5	pA
vs. Temp		**			**			**		
vs. Supply Voltage		±5			•			•		pA/V
INPUT DIFFERENCE CURRENT										
Initial Difference, 25°C		±0.3			•			•		pA
INPUT IMPEDANCE										
Differential		10^{12}			•			•		Ω
Common-mode		10^{15}			•			•		Ω
INPUT NOISE										
Voltage, f_o = 10Hz		75			•			•		nV/√Hz
f_o = 100Hz		35			•			•		nV/√Hz
f_o = 1kHz		30			•			•		nV/√Hz
f_o = 10kHz		25			•			•		nV/√Hz
0.3Hz to 10Hz, p-p		2.6			•			•		μV
10Hz to 10kHz, rms		3			•			•		μV
Current, 0.3Hz to 10Hz, p-p		15			•			•		fA
10Hz to 10kHz, rms		60			•			•		fA
INPUT VOLTAGE RANGE										
Common-mode Voltage Range		±(|Vs|-3)			•			•		V
Common-mode Rejection at ±10V		76			•			•		dB
Max. Safe Input Voltage		±Vs			•			•		VDC
POWER SUPPLY										
Rated Voltage		±15			•			•		VDC
Voltage Range, derated performance	±5		±20	•		•	•		•	VDC
Current, quiescent		2.6	4		•	•		•	•	mA
TEMPERATURE RANGE (ambient)										
Specification	-25		+85	•		•	•		•	°C
Operating	-55		+125	•		•	•		•	°C
Storage	-65		+150	•		•	•		•	°C
θ junction-ambient		235			•			•		°C/W

*Specifications same as for 3527AM.
**Doubles every +10°C.

MECHANICAL TO-99 PACKAGE

Order Number: 3527AM, 3527BM, 3527CM Weight: 1 gram



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
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F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	---	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
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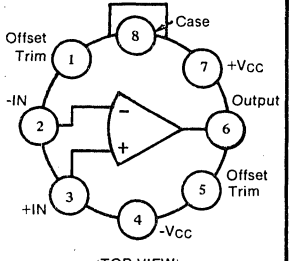
Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CONNECTION DIAGRAM



(TOP VIEW)

BURR-BROWN®

3528

NOT RECOMMENDED FOR NEW DESIGNS

Ultra Low Bias Current FET OPERATIONAL AMPLIFIER

FEATURES

- 75fA MAX INPUT BIAS CURRENT
- 250μV MAX OFFSET VOLTAGE
- 5μV/°C MAX OFFSET VOLTAGE DRIFT

APPLICATIONS

- PHOTODIODE AMPLIFIER
- PHOTOMULTIPLIER TUBE AMPLIFIER
- LOW DRIFT INTEGRATOR
- CURRENT-TO-VOLTAGE CONVERTER

DESCRIPTION

An excellent combination of specifications for applications requiring ultra low input bias currents are provided by the 3528 amplifier family. These applications include photometers, selective ion detectors, long term integrators and low-droop sample hold circuits.

The 3528 is unique in that in addition to providing bias currents as low as 75fA (3528CM) it also provides very low offset voltage drift (5μV/°C max, 3528BM) and offset voltage (250μV, 3528BM). Thus, user trimming offset voltage with an external potentiometer is usually avoided.

The output is protected from damage due to short circuits to ground or either supply and the unit is specified over the full -25°C to +85°C temperature range rather than the more limited 0°C to 70°C range.

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ELECTRICAL SPECIFICATIONS

At $T_A = 25°C$ and $\pm V_{cc} = \pm 15VDC$ unless otherwise noted.

PARAMETER	CONDITIONS	3528AM			3528BM			3528CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN LOOP GAIN, DC											
$R_L \geq 2k$	$V_o = 20V$ p-p	88	93		92	95		90	93		dB
$R_L \geq 10k$	$V_o = 20V$ p-p	94	114		100	*		98	*		
RATED OUTPUT											
Voltage	$R_L = 2k\Omega$	±10	±12		*	*		*	*		V
	$R_L = 10k$	±12	±13		*	*		*	*		V
Current	$V_o = \pm 10V$	±5	±10		*	*		*	*		mA
Output Resistance Open Loop	f = DC		1.5	3		*	*		*	*	kΩ
Short Circuit Current	$R_L = 0\Omega$		19			*			*		mA
DYNAMIC RESPONSE											
Bandwidth, Unity Gain	Small Signal		0.7			*			*		MHz
Full Power Bandwidth	$R_L = 2k\Omega$	5	11		*	*		*	*		kHz
Slew Rate	$R_L = 2k\Omega$	0.3	0.7		*	*		*	*		V/μsec
Settling time	to 1%		30			*			*		μs
	to 0.1%		150			*			*		μs
	to 0.01%		1			*			*		ms
INPUT OFFSET VOLTAGE											
Initial Offset	$T_A = 25°C$		±200	±500		±100	±250		±200	±500	μV
vs Temperature	$-25°C \leq T_A \leq +85°C$		±5	±15		±2	±5		±5	±10	μV/°C
vs Supply Voltage	$\pm V_{CC} = 15V$ to 20V, to 5V		±25	±100		*	*		*	*	μV/V
vs Time			20			*			*		μV/mo
INPUT BIAS CURRENT											
Initial	$T_A = 25°C$			-300			-150			±75	fA
at Temperature	at $T_A = 85°C$		-40	-60		-20	-30		-10	-15	pA
vs Supply Voltage			1			*			*		fA/V
INPUT DIFFERENCE CURRENT											
Initial	$T_A = 25°C$		±80			±40			±20		fA
at Temperature	at $T_A = 85°C$		±8			±4			±2		pA
INPUT IMPEDANCE											
Differential			$10^{13} \parallel 0.8$			*			*		Ω ‖ pF
Common-mode			$10^{15} \parallel 1$			*			*		Ω ‖ pF
INPUT NOISE											
Voltage Noise Density	$f_o = 1Hz$		475			*			*		nV/√Hz
	$f_o = 10Hz$		120			*			*		nV/√Hz
	$f_o = 100Hz$		55			*			*		nV/√Hz
	$f_o = 1kHz$		40			*			*		nV/√Hz
	$f_o = 10kHz$		40			*			*		nV/√Hz
Voltage Noise	$f_B = 0.3Hz$ to 10Hz		6			*			*		μV, p-p
	$f_B = 10Hz$ to 10kHz		4			*			*		μV, rms
Current Noise Density	$f_o = 1Hz$		0.25			0.2			0.15		fA/√Hz
	$f_o = 10Hz$		0.25			0.2			0.15		fA/√Hz
	$f_o = 100Hz$		0.25			0.2			0.15		fA/√Hz
	$f_o = 1kHz$		0.25			0.2			0.15		fA/√Hz
Current Noise	$f_B = 0.3Hz$ to 10Hz		7			5			4		fA, p-p
	$f_B = 10Hz$ to 10kHz		26			20			15		fA, rms
INPUT VOLTAGE RANGE											
Common-mode Voltage Range	Linear Operation		$\pm(V_{cc}-3)$			*			*		V
Common-mode Rejection	f = DC, $V_{CM} = \pm 10V$	66	74		80	86		70	86		dB
Max. Safe Input Voltage			$\pm V_{cc}$			*			*		V
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range, derated performance		±5		±20	*		*	*		*	V
Current, quiescent			1	1.5		*	*		*	*	mA
TEMPERATURE RANGE (ambient)											
Specification		-25		+85	*		*	*		*	°C
Operating, derated performance		-55		+125	*		*	*		*	°C
Storage		-65		+150	*		*	*		*	°C

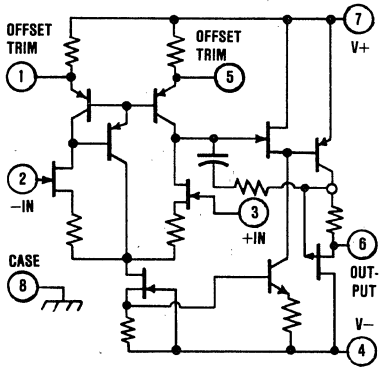
BURR-BROWN®

3550 SERIES

Fast-Settling FET OPERATIONAL AMPLIFIERS

FEATURES

- SETTLING TIME (0.01%), 600nsec, max
- TRUE DIFFERENTIAL INPUT
- SLEW RATE, 100V/μsec, min
- FULL POWER, 1.5MHz, min
- INPUT IMPEDANCE, $10^{11}\Omega$
- INTERNALLY COMPENSATED
- STABLE OPERATION, 1000pF, typ



DESCRIPTION

The 3550 is specifically designed for fast transient applications such as D/A and A/D conversion, sample/hold, multiplexer buffering and pulse amplification where the primary amplifier requirements are fast settling, good accuracy, and high input impedance.

Because the 3550 is internally compensated, elaborate compensation schemes requiring external components are not necessary. The smooth 6dB/octave rolloff of open-loop gain and the low output impedance provides the excellent step response and smooth settling without sacrificing frequency stability (no oscillations even with 1000pF of capacitive load)! A 10 to 1 improvement in settling time with large capacitive loads can be obtained with the addition of a single capacitor.

Unlike many wideband and fast settling amplifiers the 3550 has a true differential input. This means it can provide its excellent transient performance in the inverting, non-inverting, current to voltage, and difference configurations.

The 3550J and S have identical specifications except for temperature range: The 3550J is specified for 0°C to +70°C and the 3550S is specified for -55°C to +125°C. The 3550K has improved dynamic specifications and is specified over the 0°C to +70°C temperature range.

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SPECIFICATIONS

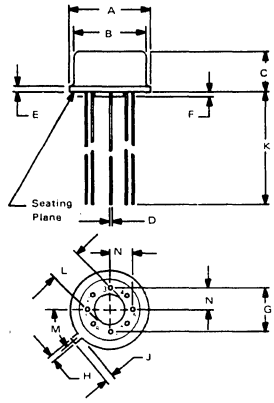
ELECTRICAL

Specifications typical at +25°C and ±15VDC Power Supply unless otherwise noted.

MODELS	3550J	3550K	3550S
OPEN LOOP GAIN, DC			
No load		100dB	
1kΩ, load min		88dB	
RATED OUTPUT			
Voltage, min		±10V	
Current, min		±10mA	
Open-loop Output Resistance		100Ω at 1MHz	
DYNAMIC RESPONSE			
Bandwidth (0dB, small signal)	10MHz	20MHz	10MHz
Full Power Response, min	1.0MHz	1.5MHz	1.0MHz
Slew Rate, min	65V/μsec	100V/μsec	65V/μsec
Settling Time (0.01%), max	1μsec	0.6μsec	1μsec
INPUT OFFSET VOLTAGE			
Initial Offset, +25°C, max		±1mV	
vs Temperature		±50μV/°C	
vs Supply Voltage		±500μV/V	
vs Time		±100μV/mo	
INPUT BIAS CURRENT			
Initial Bias, +25°C, max		−100pA (after full warm-up)	
vs Temperature		doubles every 10°C	
vs Supply Voltage		±1pA/V	
INPUT DIFFERENCE CURRENT			
Initial Difference, +25°C		±40pA	
INPUT IMPEDANCE			
Differential		$10^{11}\Omega$ || 3pF	
Common Mode		$10^{11}\Omega$ || 3pF	
INPUT NOISE			
Voltage, 0.01Hz - 10Hz, p-p		20μV	
10Hz - 10kHz, rms		4μV	
Current, 0.01Hz - 10Hz, p-p		0.2pA	
10Hz - 10kHz, rms		1.5pA	
INPUT VOLTAGE RANGE			
Common-Mode Voltage		±(|V_{cc}| −5)V	
Common-Mode Rejection		70dB at +5V, −10V	
Safe Input Voltage, max		±Supply	
POWER SUPPLY			
Rated Voltage		±15VDC	
Voltage Range, derated		±5VDC to ±20VDC	
Current, quiescent[1]		11mA (15mA max)	
TEMPERATURE RANGE			
Specification	0°C to +70°C		−55°C to +125°C
Operating	−55°C to +125°C		−55°C to +125°C
Storage		−65°C to +150°C	

NOTES:
1. The use of a finned heat sink is recommended.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.

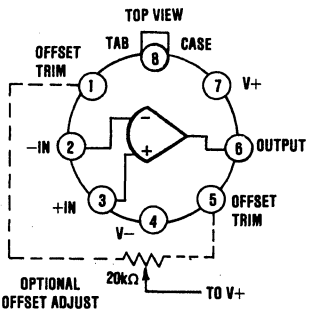
BOTTOM VIEW

Dimensions in inches are in parentheses.

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

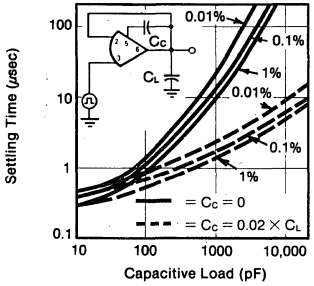
CONNECTION DIAGRAM



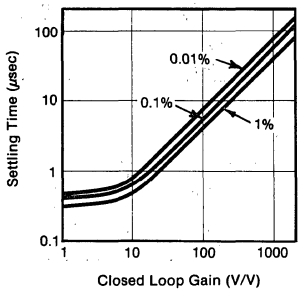
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$ $\pm V_{CC} = 15VDC$ unless otherwise indicated.

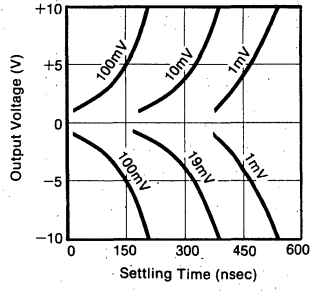
SETTLING TIME VS CAPACITIVE LOAD



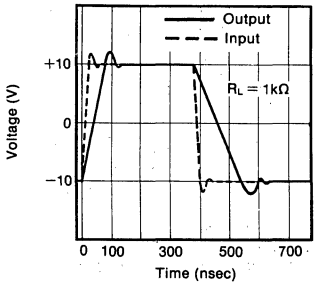
SETTLING TIME VS CLOSED LOOP GAIN



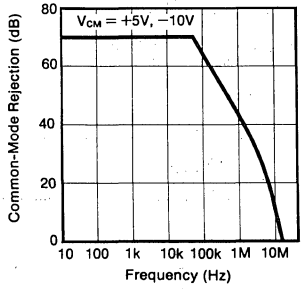
SETTLING TIME VS OUTPUT VOLTAGE CHANGE



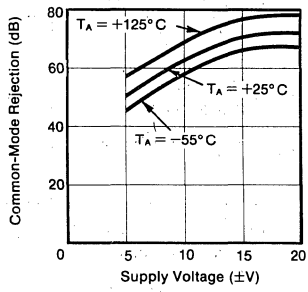
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



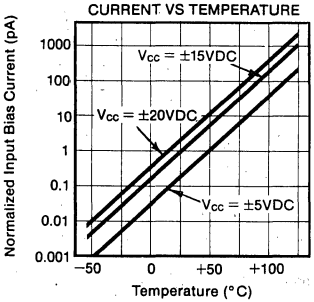
COMMON MODE REJECTION VS FREQUENCY



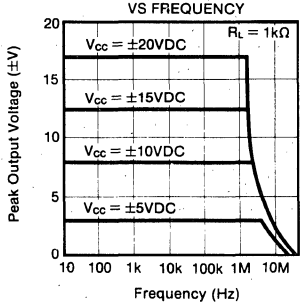
COMMON MODE REJECTION VS SUPPLY VOLTAGE



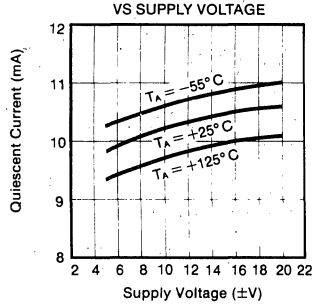
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



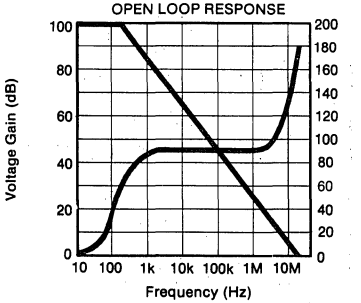
OUTPUT VOLTAGE VS FREQUENCY



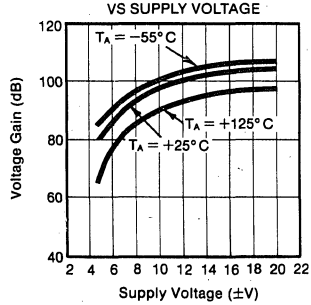
QUIESCENT CURRENT VS SUPPLY VOLTAGE



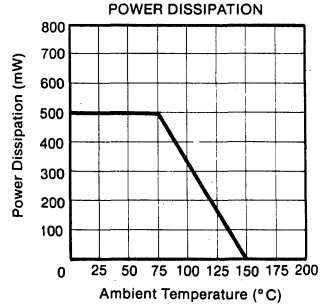
OPEN LOOP RESPONSE



OPEN LOOP GAIN VS SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION



APPLICATIONS

SETTLING TIME

Settling time of an amplifier is defined (see Figure 1) as the total time required, after an input step signal, for the output to "settle" within a specified error band around the final value. This error band is expressed as a percentage of the magnitude of the step transition. A recommended test circuit for settling time is shown in Figure 2. The output error signal appears, attenuated by a factor of two, at point A and may be observed at this point with the aid of an oscilloscope. The diodes act as limiters to prevent overloading the oscilloscope during the fast leading edge of the input signal. All resistors should be 2kΩ or less to eliminate degradation of performance due to stray capacitance. A typical measurement desired is the settling time to 0.01% for a 10-volt step input. This is the time required for the signal at point A to decrease to 0.5mV or less and remain below this level.

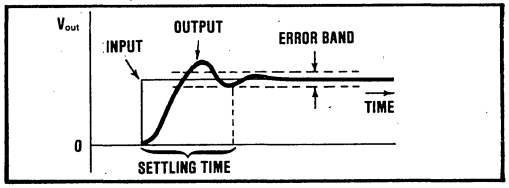


FIGURE 1. Concept of Settling Time.

Settling time for noninverting circuits can also be measured but requires the use of ultra-fast differential amplifier test fixtures. For the 3550 settling time is equal for inverting or noninverting circuits of equal gain.

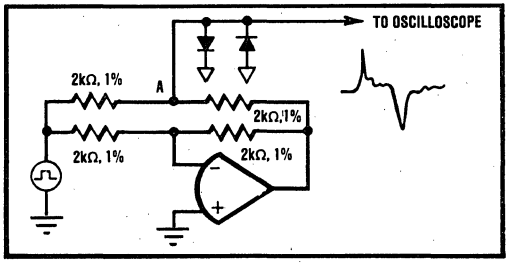


FIGURE 2. Settling Time Test Circuit.

Because settling time is affected by bandwidth which in turn is dependent upon closed-loop gain, the settling time of any operational amplifier will be a function of closed loop gain. Settling Time versus Gain curves illustrate this effect for the 3550 at several levels of settling accuracy.

The 3550 is remarkably tolerant of load capacitance because of its stable, 6dB/octave gain rolloff and low output impedance. Settling Time versus Load Capacitance curves show this characteristic for the unity-gain configuration. For larger values of load capacitance the compensation technique of Figure 3 may be used to optimize the response. The slight negative feedback provided by C_C tends to reduce any ringing at the top of the output voltage waveform without significantly affecting the slew rate. See the Settling Time versus Load Capacitance curves for typcial improvements in settling time.

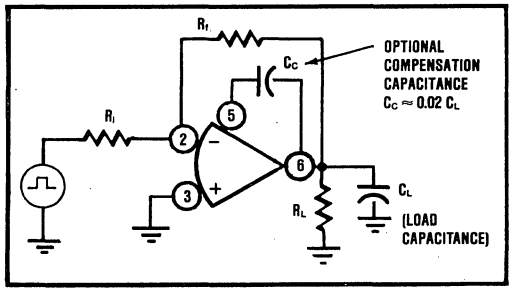


FIGURE 3. Compensation for Load Capacitance.

WIRING RECOMMENDATIONS

In order to fully realize the high frequency performance capabilities of the 3550, proper attention must be given to layout, component selection and grounding. All leads associated with the input and feedback elements should be as short as possible and all connections should be made as close to the amplifier terminals as possible. Input and feedback resistors should be made as small as possible consistent with other circuit constraints. Capacitance from the ouput to noninverting input can cause high frequency oscillations, particularly in high gain circuits operating from large source impedance. Careful layout of wiring or PC board patterns is the only satisfactory way of preventing such problems.

In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 0.001μF ceramic capacitor from pins 7 and 4 to the power supply common.

INPUT AND OUTPUT VOLTAGE RANGE

Although the 3550 is specified for best operation on power supply voltage of ±15VDC, it will operate with minor performance changes over a power supply voltage range of ±5VDC to ±20VDC. Many of the curves show performance of the 3550 when operated from supplies other than ±15VDC.

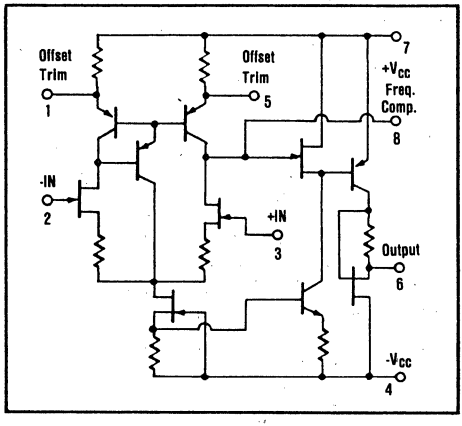
BURR-BROWN®

3551 SERIES

Wideband and Fast-Settling FET OPERATIONAL AMPLIFIERS

FEATURES

- REDUCES WIDEBAND ERRORS
  - 50MHz Gain-bandwidth product (ACL ≥10)
  - 250V/μs slew rate (Cf = 0)
- VERSATILE
  - Single compensation capacitor allows optimum response
  - True differential input
- PRESERVES DC ACCURACY
  - Bias current, 100pA, max
  - Laser-trimmed offset voltage



DESCRIPTION

The 3551 is designed to offer the user versatility in wideband steady state and fast transient applications. The use of a single external compensation capacitor allows the user to optimize frequency response for maximum bandwidth for a variety of closed loop gains and capacitive loads. The amplifier is stable at closed loop gains of greater than 10V/V, with no external compensation and may be stabilized at all gains with the single 10pF compensation capacitor.

In addition to the excellent dynamic response characteristics, the 3551 also has good DC properties. The use of a monolithic FET input stage gives the 3551 very low input bias and offset currents. This is in contrast to the high input currents usually associated with fast amplifiers having bipolar input stages. Also, the input offset voltage and offset voltage drift are low as a result of Burr-Brown's laser-trimming techniques.

Unlike many wideband and fast settling amplifiers, the 3551 has a true differential input. This means it can provide its excellent wideband response in the inverting, noninverting, current-to-voltage and difference configurations.

The 3551 is an excellent choice for applications such as fast D/A and A/D converters, high speed comparators and fast sampling circuits, to name just a few.

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SPECIFICATIONS

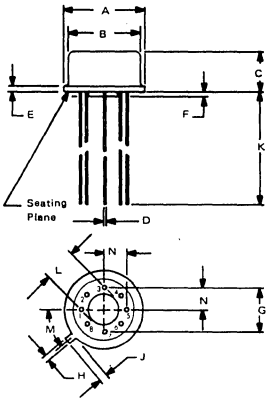
ELECTRICAL

Specifications typical at 25°C and ±15VDC Power Supply unless otherwise noted.

MODELS	3551J	3551S
OPEN LOOP GAIN, DC		
No Load	100dB	
1kΩ, Load min	88dB	
RATED OUTPUT		
Voltage, min	±10V	
Current, min	±10mA	
Open Loop Output Resistance	100Ω at 1MHz	
DYNAMIC RESPONSE		
Gain-Bandwidth Product		
Gain = 1000	50MHz	
Gain = 10	50MHz	
Slew Rate (C_f = 0)	250V/μsec	
INPUT OFFSET VOLTAGE		
Initial Offset, 25°C, max	±1mV	
vs. Temp(1)	±50μV/°C	
vs. Supply Voltage	±500μV/V	
vs. Time	±100μV/mo	
INPUT BIAS CURRENT		
Initial Bias, 25°C, max	-400pA (after full warm-up)	
vs. Temperature	doubles every 10°C	
vs. Supply Voltage	±1pA/V	
INPUT DIFFERENCE CURRENT		
Initial Difference, 25°C	±40pA	
INPUT IMPEDANCE		
Differential	$10^{11}\Omega$ || 3pF	
Common-mode	$10^{11}\Omega$ || 3pF	
INPUT NOISE		
Voltage, 0.01Hz to 10Hz, p-p	20μV	
Voltage, 10Hz to 10kHz, rms	4μV	
Current, 0.01Hz to 10Hz, p-p	0.2pA	
Current, 10Hz to 10kHz, rms	1.5pA	
INPUT VOLTAGE RANGE		
Common-mode Voltage	±(|V_{CC}|-5)V	
Common-mode Rejection	70dB at +5V, -10V	
Max. Safe Input Voltage	±Supply	
POWER SUPPLY		
Rated Voltage	±15VDC	
Voltage Range, derated	±5VDC to ±20VDC	
Current, quiescent(1)	11mA (15mA max)	
TEMPERATURE RANGE		
Specification	0°C to +70°C	-55°C to +125°C
Operating	-55°C to +125°C	-55°C to +125°C
Storage	-65°C to +150°C	

NOTE:
1. The use of a finned heat sink is recommended.

MECHANICAL TO-99



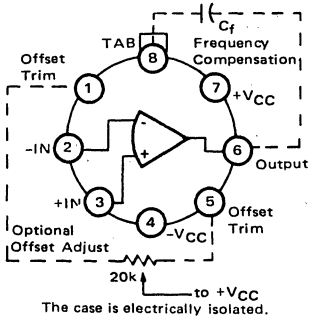
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM

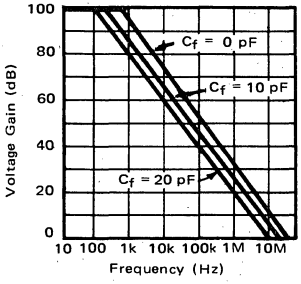


The case is electrically isolated.

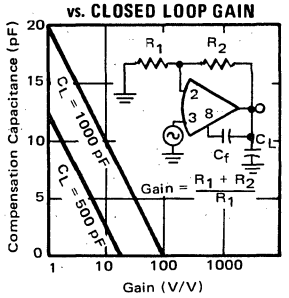
TYPICAL PERFORMANCE CURVES

$T_A = 25^oC$ $V_S = \pm 15$ VDC unless otherwise indicated.

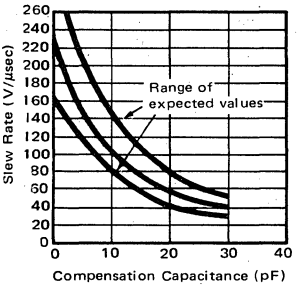
OPEN LOOP RESPONSE



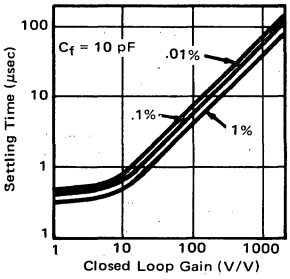
RECOMMENDED VALUES OF FREQUENCY COMPENSATION CAPACITANCE vs. CLOSED LOOP GAIN



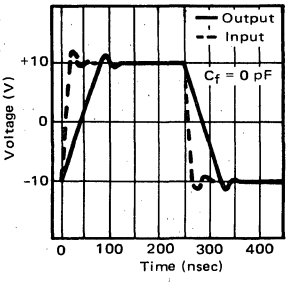
SLEW RATE vs. COMPENSATION CAPACITANCE



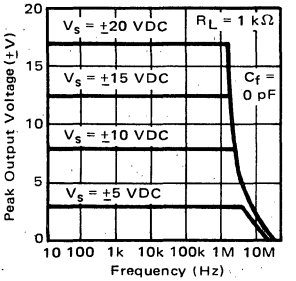
SETTLING TIME vs. CLOSED LOOP GAIN



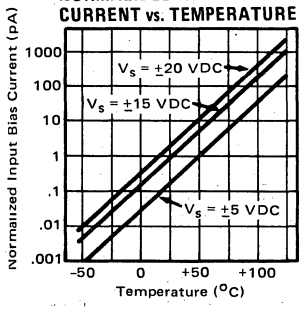
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



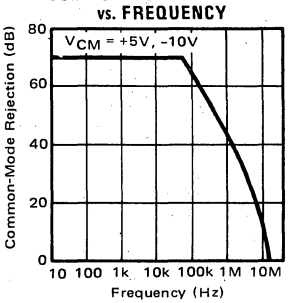
OUTPUT VOLTAGE vs. FREQUENCY



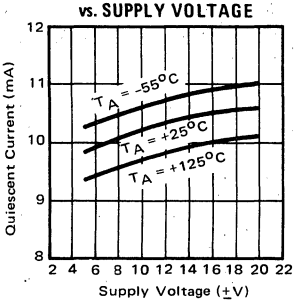
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



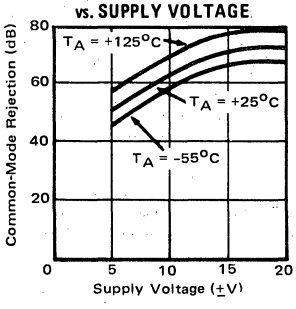
COMMON-MODE REJECTION vs. FREQUENCY



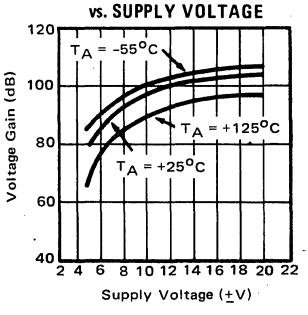
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



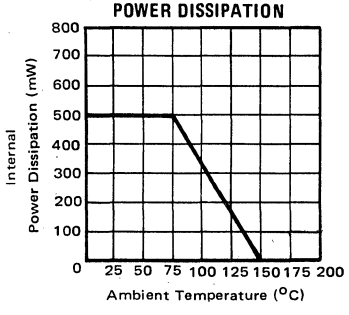
COMMON-MODE REJECTION vs. SUPPLY VOLTAGE



OPEN LOOP GAIN vs. SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION



APPLICATIONS

WIRING RECOMMENDATIONS

In order to fully realize the high frequency performance capabilities of the 3551, proper attention must be given to layout, component selection and grounding. All leads associated with the input and feedback elements should be as short as possible and all connections should be made as close to the amplifier terminals as possible. Input and feedback resistors should be made as small as possible consistent with other circuit constraints. Capacitance from the output to non-inverting input can cause high frequency oscillations, particularly in high gain circuits operating from large source impedances. Careful layout of wiring or PC board patterns is the only satisfactory way of preventing such problems.

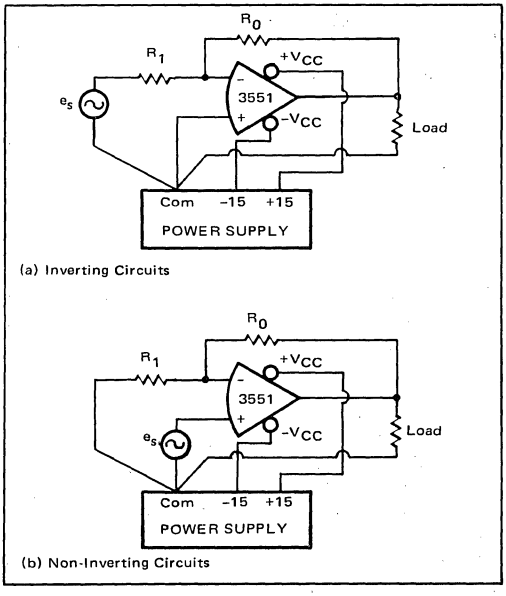


FIGURE 1. Proper Grounding Methods.

Provision for phase compensation should always be made on the PC board even if initial calculations and breadboarding may indicate that none is needed.

In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10 μf tantalum capacitor in parallel with a 0.001 μf ceramic capacitor from pins 7 and 4 to the power supply common.

INPUT AND OUTPUT VOLTAGE RANGE

Although the 3551 is specified for best operation on power supply voltage of ±15 VDC, it will operate with minor performance changes over a power supply voltage range of ±5 VDC to ±20 VDC. Many of the performance curves show performance of the 3551 when operated from supplies other than ±15 VDC.

INPUT/OUTPUT PROTECTION

All of the amplifiers listed in the specification table are designed to withstand input voltages as high as the supply voltage, without damage to the amplifier. Thus, inputs may be subjected to either supply voltage, in any combination, without damage.

Output stages are internally current limited and will withstand short-circuit-to-ground conditions. However, application of nonzero potential to the output pin may cause permanent damage and should be prevented by the proper precautions.

SETTLING TIME

Settling time of an amplifier is defined as the total time required, after an input step signal, for the output to "settle" within a specified error band around the final value. This error band is expressed as a percentage of the magnitude of the step transition.

Because settling time is affected by bandwidth which in turn is dependent upon closed loop gain, the settling time of any operational amplifier will be a function of closed loop gain. Settling time vs. gain curves illustrate this effect for the 3551 at several levels of settling accuracy.

BURR-BROWN®

3553

Wideband - Fast-Slewing BUFFER AMPLIFIER

FEATURES

- GAIN = .99V/V
- OUTPUT CURRENT, ±200mA
- BANDWIDTH, 300MHz
- SLEW RATE, 2000V/μsec
- ELECTRICALLY ISOLATED CASE
- EXTENDS OP AMP DRIVING CAPABILITY WHILE PRESERVING BANDWIDTH & SETTLING TIME

DESCRIPTION

The 3553 is a unity-gain amplifier designed to be used either as a signal buffer, or as the power output stage for an operational amplifier. Because of its wideband response (300MHz, -3dB bandwidth) and fast slewing capability (2000V/μsec) the 3553 is capable of following very fast signals. When used inside the feedback loop of an operational amplifier, these high speed characteristics are essential in order to preserve the performance and stability of the feedback amplifier circuit.

With its ±200mA of output current capability, the 3553 is capable of driving a signal of ±10V into a 50Ω load. This power capability, coupled with its extremely high speed and wide bandwidth, makes the 3553 ideally suited for line driving applications where fast pulses or wideband signals are involved.

In addition to its fast/wideband characteristics and high output current, the 3553 has low input offset voltage and drift. This adds to its versatility, particularly in stand-alone buffer amplifier applications.

The 3553 is packaged in a reliable hermetically sealed TO-3 package for environmental ruggedness. The metal case is completely electrically isolated. This simplifies mounting and reduces cost since the need for insulating spacers and bushings is eliminated.

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SPECIFICATIONS

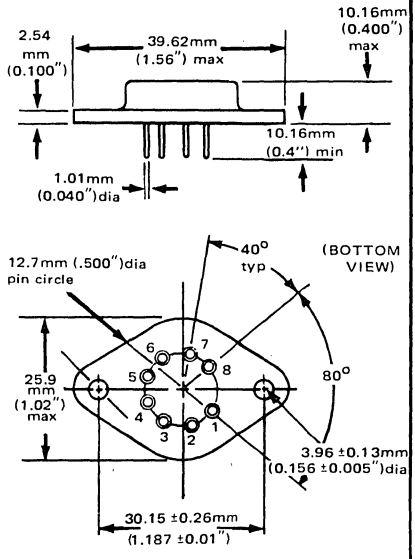
Specifications are typical at +25°C Case Temperature and ± 15 VDC power supply unless otherwise noted.

ELECTRICAL

MODEL	3553AM
GAIN, DC	
No Load	0.98 V/V
50 Ω Load, min	0.92 V/V
RATED OUTPUT	
Voltage, min	±10 V
Current, min	±200 mA
Output Resistance	1 Ω
DYNAMIC RESPONSE	
Slew Rate, min	2000 V/μsec
Full Power Bandwidth, min	32 MHz
Small Signal -3dB Bandwidth	300 MHz
Settling Time to 1%	7.2 nsec
to .01%	14.5 nsec
INPUT PARAMETERS	
Input Voltage, linear range	±10 V
Input Voltage, absolute, max	±Supply Voltage
Input Impedance	10^{11} Ω
Input Bias Current @ +25°C (doubles/+10°C)	-200 pA
OUTPUT OFFSET VOLTAGE	
Initial Offset @ +25°C, max	±50 mV
vs. Temperature (average) -25°C to +85°C	±300 μV/°C
POWER SUPPLY	
Rated Voltage	±15 VDC
Voltage Range, derated	±5 VDC to ±20 VDC
Current, Quiescent, max	±80 mA
typ	±50 mA
TEMPERATURE RANGE (Case)	
Specification	-25°C to +85°C
Operation (derate above +120°C Case)	-55°C to +125°C
Storage	-65°C to +150°C
θ_{JC} Thermal Resistance, junction to case	6°C/W
θ_{JA} Thermal Resistance, junction to ambient	33°C/W

MECHANICAL

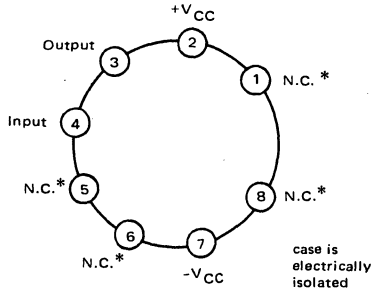
M PACKAGE (TO-3)



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM

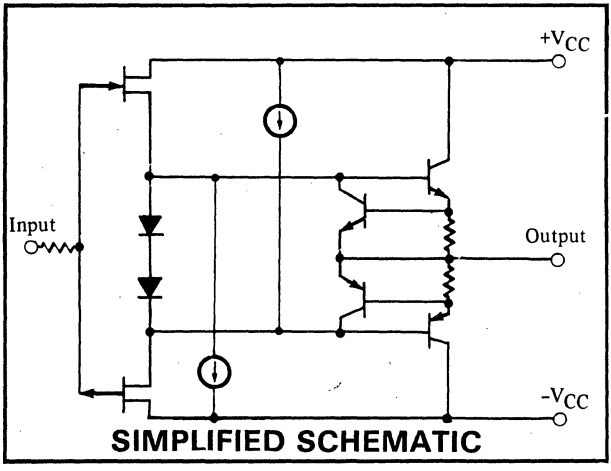
(TOP VIEW)



*No internal connection

CONNECTOR: 0803MC

HEATSINKS: 0803HS 12°C/W
0804HS 4.2°C/W
0805HS 3°C/W

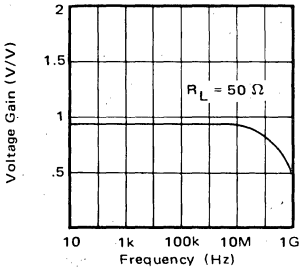


SIMPLIFIED SCHEMATIC

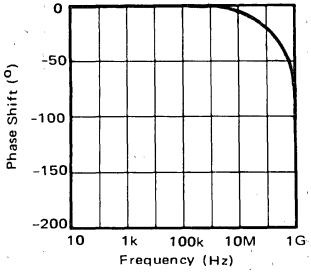
TYPICAL PERFORMANCE CURVES

Typical at 25°C and rated supply voltage unless otherwise noted.

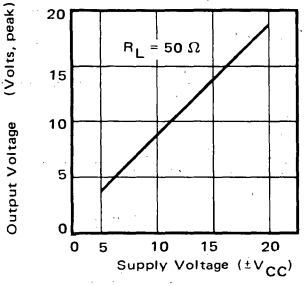
SMALL SIGNAL FREQUENCY RESPONSE



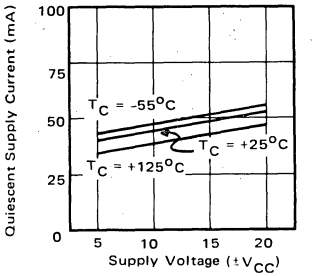
PHASE SHIFT vs FREQUENCY



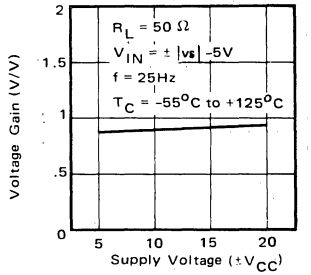
OUTPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



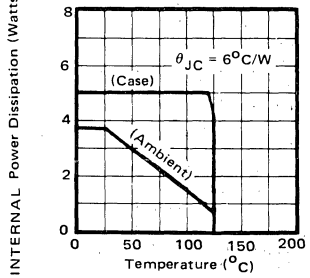
QUIESCENT POWER SUPPLY CURRENT vs SUPPLY VOLTAGE



GAIN vs SUPPLY VOLTAGE



POWER DISSIPATION



APPLICATION INFORMATION

BOOSTER AMPLIFIER

One of the primary applications for the 3553 is that of a current booster for an operational amplifier. The circuit of Figure 1 is typical of such applications. Note that the 3553 is used inside the feedback loop and becomes, effectively, the output stage of the composite amplifier. Because the 3553 has unity voltage gain, wideband response, fast slewing rate, and very little phase delay, the dynamic response of the operational amplifier is virtually unaffected by the addition of the booster.

The already low offset voltage of the 3553 is effectively reduced by a factor equal to the open loop gain of the operational amplifier and becomes a negligible factor in total offset error of the circuit.

Input impedance of the 3553 is extremely high, thus requiring almost no drive current from the operational amplifier. On the other hand, the presence of the 3553 in the circuit increases the output current capability to ±200 mA, drastically lowers the output impedance of the loop, and permits the driving of low impedance loads such as a terminated 50Ω coaxial line.

Capacitive loads, often a source of instability and oscillations in operational amplifier circuits, are buffered by the presence of the 3553. In driving heavily capacitive loads the slew rate of the 3553 will be seen to decrease. This is due simply to the large currents required by fast voltage slewing in a capacitive load,

$$I_c = C_{load} \frac{dV}{dt}.$$

The internal current limit of the 3553 (approximately 600 mA) places a limit on the slewing rate under such conditions.

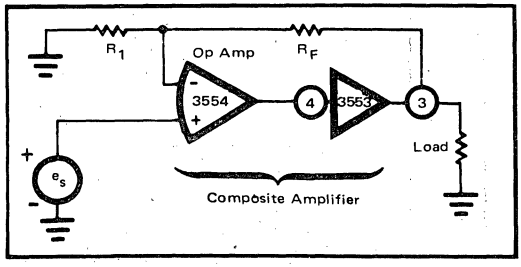


FIGURE 1. Model 3553 as a power booster.

BUFFER AMPLIFIER

The 3553 may also be used, as shown in Figure 2, as a unity gain buffer amplifier. No operational amplifier is required in this mode of operation. Since the 3553 is then operated without feedback, it's offset voltage and drift are translated to the output. While the gain is not precisely unity in this mode, the accuracy is adequate for many applications.

INPUT/OUTPUT PROTECTION

The output stage of the 3553 is current limited at approximately 600mA. This will provide a measure of output short circuit protection for the amplifier for a period of time as determined by the heatsinking used, the amplifier's thermal resistance, the ambient temperature, etc. The amplifier's output stage transistors should not be allowed to exceed 150°C (175°C absolute max).

The input stage is designed to allow the application of either supply voltage without damage to the amplifier.

POWER DISSIPATION

The power dissipation capability of the 3553 varies with ambient temperature and with the type of heat sink used. A heat sink may be used to increase the dissipation capability or to achieve a given dissipation capability at higher temperature. The power derating curve is given in the Typical Performance Curves.

WIRING RECOMMENDATIONS

No special wiring techniques are necessary with the 3553. However, it is recommended, as a good engineering practice, that the power supply lines be bypassed to common at a point near the amplifier. (A 1.0μF electrolytic in parallel with a 1000pF ceramic is recommended.) If the 3553 is used with a wideband operational amplifier, all leads must be kept as short as possible to minimize stray capacitance and unwanted feedback paths.

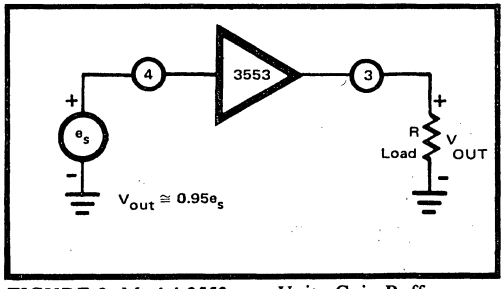


FIGURE 2. Model 3553 as a Unity Gain Buffer.

BURR-BROWN®

3554

Wideband - Fast-Settling OPERATIONAL AMPLIFIER

FEATURES

- SLEW RATE, 1000Vusec
- FAST SETTLING, 150nsec, max (to ±.05%)
- GAIN-BANDWIDTH PRODUCT, 1.7GHz
- FULL DIFFERENTIAL INPUT

APPLICATIONS

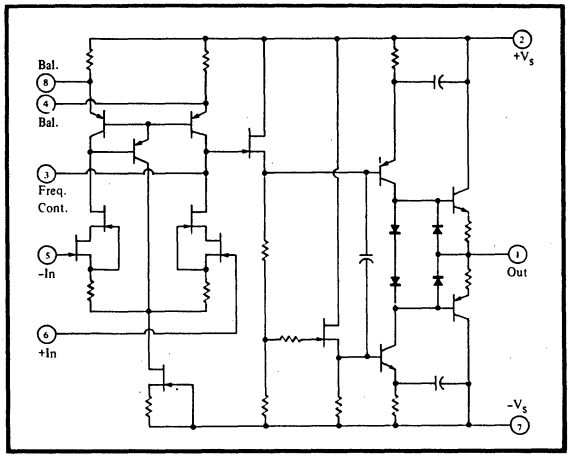
- PULSE AMPLIFIERS
- TEST EQUIPMENT
- WAVEFORM GENERATORS
- FAST D/A CONVERTERS

DESCRIPTION

The 3554 is a full differential input, wideband operational amplifier. It is designed specifically for the amplification or conditioning of wideband data signals and fast pulses. It features an unbeatable combination of gain-bandwidth product, settling time and slew rate. It uses hybrid construction. On the beryllia substrate are matched input FETs, thin-film resistors and high speed silicon dice. Active laser trimming and complete testing provide superior performance at a very moderate price.

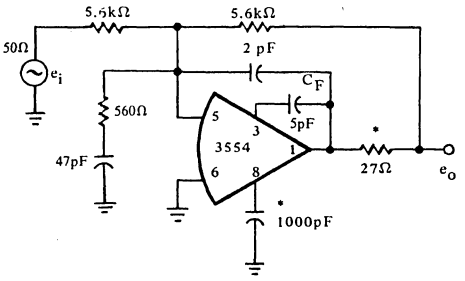
The 3554 has a slew rate of 1000V/μsec and will output ±10V and ±100mA. When used as a fast settling amplifier, the 3554 will settle to ±0.05% of the final value within 150nsec. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate or settling time in the particular application.

The 3554 is reliable and rugged and addresses almost any application when speed and bandwidth are serious considerations. It is particularly a good choice for use in fast settling circuits, fast D/A converters, multiplexer buffers, comparators, waveform generators, integrators, and fast current amplifiers. It is available in several grades to allow selection of just the performance required.

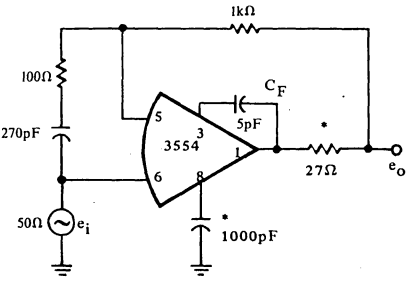


International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

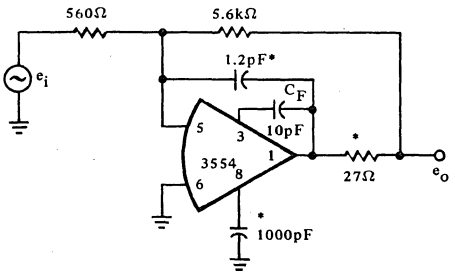
TYPICAL CIRCUITS



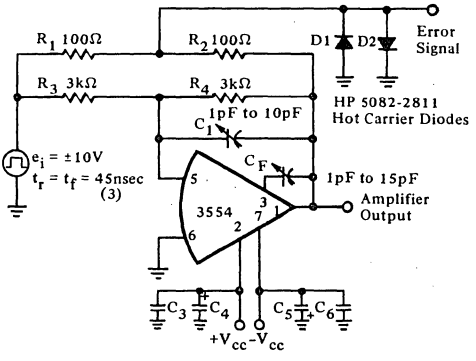
X1 Inverter



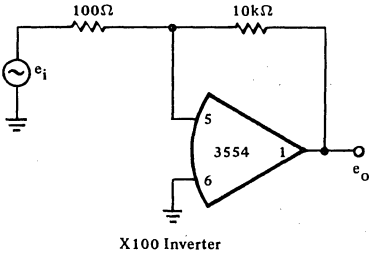
X1 Noninverter



X10 Inverter

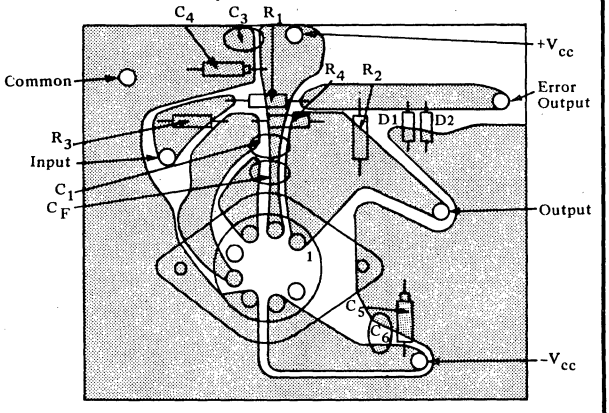


Settling Time Test Circuit Schematic



X100 Inverter

View from Component Side.
Shaded area is the pattern side conductor.



Settling Time Test Circuit Layout

NOTES:
1. These circuits are optimized for driving large capacitive loads (to 470pF).
2. The 3554 is stable at gains of greater than 55 ($C_L \leq$ 100pF) without any frequency compensation.
3. 45nsec is optimum. Very fast rise times (10-20nsec) may saturate the input stage causing less than optimum settling time performance.

*Indicates component that may be eliminated when large capacitive loads are not being driven by the device.

ELECTRICAL SPECIFICATIONS

At T_{CASE} = 25°C and ±15VDC, unless otherwise noted.

PARAMETERS	CONDITIONS	3554AM			3554BM			3554SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN, DC					*	*	*	*	*	*	
No Load		100	106								dB
Rated Load	R_L = 100Ω	90	96								dB
RATED OUTPUT					*	*	*	*	*	*	
Voltage	I_O = ±100mA	±10	±11								V
Current	V_O = ±10V	±100	±125								mA
Output Resistance, open loop	f = 10MHz		20								•Ω
DYNAMIC RESPONSE					*	*	*	*	*	*	
Bandwidth (0dB, small signal)	C_F = 0	70†	90								MHz
Gain-bandwidth Product	C_F = 0, G = 10 V/V	150	225								MHz
	C_F = 0, G = 100 V/V	425	725								MHz
	C_F = 0, G = 1000 V/V	1000	1700								MHz
Full Power Bandwidth	C_F = 0, V_o = 20Vp-p, R_L = 100Ω	16	19								MHz
Slew Rate	C_F = 0, V_o = 20Vp-p, R_L = 100Ω	1000	1200								V/µsec
Settling Time to ±1%	A = 1		60								nsec
to ±.1%	A = 1		120								nsec
to ±.05%	A = 1		140	150							nsec
to ±.01%	A = 1		200	250							nsec
INPUT OFFSET VOLTAGE											
Initial offset, T_A = 25°C			±0.5	±2		±0.2	±1		±0.2	±1	mV
vs. Temp (T_A = -25°C to +85°C)			±20	±50		±8	±15				µV/°C
vs. Temp (T_A = -55°C to +125°C)									±12	±25	µV/°C
vs. Supply Voltage			±80	±300		*	*		*	*	µV/V
INPUT BIAS CURRENT					*	*	*	*	*	*	
Initial bias, 25°C		0	-10	-50							pA
vs. Temp			**								
vs. Supply Voltage			±1								pA/V
INPUT DIFFERENCE CURRENT					*	*	*	*	*	*	
Initial difference, 25°C			±2	±10							pA
INPUT IMPEDANCE						*			*		
Differential			10^{11} ‖ 2								Ω ‖ pF
Common-mode			10^{11} ‖ 2								Ω ‖ pF
INPUT NOISE					*	*	*	*	*	*	
Voltage, f_o = 1Hz	R_S = 100Ω		125								nV/√Hz
f_o = 10Hz	R_S = 100Ω		50								nV/√Hz
f_o = 100Hz	R_S = 100Ω		25								nV/√Hz
f_o = 1kHz	R_S = 100Ω		15								nV/√Hz
f_o = 10kHz	R_S = 100Ω		10								nV/√Hz
f_o = 100kHz	R_S = 100Ω		8								nV/√Hz
f_o = 1MHz	R_S = 100Ω		7								nV/√Hz
f_B = .3Hz to 10Hz	R_S = 100Ω		2								µV, p-p
f_B = 10Hz to 1MHz	R_S = 100Ω		8								µV, rms
Current, f_B = .3Hz to 10Hz	R_S = 100Ω		45								fA, p-p
f_B = 10Hz to 1MHz	R_S = 100Ω		2								pA, rms
INPUT VOLTAGE RANGE					*	*	*	*	*	*	
Common-mode Voltage Range	Linear Operation		±(V_{CC}-4)								V
Common-mode Rejection	f = DC, V_{CM} = +7V, -10V	44	78								dB
Max. Safe Input Voltage			±Supply								V
POWER SUPPLY					*	*	*	*	*	*	
Rated Voltage			±15								VDC
Voltage Range, derated performance		±5		±18							VDC
Current, quiescent		±17	±35	±45							mA
TEMPERATURE RANGE (ambient)											
Specification		-25		+85	-25		+85	-55		+125	°C
Operating, derated performance		-55		+125	-55		+125	-55		+125	°C
Storage		-65		+150	-65		+150	-65		+150	°C
θ junction-case			15			15			15		°C/W
θ junction-ambient			45			45			45		°C/W

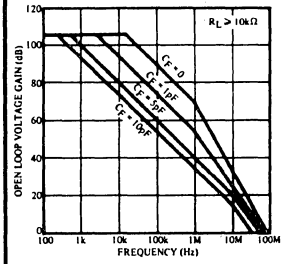
* Specifications same as for 3554AM

** Doubles every +10°C

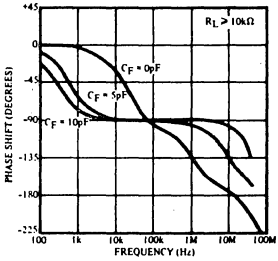
TYPICAL PERFORMANCE CURVES

at $T_C = +25^oC$ and ±15VDC unless otherwise noted.

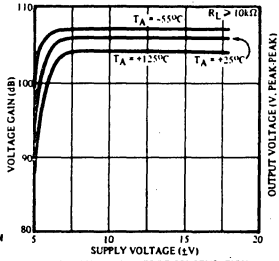
OPEN LOOP RESPONSE



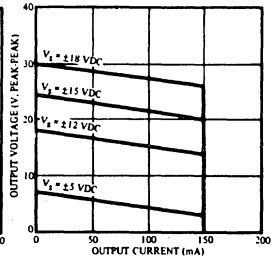
OPEN LOOP RESPONSE



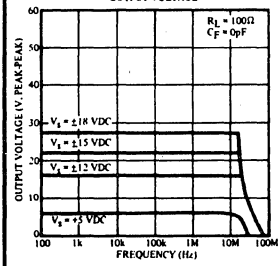
VOLTAGE GAIN



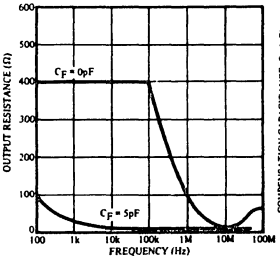
OUTPUT VOLTAGE VS OUTPUT CURRENT



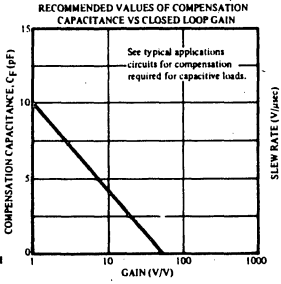
OUTPUT VOLTAGE



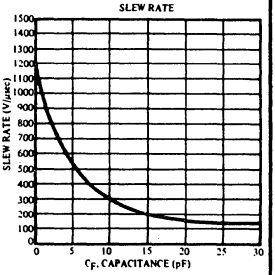
OPEN LOOP OUTPUT RESISTANCE VS FREQUENCY



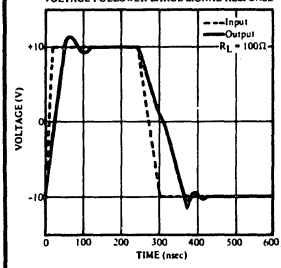
RECOMMENDED VALUES OF COMPENSATION CAPACITANCE VS CLOSED LOOP GAIN



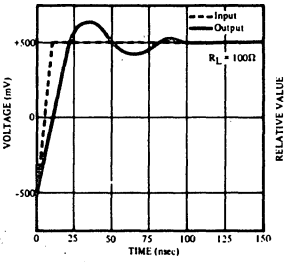
SLEW RATE



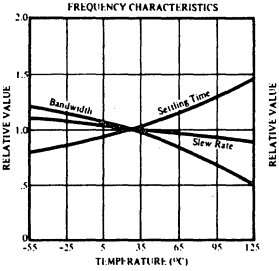
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



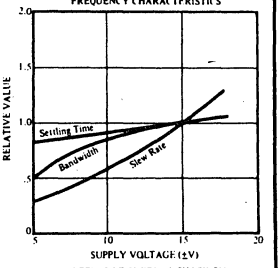
VOLTAGE FOLLOWER TRANSIENT RESPONSE



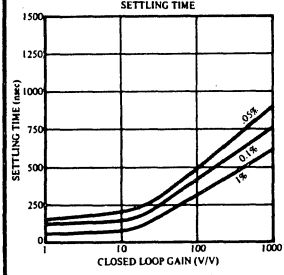
FREQUENCY CHARACTERISTICS



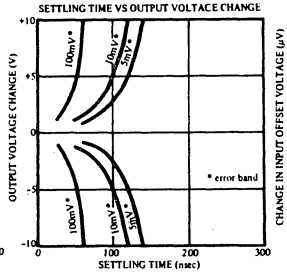
FREQUENCY CHARACTERISTICS



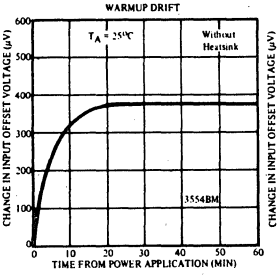
SETTLING TIME



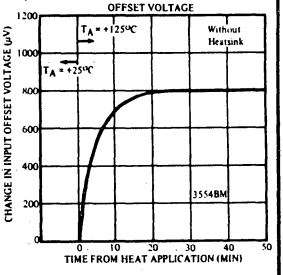
SETTLING TIME VS OUTPUT VOLTAGE CHANGE



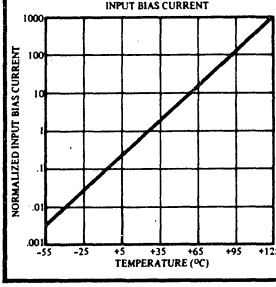
WARMUP DRIFT



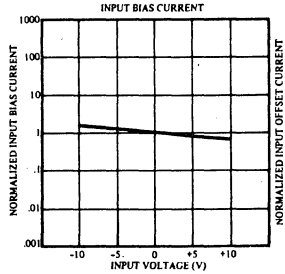
EFFECT OF THERMAL SHOCK ON OFFSET VOLTAGE



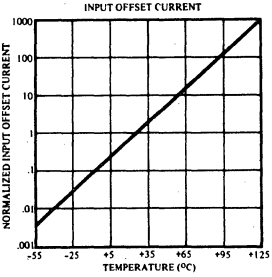
INPUT BIAS CURRENT



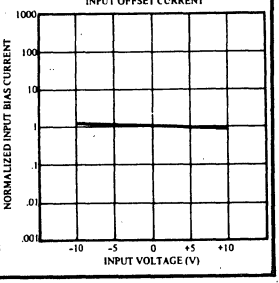
INPUT BIAS CURRENT

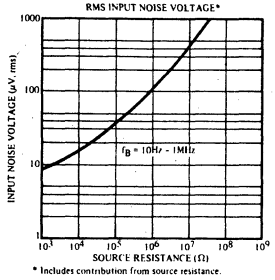


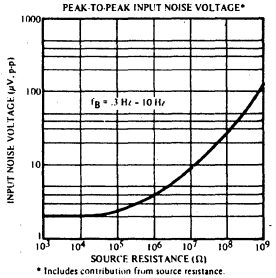
INPUT OFFSET CURRENT

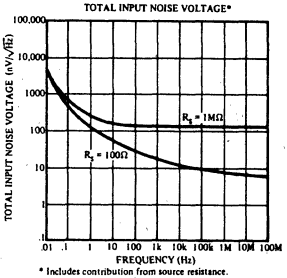


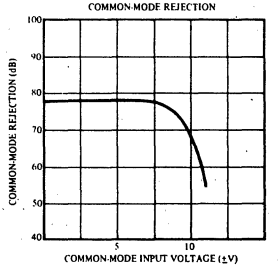
INPUT OFFSET CURRENT

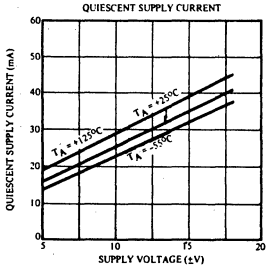


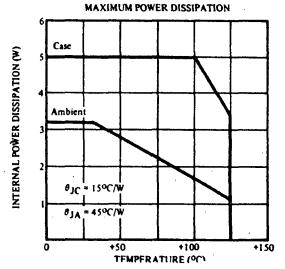




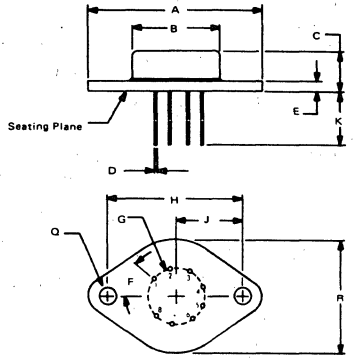








MECHANICAL

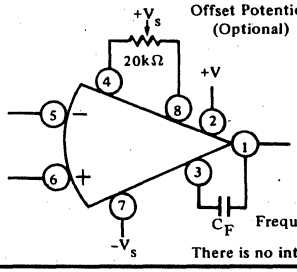


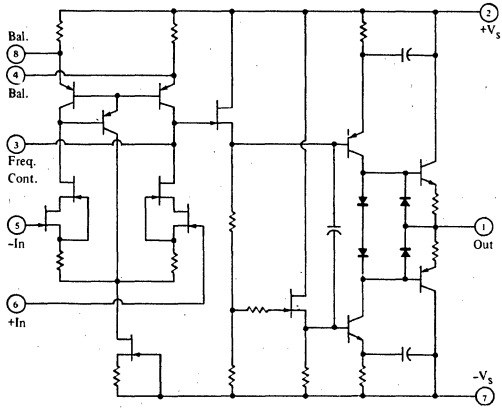
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

NOTE
Leads in true position within .010" (.25mm) R @ MMC at seating plane
Pin numbers shown for reference only
Numbers may not be marked on package

AMPLIFIER CONNECTIONS





APPLICATIONS INFORMATION

WIRING PRECAUTIONS

The 3554 is a wideband, high frequency operational amplifier that has a gain-bandwidth product exceeding 1 Gigahertz. The full performance capability of this amplifier will be realized by observing a few wiring precautions and high frequency techniques.

Of all the wiring precautions, grounding is the most important and is described in an individual section. The mechanical circuit layout also is very important. All circuit element leads should be as short as possible. All printed circuit board conductors should be wide to provide low resistance, low inductance connections and should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitances should be minimized especially at high impedance nodes such as the input terminals of the amplifier. Pin 5, the inverting input, is especially sensitive and all associated connections must be short. Stray signal coupling from the output to the input or to pin 8 should be minimized. A recommended printed circuit board layout is shown with the "Typical Circuits." It also may be used for test purposes as described below.

When designing high frequency circuits low resistor values should be used; resistor values less than 5.6kΩ are recommended. This practice will give the best circuit performance as the time constants formed with the circuit capacitances will not limit the performance of the amplifier.

GROUNDING

As with all high frequency circuits a ground plane and good grounding techniques should be used. The ground plane should connect all areas of the pattern side of the printed circuit board that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pick up. An example of an adequate ground plane and good high frequency techniques is the Settling Time Test Circuit Layout shown with the "Typical Circuits."

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A combination of a 1μF tantalum capacitor in parallel with a 470pF ceramic capacitor is a suitable bypass.

In inverting applications it is recommended that pin 6, the noninverting input, be grounded rather than being connected to a bias current compensating resistor. This assures a good signal ground at the noninverting input. A slight offset error will result; however, because the resistor values normally used in high frequency circuits are small and the bias current is small, the offset error will be minimal.

If point-to-point wiring is used or a ground plane is not, single point grounding should be used. The input signal return and the load signal return and the power supply common should all be connected at the same physical point. This will eliminate any common current paths or ground loops which could cause signal modulation or unwanted feedback.

It is recommended that the case of the 3554 not be grounded during use (it may, if desired). A grounded case will add a slight capacitance to each pin. To an already functional circuit, grounding the case will probably require slight compensation readjustment and the compensation capacitor values will be slightly different from those recommended in the typical performance curves. There is no internal connection to the case.

Proper grounding is the single most important aspect of high frequency circuitry.

GUARDING

The input terminals of the 3554 may be surrounded by a guard ring to divert leakage currents from the input terminals. This technique is particularly important in low bias current and high input impedance applications. The guard, a conductive path that completely surrounds the two amplifier inputs, should be connected to a low impedance point which is at the input signal potential. It blocks unwanted printed circuit board leakage currents from reaching the input terminals. The guard also will reduce stray signal coupling to the input.

In high frequency applications guarding may not be desirable as it increases the input capacitance and can degrade performance. The effects of input capacitance, however, can be compensated by a small capacitor placed across the feedback resistor. This is described further in the following section.

COMPENSATION

The 3554 uses external frequency compensation so that the user may optimize the bandwidth or slew rate or settling time for his particular application. Several typical performance curves are provided to aid in the selection of the correct compensation capacitance value. In addition several typical circuits show recommended compensation in different applications.

The primary compensation capacitor, C_F, is connected between pins 1 and 3. As the performance curves show, larger closed-loop gain configurations require less capacitance and an improved gain-bandwidth product will be realized. Note that no compensation capacitor is required for closed-loop gains above 55V/V and when the load capacitance is less than 100pF.

When driving large capacitive loads, 470pF and greater,

an additional capacitor, C_8, is connected between pin 8 and ground. This capacitor is typically 1000pF. It is particularly necessary in low closed loop voltage gain configurations. The value may be varied to optimize performance and will depend upon the load capacitance value. In addition, the performance may be optimized by connecting a small resistance in series with the output and a small capacitor from pin 1 to 5. See the "Typical Circuits" for the X10 Inverter.

The flat high frequency response of the 3554 may be preserved and any high frequency peaking avoided by connecting a small capacitor in parallel with the feedback resistor. This capacitor will compensate for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. Using small resistor values will keep the break frequency of this zero sufficiently high, avoiding peaking and preserving the phase margin. Resistor values less than 5.6kΩ are recommended. The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. It will typically be 2pF for a clean layout using low resistances (1kΩ) and up to 10pF for circuits using larger resistances.

SETTLING TIME

Settling time is truly a complete dynamic measure of the 3554's total performance. It includes the slew rate time, a large signal dynamic parameter, and the time to accurately reach the final value, a small signal parameter that is a function of bandwidth and open loop-gain. The settling time may be optimized for the particular application by selection of the closed-loop gain and the compensation capacitance. The best settling time is observed in low closed-loop gain circuits. A performance curve shows the settling time to three different error bands.

Settling time is defined as the total time required, from the signal input step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition.

SLEW RATE

Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed-loop gain or the bandwidth, per se. It is dependent upon compensation. Decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve. Stray capacitances may appear to the amplifier as compensation. To avoid limiting the slew rate performance, stray capacitances should be minimized.

CAPACITIVE LOADS

The 3554 will drive large capacitive loads (up to 1000pF) when properly compensated. See the section on "Compensation." The effect of a capacitive load is to decrease the phase margin of the amplifier. With compensation the amplifier will provide stable operation even with large capacitive loads.

The 3554 is particularly well suited for driving 50Ω loads connected via coaxial cables due to its ±100mA output drive capability. The capacitance of the coaxial cable, 29pF/foot of length for RG-58, does not load the amplifier when the coaxial cable or transmission line is terminated in the characteristic impedance of the transmission line.

OFFSET VOLTAGE ADJUSTMENT

The offset voltage of the 3554 may be adjusted to zero by connecting a 20kΩ linear potentiometer between pins 4 and 8 with the wiper connected to the positive supply. A small, noninductive potentiometer is recommended. The leads connecting the potentiometer to pins 4 and 8 should be extremely short to avoid stray capacitance and stray signal pickup. Stray coupling from the output, pin 1, to pin 4 (negative feedback) or to pin 8 (positive feedback) should be avoided or oscillation may occur.

The potentiometer is optional and may be omitted when the guaranteed offset voltage is considered sufficiently low for the particular application.

For each microvolt of offset voltage adjusted, the offset voltage temperature drift will change by ±0.004μV/°C.

HEAT SINKING

The 3554 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler operating temperatures. At extreme temperature and under full load conditions a heat sink will be necessary as indicated in the "Maximum Power Dissipation" curve. A heat sink with 8 holes for the 8 amplifier pins should be used. Burr-Brown has heat sinks available in three sizes - 3°C/W, 4.2°C/W and 12°C/W. A separate product data sheet is available upon request.

When heat sinking the 3554, it is recommended that the heat sink be connected to the amplifier case and the combination not connected to the ground plane. For a single-sided printed circuit board, the heat sink may be mounted between the 3554 and the nonconductive side of the PC board, and insulating washers, etc., will not be required. The addition of a heat sink to an already functional circuit will probably require slight compensation readjustment for optimum performance due to the change in stray capacitances. The added stray capacitance from the heat sink to each pin will depend on the thickness and type of heat sink used.

SHORT CIRCUIT PROTECTION

The 3554 is short circuit protected for continuous output shorts to common. Output shorts to either supply will destroy the device, even for momentary connections. Output shorts to other potential sources are not recommended as they may cause permanent damage.

TESTING

The 3554 may be tested in conventional operational amplifier test circuits; however, to realize the full performance capabilities of the 3554, the test fixture must not limit the full dynamic performance capability of the amplifier. High frequency techniques must be employed. The most critical dynamic test is for settling time. The 3554 Settling Time Test Circuit Schematic and a test circuit layout is shown with the "Typical Circuits." The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. The layout exemplifies the high frequency considerations that must be observed. The layout also may be used as a guide for other test circuits. Good grounding, truly square drive signals, minimum stray coupling and small physical size are important.

Every 3554 is thoroughly tested prior to shipment assuring the user that all parameters equal or exceed their specifications.

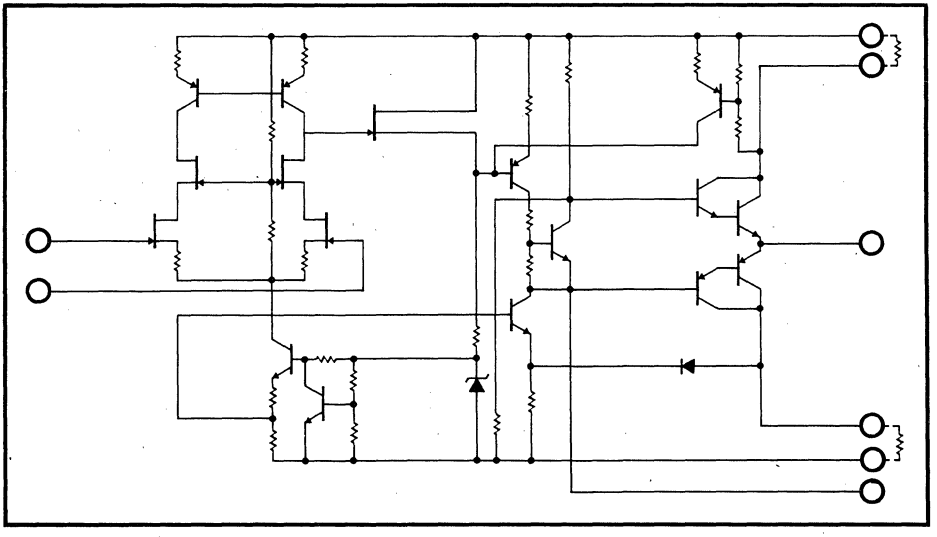
BURR-BROWN®

3571
3572

High Current — High Power OPERATIONAL AMPLIFIERS

FEATURES

- HIGH CURRENT
  Up to 5A Peak, 2A Continuous
- EASY TO USE
  Adjustable Current Limits
  Electrically Isolated Case
  Small Size — 8-Pin TO-3 Package
- HIGH VOLTAGE
  Up to 70V p-p Output
- SELF-PROTECTED
  Self-Contained Automatic Thermal Sensing and Shutdown
- HIGH POWER
  Delivers up to 70W to Load



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DESCRIPTION

The 3571AM and 3572AM are high output current integrated circuit operational amplifiers. Their performance, ease of use and compact size make them ideal to use in a variety of high current applications. They are especially well suited for driving permanent magnet DC servo and torque motors.

The equivalent circuit for the 3571AM and 3572AM is shown in Figure 1. The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The high input impedance provides negligible source impedance loading errors when the noninverting circuit configuration is used. The low bias currents minimize offset errors when large values of source and feedback resistors are used.

The input offset voltage at 25°C and the input offset voltage drift versus temperature are compensated by state-of-the-art laser trimming techniques. The offset voltage is low enough so that trimming will not be required in most applications. The excellent input characteristics and the high gain available mean that the use of a preamplifier, sometimes required with other servo type amplifiers, will not be necessary with the 3571AM and 3572AM.

The output stage is a class AB design which provides low distortion and minimizes quiescent current drain. The output circuitry provides for external current limiting resistors for both positive and negative output currents. This allows the user to select the current limit value suited to his particular application. This is especially desirable for driving permanent magnet motors where the high current seen during direction reversal (plugging) can demagnetize the motor.

The 3571AM and 3572AM have been designed to operate over a relatively wide supply range (±15VDC to ±40VDC) while still maintaining the high output current capability. This allows the user a wide range for the selection of the proper output voltage and current and makes the amplifiers useful for many different types of loads.

The output circuit has a unique protection feature which is practical only in integrated circuit amplifiers - self-contained automatic thermal-sensing and shut-off circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the amplifiers biasing network when the temperature reaches 150°C. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases. The output current may remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal load condition is removed.

Internal thermal protection removes some of the constraints of power derating for abnormal operating conditions. The amplifier will protect itself for many conditions of excess power dissipation (see Power Derating Curve). This allows the use of a smaller heat sink to protect against abnormal output conditions since the amplifier has its own internal protection for many conditions of excess power dissipation. The output constraints of the Safe Operating Area Curves must still be observed.

The 3571AM and 3572AM have several other features that improve their utility. For instance, the metal case of the units is completely electrically isolated. (This can be contrasted to most power semiconductors where the case is connected to the collector of the device.) This simplifies mounting and reduces cost because the need for insulating spacers and bushings is eliminated. The hermetically sealed package improves reliability and will withstand severe environments better than discrete component amplifiers. The small package size makes mounting more convenient.

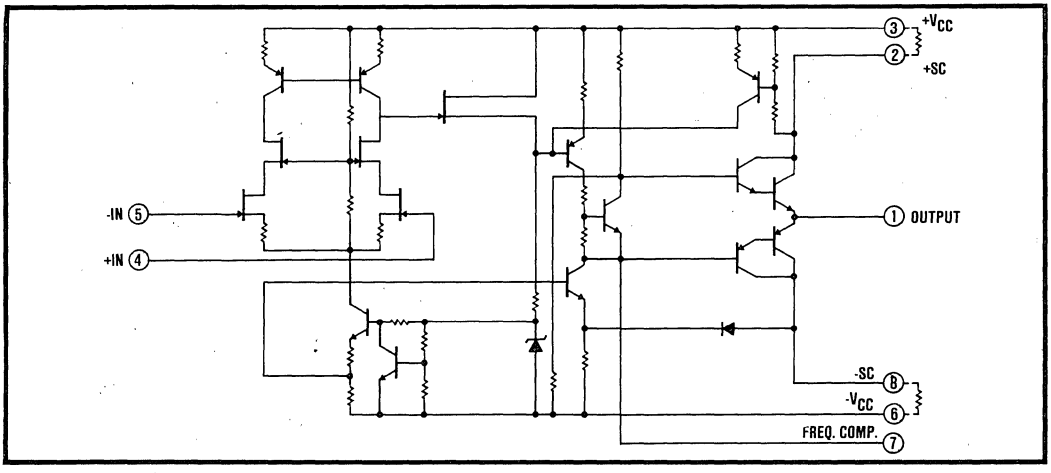


FIGURE 1. Equivalent Circuit

SPECIFICATIONS

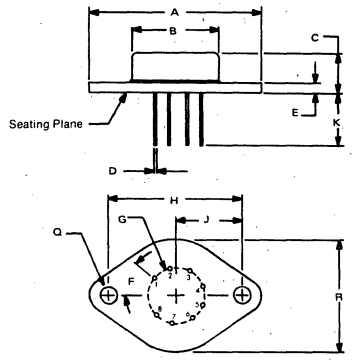
ELECTRICAL

Typical at T_{case} = 25°C and $\pm V_{CC}$ = ±35VDC max unless otherwise noted.

MODELS	3571AM	3572AM
RATED OUTPUT (to load)		
Power to Load		
Continuous, min(1)	30W	60W
Peak, min(1)	60W	150W
Output Voltage, ±(|V_{CC}|-5)V		
Continuous, min(1)	±30V at ±1A	±30V at ±2A
Peak, min(1)	±30V at 2A	±30A at 5A
Load Capacitance, min. C_C = 0	3300pF	
C_C = 1000pF	15µF	
DISSIPATION RATING		
At 25°C Case Temperature	33W	50W
Derating Above 25°C	See Typical Performance Curves	
Thermal Resistance, Case to Free Air	30°C/W	
Thermal Time Constant (no heat sink)	2 minutes	
Thermal Resistance, Junction to Case	2.5°C/W	
POWER SUPPLY		
Voltage, ±V_{CC}	±15VDC to ±40VDC	
Quiescent Current, max	±35mA	
OPEN LOOP		
Gain min, at R_{load} = 30Ω (3572AM)	94dB	
R_{load} = 60Ω (3571AM)		
Output Impedance	2.5Ω	
FREQUENCY RESPONSE		
Unity Gain Bandwidth, Small Signal	500kHz	
Full Power Bandwidth	16kHz at Vpk = 30V	
Slew Rate, C_C = 1000pF	3V/µsec	
INPUT OFFSET VOLTAGE		
Initial at 25°C, max	±2mV	
Drift vs. Temp., max	±40µV/°C	
Drift vs. Supply Voltage	±100µV/V	
Drift vs. Time	50µV/mo	
Drift vs. Power Dissipation (T_C constant)	20µV/W	
INPUT BIAS CURRENT		
Initial at 25°C, max	-100pA	
Drift vs. Temp.	doubles every 10°C	
Drift vs. Supply Voltage	0.5pA/V	
INPUT OFFSET CURRENT		
Initial at 25°C	±50pA	
Drift vs. Temp.	doubles every 10°C	
Drift vs. Supply Voltage	0.5pA/V	
INPUT IMPEDANCE		
Differential	10^{11}Ω || 10pF	
Common-mode	10^{11}Ω	
INPUT NOISE		
Voltage 0.01Hz to 10Hz, p-p	4µV	
10Hz to 1kHz, rms	3µV	
Current 0.01Hz to 10Hz, p-p	1pA	
10Hz to 1kHz, rms	0.1pA	
INPUT VOLTAGE RANGE		
Max Safe Differential Voltage	(+V_{CC} +| -V_{CC}|)	
Max Safe Common-mode Voltage	+V_{CC} to -V_{CC}	
Common-mode Voltage, Linear Operation	±(|V_{CC}| -10)V	
Common-mode Rejection	80dB min., 90dB, typ.	
TEMPERATURE RANGE (Case)		
Specification	-25°C to +85°C	
Operating	-55°C to +125°C	
Storage	-55°C to +125°C	

NOTE:
1. Safe Operating Area and Power Derating limitations must be observed.

MECHANICAL

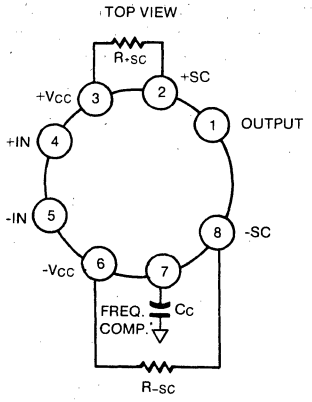


NOTE:
Leads in true position within 0.010" 0.25mm R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2 67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.583 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

CONNECTION DIAGRAM



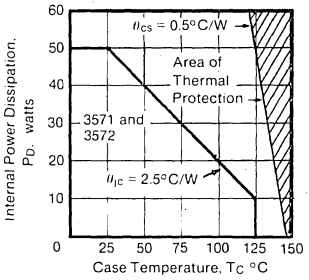
The case is electrically isolated. It is recommended that the case be grounded during use.

*A 1000pF ±20% ceramic capacitor is recommended for all circuit configurations and at all amplifier gains. The capacitor's lead lengths should be short. For gains above 10V/V, C_C is not absolutely required but is recommended.

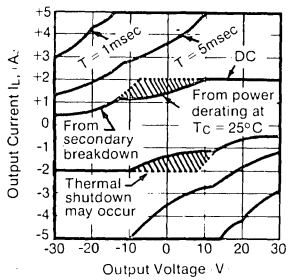
TYPICAL PERFORMANCE CURVES

(Typical T_{case} = 25°C and ±V_{CC} = ±35VDC unless otherwise noted.)

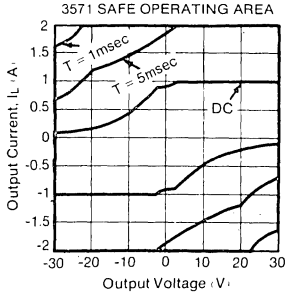
POWER DERATING



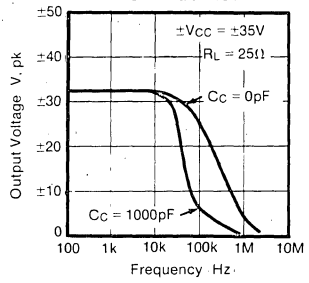
3572 SAFE OPERATING AREA



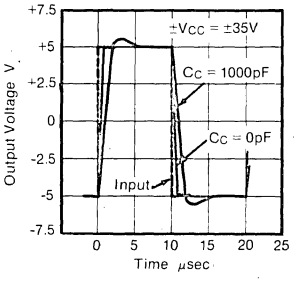
3571 SAFE OPERATING AREA



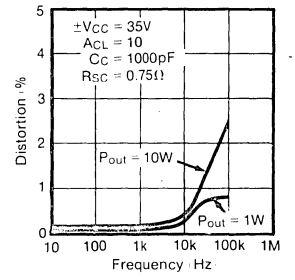
OUTPUT VOLTAGE VS. FREQUENCY



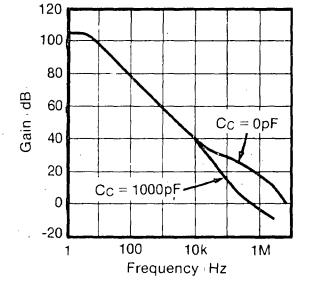
VOLTAGE FOLLOWER PULSE RESPONSE



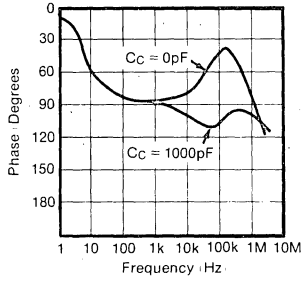
DISTORTION VS FREQUENCY



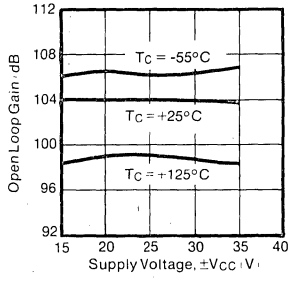
OPEN-LOOP GAIN VS FREQUENCY



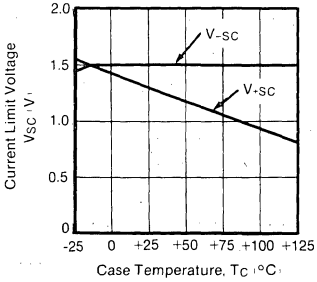
OPEN-LOOP PHASE



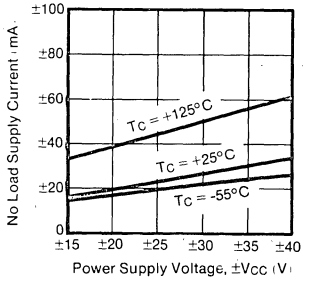
OPEN-LOOP GAIN VS SUPPLY VOLTAGE



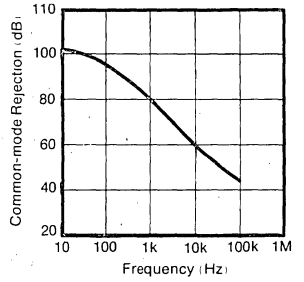
CURRENT LIMIT VOLTAGE VS TEMPERATURE



QUIESCENT CURRENT VS SUPPLY VOLTAGE



COMMON-MODE REJECTION VS FREQUENCY



INSTALLATION AND OPERATING INSTRUCTIONS

GENERAL PRECAUTIONS

Current Limiting

It is recommended that during initial amplifier setup, particularly in breadboarding and when a lack of familiarity with the amplifier exists, that the current limit be set at about 250mA ($R_{SC} \cong 5.6\Omega$). This will allow verification of the circuit and will minimize the possibility of damaging the amplifier. Later, when the circuit configuration and connections have been proven, the current limits can be raised to the desired value.

Minimum Heat Sink

The 3571AM and 3572AM require a minimum heat sink of 16°C W or lower in order to insure thermal stability (mounting on a 3" x 3" x 0.06" piece of 80% copper-clad printed circuit board material will be sufficient). Normally, this will not be a consideration since a larger heat sink will be used to provide the proper power dissipation as described in the Thermal Considerations section which follows.

Proper Grounding and Power Supply Bypassing

Particular attention should be given to proper grounding practices because the large output currents can cause significant grounding-loop errors. Proper connections are shown in Figure 2.

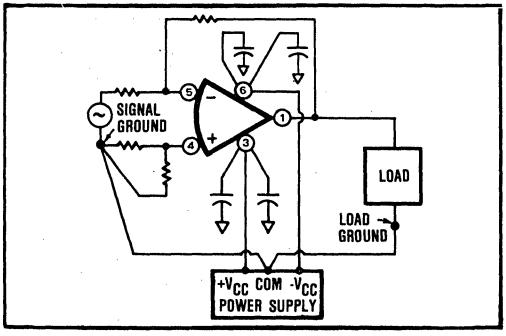


FIGURE 2. Proper Power Supply Connections.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be physically separated from the amplifier input and signal leads.

The amplifier power supply should be bypassed with 50μF tantalum capacitors connected in parallel with 0.01μF ceramic capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

CURRENT LIMITS

The amplifiers are designed so that both the positive and negative load current limits can be adjusted with external resistors, R_{+SC} and R_{-SC} respectively. The value of the resistors are given by the following equations:

$$R_{+SC} = \frac{1.3\ (\text{volts})}{I_{+\text{limit}}(\text{amps})},\quad R_{-SC} = \frac{1.5\ (\text{volts})}{I_{-\text{limit}}(\text{amps})}$$

I_{limit} is the desired maximum current. The maximum power dissipation of the resistors is $P_{max} = R_{SC}(I_{limit})^2$. The current limits determined by the equations above are accurate to about ±10%. The variation of I_{limit} versus temperature is shown in the Typical Performance Curves. Both $+V_{CC}$ and $-V_{CC}$ must be on for the current limits to function.

To avoid introducing unwanted inductance into the current limit circuitry, which may introduce oscillations and permanent damage, both current limit resistors must be noninductive. Do not use wire wound resistors. Carbon composition resistors are preferred and paralleling them can provide a wide current limit range at the wattage needed.

The maximum value of the negative current limit resistor is 15Ω (100mA, min). Exceeding this value, or an open circuit, could permanently damage the internal 75Ω, thin-film resistor which parallel R_{-SC}.

The amplifier should be used with as low a current limit as possible for the particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and increase reliability by limiting the internal power dissipation of the amplifier.

THERMAL CONSIDERATIONS

The 3571AM and 3572AM are rated for 150°C maximum junction temperature. The thermal resistance from junction to case (θ_{jc}) is 2.5°C W. The corresponding Power Derating Curve is given in the Typical Performance Curves.

The internal power dissipation of the amplifier is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipated in the output stage due to the load. (For $\pm V_{CC} = \pm 40V$, $P_{DQ} = 80 \times 0.035 = 2.8W$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{out}$) the maximum value of P_{DL} occurs at $\pm V_{out} = \pm V_{CC}/2$ and is equal to $P_{DL,max} = (\pm V_{CC})^2/4R_L$. Figure 3 shows P_D as function of the output voltage with the load resistance as a running parameter.

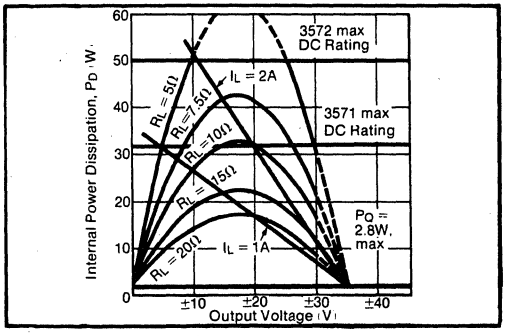


FIGURE 3. Internal Power Dissipation vs. Output Voltage.

P_{DL} for any other value of V_{out} can be computed from

$$P_{DL} = (\pm V_{CC} - \pm V_{out}) \cdot I_L = (\pm V_{CC} - \pm V_{out}) \left(\frac{\pm V_{out}}{R_L} \right).$$

The use of an adequate heat sink is mandatory and thermal resistance of the heat sink (θ_{hs}) can be determined from the equation:

$$\theta_{hs} = (T_J - T_A / P_D) - \theta_{jc}$$

where T_J is the desired amplifier junction temperature (+150°C, max), T_A is the ambient temperature, P_D is the amplifiers dissipation, $P_D = P_{DO} + P_{DL}$, and θ_{jc} is the junction to case thermal resistance of the amplifier. Burr-Brown Application Note AN-83 entitled, "How to Determine What Heat Sink to Use", is available for additional information.

The electrically isolated case of the 3571AM and 3572AM simplifies mounting the amplifiers to the heat sink (and the heat sink to any other assemblies) since there is no need for electrical insulation. Thermal joint compound and lock washers should be used to prevent mechanical relaxation due to thermal stresses.

Safe Operating Area

There are additional constraints on the output voltage and current other than those just due to the maximum internal power dissipation of the amplifiers. These are related to the prevention of secondary breakdown in the output stage transistors. These restrictions are shown in the Safe Operating Area Curves in the Typical Performance Curves.

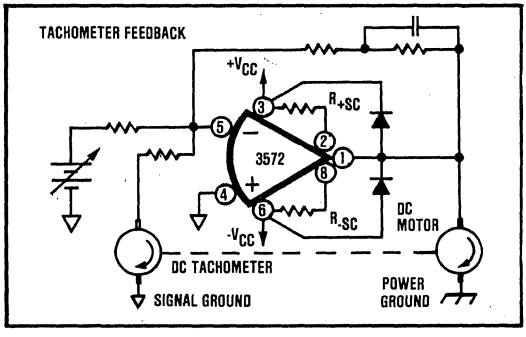
Application Constraint

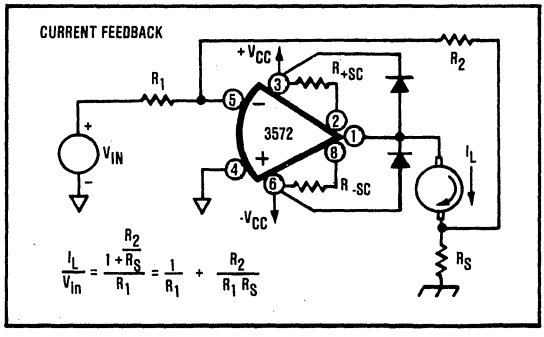
Because of the possibility of damaging the output stage if frequency instability (oscillations) occurs, applications with an inductive load which will activate the current limit of the amplifier, are limited to a load impedance phase angle of less than 60°C leading, over the frequency band of 10kHz to 100kHz. Increasing the load's series resistance will decrease the angle, if necessary. Larger inductive loads may be applied if current limit is not activated.

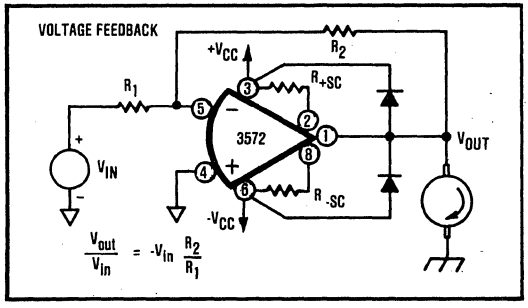
Frequency Compensation

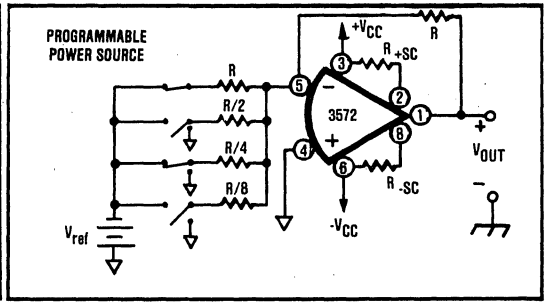
The optimum value of the compensation capacitor is 1000pF. A ±20% tolerance ceramic capacitor is recommended. The compensation capacitor should be used with all circuit configurations and at all amplifier gains (see note on Connection Diagram).

TYPICAL APPLICATIONS









BURR-BROWN®

3573

High Current - High Power OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT POWER
  - 100 Watts Peak
  - 40 Watts Continuous
- WIDE SUPPLY RANGE
  - ±10 to ±34 Volts
- HIGH OUTPUT CURRENT
  - ±5 Amps Peak
  - ±2 Amps Continuous
- SMALL SIZE: TO-3 PACKAGE
- LOW COST

APPLICATIONS

- DC MOTORS
- AC MOTORS
- ACTUATORS
- ELECTRONIC VALVES
- SYNCROS

DESCRIPTION

If you need to supply 100 watts peak or 40 watts continuous, yet must choose a small, easy to use op amp, you'll find the 3573 a logical solution. This hybrid IC delivers ±5A peak minimum at ±20V minimum to the load when operated from ±28V power supplies. The design of this op amp has been optimized for low cost while preserving moderately good input and distortion characteristics.

Output circuitry provides for external current limiting resistors for both positive and negative currents. This allows current limits to be set to values dictated by the op amp's application. 3573 is internally frequency compensated and is unconditionally stable with capacitive loads to 3300pF.

Housed in a small, rugged, hermetically sealed 8-lead TO-3 package, 3573 will withstand severe environments far better than discrete component amplifiers. The metal case is completely electrically isolated from the amplifier circuitry. Thus, mounting is easier (no isolation washers or spacers) and the hazards of a case connected to the output or supply voltage is eliminated.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

ELECTRICAL SPECIFICATIONS

At T_{case} = 25°C and $\pm V_{CC}$ = ±28VDC unless otherwise noted.

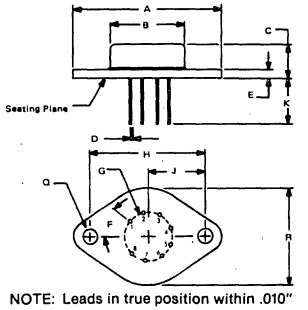
PARAMETER	CONDITIONS	3573AM MIN	3573AM TYP	3573AM MAX	UNITS
OPEN LOOP GAIN, DC	$R_L \geq 30\Omega$	94	115		dB
RATED OUTPUT					
Power to Load[1]					
Continuous		40			W
Peak		100			W
Output Current					
Continuous		±2			A
Peak		±5			A
Output Voltage	I_{out} = ±5A[4]	±20	±23		V
DYNAMIC RESPONSE					
Bandwidth, Unity Gain	Small Signal		1		MHz
Full Power Bandwidth		15	23		kHz
Slew Rate		1.35	1.5		V/µs
INPUT OFFSET VOLTAGE					
Initial Offset			±5	±10	mV
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±10	±65	µV/°C
vs Supply Voltage			±35		µV/V
INPUT BIAS CURRENT					
Initial	T_{case} = 25°C		15	40	nA
vs Temperature			±0.05		nA/°C
vs Supply Voltage			±0.02		nA/V
INPUT DIFFERENCE CURRENT					
Initial	T_{case} = 25°C		±5	±10	nA
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±0.01		nA/°C
INPUT IMPEDANCE					
Differential			10		MΩ
Common-mode			250		MΩ
INPUT NOISE					
Voltage Noise	f_n = 0.3Hz to 10Hz		3		µV p-p
	f_n = 10Hz to 10kHz		5		µVrms
Current Noise	f_n = 0.3Hz to 10Hz		20		pA p-p
	f_n = 10Hz to 10kHz		4.5		pA rms
INPUT VOLTAGE RANGE					
Common-mode Voltage	Linear Operation	±(V_{CC}-6)	±(V_{CC}-3)		V
Common-mode Rejection	f = DC, V_{CM} = ±22	70	110		dB
POWER SUPPLY					
Rated Voltage			±28		V
Voltage Range, derated		±10		±34	V
Current, quiescent			±2.6	±5	mA
TEMPERATURE RANGE					
Specification		-25		+85	°C
Operating,derated performance		-25		+85	°C
Storage		-65		+150	°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	±34VDC
Internal Power Dissipation[1]	45W
Differential Input Voltage[2]	±62VDC
Input Voltage Range[2]	±31VDC
Storage Temperature Range	-65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C
Output Short-Circuit Duration[3]	Continuous
Junction Temperature	150°C

1. Package must be derated based on a junction to case thermal resistance of 2.8°C/W, or a junction to ambient thermal resistance of 30°C/W.
2. For supply voltages less than ±34VDC, the absolute maximum voltage is three volts less than supply voltage.
3. Safe Operating Area and Power Derating Curves must be observed.
4. With R±SC = 0.

MECHANICAL

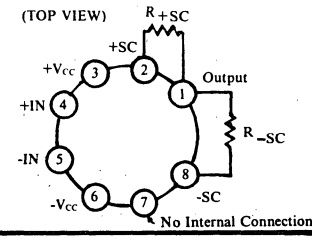


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.240	.290	6.10	7.37
D	.038	.042	.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

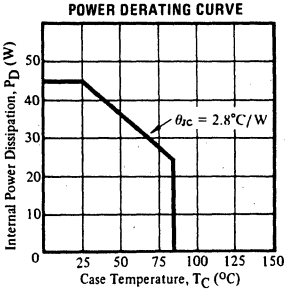
CONNECTION DIAGRAM



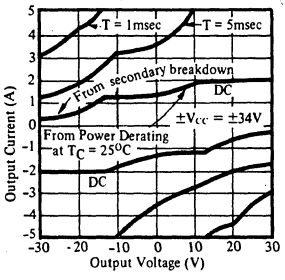
TYPICAL PERFORMANCE CURVES

(Typical at 25°Case and $\pm V_{CC} = \pm 28$ VDC unless otherwise noted.)

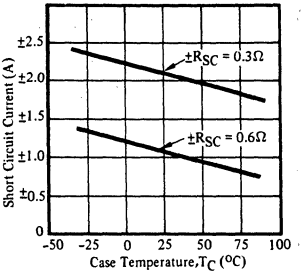
POWER DERATING CURVE



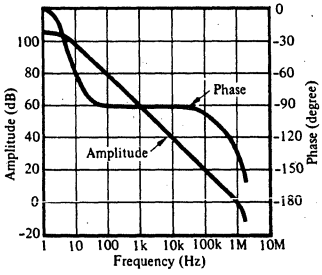
SAFE OPERATING AREA



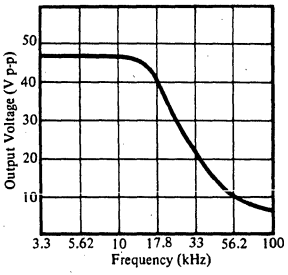
CURRENT LIMITING



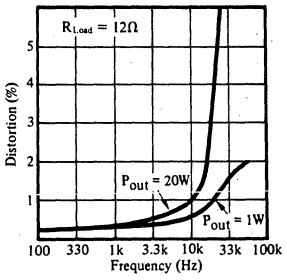
OPEN LOOP FREQUENCY RESPONSE



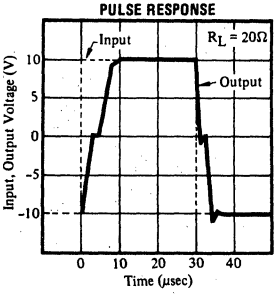
OUTPUT VOLTAGE VS FREQUENCY



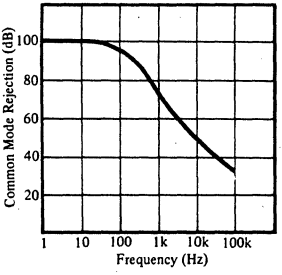
HARMONIC DISTORTION



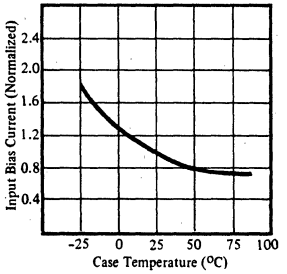
VOLTAGE FOLLOWER PULSE RESPONSE



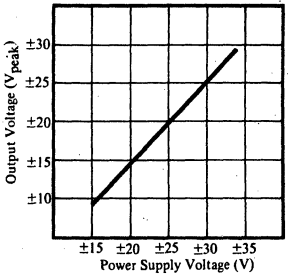
COMMON MODE REJECTION VS FREQUENCY



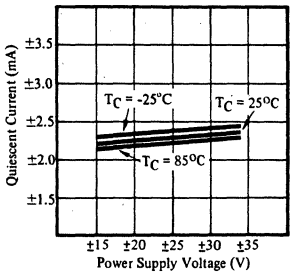
INPUT BIAS CURRENT VS TEMPERATURE



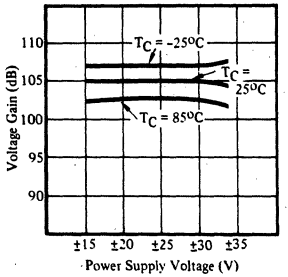
OUTPUT VOLTAGE SWING VS POWER SUPPLY VOLTAGE



QUIESCENT CURRENT VS POWER SUPPLY VOLTAGE



OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



INSTALLATION AND OPERATING INSTRUCTIONS

GENERAL PRECAUTIONS

CURRENT LIMITING

It is recommended that during initial amplifier setup, particularly in breadboarding and when a lack of familiarity with the amplifier exists, that the current limit be set at about 250mA ($R_{SC} \cong 2.6\Omega$). This will allow verification of the circuit and will minimize the possibility of damaging the amplifier. Later, when the circuit configuration and connections have been proven, the current limits can be raised to the desired value.

PROPER GROUNDING & POWER SUPPLY BYPASSING

Particular attention should be given to proper grounding practices because the large output currents can cause significant ground loop errors. Figure 1 illustrates proper connections.

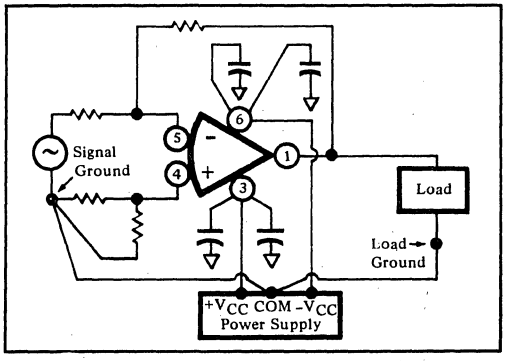


FIGURE 1. Proper Power Supply Connections.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

The amplifier should be power supply bypassed with 50μF tantalum capacitors connected in parallel with 0.01 μF ceramic capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

CURRENT LIMITS

The amplifier is designed so that both the positive and negtive load current limits can be adjusted with external resistors, R_{+SC} and R_{-SC} respectively. The value of the resistors are given by the following equation:

$$R_{SC} = \frac{0.65 \text{ (volts)}}{I_{limit} \text{ (amps)}}$$

I_{limit} is the desired maximum current. The maximum power dissipation of the resistors is $P_{max} = R_{SC} (I_{limit})^2$. The current limits determined by the equations above are accurate to about ±10%. The variation of I_{limit} vs temperature is shown in the Typical Performance Curves.

The amplifier should be used with as low a current limit as possible for the particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and increase reliability by limiting the internal power dissipation of the amplifier.

THERMAL CONSIDERATIONS

The 3573AM is rated for 150°C maximum junction temperature. The thermal resistance from junction to case (θ_{jc}) is 2.8°C/W per watt. The corresponding Power Derating Curve is given in the Typical Performance Curves section.

The internal power dissipation of the amplifier is given by the equation $P_D = P_{DQ} + P_{DL}$ where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipated in the output stage due to the load.

The thermal resistance of the required heat sink (θ_{hs}) can be determined from the equation:

$$\theta_{hs} = \frac{T_J - T_A}{P_D} - \theta_{jc}$$

where T_J is the desired amplifier junction temperature (+150°C max), T_A is the ambient temperature, P_D is the amplifier's dissipation, $P_D = P_{DQ} + P_{DL}$, and θ_{jc} is the junction to case thermal resistance of the amplifier.

The electrically isolated case of the 3573AM simplifies mounting the amplifiers to the heat sink (and the heat sink to any other assemblies) since there is no need for electrical insulation. Thermal joint compound and lock washers should be used to prevent mechanical relaxation due to thermal stresses.

SAFE OPERATING AREA

There are additional constraints on the output voltage and current other than those just due to the maximum internal power dissipation of the amplifiers. These are related to the prevention of secondary breakdown in the output stage transistors. These restrictions are shown in the SAFE OPERATING AREA CURVES in the Typical Performance Curves.

BURR-BROWN®

3580
3581
3582

For a /883B version of this product, see OPA8780/883B in the Military Products section.

High Voltage OPERATIONAL AMPLIFIERS

FEATURES

- HIGH OUTPUT SWINGS, up to ±145V (3582)
- LARGE LOAD CURRENTS, up to ±60mA (3580)
- DIFFICULT TO DAMAGE, automatic thermal shutoff
- REDUCES SOURCE LOADING, $10^{11}\Omega$ Input Z
- PRESERVES SYSTEM ACCURACY, 110dB CMR 20pA bias current

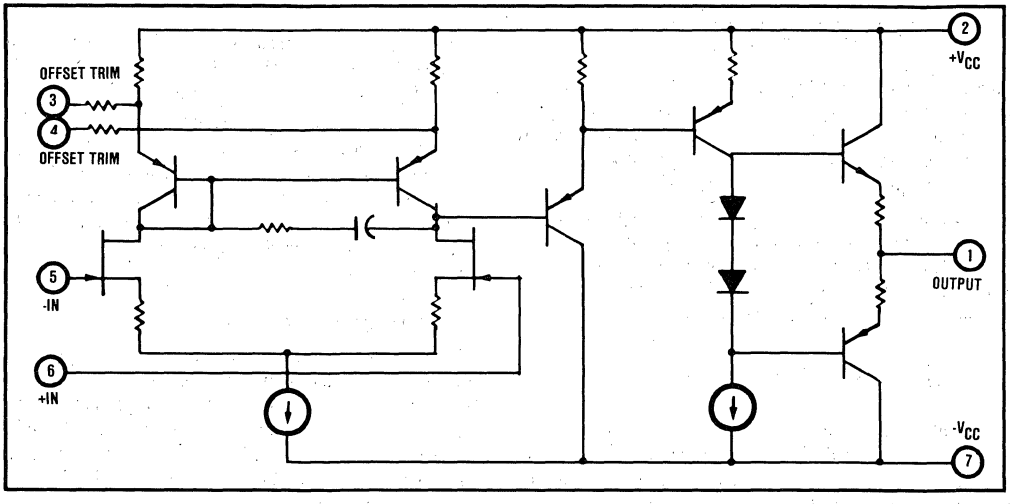
DESCRIPTION

The 3580 series is the first family of Integrated Circuit operational amplifiers which will provide output voltage swings of up to ±145V.

The monolithic FET input stage has low bias currents (20pA) which minimizes the offset voltages caused by the bias current and the large resistance normally associated with high voltage circuits.

The 3580 series is packaged in a TO-3 package which will dissipate over 3W of power without a heat sink and 4.5W with a suitable heat sink.

The input stage is protected against overvoltages and the output stage is protected against short-circuits-to-ground. A special thermal sensing circuit prevents damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.



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THEORY OF OPERATION

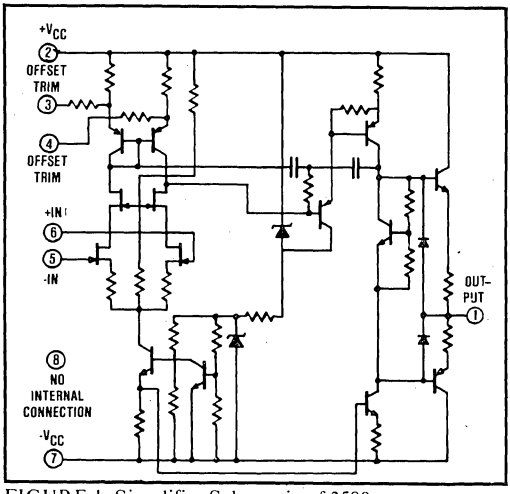


FIGURE 1. Simplifier Schematic of 3580.

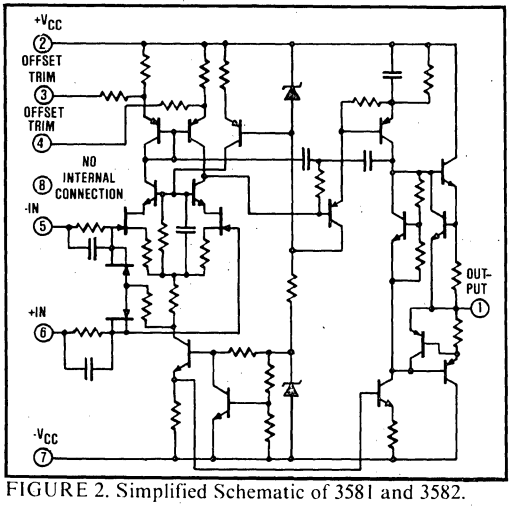


FIGURE 2. Simplified Schematic of 3581 and 3582.

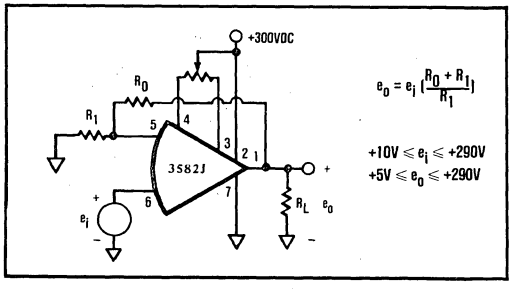


FIGURE 3. Operation from a Single Supply.

The 3580 family of integrated circuit high voltage amplifiers provides performance which previously was only available in bulky modular packages (see Figures 1 and 2). In addition to the smaller size and inherent reliability, the integrated circuit construction offers other advantages not normally available in modular or discrete component units. The amplifiers have thermal sensing and shut-off circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the input stage current source when the temperature reaches a critical level. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases.

If the cause of the abnormal power dissipation is continuous (such as a short circuit across the load) the output current may remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal condition is removed.

The incorporation of thermal sensing and shut-off in the amplifier will allow the use of a smaller heat sink than would otherwise be required. This is due to the fact that the amplifier will protect itself and does not require a massive heat sink for protection under abnormal conditions.

Another unique feature of the 3580 family is the thorough testing of the unit receiver. In addition to the normal tests, all amplifiers are 100% tested for input protection at the full rated differential voltage ($+V_{CC}$ -V_{CC}). Each unit is also 100% tested for output short circuit to common at maximum supply voltage.

The 3581 and 3582 have a unique feature that is important in many high voltage applications. In these two models the input bias current is virtually independent of the applied common-mode voltage. This is accomplished by the true cascode input stage which keeps the drain-to-source voltage of the input transistors constant as the common-mode voltage changes.

OPERATION FROM A SINGLE SUPPLY

It may be desirable in some applications to operate the amplifiers from a single supply. The circuit in Figure 3 illustrates a typical application.

Note that there are restrictions on the input and output voltages (e_i and e_o) which are necessary in order to keep the amplifier circuits operating in a linear manner.

It should be noted that when the 3581 and 3582 amplifiers are operated from a single supply, the output stage, which is still short-circuit-current limited and thermally protected, is not protected against short circuits to ground (the 3580 will still be short circuit protected under these conditions). When the amplifiers are operated from a single supply, the voltage across one of the output transistors is high enough that secondary breakdown is a consideration. The output current must be limited in order to prevent damage. This can be done by keeping the load resistor larger than 5kΩ for the 3582 and greater than 1kΩ for the 3581.

SPECIFICATIONS

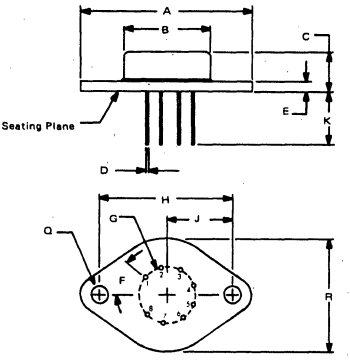
ELECTRICAL

Typical at T_{CASE} = +25°C max unless otherwise noted.

MODELS	3580J	3581J	3582J
POWER SUPPLY			
Voltage, $\pm V_{CC}$	±15VDC to ±35VDC	+32VDC to ±75VDC	±70VDC to ±150VDC
Quiescent Current, max	±10mA	±8mA	±6.5mA
RATED OUTPUT			
Voltage, $\pm\lvert V_{CC}\rvert$ -5 VDC, min	±10VDC to ±30VDC	±27VDC to ±70VDC	±65VDC to ±145VDC
Current, min	±60mA	±30mA	±15mA
Current, Short Circuit	+100mA	±50mA	±25mA
Load Capacitance, max		10nF	
OPEN-LOOP GAIN			
No Load, DC	106dB	112dB	118dB
Rated Load, DC, min	86dB	94dB	100dB
FREQUENCY RESPONSE			
Unity Gain Bandwidth, Small Signal		5MHz, min	
Full Power Bandwidth	100kHz	60kHz	30kHz
Slew Rate	15V/µs	20V/µs	20V/µs
Settling Time, 0.1%		12µs	
INPUT OFFSET VOLTAGE			
Initial at T_{CASE} = +25°C, max	+10mV	+3mV	+3mV
Drift vs Temp, max	+30µV/°C	+25µV/°C	+25µV/°C
Drift vs Supply Voltage	100µV/V	20µV/V	20µV/V
Drift vs Time	100µV/mo	50µV/mo	50µV/mo
INPUT BIAS CURRENT			
Initial at T_{CASE} = +25°C, max	-50pA	-20pA	-20pA
Drift vs Temp		doubles every 10°C	
Drift vs Supply Voltage	0.5pA/V	0.2pA/V	0.2pA/V
INPUT OFFSET CURRENT			
Initial at T_{CASE} = +25°C, max		±20pA	
Drift vs Temp		doubles every 10°C	
Drift vs Supply Voltage	0.5pA/V	0.2pA/V	0.2pA/V
INPUT IMPEDANCE			
Differential		$10^{11}\Omega$ 10pF	
Common-mode		$10^{11}\Omega$	
INPUT NOISE			
Voltage 0.01Hz to 10Hz, p-p		5µV	
10Hz to 1kHz, rms	1µV	1.7µV	1.7µV
Current 0.01Hz to 10Hz, p-p	1pA	0.3pA	0.3pA
INPUT VOLTAGE RANGE			
Max Safe Differential Voltage(1)		$+V_{CC}$ + $-V_{CC}$	
Max Safe Common-mode Voltage		$+V_{CC}$ to $-V_{CC}$	
Common-mode Voltage, Linear Operation	$-V_{CC}$ -8 V	+ V_{CC} -10 V	± V_{CC} -10 V
Common-mode Rejection	86dB	110dB	110dB
TEMPERATURE Case			
Specification		0°C to 70°C	
Operating		-55°C to +125°C	
Storage		-55°C to +150°C	

NOTE:
1. On Models 3581 and 3582 the inputs may be damaged by pulses at pins 5 or 6 with $dV/dt \geq 1V/ns$. Any possible damage can be eliminated by limiting the input current to 150mA with external resistors in series with those pins. No external protection is needed for slower voltage.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

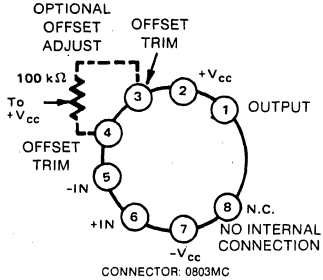
ORDER NUMBER: 3580J
3581J
3582J

WEIGHT: 15 GRAMS

CASE: METAL

PIN CONFIGURATION

TOP VIEW



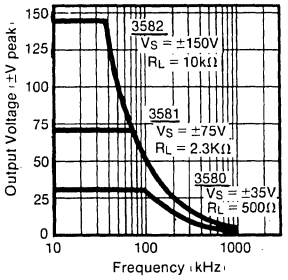
CONNECTOR: 0803MC
HEAT SINK: 0803HS
0804HS
0805HS

*The case is electrically isolated. It is recommended that the case be grounded during use.

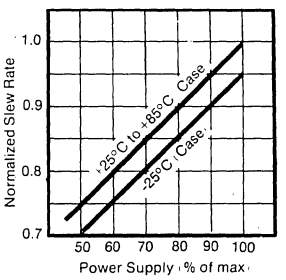
TYPICAL PERFORMANCE CURVES

T_{CASE} = +25°C and $\pm V_{CC}$ max unless otherwise noted.

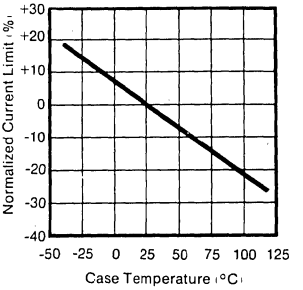
OUTPUT VOLTAGE VS FREQUENCY



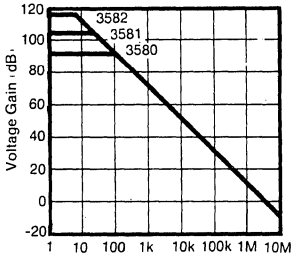
SLEW RATE VS SUPPLY VOLTAGE AT FULL LOAD



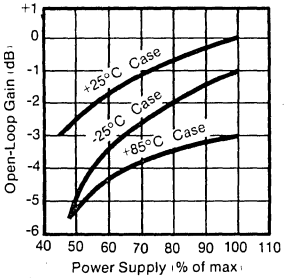
CURRENT LIMIT VS TEMPERATURE



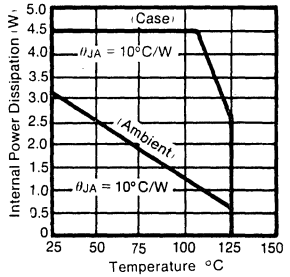
OPEN-LOOP FREQUENCY RESPONSE-FULL LOAD



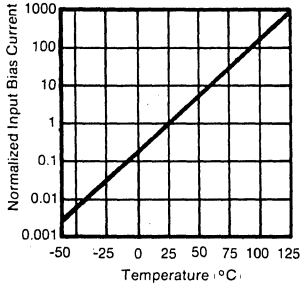
OPEN-LOOP GAIN VS SUPPLY VOLTAGE AT MAX LOAD



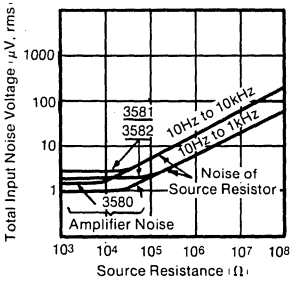
MAXIMUM POWER DISSIPATION



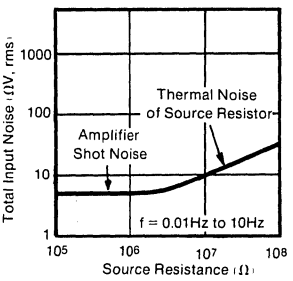
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



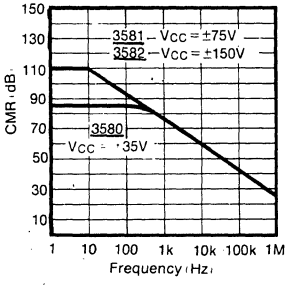
TOTAL INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



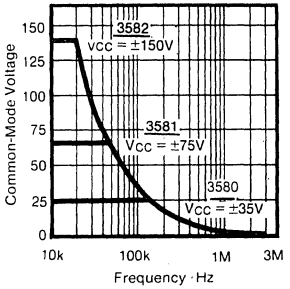
TOTAL LOW FREQUENCY INPUT NOISE VS SOURCE RESISTANCE



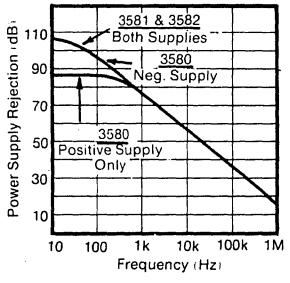
COMMON-MODE REJECTION VS FREQUENCY



MAXIMUM COMMON-MODE VOLTAGE VS FREQUENCY



POWER SUPPLY REJECTION VS FREQUENCY



BURR-BROWN®

3583

High Voltage - High Current OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT SWINGS, Up to ±140V
- LARGE LOAD CURRENTS, ±75mA
- PROTECTED OUTPUT STAGE, Automatic Thermal Shutoff
- REDUCES SOURCE LOADING, $10^{11}\Omega$ Input Z
- PRESERVES SYSTEM ACCURACY, 110dB CMR 20pA Bias Current

APPLICATIONS

- PROGRAMMABLE POWER SUPPLY OUTPUT AMPLIFIER
- HIGH VOLTAGE CURRENT SOURCE
- POWER BOOSTER
- HIGH VOLTAGE INTEGRATOR
- DIFFERENTIAL AMPLIFIER FOR HIGH COMMON-MODE VOLTAGE CIRCUITS

DESCRIPTION

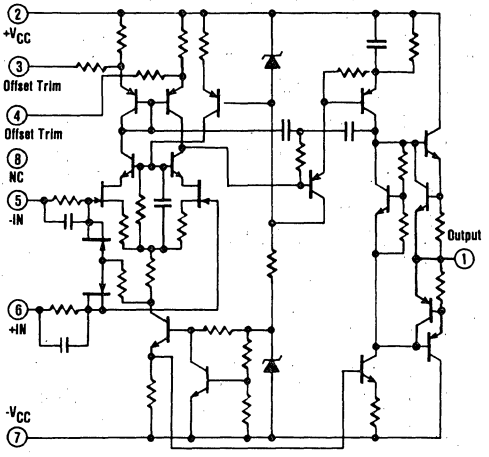
The 3583 is the first integrated circuit operational amplifier to provide output voltage swings of ±140V with currents as high as ±75mA.

The amplifier operates over a wide supply range (±50VDC to ±150VDC) and has excellent input characteristics (110dB CMR, 3mV V_{OS}, 25μV/°C $\Delta V_{OS}/\Delta T$).

The monolithic FET input stage has low bias current (20pA) which minimizes the offset voltages caused by the bias current and the large resistances normally associated with high voltage circuits.

The input stage is protected against overvoltages and the output stage is protected against short-circuits to ground for supply voltages below ±100VDC. A special thermal sensing circuit prevents damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

Two temperature ranges are available: 0°C to +70°C (3583JM) and -25°C to +85°C (3583AM).



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SPECIFICATIONS

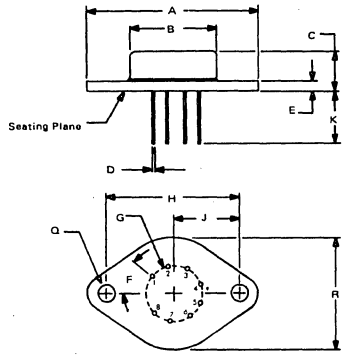
ELECTRICAL

Specifications typical at T_{CASE} = +25°C and $\pm V_{CC}$ = 150VDC unless otherwise noted.

MODELS	3583AM	3583JM
POWER SUPPLY		
Voltage, $\pm V_{CC}$	±50VDC to ±150VDC	
Quiescent Current, max	8.5mA	
RATED OUTPUT		
Voltage, $\pm$| V_{CC}| -10 VDC, min	±40VDC to ±140VDC	
Current, min	±75mA	
Current, Short Circuit	±100mA	
Load Capacitance, max	10nF	
OPEN-LOOP GAIN		
No Load, DC	118dB	
Rated Load, DC	94dB, min; 105dB, typ	
FREQUENCY RESPONSE		
Unity Gain Bandwidth, Small Signal	5MHz	
Full Power Bandwidth, R_L = 10kΩ	60kHz	
Slew Rate	30V/μsec	
Settling Time, 0.1%	12μsec	
INPUT OFFSET VOLTAGE T_A = +25°C		
Initial at 25°C, max	±3mV	
Drift vs Temp, max	±23μ/°C	
Drift vs Supply Voltage	±20μV/V	
Drift vs Time	±50μV/mo	
INPUT BIAS CURRENT		
Initial at 25°C, max	-20pA	
Drift vs Temp	doubles every 10°C	
Drift vs Supply Voltage	0.2pA/V	
INPUT OFFSET CURRENT		
Initial at 25°C	±20pA	
Drift vs Temp	doubles every 10°C	
Drift vs Supply Voltage	0.2pA/V	
INPUT IMPEDANCE		
Differential	10^{11}Ω ||10pF	
Common-mode	10^{11}Ω	
INPUT NOISE		
Voltage 0.01Hz to 10Hz, p-p	5μV	
10Hz to 1kHz, rms	1.7μV	
Current 0.01Hz to 10Hz, p-p	0.3pA	
INPUT VOLTAGE RANGE		
Max Safe Differential Voltage(1)	|+V_{CC} +| -V_{CC}|	
Max Safe Common-mode Voltage	+V_{CC} to -V_{CC}	
Common-mode Voltage, Linear Operation	$\pm$| V_{CC}| -10V	
Common-mode Rejection	110dB	
TEMPERATURE RANGE (Case)		
Specification	-25°C to +85°C	0°C to 70°C
Operating	-55°C to +125°C	
Storage	-55°C to +125°C	

NOTES:
1. The inputs may be damaged by pulses at pins 5 or 6 with dV/dt ≥ 1V/nsec. Any possible damage can be eliminated by limiting the input current to 150mA with external resistors in series with those pins. No external protection is needed for slower voltage changes.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

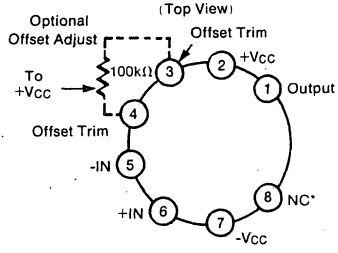
ORDER NUMBER:
3583AM 3583JM

WEIGHT:
15.1 Grams

MATING CONNECTOR:
0803MC

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.240	.290	6.10	7.37
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

CONNECTION DIAGRAM

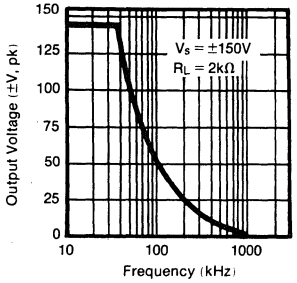


* No internal connection.
The metal case is electrically isolated. It is recommended that the case be grounded during use.

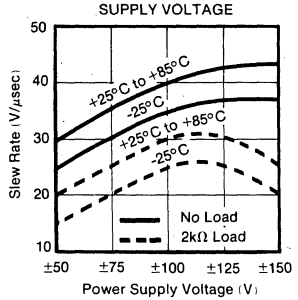
TYPICAL PERFORMANCE CURVES

Typical at T_{CASE} = +25°C and $\pm V_{CC}$ = 150VDC unless otherwise noted.

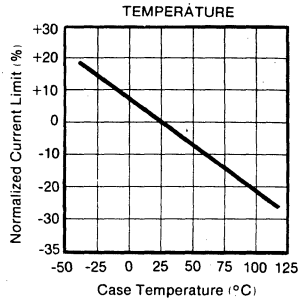
OUTPUT VOLTAGE vs FREQUENCY



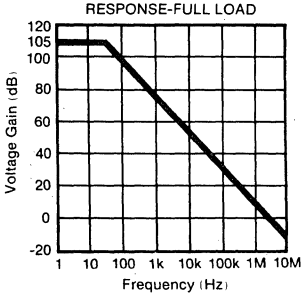
SLEW RATE vs SUPPLY VOLTAGE



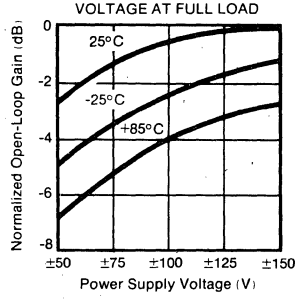
CURRENT LIMIT vs TEMPERATURE



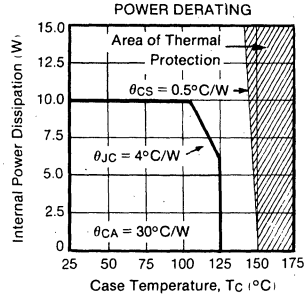
OPEN-LOOP FREQUENCY RESPONSE-FULL LOAD



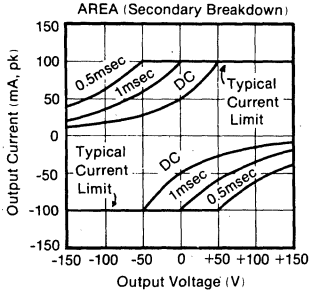
OPEN-LOOP GAIN vs SUPPLY VOLTAGE AT FULL LOAD



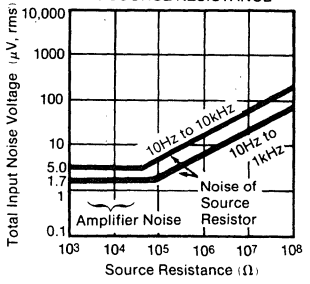
RECOMMENDED POWER DERATING



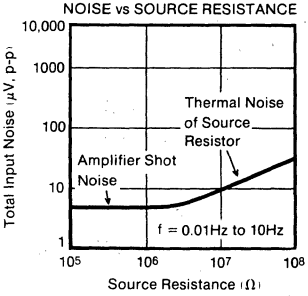
RECOMMENDED SAFE OPERATING AREA (Secondary Breakdown)



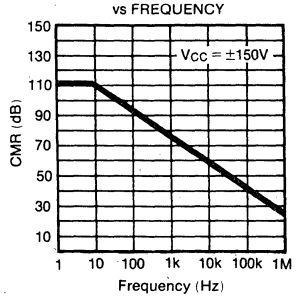
TOTAL INPUT NOISE VOLTAGE vs SOURCE RESISTANCE



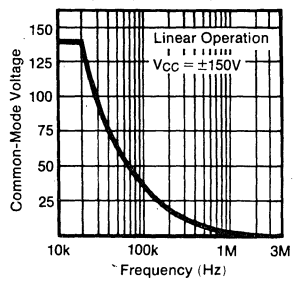
TOTAL LOW FREQUENCY INPUT NOISE vs SOURCE RESISTANCE



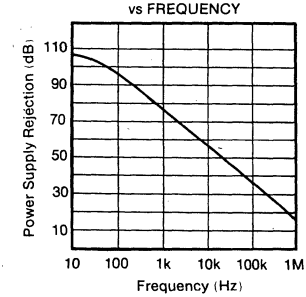
COMMON-MODE REJECTION vs FREQUENCY



COMMON-MODE VOLTAGE vs FREQUENCY



POWER SUPPLY REJECTION vs FREQUENCY



APPLICATIONS INFORMATION

The 3583 is a high voltage, high output current integrated circuit operational amplifier. Its ease of use, compact size, and excellent input and output specifications makes it well suited for a wide variety of high voltage applications.

The equivalent circuit for the 3583 is shown in Figure 1. The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The offset voltage at 25°C and the drift versus temperature are compensated by state-of-the-art laser-trimming techniques. They are low enough so that user-trimming will not be required in most applications. The high input impedance provides negligible source impedance loading errors when the noninverting circuit configuration is used. The low bias currents minimize offset errors when large values of source and feedback resistors are used.

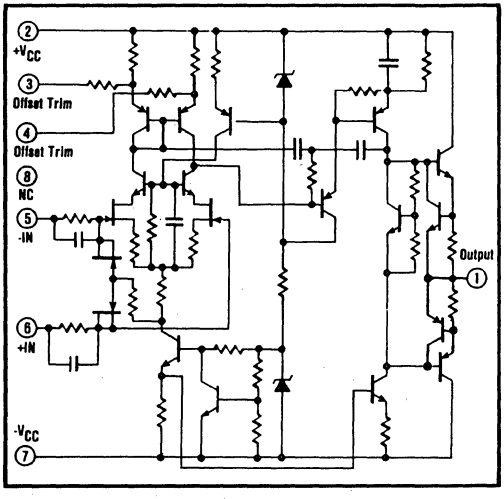


FIGURE 1. 3583 Equivalent Circuit.

A true cascade input stage is used together with considerable protection circuitry. There are voltage limiting transistors to prevent damage due to reverse bias breakdown of the input pair and current limiting resistors to limit the input current to 1mA with the inputs at ±150 volts. The units are conservatively rated (and 100% tested) at full rated differential voltage (+150V and -150V) but typically will withstand a 50% overvoltage without damage.

The unit operates over a wide supply range (±50V to ±150V) with outstanding common-mode rejection (110dB). It also has another feature which is important in many high voltage applications. The input bias current is virtually independent of applied common-mode voltage. The output circuit has a unique protection feature which is only practical in integrated-circuit amplifiers - self-contained automatic thermal sensing and shutoff circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the amplifier's biasing network when the temperature reaches 150°C. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases. The output current will remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal load condition is removed.

The internal thermal protection removes some of the constraints of power derating for abnormal operating conditions. The amplifier will protect itself for many conditions of excess power dissipation (see the Power Derating Curve). This allows the use of a smaller heat sink to protect against abnormal output conditions since the amplifier has its own internal protection for many conditions of excess power dissipation. The output constraints of the Recommended Safe Operating Area curves must still be observed.

The 3583 has several other features that improve its utility. For instance, the metal case of the unit is completely electrically isolated. (This can be contrasted to most power semiconductors where the case is connected to the collector of the device.) This simplifies mounting and reduces cost since the need for insulating spacers and bushings is eliminated. The hermetically sealed package improves reliability and will more easily withstand severe environments than do discrete component amplifiers. The small package size reduces weight and makes mounting more convenient.

Burr-Brown offers three heat sinks as accessories; 0803HS with a thermal resistance of 12°C/watt, 0804HS at 4.2°C/watt, and 0805HS at 3°C/watt. A convenient mating connector, 0803MC is also available.

BURR-BROWN®

3584

High Voltage OPERATIONAL AMPLIFIER

FEATURES

- TYPICAL GAIN-BANDWIDTH, 50MHz
- OUTPUT, +145V
- PROTECTED OUTPUT, automatic thermal shutoff
- BIAS CURRENT, -20pA
- CMR, 110dB
- SLEW RATE, 150V/μs

APPLICATIONS

- ANALOG SIMULATORS
- DIGITALLY-CONTROLLED POWER SUPPLIES
- CRT DEFLECTION
- ELECTROSTATIC TRANSDUCERS

DESCRIPTION

The 3584 is a high voltage, integrated circuit operational amplifier that will provide up to ±145V output.

The amplifier will provide a gain-bandwidth product of 20MHz minimum, 50MHz typical. The amplifier uses external frequency compensation (one R and one C) so that the user may optimize the bandwidth and slew rate for his particular application.

The amplifier operates over a wide supply range (±70VDC to ±150VDC) and has excellent input characteristics (110dB CMR, 3mV E_{os}, and 25μV/°C E_{os} Drift). The input stage is a FET. The low -20pA bias current minimizes the offset errors caused by the large value resistors normally used in high voltage circuits.

The input stage is protected against overvoltages and the output stage is protected against short circuits to ground. A special thermal sensing circuit helps to prevent damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

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DISCUSSION

The 3584 is a high voltage, integrated circuit operational amplifier. Its ease of use, compact size, and excellent input and output specifications makes it well suited for a wide variety of high voltage and high speed applications.

The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The offset voltage and the drift are laser trimmed. They are low enough so that user trimming will not be required in most applications.

To achieve the high common-mode voltage capability and rejection a true cascode input stage is used together with considerable protection circuitry. There are voltage limiting diodes to prevent damage due to reverse bias breakdown of the input pair and current limiting resistors to limit the steady state input current to 1mA with the inputs at ±150 volts. The units are conservatively rated (and 100% tested) at full rated differential voltage (+150 and -150V) but typically will withstand a 50% overvoltage without damage.

It also has another feature which is important in many high voltage applications. The input bias current is virtually independent of applied common-mode voltage. This is a benefit of the true cascode input stage which keeps the drain to source voltage of the input transistors constant as the common-mode voltage changes.

The amplifier contains automatic thermal sensing and shut-off circuitry which automatically turns the amplifier off when the internal (substrate) temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating all current sources when the temperature reaches a critical level. As this happens, the output current gradually decreases to zero. The output current may remain at a low value or oscillate between 2 values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal condition is removed.

The incorporation of thermal sensing and shut-off in the amplifier will require a smaller heat sink than normal. This is due to the fact that the amplifier will protect itself and does not require a massive heat sink for protection under abnormally high power dissipation.

The 3584 has several other features that improve its utility. The metal case of the unit is completely electrically isolated. This simplifies mounting and reduces cost since the need for insulating spacers is eliminated. The hermetically sealed package improves reliability and will withstand severe environments better. And the small package size reduces weight and makes mounting more convenient.

OPERATION FROM A SINGLE SUPPLY

It may be desirable in some applications to operate the amplifiers from a single supply. The circuit in Figure 1 illustrates a typical application. Note that there are restrictions on the input and output voltages (e_i and e_o) which are necessary in order to keep the amplifier circuits operating in a linear manner.

It should be noted that when the amplifier is operated from a single supply, the output stage, which is still short circuit current limited and thermally protected, is not protected for short circuits to ground under all operating conditions. Consult the safe operating area curve.

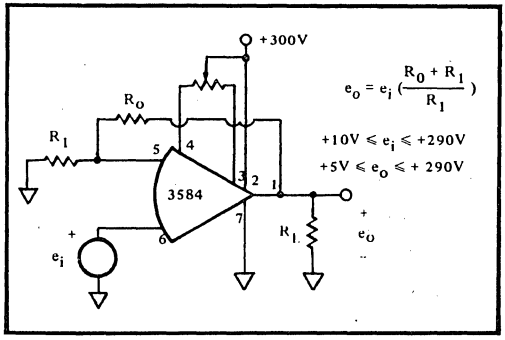


FIGURE 1. Operation from a single supply.

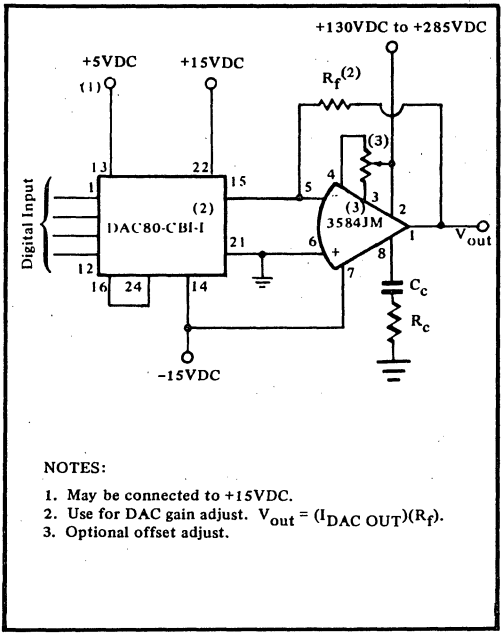


FIGURE 2. High Speed, High Voltage DAC.

SPECIFICATIONS

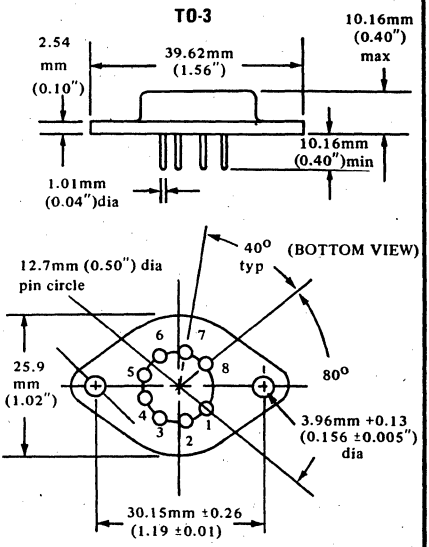
ELECTRICAL

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

MODELS	3584JM
POWER SUPPLY	
Voltage, $\pm V_{cc}$	±70 to ±150 VDC
Quiescent Current, max	±6.5mA
RATED OUTPUT	
Voltage, ± (| V_{cc} | -5)VDC, min	±65 to ±145 VDC
Current, min	±15mA
Current, Short Circuit	±25mA
Load Capacitance, max	10 nF
OPEN LOOP GAIN	
No Load, DC	120 dB
Rated Load, DC, min	100dB
FREQUENCY RESPONSE	
Unity Gain Bandwidth, Small Signal	7 MHz
Gain-bandwidth Product, f = 1 kHz, G = 100	20 MHz, min
Full Power Bandwidth, G = 100	135 kHz
Slew Rate, G = 100	150 V/μs
Settling Time, 0.1%, G = 100	12 μs
INPUT OFFSET VOLTAGE	
Initial @ 25°C, max	3 mV
Drift vs Temp, max	25 μV/°C
Drift vs Supply Voltage	20 μV/V
Drift vs Time	50 μV/mo
INPUT BIAS CURRENT	
Initial @ 25°C, max	-20 pA
Drift vs Temp	doubles every 10°C
Drift vs Supply Voltage	0.2 pA/V
INPUT OFFSET CURRENT	
Initial @ 25°C	±20 pA
Drift vs Temp	doubles every 10°C
Drift vs Supply Voltage	0.2 pA/V
INPUT IMPEDANCE	
Differential	10^{11} Ω ‖ 10 pF
Common Mode	10^{11} Ω
INPUT NOISE	
Voltage 0.01 Hz to 10 Hz p-p	5 μV
10 Hz to 1 kHz rms	1.7 μV
Current 0.01 Hz to 10 Hz p-p	0.3 pA
INPUT VOLTAGE RANGE	
Max Safe Differential Voltage(1)	$(+V_{cc} + \| -V_{cc} \|)$
Max Safe Common Mode Voltage	$+V_{cc}$ to $-V_{cc}$
Common Mode Voltage, Linear Operation	±(| V_{cc} | -10)V
Common Mode Rejection	110dB
TEMPERATURE RANGE (Case)	
Specification:	0°C to 70°C
Operating	-55°C to +125°C
Storage	-55°C to +150°C

(1) The inputs may be damaged by pulses at pins 5 or 6 with $dV/dt \geq 1$ V/ns. Any possible damage can be eliminated by limiting the input current to 150mA with external resistors in series with those pins. No external protection is needed for slower voltage changes.

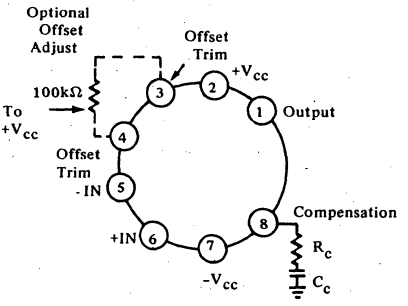
MECHANICAL



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM

(TOP VIEW)



Connector: 0803MC
Heatsinks: 0803HS, 0804HS, or 0805HS

Compensation		
Gain	C_C	R_C
1	10 nF	200Ω
10	500 pF	2kΩ
100	50 pF	20kΩ
1000	not required	

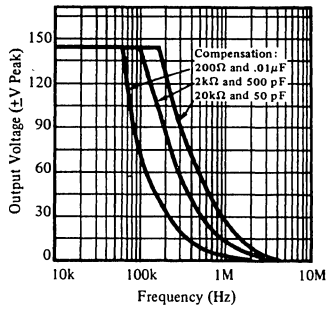
For intermediate values of gain, R and C values may be interpolated.

The case is electrically isolated. It is recommended that the case be grounded during use.

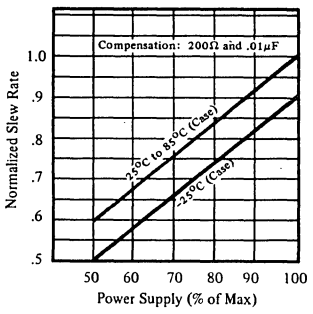
TYPICAL PERFORMANCE CURVES

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

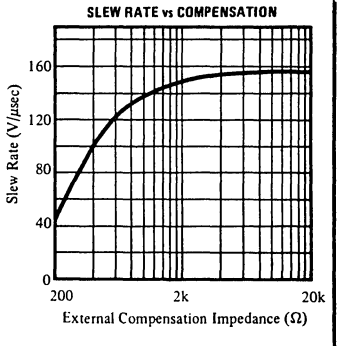
OUTPUT VOLTAGE vs FREQUENCY



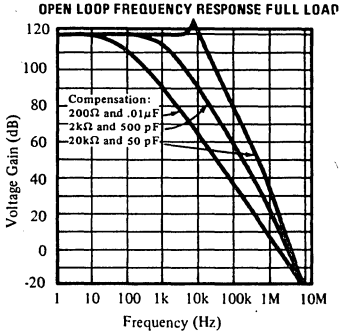
SLEW RATE vs SUPPLY VOLTAGE @ FULL LOAD



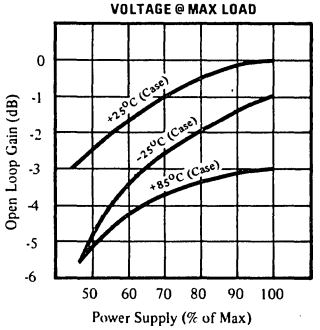
SLEW RATE vs COMPENSATION



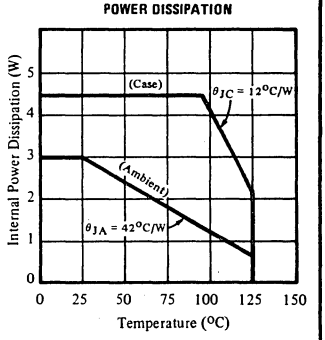
OPEN LOOP FREQUENCY RESPONSE FULL LOAD



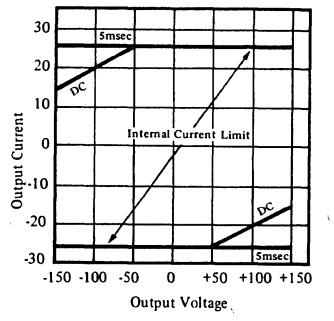
OPEN LOOP GAIN vs SUPPLY VOLTAGE @ MAX LOAD



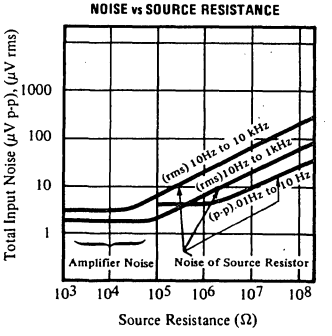
POWER DISSIPATION



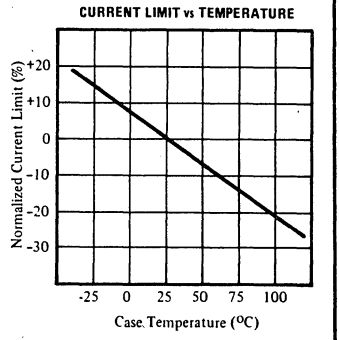
SAFE OPERATING AREA (Secondary Breakdown)



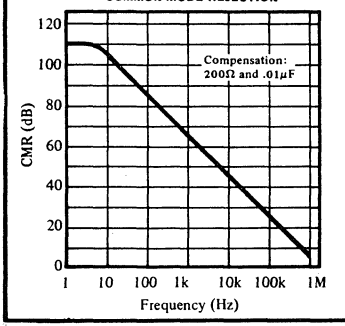
NOISE vs SOURCE RESISTANCE



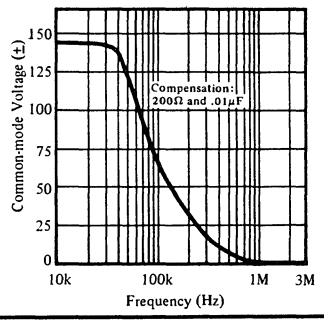
CURRENT LIMIT vs TEMPERATURE



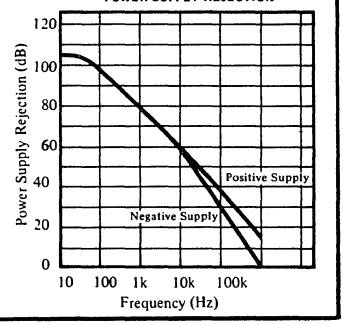
COMMON-MODE REJECTION



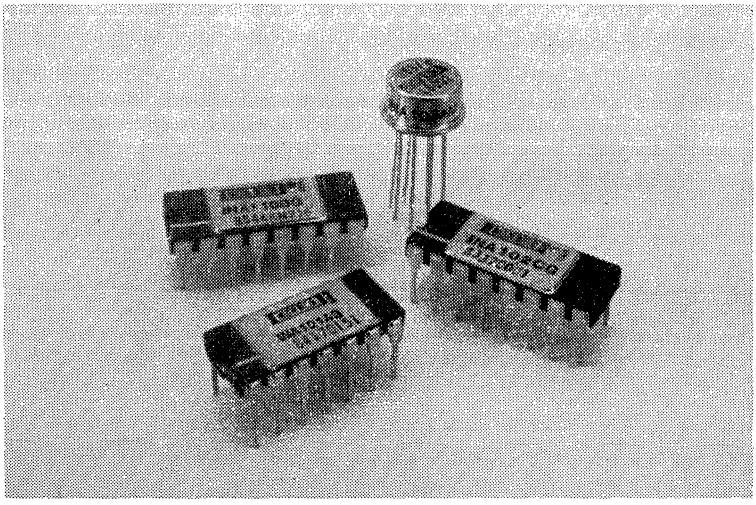
MAXIMUM COMMON-MODE VOLTAGE vs FREQUENCY



POWER SUPPLY REJECTION



INSTRUMENTATION AMPLIFIERS



WHAT IS AN INSTRUMENTATION AMPLIFIER?

An instrumentation amplifier is a closed-loop, differential input gain block. It is a committed circuit with the primary function of accurately amplifying the voltage applied to its inputs.

Ideally, the instrumentation amplifier responds only to the difference between the two input signals and exhibits extremely-high impedances between the two input terminals, and from each terminal to ground. The output voltage is developed single-ended with respect to ground and is equal to the product of amplifier gain and the difference of the two input voltages (see Figure 1).

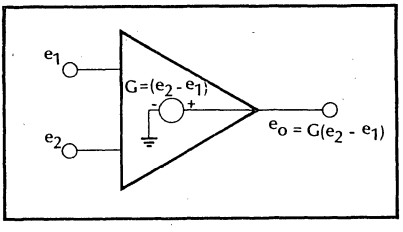


FIGURE 1. Idealized Model of an Instrumentation Amplifier.

The amplifier gain G is normally set by the user with a single external resistor. The properties of this model may be summarized as infinite input impedance, zero output impedance, the output voltage proportional to only the difference voltage ($e_2 - e_1$), a precisely known gain constant (implying no nonlinearity), and unlimited bandwidth. This amplifier would completely reject signal components common to both inputs (common-mode rejection) and would exhibit no DC offset voltage or drift.

CHARACTERISTICS OF INSTRUMENTATION AMPLIFIERS

It is desirable to achieve, as close as possible, the characteristics of the ideal instrumentation amplifier. The following paragraphs are a discussion of the, other-than-ideal, characteristics of the instrumentation amplifiers.

Input Impedance - A simple model of realistic instrumentation amplifier is shown in Figure 2. The impedance Z_{id} represents the differential input impedance. The common-mode input impedance Z_{icm} is represented as two

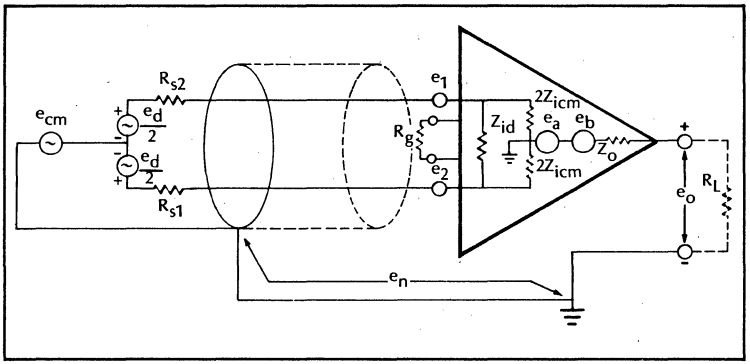


FIGURE 2. Simple Model of an Instrumentation Amplifier Shown in a Typical Application Configuration.

equal components, $2Z_{icm}$, *from each input to ground. These finite resistances contribute an effective gain error due to loading of the source resistance. The instrumentation amplifier provides a load on the source of* $Z_i = Z_{id} \parallel Z_{icm}$. If source impedance is $R_S = R_{s1} + R_{s2}$, the gain error caused by this loading is:

$$\text{Gain Error} = 1 - \frac{Z_i}{Z_i + R_s} = \frac{R_s}{Z_i + R_s} \cong \frac{R_s}{Z_i} \text{ if } Z_i \gg R_s$$

If R_S is 10kΩ and Z_i is 10MΩ,

$$\text{Gain Error} \cong \frac{10 \times 10^3}{10 \times 10^6} = 0.1\%$$

The DC common-mode input impedance Z_{icm} will be independent of gain. The DC differential input impedance Z_{id} may vary as a function of gain. Specifications give the worst-case value. The nonzero output impedance of the amplifier will also create a gain error, the value of which depends on the load resistance.

Nonlinearity - The linearity of gain is possibly of more importance than the gain accuracy, since the value of the gain can be adjusted to compensate for simple gain errors. The nonlinearity is specified to be the peak deviation from a "best fit" straightline, expressed as a percent of peak-to-peak full scale output.

Common-mode Rejection - As illustrated in Figure 2, the output voltage has two components. One component is proportional to the differential input voltage $e_d = (e_2 - e_1)$. The second component is proportional to the common-mode input voltage. The common-mode voltage which appears at the amplifier's input terminals is defined as $E_{cm} = e_2 + e_1/2$. This may consist of some common-mode voltage in the source itself, e_{cm}, (such as bridge excitation) plus any noise voltage, e_n, between the source common and the amplifier common. As shown in Figure 2, the constant G represents the

differential amplifier gain factor (fixed by the external gain-setting resistor). The constant (G/CMRR) represents the commo-mode signal gain of the amplifier. The CMRR (common-mode rejection ratio) is the ratio of differential gain to common-mode gain. Thus CMRR is proportional to the differential gain and CMRR increases as the differential (gain G) increased. Hence, CMRR is usually specified for the maximum and the minimum values of gain of the amplifier. The common-mode rejection may be expressed in dB as - CMRR (dB) = 20 $\log_{10}$ CMRR.

For an ideal instrumentation amplifier the output voltage component due to common-mode voltage should be zero. For a realistic instrumentation amplifier, the CMRR though very high, is still not infinite and so will cause an error voltage of E_{cm}/CMRR x G to appear at the output.

Source Impedance Unbalance - If the source impedances are unbalanced the source voltages ($e_{cm} + e_n$) are divided unequally upon the common-mode impedances and a differential signal is developed at the amplifier's input. This error signal cannot be separated from the desired signal. In the circuit in Figure 2 if $R_{s2} = 0$, $R_{s1} = 1k\Omega$, $e_{cm} + e_n = 10V$, and $Z_{cm} = 100M\Omega$, then the effect of unbalance is to generate a voltage.

$$e_2 - e_1 = 10V - 10V\frac{10^8}{10^8 + 10^3} = 10V\frac{10^3}{10^8 + 10^3} \cong \frac{10V}{10^5} = 0.1mV$$

If e_d full scale is 10mV then this error is:

$$\text{Error} = \frac{0.1mV}{10mV} = 1\% \text{ of full scale.}$$

Offset Voltage and Drift - Most instrumentation amplifiers are two stage devices - they have a variable gain input stage and a fixed gain output stage. If V_i and V_o are the offset voltages of the input and output stages respectively, then the amplifiers total offset voltage referred to the input (RTI) = $V_i + V_o/G$ where G is the amplifier's gain. [Note that E_{os} (RTI) x G.]

The initial offset voltage is usually adjustable to zero and therefore, the voltage drift is the more significant term since it cannot be nulled. The offset voltage drift also has two components - one due to the input stage of the amplifier and the other due to the output stage. When the amplifier is operated at high gain, the drift of the input stage predominates. At low values of gain, the drift of the output stage will be the major component of drift. When the total output drift is referred to the input, the effective input voltage drift is largest for low values of gain. Output voltage drift will always be lowest at low gains. If $\Delta V_i/\Delta T = 2\mu V/^oC$ and $\Delta V_o/\Delta T = 500\mu V/^oC$ and the amplifier in a gain of 1000V/V is nulled at 25°C, then at 65°C the offset voltage will be:

$$E_{os}\,(RTI)_{65^o} = 40^oC\,[2\mu V/^oC + (500\mu V/^oC/1000V/V)]$$
$$= 40^oC\,(2.5\mu V/^oC) = 100\mu V = 0.1mV$$

If the full scale input is 10mV then the error due to voltage drift is:

$$\text{Error} = 0.1mV/10mV = 1\% \text{ of full scale.}$$

Input Bias and Offset Currents - The input bias currents are the currents that flow out of (or into) either of the two inputs of the amplifier. They are the base currents for bipolar input stages and the JFET leakage currents for FET input stage. Offset currents are the difference of the two bias currents.

The bias currents flowing into the source resistances will generate offset voltages of $E_{os2} = 1_{B2} \times R_{s2}$ and $E_{os1} = 1_{B1} \times R_{s1}$. If $R_{s1} = R_{s2} = R_s/2$ the offset voltage at the input is $E_{os2} - E_{os1} = I_{os} \times R_x/2$. This input referred offset error may be compared directly with the input voltage to compute percent error. (Note that the source must be returned to power supply common or R_s will be infinite and the amplifier will saturate.)

APPLICATIONS OF INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are generally used in applications where extracting and accurately amplifying low level differential signals riding on high common-mode voltages (±10V) is very important. Such applications require high input impedance, high CMRR, low input noise, and excellent DC levels stability (low offset voltage drift).

Instrumentation amplifiers are used as transducer amplifiers for various types of transducers such as strain gage bridges, load cells, thermistor networks, thermocouples, current shunts, biological probes, weather gauges and so forth. Other applications include recorder preamplifiers, multiplexer buffers, servo error amplifiers, current sensors, signal conditioners in process control and data acquisition systems, and in general measurements of small differential signals riding on common-mode voltages.

The small size, low cost, and high performance of these amplifiers offer an attractive approach for data acquisition applications, that is, assigning a fixed-gain amplifier to each transducer and locating the amplifier physically near the transducer. This approach largely eliminates common-mode noise pickup problems since a high level signal (rather than a low level transducer signal) is then retransmitted to the data gathering station. The result is a higher signal/noise ratio at the output. Using one amplifier per point may well be more economical, as well as offering better peformance and flexibility, than the approach of using low level multiplexers.

SELECTION GUIDE

INSTRUMENTATION AMPLIFIERS

Description	Model	Gain Range	Gain Accuracy, G = 100, 25°C, max	Gain Drift, G = 100 (ppm/°C)	Non-Linearity, G = 100, max (%)	Input Parameters: CMR, DC to 60Hz, G = 10, 1kΩ Unbal., min (dB)	Input Parameters: Offset Voltage vs Temp, max (μV/°C)	Dynamic Response, G = 100, ±3dB BW (kHz)	Temp Range [1]	Package	Page
Very-High Accuracy	INA104HP	1-1000[2]	0.15	22	±0.007	96	±(2 ± 20/G)	25	Com	DIP	2-26
	INA104JP	1-1000[2]	0.15	22	±0.003	96	±(0.25 ± 10/G)	25	Com	DIP	2-26
	INA104KP	1-1000[2]	0.15	22	±0.003	96	±(0.75 ± 10/G)	25	Com	DIP	2-26
	INA104AM	1-1000[2]	0.15	22[3]	±0.007	96	±(2 ± 20/G)	25	Ind	DIP	2-26
	INA104BM	1-1000[2]	0.15	22[3]	±0.003	96	±(0.75 ± 10/G)	25	Ind	DIP	2-26
	INA104CM	1-1000[2]	0.15	22[3]	±0.003	96	±(0.25 ± 10/G)	25	Ind	DIP	2-26
	INA104SM	1-1000[2]	0.15	22[3]	±0.003	96	±(0.75 ± 10/G)	25	MIL	DIP	2-26
	INA101AM	1-1000[2]	0.03	22[4]	±0.007	96	±(2 + 20/G)	25	Ind	TO-100	2-7
	INA101CM	1-1000[2]	0.03	22[4]	±0.004	96	±(0.25 + 10/G)	25	Ind	TO-100	2-7
	INA101SM	1-1000[2]	0.03	22[4]	±0.004	96	±(0.25 + 10/G)	25	MIL	TO-100	2-7
	INA101AG	1-1000[2]	0.03	22[3]	±0.007	96	±(2 + 20/G)	25	Ind	DIP	2-7
	INA101CG	1-1000[2]	0.03	22[3]	±0.003	96	±(0.25 + 10/G)	25	Ind	DIP	2-7
	INA101SG	1-1000[2]	0.03	22[3]	±0.003	96	±(0.25 + 10/G)	25	MIL	DIP	2-7
	INA101HP	1-1000[2]	0.3	22[3]	±0.007	90dB	±(2 + 20/G) typ	25	Com	DIP	2-7
Low Quiescent Power	INA102AG	1, 10, 100,	0.25	20	±0.05	80	±(5 + 10/G)	3	Ind	DIP	2-18
	INA102CG	1000	0.15	15	±0.02	90	±(2 + 5/G)	3	Ind	DIP	2-18
Fast Settling FET Input	INA110AG	1, 10, 100,	0.2	40	±0.02	87	±(5 + 100/G)	470	Ind	DIP	2-46
	INA110BG	200, 500	0.1	20	±0.01	96	±(2 + 50/G)	470	Ind	DIP	2-46
Buffer, Unity-Gain Differential	3627AM	1V/V, fixed	0.01	5	±0.001[3]	90	30	800[3]	Ind	TO-99	2-122
	3627BM	1V/V, fixed	0.01	5	±0.001[1]	100	20	800[3]	Ind	TO-99	2-122
	INA105AM	1V/V, fixed	0.01	5	±0.01	80	20	1000[3]	Ind	TO-99	2-36
	INA105BM	1V/V, fixed	0.01	5	±0.001	86	10	1000[3]	Ind	TO-99	2-36
	INA105KP	1V/V, fixed	0.01	1[5]	±0.001	72	5[5]	1000[3]	Com	DIP	2-36

PROGRAMMABLE GAIN AMPLIFIERS

Description	Model	Gain Range	Gain Accuracy, G = 100, 25°C, max	Gain Drift, G = 100 (ppm/°C)	Non-Linearity, G = 100, max (%)	Input Parameters: CMR, DC to 60Hz, G = 10, 1kΩ Unbal., min (dB)	Input Parameters: Offset Voltage vs Temp, max (μV/°C)	Dynamic Response, G = 100, ±3dB BW (kHz)	Temp Range [1]	Package	Page
Noninverting Multiplexed Input	PGA100AG	Gain set	0.05	10	±0.01	NA	6[5]	5MHz	Ind	DIP	2-58
	PGA100BG	with 4-bit word 1, 2, 4, 8, . . . 128	0.02	10	±0.005	NA	6[5]	5MHz	Ind	DIP	2-58
	PGA102AG	Gain set	0.02	20	0.01	—	3, G = 100	250	Ind	DIP	2-66
	PGA102BG	with 2-bit	0.01	20	0.01	—	3, G = 100	250	Ind	DIP	2-66
	PGA102SG	word 1, 10	0.01	20	0.01	—	3, G = 100	250	Ind	DIP	2-66
	PGA102KP	100	0.02	50	0.01	—	3, G = 100	250	Com	DIP	2-66
Instrumentation Amplifier Input	PGA200AG	Gain set	0.05	20	±0.007	96	2(G = 100)	30	Ind	DIP	2-76
	PGA200BG	with 2-bit word 1, 10, 100, 1000	0.02	10	±0.003	96	0.4(G = 100)	30	Ind	DIP	2-76
Differential Input	3606AG	Gain set	0.05	10	0.004	90, G = 1	±(3 + 50/G)	40	Ind	DIP	2-114
	3606AM	with 3-bit	0.05	10	0.004	90, G = 1	±(3 + 50/G)	40	Ind	DIP	2-114
	3606BG	word 1, 2, 4	0.02	10	0.004	90, G = 1	±(1 + 20/G)	40	Ind	DIP	2-114
	3606BM	8 . . . 1024	0.02	10	0.004	90, G = 1	±(1 + 20/G)	40	Ind	DIP	2-114

PRECISION TRANSMITTERS

Description	Model	Span: Untrimmed Error, max (%)	Span: Non-Linearity, max (%)	Span: Temp Drift (ppm/°C)	Input Parameters: Offset Voltage, max (μV)	Input Parameters: Offset Voltage vs Temp, max (μV/°C)	Input Parameters: CMR, DC, min (dB)	Output Parameters: Current Range (mA)	Output Parameters: Offset Current Error, max (μA)	Output Parameters: FS Output Current Error, max (μA)	Temp Range [1]	Package	Page
Two-Wire	XTR100AM	−3	0.01	±100	±50	±1	90	4-20	±4	±20	Ind	DIP	2-82
	XTR100AP	−3	0.01	±100	±50	±1	90	4-20	±4	±20	Ind	DIP	2-82
	XTR100BM	−3	0.01	±100	±25	±0.5	90	4-20	±4	±20	Ind	DIP	2-82
	XTR100BP	−3	0.01	±100	±25	±0.5	90	4-20	±4	±20	Ind	DIP	2-82
	XTR101AG	−5	0.01	±100	±60	±1.5	90	4-20	±10	±40	Ind	DIP	2-94
	XTR101BG	−5	0.01	±100	±30	±0.75	90	4-20	±6	±30	Ind	DIP	2-94
Three-Wire and Current Source	XTR110AG	0.6	0.025	50	—	—	—	4-20,	±64	±96	Ind	DIP	2-104
	XTR110BG	0.2	0.005	30	—	—	—	0-20,	±16	±32	Ind	DIP	2-104
	XTR110KP	0.6	0.025	50	—	—	—	5-25 [6]	±64	±96	Com	DIP	2-104

NOTES: (1) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (2) Set with external resistor. (3) Unity-gain. (4) With zero TC external resistor. (5) Typical. (6) Many more ranges with appropriate circuit.

GLOSSARY OF TERMS & DEFINITIONS
Instrumentation Amplifiers

COMMON-MODE INPUT IMPEDANCE
The effective impedance (resistance in parallel with capacitance) between either input of an amplifier and its common, or ground, terminal.

COMMON-MODE REJECTION (CMR)
When both inputs of a differential amplifier experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) which produces the same output change.

$$\text{CMR (in dB)} = 20 \log_{10} \text{CMV/Error Voltage}$$

Thus a CMR of 80dB means that 1V of common-mode voltage will cause an error of 100μV (referred to input).

COMMON-MODE REJECTION RATIO (CMRR)
The ratio of the differential voltage gain of an amplifier to its common-mode voltage gain.

COMMON-MODE VOLTAGE (CMV)
That portion of an input signal which is common to both inputs of a differential amplifier. Mathematically it is defined as the average of the signals at the two inputs:

$$\text{CMV} = e_1 + e_2/2$$

FEEDBACK
The return of a portion of the output signal from a device to the input of the device.

FULL POWER FREQUENCY RESPONSE
The maximum sinewave frequency at which a device can supply its peak-to-peak rated output voltage and current, without introducing significant distortion.

GAIN
The ratio of the output signal to the associated input signal of a device.

GAIN ERROR
The difference between the actual gain of an amplifier and the one predicted by the ideal gain expression.

INPUT BIAS CURRENT
The DC input current required at each input of an amplifier to provide zero output voltage when the input signal and input offset voltage are zero. The specified maximum is for each input.

INPUT BIAS CURRENT DRIFT
The rate of change of input bias current with temperature or time.

INPUT GUARDING
The use of an input shield that is sometimes driven to follow the voltage level of the input signal and, thereby, remove leakage and loss-inducing voltage differences between the input signal path and surrounding stray conduction paths.

INPUT OFFSET CURRENT
The difference of the two input bias currents in a differential amplifier.

INPUT OFFSET VOLTAGE
The DC input voltage required to provide zero voltage at the output of an amplifier when the input signal and input bias currents are zero.

INPUT PROTECTION
A means of protecting an input of a device from damage due to the application of excessive input voltage.

INSTRUMENTATION AMPLIFIER
A closed-loop differential input gain block exhibiting high input impedance and high common-mode rejection. Its primary function is to accurately amplify the voltage applied to its inputs.

NONLINEARITY
The peak deviation from a best straightline (curve fitting on input-output graph) expressed as a percent of peak-to-peak full scale output.

OVERLOAD RECOVERY TIME
The time required for the output of an amplifier to return from saturation to linear operation, following the removal of an input overdrive signal.

SETTLING TIME
The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE
The maximum rate of change of an output voltage when supplying the rated output.

BURR-BROWN®

INA101

Very-High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- ULTRA-LOW VOLTAGE DRIFT - 0.25μV/°C
- LOW OFFSET VOLTAGE - 25μV
- LOW NONLINEARITY - 0.002%
- LOW NOISE - 13nV/$\sqrt{Hz}$ at f_0 = 1kHz
- HIGH CMR - 106dB at 60Hz
- HIGH INPUT IMPEDANCE - $10^{10}\Omega$
- LOW COST, TO-100, CERAMIC DIP AND PLASTIC PACKAGE

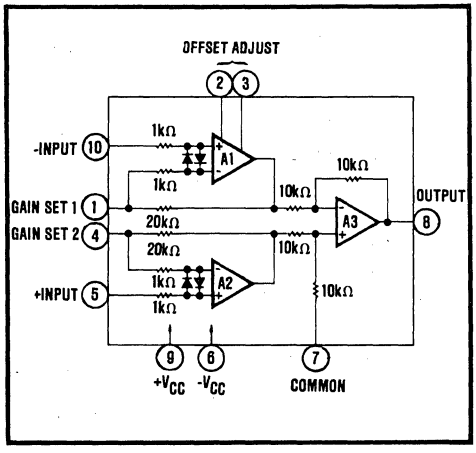
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gages
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS
- MEDICAL INSTRUMENTATION

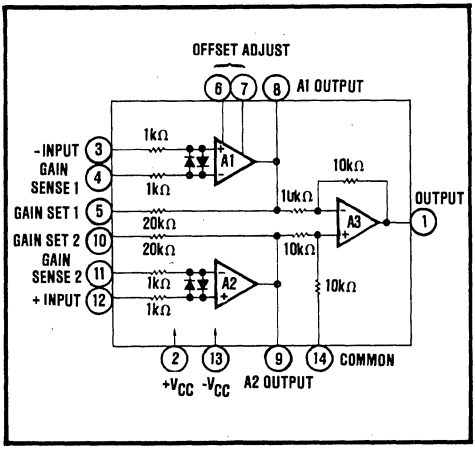
DESCRIPTION

The INA101 is a high accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very-high performance is desired. All circuits, including the interconnected laser-trimmed thin-film resistors, are integrated on a single monolithic substrate.

A multiamplifier design is used to provide the highest performance and maximum versatility with monolithic construction for low cost. The input stage uses Burr-Brown's ultra-low drift, low noise technology to provide exceptional input characteristics.



M Package



G and P Packages

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

MODEL	INA101AM/AG			INA101SM/SG			INA101CM/CG			INA101HP			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN													
Range of Gain	1		1000	*		*	*		*	*	*	*	V/V
Gain Equation		G=1+(40k/R_G)			*			*			*		V/V
Error From Equation, DC[1]		±(0.04+0.00016 −0.02/G)	±(0.1+0.0003G −0.05/G)		*	*		*	*		±(0.1+ 0.00015G) −0.05/G	±(0.3+ 0.0002G) −0.10/G	%
Gain Temp. Coefficient[3]													
G = 1		2	5		*	*		*	*		*	*	ppm/°C
G = 10		20	100		*	*		10	*		*	*	ppm/°C
G = 100		22	110		*	*		11	*		*	*	ppm/°C
G = 1000		22	110		*	*		11	*		*	*	ppm/°C
Nonlinearity, DC[2]		±(0.002+10^{-5}G)	±(0.005+2×10^{-5}G)		±(0.001 +10^{-5}G)	±(0.002 +10^{-5}G)		±(0.001 +10^{-5}G)	±(0.002 +10^{-5}G)		*	*	% of p-p FS
RATED OUTPUT													
Voltage	±10	±12.5		*	*		*	*		*	*		V
Current	±5	±10		*	*		*	*		*	*		mA
Output Impedance		0.2			*			*			*		Ω
Capacitive Load		1000			*			*			*		pF
INPUT OFFSET VOLTAGE													
Initial Offset at +25°C		±(25+200/G)	±(50+400/G)		±(10+ 100/G)	±(25 +200/G)		±(10+ 100/G)	±(25+ 200/G)		±(125+ 450/G)	±(250+ 900/G)	μV
vs Temperature			±(2+20/G)			±(0.75 +10/G)			±(0.25+ 10/G)		±(2+20/G)		μV/°C
vs Supply		±(1+20/G)			*			*			*		μV/V
vs Time		±(1+20/G)			*			*			*		μV/mo
INPUT BIAS CURRENT													
Initial Bias Current (each input)		±15	±30		±10	*		±5	±20		*	*	nA
vs Temperature		±0.2			*			*			*		nA/°C
vs Supply		±0.1			*			*			*		nA/V
Initial Offset Current		±15	±30		±10	*		±5	±20		*	*	nA
vs Temperature		±0.5			*			*			*		nA/°C
INPUT IMPEDANCE													
Differential		10^{10}||3			*			*			*		Ω||pF
Common-mode		10^{10}||3			*			*			*		Ω||pF
INPUT VOLTAGE RANGE													
Range, Linear Response	±10	±12		*	*		*	*		*	*		V
CMR with 1kΩ Source Imbal.													
DC to 60Hz, G=1	80	90		*	*		*	*		65	85		dB
DC to 60Hz, G=10	96	106		*	*		*	*		90	95		dB
DC to 60Hz, G=100 to 1000	106	110		*	*		*	*		100	105		dB
INPUT NOISE													
Input Voltage Noise													
f_B=0.01Hz to 10Hz		0.8			*			*			*		μV, p-p
Density, G=1000													
f_O=10Hz		18			*			*			*		nV/√Hz
f_O=100Hz		15			*			*			*		nV/√Hz
f_O=1kHz		13			*			*			*		nV/√Hz
Input Current Noise													
f_B=0.01Hz to 10Hz		50			*			*			*		pA, p-p
Density													
f_O=10Hz		0.8			*			*			*		pA/√Hz
f_O=100Hz		0.46			*			*			*		pA/√Hz
f_O=1kHz		0.35			*			*			*		pA/√Hz
DYNAMIC RESPONSE													
Small Signal, ±3dB Flatness													
G = 1		300			*			*			*		kHz
G = 10		140			*			*			*		kHz
G = 100		25			*			*			*		kHz
G = 1000		2.5			*			*			*		kHz
Small Signal, ±1% Flatness													
G = 1		20			*			*			*		kHz
G = 10		10			*			*			*		kHz
G = 100		1			*			*			*		kHz
G = 1000		200			*			*			*		Hz
Full Power, G=1 to 100		6.4			*			*			*		kHz
Slew Rate, G=1 to 100	0.2	0.4		*	*		*	*		*	*		V/μs
Settling Time (0.1%)													
G = 1		30	40		*	*		*	*		*	*	μs
G = 100		40	55		*	*		*	*		*	*	μs
G = 1000		350	470		*	*		*	*		*	*	μs
Settling Time (0.01%)													
G = 1		30	45		*	*		*	*		*	*	μs
G = 100		50	70		*	*		*	*		*	*	μs
G = 1000		500	650		*	*		*	*		*	*	μs
POWER SUPPLY													
Rated Voltage		±15			*			*			*		V
Voltage Range	±5		±20	*		*	*		*	*		*	V
Current, Quiescent[2]		±6.7	±8.5		*	*		*	*		*	*	mA
TEMPERATURE RANGE[5]													
Specification	−25		+85	−55		+125	*		*		0	+70	°C
Operation	−55		+125	*		*	*		*		−25	+85	°C
Storage	−65		+150	*		*	*		*		−40	+85	°C

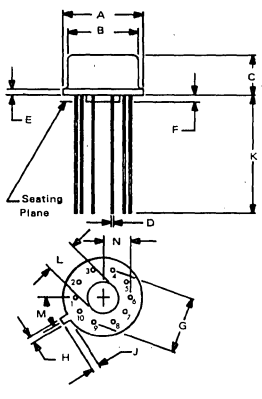
* Specifications same as for INA101AM/AG.

NOTES: (1) Typically the tolerance of R_G will be the major source of gain error. (2) Nonlinearity is the maximum peak deviation from the best straight-line as a percentage of peak-to-peak full scale output. (3) Not including the TCR of R_G. (4) Adjustable to zero at any one gain. (5) θ_{JC} output stage = 113°C/W, θ_{JC} quiescent circuitry = 19°C/W, θ_{CA} = 83°C/W.

MECHANICAL

M Package

TO-100



BOTTOM VIEW

Case = $-V_{CC}$

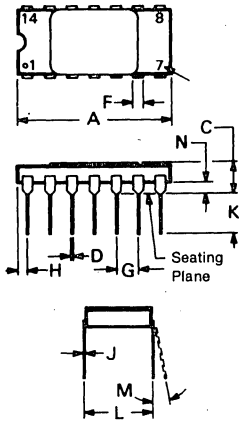
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

G Package

Hermetic DIP



Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.009	.060	0.23	1.52

ORDERING INFORMATION

INA101 C G

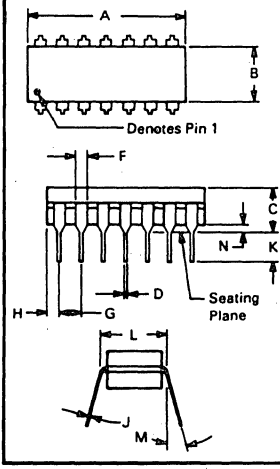
Basic Model Number

Performance Grade Code
- S: −55°C to +125°C
- A, C: −25°C to +85°C
- H: 0°C to +70°C

Package Code
- M: TO-100
- G: 14-Pin Hermetic DIP
- P: 14-Pin Plastic DIP

TO-100 (M Suffix)	Hermetic DIP (G Suffix)	Plastic DIP (P Suffix)
INA101AM	INA101AG	INA101HP
INA101CM	INA101CG	
INA101SM	INA101SG	

P Package



Case = $-V_{CC}$

Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

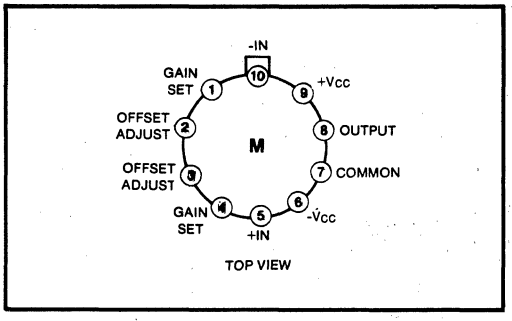
Pin numbers shown for reference only. Numbers may not be marked on package.

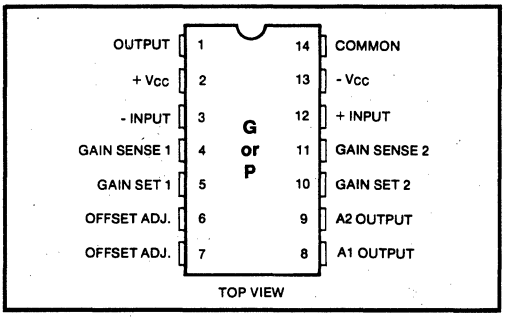
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.660	.785	16.76	19.94
B	.220	.280	5.59	7.11
C	–	.200	–	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095		
J	.008	.015	0.20	0.38
K	.100	–	2.54	–
L	.300 BASIC		7.62 BASIC	
M	–	15°	–	15°
N	.020	.050	0.51	1.27

ABSOLUTE MAXIMUM RATINGS

Supply	±20V
Internal Power Dissipation	600mW
Input Voltage Range	$\pm V_{CC}$
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range:	
M, G	−65°C to +150°C
P	−40°C to +85°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration	Continuous to ground

PIN CONFIGURATION

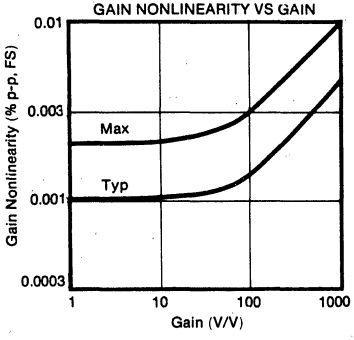




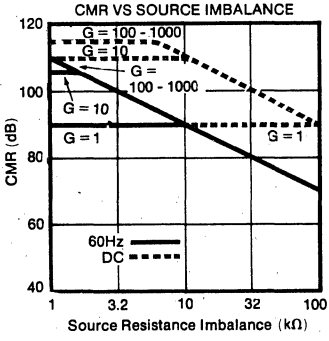
TYPICAL PERFORMANCE CURVES

At +25°C and in circuit of Figure 2 unless otherwise noted.

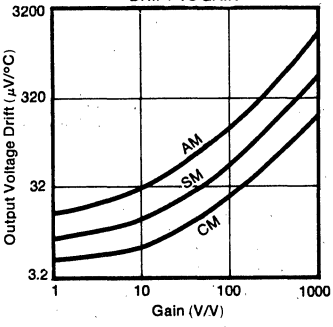
GAIN NONLINEARITY VS GAIN



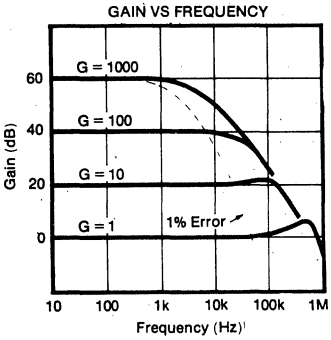
CMR VS SOURCE IMBALANCE



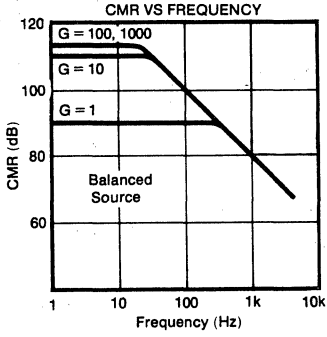
TOTAL OFFSET VOLTAGE DRIFT VS GAIN



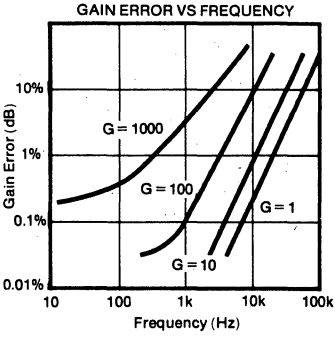
GAIN VS FREQUENCY



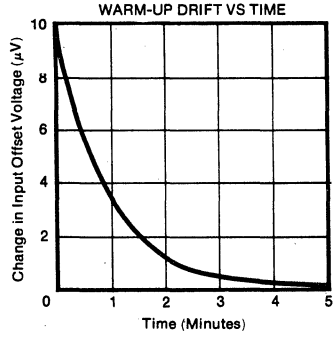
CMR VS FREQUENCY



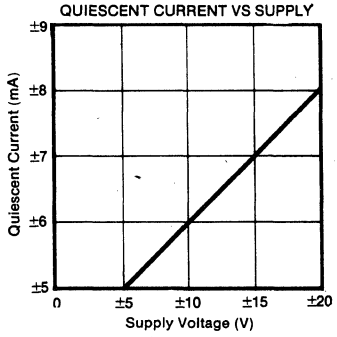
GAIN ERROR VS FREQUENCY



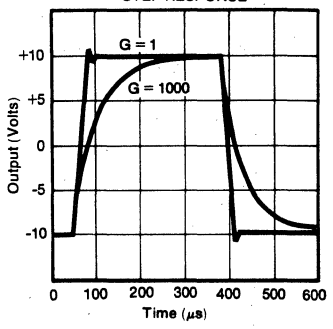
WARM-UP DRIFT VS TIME

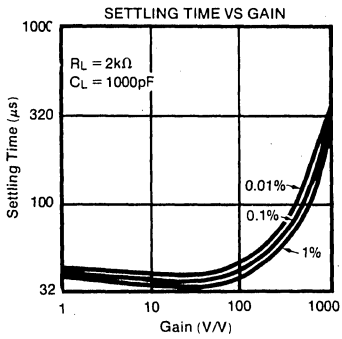


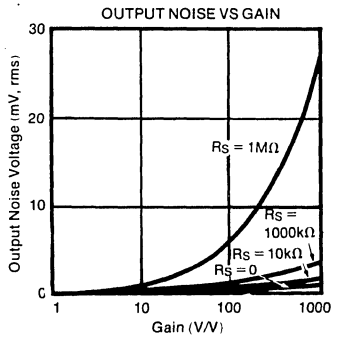
QUIESCENT CURRENT VS SUPPLY

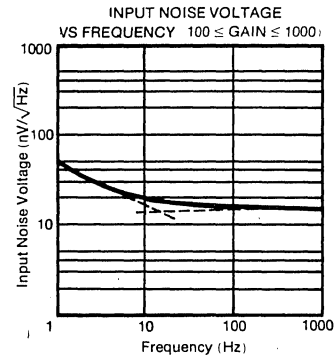


STEP RESPONSE









DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely-high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems.

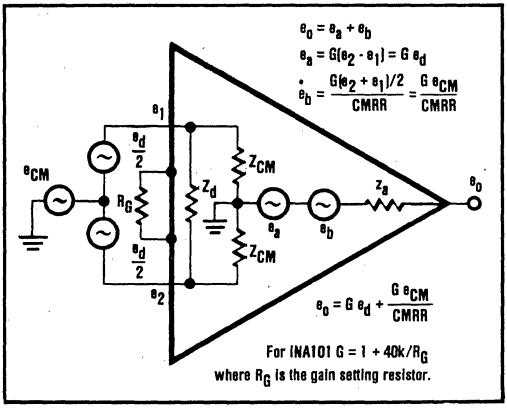


FIGURE 1. Model of an Instrumentation Amplifier.

THE INA101

Simplified schematics of the INA101 are shown on the first page. It is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found in integrated circuit instrumentation amplifiers.

The input section (A1 and A2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature is low due to the monolithic design and improved even further by the state-of-the-art laser-trimming techniques.

The output section (A3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the internal resistors are compatible thin-film nichrome formed with the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability of trimmed resistors and simultaneous achievement of excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA101 is operated over wide temperature ranges.

USING THE INA101

Figure 2 shows the simplest configuration of the INA101. The gain is set by the external resistor, R_G, with a gain equation of $G = 1 + (40K/R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

For gains greater than unity, resistor R_G is connected externally between pins 1 and 4. At high gains where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

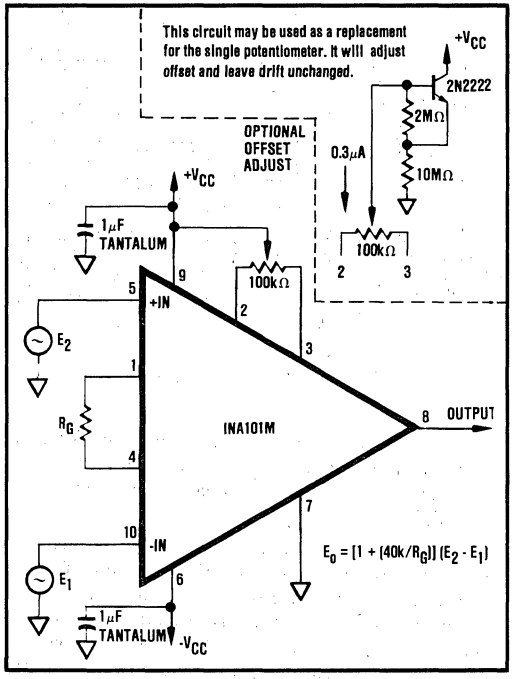


FIGURE 2. Basic Circuit Connection for the INA101 Including Optional Input Offset Null Potentiometer.

The optional offset null capability is shown in Figure 2. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately $0.31\mu V/°C$ per $100\mu V$ of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offsetting can be accomplished in Figure 3 by applying a voltage to Common (pin 7) through a buffer amplifier. This limits the resistance in series with pin 7 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 106dB. Be certain to keep this resistance low.

It is important to not exceed the input amplifiers' dynamic range. The amplified differential input signal and its associated common-mode voltage should not cause the output of A_1 or A_2 to exceed approximately ±10V or nonlinear operation will result.

BASIC CIRCUIT CONNECTION

The basic circuit connection for the INA101 is shown in Figure 2. The output voltage is a function of the differential input voltage times the gain.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is frequently desirable to null the input component of offset (Figure 2) and occasionally that of the output (Figure 3). The quality of the potentiometer will affect the results, therefore, choose one with good temperature and mechanical-resistance stability. The procedure is as follows:

1. Set $E_1 = E_2 = 0V$ (be sure a good ground return path exists to the input).
2. Set the gain to the desired value by choosing R_G.
3. Adjust to 100kΩ potentiometer in Figure 2 until the output reads 0V ±1mV or desired setting. Note that the offset will change when the gain is changed. If the output component of offset is to be removed or if it is desired to establish an intentional offset, adjust the 100kΩ potentiometer in Figure 3 until the output reads 0V ±1mV or desired setting. Note that the offset will not change with gain, but be sure to use a stable external amplifier with good DC characteristics. The range of adjustment is ±15mV as shown. For larger ranges change the ratio of R_1 to R_2.

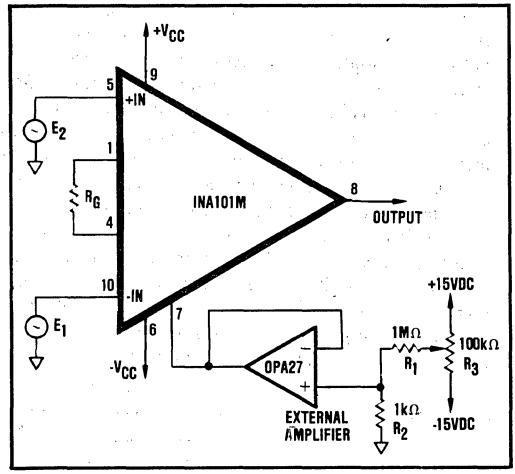


FIGURE 3. Optional Output Offset Nulling or Offsetting Using External Amplifier (Low Impedance to Pin 7).

THERMAL EFFECTS ON OFFSET

To maintain specified offset performance, especially in high gain, prevent air currents from circulating around the input pins. This can be done by using a skirted heat sink on the INA101M package. Rapid changes in die temperature and thermocouple effects on the pins will then be minimized. Surrounding the package with low power components will also help to reduce air flow across the package and pins.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low level differential signals from

bridges and transducers such as strain gages, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA101 accomplishes all of these with high precision.

Figures 4 through 16 show some typical applications circuits.

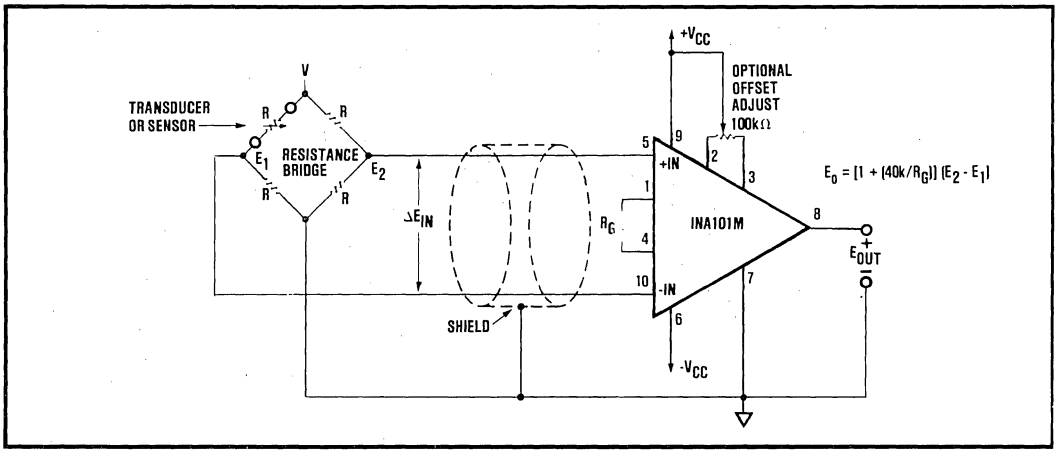


FIGURE 4. Amplification of a Differential Voltage from a Resistance Bridge.

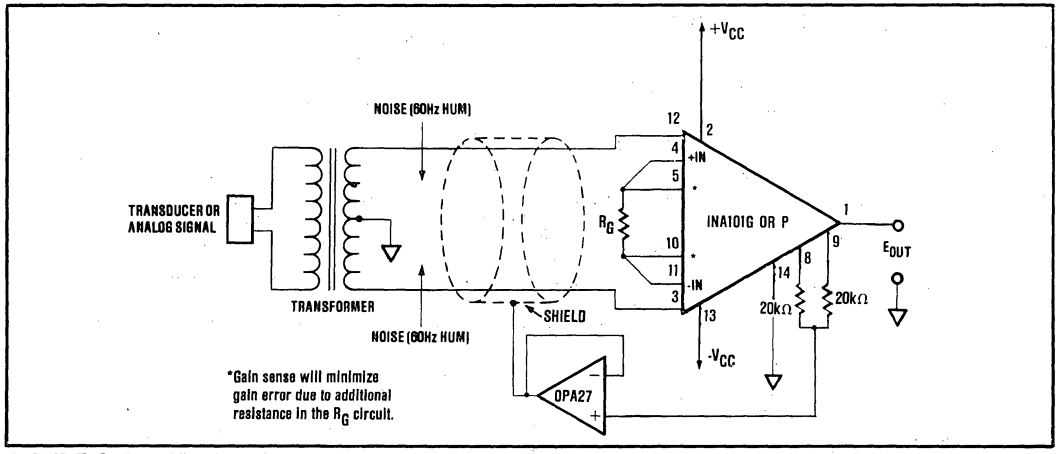


FIGURE 5. Amplification of a Transformer-Coupled Analog Signal.

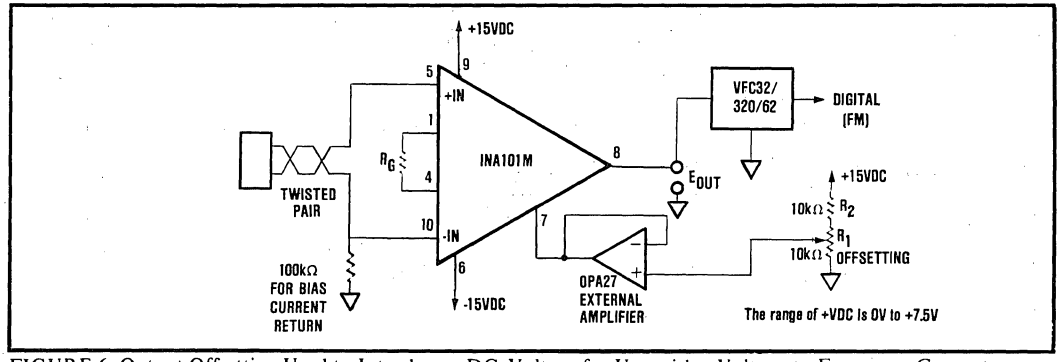


FIGURE 6. Output Offsetting Used to Introduce a DC Voltage for Use with a Voltage-to-Frequency Converter.

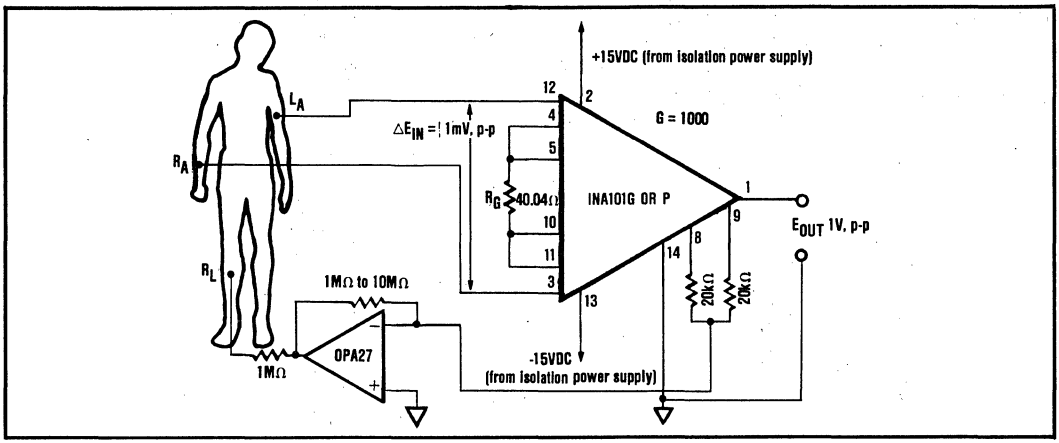


FIGURE 7. ECG Amplifier or Recorder Preamp for Biological Signals.

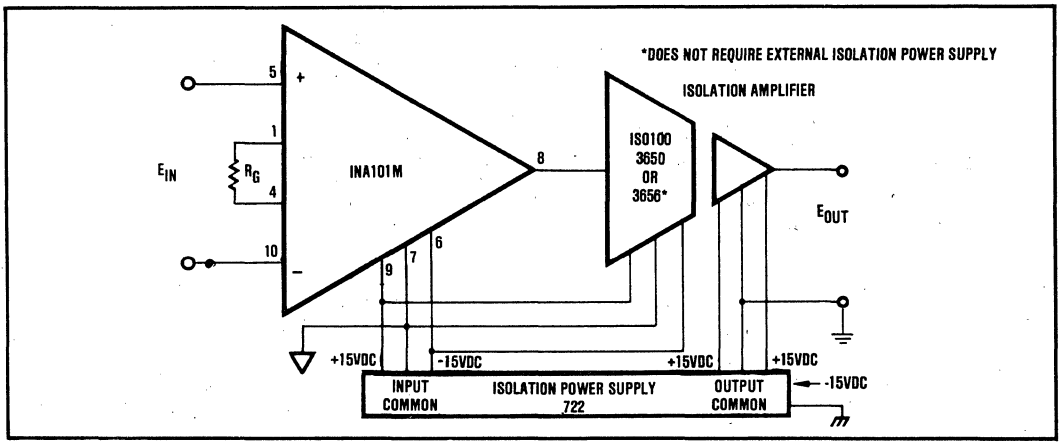


FIGURE 8. Precision Isolated Instrumentation Amplifier.

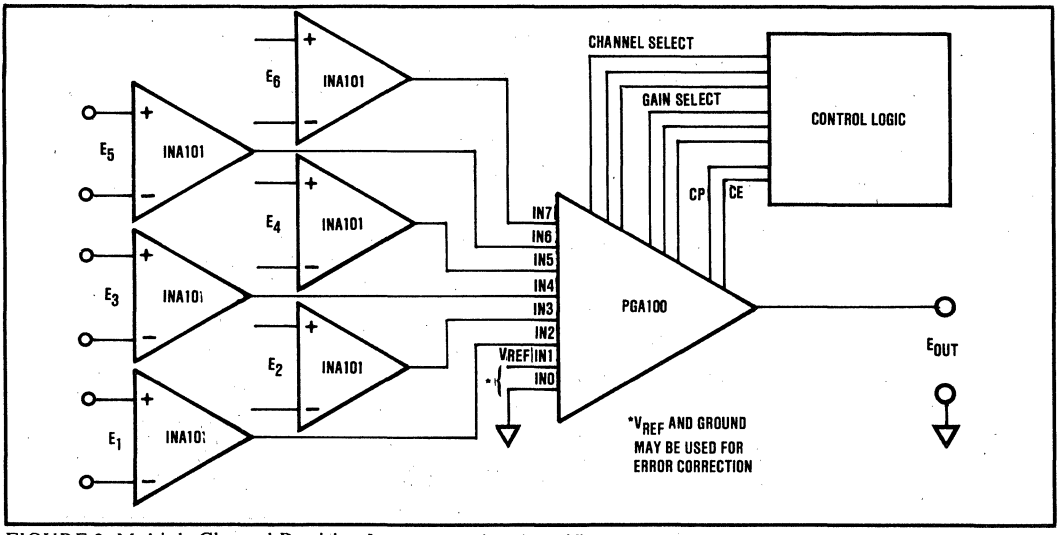


FIGURE 9. Multiple Channel Precision Instrumentation Amplifier.

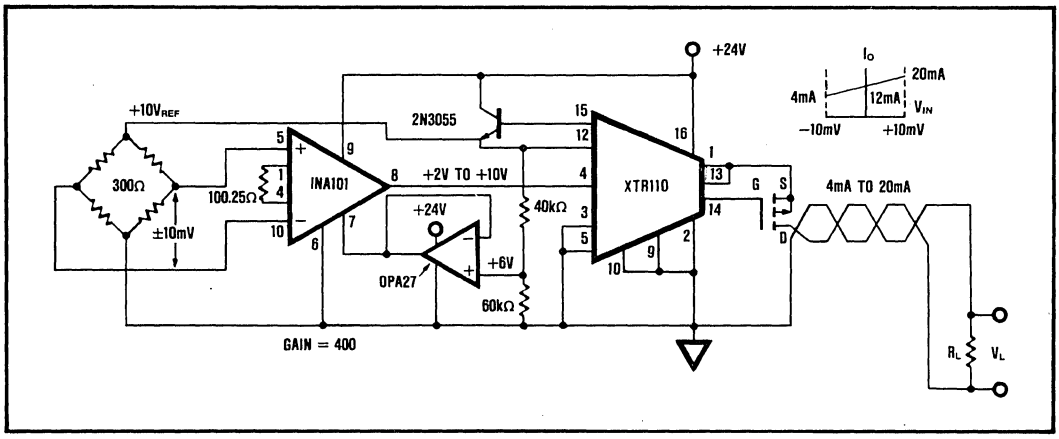


FIGURE 10. 4mA to 20mA Bridge Transmitter Using Single Supply Instrumentation Amplifier.

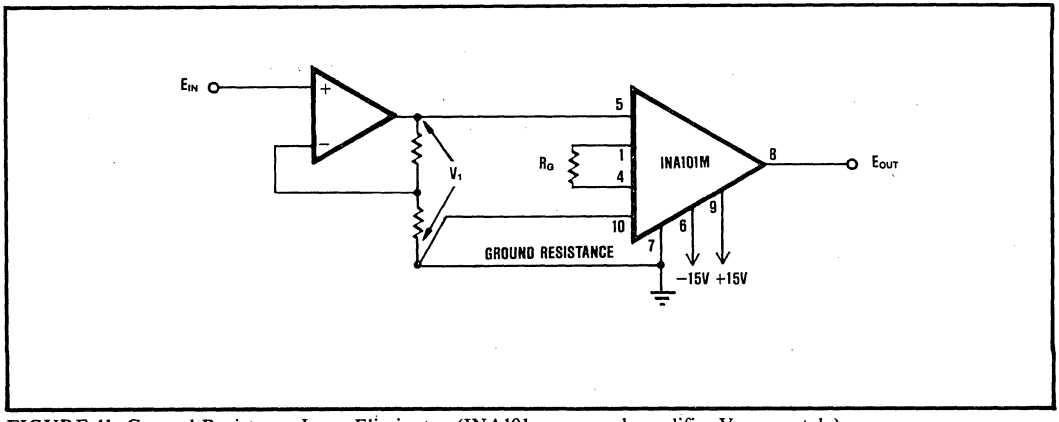


FIGURE 11. Ground Resistance Loop Eliminator (INA101 senses and amplifies V_1 accurately).

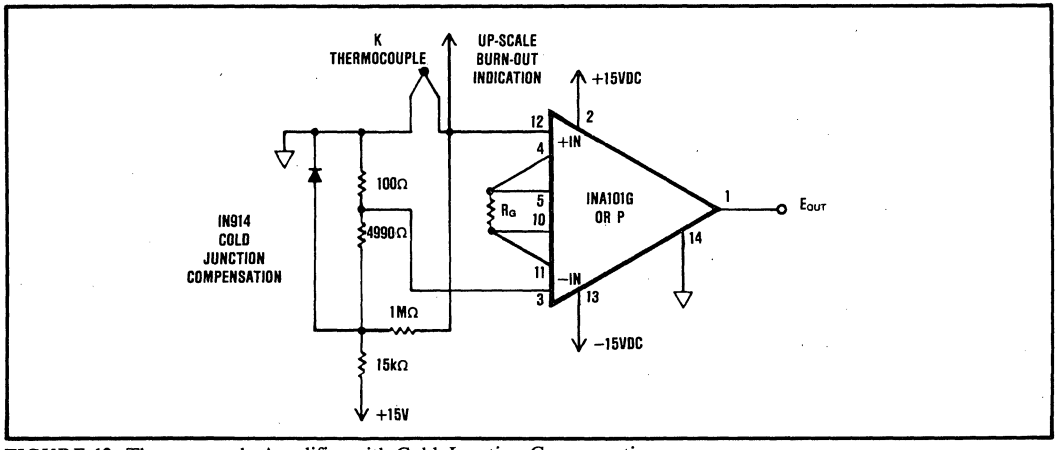


FIGURE 12. Thermocouple Amplifier with Cold Junction Compensation.

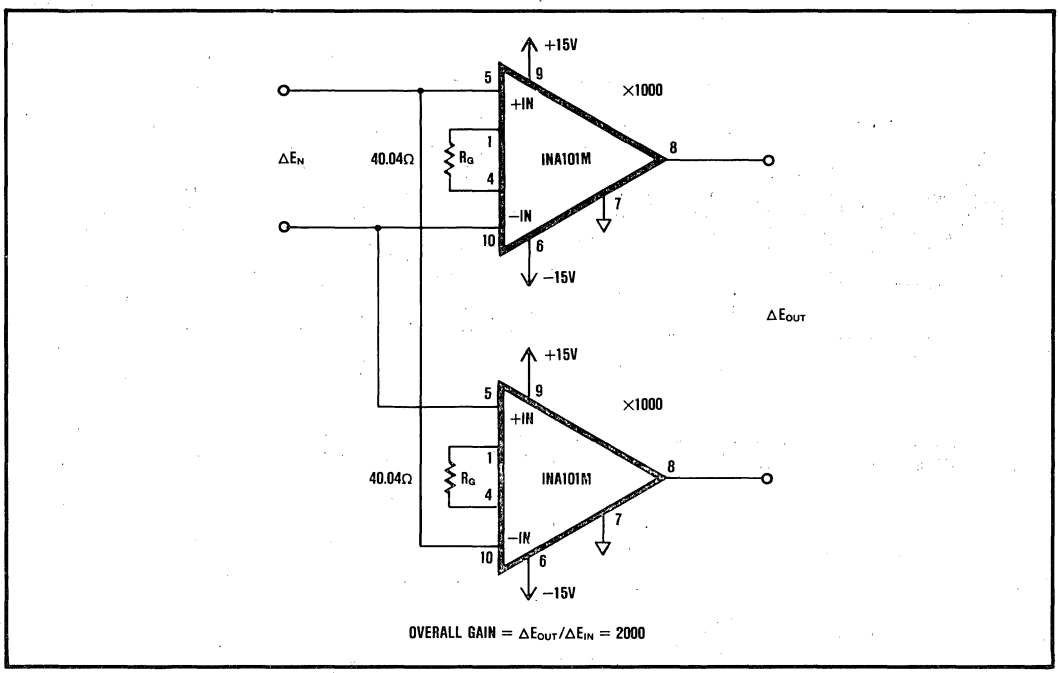
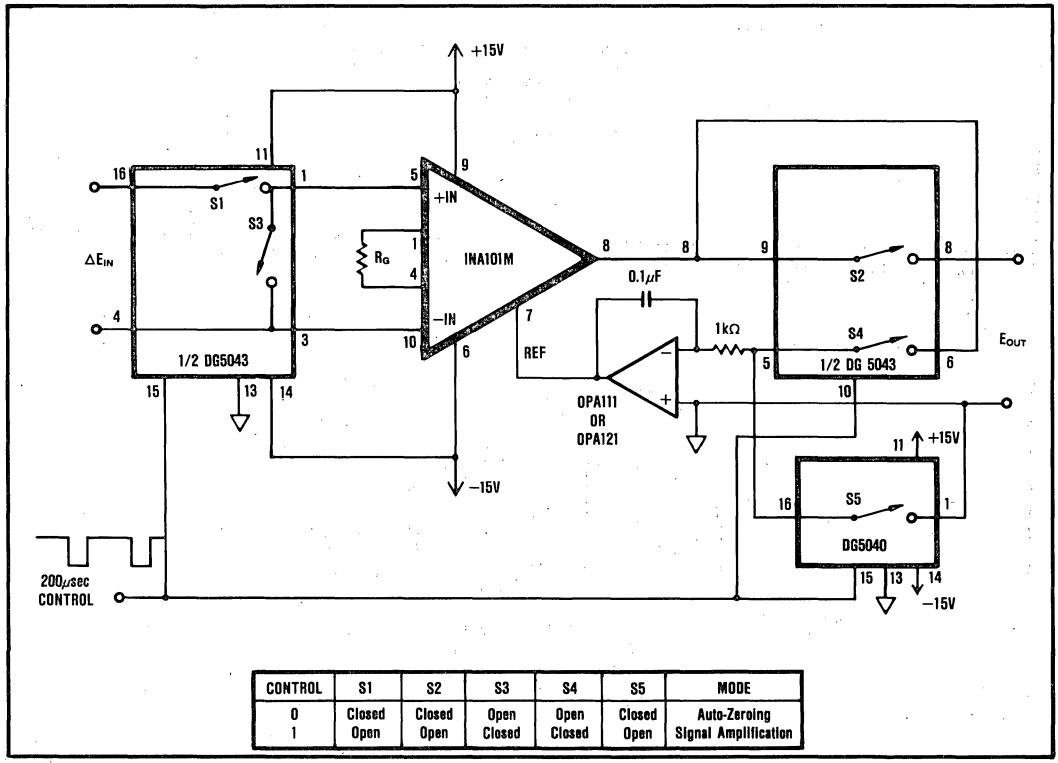


FIGURE 13. Differential Input/Differential Output Amplifier (twice the gain of one INA).



CONTROL	S1	S2	S3	S4	S5	MODE
0	Closed	Closed	Open	Open	Closed	Auto-Zeroing
1	Open	Open	Closed	Closed	Open	Signal Amplification

FIGURE 14. Auto-Zeroing Instrumentation Amplifier Circuit.

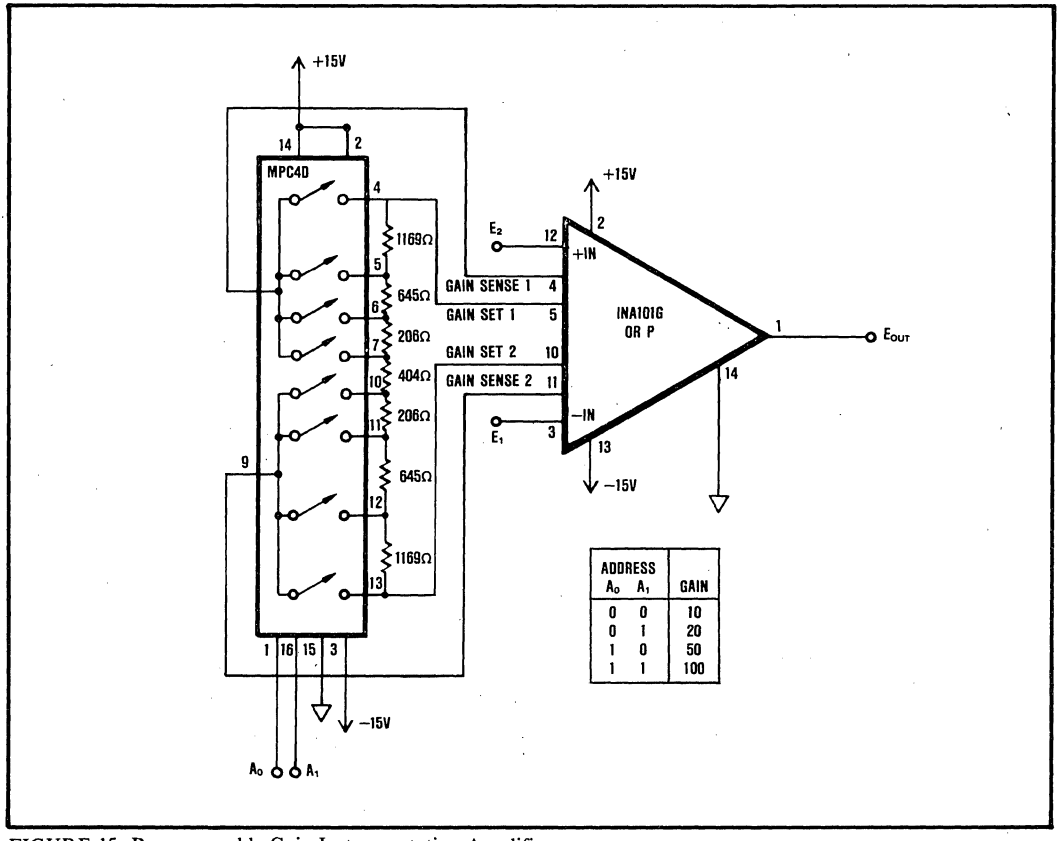


FIGURE 15. Programmable Gain Instrumentation Amplifier.

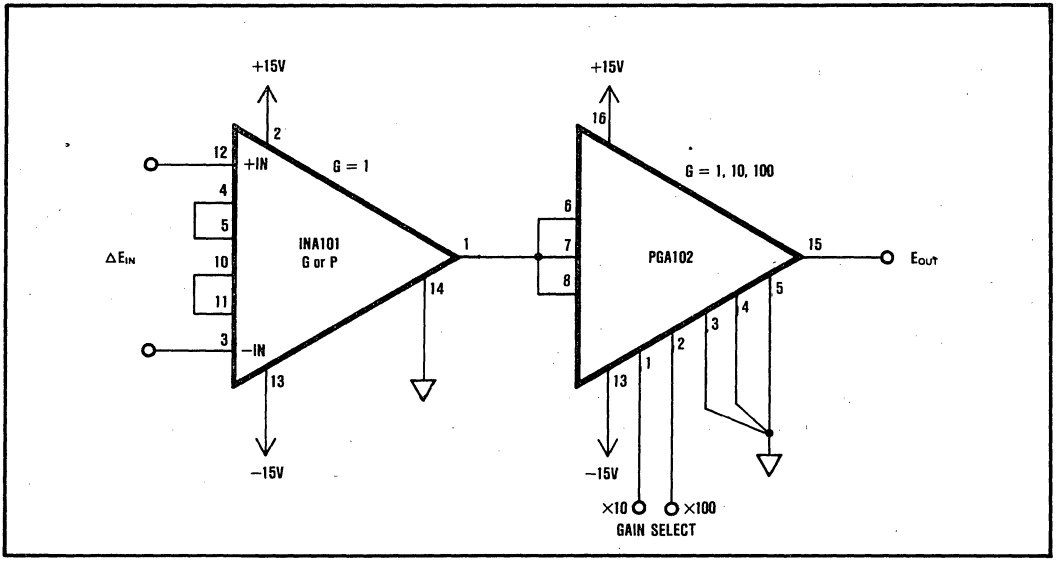


FIGURE 16. Programmable-Gain Instrumentation Amplifier Using the INA101 and PGA102.

BURR-BROWN®

INA102

Low Power
High Accuracy
INSTRUMENTATION AMPLIFIER

FEATURES

- LOW QUIESCENT CURRENT: 750μA, max
- INTERNAL GAINS: X 1, 10, 100, 1000
- LOW GAIN DRIFT: 5ppm/°C, max
- HIGH CMR: 90dB, min
- LOW OFFSET VOLTAGE DRIFT: 2μV/°C, max
- LOW OFFSET VOLTAGE: 100μV, max
- LOW NONLINEARITY: 0.01%, max
- HIGH INPUT IMPEDANCE: $10^{10}\Omega$
- LOW COST

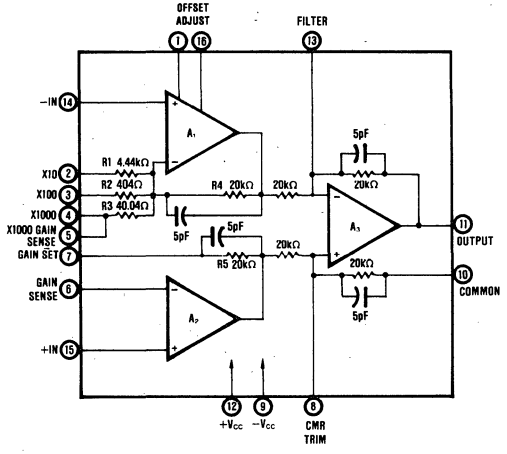
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gauges
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCER AMPLIFIER
- LOW LEVEL SIGNAL AMPLIFIER
- MEDICAL INSTRUMENTATION
- MULTICHANNEL SYSTEMS
- BATTERY POWERED EQUIPMENT

DESCRIPTION

The INA102 is a high-accuracy monolithic instrumentation amplifier designed for signal conditioning applications where low quiescent power is desired. On-chip thin-film resistors provide excellent temperature and stability performance. State-of-the-art laser trimming technology insures high gain accuracy and common-mode rejection while avoiding expensive external components. These features make the INA102 ideally suited for battery powered and high volume applications.

The INA102 is also convenient to use. A gain of 1, 10, 100, or 1000 may be selected by simply strapping the appropriate pins together. 5ppm/°C gain drift in low gains can then be achieved without external adjustment. When higher than specified CMR is required, CMR can be trimmed using the pins provided. In addition, balanced filtering can be accomplished in the output stage.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

MODEL		INA102AG			INA102CG			
	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN								
Range of Gain	−10V ≦ V_o ≦ +10V	1		1000	*		*	V/V
Gain Equation,			G = 1 +					
External, ±20%			(40k/R_G)[1]			*		V/V
Error, DC: G = 1	T_A = +25°C			0.1			0.05	%
G = 10	T_A = +25°C			0.1			0.05	%
G = 100	T_A = +25°C			0.25			0.15	%
G = 1000	T_A = +25°C			0.75			0.5	%
G = 1	T_A = T_{MIN} to T_{MAX}			0.16			0.08	%
G = 10	T_A = T_{MIN} to T_{MAX}			0.19			0.11	%
G = 100	T_A = T_{MIN} to T_{MAX}			0.37			0.21	%
G = 1000	T_A = T_{MIN} to T_{MAX}			0.93			0.62	%
Gain Temp. Coefficient								
G = 1				10			5	ppm/°C
G = 10				15			10	ppm/°C
G = 100				20			15	ppm/°C
G = 1000				30			20	ppm/°C
Nonlinearity, DC								
G = 1	T_A = +25°C			0.03			0.01	% of FS
G = 10	T_A = +25°C			0.03			0.01	% of FS
G = 100	T_A = +25°C			0.05			0.02	% of FS
G = 1000	T_A = +25°C			0.1			0.05	% of FS
G = 1	T_A = T_{MIN} to T_{MAX}			0.045			0.015	% of FS
G = 10	T_A = T_{MIN} to T_{MAX}			0.045			0.015	% of FS
G = 100	T_A = T_{MIN} to T_{MAX}			0.075			0.03	% of FS
G = 1000	T_A = T_{MIN} to T_{MAX}			0.15			0.1	% of FS
RATED OUTPUT								
Voltage	R_L = 10kΩ	±(|V_{CC}|−2.5)			*	*		V
Current		±1			*			mA
Short-Circuit Current			2			*		mA
Output Impedance								
G = 1000			0.1			*		Ω
INPUT								
OFFSET VOLTAGE								
Initial Offset[2]	T_A = +25°C			±300 ±300/G			±100 ±200/G	μV
vs Temperature				±5 ±10/G			±2 ±5/G	μV/°C
vs Supply				±40 ±50/G			±10 ±20/G	μV/V
vs Time			±(20 + 30/G)			*		μV/mo
BIAS CURRENT								
Initial Bias Current								
(each input)	T_A = T_{MIN} to T_{MAX}		±25	50		6	30	nA
vs Temperature			±0.1			*		nA/°C
vs Supply			±0.1			*		nA/V
Initial Offset Current	T_A = T_{MIN} to T_{MAX}		±2.5	±15		±2.5	±10	nA
vs Temperature			±0.1			*		nA/°C
IMPEDANCE								
Differential			10^{10}||2			*		Ω || pF
Common-mode			10^{10}||2			*		Ω || pF
VOLTAGE RANGE								
Range, Linear Response	T_A = +25°C	±(|V_{CC}|−2.5)			*			V
CMR with 1kΩ								
Source Imbalance								
G = 1	DC to 60 Hz	80	94		90	94		dB
G = 10	DC to 60 Hz	80	100		90	100		dB
G = 10 to 1000	DC to 60 Hz	80	100		90	100		dB
NOISE								
Input Voltage Noise								
f_B = 0.01Hz to 10Hz			0.1			*		μV, p-p
Density, G = 1000								
f_O = 10Hz			30			*		nV/√Hz
f_O = 100Hz			25			*		nV/√Hz
f_O = 1kHz			25			*		nV/√Hz
Input Current Noise								
f_B = 0.01Hz to 10Hz			25			*		pA p-p
Density: f_O = 10Hz			0.3			*		pA/√Hz
f_O = 100Hz			0.2			*		pA/√Hz
f_O = 1kHz			0.15			*		pA/√Hz
DYNAMIC RESPONSE								
Small Signal								
±3dB Flatness	V_{OUT} = 0.1V_{RMS}							
G = 1			300			*		kHz
G = 10			30			*		kHz
G = 100			3			*		kHz
G = 1000			0.3			*		kHz

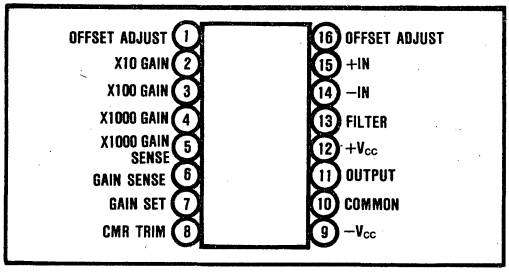
ELECTRICAL (CONT)

MODEL	CONDITIONS	INA102AG			INA102CG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Small Signal, ±1% Flatness	V_{OUT} = 0.1V_{RMS}							
G = 1			30			*		kHz
G = 10			3			*		kHz
G = 100			0.3			*		kHz
G = 1000			0.03			*		kHz
Full Power, G = 1 to 100	V_{OUT}=10V, R_L=10kΩ	2.4	3		*			kHz
Slew Rate, G = 1 to 100	V_{OUT}=10V, R_L=10kΩ	0.15	0.2		*			V/μsec
Settling Time	R_L=10kΩ, C_L=100pF							
0.1%: G = 1	10V step		50			*		μsec
G = 100			360			*		μsec
G = 1000			3300			*		μsec
0.01%: G = 1	10V step		60			*		μsec
G = 100			500			*		μsec
G = 1000			4500			*		μsec
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range		±3.5		±18	*		*	V
Quiescent Current[3]	V_O = 0V, $T_A = T_{MIN}$ to T_{MAX}		±500	±750		*	*	μA
TEMPERATURE RANGE								
Specification		−25		+85	*		*	°C
Operation	$R_L > 50k\Omega$[3]	−25		+85	*		*	°C
Storage		−65		+150	*		*	°C

*Specifications same as for INA102AG.

NOTES: (1) The internal gain set resistors have an absolute tolerance of ±20%; however, their tracking is 50ppm/°C. R_G will add to the gain error if gains other than 1, 10, 100 or 1000 are set externally. (2) Adjustable to zero at any one time. (3) At high temperature, output drive current is limited. An external buffer can be used if required.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18V
Input Voltage Range ..... ±V_{CC}
Operating Temperature
Range ..... −25°C to +85°C
Storage Temperature
Range ..... −65°C to +150°C
Lead Temperature
(soldering 10 seconds)..... +300°C
Output Short-Circuit
Duration.....Continuous to ground

ORDERING INFORMATION

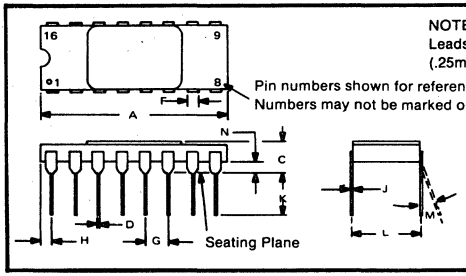
INA102 X G

Basic Model Number
Performance Grade Code
A, C: −25°C to +85°C

Package Code
G: 16-pin Hermetic DIP

INA102AG, INA102CG

MECHANICAL



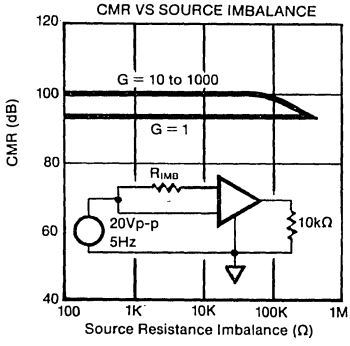
Pin numbers shown for reference only.
Numbers may not be marked on package.

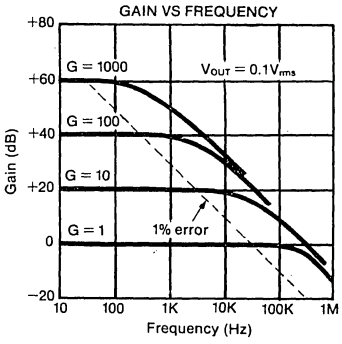
NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

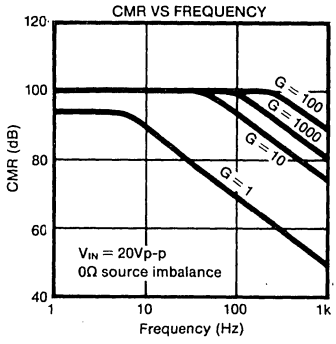
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

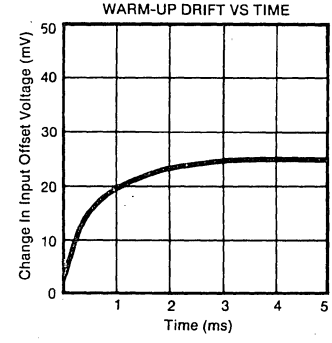
TYPICAL PERFORMANCE CURVES

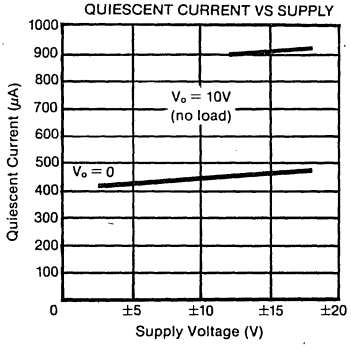
At +25°C and in circuit of Figure 2 unless otherwise noted.

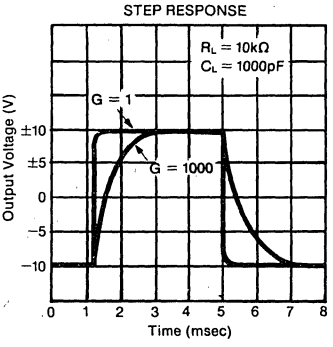


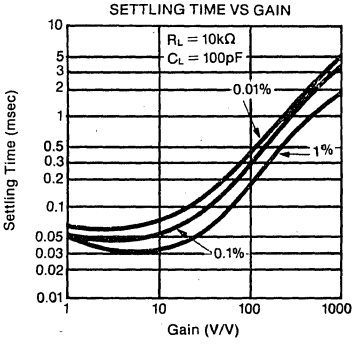


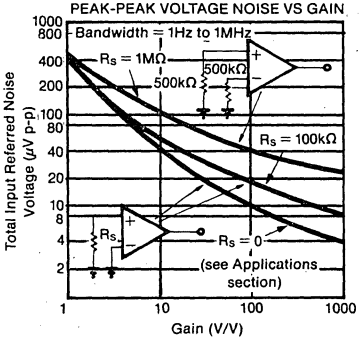


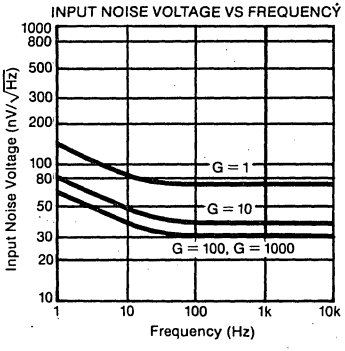












DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond mainly to the difference between the two input signals and exhibit extremely-high input impedance, both differential and common-mode. The feedback networks of this instrumentation amplifier are included on the monolithic chip. No external resistors are required for gains of 1, 10, 100 and 1000 in the INA102.

An operational amplifier, on the other hand, is an open-loop, uncommitted device that requries external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems.

THE INA102

A simplified schematic of the INA102 is shown on the

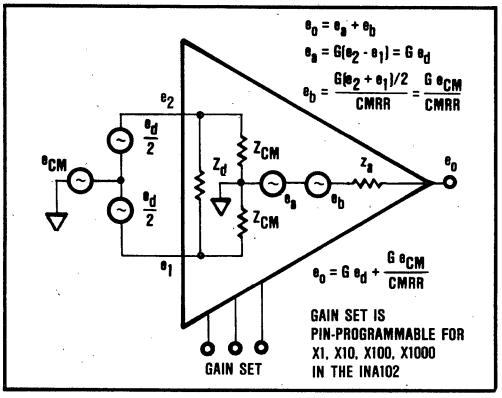


FIGURE 1. Model of an Instrumentation Amplifier.

first page. A three-amplifier configuration is used to provide the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found in integrated circuit instrumentation amplifiers.

The input buffers (A1 and A2) incorporate high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in instrumentation amplifier applications. The offset voltage and offset voltage versus temperature are low due to the monolithic design, and improved even further by state-of-the-art laser-trimming techniques.

The output stage (A3) is connected in a unity-gain differential amplifier configuration. A critical part of this stage is the matching of the four 20kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain good common-mode rejection.

All of the internal resistors are made of thin-film nichrome on the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability and provides excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA102 is operated over wide temperature ranges.

USING THE INA102

Figure 2 shows the simplest configuration of the INA102. The output voltage is a function of the differential input voltage times the gain.

A gain of 1, 10, 100, or 1000 is selected by programming pins 2 through 7 (see Table I). Notice that for the gain of 1000, a special gain sense is provided to preserve accuracy. Although this is not always required, gain errors caused by external resistance in series with the low value 40.04Ω internal gain set resistor are thus eliminated.

Other gains between 1 and 10, 10 and 100, and 100 and 1000 can also be obtained by connecting an external resistor between pin 6 and either pin 2, 3, or 4, respectively (see Figure 6 for application).

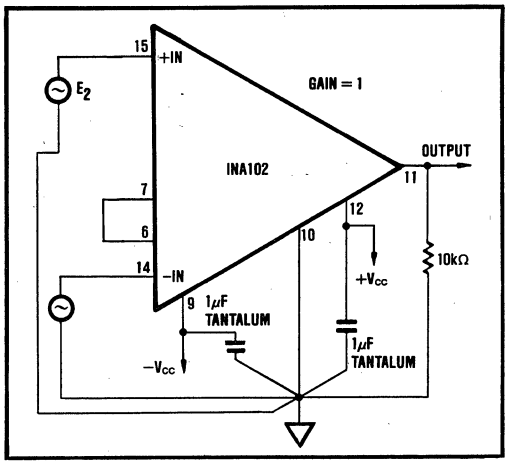


FIGURE 2. Basic Circuit Connection for the INA102.

$G = 1 + (40/R_G)$ where R_G is the total resistance between the two inverting inputs of the input op amps. At high gains, where the value of R_G becomes small, additional resistance (i.e., relays or sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

TABLE I. Pin-Programmable Gain Connections.

GAIN	CONNECT PINS
1	6 to 7
10	2 to 6 and 7
100	3 to 6 and 7
1000	4 to 7 and separately 5 to 6

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is sometimes desirable to null the input and/or output offset to achieve higher accuracy. The quality of the potentiometer will affect the results; therefore, choose one with good temperature and mechanical-resistance stability.

The optional offset null capabilities are shown in Figure 3. R_4 adjustment affects only the input stage component of the offset voltage. Note that the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately 0.31μV/°C per 100μV of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offset correction can be accomplished with A_1, R_1, R_2, and R_3, by applying a voltage to Common (pin 10) through a buffer amplifier. This buffer limits the resistance in series with pin 10 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 100dB. Be certain to keep this resistance low.

It is important to not exceed the input amplifier's dynamic range. The amplified differential input signal and its associated common-mode voltage should not

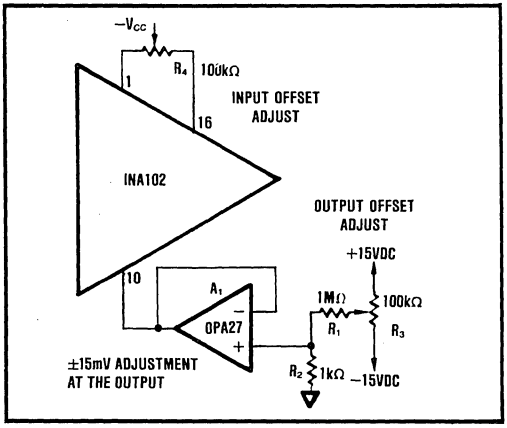


FIGURE 3. Optional Offset Nulling

cause the output of A_1 or A_2 to exceed approximately ±12V with ±15V supplies or nonlinear operation will result. To protect against moisture, especially in high gain, sealing compound may be used. Current injected into the offset pins should be minimized.

OPTIONAL FILTERING

The INA102 has provisions for accomplishing filtering with one external capacitor between pins 11 and 13. This single-pole filter can be used to reduce noise outside the signal bandwidth, but with degradation to AC CMR.

When it is important to preserve CMR versus frequency (especially at 60Hz), two capacitors should be used. The additional capacitor is connected between pins 8 and 10. This will maintain a balance of impedances in the output stage. Either of these capacitors could also be trimmed slightly to maximize CMR, if desired. Note that their ratio tracking will affect CMR over temperature.

OPTIONAL COMMON-MODE REJECTION TRIM

The INA102 is laser-adjusted during manufacturing to assure high CMR. However, if desired, a small resistance can be added in series with pin 10 to trim the CMR to an improved level. Depending upon the nature of the internal imbalances, either a positive or negative resistance

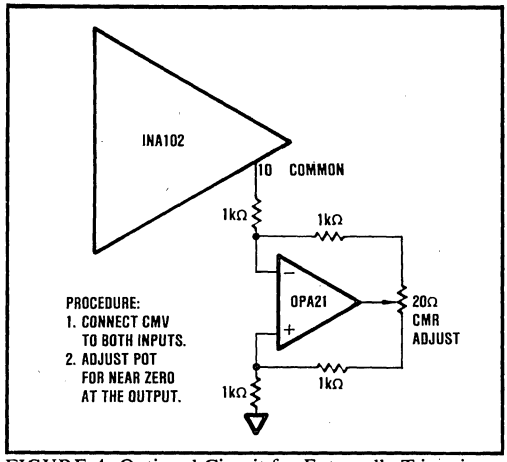


FIGURE 4. Optional Circuit for Externally Trimming CMR.

value could be required. The circuit shown in Figure 4 acts as a bipolar potentiometer and allows easy adjustment of CMR.

TYPICAL APPLICATIONS

Many applications of instrumentaition amplifiers involve the amplification of low level differential signals from bridges and transducers such as strain gauges, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA102 accomplishes all of these with high precision at surprisingly low quiescent current. However, in higher gains (>10) with high source impedances (>100kΩ), the bias current can cause a large offset at the output. This can saturate the output unless the source impedance is separated, e.g., two 500kΩ paths instead of one 1MΩ unbalanced input. The input offset current times 500kΩ will then generate a small DC voltage error.

Figures 5 through 11 show some typical applications circuits.

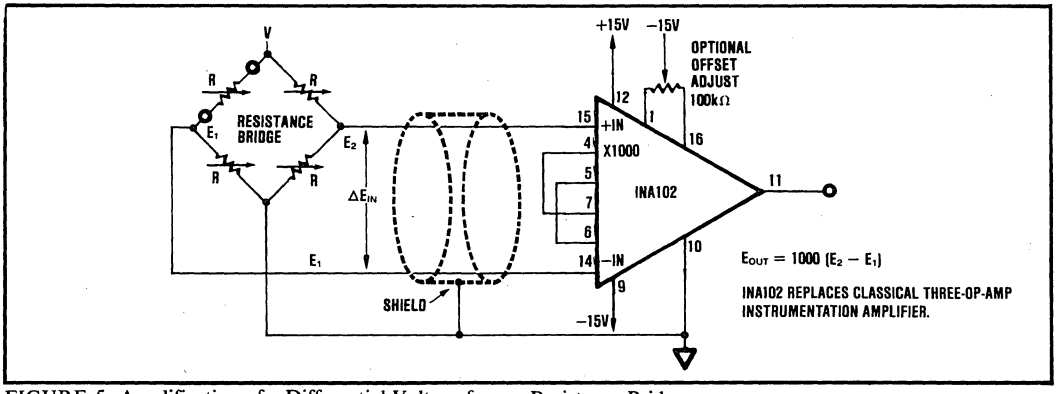


FIGURE 5. Amplification of a Differential Voltage from a Resistance Bridge.

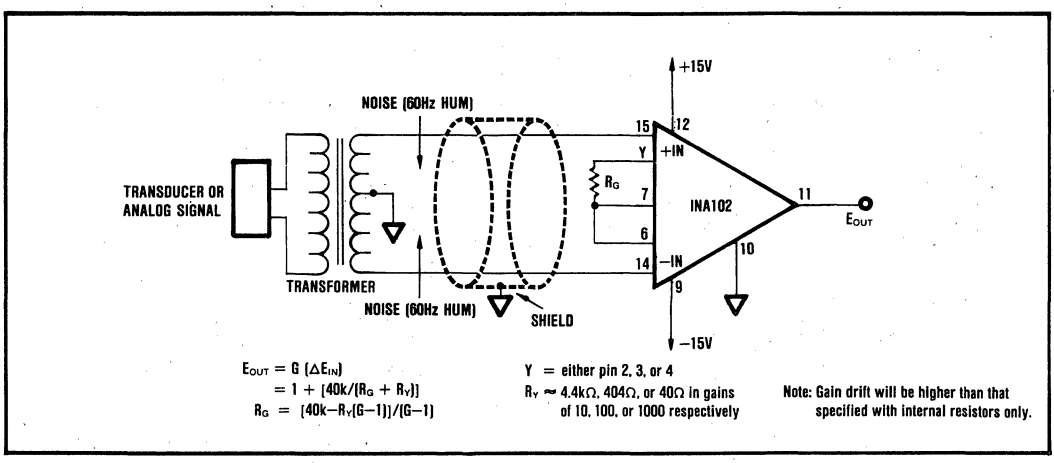


FIGURE 6. Amplification of a Transformer-Coupled Analog Signal Using External Gain Set.

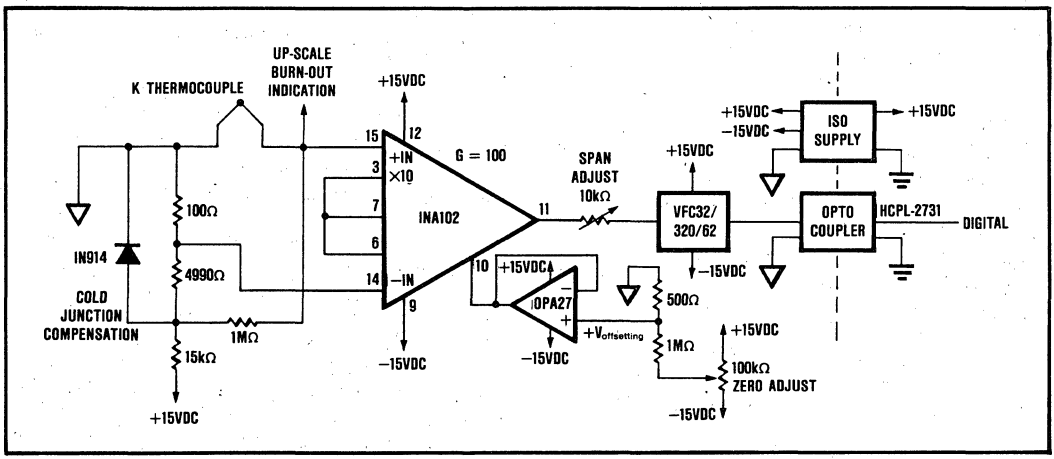


FIGURE 7. Isolated Thermocouple Amplifier with Cold Junction Compensation.

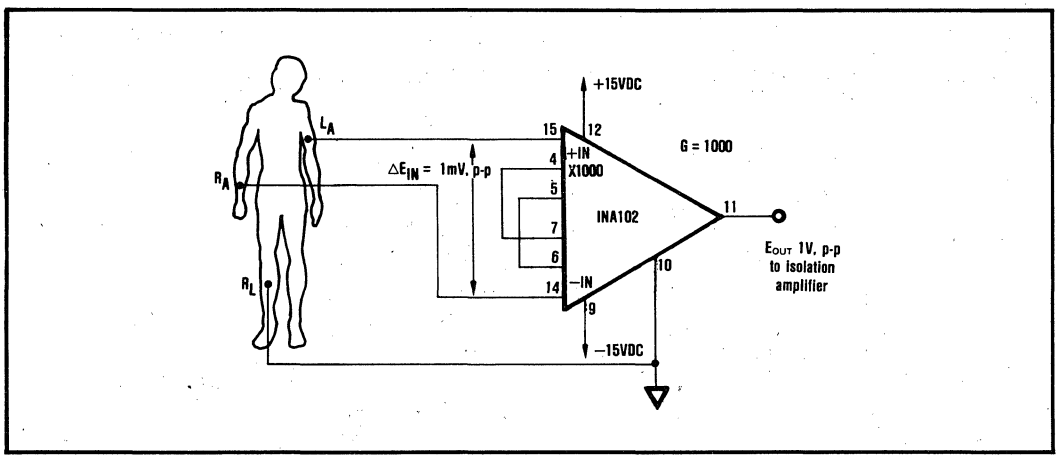


FIGURE 8. ECG Amplifier or Recorder Preamp for Biological Signals.

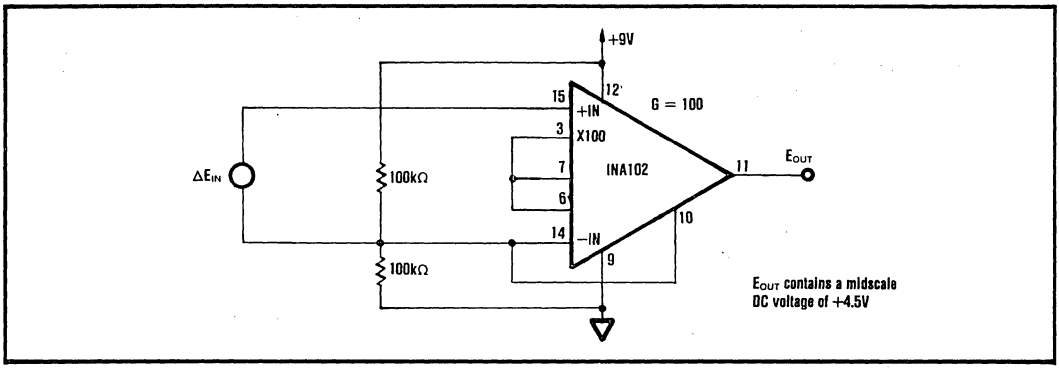


FIGURE 9. Single Supply Low Power Instrumentation Amplifier.

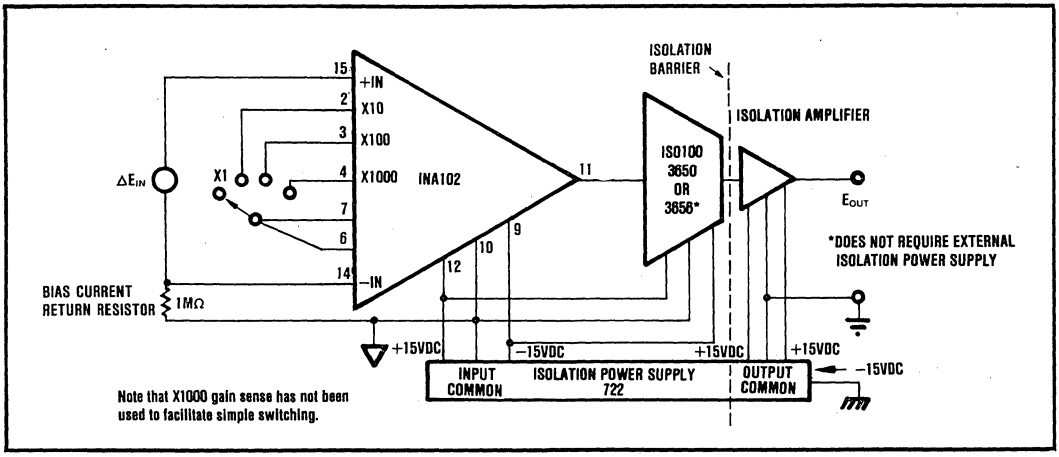


FIGURE 10. Precision Isolated Instrumentation Amplifier.

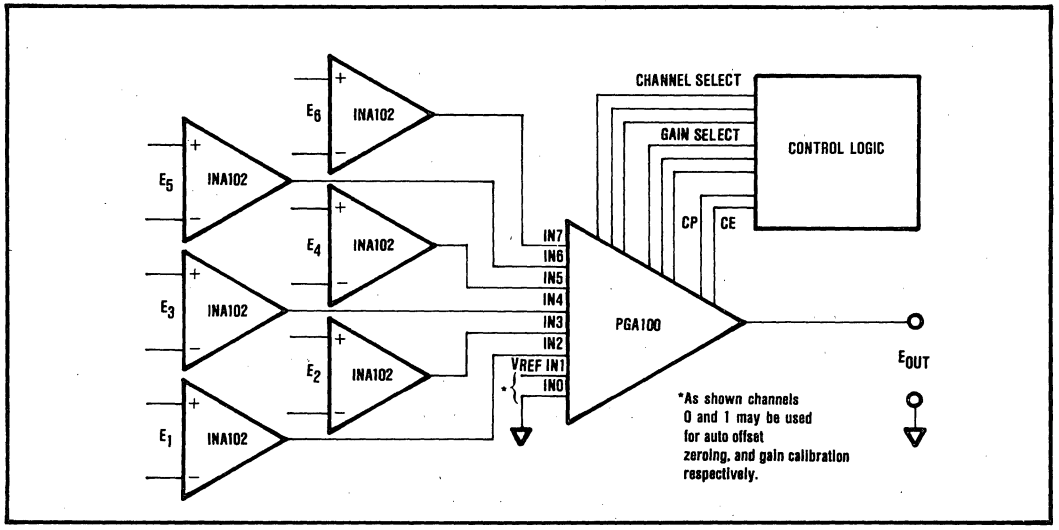


FIGURE 11. Multiple Channel Precision Instrumentation Amplifier With Programmable Gain.

BURR-BROWN®

INA104

Very-High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- VERSATILE FOUR-OP AMP DESIGN
- ULTRA-LOW VOLTAGE DRIFT - 0.25μV/°C, max
- LOW OFFSET VOLTAGE - 25μV, max
- LOW NONLINEARITY - 0.002%, max
- LOW NOISE - 13nV/$\sqrt{Hz}$ at f_0 = 1kHz
- HIGH CMR - 106dB at 60Hz, min
- HIGH INPUT IMPEDANCE - $10^{10}\Omega$
- LOW COST

APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gages
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCER AMPLIFIER
- LOW LEVEL SIGNAL CONDITIONER
- MEDICAL INSTRUMENTATION

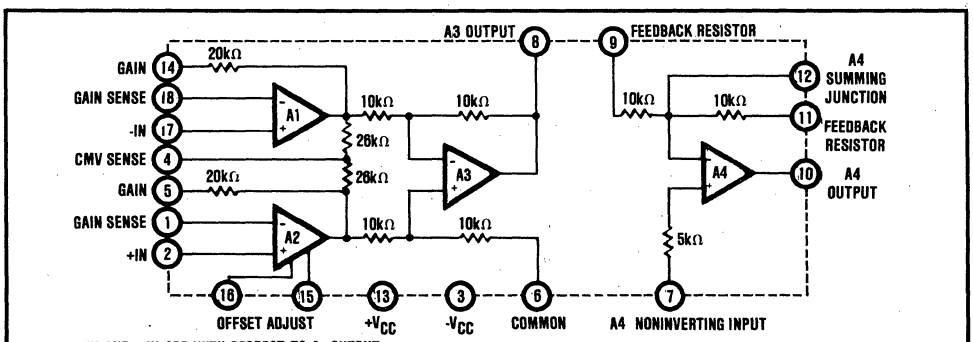
DESCRIPTION

The INA104 is a high accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very-high performance is desired.

A multiamplifier, monolithic design, which uses Burr-Brown's ultra-low drift, low noise technology, provides the highest performance with maximum versatility at the lowest cost and this makes the INA104 ideal for even high volume applications.

Burr-Brown's compatible thin-film resistors and state-of-the-art wafer level laser-trimming techniques are used for minimizing offset voltage and temperature drift. This advanced technique also maximized common-mode rejection and gain accuracy.

The INA104 also contains a fourth operational amplifier, specified separately, which can conveniently be used for some important applications such as single capacitor active low-pass filtering, easy output level shifting, Common-mode voltage active guard drive, and increased gain (x 10,000 and greater).



NOTE: +IN AND −IN ARE WITH RESPECT TO A_3 OUTPUT.
IF A_4 IS USED INVERTING, +IN AND −IN ARE REVERSED.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C with ±15VDC power supply and in circuit of Figure 1 unless otherwise noted.

	INA104AM/HP			INA104BM/SM/JP			INA104CM/KP			
MODEL	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INSTRUMENTATION AMPLIFIER										
GAIN										
Range of Gain	1		1000	*		*	*		*	V/V
Gain Equation		G = 1 + (40k/R_G)			*			*		V/V
Error From Equation, DC[1]		±(0.08 - 0.05/G)	±(0.15 - 0.1/G)		*	*		*	*	% of FS
Gain Temp. Coefficient[2]										
G = 1		2	5		*	*		*	*	ppm/°C
G = 10		20	100		*	*		10	50	ppm/°C
G = 100		22	110		*	*		11	55	ppm/°C
G = 1000		22	110		*	*		11	55	ppm/°C
Nonlinearity, DC		±(0.002 + 10^{-5}G)	±(0.005 + 2 x 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.002 + 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.002 + 10^{-5}G)	% of p-p FS
RATED OUTPUT										
Voltage	±10	+11.5, −12.5		*	*		*	*		V
Current	±5	+11.5, −12.5		*	*		*	*		mA
Output Impedance		0.2			*			*		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at +25°C[3]		±25 ±200/G	±50 ±400/G		±10 ±100/G	±25 ±200/G		±10 ±100/G	±25 ±200/G	µV
vs Temperature			±2 ±20/G			±0.75 ±10/G			±0.25 ±10/G	µV/°C
vs Supply		±(1 + 50/G)			*			*		µV/V
vs Time		±(1 + 20/G)			*			*		µV/mo
INPUT BIAS CURRENT										
Initial Bias Current (each input)		±15	±30		±10	*		±5	±20	nA
vs Temperature		±0.2			*			*		nA/°C
vs Supply		±0.1			*			*		nA/V
Initial Offset Current		±5	±30		±2	*		±2	±20	nA
vs Temperature		±0.5			*			*		nA/°C
INPUT IMPEDANCE										
Differential		10^{10} || 3			*			*		Ω || pF
Common-mode		10^{10} || 3			*			*		Ω || pF
INPUT VOLTAGE RANGE										
Range, Linear Response	±10			*			*			V
CMR with 1kΩ Source Imbal.										
DC to 60Hz, G = 1	80	90		*	*		*	*		dB
DC to 60Hz, G = 10	96	106		*	*		*	*		dB
DC to 60Hz, G = 100 to 1000	106	110		*	*		*	*		dB
INPUT NOISE										
Input Voltage Noise										
f_B = 0.1Hz to 10Hz		0.8			*			*		µV, p-p
Density, G = 1000										
f_o = 10Hz		18			*			*		nV/√Hz
f_o = 100Hz		15			*			*		nV/√Hz
f_o = 1kHz		13			*			*		nV/√Hz
Input Current Noise										
f_B = 0.01Hz to 10Hz		50			*			*		pA, p-p
Density										
f_o = 10Hz		0.8			*			*		pA/√Hz
f_o = 100Hz		0.46			*			*		pA/√Hz
f_o = 1kHz		0.35			*			*		pA/√Hz
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness										
G = 1		300			*			*		kHz
G = 10		140			*			*		kHz
G = 100		25			*			*		kHz
G = 1000		2.5			*			*		kHz
Small Signal, ±1% Flatness										
G = 1		20			*			*		kHz
G = 10		10			*			*		kHz
G = 100		1			*			*		kHz
G = 1000		200			*			*		Hz
Full Power, G = 1 - 100		6.4			*			*		kHz
Slew Rate, G = 1 - 100	0.2	0.4		*	*		*	*		V/µsec
Settling Time (0.1%)										
G = 1		30	40		*	*		*	*	µsec
G = 100		40	55		*	*		*	*	µsec
G = 1000		350	470		*	*		*	*	µsec
Settling Time (0.01%)										
G = 1		30	45		*	*		*	*	µsec
G = 100		50	70		*	*		*	*	µsec
G = 1000		500	650		*	*		*	*	µsec

ELECTRICAL (CONT)

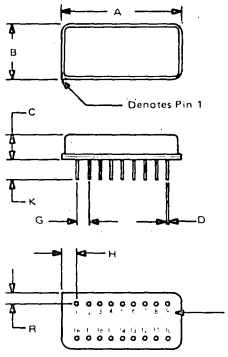
	INA104AM/HP			INA104BM/SM/JP			INA104CM/KP			
MODEL	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
					OUTPUT AMPLIFIER, A_4					
OPEN-LOOP GAIN, $V_O = \pm 100$										
Rated Load $R_L \geq 2k\Omega$	100	115		•	•		•	•		dB
$R_L \geq 10k\Omega$	110	125		•	•		•	•		dB
RATED OUTPUT										
Voltage at $R_L = 2k\Omega$	10	+13, −14.5		•	•		•	•		V
$R_L = 10k\Omega$		+13, −14.5			•			•		V
Current	5	7.5		•	•		•	•		mA
Output Impedance		2			•			•		kΩ
Load Capacitance (unity-gain inverting)		2000			•			•		pF
Short Circuit Current		10			•			•		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			•			•		MHz
Full Power		9			•			•		kHz
Slew Rate	0.35	0.55		•	•		•	•		V/μsec
Settling Time (unity gain)										
0.1%		37			•			•		μsec
0.01%		40			•			•		μsec
INPUT OFFSET VOLTAGE										
Initial, $T_A = +25°C$		±1	±2		•	•		•	•	mV
vs Temperature		±5			•			•		μV/°C
INPUT BIAS CURRENT		+55	+150							nA
INPUT IMPEDANCE										
Differential		500			•			•		kΩ
Common-Mode		100			•			•		MΩ
RESISTORS, 10kΩ										
Accuracy		0.5	5		•			•		%
Drift		30	50		•	•		•	•	ppm/°C
Ratio Match		0.06	0.12		•	•		•	•	%
Drift		5			•			•		ppm/°C
INPUT VOLTAGE NOISE										
F_B = 0.1Hz to 10Hz		1.5			•			•		μV,p-p
Density										
f_o = 10Hz		35			•			•		$nV\sqrt{Hz}$
f_o = 100Hz		33			•			•		$nV\sqrt{Hz}$
f_o = 1kHz		32			•			•		$nV\sqrt{Hz}$
POWER SUPPLY, TOTAL										
Rated Voltage		±15			•			•		V
Voltage Range	±5		±20	•		•	•		•	V
Current, Quiescent		±8.1	±9.6		•	•		•	•	mA
TEMPERATURE RANGE										
Specification										
INA104HP/JP/KP	0		+70							°C
INA104AM/BM/CM	−25		+85							°C
INA104SM	−55		+125							°C
Operation										
INA104HP/JP/KP	−40		+85							°C
INA104AM/BM/CM/SM	−55		+85							°C
Storage										
INA104HP/JP/KP	−40		+85							°C
INA104AM/BM/CM/SM	−65		+150							°C
θ_{J-C}		115			•			•		0°C/W
θ_{J-A}		350			•			•		0°C/W

*Specifications same as for INA104HP.

NOTES:
1. Typically the tolerance of R_G will be the major source of gain error. 2. Not including the TCR of R_G. 3. Adjustable to zero at any one gain.

MECHANICAL

METAL HERMETIC DIP

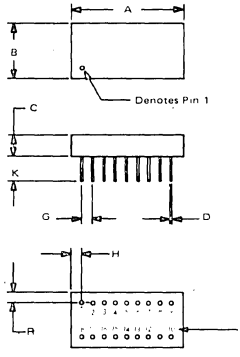


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.060	1.080	26.92	27.43
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

NOTE: Leads in true position within 0.01" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers are not marked on package.

PLASTIC DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.990	1.010	25.15	25.65
B	.490	.510	12.45	12.95
C	.190	.210	4.83	5.33
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

NOTE: Leads in true position within 0.01" (.25mm) R at MMC at seating plane.

Pin numbers shown fo reference only. Numbers are not marked on package.

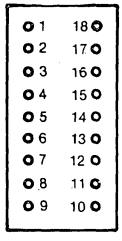
ABSOLUTE MAXIMUM RATINGS

Supply	±20V
Internal Power Dissipation	980mW
Input Voltage Range	±V_{CC}
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +85°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground

PIN DESIGNATIONS

1. GAIN SENSE
2. +IN
3. NEGATIVE SUPPLY
4. COMMON-MODE VOLTAGE SENSE
5. GAIN
6. COMMON
7. NONINVERTING INPUT TO A_4
8. OUTPUT
9. FEEDBACK RESISTOR
10. OUTPUT OF A_4
11. FEEDBACK RESISTOR
12. SUMMING JUNCTION OF A_4
13. POSITIVE SUPPLY
14. GAIN
15. OFFSET ADJUST
16. OFFSET ADJUST
17. -IN
18. GAIN SENSE

(TOP VIEW)



ORDERING INFORMATION

INA104 X X

Basic Model Number

Performance Grade Code
H, J, K: 0°C to +70°C
A, B, C: −25°C to +85°C
S: −55°C to +125°C

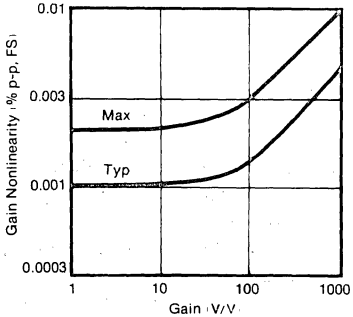
Package Code
P - Plastic DIP
M - Metal Hermetic DIP

Plastic DIP (Hybripak):	Metal DIP
INA104HP	INA104AM
INA104JP	INA104BM
INA104KP	INA104CM
	INA104SM

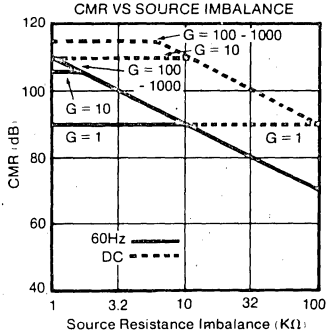
TYPICAL PERFORMANCE CURVES

At +25°C, ±V_{CC} = 15VDC, and in circuit of Figure 1 unless otherwise specified.

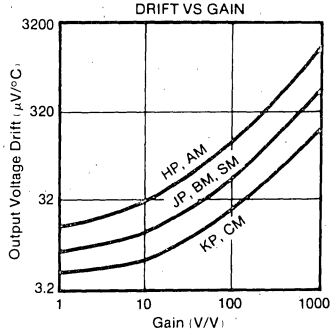
GAIN NONLINEARITY VS GAIN

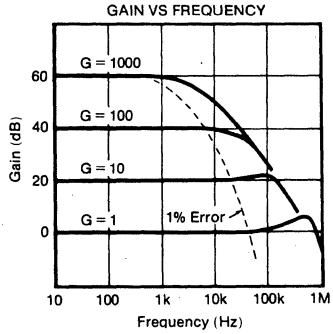


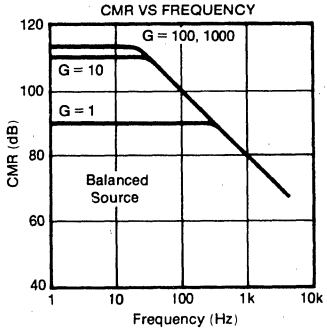
CMR VS SOURCE IMBALANCE

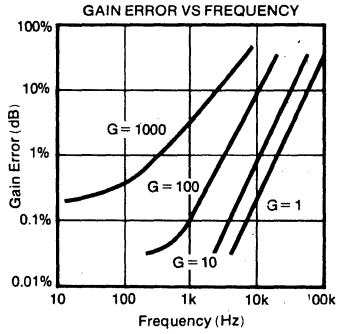


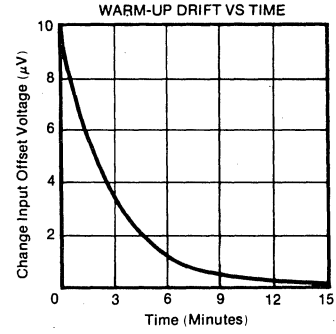
TOTAL OFFSET VOLTAGE DRIFT VS GAIN

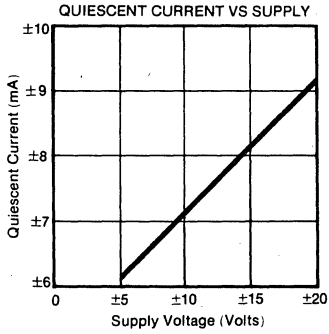


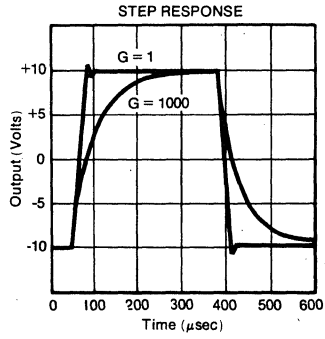


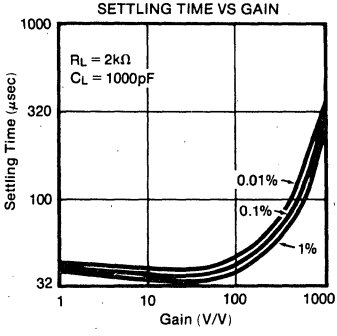


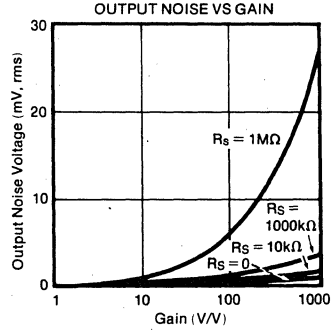


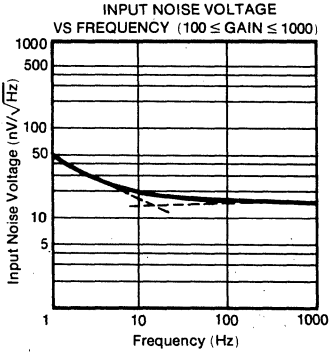












DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are closed-loop gain blocks whose committed circuitry accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely-high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While operational amplifiers can be used to achieve the same basic function as instrumentation amplifiers, it is difficult to reach the same level of performance. Using operational amplifiers often leads to design trade-offs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances.

THE INA104

A simplified schematic of the INA104 is shown on the first page of this data sheet. It is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found on integrated circuit instrumentation amplifiers.

The input section (A1 and A2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide

the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature is low due to the monolithic design and improved even further by the state-of-the-art laser-trimming techniques.

The output section (A3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the internal resistors are compatible thin-film nichrome formed with the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability of trimmed resistors and simultaneous achievement of excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA104 is operated over wide temperature ranges.

The fourth op-amp (A4) of the INA104 adds a great deal of versatility and convenience to the amplifier. Its use allows easy implementation of active low-pass filtering, output offsetting, and additional gain generation. The pin connections make the use of this stage optional and the specifications appear separately in the table of Electrical Specifications.

USING THE INA104

Figure 1 shows the simplest configuration of the INA104. The gain is set by the external resistor, R_G, with a gain equation of $G = 1 + (40K/R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

For gains greater than unity, resistor R_G is connected externally between pins 5 and 14. At high gains where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect. However, this error can be virtually eliminated with the INA104 by using the gain sense circuit connection.

Pins 1, 5, 14, and 18 are accessible so that a four-terminal connection can be made to R_G. (Pins 1 and 18 are the voltage sense terminals since no signal current flows into the operational amplifiers' inputs.) This may be useful at high gains where the value of R_G becomes small.

The optional offset adjust capability is shown in Figure 1. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed (if input offset is not adjusted to zero) when the gain is changed. Also, the input drift will be affected by approximately $0.31\mu V/°C$ per $100\mu V$ of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is frequently desirable to null the input component of offset (Figure 1) and occasionally that of the output

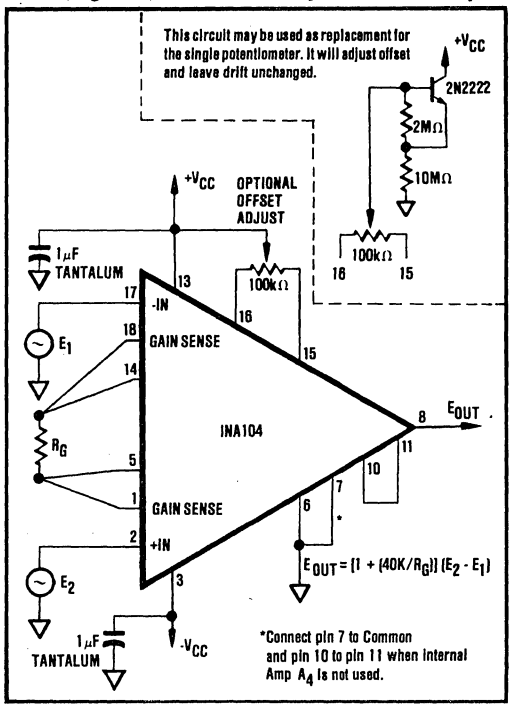


FIGURE 1. Basic Circuit Connection for the INA104 Including Optional Input Offset Null Potentiometer.

(Figure 2). The quality of the potentiometer will affect the results, therefore, choose one with good temperature and mechanical-resistance stability. The procedure is as follows:

1. Set $E_1 = E_2 = 0V$ (be sure a good ground return path exists to the input).
2. Set the gain to the desired value (greater than 1) by choosing R_G.
3. Adjust the 100kΩ potentiometer in Figure 1 until the output reads 0V ±1mV or desired setting. Note that the offset will change when the gain is changed. If the output component of offset is to be removed or if it is desired to establish an intentional offset, adjust the 100kΩ potentiometer in Figure 2 until the output reads 0V ±1mV or desired setting. Note that the offset will not change with gain, but be sure to use a stable amplifier with good DC characteristics. The range of adjustment is ±15mV as shown. For larger ranges change the ratio of R_1 to R_2. The op amp is used to maintain a low resistance (<0.1Ω) from pin 6 to Common to avoid CMR degradation.

BASIC CIRCUIT CONNECTION

The basic circuit connection for the INA104 is shown in Figure 1. The output voltage is a function of the differential input voltage times the gain.

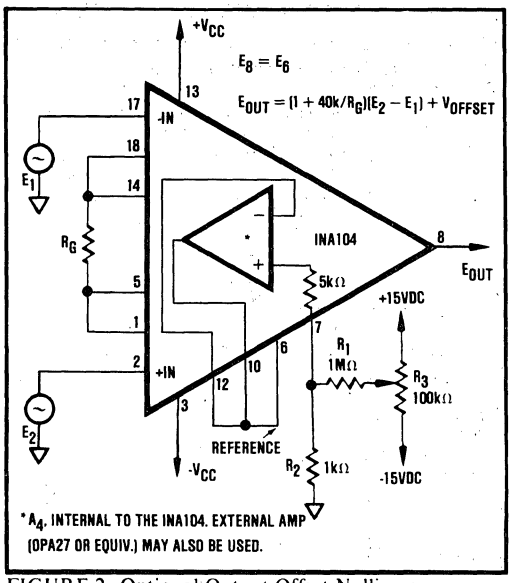


FIGURE 2. Optional Output Offset Nulling or Offsetting Using an Amplifier (Low Impedance to Pin 6).

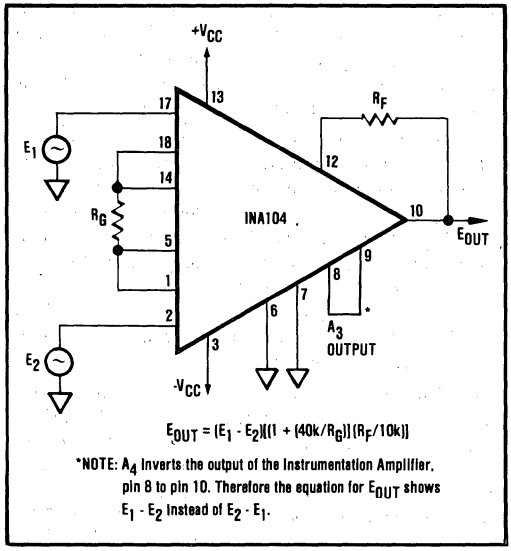


FIGURE 3. Additional Gain From Output Stage.

Figure 1 does not include additional internal op amp A_4. Power supply bypassing with a 1μF tantalum capacitor or equivalent is always recommended.

In applications which do not use the fourth internal amplifier (A_4 - pins 7, 9, 10, 11, and 12), pin 7 should be connected to Common and pins 10 and 11 should be connected together. This will prevent the output of A_4 from saturating ("locking-up") and affecting the offset of the instrumentation amplifier, A_1, A_2, and A_3.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gages, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA104 accomplishes all of these with high precision.

Figures 3 through 13 show some typical applications circuits.

Figure 3 shows how the output stage may be used to provide additional gain. If gains greater than 1000V/V (10,000 up to 100,000 and greater) are desired it is better to place some gain in the output amplifier rather than the input stage due to the low values of R_G required ($R_G <$ 40Ω for $(1 + 40k/R_G) > 1000$). Note, however, that accuracy can degrade due to very-high amplification of offset, drift, and noise errors.

Output offsetting ("zero suppression" or "zero elevation") may be more easily accomplished with the INA104 than with most other IC instrumentation amplifiers as shown in Figure 4. The use of the extra internal op amp, A_4, means that CMR of the instrument amp is not disturbed, and that a convenient value of variable resistor can be used. The circuit shown in Figure 2 can also be used to achieve the desired offsetting by scaling the resistors R_1 and R_2. A low impedance path from pin 6 to Common should be provided to achieve the high CMR specified. Resistance above 0.1Ω will cause the CMR to fall below 106dB.

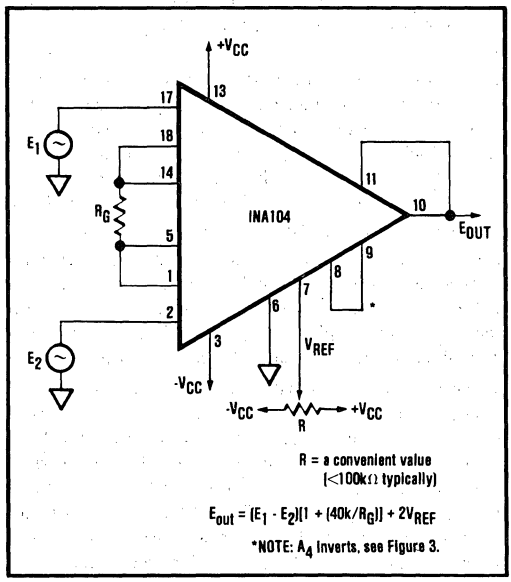


FIGURE 4. Output Offsetting.

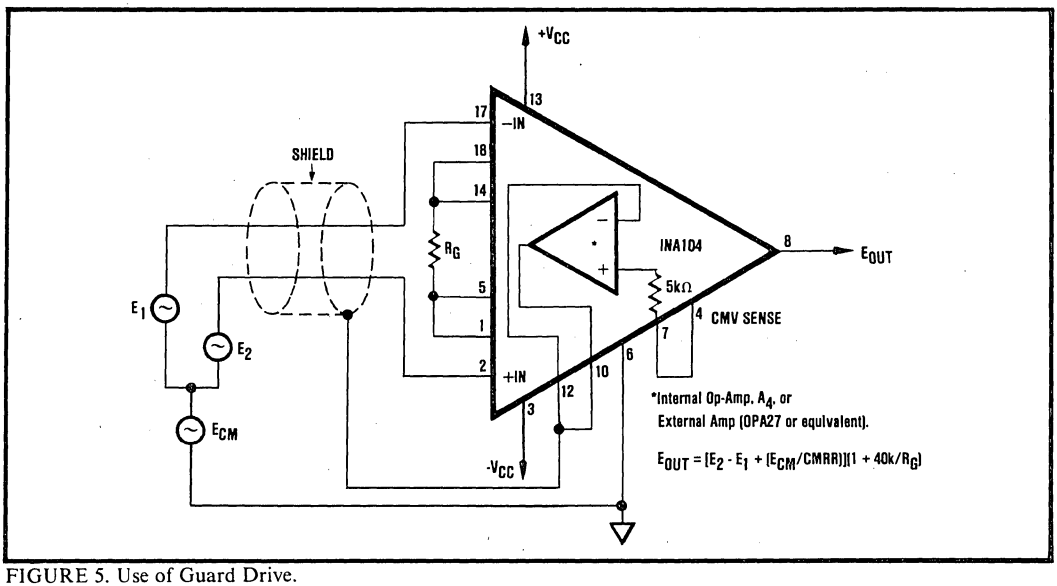


FIGURE 5. Use of Guard Drive.

Amplifier A_4 also allows active low-pass filtering to be implemented conveniently with a single capacitor. Filtering can be used for noise reduction or band-limiting of the output signal as shown in Figure 6.

The common-mode voltage from the 26kΩ resistors in the input section appears at pin 4. Figure 5 shows how this voltage can be used to drive the shield of the input cable. Since the cable is driven at the common-mode voltage, the effects of distributed capacitance is reduced and the AC system common-mode rejection may be improved. Amplifier A_4 buffers the CMV at pin 4 from the input cable.

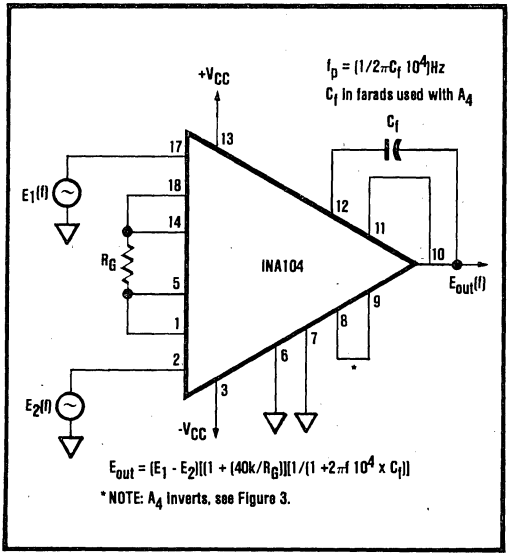


FIGURE 6. Active Low Pass Filtering.

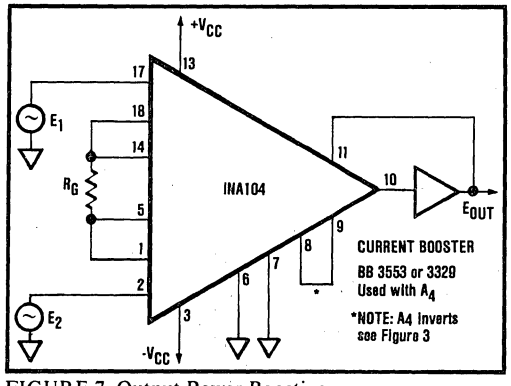


FIGURE 7. Output Power Boosting.

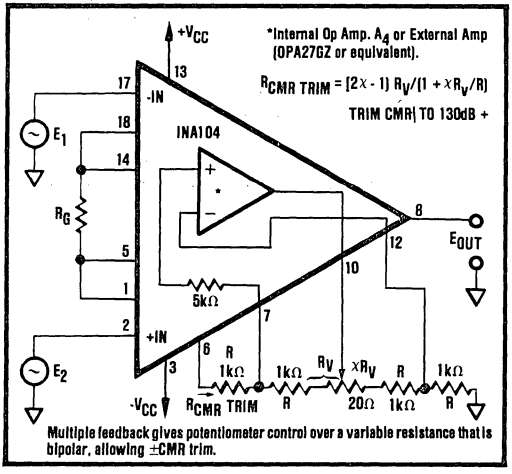


FIGURE 8. CMR Trim.

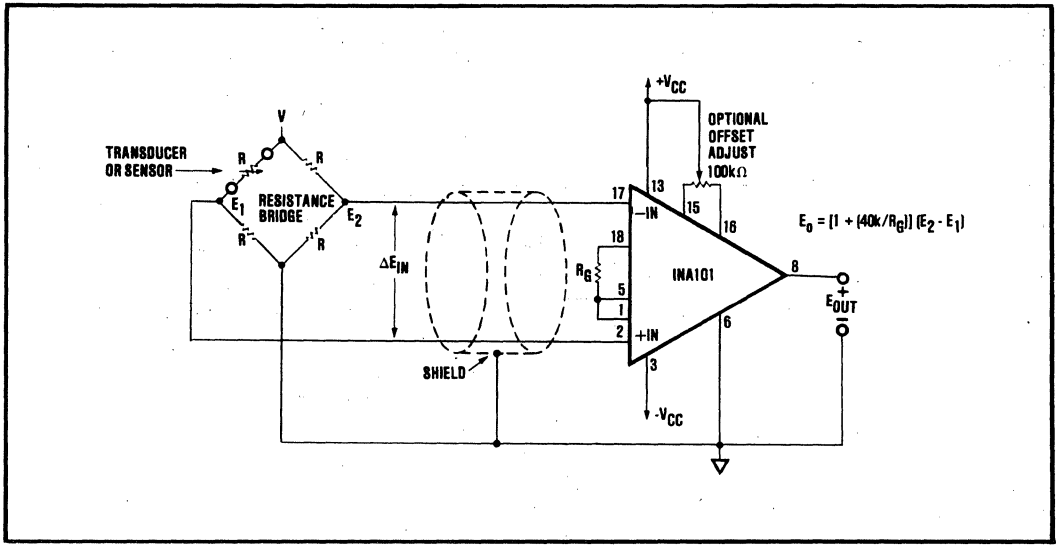


FIGURE 9. Amplification of a Differential Voltage from a Resistance Bridge.

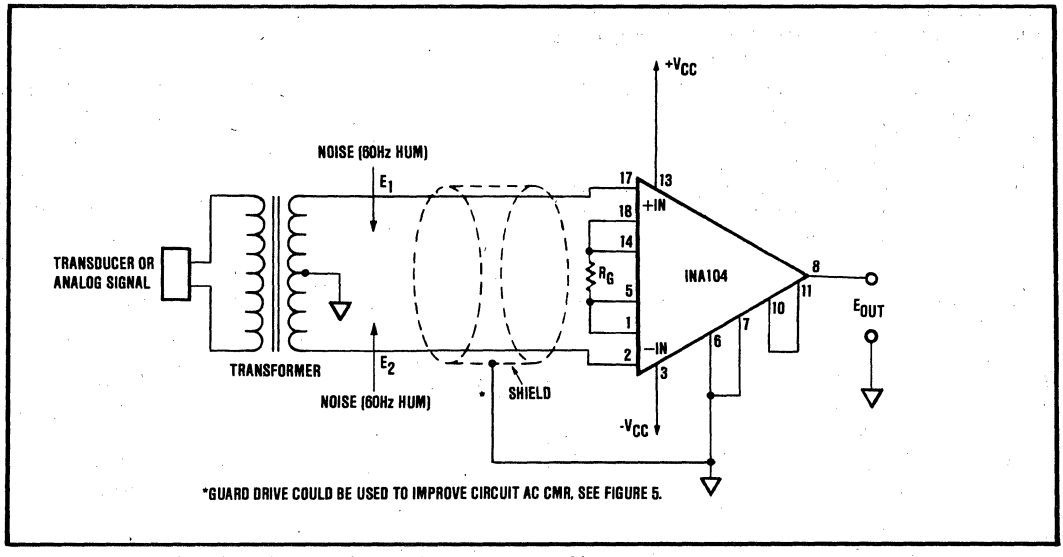


FIGURE 10. Amplification of a Transformer Coupled Analog Signal.

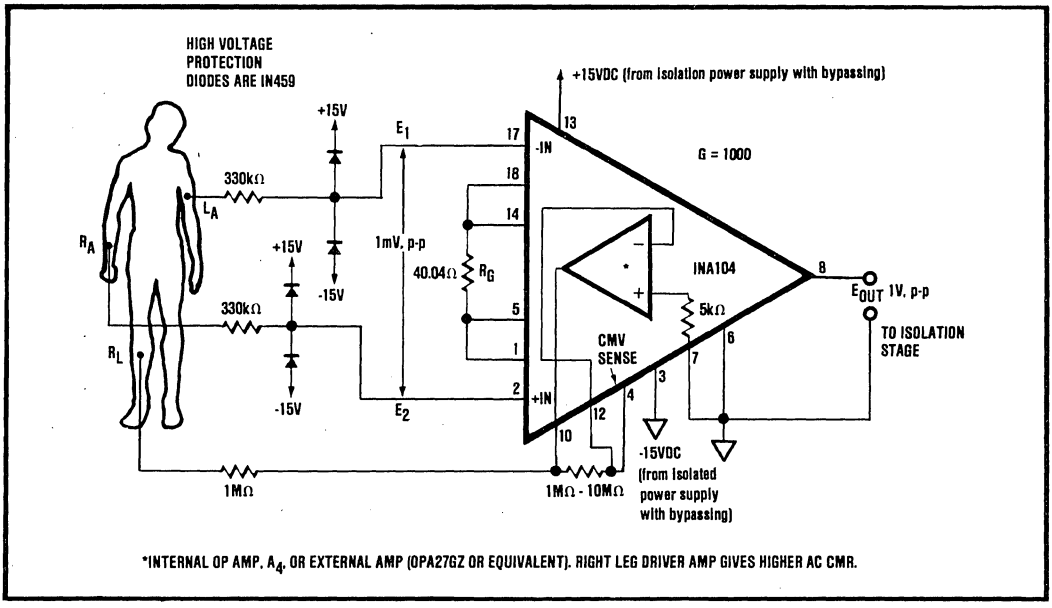


FIGURE 11. ECG Amplifier or Recorder Preamp for Biological Signals.

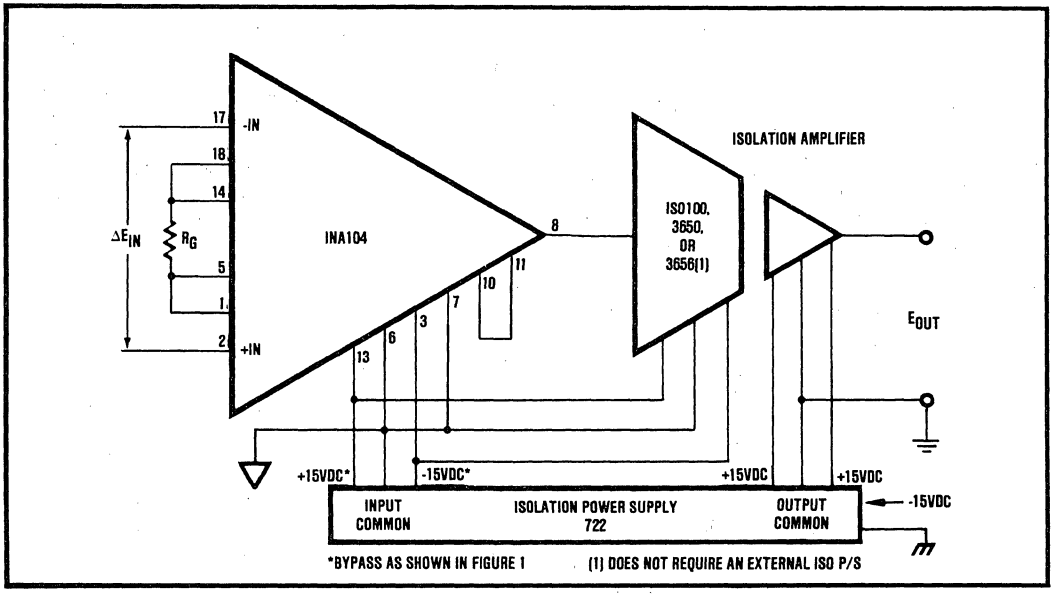


FIGURE 12. Precision Isolated Instrumentation Amplifier.

BURR-BROWN®

INA105

Precision Unity Gain DIFFERENTIAL AMPLIFIER

FEATURES

- CMR 86dB min over temp
- GAIN ERROR 0.01% max
- NONLINEARITY 0.001% max
- NO EXTERNAL ADJUSTMENTS REQUIRED
- EASY TO USE
- COMPLETE SOLUTION
- HIGHLY VERSATILE
- LOW COST
- TO-99 HERMETIC METAL AND LOW COST PLASTIC PACKAGES

APPLICATIONS

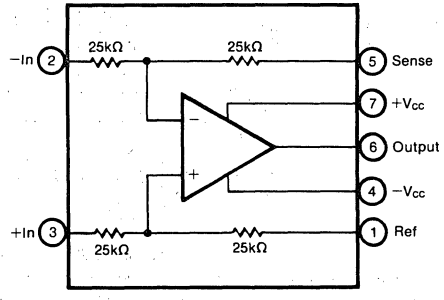
- DIFFERENTIAL AMPLIFIER
- BASIC INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- UNITY-GAIN INVERTING AMPLIFIER
- GAIN-OF-1/2 AMPLIFIER
- NONINVERTING GAIN-OF-2 AMPLIFIER
- AVERAGE VALUE AMPLIFIER
- ABSOLUTE VALUE AMPLIFIER
- SUMMING AMPLIFIER
- SYNCHRONOUS DEMODULATOR
- CURRENT RECEIVER WITH COMPLIANCE TO RAILS
- 4mA to 20mA TRANSMITTER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- ALL-PASS FILTERS

DESCRIPTION

The INA105 is a precision unity-gain differential amplifier. As a monolithic circuit, it offers high reliability at low cost. It consists of a premium grade operational amplifier and an on-chip precision resistor network.

As a special feature, the INA105 can drive 20mA from the positive supply. This simplifies construction of 4mA to 20mA current sources and transmitters.

The INA105 is completely self-contained and offers the user a highly versatile function. No adjustments to gain, offset, and CMR are necessary. This provides three important advantages: (1) lower initial design engineering time, (2) lower manufacturing assembly time and cost, and (3) easy cost-effective field repair of a precision circuit.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	INA105AM MIN	INA105AM TYP	INA105AM MAX	INA105BM MIN	INA105BM TYP	INA105BM MAX	INA105KP MIN	INA105KP TYP	INA105KP MAX	UNITS
GAIN											
Initial[1]			1			*			*		V/V
Error			0.005	0.01		*	*		0.01	0.025	%
vs Temperature			1	5		*	*		*		ppm/°C
Nonlinearity[2]			0.0002	0.001		*	*		*	*	%
OUTPUT											
Rated Voltage	I_O = +20mA, −5mA	10	12		*	*		*	*		V
Rated Current	E_O = 10V	+20, −5			*			*			mA
Impedance			0.01			*			*		Ω
Current Limit	To common		+40/−10			*			*		mA
Capacitive Load	Stable operation		1000			*			*		pF
INPUT											
Impedance	Differential		50			*			*		kΩ
	Common-mode		50			*			*		kΩ
Voltage Range	Differential	±10			*			*			V
	Common-mode	±20			*			*			V
Common-mode Rejection[3]	$T_A = T_{MIN}$ to T_{MAX}	80	90		86	100		72	*		dB
OFFSET VOLTAGE	RTO[4][5]										
Initial			50	250		*	*		*	500	μV
vs Temperature			5	20		5	10		*		μV/°C
vs Supply	±V_{CC} = 6V to 18V		1	25		*	15		*	*	μV/V
vs Time			20			*			*		μV/mo
OUTPUT NOISE VOLTAGE	RTO[4][6]										
F_B = 0.01Hz to 10Hz			2.4			*			*		μV p-p
F_O = 10kHz			60			*			*		nV/√Hz
DYNAMIC RESPONSE											
Small Signal	−3dB		1			*			*		MHz
Full Power BW	V_O = 20V p-p	30	50		*	*		*	*		kHz
Slew Rate		2	3		*	*		*	*		V/μs
Settling Time: 0.1%	V_O = 10V step		4			*			*		μs
0.01%	V_O = 10V step		5			*			*		μs
0.01%	V_{CM} = 10V step, V_{DIFF} = 0V		1.5			*			*		μs
POWER SUPPLY											
Rated			±15			*			*		V
Voltage Range	Derated performance	±5		±18	*		*	*		*	V
Quiescent Current	V_{OUT} = 0V		±1.5	±2		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		−25		+85	*		*	0		+70	°C
Operation		−55		+125	*		*	−25		+85	°C
Storage		−65		+150	*		*	−40		+85	°C

* Specification same as for INA105AM.

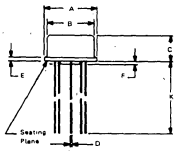
NOTES: (1) Connected as difference amplifier (see Figure 4). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) With zero source impedance (see Maintaining CMR section). (4) Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifier's offset voltage and noise voltage. (5) Includes effects of amplifier's input bias and offset currents. (6) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

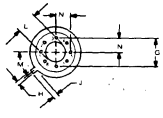
MECHANICAL

TO-99 PACKAGE

NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

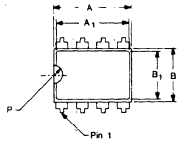
Pin numbers shown for reference only. Numbers are not marked on package.

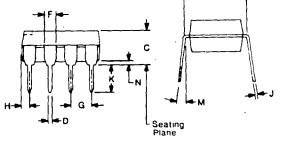




DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

"P" PACKAGE Plastic DIP

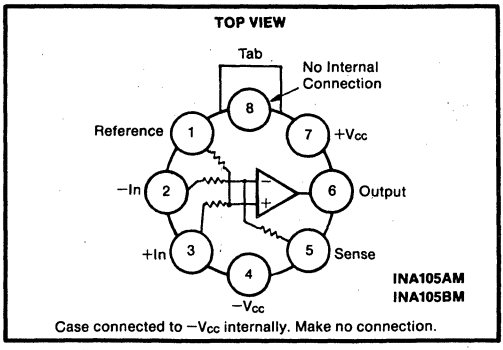




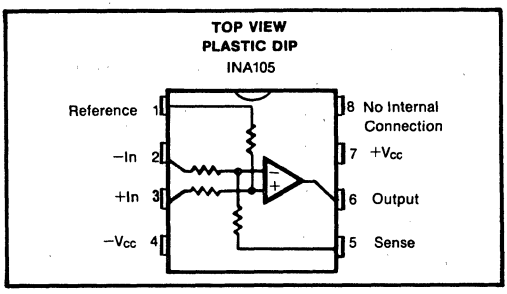
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.355	.400	9.03	10.16
A_1	.340	.386	8.65	9.80
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

PIN DESIGNATIONS



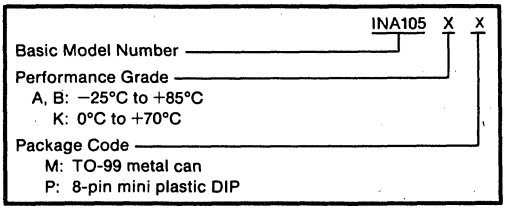
PIN DESIGNATIONS



ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Voltage Range	±Vcc
Operating Temperature Range: M	−55°C to +125°C
P	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short Circuit to Common	Continuous

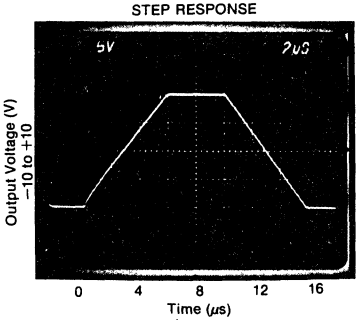
ORDERING INFORMATION



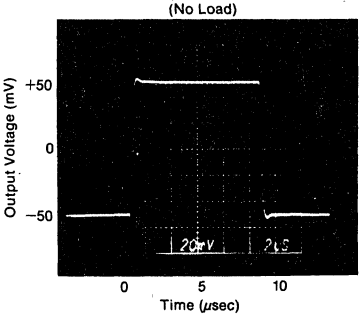
TYPICAL PERFORMANCE CURVES

$T_A = 25°C$, $\pm V_{CC} = 15VDC$ unless otherwise noted.

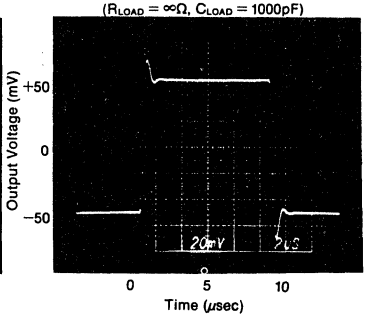
STEP RESPONSE



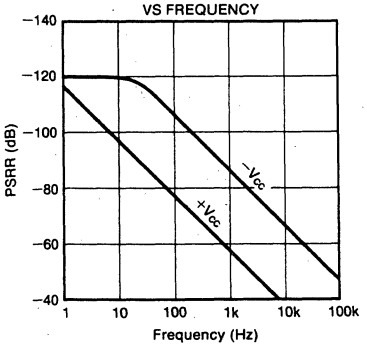
SMALL SIGNAL RESPONSE
(No Load)



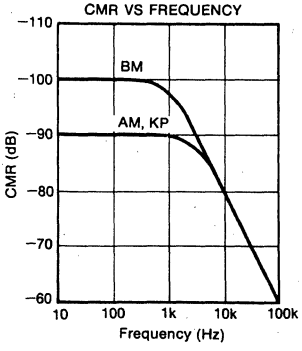
SMALL SIGNAL RESPONSE
($R_{LOAD} = \infty\Omega$, $C_{LOAD} = 1000pF$)



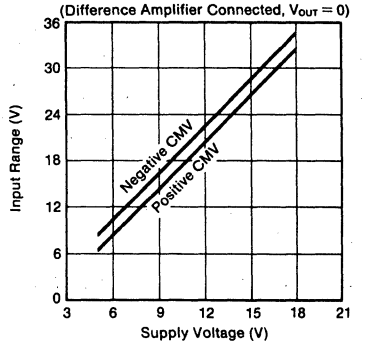
POWER SUPPLY REJECTION
VS FREQUENCY



CMR VS FREQUENCY

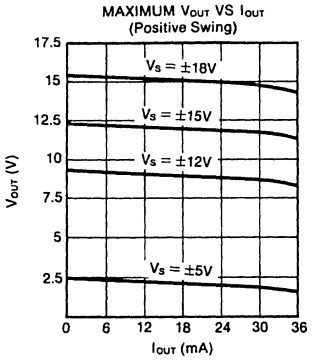


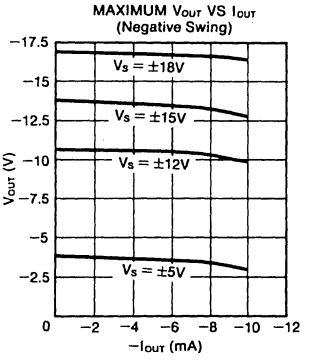
COMMON-MODE INPUT RANGE VS SUPPLY
(Difference Amplifier Connected, $V_{OUT} = 0$)



TYPICAL PERFORMANCE CURVES [CONT]

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.





DISCUSSION OF PERFORMANCE

The INA105 is the new solution to a widely occurring problem—how to realize a very accurate unity-gain differential amplifier at low cost. Burr-Brown's solution is a reliable monolithic circuit including both operational amplifier and thin-film resistors on the chip. State-of-the-art laser-trimming techniques assure total error of less than ±0.015% (gain error, nonlinearity, offsets, and common-mode rejection).

The performance of the unity-gain differential amplifier circuit can mistakenly be taken for granted. The necessary resistor accuracy is difficult to achieve, especially over temperature. Two classical techniques employed for obtaining the necessary accuracy are either manual trimming or the use of available packaged matched and tracking resistor networks. Both are expensive compared to the cost of the complete INA105.

The INA105 provides the total solution. By using a computer-controlled laser-trimming procedure, both accuracy and low cost are guaranteed. This makes external adjustment of gain, CMR, and offset voltage unnecessary. The user can be assured of excellent accuracy over temperature due to the properties inherent in Burr-Brown's thin-film resistors.

Other advantages are also apparent. Design, purchasing, and inventory costs are reduced. Labor time in adjusting independent resistors is eliminated both during manufacturing and field repair. Best of all, expensive potentiometers are not required. This further enhances circuit reliability.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1μF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance.

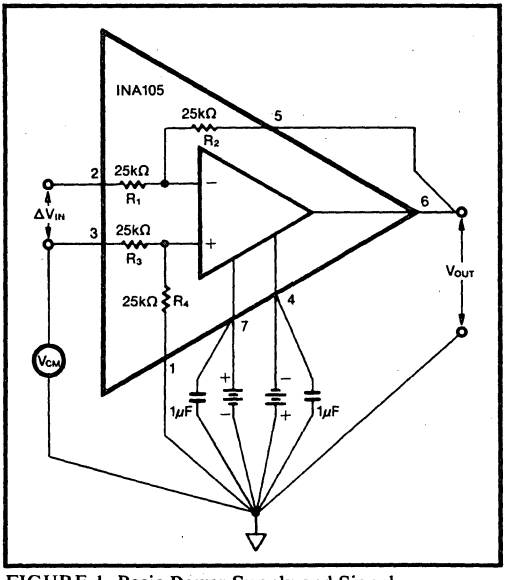


FIGURE 1. Basic Power Supply and Signal Connections.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuit for the INA105. This circuit will allow ±300μV of adjustment and will not affect the gain accuracy or CMR.

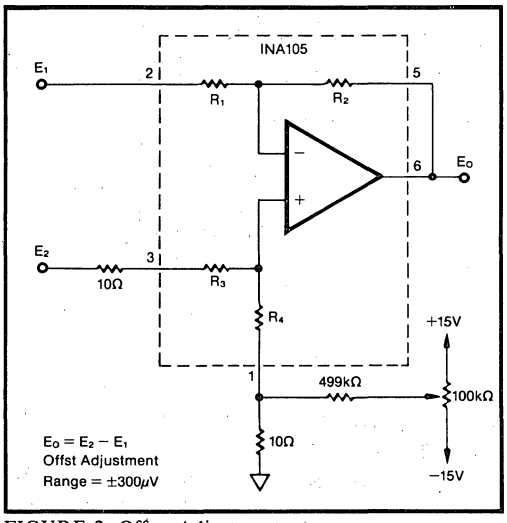


FIGURE 2. Offset Adjustment.

MAINTAINING COMMON-MODE REJECTION

Two factors are important in maintaining high CMR: (1) resistor matching and tracking (the internal INA105 circuitry does this for the user) and (2) source impedance including its imbalance.

Referring to Figure 1, the CMR depends upon the match of the internal R_4/R_3 ratio to the R_1/R_2 ratio. A CMR of 100dB requires resistor matching of 0.002%. To maintain 86dB, minimum CMR to +85°C, the resistor TCR tracking must be better than 2ppm/°C. These accuracies are difficult and expensive to reliably achieve with discrete components.

Any source impedance adds directly to the input resistors, R_1 and R_3, and will degrade DC and AC CMR. Likewise any wiring resistance adds directly to any of the precision difference resistors. A resistance of 0.5Ω (0.002% of 25kΩ) will degrade the 100dB CMR of the INA105; 5Ω will degrade the CMR to 80dB. Don't be tempted to interchange pins 1 and 3 or pins 2 and 5. The resistors in the INA105 are carefully matched to faithfully preserve the proper ratios. If they are switched, CMR and temperature drift performance will be degraded.

When input filters are used preceding an instrumentation amplifier (see Figure 5), care should also be taken to match RCs on the two input lines. For example, mismatched input filters for high frequencies will reduce the CMR at lower frequencies, e.g, 60Hz. Differential filters will not degrade AC CMR.

RESISTOR NOISE IN THE INA105

Figure 3 shows the model for calculating resistor noise in the INA105. Resistors have Johnson noise resulting from thermal agitation. The expression for this noise is:

$$E_{RMS} = \sqrt{4KTRB}$$

Where: K = Boltzman's constant (J/°K)
T = Absolute temperature (°K)
R = Resistance (Ω)
B = Bandwidth (Hz)

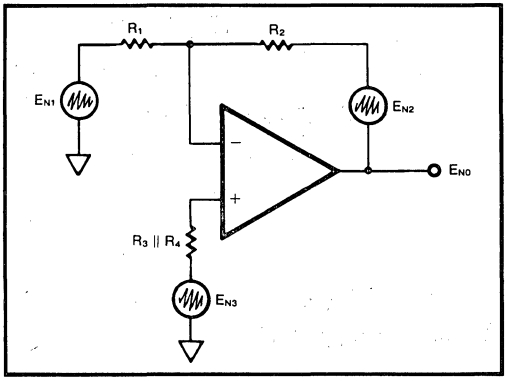


FIGURE 3. Resistor Noise Model.

At room temperature, this noise becomes:

$$E_N = 1.3^{-10}\sqrt{R} \qquad (V/\sqrt{Hz})$$

The three noise sources in Figure 2 are:

$$E_{N1} = 1.3^{-10}\,(R_2/R_1)\,\sqrt{R_1}$$
$$E_{N2} = 1.3^{-10}\,\sqrt{R_2}$$
$$E_{N3} = 1.3^{-10}\,(1 + R_2/R_1)\,\sqrt{R_3 \| R_4}$$

The output noise (given $R_1 = R_2 = R_3 = R_4 = 25k\Omega$) is:

$$E_{NO} = 2.6^{-10}\sqrt{R}$$
$$\boxed{E_{NO} = 41nV_{RMS}/\sqrt{Hz}}$$

For example,

E_{NO} within a 100Hz BW = $410nV_{RMS}$
= $2460nV_{P-P}$ with a crest factor of 6 (statistically includes 99.7% of all noise peak occurrences)

This is the noise due to the resistors alone. It is included in the noise specification of the INA105.

APPLICATIONS CIRCUITS

The INA105 is ideally suited for a wide range of circuit functions. Figures 4 through 29 show many applications circuits ranging from difference amplifiers and single-ended gain blocks to average and absolute value amplifiers. It is ideal as a current-loop receiver. Also, since the positive output current drive has been extended, it serves uniquely as a current transmitter for ranges such as 4mA to 20mA.

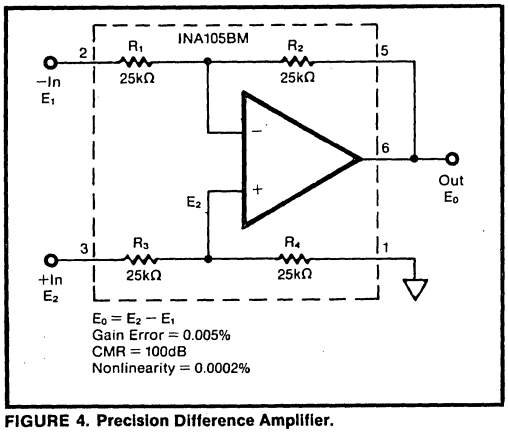
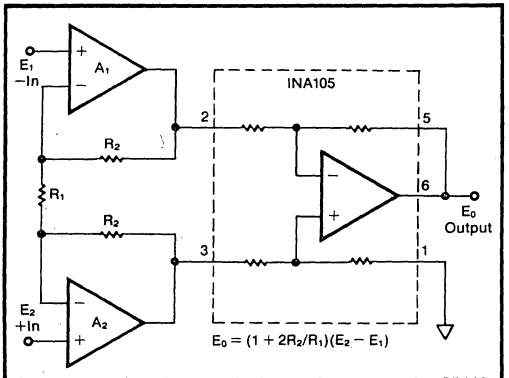


FIGURE 4. Precision Difference Amplifier.



For low source impedance applications, an input stage using OPA37 op amps will give the best low noise, offset, and temperature drift performance. At source impedances above about 10kΩ, the bias current noise of the OPA37 reacting with the input impedance begins to dominate the noise performance. For these applications, using the OPA111 or Dual OPA2111 FET input op amp will provide lower noise performance. For lower cost use the OPA121 plastic. To construct an electrometer use the OPA128.

A_1, A_2	R_1 (Ω)	R_2 (Ω)	Gain (V/V)	CMRR (dB)	Max I_B	Noise at 1kHz (nV/√Hz)
OPA37A	50.5	2.5k	100	128	40nA	4
OPA111B	202	10k	100	110	1pA	10
OPA128LM	202	10k	100	118	75fA	38

FIGURE 5. Precision Instrumentation Amplifier.

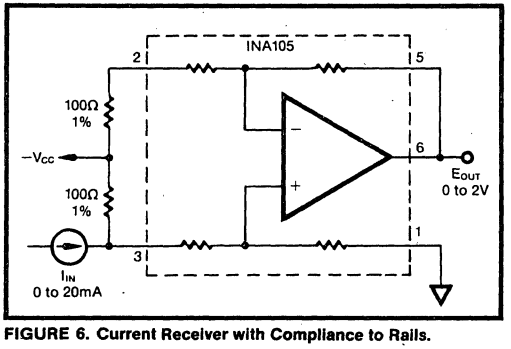


FIGURE 6. Current Receiver with Compliance to Rails.

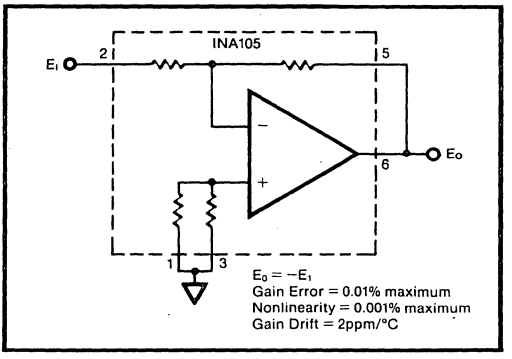


FIGURE 7. Precision Unity-Gain Inverting Amplifier.

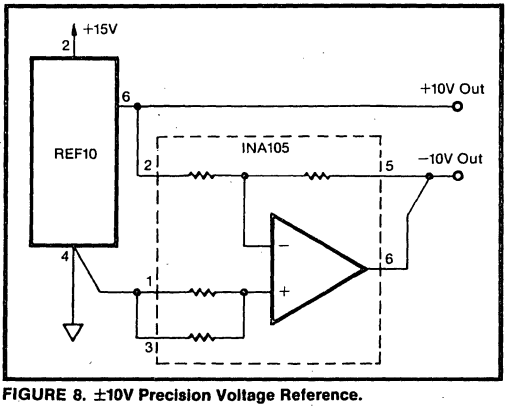


FIGURE 8. ±10V Precision Voltage Reference.

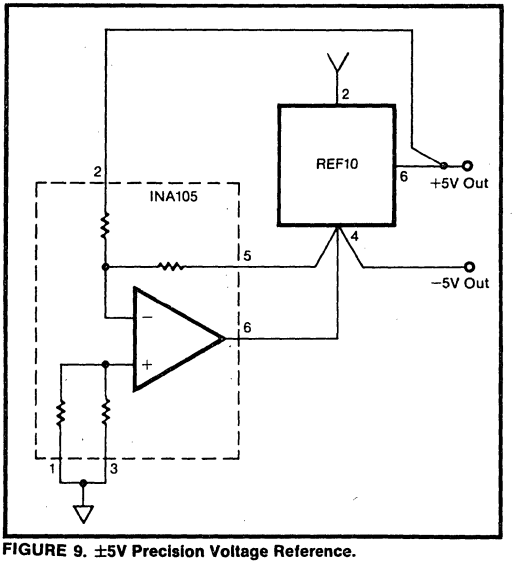


FIGURE 9. ±5V Precision Voltage Reference.

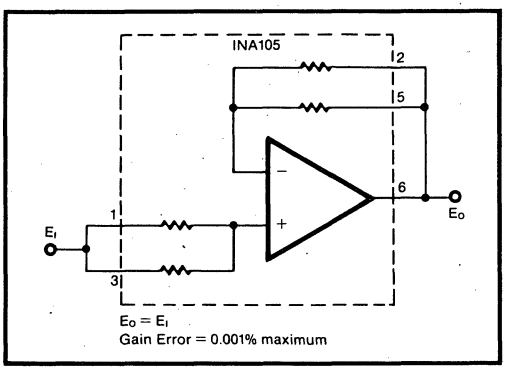


FIGURE 10. Precision Unity-Gain Buffer.

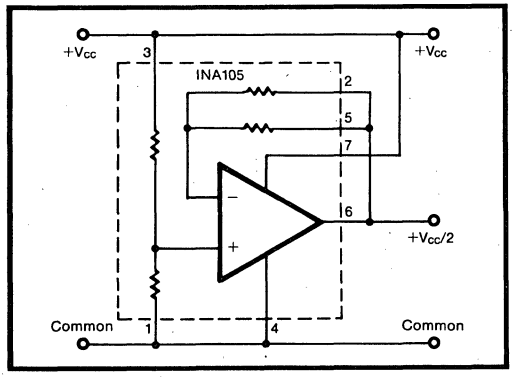


FIGURE 11. Pseudoground Generator.

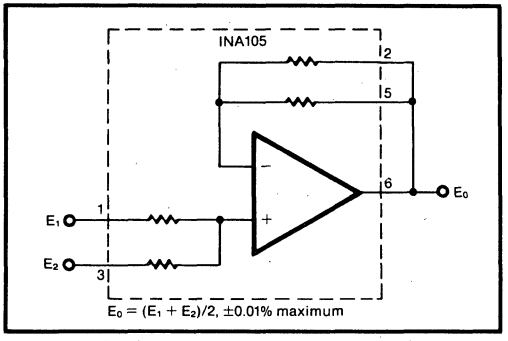


FIGURE 12. Precision Average Value Amplifier.

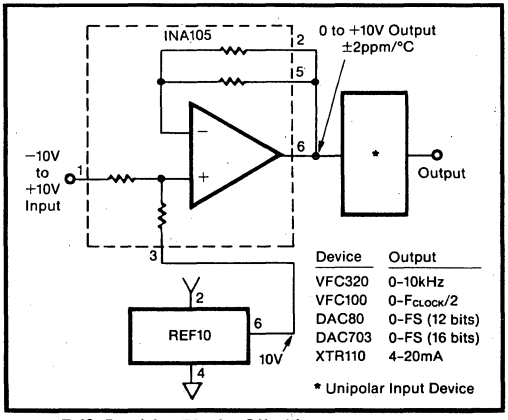


FIGURE 13. Precision Bipolar Offsetting..

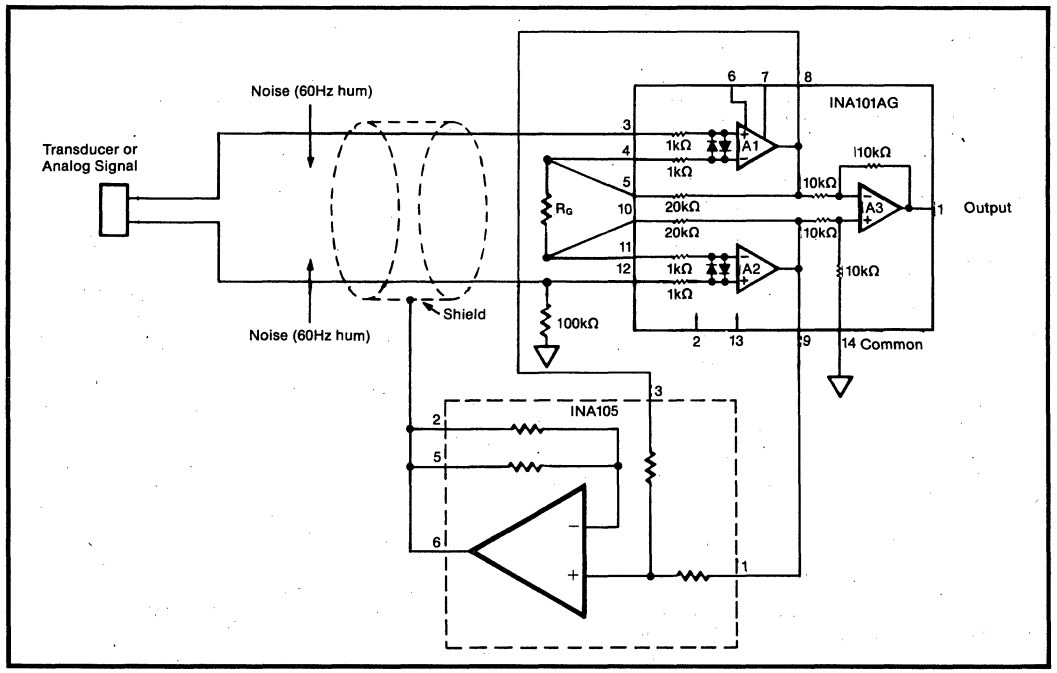


FIGURE 14. Instrumentation Amplifier Guard Drive Generation.

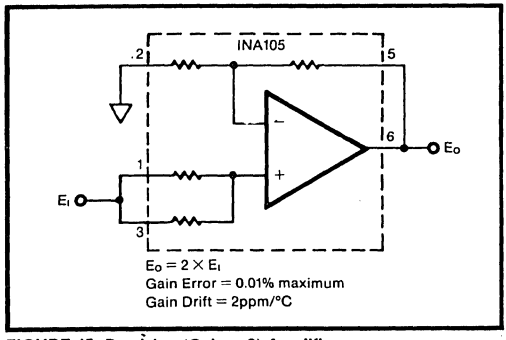


FIGURE 15. Precision (Gain = 2) Amplifier.

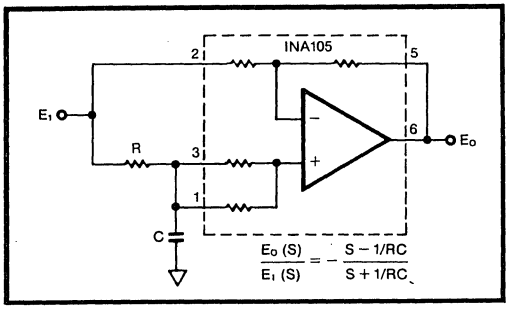


FIGURE 16. All-Pass Filter (provides unity gain and 0° to 180° phase shift output for frequencies of DC to ∞Hz).

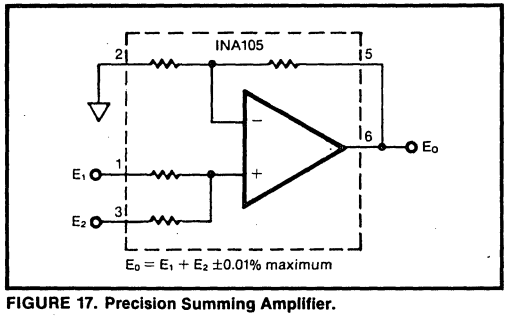


FIGURE 17. Precision Summing Amplifier.

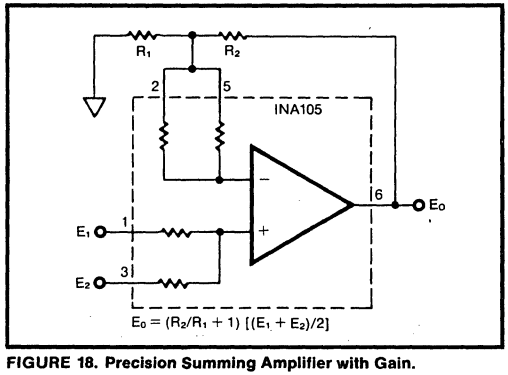


FIGURE 18. Precision Summing Amplifier with Gain.

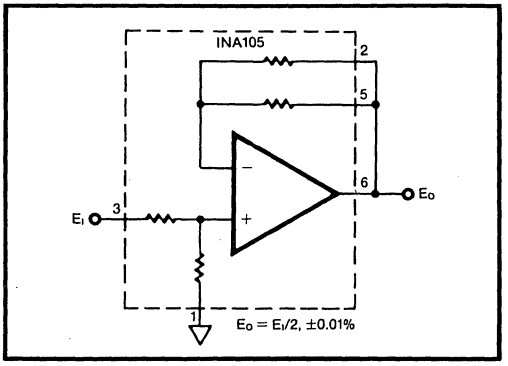


FIGURE 19. Precision (Gain = 1/2) Amplifier. Allows ±20V Input with ±15V Power Supplies.

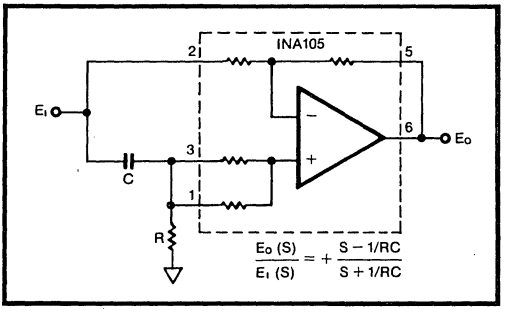


FIGURE 20. All-Pass Filter (provides unity gain and −180° to 0° phase shift output for frequencies of DC to ∞Hz).

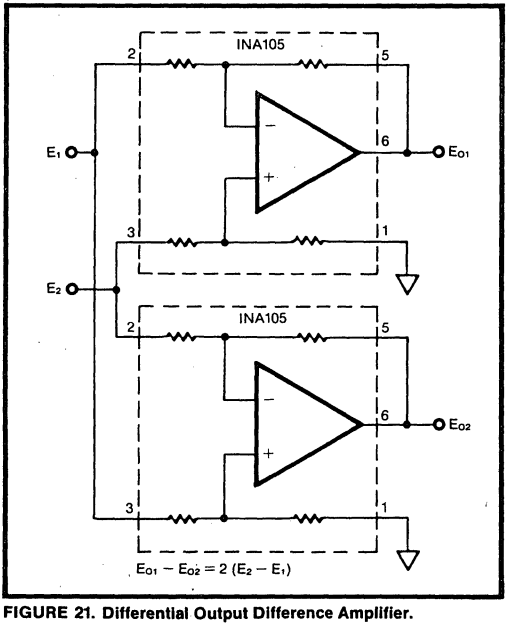


FIGURE 21. Differential Output Difference Amplifier.

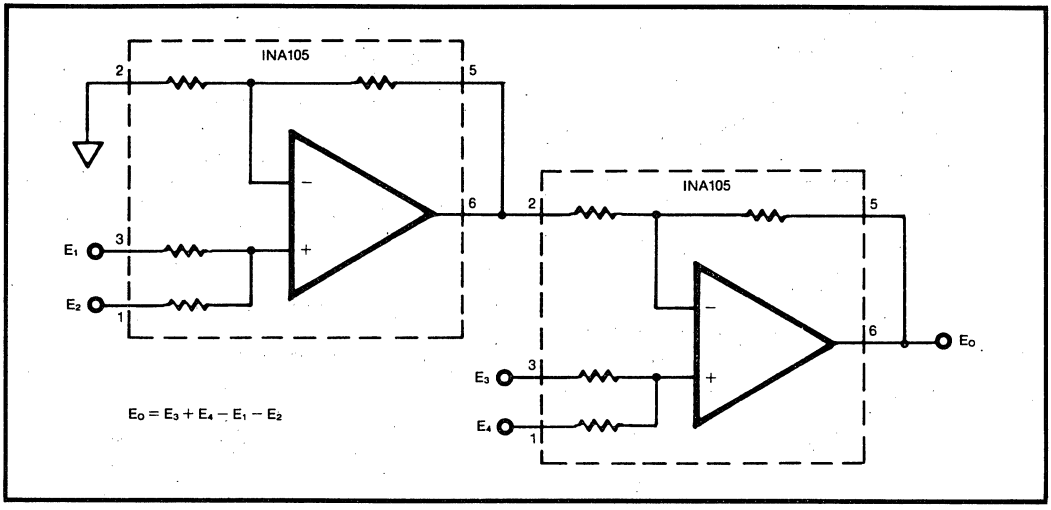


FIGURE 22. Precision Summing Instrumentation Amplifier.

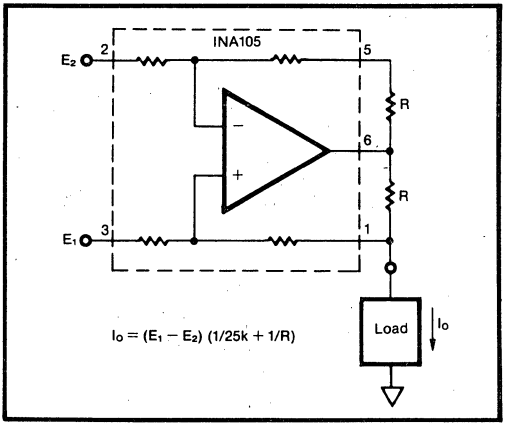


FIGURE 23. Precision Voltage-to-Current Converter with Differential Inputs.

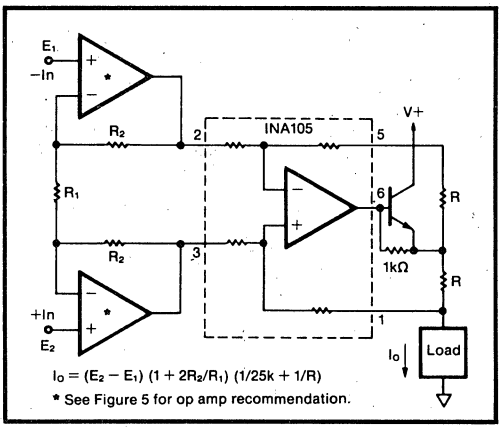


FIGURE 25. Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain.

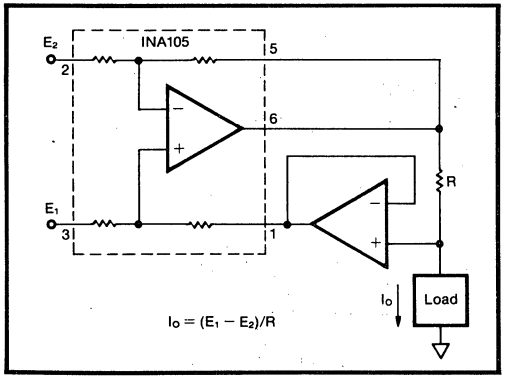


FIGURE 24. Differential Input Voltage-to-Current Converter for Low I_{OUT}.

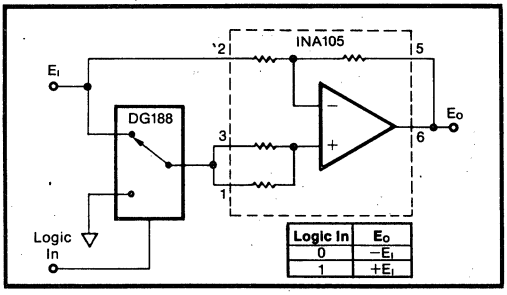


FIGURE 26. Digitally-Controlled Gain of ±1 Amplifier.

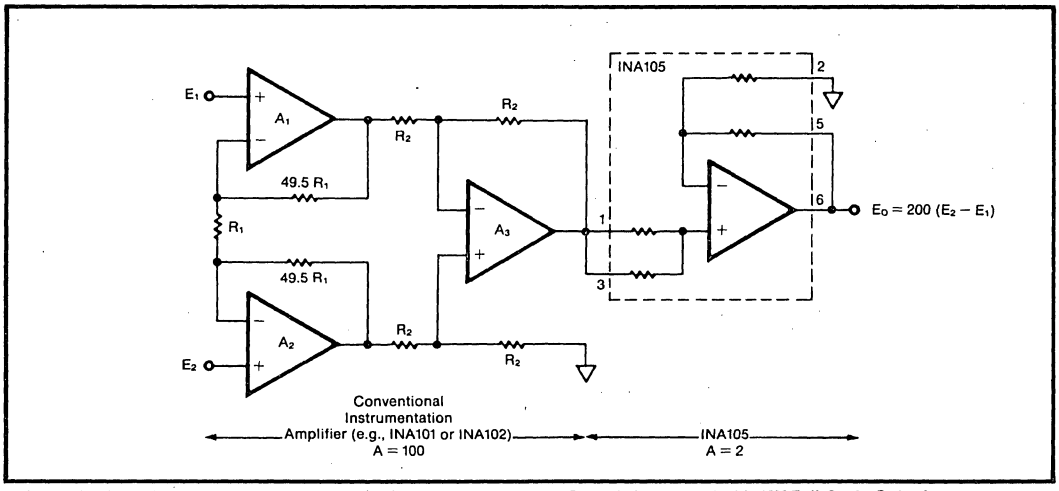


FIGURE 27. Boosting Instrumentation Amplifier Common-Mode Range From ±5V to ±7.5V with 10V Full-Scale Output.

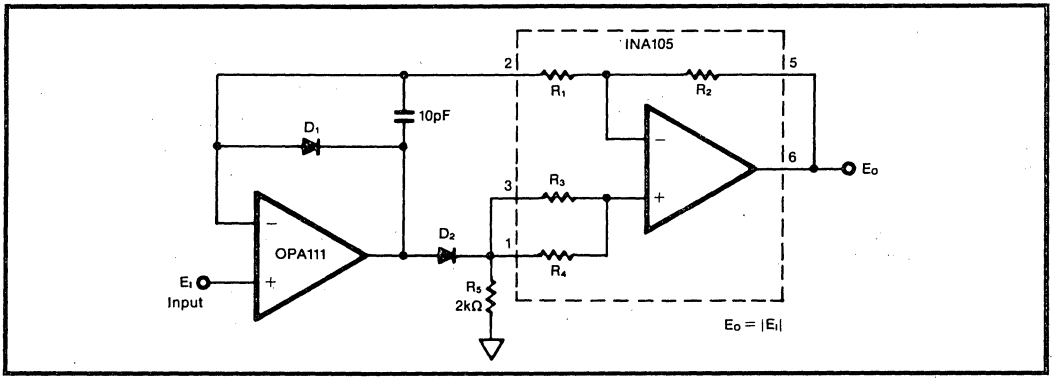


FIGURE 28. Precision Absolute Value Buffer.

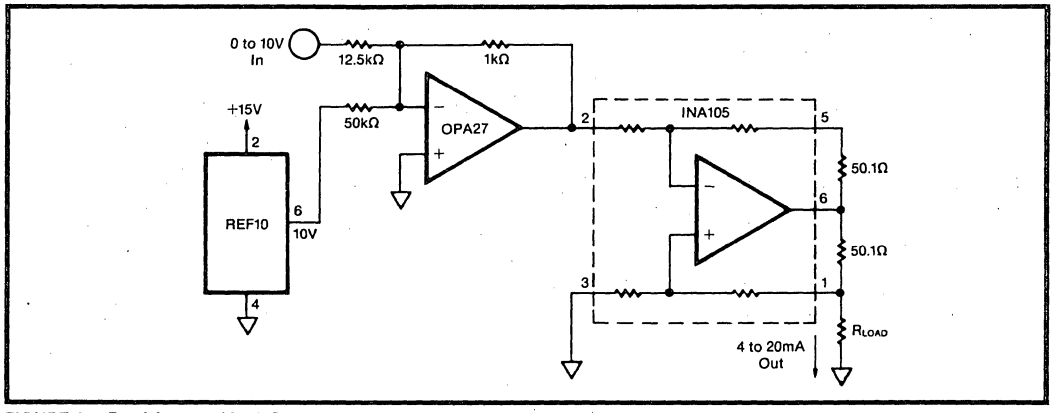


FIGURE 29. Precision 4 to 20mA Current Transmitter.

BURR-BROWN®

INA110

Fast-Settling FET-Input Very High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- LOW BIAS CURRENT: 50pA, max
- FAST SETTLING: 4μs to 0.01%
- HIGH CMR: 106dB, min; 90dB at 10kHz
- CONVENIENT INTERNAL GAINS: 1, 10, 100, 200, 500
- VERY-LOW GAIN DRIFT: 10 to 50ppm/°C
- LOW OFFSET DRIFT: 2μV/°C
- LOW COST
- PINOUT COMPATIBLE WITH AD524 AND AD624, allowing upgrading of many existing applications

APPLICATIONS

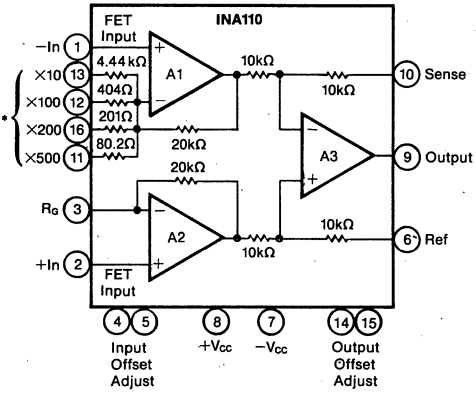
- Fast scanning rate multiplexed input data acquisition system amplifier
- Fast differential pulse amplifier
- High speed, low drift gain block
- Amplification of low level signals from high impedance sources and sensors
- Instrumentation amplifier with input low pass filtering using large series resistors
- Instrumentation amplifier with overvoltage input protection using large series resistors
- Amplification of signals from strain gauges, thermocouples, and RTDs

DESCRIPTION

The INA110 is a monolithic FET input instrumentation amplifier with a maximum bias current of 50pA. The circuit provides fast settling of 4μs to 0.01%. Laser trimming guarantees exceptionally good DC performance. Voltage noise is low, and current noise is virtually zero. Internal gain set resistors guarantee high gain accuracy and low gain drift. Gains of 1, 10, 100, 200, and 500 are provided.

The inputs are inherently protected by P-channel FETs on each input. Differential and common-mode voltages should be limited to $\pm V_{CC}$. When severe overvoltage exists, use diode clamps as shown in the application section.

The INA110 is ideally suited for applications requiring large input resistors for overvoltage protection or filtering. Input signals from high source impedances can easily be handled without degrading DC performance. Fast settling for rapid scanning data acquisition systems is now achievable with one component, the INA110.



* Connect to R_G for desired gain.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 15VDC, R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	INA110AG MIN	INA110AG TYP	INA110AG MAX	INA110BG MIN	INA110BG TYP	INA110BG MAX	UNITS
GAIN								
Range of Gain		1		800	*		*	V/V
Gain Equation[1]				G = 1 + [40K/(R_G + 50Ω)]				V/V
Gain Error, DC: G = 1			0.002	0.04		*	0.02	%
G = 10			0.01	0.1		0.005	0.05	%
G = 100			0.02	0.2		0.01	0.1	%
G = 200			0.04	0.4		0.02	0.2	%
G = 500			0.1	1.0		0.05	0.5	%
Gain Temp. Coefficient: G = 1			±3	±20		*	±10	ppm/°C
G = 10			±4	±20		±2	±10	ppm/°C
G = 100			±6	±40		±3	±20	ppm/°C
G = 200			±10	±60		±5	±30	ppm/°C
G = 500			±25	±100		±10	±50	ppm/°C
Nonlinearity, DC: G = 1			±0.001	±0.01		±0.0005	±0.005	% of FS
G = 10			±0.002	±0.01		±0.001	±0.005	% of FS
G = 100			±0.004	±0.02		±0.002	±0.01	% of FS
G = 200			±0.006	±0.02		±0.003	±0.01	% of FS
G = 500			±0.01	±0.04		±0.005	±0.02	% of FS
OUTPUT								
Voltage, R_L = 2kΩ	Over temp	±10	±12.7		*	*		V
Current	Over temp	±5	±25		*	*		mA
Short-Circuit Current			±25			*		mA
Capacitive Load	Stability		5000			*		pF
INPUT								
OFFSET VOLTAGE[2]								
Initial Offset			±(100+1000/G)	±(500+5000/G)		±(50+600/G)	±(250+3000/G)	µV
vs Temperature			±(2+20/G)	±(5+100/G)		±(1+10/G)	±(2+50/G)	µV/°C
vs Supply	V_{CC} = ±6V to ±18V		±(4+60/G)	±(30+300/G)		±(2+30/G)	±(10+180/G)	µV/V
BIAS CURRENT								
Initial Bias Current	Each input		20	100		10	50	pA
Initial Offset Current			2	50		1	25	pA
Impedance: Differential			$5\times10^{12}\|\|6$			*		Ω||pF
Common-Mode			$2\times10^{12}\|\|1$			*		Ω||pF
VOLTAGE RANGE	V_{IN} Diff. = 0V[3]							
Range, Linear Response		±10	±12					V
CMR with 1kΩ Source Imbalance:								
G = 1	DC	70	90		80	100		dB
G = 10	DC	87	104		96	112		dB
G = 100	DC	100	110		106	116		dB
G = 200	DC	100	110		106	116		dB
G = 500	DC	100	110		106	116		dB
NOISE, Input[4]								
Voltage, f_O = 10kHz			10			*		$nV/\sqrt{Hz}$
f_B = 0.1Hz to 10Hz			1			*		µVp-p
Current, f_O = 10kHz			1.8			*		$fA/\sqrt{Hz}$
NOISE, Output[4]								
Voltage, f_O = 10kHz			65			*		$nV/\sqrt{Hz}$
f_B = 0.1Hz to 10Hz			8			*		µVp-p
DYNAMIC RESPONSE								
Small Signal: G = 1	−3dB		2.5			*		MHz
G = 10			2.5			*		MHz
G = 100			470			*		kHz
G = 200			240			*		kHz
G = 500			100			*		kHz
Full Power	V_{OUT} = ±10V, R_L = 2kΩ	190	270		*	*		kHz
Slew Rate	G = 1 to 200	12	17		*	*		V/µs
Settling Time:								
0.1%, G = 1	V_O = 20V step		4			*		µs
G = 10			2			*		µs
G = 100			3			*		µs
G = 200			5			*		µs
G = 500			11			*		µs

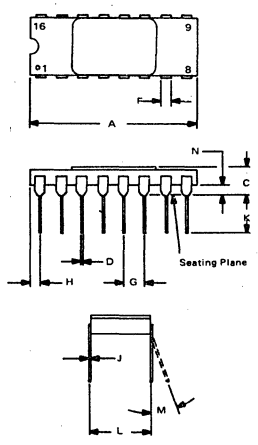
ELECTRICAL (CONT)

PARAMETER	CONDITIONS	INA110AG MIN	INA110AG TYP	INA110AG MAX	INA110BG MIN	INA110BG TYP	INA110BG MAX	UNITS
Settling Time:								
0.01%, G = 1	V_O = 20V step		5	12.5		*	*	µs
G = 10			3	7.5		*	*	µs
G = 100			4	7.5		*	*	µs
G = 200			7	12.5		*	*	µs
G = 500			16	25		*	*	µs
Overload Recovery[5]	50% overdrive		1			*		µs
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range		±6		±18	*		*	V
Quiescent Current	V_O = 0V		±3.0	±4.5		*	*	mA
TEMPERATURE RANGE								
Specification		−25		+85	*		*	°C
Operation		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C
θ_{JA}			100			*		°C/W

* Same as INA110AG.

NOTES: (1) Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 11, 12, and 16. Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. (2) Adjustable to zero. (3) For differential input voltage other than zero, see Typical Performance Curves. (4) $V_{NOISE\ RTI} = \sqrt{V_{N\ INPUT}^2 + (V_{N\ OUTPUT}/Gain)^2}$. (5) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.

MECHANICAL



Note: Leads in true position within 0.10" (0.25mm) R at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

PIN CONFIGURATION

−In	1	16	×200
+In	2	15	Output Offset Adjust
R_G	3	14	Output Offset Adjust
Input Offset Adjust	4	13	×10
Input Offset Adjust	5	12	×100
Reference	6	11	×500
−Vcc	7	10	Output Sense
+Vcc	8	9	Output

ORDERING INFORMATION

INA110 X G

Basic Model Number

Performance Grade Code
A, B: −25°C to +85°C

Package Code
G: 16-Pin Hermetic DIP

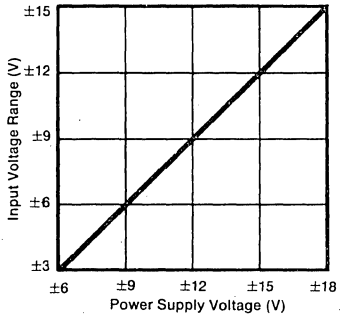
ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18V
Input Voltage Range ..... ±Vcc
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (soldering 10 seconds) ..... +300°C
Output Short-Circuit Duration ... Continuous to Common

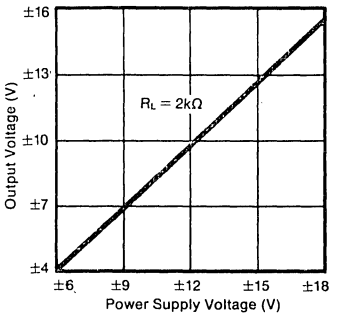
TYPICAL PERFORMANCE CURVES

T_A = 25°C, $\pm V_{CC}$ = 15VDC unless otherwise noted.

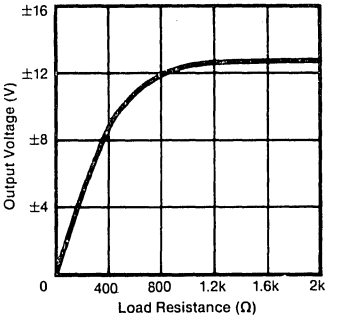
INPUT VOLTAGE RANGE VS SUPPLY



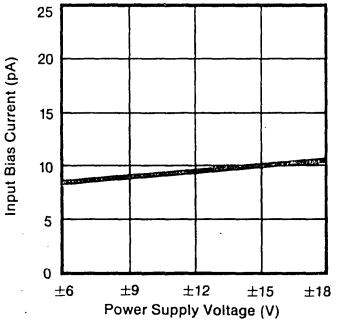
OUTPUT SWING VS SUPPLY



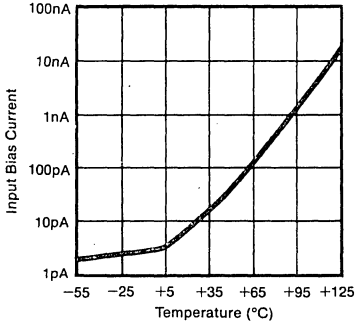
OUTPUT SWING VS LOAD RESISTANCE



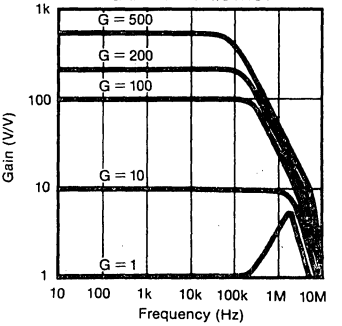
BIAS CURRENT VS SUPPLY



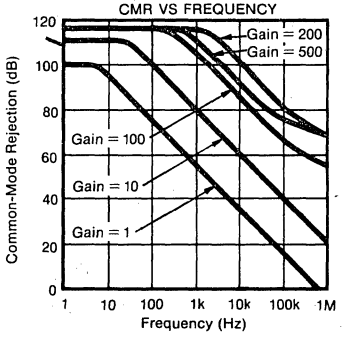
BIAS CURRENT VS TEMPERATURE



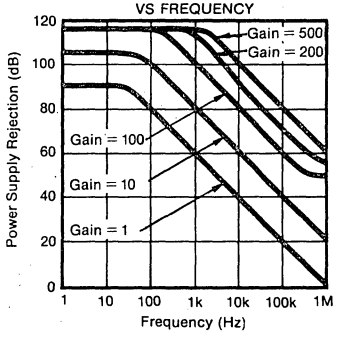
GAIN VS FREQUENCY



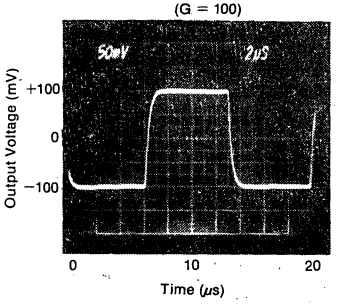
CMR VS FREQUENCY



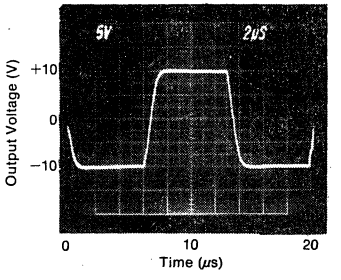
POWER SUPPLY REJECTION VS FREQUENCY



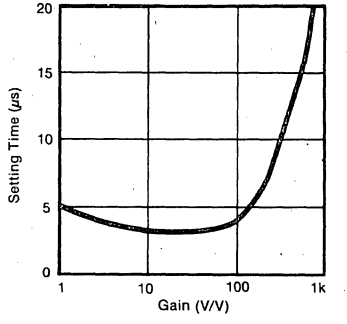
SMALL SIGNAL TRANSIENT RESPONSE (G = 100)



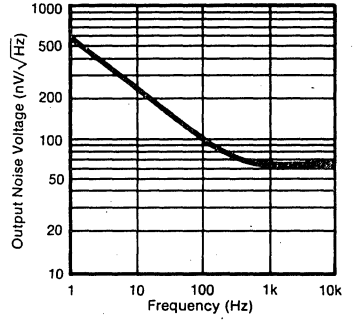
LARGE SIGNAL TRANSIENT RESPONSE (G = 100)



SETTLING TIME VS GAIN (0.01%, 20V STEP)



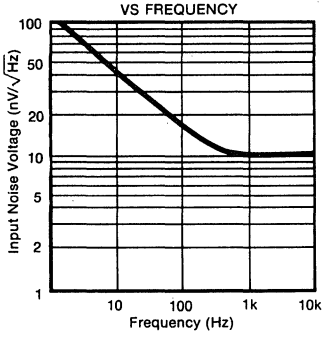
OUTPUT NOISE VOLTAGE VS FREQUENCY



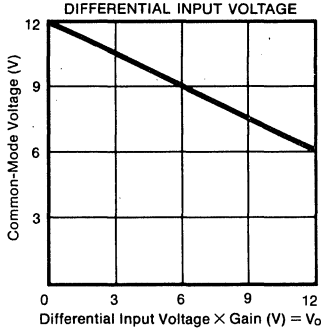
TYPICAL PERFORMANCE CURVES (CONT)

T_A = 25°C, ±V_{CC} = 15VDC unless otherwise noted.

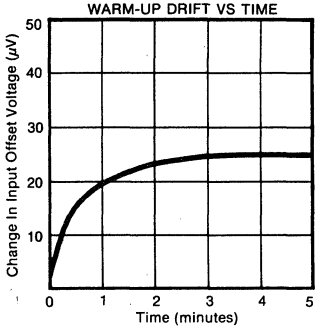
INPUT NOISE VOLTAGE VS FREQUENCY



COMMON-MODE VOLTAGE VS DIFFERENTIAL INPUT VOLTAGE



WARM-UP DRIFT VS TIME



DISCUSSION OF PERFORMANCE

A simplified diagram of the INA110 is shown on the first page. The design consists of the classical three operational amplifier configuration with precision FET buffers on the input. The result is an instrumentation amplifier with premium performance not normally found in integrated circuits.

The input section (A_1 and A_2) incorporates high performance, low bias current, and low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide high input impedance ($10^{12}\Omega$). Laser-trimming is used to achieve low offset voltage. Input cascoding assures low bias current and high CMR. Thin-film resistors on the integrated circuit provide excellent gain accuracy and temperature stability.

The output section (A_3) is connected in a unity-gain difference amplifier configuration. Precision matching of the four 10kΩ resistors, especially over temperature and time, assures high common-mode rejection.

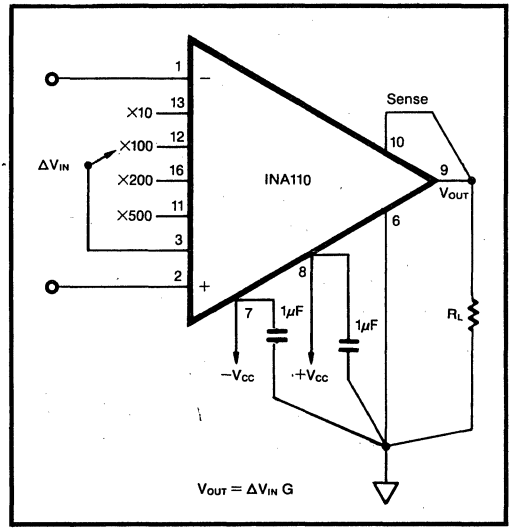


FIGURE 1. Basic Circuit Connection.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1μF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Resistance in series with the reference (pin 6) will degrade CMR. Also to maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins. The layout shown in Figure 2 is suggested for best performance.

OFFSET ADJUSTMENT

Figure 3 shows the offset adjustment circuit for the INA110. Both the offset of the input stage and output stage can be adjusted separately. Notice that the offset referred to the INA110's input (RTI) is the offset of the input stage plus the offset of the output stage divided by

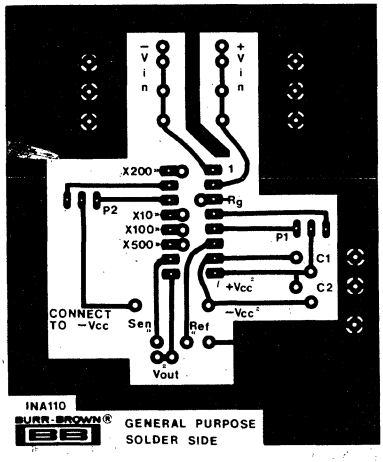


FIGURE 2. Recommended PC Board Layout for INA110.

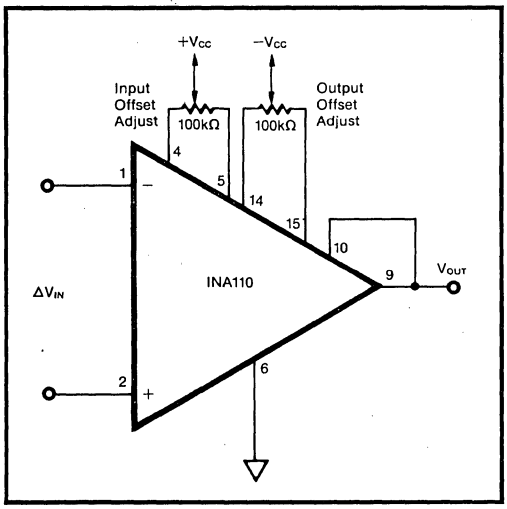


FIGURE 3. Offset Adjustment Circuit.

the gain of the input stage. This allows specification of offset independent of gain.

For systems using computer autozeroing techniques, neither offset nor offset drift are of concern. In many other applications the factory-trimmed offset gives excellent results. When greater accuracy is desired, one adjustment is usually sufficient. In high gains (>100) adjust only the input offset, and in low gains the output offset. For higher precision in all gains, both can be adjusted by first selecting high gain and adjusting input offset and then low gain and adjusting output offset. The offset adjustment will, however, add to the drift by approximately 0.33μV/°C per 100μV of input offset voltage that is adjusted. Therefore, care should be taken when considering use of adjustment.

Output offsetting can be accomplished as shown in Figure 4 by applying a voltage to the reference (pin 6)

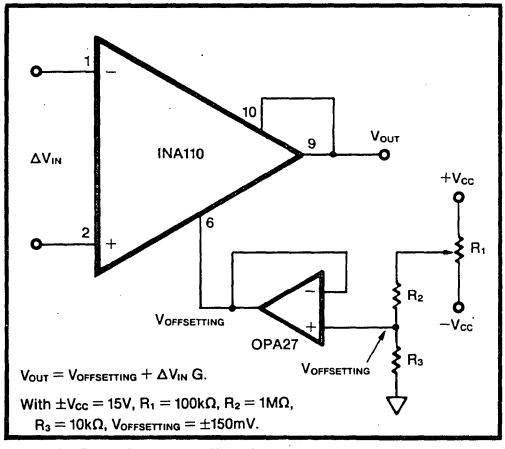


FIGURE 4. Output Offsetting.

through a buffer. This limits the resistance in series with pin 6 to minimize CMR error. Be certain to keep this resistance low. Note that the offset error can be adjusted at this reference point with no appreciable degradation in offset drift.

GAIN SELECTION

Gain selection is accomplished by strapping the appropriate pins together on the INA110. Table I shows possible gains from the internal resistors. Keep the connections as short as possible to maintain accuracy.

TABLE I. Internal Gain Connections.

Gain	Connect pin 3 to pin —	Gain Accuracy (%)	Gain Drift (ppm/°C)
The following gains have guaranteed accuracy:			
1	none	0.02	10
10	13	0.05	10
100	12	0.1	20
200	16	0.2	30
500	11	0.5	50
The following gains have typical accuracy as shown:			
300	12 & 16	0.25	10
600	11 & 12	0.25	40
700	11 & 16	2.0	40
800	11, 12, & 16	2.0	80

Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 12, 16, and 11. Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. The equation for choosing R_G is shown below.

$$R_G = \frac{40k}{G - 1} - 50\Omega$$

Gain can also be changed in the output stage by adding resistance to the feedback loop shown in Figure 5. This is useful for increasing the total gain or reducing the input stage gain to prevent saturation of input amplifiers.

The output gain can be changed as shown in Table II. Matching of R_1 and R_3 is required to maintain high CMR. R_2 sets the gain with no effect on CMR.

TABLE II. Output Stage Gain Control.

Output Stage Gain	R_1 and R_3	R_2
2	1.2kΩ	2.74kΩ
5	1kΩ	511Ω
10	1.5kΩ	340Ω

COMMON-MODE INPUT RANGE

It is important not to exceed the input amplifiers' dynamic range (see Typical Performance Curves). The differential input signal and its associated common-mode voltage should not cause the output of A_1 and A_2 (input amplifiers) to exceed approximately ±10V with ±15V supplies or nonlinear operation will result. Such large common-mode voltages, when the INA110 is in high gain, can cause saturation of the input stage even though the differential input is very small. This can be avoided by reducing the input stage gain and increasing the output stage gain with an H pad attenuator (see Figure 5).

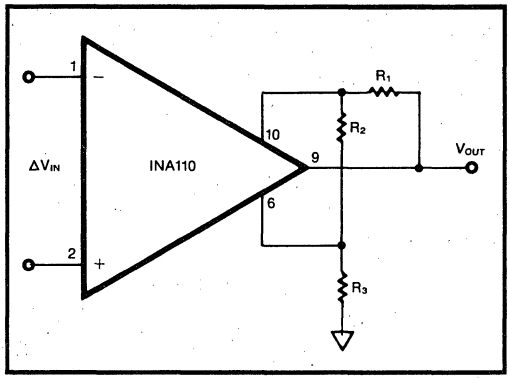


FIGURE 5. Gain Adjustment of Output Stage Using H Pad Attenuator.

OUTPUT SENSE

An output sense has been provided to allow greater accuracy in connecting the load. By attaching this feedback point to the load at the load site, IR drops due to load currents are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more current is to be supplied, a power booster can be placed within the feedback loop as shown in Figure 6. Buffer errors are minimized by the loop gain of the output amplifier.

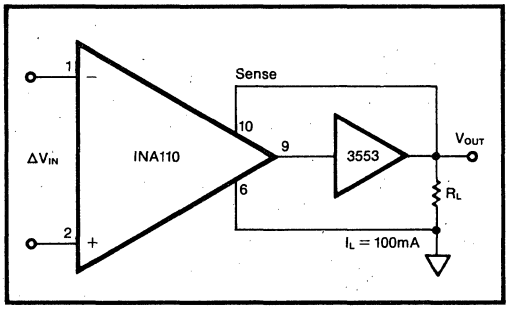


FIGURE 6. Current Boosting the Output.

LOW BIAS CURRENT OF FET INPUT ELIMINATES DC ERRORS

Because the INA110 has FET inputs, bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp levels produce no more than microvolts through megohm sources. Thus, input filtering and input series protection are readily achievable.

A return path for the input bias currents must always be provided to prevent charging of stray capacitance. Otherwise the output can wander and saturate. A 1MΩ to 10MΩ resistor from the input to common will return floating sources such as transformers, thermocouples, and AC-coupled inputs (see Applications section).

DYNAMIC PERFORMANCE

The INA110 is a fast-settling FET input instrumentation amplifier. Therefore, careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with input capacitance to reduce the overall bandwidth. Also, to maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins (see Figure 2 for PC board layout).

When using high source resistance (>20kΩ) in the positive input only, bypass it to ground with at least 50pF to maintain stability.

The INA110 is designed for fast settling with easy gain selection. It has especially excellent settling in high gain. It can also be used in fast-settling unity-gain applications. As with all such amplifiers, the INA110 does exhibit signficant gain peaking when set to a gain of 1. It is, however, unconditionally stable. The gain peaking can be cancelled by band-limiting the negative input to 400kHz with a simple external RC circuit for applications requiring flat response.

Another distinct advantage of the INA110 is the high frequency CMR response. High frequency noise and sharp common-mode transients will be rejected. To preserve AC CMR, be sure to minimize stray capacitance on the input lines. Matching the RCs in the two inputs will help to maintain high AC CMR.

APPLICATIONS

In addition to general purpose uses, the INA110 is designed to accurately handle two important and demanding applications: (1) inputs with high source impedances such as capacitance/crystal/photodetector sensors and low-pass filters and series-input protection devices, and (2) rapid-scanning data acquisition systems requiring fast settling time. Because the user has access to the output sense, current sources can also be constructed using a minimum of external components. Figures 7 through 24 show application circuits.

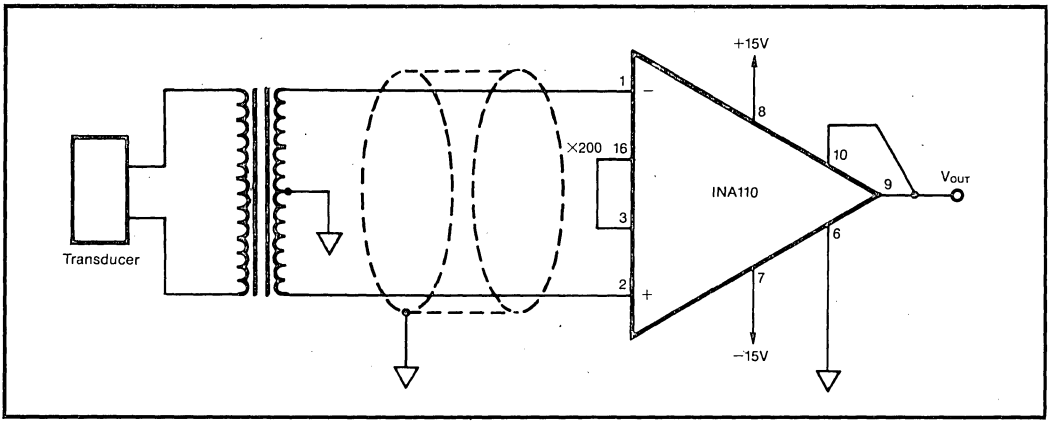


FIGURE 7. Transformer-Coupled Amplifier.

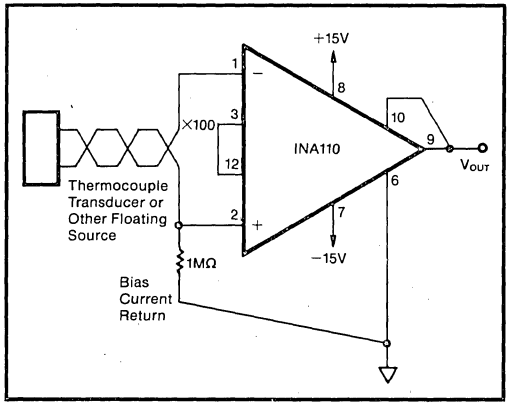


FIGURE 8. Floating Source Instrumentation Amplifier.

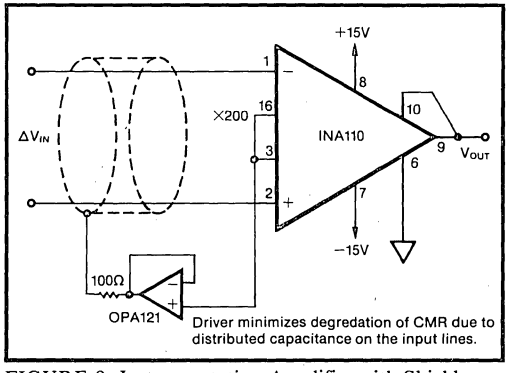


FIGURE 9. Instrumentation Amplifier with Shield Driver.

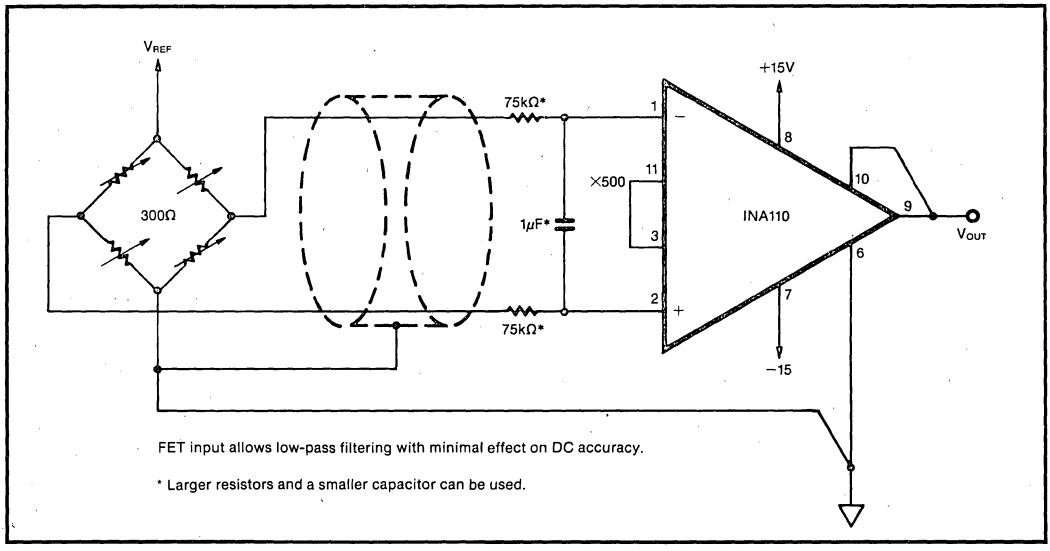


FIGURE 10. Bridge Amplifier with 1Hz Low-Pass Input Filter.

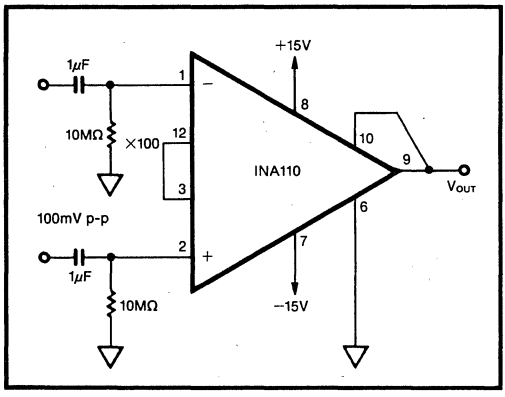


FIGURE 11. AC-Coupled Differential Amplifier for Frequencies Greater Than 0.016Hz.

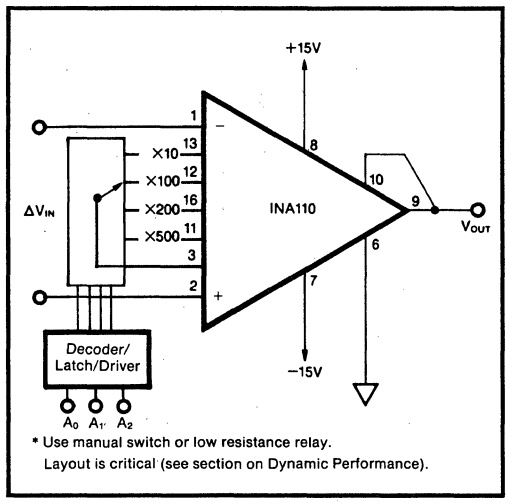


FIGURE 12. Programmable-Gain Instrumentation Amplifier (Precision Noninverting or Inverting Buffer with Gain).

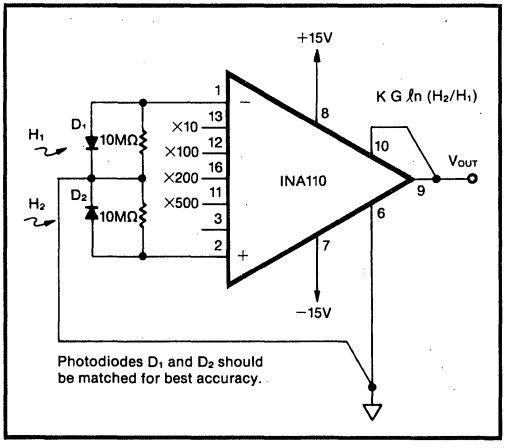


FIGURE 13. Ratiometric Light Amplifier (Absorbance Measurement).

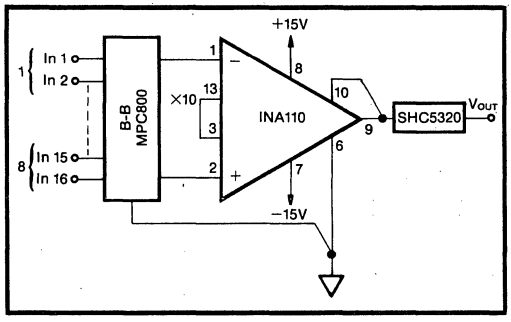


FIGURE 14. Rapid-Scanning-Rate Data Acquisition Channel with 5μs Settling to 0.01%.

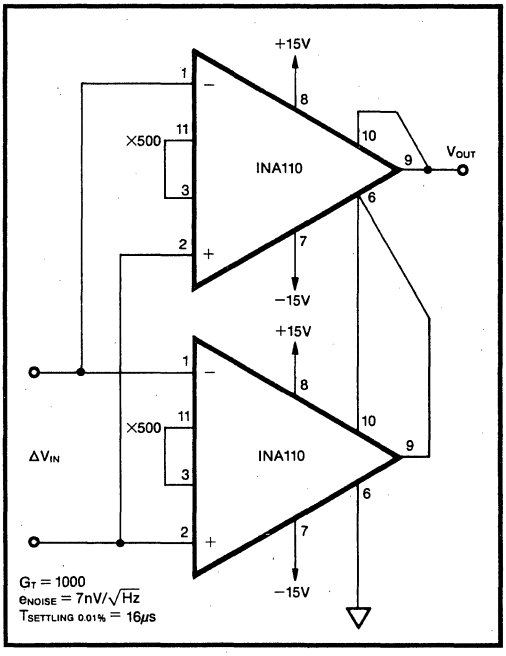


FIGURE 15. Fast-Settling Low-Noise Instrumentation Amplifier with Gain of 1000.

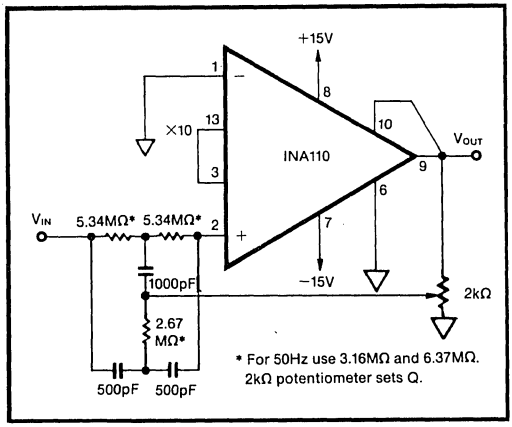


FIGURE 16. Precision Gain-of-10 Amplifier with 60Hz Input Notch Filter.

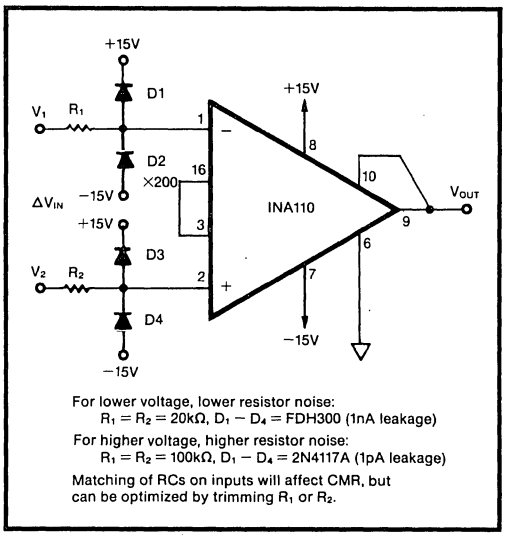


FIGURE 17. Input-Protected Instrumentation Amplifier with Minimal Degradation of DC Accuracy.

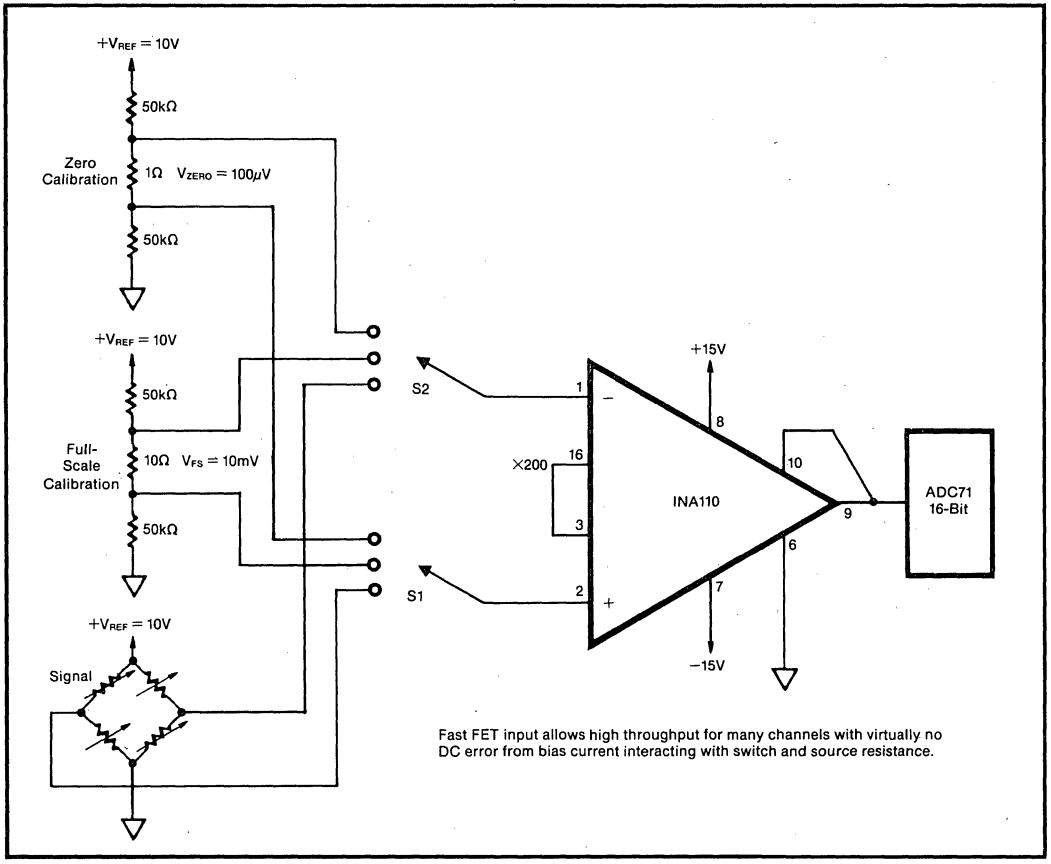


FIGURE 18. Load Cell Weighing Scale Instrumentation Amplifier.

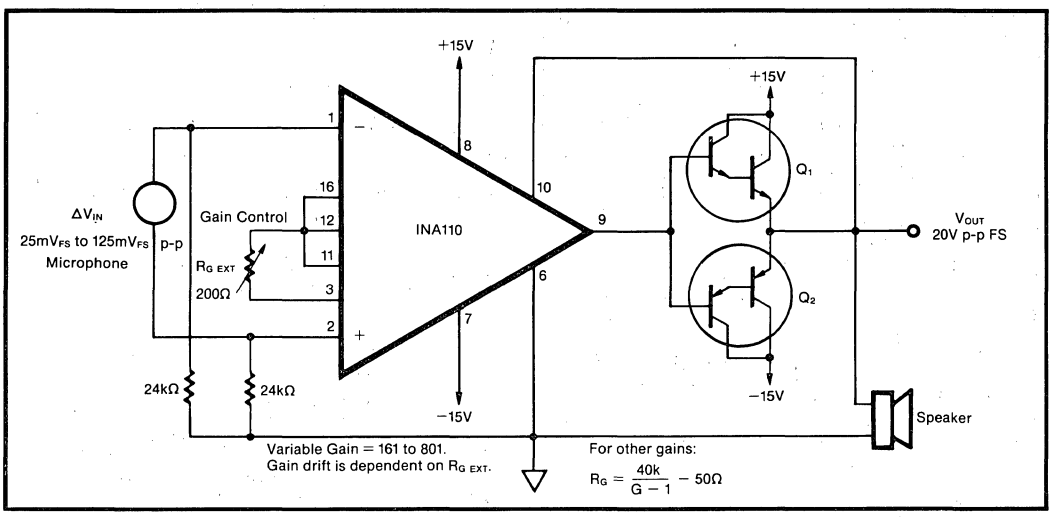


FIGURE 19. Differential Input Power Amplifier.

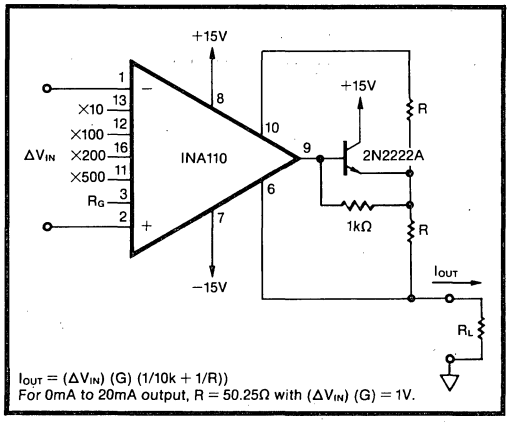


FIGURE 20. Differential Input FET Buffered Current Source.

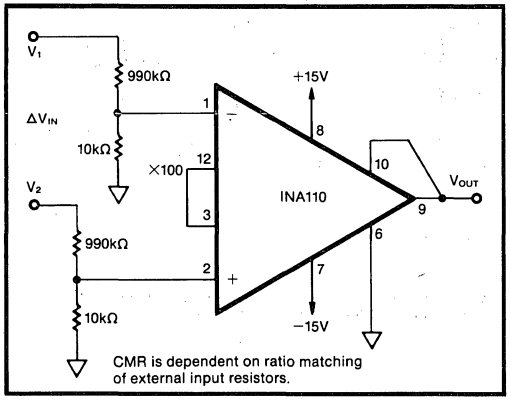


FIGURE 21. Unity-Gain Differential Amplifier with Common-Mode Voltage Range of 1000V.

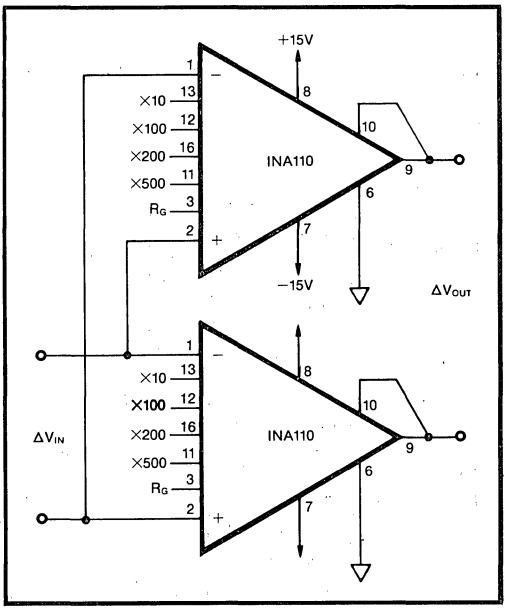
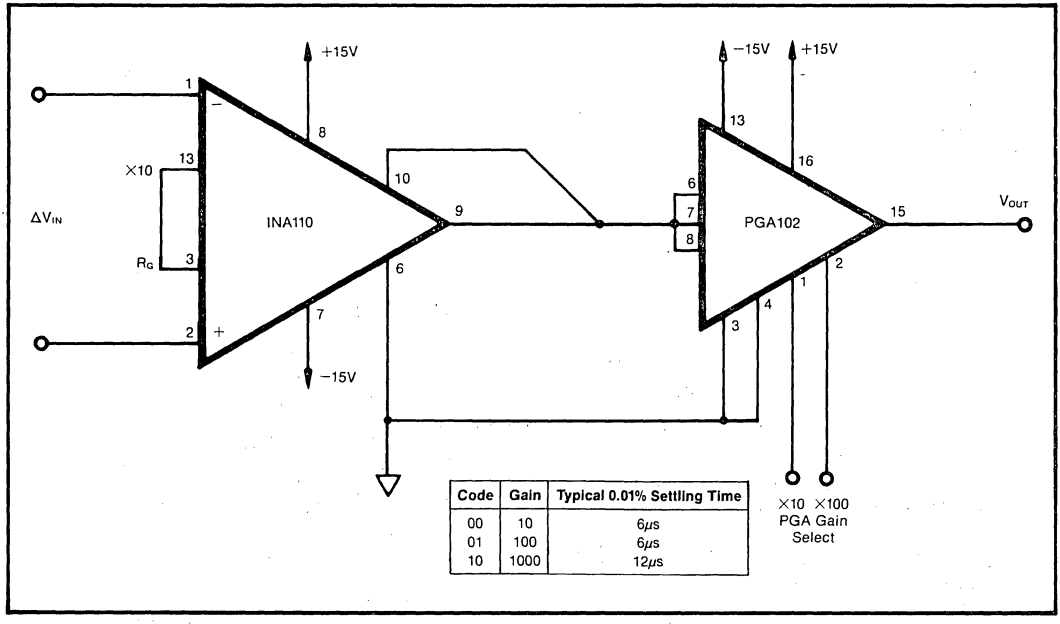


FIGURE 22. Differential Input/Differential Output Amplifier.



Code	Gain	Typical 0.01% Settling Time
00	10	6μs
01	100	6μs
10	1000	12μs

FIGURE 23. Digitally-Controlled Fast-Settling Programmable-Gain Instrumentation Amplifier.

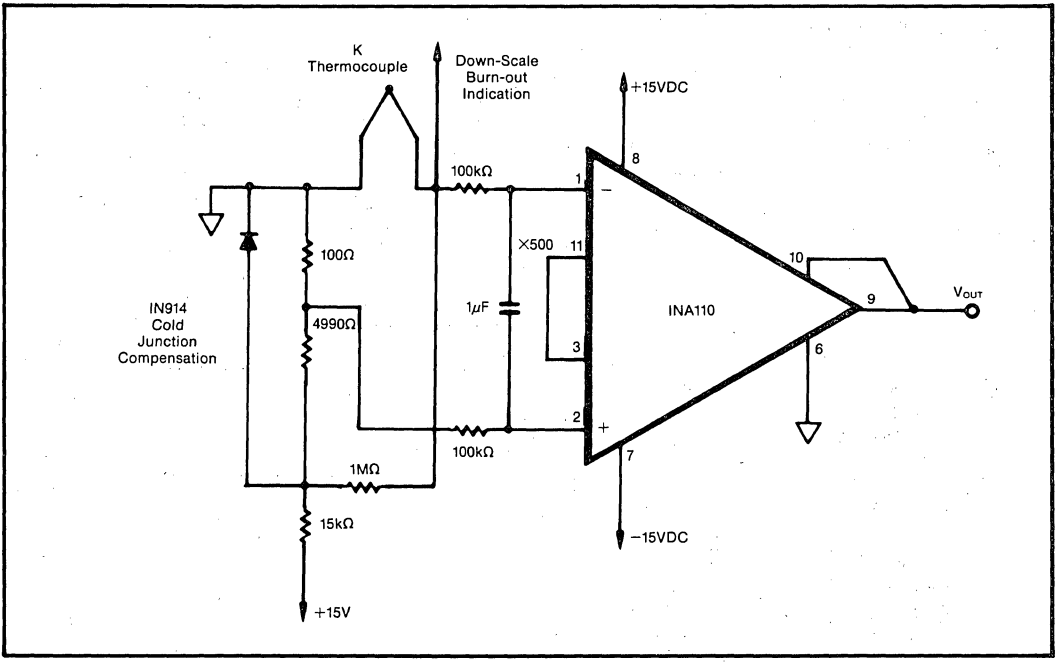


FIGURE 24. Thermocouple Amplifier with Cold Junction Compensation and Input Low-Pass Filtering (<1Hz).

BURR-BROWN®

PGA100

Digitally-Controlled Programmable Gain/Multiplexed Input OPERATIONAL AMPLIFIER

FEATURES

- HIGH GAIN ACCURACY, ±0.02%, max (B grade)
- LOW NONLINEARITY, ±0.005%, max (B grade)
- FAST SETTLING, 5μsec to 0.01%
- LOW CHANNEL-TO-CHANNEL CROSSTALK, ±0.003%
- INPUT PROTECTION, ±20V, max above $\pm V_{CC}$
- 8 ANALOG INPUT CHANNELS WITH HIGH Z_{IN}, $10^{11}\Omega$
- 8 BINARY GAINS 1, 2, 4, 8, 16, 32, 64, 128 (V/V)
- FULLY MICROPROCESSOR-COMPATIBLE

APPLICATIONS

- DATA ACQUISITION SYSTEM AMPLIFIER
- SOFTWARE ERROR CORRECTION
- AUTO-ZEROING CAPABILITY
- DIGITALLY-CONTROLLED AUTORANGING SYSTEM
- TEST EQUIPMENT
- REMOTE INSTRUMENTATION SYSTEM
- SYSTEM DYNAMIC RANGE AND RESOLUTION IMPROVEMENT

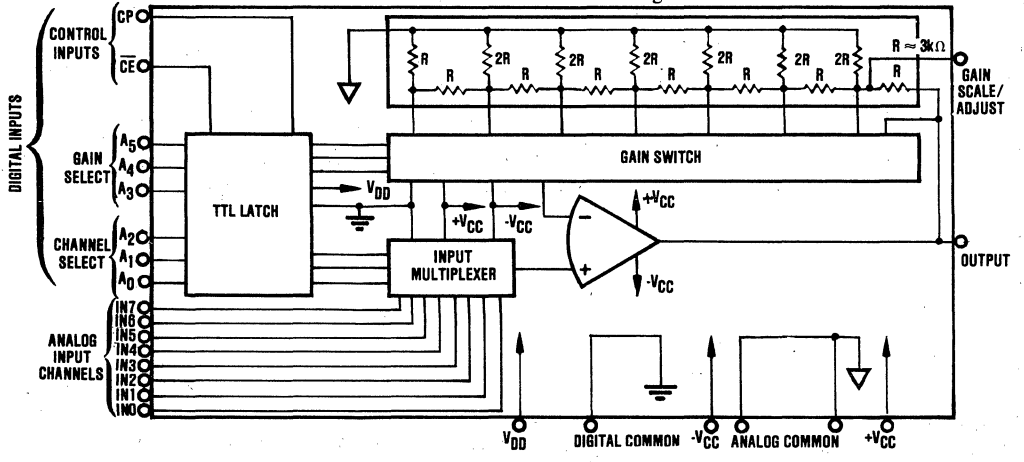
DESCRIPTION

The PGA100 is a precision, digitally-programmable-gain multiplexed-input amplifier. The user can select any one of eight analog input channels simultaneously with any one of eight noninverting binarily weighted gain steps from 1 to 128 (V/V). The digital gain and channel select are latchable for microprocessor interface. Also, the fast 5μsec settling time is ideal for rapid channel scanning in data acquisition systems.

Precision laser-trimming of both offset voltage and gain accuracy, with good temperature tracking of feedback resistor ratios, permits direct use without adjustments. However, hardware or software correction of errors is readily achievable.

In addition, gain scaling to gains other than 1 to 128V/V can easily be accomplished.

Microcircuit construction and the use of laser-trimmed thin-film feedback resistors achieve high accuracy, small size, and low cost not obtained with discrete designs.



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PDS-457A

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C, ±V_{CC} = 15VDC, V_{DD} = +5VDC unless otherwise noted.

PARAMETER	CONDITIONS	PGA100AG MIN	PGA100AG TYP	PGA100AG MAX	PGA100BG MIN	PGA100BG TYP	PGA100BG MAX	UNITS
GAIN, G								
Inaccuracy(1)	G = 1 to 128, I_o = 1mA		±0.01	±0.05		±0.005	±0.02	%
vs Temperature(2)	-25°C ≤ T_A ≤ +85°C		±5	±10		•	•	ppm/°C
vs Time			±0.001			•		%/1000 hrs.
Nonlinearity(3)	G = 1 to 128, I_o = 1mA		±0.004	±0.01		±0.002	±0.005	% of FS
vs Temperature(2)	-25°C ≤ T_A ≤ +85°C		±2	±5		•	•	ppm/°C
vs Time			±0.001			•		%/1000 hrs.
Warm-up Time		1			•			min
RATED OUTPUT								
Voltage	I_o = ±2mA	±10			•			V
Current	V_o = ±10V	±2			•			mA
Output Resistance	G ≤ 128		0.05			•		Ω
Short Circuit Current			±15			•		mA
Capacitive Load Range	Phase Margin ≥ 25°		1000			•		pF
INPUT OFFSET VOLTAGE								
Initial	T_A = +25°C		±0.1	±1		±0.05	±0.5	mV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±6			•		µV/°C
vs Supply Voltage	±8VDC ≤ | V_{CC} | ≤ ±18VDC		±10	±80		•	•	µV/V
vs Time			±15			•		µV/mo.
INPUT BIAS CURRENT								
Initial	T_A = +25°C							
"OFF" Channel			±10			•		pA
"ON" Channel			±0.1			•	±1	nA
vs Temperature			Note 4			•		
INPUT DIFFERENCE CURRENT, BETWEEN CHANNELS								
Initial	T_A = +25°C							
"OFF" Channel			±20			•		pA
"ON" Channel			±0.2			•	±2	nA
vs Temperature			Note 4			•		
ANALOG INPUT CHARACTERISTICS								
Absolute Max Voltage	No damage			±(|Vcc|+20)			•	V
Input Voltage Range	Linear operation	±10			•			V
Input Impedance								
"OFF" Channel			10^{12} || 5			•		Ω || pF
"ON" Channel			10^{11} || 25			•		Ω || pF
INPUT NOISE								
Voltage Noise Density	f_o = 1Hz		200			•		nV/√Hz
	f_o = 10Hz		60			•		nV/√Hz
	f_o = 100Hz		25			•		nV/√Hz
	f_o = 1kHz		18			•		nV/√Hz
	f_o = 10kHz		18			•		nV/√Hz
	f_o = 100kHz		18			•		nV/√Hz
Voltage Noise	f_B = 0.1Hz to 10Hz		2.6			•		µV, p-p
Current Noise Density	f_o = 0.1Hz thru 8kHz		6			•		fA/√Hz
Current Noise	f_B = 0.1Hz to 10Hz		115			•		fA, p-p
DYNAMIC RESPONSE								
Gain Bandwidth Product			5			•		MHz
Full Power Bandwidth	G = 1, V_o = 20V, p-p, R_L = 5kΩ		220		80	•		kHz
Slew Rate	G = 1, V_o = ±10V, R_L = 5kΩ		14		5	•		V/µsec
Settling Time(5)	G = 1, V_o = ±10V, R_L = 5kΩ							
ε = 1%			2.5			•		µsec
ε = 0.1%			3			•		µsec
ε = 0.01%			5			•		µsec
Rise Time	10% to 90%, small signal		70			•		nsec
Phase Margin	G = 1, R_L = 5kΩ		60			•		Degrees
Overload Recovery (6)	G = 1, 50% overdrive		2			•		µsec
Crosstalk, RTI(5)(7)	20V, p-p, 1kHz sine, R_S = 1kΩ on all OFF channels		±0.003			•		%
DIGITAL INPUT(8)								
Input "Low" Threshold, V_{IL}				0.8			•	V
Input "High" Threshold, V_{IH}		2.0			•			V
f_{max}, Maximum Clock Frequency		30			•			MHz
t_{WL}, Clock Pulse Width (Low)	Figure 1	20			•			nsec
t_{s_1}, Setup Time (Data to CP)	Figure 1	20			•			nsec
t_{h_1}, Hold Time (Data to CP)	Figure 1	5			•			nsec
t_{s_2}, Setup Time ($\overline{CE}$ to CP)	Figure 1	25			•			nsec
t_{h_2}, Hold Time ($\overline{CE}$ to CP)	Figure 1	5			•			nsec

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	PGA100AG MIN	PGA100AG TYP	PGA100AG MAX	PGA100BG MIN	PGA100BG TYP	PGA100BG MAX	UNITS
ANALOG SUPPLY								
Rated Voltage			±15					VDC
Voltage Range	Derated performance	±8		±18	*		*	V
Positive Quiescent Current			+20	+27		+15	+20	mA
Negative Quiescent Current			-10	-16		-7.5	-12	mA
DIGITAL SUPPLY								
Rated Voltage			+5					VDC
Voltage Range		+4.75		+5.25	*		*	V
Quiescent Current	V_{DD} = +5.25V		15	27		*	*	mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Operating	Derated performance	-55		+125	*		*	°C
Storage		-55		+125	*		*	°C

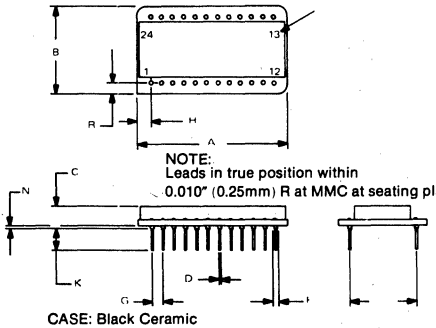
*Specifications same as PGA100AG.

NOTES:

1. Inaccuracy is the percent error between the actual and ideal gain selected. It may be externally adjusted to zero.
2. Parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.
3. Nonlinearity is the maximum peak deviation from a "best straight line" (curve fitting on input-output graph) expressed as a percent of the full scale peak-to-peak output. Gain constant, V_{OUT} ranges from -10V to +10V.
4. Doubles approximately every 10°C.
5. See Typical Performance Curves.
6. Time required for the output to return from saturation to linear operation following the removal of an input overdrive signal.
7. Crosstalk is the amount of signal feedthrough from all OFF channels that appears at the output of the input multiplexer. It is expressed as a percent of the signal applied to all OFF channels.
8. All digital inputs are one 74LSTTL load.

MECHANICAL

Pin numbers shown for reference only.
Numbers may not be marked on package.



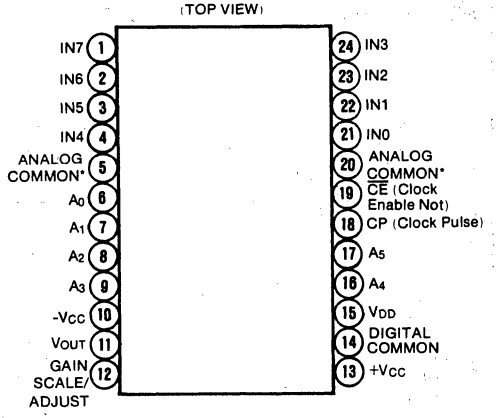
CASE: Black Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 6.3 grams (0.225 oz.)
HERMETICITY: Conform to method 1014 Condition C Step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	002	.010	0.05	0.25
R	085	105	2.16	2.67

ABSOLUTE MAXIMUM RATINGS

Analog Supply	±18V
Digital Supply	+7V
Input Voltage Range, Analog	±(|Vcc| +20)V
Input Voltage Range, Digital	+7V
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering 10 seconds)	300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	175°C

PIN DESIGNATIONS

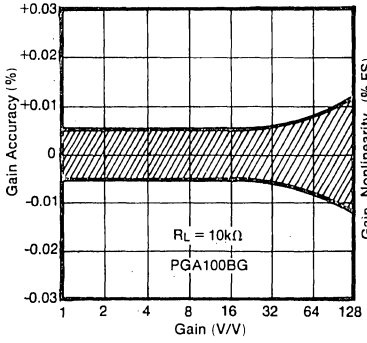


*Connected internally. Use pin 20 as the primary analog common.

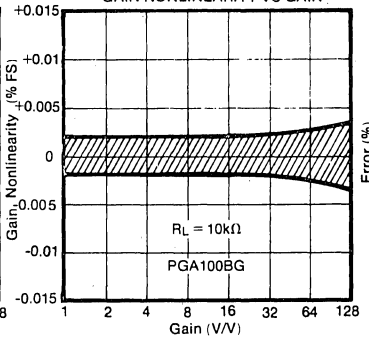
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = 15VDC, V_{DD} = +5VDC, unless otherwise noted.)

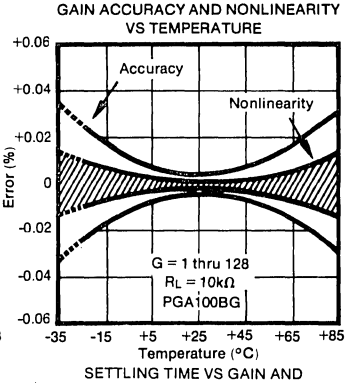
GAIN ACCURACY VS GAIN



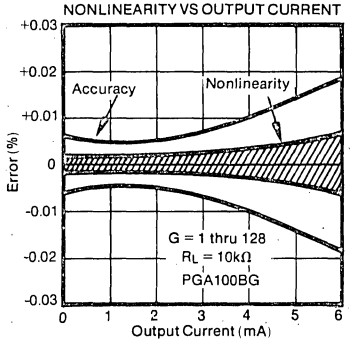
GAIN NONLINEARITY VS GAIN



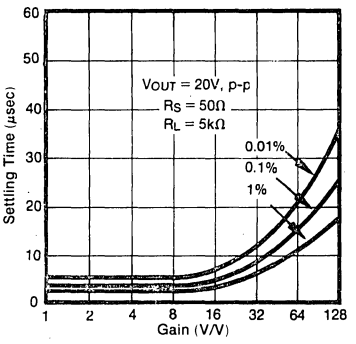
GAIN ACCURACY AND NONLINEARITY VS TEMPERATURE



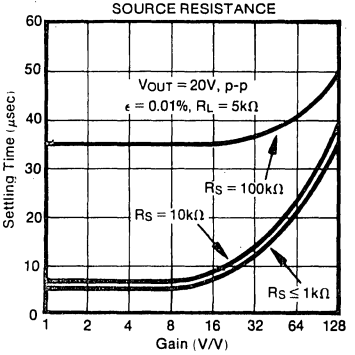
GAIN ACCURACY AND NONLINEARITY VS OUTPUT CURRENT



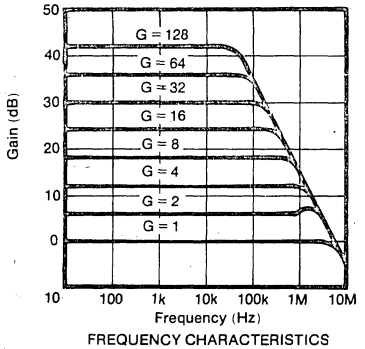
SETTLING TIME VS GAIN



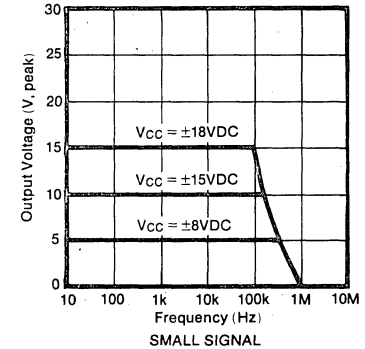
SETTLING TIME VS GAIN AND SOURCE RESISTANCE



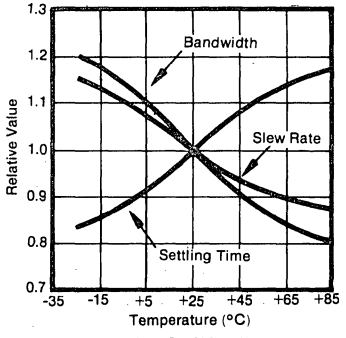
SMALL SIGNAL FREQUENCY RESPONSE



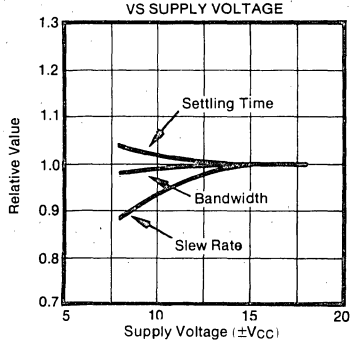
LARGE SIGNAL OUTPUT VOLTAGE VS FREQUENCY



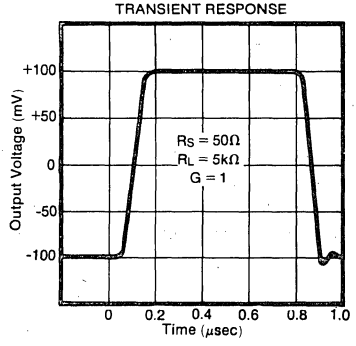
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



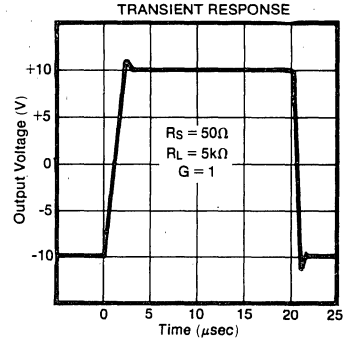
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



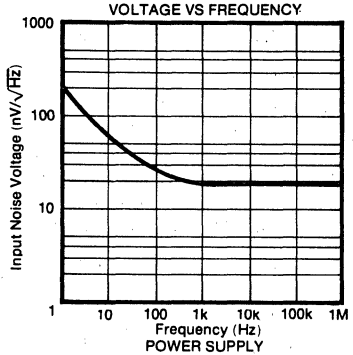
SMALL SIGNAL TRANSIENT RESPONSE



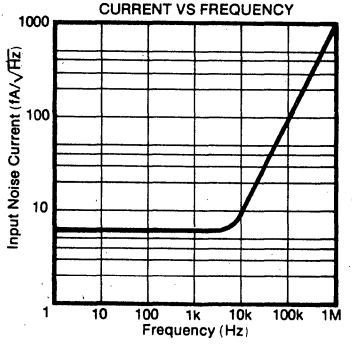
LARGE SIGNAL TRANSIENT RESPONSE



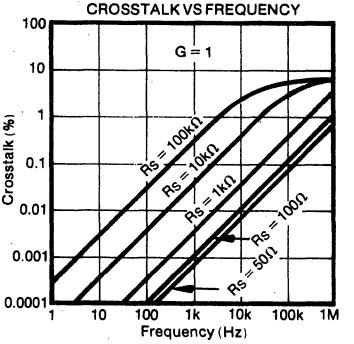
INPUT NOISE VOLTAGE VS FREQUENCY



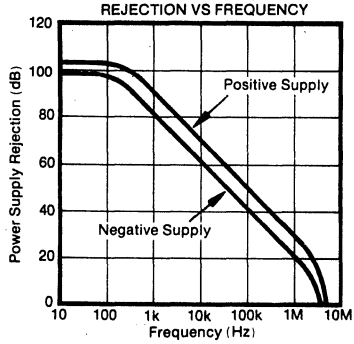
INPUT NOISE CURRENT VS FREQUENCY



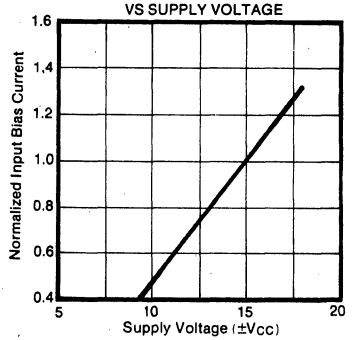
CHANNEL-TO-CHANNEL CROSSTALK VS FREQUENCY



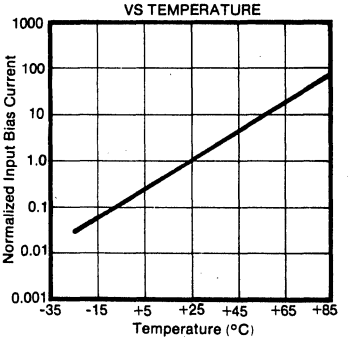
POWER SUPPLY REJECTION VS FREQUENCY



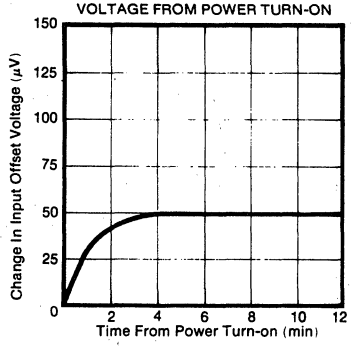
INPUT BIAS CURRENT VS SUPPLY VOLTAGE



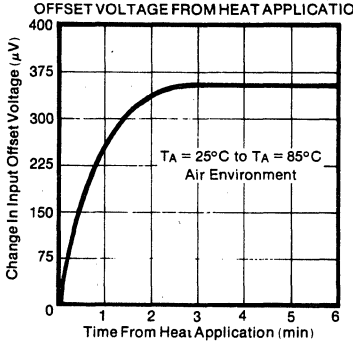
INPUT BIAS CURRENT VS TEMPERATURE



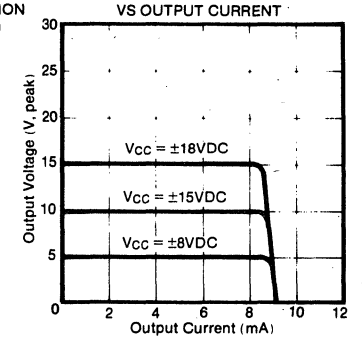
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



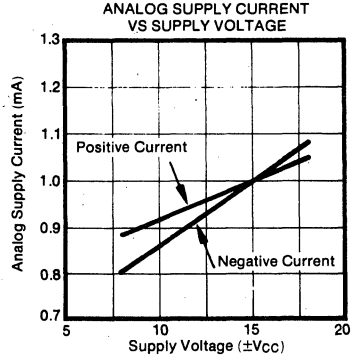
THERMAL RESPONSE TIME OF INPUT OFFSET VOLTAGE FROM HEAT APPLICATION



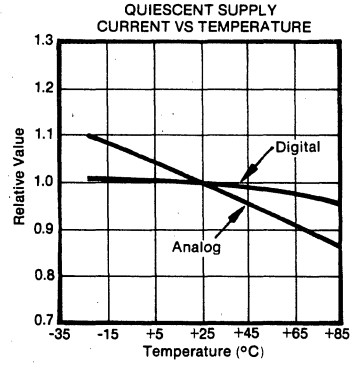
OUTPUT VOLTAGE VS OUTPUT CURRENT



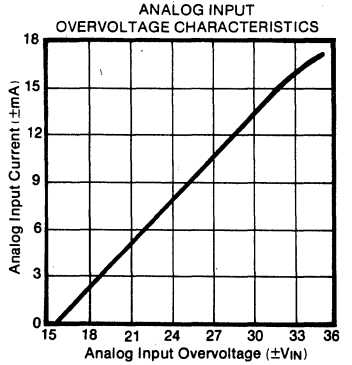
ANALOG SUPPLY CURRENT VS SUPPLY VOLTAGE



QUIESCENT SUPPLY CURRENT VS TEMPERATURE



ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



DISCUSSION OF PERFORMANCE

The PGA100 is a self-contained programmable-gain amplifier whose gain can be changed in 8 binarily weighted steps from 1 to 128 or as scaled externally through the gain scale/adjust pin. The gain control is accomplished by the gain switch (break-before-make) whose position is determined by the 3-bit TTL address, A_3, A_4, and A_5. When selected, 1 of 8 positions connects the thin-film resistor network to the feedback loop of the op amp. This establishes the desired gain. (See Installation and Operating Instructions for gain scaling.)

Similarly, the 8 analog input channels are switched by the input multiplexer (break-before-make) whose position is determined by the 3-bit TTL address, A_0, A_1, and A_2. Gain and channel selection appear in Table I. 64-channel/gain combinations are possible.

The digital inputs are latched by the positive transition of the clock pulse, pin 18, when the clock enable, pin 19, is low. The relative set up and holding times specified in the Electrical Specifications are shown in Figure 1. The internal latch is similar to the industry standard 74LS378. Figure 2 shows a timing diagram for selected addresses indicating: the enable function, changing channel and gain, changing channel/constant gain, and constant channel/changing gain.

TABLE I. Gain and Channel Select Truth Table.

GAIN SELECT			GAIN	CHANNEL SELECT			CHANNEL
A_5	A_4	A_3		A_2	A_1	A_0	
0	0	0	1	0	0	0	IN0
0	0	1	2	0	0	1	IN1
0	1	0	4	0	1	0	IN2
0	1	1	8	0	1	1	IN3
1	0	0	16	1	0	0	IN4
1	0	1	32	1	0	1	IN5
1	1	0	64	1	1	0	IN6
1	1	1	128	1	1	1	IN7

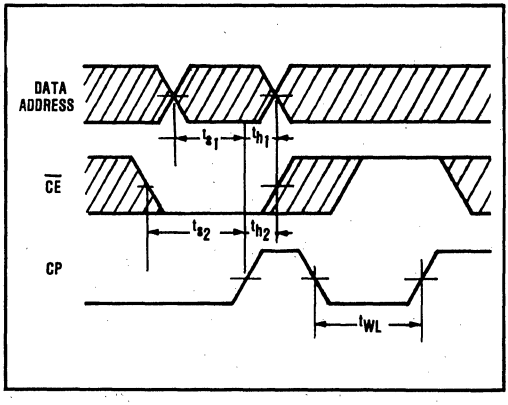


FIGURE 1. Data Address and Clock Enable Setup and Hold Times.

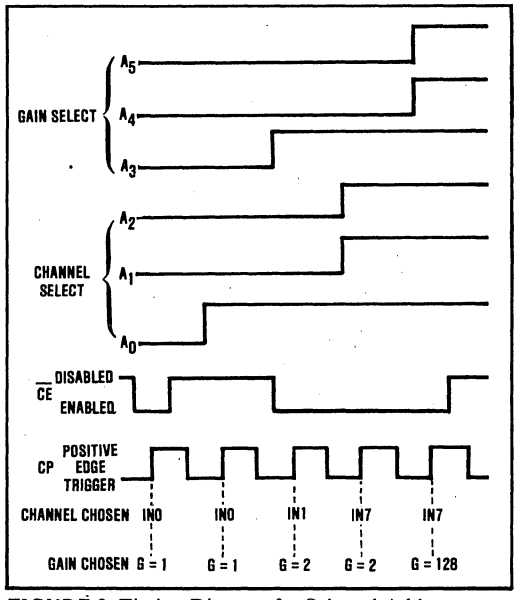


FIGURE 2. Timing Diagram for Selected Addresses.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

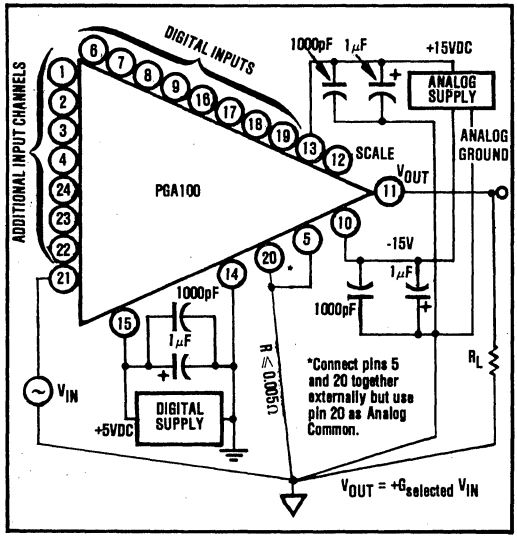


FIGURE 3. Basic Power Supply, Ground, and Signal Connections.

Figure 3 shows the proper analog and digital power supply connections. The supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible. To avoid gain errors connect grounds as indicated being sure to minimize ground resistance. Note that a resistance of greater than

0.005Ω in series with the analog common will degrade the specified gain accuracy. IMPORTANT: Normally the digital ground is brought in from the digital power supply on a separate line. However, the analog and digital commons must be connected together somewhere in the system.

OPTIONAL GAIN SCALE/ADJUST

The gain scale/adjust pin is shown in Figure 4. When no connection is made, gains appear as in Table I. At least two functions can be performed. First, the gain range can be scaled to gains other than 1 to 128, for example, 1 to 100 or 1 to 1024. Gain steps, however, retain binary weighting. Some examples are: (1, 1, 2, 4, 8, 16, 32, 64 with pins 11 and 12 connected together), (1, 1.5625, 3.125, 6.25, 12.5, 25, 50, 100), (1, 12.5, 25, 50, 100, 200, 400, 800), and (1, 16, 32, 64, 128, 256, 512, 1024). Scaling is accomplished by using a potentiometer, R_1, shown in Figure 4. Be certain to use a potentiometer of good mechanical and thermal stability. Additional gain drift with temperature should be minimal since it depends on the thermal tracking of the resistance ratio, R_A to R_B, set by the potentiometer.

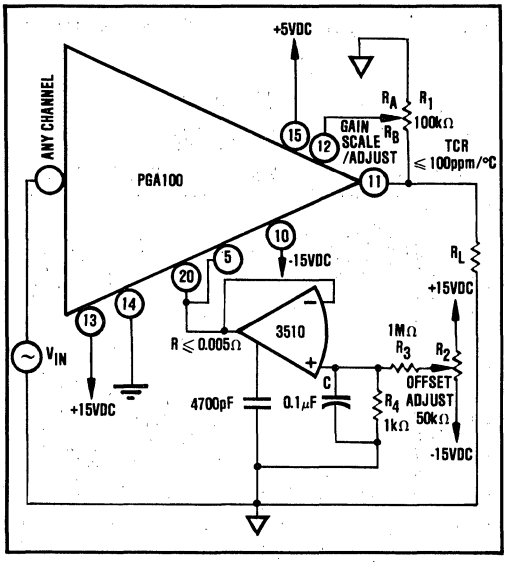


FIGURE 4. External Gain and Offset Adjustment.

Second, the gain inaccuracy, remaining after laser trimming at the factory, can be adjusted to zero at any gain other than unity. To improve resolution and limit adjustment range, a resistor may be added in series with the wiper of the potentiometer and pin 12. This will, however, increase gain drift. Figure 5 shows the effect of gain adjustment. R_1 does not affect gain linearity.

OPTIONAL OFFSET ADJUSTMENT

Figure 4 also illustrates a technique for offset adjustment. This adjustment has no effect at unity gain. R_2 will trim the offset to zero and have neglible effect on the gain accuracy. For best results, trim the offset at the highest

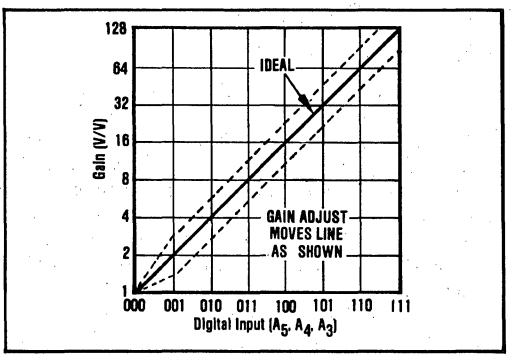


FIGURE 5. Effect of Gain Adjustment.

gain. If R_3 is made smaller, output offsetting can be accomplished. This can be used to introduce an intentional DC voltage at the output. The external amplifier used will add to the input noise, therefore, use one with a noise level of at least three times lower than that specified for the PGA100.

LAYOUT CONSIDERATIONS

Proper attention to layout is necessary to achieve the specified performance of the PGA100. Major goals are to reduce crosstalk, noise pickup, noise coupled from the power supply, and gain errors.

Be certain to separate analog and digital runs to avoid coupling of digital transients. To reduce gain errors, connect analog grounds with a ground plane or a low resistance star configuration as shown in Figure 3. Analog and digital commons must be connected at some point in the system to insure proper operation.

GAIN INACCURACY AND NONLINEARITY

As shown in Figure 3, connect pins 5 and 20 directly together at the unit and use pin 20 as the primary analog common. Ground resistance in series with pin 20 also appears in series with the internal gain-setting resistors and will decrease the magnitude of all gains except unity. The resulting accuracy error varies nonlinearly with the gain selected and therefore cannot be externally adjusted to zero for more than one gain at a time. Gain linearity is not affected by external ground resistance (see Performance Curves.)

CROSSTALK

Crosstalk is the amount of signal feedthrough from all OFF channels that appears at the output of the input multiplexer. It is expressed as a percent of the input signal applied to all OFF channels. For example, the 0.003% specification indicates that 0.6mV, p-p, out of a 20V, p-p, 1kHz sine wave (applied to 7 OFF channels) will appear at the noninverting input of the internal op amp. Note that crosstalk increases with high frequencies due to the capacitive coupling between ON and OFF channels. It also increases with greater source resistance. However, because both the input signal and crosstalk noise are amplified equally, the resulting output signal-to-noise

ratio is independent of gain. Unused input channels should be grounded in order to reduce crosstalk and extraneous noise pickup. (See Performance Curves.)

SETTLING TIME

Settling time is the time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value. It is a very important consideration since this will be the limiting parameter in determining the maximum channel scanning or throughput rate. The PGA100 specification includes the effects of both the multiplexer and amplifier. Note that settling time increases with increasing source resistance and gain. Minimum settling time is achieved by choosing a low source resistance, for example, $R_S \leq 10k\Omega$ and gains ≤ 16. (See Performance Curves.)

INPUT OVERVOLTAGE PROTECTION

The PGA100 provides input overvoltage protection of 20V in excess of either power supply voltage expressed as $\pm(|V_{CC}|+20)$. This is achieved in the dielectrically isolated analog multiplexer which will withstand overvoltage even when the power supplies are off. As a consequence the PGA100 is protected against high input levels and brief transient spikes of up to several hundred volts that can result from signals originating from outside the system. (See Performance Curves.)

TYPICAL APPLICATIONS

The PGA100 is ideal for a variety of applications, especially where low channel-to-channel crosstalk is required. In many applications the PGA100 will not require trimming of offset and gain errors. However, these can be minimized utilizing hardware or software error correction techniques. Figures 6 and 7 show applications of the PGA100 separately and in a data acquisition system.

Figure 7 shows a Data Acquisition System. In this system the PGA100 allows the user to deal with signals of wide dynamic range while maintaining high system resolution. For example: When used with a 12-bit A/D converter in a "floating point" system, the 2^7 gain range of the PGA100 plus the 2^{12} range of the converter produces a total system resolution of 2^{19} (524,000 to 1).

Also the user can modify and reprogram gain values for different analog input channels merely by changing the software computer program. Since different dedicated amplifiers are not required for various input channels, the PGA100 also saves space and overall system costs. Software correction virtually eliminates system offset and gain errors over both time and temperature.

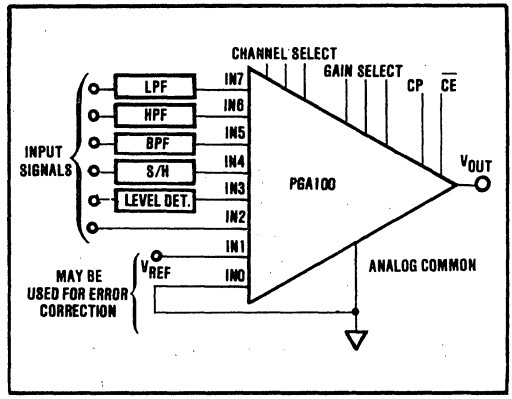


FIGURE 6. Digitally Selectable Function Amplifier.

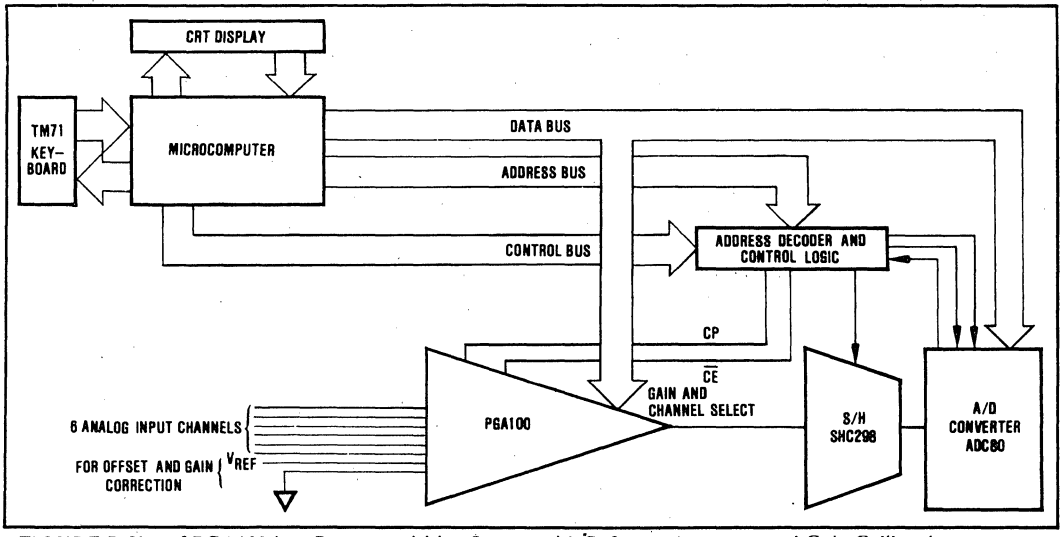


FIGURE 7. Use of PGA100 in a Data Acquisition System with Software Auto-zero and Gain Calibration.

BURR-BROWN®

PGA102

Digitally-Controlled Programmable-Gain/Fast-Settling OPERATIONAL AMPLIFIER

FEATURES

- DIGITALLY-PROGRAMMABLE GAINS, X1, X10, X100
- LOW GAIN ERROR, 0.01%, max
- LOW GAIN DRIFT, 5ppm/°C, max
- LOW NONLINEARITY, 0.003%, max, 14-BIT
- FAST SETTLING, 2.8μs, 0.01%, typ
- THREE INDEPENDENT INPUT CHANNELS WITH SEPARATE GAIN ADJUSTMENT
- LOW COST
- SMALL 16-PIN DIP PACKAGE, CERAMIC AND PLASTIC

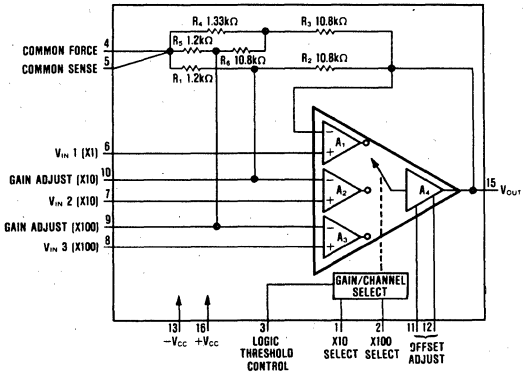
APPLICATIONS

- DATA ACQUISITION AMPLIFIER
- AUTORANGING AMPLIFIER UNDER COMPUTER CONTROL
- SUPER-ACCURACY, LOW COST, FIXED GAIN BLOCK
- TEST EQUIPMENT GAIN CONTROL
- PORTABLE INSTRUMENT GAIN SELECTION
- DATA LOGGING RANGING CONTROL
- 3-CHANNEL MULTIPLEXER

DESCRIPTION

The PGA102 is a precision digitally-programmable gain block. Its monolithic design permits low cost and high reliability. The user can select one of three gains (1, 10, 100), two of which are independently adjustable. The logic section has high input impedance and functions without a separate supply. Precision laser-trimmed offset and gains permit use without external adjustments. High performance thin-film resistors with excellent temperature tracking assure low gain drift and excellent stability.

The fast 2.8μsec settling makes the PGA102 ideal for rapid channel scanning in data acquisition systems. Also the high accuracy is very beneficial in test equipment and instrumentation applications where programmable or fixed gain is required.



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SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 15VDC unless otherwise specified.

PARAMETER	CONDITIONS	PGA102AG			PGA102BG/SG			PGA102KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Inaccuracy[1]	R_L = 2kΩ, G = 1		±0.007	±0.02		±0.003	±0.01		•	•	%
	G = 10		±0.015	±0.03		±0.01	±0.02		•	±0.05	%
	G = 100		±0.02	±0.05		±0.015	±0.025		•	±0.06	%
vs Temperature	G = 1		±0.4	±5		•	•		•	•	ppm/°C
	G = 10		±2	±7		•	•		•	•	ppm/°C
	G = 100		±7	±20		•	•		±9	•	ppm/°C
Nonlinearity	R_L = 2kΩ, G = 1		0.001	0.003		•	•		•	•	% of FS
	G = 10		0.002	0.005		•	•		•	•	% of FS
	G = 100		0.003	0.01		•	•		•	•	% of FS
RATED OUTPUT											
Voltage	R_L = 2kΩ	±10	±12.5		•	•		•	•		V
Current	V_{OUT} = 10V	±5	±10		•	•		•	•		mA
Short Circuit Current		±10	±25		•	•		•	•		mA
Output Resistance			0.01			•			•		Ω
Load Capacitance	For stable operation		2000			•			•		pF
INPUT OFFSET VOLTAGE											
Initial[2]	G = 1		±200	±500		±100	±250		•	±1500	µV
	G = 10		±70	±200		±50	±100		•	±600	µV
	G = 100		±70	±200		±50	±100		•	±600	µV
vs Temperature	G = 1		±5	±20		•	•		±7	±50	µV/°C
	G = 10		±1	±7		•	•		±3	±10	µV/°C
	G = 100		±0.5	±3		•	•		±2	±7	µV/°C
vs Supply Voltage	±5 < V_{CC} < ±18V										
	G = 1		±30	±70		•	•		•	•	µV/V
	G = 10		±8	±30		•	•		•	•	µV/V
	G = 100		±8	±30		•	•		•	•	µV/V
INPUT BIAS CURRENT											
Initial	T_A = +25°C		±20	±50		•	•		•	•	nA
Over Temperature	$T_{A\ MIN}$ to $T_{A\ MAX}$		±25	±60		•	•		•	•	nA
ANALOG INPUT CHARACTERISTICS											
Voltage Range	Linear operation	±10	±12		•	•		•	•		V
Resistance			7×10^8			•			•		Ω
Capacitance			4			•			•		pF
INPUT NOISE											
Voltage Noise	f_B = 0.1Hz to 10Hz										
	G = 1		4.5			•			•		µV p-p
	G = 10		1.5			•			•		µV p-p
	G = 100		0.6			•			•		µV p-p
Voltage Noise Density	f_O = 1Hz, G = 1		490			•			•		nV/√Hz
	G = 10		178			•			•		nV/√Hz
	G = 100		83			•			•		nV/√Hz
	f_O = 10Hz, G = 1		155			•			•		nV/√Hz
	G = 10		56			•			•		nV/√Hz
	G = 100		20			•			•		nV/√Hz
	f_O = 100Hz, G = 1		93			•			•		nV/√Hz
	G = 100		31			•			•		nV/√Hz
	G = 100		18			•			•		nV/√Hz
	f_O = 1kHz, G = 1		79			•			•		nV/√Hz
	G = 10		31			•			•		nV/√Hz
	G = 100		18			•			•		nV/√Hz
Current Noise	f_B = 0.1Hz to 10Hz		76			•			•		pA p-p
Current Noise Density	f_O = 1Hz		8.8			•			•		pA/√Hz
	f_O = 10Hz		2.8			•			•		pA/√Hz
	f_O = 100Hz		0.99			•			•		pA/√Hz
	f_O = 1kHz		0.43			•			•		pA/√Hz

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	PGA102AG			PGA102BG/SG			PGA102KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE											
±3dB Bandwidth	Small signal, G = 1		1500			•			•		kHz
	G = 10		750			•			•		kHz
	G = 100		250			•			•		kHz
Full Power Bandwidth	V_{OUT} = ±10V, R_L = 2kΩ		160			•			•		kHz
Slew Rate	V_{OUT} = ±10V step,										
	R_L = 2kΩ	6	9		•	•		•	•		V/µs
Settling Time (0.1%)	V_{OUT} = 10V step, G = 1		1.6			•			•		µs
	G = 10		2.2			•			•		µs
	G = 100		5.2			•			•		µs
Settling Time (0.01%)	V_{OUT} = 10V step, G = 1		2.8			•			•		µs
	G = 10		2.8			•			•		µs
	G = 100		8.2			•			•		µs
Overload Recovery Time, 0.1%	50% overdrive, G = 1 (see Performance Curve)		2.5			•			•		µs
CROSSTALK											
DC	±10V to both Off channels		−155			•			•		dB
60Hz	±10V to both Off channels		−144			•			•		dB
DIGITAL INPUT CHARACTERISTICS											
Input "Low" Threshold	V_{IL}[3] on pin 1 or 2			VLTC+0.8			•			•	V
Input "Low" Current				1			•			•	µA
Input "High" Threshold	V_{IH}[3] on pin 1 or 2	VLTC+2		1	•		•	•		•	V
Input "High" Current			0.1	1		•	•		•	•	µA
Logic Threshold Control	VLTC on pin 3	$-V_{CC}$		V_{CC} − 4	•		•	•		•	V
Switching Time[4]	Between channels		1			•			•		µs
POWER SUPPLY											
Rated Voltage			±15				•			•	VDC
Voltage Range		±5		±18	•		•	•		•	VDC
Quiescent Current	V_{OUT} = 0V		±2.4	±3.3		•	•		•	•	mA
	No external load, V_{OUT} = ±10V			±5.3			•			•	mA
TEMPERATURE RANGE											
Specification, KP grade	$T_{A\ MIN}$ to $T_{A\ MAX}$							0		+70	°C
AG and BG grades		−25		+85	•		•				°C
SG grade					−55		+125				°C
Operating		−55		+125	•		•	−25		+85	°C
Storage		−65		+150	•		•	−55		+125	°C
Thermal Resistance	θ_{JA}		100			•			•		°C/W

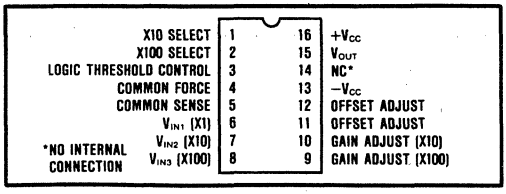
* Specification same as AG grade.

NOTES: (1) Gain inaccuracy is the percent error between the actual and ideal gain selected. It may be externally adjusted to zero for gains of 10 and 100. (2) Offset voltage can be adjusted for any one channel. Adjustment affects temperature drift by approximately ±0.3µV/°C for each 100µV of offset adjusted. (3) Voltage on the logic threshold control pin, VLTC, adjusts the threshold for "Low" and "High" logic levels. (4) Total time to settle equals switching time plus settling time of the newly selected gain.

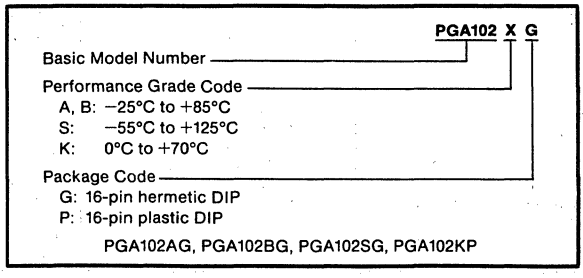
ABSOLUTE MAXIMUM RATINGS

Power Supply ..... ±18V
Input Voltage Range: Analog ..... ±V_{CC}
Digital ..... ($V_{PIN\ 3}$ − 5.6V) to +V_{CC}
Storage Temperature Range: G Package ..... −65°C to +150°C
P Package ..... −55°C to +125°C
Lead Temperature (soldering 10 seconds) ..... +300°C
Output Short-Circuit Duration ..... Continuous to Common
Junction Temperature: G Package ..... +175°C
P Package ..... +110°C

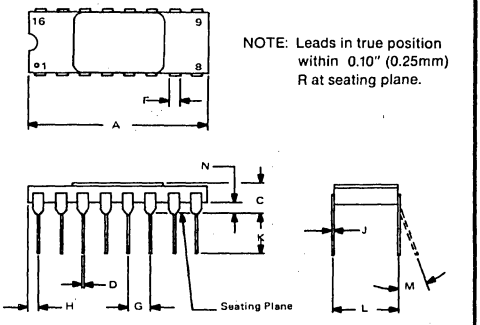
PIN CONFIGURATION



ORDERING INFORMATION

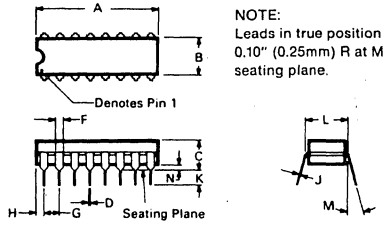


MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

EPOXY DUAL-IN-LINE



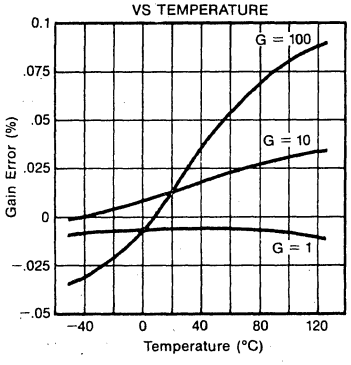
NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.760	.885	19.30	22.48
B	.220	.280	5.59	7.11
C	--	.200	--	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100	--	2.54	--
L	.300 BASIC		7.62 BASIC	
M	--	15°	--	15°
N	.020	.050	0.51	1.27

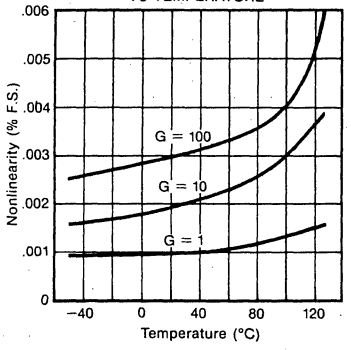
TYPICAL PERFORMANCE CURVES

$T_A = 25°C$, $\pm V_{CC} = 15VDC$ unless otherwise noted.

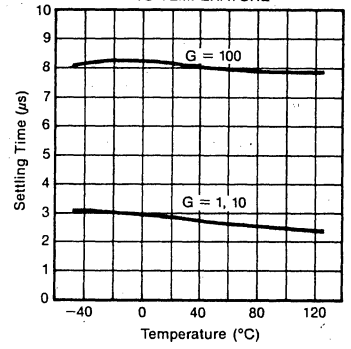
GAIN ERROR VS TEMPERATURE



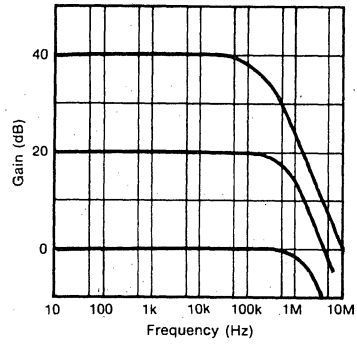
NONLINEARITY VS TEMPERATURE



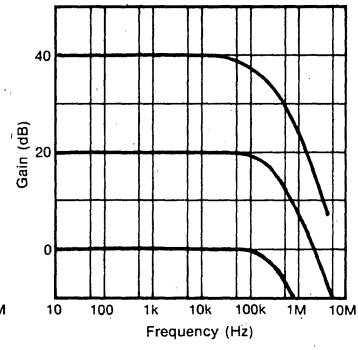
SETTLING TIME VS TEMPERATURE



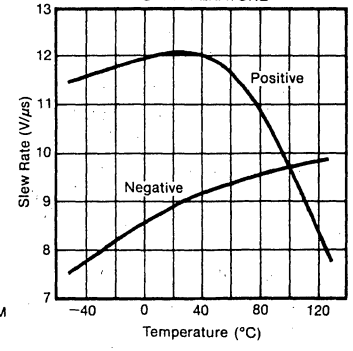
SMALL SIGNAL FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



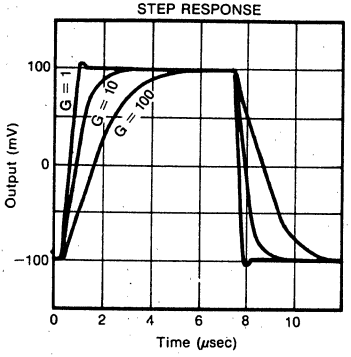
SLEW RATE VS TEMPERATURE



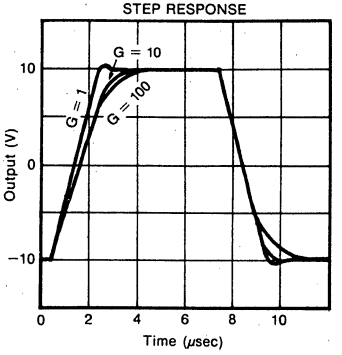
TYPICAL PERFORMANCE CURVES (CONT)

T_A = 25°C, ±V_{CC} = 15VDC unless otherwise noted.

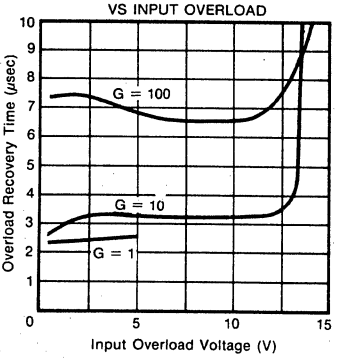
SMALL SIGNAL STEP RESPONSE



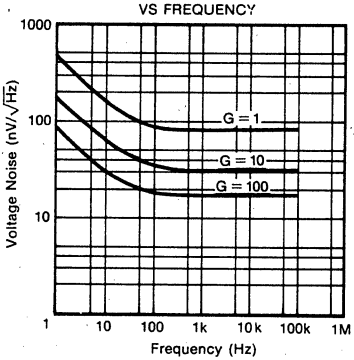
LARGE SIGNAL STEP RESPONSE



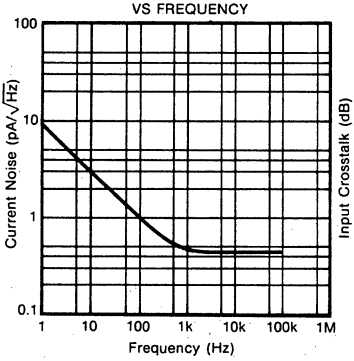
OVERLOAD RECOVERY VS INPUT OVERLOAD



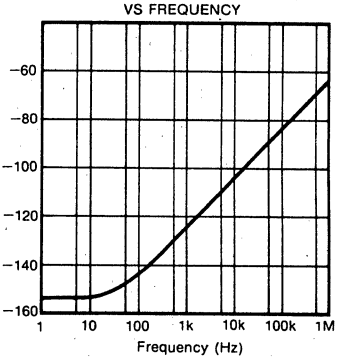
INPUT VOLTAGE NOISE VS FREQUENCY



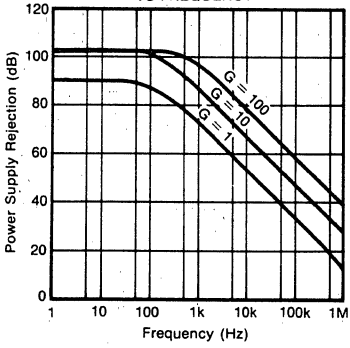
INPUT CURRENT NOISE VS FREQUENCY



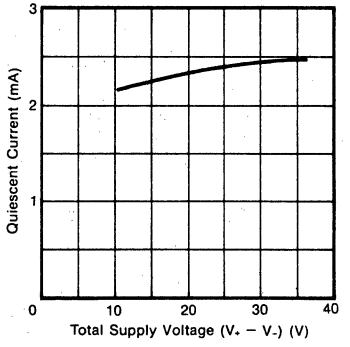
INPUT CROSSTALK VS FREQUENCY



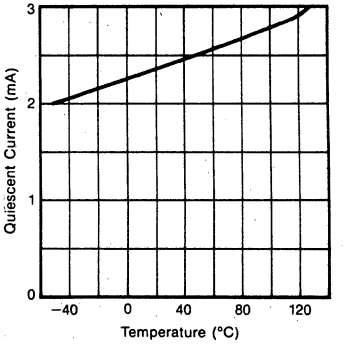
POWER SUPPLY REJECTION VS FREQUENCY



QUIESCENT CURRENT VS SUPPLY VOLTAGE



QUIESCENT CURRENT VS TEMPERATURE



THEORY OF OPERATION

The PGA102 is a self-contained programmable-gain amplifier with digitally selectable gains of 1, 10, and 100.

A block diagram of the PGA102 is shown on the first page of this data sheet. The circuit contains three sections: (1) 3-channel switchable-input operational amplifier, (2) precision thin-film resistor network (R_1–R_6), and (3) gain/channel select digital circuit.

Under control of the channel select circuitry, only one input stage (A_1, A_2, or A_3) is active at any time. The selected input stage steers input signals (V_{IN1}, V_{IN2}, or V_{IN3}) to the output amplifier (A_4). At this time the unselected input stages are turned off by deactivation of their internal bias circuitry. Three different precision gains are produced by closing the feedback loop through the selected input stage. This unique feature of having each channel set to a specific gain allows the user more flexibility in applications. Low gain drift is achieved by the excellent tracking of the thin-film gain set resistors. The "trip point" on select pins 1 and 2 for changing channels, and hence gain, is set by the logic threshold control voltage on pin 3.

INSTALLATION AND OPERATING INSTRUCTIONS

Figure 1 shows proper power supply and signal connections. The supplies should be decoupled with 0.1μF capacitors as close to the package as possible. To avoid gain errors, connect ground as indicated, being sure to minimize ground resistance. The PGA102 has a separate ground force and ground sense which virtually eliminate gain errors due to resistance in the common line. The gain error results from any resistance added in series with the internal junction of R_1, R_4, and R_5. Internally, wire bond resistance of 0.2Ω can cause a 0.02% error for gain of 10 and 0.2% error for gain of 100. By minimizing the current in the sense line, specified performance is achievable.

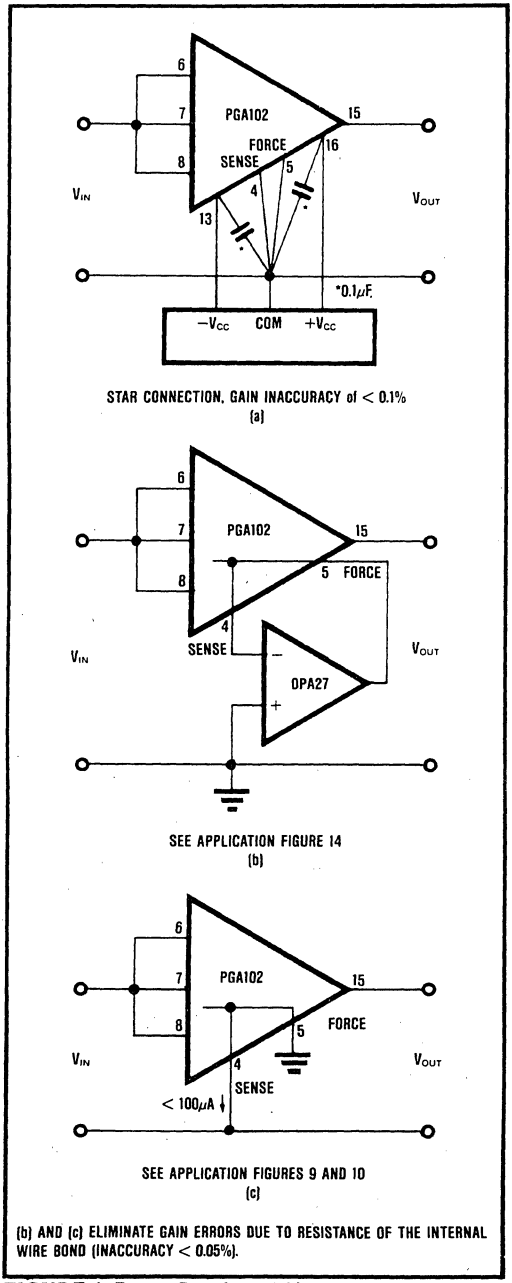
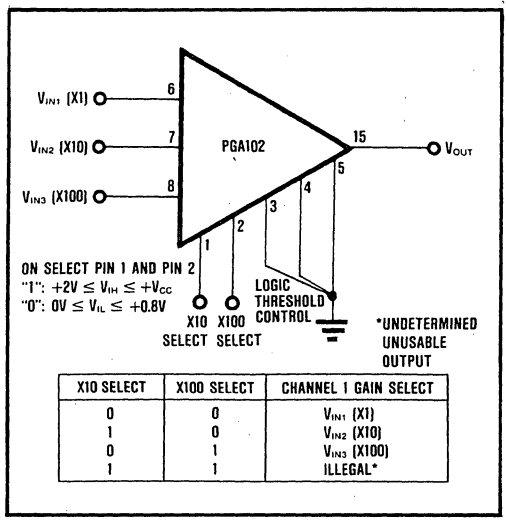


FIGURE 1. Power Supply and Signal Connections.

GAIN/CHANNEL SELECTION

Gain is chosen by digitally manipulating the voltage level on the X10 and X100 select pins as shown in Figure 2. The table in Figure 2 shows how to select a specific channel which has a gain of 1, 10, or 100. In this circuit, the logic threshold control has been grounded to give compatibility with TTL levels. However, this threshold can be set anywhere between $[-V_{CC} + 4V]$ and $[+V_{CC} - 2.6V]$ for compatibility with other logic such as CMOS.



X10 SELECT	X100 SELECT	CHANNEL 1 GAIN SELECT
0	0	V_{IN1} (X1)
1	0	V_{IN2} (X10)
0	1	V_{IN3} (X100)
1	1	ILLEGAL*

FIGURE 2. Channel Selection for Ground-Referenced Logic Threshold (TTL-compatible).

In general, the logic state is determined by the voltage on pin 1 or pin 2 relative to the threshold control voltage on pin 3. The input high (V_{IH}) and low (V_{IL}) voltages to switch states are shown below:

Logic one, "1": $(V_{LTC} + 2V) < V_{IH} < +V_{CC}$

Logic zero, "0": $(V_{LTC} - 5.6) < V_{IL} < (V_{LTC} + 0.8V)$

An external decoder and latch on the select lines may be added for operation in computer-controlled analog input/output systems.

OPTIONAL OFFSET ADJUSTMENT

The input offset voltage is laser trimmed and will not require user adjustment for most applications. However, pins 11 and 12 may be used to adjust the offset of the

active channel to zero as shown in Figure 3. This also affects the inactive channels (all offsets move as the potentiometer is adjusted). By compromising, the user can adjust for the average offset of all three channels using one potentiometer; or a compromise for just the X10 and X100 channels can be made, considering the unity gain channel's offset is insignificant for high-level inputs.

Figure 4 shows another approach to offset adjustment. An inexpensive CMOS switch (4016) may be used to independently connect the wipers of three potentiometers to $-V_{CC}$. Therefore, R_1, R_2, and R_3 adjust the offset of channels 1, 2, and 3 respectively.

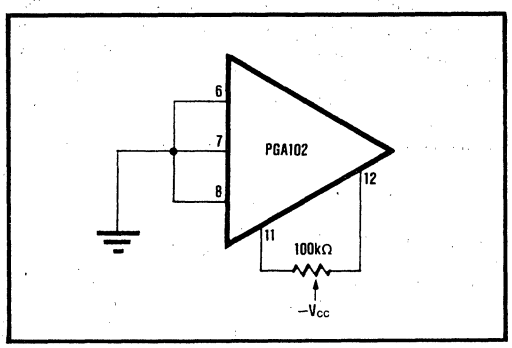


FIGURE 3. Offset Adjustment.

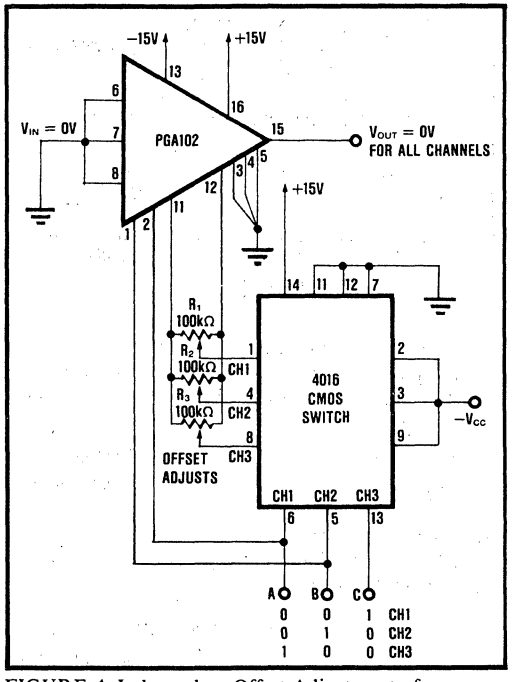


FIGURE 4. Independent Offset Adjustment of Channels 1, 2, and 3.

OPTIONAL GAIN ADJUSTMENT

The initial gain accuracy has been internally laser trimmed to high precision, but can be adjusted. Figure 5 shows independent fine-gain adjustment of channels 2 and 3. This involves either paralleling the internal input resistors for gain up or the internal feedback resistors for gain down. External resistors R_2, R_3, R_5, and R_6 are chosen to trade off range and resolution. Channel 1's gain cannot be adjusted due to the internal zero feedback resistance.

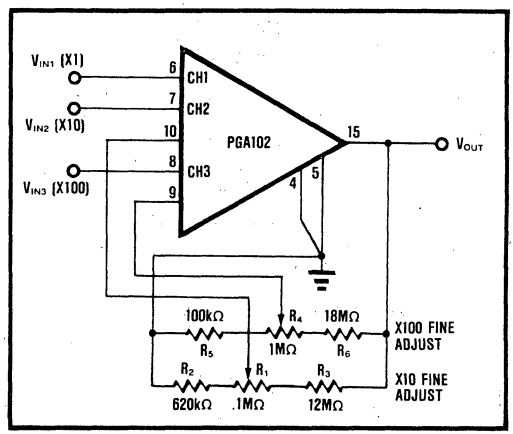


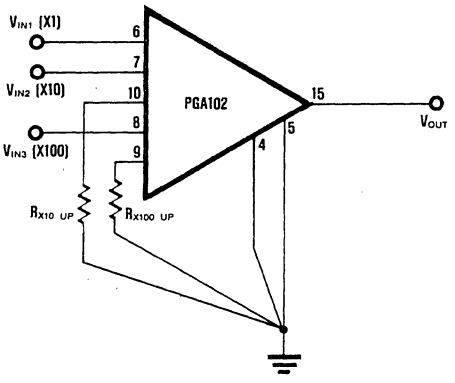
FIGURE 5. Independent Fine Gain Adjustment of Channels 2 and 3.

For applications requiring gains other than 1, 10, or 100, the PGA102 can be gained up (Figure 6) or down (Figure 7). It is important to realize that the temperature drift of the external gain adjustment resistors will affect the total gain drift. This becomes more predominant as the gain is changed further from the factory-set specification. For example, with small adjustments (20% or so), a 30ppm/°C external resistor will add 6ppm/°C to the 10ppm/°C internal resistor ratio tracking. For large adjustment (50% or so), the effect becomes larger. The best that can be achieved is 25ppm/°C (the TCR of one internal resistor) when the external resistor has 0ppm/°C. Also when adjusting the X10 channel, keep the gain above 5 to assure frequency stability.

LAYOUT CONSIDERATIONS

Proper attention to layout is necessary to achieve the specified performance of the PG102. Major goals are to reduce crosstalk, noise pickup, noise coupled from the power supply, and gain errors.

Be certain to separate the runs for analog and digital grounds to avoid coupling of digital transients. To reduce gain errors, connect analog grounds with a ground plane or a low resistance star configuration. Properly using the PGA102 ground force and sense (see Figure 1) assures the best performance, especially in high gains.



$$R_{X10\ UP} \approx \frac{10.8k\Omega}{G_{X10\ UP} - 10}$$

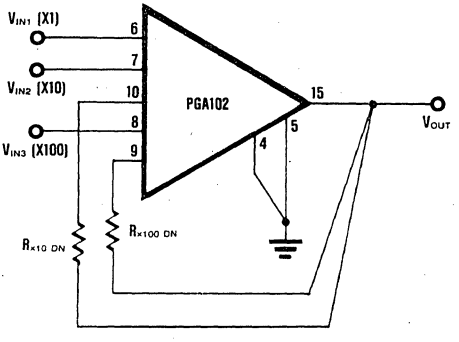
$$R_{X100\ UP} \approx \frac{108k\Omega}{G_{X100\ UP} - 100}$$

Example:

$R_{X10\ UP} \approx 1.08k\Omega$ and $R_{X100\ UP} \approx 1.08k\Omega$

Gives gains of 1, 20, 200

FIGURE 6. Gain Up Control.



$$R_{X10\ DN} \approx -\left(\frac{97.2k\Omega}{G_{X10\ DN} - 10} + 10.8k\Omega\right)$$

$$R_{X100\ DN} \approx 100\left(\frac{108k\Omega}{100 - G_{X100\ DN}} - 1.09k\Omega\right)$$

Example:

$R_{X10\ DN} \approx 8.64k\Omega$ and $R_{X100\ DN} \approx 107k\Omega$

Gives gains of 1, 5, 50

FIGURE 7. Gain Down Control.

CROSSTALK

Crosstalk expresses the signal feedthrough from an OFF channel that appears at the active input. It is expressed in dB, which translates to a percent of the input signal applied to the OFF channel. Crosstalk increases with increasing frequency (see Typical Performance Curve). Best performance is achieved by keeping input lines short and band limiting if possible.

SETTLING TIME

The PGA102 is designed for applications requiring fast settling. Settling time is the time required, after the onset of a step input signal, for the output voltage to settle and remain within a specified error band around the final value. It is very important because it limits maximum channel scanning or throughput rate in multiplexed systems. Since the error increases with source resistance, keep sources < 10kΩ for best results.

INPUT OVERLOAD RECOVERY

Another important parameter in data acquisition systems is overload recovery, especially when high gain is selected. The PGA102's fast recovery limits delays in capturing input signals in the presence of large transients. Best results are obtained by clamping input overvoltages to less than 13V (see Typical Performance Curve).

TYPICAL APPLICATIONS

The PGA102 is ideal for auto-gain-ranging systems with many multiplexed input channels that must be scanned quickly. Its high gain accuracy and low temperature drift permit application where computer error correction is not available. In other cases, the PGA102 provides an inexpensive precision fixed gain block requiring no precision external components. An external decoder and latch allow the user flexibility to configure the system as desired. Figures 8 through 15 show application circuits.

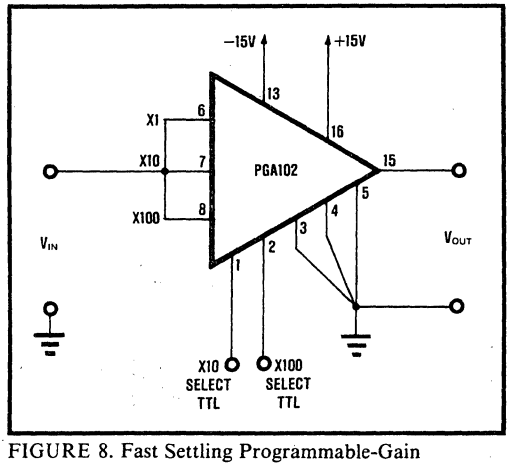


FIGURE 8. Fast Settling Programmable-Gain Amplifier (Gain = 1, 10, 100).

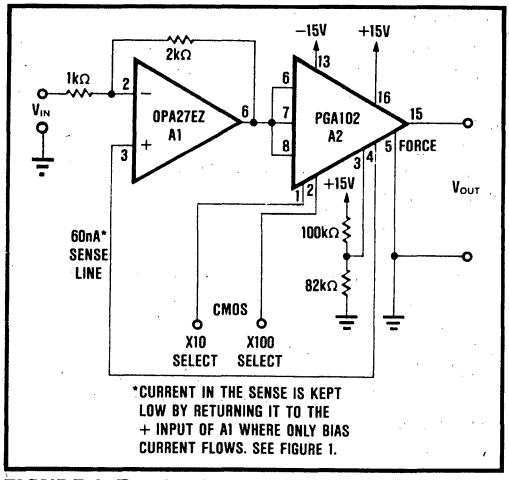


FIGURE 9. Fast-Settling Programmable-Gain Amplifier (Gain = 2, 20, 200).

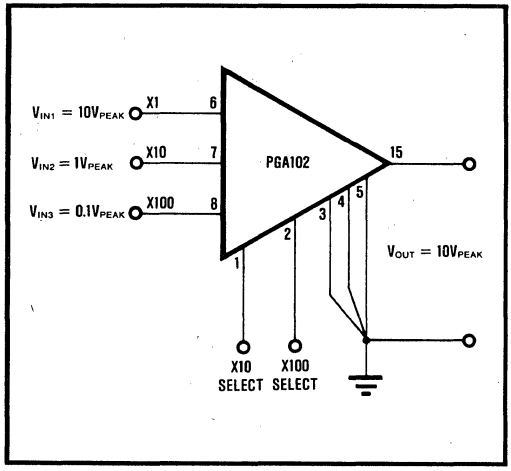


FIGURE 10. Three-Channel Separate Gain Amplifier.

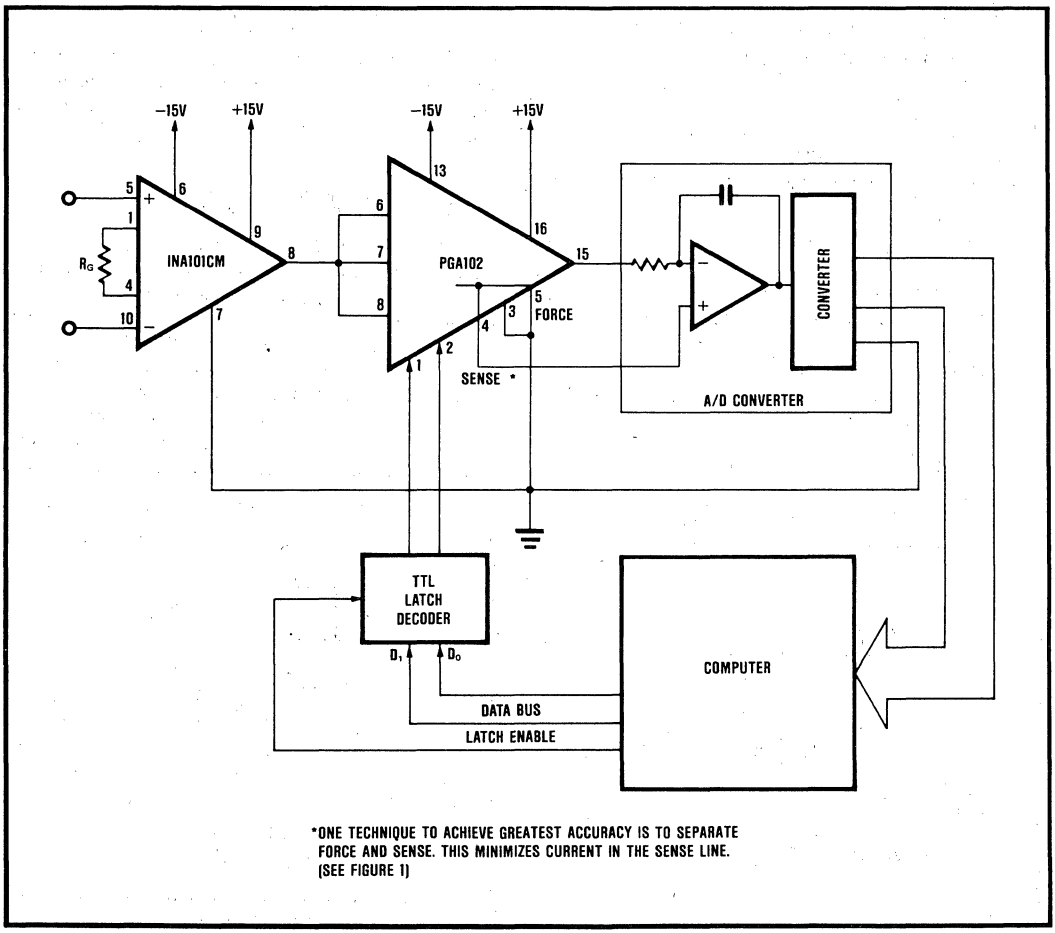


FIGURE 11. Auto-Gain Ranging Instrumentation Amplifier for Data Acquisition.

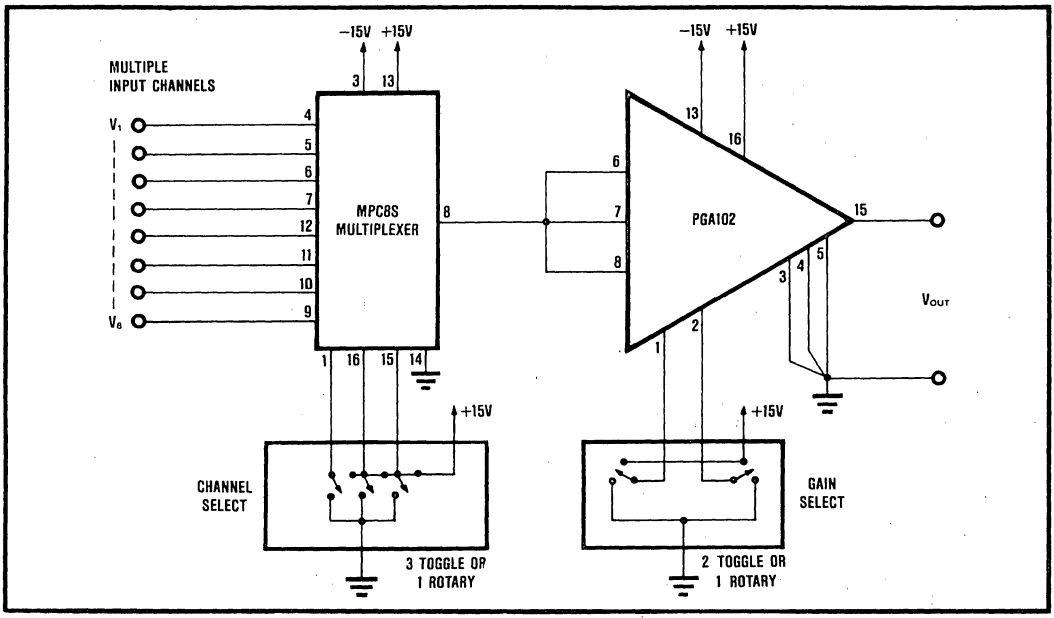


FIGURE 12. Manually Controlled Gain-Ranging Amplifier for Portable Test Equipment.

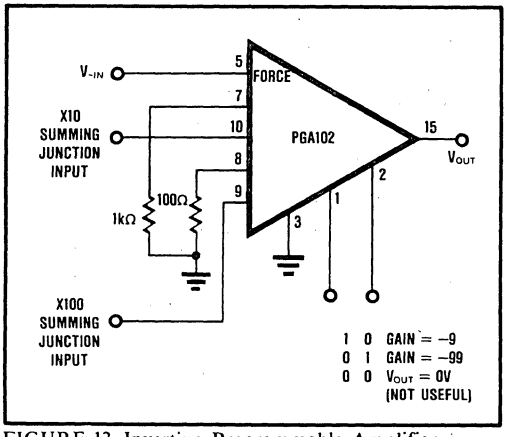


FIGURE 13. Inverting Programmable Amplifier. Summing Junctions Can Be Used for Offsetting.

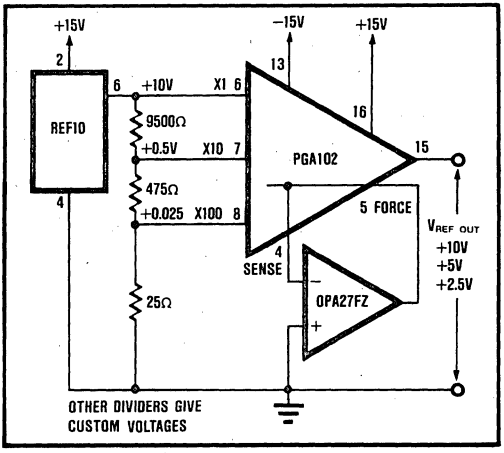


FIGURE 14. Precision Programmable Voltage Reference.

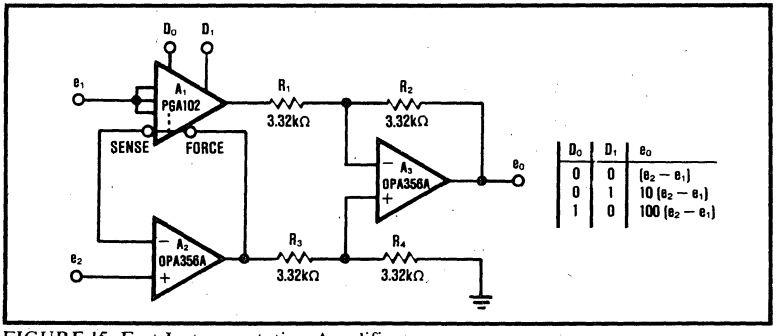


FIGURE 15. Fast Instrumentation Amplifier.

BURR-BROWN®

PGA200/201

Digitally-Controlled Programmable-Gain INSTRUMENTATION AMPLIFIER

FEATURES

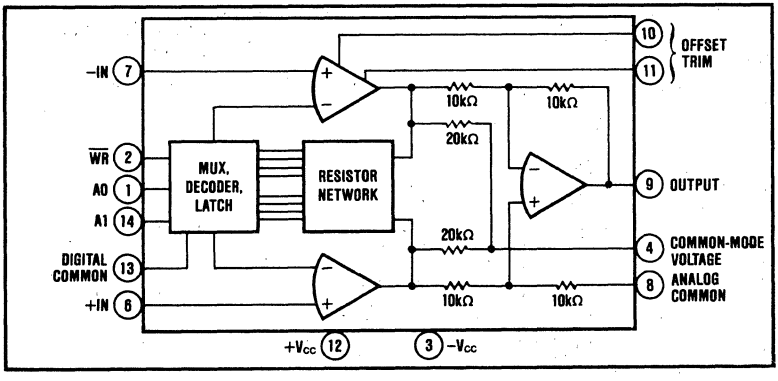
- DIGITALLY-PROGRAMMABLE GAIN
  - — Decade Model - PGA200
    Gains of 1, 10, 100, 1000
  - — Binary Model - PGA201
    Gains of 1, 8, 64, 512
- EXCELLENT GAIN ACCURACY (0.02%, max)
- LOW GAIN NONLINEARITY (0.012%, max; G = 1000)
- LOW GAIN DRIFT (10ppm/°C, max; G = 1000)
- 2-BIT LATCHED TTL-COMPATIBLE GAIN CONTROL
- LOW OFFSET VOLTAGE (25μV RTI, max; G = 1000)
- LOW OFFSET VOLTAGE DRIFT (0.30μV/°C, max; G = 1000)

APPLICATIONS

- DATA ACQUISITION SYSTEM AMPLIFIER
- DIGITALLY-CONTROLLED AUTORANGING SYSTEM
- SYSTEM DYNAMIC RANGE EXPANSION
- REMOTE INSTRUMENTATION SYSTEM
- TEST EQUIPMENT

DESCRIPTION

The PGA200 is a hybrid IC instrumentation amplifier with digitally-controlled decade gain steps of 1, 10, 100, and 1000. The PGA201 differs only by providing binary steps of 1, 8, 64, and 512. Both have TTL-compatible latched inputs for microprocessor interface. The logic section has high input impedance and functions without a separate logic power supply. Precision laser-trimmed offset and gain permits use without external adjustments. High performance thin-film resistors with excellent tracking assure low gain drift and excellent stability.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply unless otherwise noted.

MODEL[1]		PGA200/201AG			PGA200/201BG			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
GAIN								
Inaccuracy[2] G = 1			0.02	0.05		0.01	0.02	%
G = 10			0.02	0.05		0.01	0.02	%
G = 100			0.02	0.05		0.01	0.02	%
G = 1000			0.02	0.05		0.01	0.02	%
Nonlinearity, G = 1			0.002	0.005		0.001	0.002	%
G = 10			0.002	0.005		0.001	0.002	%
G = 100			0.003	0.007		0.002	0.003	%
G = 1000			0.012	0.025		0.011	0.012	%
Drift vs Temperature, G = 1			10	20		5	10	ppm/°C
G = 10			10	20		5	10	ppm/°C
G = 100			10	20		5	10	ppm/°C
G = 1000			10	20		5	10	ppm/°C
Stability vs Time			0.01			*		%/1khr
RATED OUTPUT								
Voltage	I_O = 5mA	10	12.5		*	*		V
Current	V_O = 10V	5	10.0		*	*		mA
Impedance			0.3			*		Ω
Capacitive Load			1000			*		pF
ANALOG INPUT CHARACTERISTICS								
Common-Mode Range		10			*			V
Absolute Maximum Voltage	No Damage			V_{CC}			*	V
Impedance, Differential			10^{10} || 3			*		Ω || pF
Common-Mode			10^{10} || 3			*		Ω || pF
OFFSET VOLTAGE (RTI)								
Initial Offset, max[3], G = 1			225	450		110	225	µV
G = 10			45	90		20	45	µV
G = 100			27	54		11	27	µV
G = 1000			25	50		10	25	µV
vs Temperature, G = 1			10	22		5	10	µV/°C
G = 10			2	4		0.75	1.5	µV/°C
G = 100			1	2		0.20	0.40	µV/°C
G = 1000			1	2		0.15	0.30	µV/°C
vs Time			1 + (20/G)			*		µV/mo
vs Supply	10 < V_{CC} < 18V		1 + (20/G)			*		µV/V
INPUT BIAS CURRENT								
Initial at 25°C	Each input		10	30		5	20	nA
vs Temperature			0.2			*		nA/°C
vs Supply			0.1			*		nA/V
Offset Current			10	30		5	20	nA
vs Temperature			0.5			*		nA/°C
COMMON-MODE REJECTION								
G = 1	DC to 60Hz,	80	95		*	*		dB
G = 10	1kΩ Source	96	110		*	*		dB
G = 100	Imbalance	106	120		*	*		dB
G = 1000		106	120		*	*		dB
INPUT NOISE[4]								
Input Voltage Noise, f_B = 0.1Hz to 10Hz			0.8			*		µV, p-p
Density, f_o = 10Hz			18			*		nV/√Hz
f_o = 100Hz			15			*		nV/√Hz
f_o = 1kHz			13			*		nV/√Hz
Input Current Noise, f_B = 0.1Hz to 10Hz			50			*		pA, p-p
Density, f_o = 10Hz			0.8			*		pA/√Hz
f_o = 100Hz			0.46			*		pA/√Hz
f_o = 1kHz			0.35			*		pA/√Hz
DYNAMIC RESPONSE								
±3dB Flatness	Small signal							
G = 1			500			*		kHz
G = 10			150			*		kHz
G = 100			30			*		kHz
G = 1000			2.4			*		kHz
±1% Flatness	Small signal							
G = 1			50			*		kHz
G = 10			25			*		kHz
G = 100			3			*		kHz
G = 1000			300			*		Hz

ELECTRICAL (CONT)

MODEL[1]		PGA200/201AG			PGA200/201BG			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DYNAMIC RESPONSE								
±1% Flatness	Small signal							
G = 1			50			*		kHz
G = 10			25			*		kHz
G = 100			53			*		kHz
G = 1000			300			*		Hz
Full Power	G = 1 to 100		6.4			*		kHz
Slew Rate	G = 1 to 100	0.2	0.4			*		V/μsec
Settling Time (0.1%), G = 1			35			*		μsec
G = 10			35			*		μsec
G = 100			50			*		μsec
G = 1000			480			*		μsec
Settling Time (0.01%), G = 1			40			*		μsec
G = 10			40			*		μsec
G = 100			80			*		μsec
G = 1000[5]			670			*		μsec
Overload Recovery Time	50% overdrive							
G = 1 to 100			12			*		μsec
G = 1000			22			*		μsec
DIGITAL INPUT CHARACTERISTICS								
Input Low Threshold				0.8			*	V
Input Low Current				30			*	μA
Input High Threshold		2.4			*			V
Input High Current				30			*	μA
T_{WW}, Write Pulse Width		300			*			nsec
T_S, Data Setup Time		180			*			nsec
T_H, Data Hold Time		30			*			nsec
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range		10		18	*		*	V
Quiescent Current			±10	±12		*	*	mA
TEMPERATURE RANGE								
Specification		−40		+85	*		*	°C
Operating		−55		+125	*		*	°C
Storage		−55		+150	*		*	°C

*Specifications same as for PGA200/201AG.

NOTES: (1) All specifications pertain to both PGA200 and PGA201. Values for gains of 10, 100, and 1000 for the PGA200 are the same for gains of 8, 64 and 512. (2) Measured with a 10kΩ load. (3) Adjustable to zero. This offset is the total offset including both input and output components referred to the input. (4) Noise due to the input stage. There is also an output component which becomes significant in low gain (see Typical Performance Curves). (5) Settling time of the average value of the output waveform since the noise floor in a gain of 1000 is on the order of 0.01% of full scale.

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation	600mW
Analog And Digital Inputs	±V_{CC}
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering 10 Seconds)	+300°C
Output Short-Circuit Duration	Continuous To Ground
Junction Temperature	175°C

PIN DESIGNATIONS

1.	AO	8.	Analog Common
2.	$\overline{WR}$	9.	Output
3.	$-V_{CC}$	10.	Offset Trim
4.	Common-Mode Voltage	11.	Offset Trim
5.	NC	12.	$+V_{CC}$
6.	+IN	13.	Digital Common
7.	−IN	14.	A1

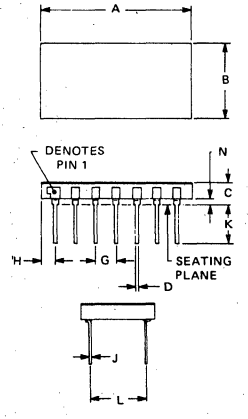
ORDERING INFORMATION

PGA200 or PGA201 X G

Grade: A, B

14-pin DIP, G package

MECHANICAL



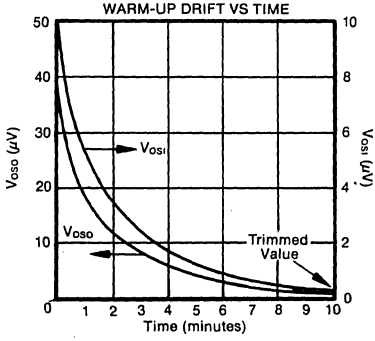
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.770	.810	19.56	20.57
B	.480	.500	12.19	12.70
C	.155	.215	3.94	5.46
D	.016	.020	.41	.51
G	.100 BASIC		2.54 BASIC	
H	.080	.110	2.03	2.79
J	.009	.012	.23	.30
K	.150	.210	3.81	5.33
L	.300 BASIC		7.62 BASIC	
N	.015	.035	.38	.89

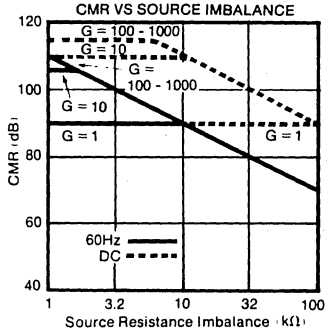
TYPICAL PERFORMANCE CURVES

T_A = +25°C, ±V_{CC} = 15VDC, unless otherwise noted.

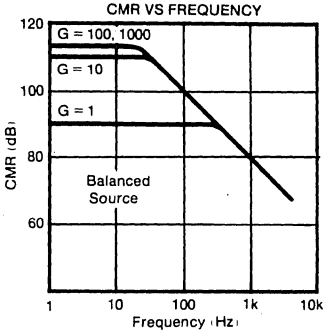
WARM-UP DRIFT VS TIME



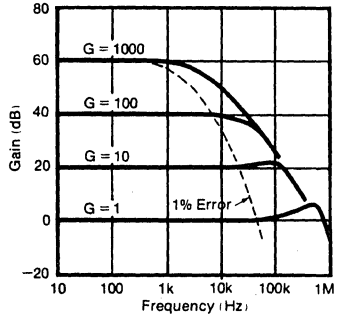
CMR VS SOURCE IMBALANCE



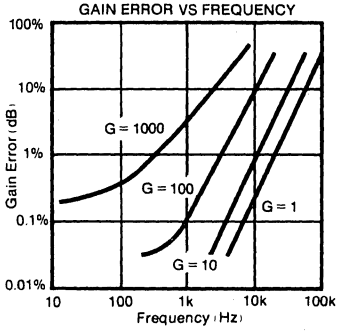
CMR VS FREQUENCY



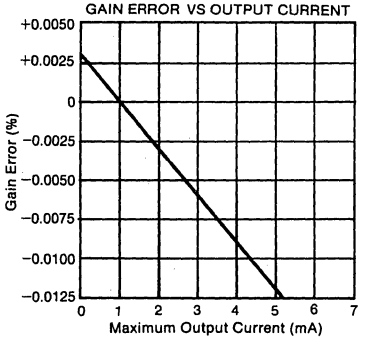
GAIN VS FREQUENCY



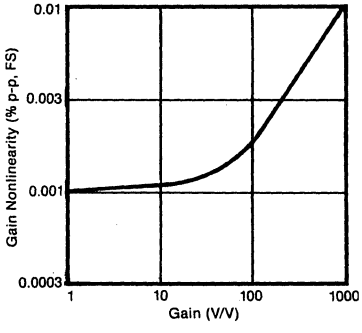
GAIN ERROR VS FREQUENCY



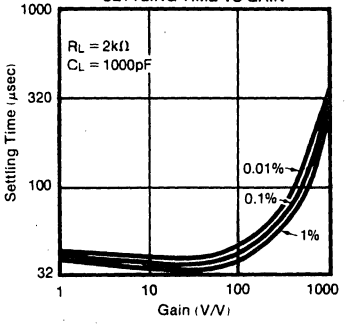
GAIN ERROR VS OUTPUT CURRENT



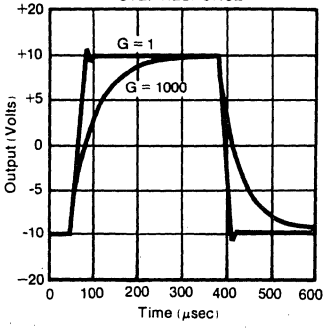
GAIN NONLINEARITY VS GAIN



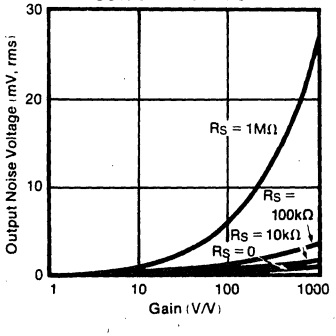
SETTLING TIME VS GAIN



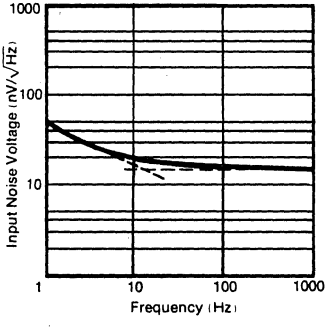
STEP RESPONSE



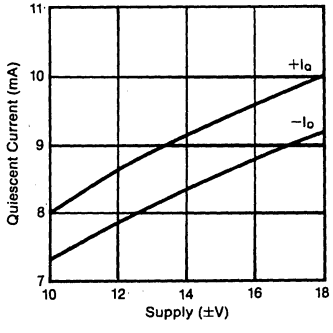
OUTPUT NOISE VS GAIN



INPUT NOISE VOLTAGE VS FREQUENCY 100 ≤ GAIN ≤ 1000



IQ VS SUPPLY



THEORY OF OPERATION

A simplified block diagram of the PGA200/201 appears on the first page. The diagram consists of three distinct parts. Together these parts form a high-perfomance, differential-input, digitally-programmable dedicated gain block. Each of the parts is optimized for a specific function.

The operational amplifiers are arranged on a monolithic substrate in the classical three-op-amp IA configuration. A nitride-passivated compatible thin-film bipolar process is used to achieve excellent offset and common-mode rejection stability over time and temperature. Advanced laser trimming techniques are used to minimize both the initial input offset and the input offset drift which are typically below 10μV and 0.15μ/V°C respectively. Additionally, careful layout techniques assure input stage thermal tracking with varying load conditions.

The gain-setting resistors are arranged on a separate substrate which is thermally isolated from the output stage. This results in minimum thermal interaction and a layout optimized for resistor tracking. All gains are dependent on the ratio of resistors which are composed of combinations of equal valued segments. The segmented approach provides the ultimate in accuracy and stability.

The latch and multiplexer, which set the gain, are implemented in CMOS. This provides high impedance logic inputs, low quiescent current and TTL compatibility without the need for a separate logic power supply. The logic threshold is internally derived from the $+V_{CC}$ power supply and is referenced to digital common. The circuit is arranged so that multiplexer ON resistance is in series with the high input impedance of the input amplifiers and hence contributes negligible gain error.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper analog and digital power supply connections. The analog supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors with connections made as close as possible to the amplifier supply terminals and load common connection.

Because the amplifier is direct-coupled, it must have a ground return path for the bias currents associated with the amplifier inputs at pins 6 and 7. If the ground return path is not inherent in the signal source (floating source), it must be provided externally. The ground return resistance (R_{gr}) should be kept as low as practical. The upper limit is approximately 50MΩ because of the input bias current of the amplifier and its common-mode voltage range.

In order to maintain linear operation of the input amplifiers the common-mode input voltage must be kept within the following limits:

$$-10V + (E_{in} \times G)/2 < E_{cm} < +10V - (E_{in} \times G)/2.$$

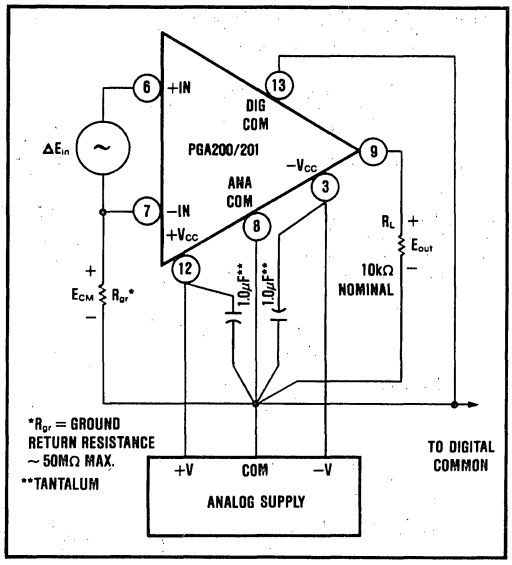


FIGURE 1. Power Supply and Signal Connections.

GAIN SETTING

Gain is determined by a 2-bit digital word applied to the A0 and A1 inputs (see Table I). The $\overline{WR}$ (pin 2) provides a latch function. When $\overline{WR}$ is a logic low, the latch is transparent and the gain directly follows the code on A0 and A1. When $\overline{WR}$ goes to a logic high, the gain is latched according to the previous state of A0 and A1. The timing requirements illustrated in Figure 2 must be observed. The minimum write pulse width is 300nsec while the data setup and hold times are 180nsec and 30nsec respectively. Although the logic inputs are TTL compatible, they are high impedance and the allowable logic high voltage extends to $+V_{CC}$.

Table I shows the gain select truth table. The gains for the PGA201 are shown in parenthesis.

TABLE I. Gain Select Truth Table.

A1	A0	$\overline{WR}$	GAIN PGA200 [PGA201]
X	X	⎍	Maintains previous gain
0	0	0	1 (1)
0	1	0	10 (8)
1	0	0	100 (64)
1	1	0	1000 (512)

Logic "1": $V_{AH} \geq 2.4V$
Logic "0": $V_{AL} \leq 0.8V$

INPUT AND OUTPUT OFFSETTING

Figure 3 illustrates the appropriate connections for offset adjustment. Since the instrumentation amplifier is a two-stage device, the total offset is composed of two parts, an input and an output component. Because both are actively laser trimmed, adjustment is not required in most applications. The input component is due to the mismatch in the offset voltage of the two input amplifiers

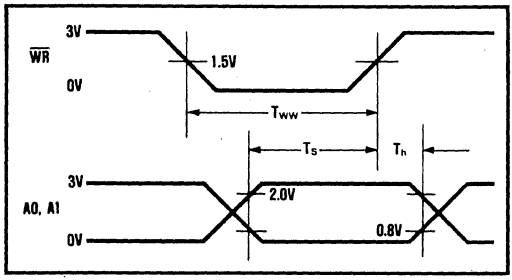


FIGURE 2. Timing Diagrams.

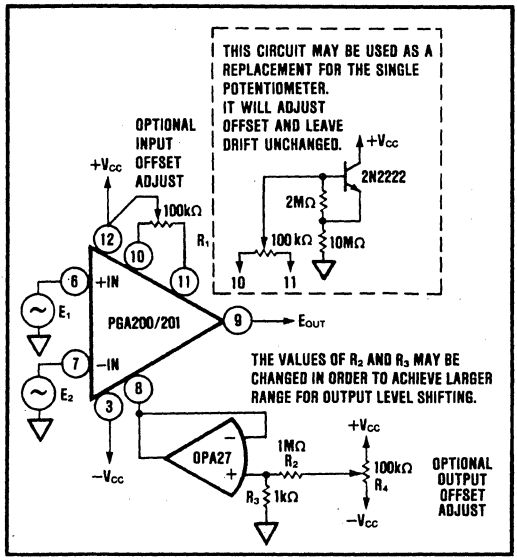


FIGURE 3. Optional Input/Output Offset Adjust.

and changes with gain. The output component is due to the offset of the second stage amplifier and is constant.

R_1 may be used to null the input offset. Its quality will affect the results; therefore, choose a potentiometer with good temperature and mechanical resistance stability. The wiper should be connected to $+V_{CC}$ at a point as close as possible to the $+V_{CC}$ terminal of the instrumentation amplifier. Null the offset as follows:

1. Set $E_1 = E_2 = 0$ (be sure a good ground return path exists to the inputs).
2. Set the gain to 1000 (or 512 for PGA201).
3. Adjust R_1 until the output reaches 0V ±1mV or desired value.

Input offset adjustment will affect the offset drift by approximately 3.1μV/°C/mV of offset that is trimmed. This effect can be greatly reduced by using the alternate offset adjust circuit shown inside the dashed line.

The output offset may be nulled or, alternately, the output can be level shifted with R_4. R_2 and R_3 divide the wiper voltage of R_4 down for increased sensitivity. Their ratio may be changed in order to increase the range of adjustment if desired. The buffer amplifier is required in order to keep the impedance at pin 8 low so that the gain and common-mode rejection will not be disturbed.

GUARD DRIVE

Use of the guard drive connection in Figure 4 can improve system common-mode rejection when the distributed capacitance of the input lines is significant.

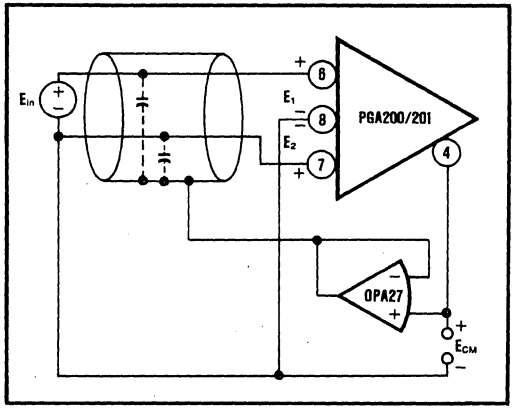


FIGURE 4. Guard Drive.

The common-mode voltage which appears on pin 4 is resistively derived from the output of the first stage amplifiers and has the value $(E_1 - E_2)/2$. This voltage is used to drive the shield which preferably should extend up to and around the input pins 6 and 7. This configuration improves common-mode rejection by reducing the common-mode current flow. The buffer amplifier is used in order to supply more current than the internal 20kΩ resistors can provide so that the guard can accurately track the actual common-mode voltage.

TYPICAL APPLICATIONS

The PGA200 and PGA201 are ideal for computer-controlled data acquisition systems as shown in Figure 5.

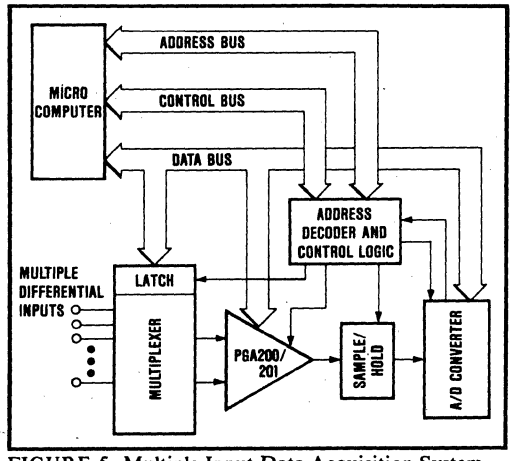


FIGURE 5. Multiple Input Data Acquisition System With Various Input Ranges.

BURR-BROWN®

XTR100

Precision, Low Drift 4mA to 20mA TWO-WIRE TRANSMITTER

FEATURES

- INSTRUMENTATION AMPLIFIER INPUT
  - Low Offset Voltage, 25μV max
  - Low Voltage Drift, 0.5μV/°C max
  - Low Nonlinearity, 0.01% max
- TRUE TWO-WIRE OPERATION
  - Power and Signal on One Wire Pair
  - Current Mode Signal Transmission
  - High Noise Immunity
- DUAL MATCHED CURRENT SOURCES
- WIDE SUPPLY RANGE, 11.6V to 40V
- -40°C TO +85°C SPECIFICATION RANGE
- SMALL 14-PIN DIP PACKAGE

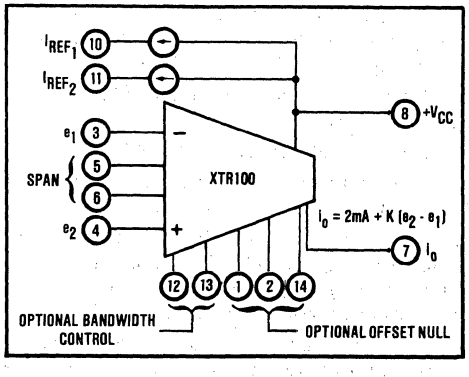
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  - Pressure Transmitters
  - Temperature Transmitters
  - Millivolt Transmitters
- RESISTANCE BRIDGE INPUTS
- THERMOCOUPLE INPUTS
- RTD INPUTS
- CURRENT SHUNT (mV) INPUTS
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR100 is a microcircuit, 4mA to 20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage controlled output current source, and dual-matched precision current references. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTD's, thermistors, and strain gauge bridges. State-of-the art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers. Also, the XTR100 is generally very useful for low noise, current-mode signal transmission.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, +V_{CC} = 24VDC, R_L = 100Ω unless otherwise noted.

PARAMETER	CONDITIONS/DESIGNATION	XTR100AM/AP MIN	XTR100AM/AP TYP	XTR100AM/AP MAX	XTR100BM/BP MIN	XTR100BM/BP TYP	XTR100BM/BP MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS								
Current	Linear Operating Region	4		20	*		*	mA
Current	Derated Performance	3.8		22	*		*	mA
Current Limit	I_O min		28	38		*	*	mA
Offset Current Error	I_{OS}, I_O = 4mA		±1.5	±4		*	*	µA
Offset Current Error vs Temp.	$\Delta I_{OS}/\Delta T$		±5	±10		*	*	ppm, FS/°C
Full Scale Output Current Error	Full Scale = 20mA			±20			*	µA
Power Supply Rejection		110	135		*	*		dB
Power Supply Voltage	V_{CC}, pins 7 & 8, compliance(1)	+11.6		+40	*		*	VDC
Load Resistance	At V_{CC} = +24V, I_O = 20mA			600			*	Ω
	At V_{CC} = +40V, I_O = 20mA			1400			*	Ω
SPAN								
Equation	R_S in Ω, e_1 and e_2 in V	$i_O = 4mA + [0.016Ω + (40/R_S)]\ (e_2 - e_1)$						
Untrimmed Error(2)	ϵ_{SPAN}	-5	-2.5	0	*	*	*	%
Nonlinearity	$\epsilon_{NONLINEARITY}$			0.01			*	%
Hysteresis			0			*		%
Dead Band			0			*		%
Temperature Effects			30	±100		*	*	ppm %/°C
INPUT CHARACTERISTICS								
Impedance								
Differential			0.4 || 0.047			*		GΩ || µF
Common-Mode			10 || 180			*		GΩ || pF
Voltage Range, Full Scale	$\Delta e = (e_2 - e_1)$(3)	0		1	*		*	V
Offset Voltage	V_{OS}			±50			±25	µV
vs Temperature	$\Delta V_{OS}/\Delta T$		±0.7	±1		±0.25	±0.5	µV/°C
Bias Current	I_B		60	150		*	*	nA
vs Temperature	$\Delta I_B/\Delta T$		0.30	1		*	*	nA/°C
Offset Current	I_{OSI}		10	±30		*	±20	nA
vs Temperature	$\Delta I_{OSI}/\Delta T$		0.1	0.3		*	*	nA/°C
Common-Mode Rejection(4)	DC	90	100		*	*	*	dB
Common-Mode Range	e_1 and e_2 with respect to pin 7	4		6	*		*	V
CURRENT SOURCES								
Magnitude			1			*		mA
Accuracy	V_{CC} = 24V, $V_{PIN\ 8} - V_{PIN\ 10,\ 11}$ = 19V, R_2 = 5kΩ, Fig. 3		±0.03	±0.1		±0.015	±0.05	%
vs Temperature				±30			*	ppm/°C
vs Time			±8			*		ppm/mo.
Ratio Match	Tracking							
Accuracy	1 - I_{REF1}/I_{REF2}		±0.006	±0.02			*	%
vs Temperature				±15			10	ppm/°C
vs Time			±1			*		ppm/mo.
Output Impedance		10	20		*			MΩ
TEMPERATURE RANGE								
Specification		-40		+85	*		*	°C
Operating (AM, BM)		-55		+125	*		*	°C
(AP, BP)		-40		+85	*		*	°C
Storage (AM, BM)		-55		+165	*		*	°C
(AP, BP)		-40		+85	*		*	°C

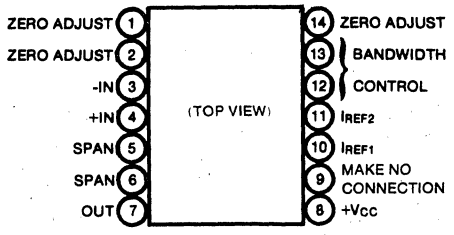
*Same as XTR100AM/AP.

NOTES:
1. See Typical Performance Curves.
2. Span error shown is untrimmed and may be adjusted to zero.
3. e_1 and e_2 are signals on the -IN and +IN terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR100A and XTR100B grades respectively. 2mV FS is also possible with the B grade; but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise.
4. Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed. See Application Information section.

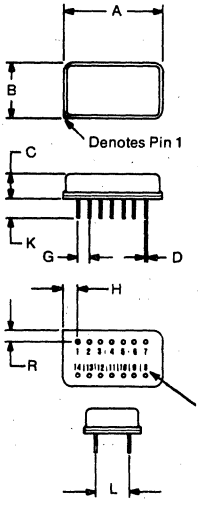
ABSOLUTE MAXIMUM RATINGS

Power Supply, Vcc	40V
Input Voltage, e_1, or e_2	≥ VOUT, ≤ +Vcc
Storage Temperature Range, metal	-55°C to +165°C
Storage Temperature Range, plastic	-40°C to +85°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	+165°C

PIN DESIGNATIONS



MECHANICAL



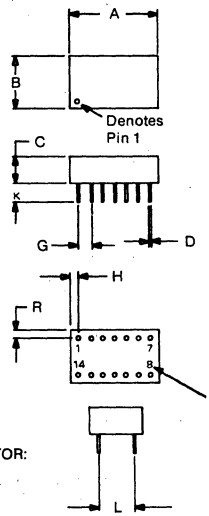
XTR100AM/BM (Metal)

NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

Pin numbers shown for reference only. Numbers are not marked on package.

MATING CONNECTOR: 0145MC



XTR100AP/BP (Plastic)

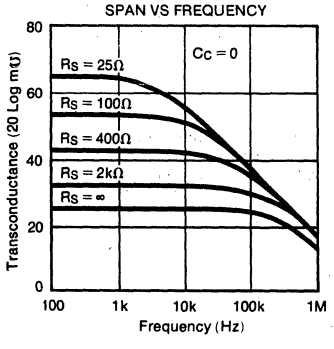
NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

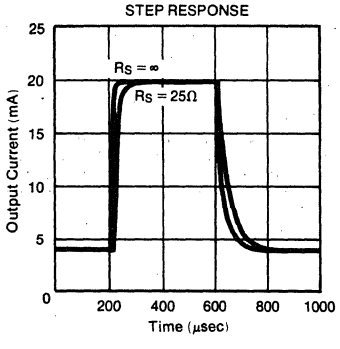
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.210	4.83	5.33
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

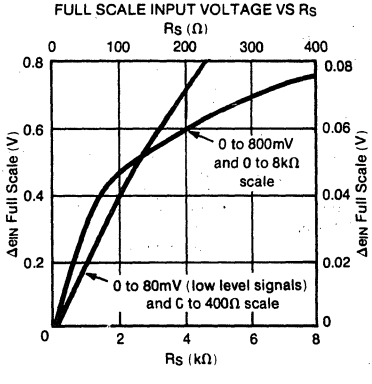
Pin numbers shown for reference only. Numbers are not marked on package.

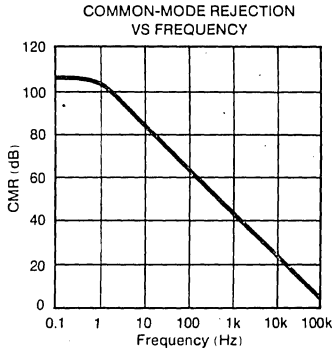
TYPICAL PERFORMANCE CURVES

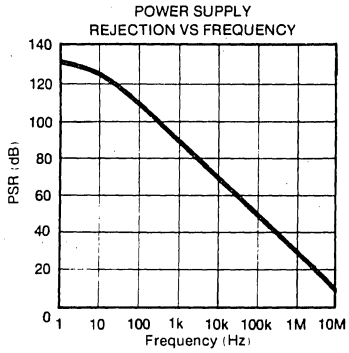
(T_A = +25°C, +Vcc = 24VDC unless otherwise noted)

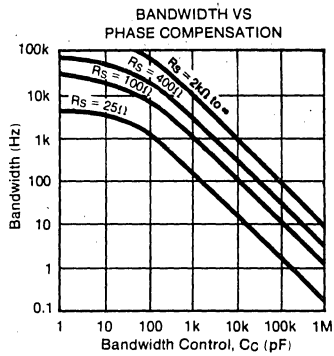


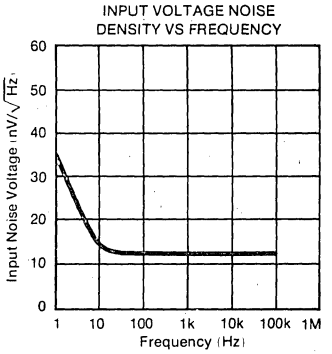


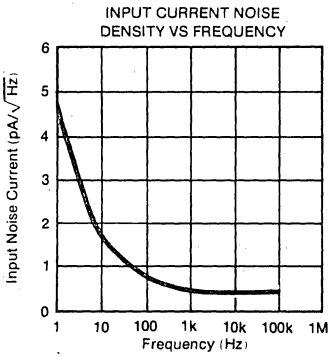


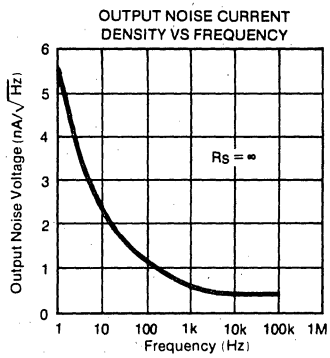












THEORY OF OPERATION

A simplified schematic of the XTR100 is shown in Figure 1. Basically the amplifiers, A_1 and A_2, act as an instrumentation amplifier controlling a current source, A_3 and Q_1. Operation is determined by an internal feedback loop. e_1 applied to pin 3 will also appear at pin 5 and similarly e_2 will appear at pin 6. Therefore the current in R_S, the span setting resistor, will be $I_S = (e_2 - e_1)/R_S = e_{IN}/R_S$. This current combines with the current, I_3, to form I_1. The circuit is configured such that I_2 is 19 times I_1. From this point the derivation of the transfer function is straightforward but lengthy. The result is shown in Figure 1.

Examination of the transfer function shows that I_O has a lower range-limit of 4mA when $e_{IN} = e_2 - e_1 = 0V$. This 4mA is composed of 2mA quiescent current exiting pin 7 plus 2mA from the current sources. The upper range limit of I_O is set to 20mA by the proper selection of R_S based on the upper range limit of e_{IN}. Specifically R_S is chosen for a 16mA output current span for the given full scale input voltage span; i.e., $(0.016\Omega + 40/R_S)(e_{IN}$ full scale$) = 16mA$. Note that since I_O is unipolar e_2 must be kept larger than e_1; i.e., $e_2 \geq e_1$ or $e_{IN} \geq 0$. Also note that in order not to exceed the output upper range limit of 20mA, e_{IN} must be kept less than 1V when $R_S = \infty$ and proportionately less as R_S is reduced.

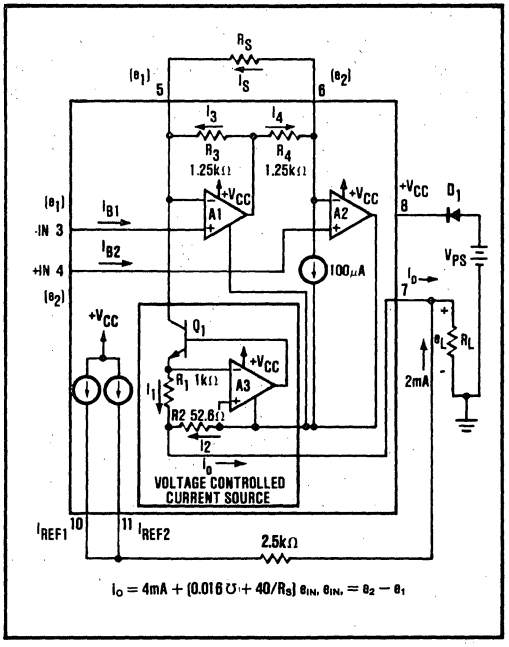


FIGURE 1. Simplified Schematic of the XTR100.

INSTALLATION AND OPERATING INSTRUCTIONS

Major points to consider when designing with the XTR100:

1. The leads to R_S should be kept as short as possible to reduce noise pick-up and parasitic resistance.
2. $+V_{CC}$ should be bypassed with a 0.01μF capacitor as close to the unit at possible (pin 8 to 7).
3. Always keep the input voltages within their range of linear operation
   $$+4V \leqslant e_1 \leqslant +6V$$
   $$+4V \leqslant e_2 \leqslant +6V$$
   (e_1 and e_2 measured with respect to pin 7).
4. The maximum input signal level ($e_{IN_{FS}}$) is 1V with $R_S = \infty$ and proportionally less as R_S decreases.
5. Always return the current references (pins 10 and 11) to the output (pin 7) through an appropriate resistor. If the references are not used for biasing or excitation connect them together and through a 1kΩ resistor to pin 7. Each reference must have between +1V and +(V_{CC} -4V) with respect to pin 7. Filter with one 0.01μF or two 0.0047μF capacitors.
6. Always choose R_L (including line resistance) so that the voltage between pins 7 and 8 ($+V_{CC}$) remains within the 11.6V to 40V range as the output changes between the 4mA to 20mA range (see Figure 2).
7. It is recommended that a reverse polarity protection diode (D_1 in Figure 1) be used. This will prevent damage to the XTR100 caused by momentary (e.g., transient) or long term application of the wrong polarity of voltage between pins 7 and 8.
8. When the XTR100 is in high gain, use a compensation capacitor, pins 12 and 13, and consider PC board layout which minimizes parasitic capacitance.

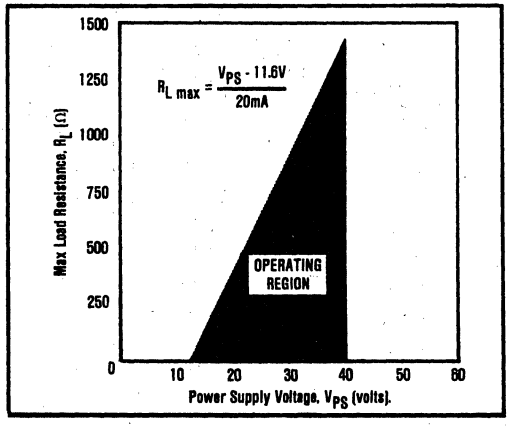


FIGURE 2. Power Supply Operating Range.

SELECTING R_S

R_{SPAN} is chosen so that a given full scale input span $e_{IN_{FS}}$ will result in the desired full scale output span of ΔI_{OFS},

$[(0.016\Omega) + (40/R_S)]\,\Delta e_{IN} = \Delta I_O = 16mA.$

Solving for R_S;

$$R_S = \frac{40}{\Delta I_O/\Delta e - 0.016\Omega} \qquad (1)$$

For example, if $\Delta e_{IN_{FS}} = 100mV$ for $\Delta I_{O_{FS}} = 16mA$

$$R_S = \frac{40}{(16mA/100mV)} = \frac{40}{0.16 - 0.016} = \frac{40}{0.144} = 278\Omega$$

See Typical Performance Curves for a plot of R_S vs $\Delta e_{IN_{FS}}$. Note that in order not to exceed the 20mA upper range limit e_{IN} must be less than 1V when $R_S = \infty$ and proportionately smaller as R_S decreases.

BIASING THE INPUTS

The internal circuitry of the XTR100 is such that both e_1 and e_2 must be kept approximately 5V above the voltage at pin 7. This is easily done by using one or both current sources and an external resistor R_2. Figure 3 shows the simplest case - a floating voltage source e'_2. The 2mA from the current sources flows through the 2.5kΩ value of R_2 and both e_1 and e_2 are raised by the required 5V with respect to pin 7. For linear operation the constraint is

$$+4V \leqslant e_1 \leqslant +6V$$
$$+4V \leqslant e_2 \leqslant +6V$$

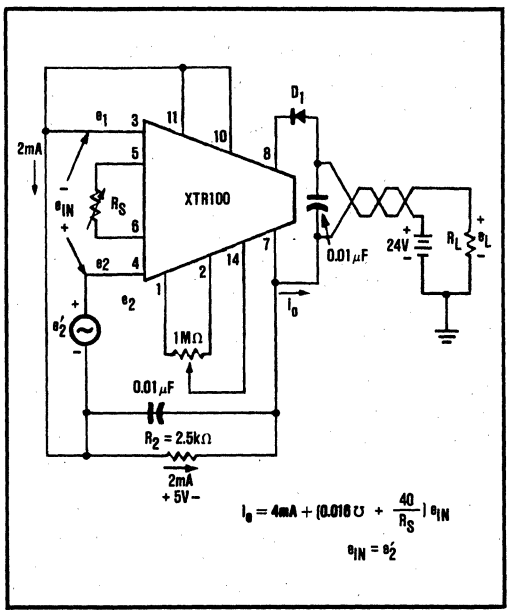


FIGURE 3. Basic Connection for Floating Voltage Source.

Figure 4 shows a similar connection for a resistive transducer. The transducer could be excited either by one (as shown) or both current sources.

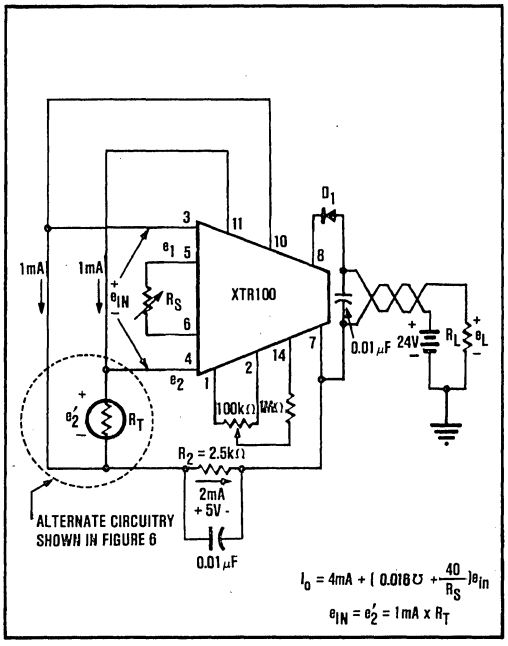


FIGURE 4. Basic Connection for Resistive Source.

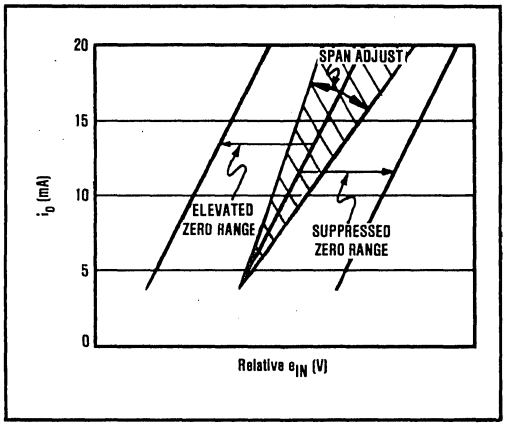


FIGURE 5. Elevation and Suppression Graph.

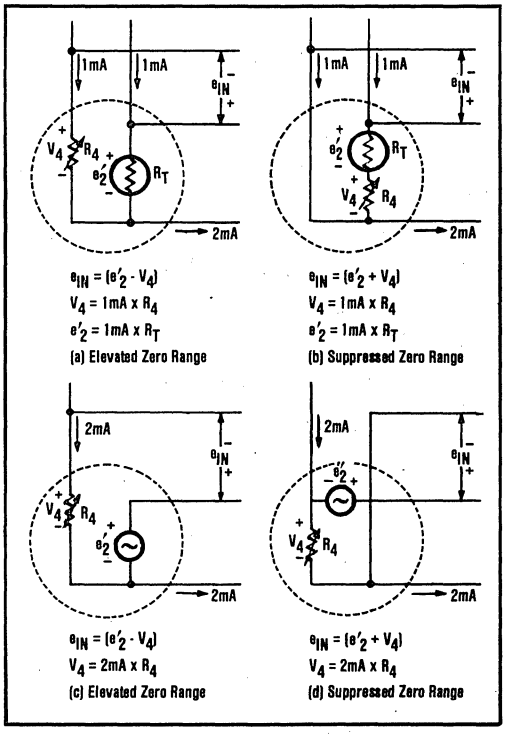


FIGURE 6. Elevation and Suppression Circuits.

CMV AND CMR

Thus the XTR100 is designed to operate with a nominal 5V common-mode voltage at the input and will function properly with either input operating over the range of 4V to 6V with respect to pin 7. The error caused by the 5V CMV is already included in the accuracy specifications. If the inputs are biased at some other CMV then an input offset error term is (CMV - 5)/CMRR; CMR is in dB, CMRR is in V/V.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (input signal elevation) or elevated zero range (input signal suppression). This is easily accomplished with the XTR100 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figures 5 and 6(a). In this example the sensor voltage is derived from R_T (a thermistor, RTD or other variable resistance element) excited by one of the 1mA current sources. The other current source is used to create the elevated zero range voltage. Figures 6(b), (c) and (d) show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments. Note: It is not recommended to use the optional offset voltage null (pins 1, 2, and 14) for elevation/suppression. This trim capability is used only to null the amplifier's input offset voltage. In many applications the already low offset voltage (typically 20μV) will not need to be nulled at all. Adjusting the offset voltage to nonzero values will disturb the voltage drift by ±0.3μV/°C per 100μV of induced offset.

APPLICATION INFORMATION

The small size, low offset voltage and drift, excellent linearity, and internal precision current sources, make the XTR100 ideal for a variety of two-wire transmitter applications. It can be used by OEM's producing different types of transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise

interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus the XTR100 is, in general, very suitable for individualized and special purpose applications.

EXAMPLE 1 - RTD Transducer shown in Figure 7. Given a process with temperature limits of +25°C and +150°C, configure the XTR100 to measure the temperature with a platinum RTD which produces 100Ω at 0°C and 200Ω at +266°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C.

Computing R_S.

The sensitivity of the RTD is $\Delta R/\Delta T = 100\Omega/266°C$. When excited with a 1mA current source for a 25°C to 150°C range (i.e., 125°C span) the span of e_{IN} is 1mA x (100Ω/266°C) x 125°C = 47mV = Δe_{IN}.

$$\text{From equation 1, } R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{in}} - 0.016\,\mho}$$

$$R_S = \frac{40}{\frac{16mA}{47mV} - 0.016\,\mho} = \frac{40}{0.3244} = 123.3\Omega$$

Span adjustment (calibration) is accomplished by trimming R_S.

Computing R_4:

$$\text{At } 25°C,\ e'_2 = 1mA \times [100\Omega + (\frac{100\Omega}{266°C} \times 25°C)]$$
$$= 1mA \times 109.4\Omega$$
$$= 109.4mV$$

In order to make the lower range limit of 25°C correspond to the output lower range limit of 4mA the input circuitry shown in Figure 7 is used.

e_{IN} is made 0 at 25°C
or $e'_{2\,25°C} - V_4 = 0$
thus, $V_4 = e'_{2\,25°C} = 109.4mV$

$$R_4 = \frac{V_4}{1mA} = \frac{109.4mV}{1mA} = 109.4\Omega$$

Computing R_2 and checking CMV:

At 25°C, $e'_2 = 109.4mV$

$$\text{At } 150°C,\ e'_2 = 1mA \times [100\Omega + (\frac{100\Omega}{266°C} \times 150°C)]$$
$$= 156.4mV$$

Since both e'_2 and V_4 are small relative to the desired 5V common-mode voltage they may be ignored in computing R_2 as long as the CMV is met.

$R_2 = 5V/2mA = 2.5k\Omega$

e_2 min = 5V + 0.1094V
e_2 max = 5V + 0.1564V
e_1 = 5V + 0.1094V

The +4V to +6V CMV requirement is met.

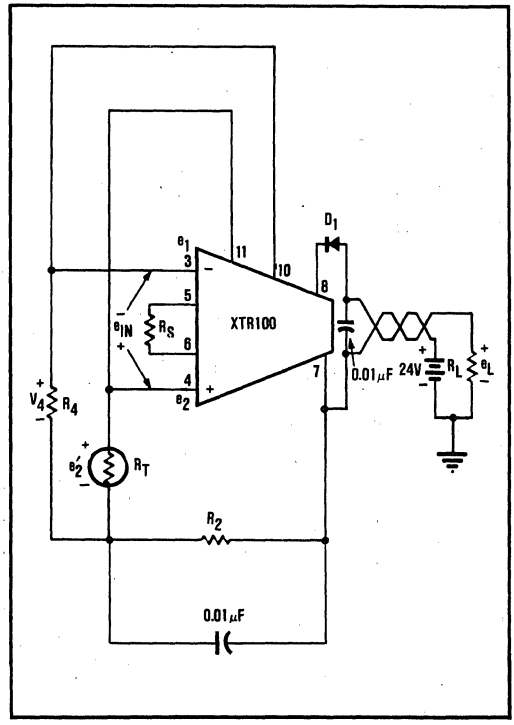


FIGURE 7. Circuit for Example 1.

EXAMPLE 2 - Thermocouple Transducer shown in Figure 8. Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the XTR100 to measure the temperature with a type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, V_{R6}, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At a typical ambient of +25°C this is 1.28mV (obtained from standard thermocouple tables with reference junction of 0°C). Transmit 4mA for T_1 = 0°C and 20mA for T_1 = +1000°C. Note: $e_{IN} = e_2 - e_1$ indicates that T_1 is relative to T_2.

Establishing R_S:

The input full scale span is 58mV ($\Delta e_{IN_{FS}} = 58mV$).

R_S is found from equation (1)

$$R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{IN}} - 0.016\,\mho}$$

$$= \frac{40}{\frac{16mA}{58mV} - 0.016\,\mho} = \frac{40}{0.2599}$$

$R_S = 153.9\Omega$

Selecting R_4:

R_4 is chosen to make the output 4mA at $T_{TC} = 0°C$ (V_{TC} = -1.28mV) and $T_D = 25°C$ ($V_D = 0.6V$). A circuit is shown in Figure 8.

V_{TC} will be -1.28mV when $T_{TC} = 0°C$ and the reference junction is at +25°C. e_1 must be computed for the condition of $T_D = +25°C$ to make $e_{IN} = 0V$.

$V_{D_{25°C}}$ = 600mV.
$e_{1_{25°C}}$ = 600mV x 51/2051 = 14.9mV
e_{IN} = $e_2 - e_1 = +V_{TC} + V_4 - e_1$
with e_{IN} = 0 and V_{TC} = -1.28mV
V_4 = $e'_1 + e_{IN} - V_{TC}$ = 14.9mV + 0V -(-1.28mV)
1mA x R_4 = 16.18mV
R_4 = 16.18Ω

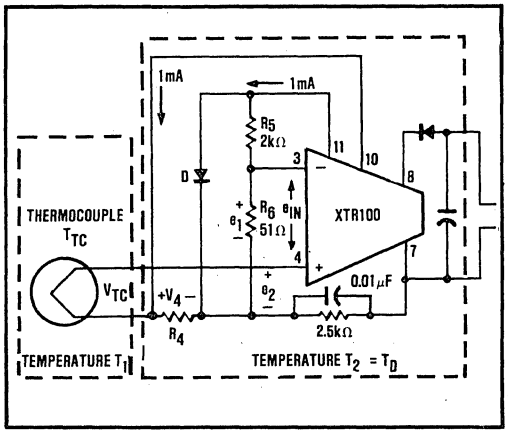


FIGURE 8. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

Cold Junction Compensation:

The temperature reference circuit is shown in Figure 9.

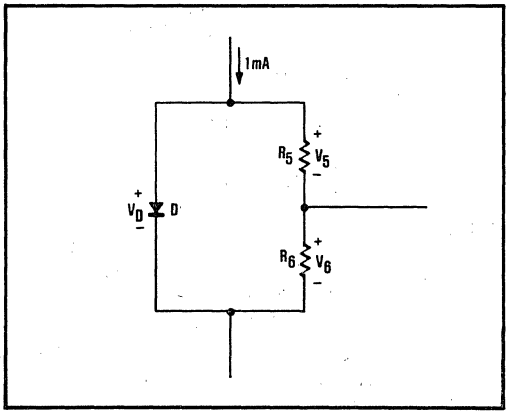


FIGURE 9. Cold Junction Compensation Circuit.

The diode voltage has the form

$$V_D = \frac{KT}{q} \ln \frac{I_{DIODE}}{I_{SAT}}$$

Typically at $T_2 = 25°C$, $V_D = 0.6V$ and $\Delta V_D/\Delta T$ = -2mV/°C. R_5 and R_6 form a voltage divider for the diode voltage V_D. The divider values are selected so that the gradient $\Delta V_D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At 25°C this is approximately 52μV/°C (obtained from standard thermocouple table) therefore,

$$\Delta V_{TC}/\Delta T = \Delta V_D/\Delta T \left(\frac{R_6}{R_5 + R_6}\right) \quad (2)$$

$$52\mu V/°C = 2000\mu V/°C \left(\frac{R_6}{R_5 + R_6}\right)$$

R_5 is chosen as 2kΩ to be much larger than the resistance of the diode. Solving for R_6 yields 51Ω.

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to either limit when the thermocouple impedance goes very high. The circuits of Figures 14 and 15 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the +input (large impedance) will cause I_O to go to its lower range limit value (about 3.8mA). If up scale indication is desired the circuit of Figure 16 should be used. When the TC opens the output will go to its upper range limit value (about 25mA or higher).

OPTIONAL INPUT OFFSET VOLTAGE TRIM

The XTR100 has provisions for nulling the input offset voltage associated with the input amplifiers. In many applications the already low offset voltage (25μV max for the B grade, 50μV max for the A grade) will not need to be nulled at all. The null adjustment can be done with a potentiometer at pins 1, 2, and 14 as shown in Figures 3 and 4. Either of these two circuits may be used. NOTE: It is not recommended to use this input offset voltage nulling capability for elevation or suppression. See the Signal Suppression and Elevation section for the proper techniques.

OPTIONAL BANDWIDTH CONTROL

Low-pass filtering is recommmended where possible and can be done by either one of two techniques shown in Figure 10. C_2 connect to pins 3 and 4 will reduce the bandwidth with a cutoff frequency given by,

$$f_{CO} = \frac{1.59 \times 10}{(R_1 + R_2 + R_3 + R_4)(C_2 + 0.047\mu F)}$$

with f_{CO} in Hz, all R_S in Ω and C_2 in μF. This method has the disadvantage of having f_{CO} vary with R_1, R_2, R_3, R_4, and it may require large values of R_3 and R_4. The other method, using C_1 will use smaller values of capacitance and is not a function of the input resistors. It is however, more subject to nonlinear distortion caused by slew rate limiting. This is normally not a problem with the slow signals associated with most process control transducers. The relationship between C_1 and f_{CO} is shown in the Typical Performance Curves.

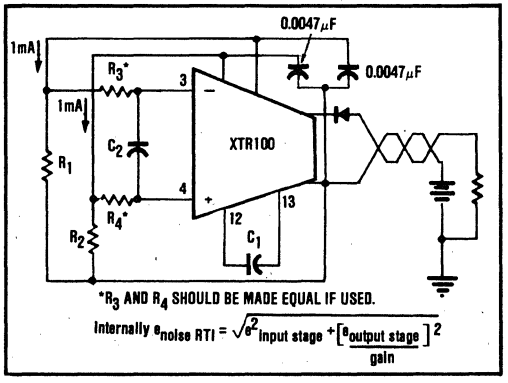


FIGURE 10. Optional Filtering.

APPLICATION CIRCUITS

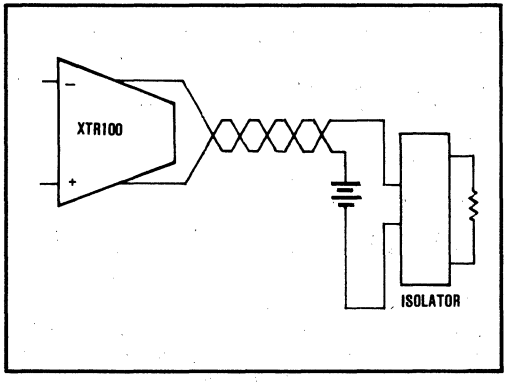


FIGURE 11. XTR100 with Loop-powered Isolation.

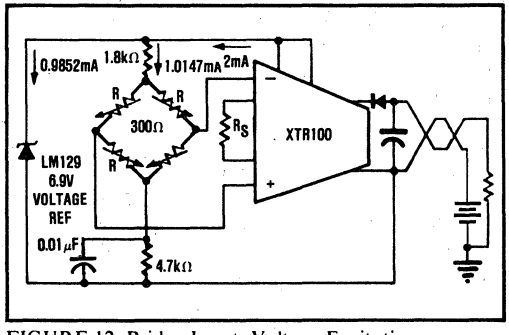


FIGURE 12. Bridge Input, Voltage Excitation.

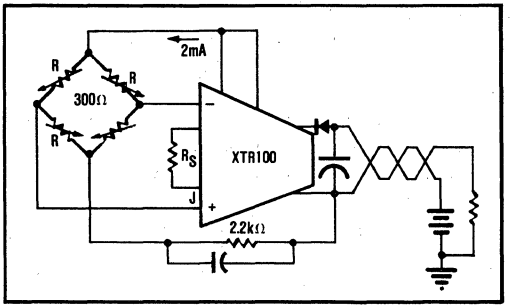


FIGURE 13. Bridge Input, Current Excitation.

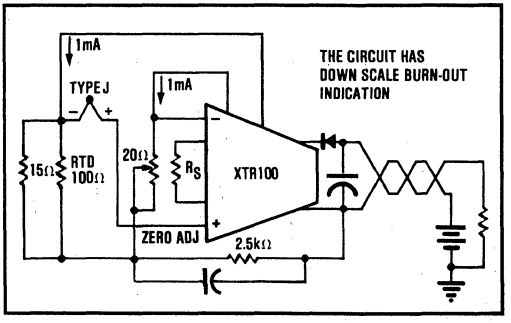


FIGURE 14. Thermocouple Input with RTD Cold Junction Compensation.

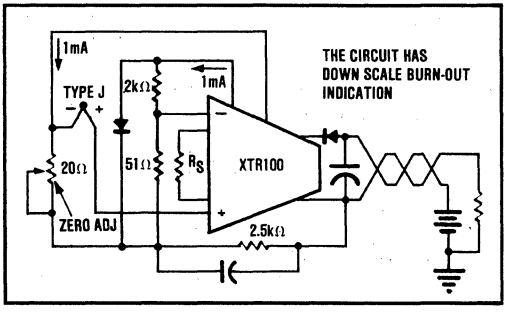


FIGURE 15. Thermocouple Input with Diode Cold Junction Compensation.

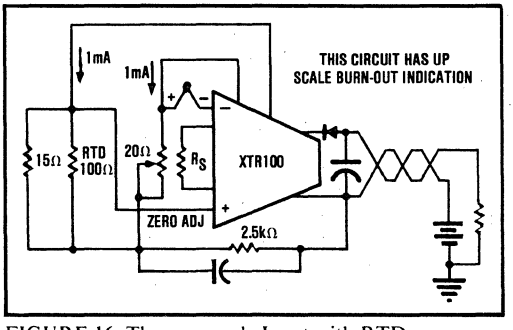


FIGURE 16. Thermocouple Input with RTD Cold Junction Compensation.

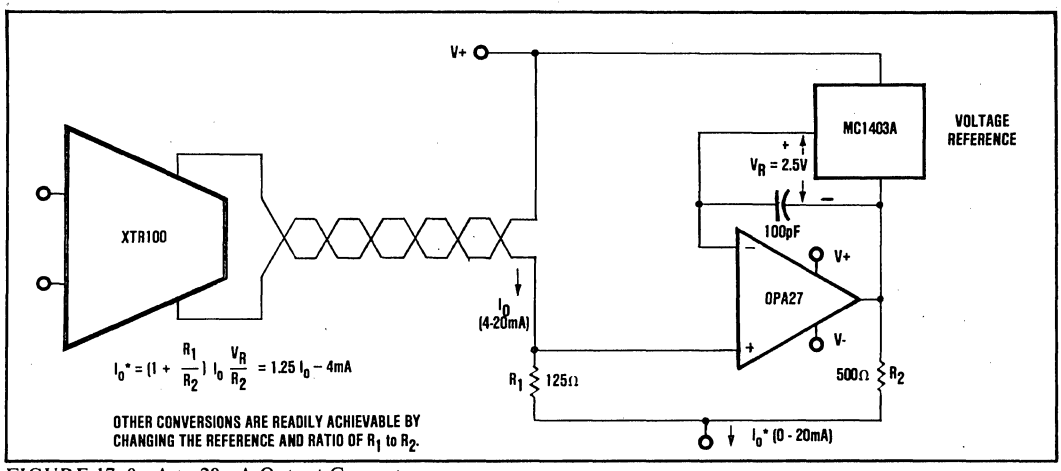


FIGURE 17. 0mA to 20mA Output Converter.

DETAILED ERROR ANALYSIS

The ideal output current is

$$i_{O\ IDEAL} = 4mA + K\ e_{IN} \quad (3)$$

K is the span (gain) term, $(0.016mA/mV) + (40/R_S)$

The nature of the XTR100 circuit is such that there are three major components of error

σ_O = error associated with the output stage.
σ_S = errors associated with span adjustment.
σ_I = errors associated with input stage.

The transfer function including these errors is

$$I_{O\ ACTUAL} = (4mA + \sigma_O) + K\ (1 + \sigma_S)(e_{IN} + \sigma_I) \quad (4)$$

When this expression is expanded, second order terms (σ_S σ_I) dropped, and terms collected, the result is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\ e_{IN} \text{ "} K\sigma_I + K\sigma_S\ e_{IN} \quad (5)$$

The error in the output current is $i_{O\ ACTUAL}$ - $i_{O\ IDEAL}$ and can be found by subtracting equations (5) and (3).

$$i_{O\ ERROR} = \sigma_O + K\sigma_S + K\ \sigma_S\ e_{IN} \quad (6)$$

This is a general error expression. The composition of each component of error depends on the circuitry inside the XTR100 and the particular circuit in which it is applied. The circuit of Figure 7 will be used to illustrate the principles.

$$\sigma_O = Ios_{RTO} \quad (7)$$

Ios_{RTO}* = the output offset error current.

For the circuit of Figure 7,

$$\sigma_I = V_{OSI} + [I_{B1}\ R_T - I_{B2}\ R_4] + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5V}{CMRR} \quad (8)$$

The term in brackets maybe written in terms of offset current and resistor mismatches as $I_{B1}\ \Delta R + I_{OS}' R_4$.

V_{OSI}* = input offset voltage
I_{B1},* I_{B2}* = input bias current
I_{OSI}* = input offset current
$\Delta R = R_T - R_4$ = mismatch in resistor
ΔV_{CC} = change supply voltage between pins 7 and 8 away from 24V nomimal
PSRR* = power supply rejection ratio
CMRR* = common-mode rejection ratio

$\sigma_S = \epsilon_{NONLIN} + \epsilon_{SPAN}$
ϵ_{NONLIN}* = span nonlinearity
ϵ_{SPAN}* = span equation error. Untrimmed error = 3% max. May be trimmed to zero.

*Items marked with an asterisk (*) can be found in the Electrical Specifications.

EXAMPLE 3

Given the circuit in Figure 7 with the XTR100B specifications and the following conditions: R_T = 109.4Ω at 25°C, R_T = 156.4Ω at 150°C, I_o = 4mA at 25°C, I_o = 20mA at 150°C, R_S = 123.3Ω, R_4 = 109Ω, R_L = 250Ω, R_{LINE} = 100Ω, V_{D1} = 0.6V, V_{PS} = 24V ±0.5%. Determine the % error at the upper and lower range values.

A. At the lower range value (T = 25°C).

$$\sigma_O = Ios_{RTO} = \pm 4\mu A$$

$$\sigma_I = V_{OSI} + [I_{B1}\ \Delta R + I_{OSI}\ R_4] + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5}{CMRR}$$

$$\Delta R = R_{T_{25°C}} - R_4 = 109.4 - 109 \approx 0$$

$$\Delta V_{CC} = 24 \times 0.005 + 4mA\ (250\Omega + 100\Omega) + 0.6V$$
$$= 120mV + 1400mV + 600mV = 2120mV$$

$e_1 = (2mA \times 2.5k\Omega) + (1mA \times 109\Omega) = 5.109V$
$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 109.4\Omega) = 5.1094V$
$(e_1 + e_2)/2 - 5 \approx 0$

$PSRR = 3.16 \times 10^5$ for 110dB
$CMRR = 31.6 \times 10^3$ for 90dB

$$\sigma_I = 25\mu V + (150nA \times 0 + 30nA \times 109\Omega) \quad (9)$$

$$+ \frac{2120mV}{3.16 \times 10^5} + \frac{0}{31.6 \times 10^3}$$

$$= 25\mu V + 3.27\mu V + 6.7\mu V + 0$$
$$= 34.97$$

$\sigma_S = \epsilon_{NONLIN} + \epsilon_{SPAN}$
$= 0.0001 + 0$ (assumes trim of R_S)
i_O error $= \sigma_O + K\,\sigma_I + K\,\sigma_S\,e_{IN}$

$$K = 0.016 + \frac{40}{R_S} = 0.016 + \frac{40}{123.3\Omega} = 0.341\text{Ʊ}$$

$e_{IN} = e_2 - V_4 = I_{REF1}\,R_{T_{25°C}} - I_{REF2}\,R_4$
since $R_{T\ 25°C} = R_4$
$e_{IN} = (I_{REF1} - I_{REF2})\,R_4 = 0.1\mu A \times 109\Omega = 10.9\mu V$

Since the maximum mismatch of the current references is 0.01% of 1mA = 0.1μA

i_O error $= 4\mu A + (0.34\text{Ʊ} \times 34.97) + (0.341 \times 0.0001)$
$\times\ 10.9\mu V = 4\mu A + 11.89\mu A + 0.0004\mu A = 15.89\mu A$

$$\%\ \text{error} = \frac{15.89}{4mA} \times 100\% = 0.4\ \text{at lower range value.}$$

B. At the upper range value (T = 150°C)

$\Delta R = R_{T\ 150°C} - R_4 = 156.4 - 109.4 = 47\Omega$
$\Delta V_{CC} = 24 \times 0.005 + 20mA\ (250\Omega + 100\Omega) + 0.6$
$= 7720mV$
$e_1 = 5.109V$
$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 156.4\Omega) = 5.156V$
$(e_1\ e_2)/2 - 5V \approx 0$
$\Delta R = -R_{T\ 150°C} + R_4 = 156.4 - 109 = 47\Omega$
$\sigma_O = 4\mu A$
$\sigma_I = 25\mu V + (150nA \times 47\Omega + 30nA \times 109\Omega)$

$$+ \frac{7720mV}{3.16 \times 10^5} + \frac{0}{31.6 \times 10^3}$$

$= 25\mu V + 10.33\mu V + 24\mu V\ F0 = 59.33\mu V$
$\sigma_S = 0.0001$
$e_{IN} = e_2' - V_4 = I_{REF1}\,R_{T\ 150°C} - I_{REF2}\,R_4$
$= (1mA \times 156.4\Omega) - (1mA - 109\Omega)$
$= 47mV.$

$i_{O\ ERROR} = \sigma_O + K\,\sigma_I + K\,\sigma_S \times e_{IN}$ (10)
$= 4\mu A + 0.341\text{Ʊ} \times 59.33\mu V + 0.341\text{Ʊ} \times$
$0.0001 \times 47000\mu V$
$= 4 \times 20.23 + 1.6 = 25.83\mu A$

$$\%\ \text{error} = \frac{25.83\mu A}{20mA} \times 100\% = 0.13\%\ \text{at upper}$$

range value or % of FS.

CONCLUSIONS

From equation (9) it is observed that the predominant error term is the input offset voltage (25μV for the B grade). This is of little consequence in many applications. $V_{OS\ RTI}$ can, however, be nulled using the pot shown in Figures 3 and 4. From equation (10), the predominant errors are $I_{OS\ RTI}$ (4μA), $V_{OS\ RTI}$ (25μV), and I_B (150nA), max, B grade.

A NOTE FOR HIGH GAIN APPLICATIONS

In applications where e_{in} full scale is small (<50mV) and R_{span} is small (<≈150Ω), caution should be taken to consider errors from the external span circuit plus high amplification of offset drift and noise.

In such applications, be sure to include the effect of the normal thermal feedback within the XTR100 package. Small additional errors occur from a change in input offset voltage and current due to a change in chip temperature resulting from a change in output current (4mA up to 20mA).

The XTR100 has two thermal resistance specifications:

$\theta_{JA} = 115°C$

This is the thermal resistance from output transistor to ambient. It is used for normal power dissipation considerations (see Figure 18).

$\theta_{JI} = 60°C/W$

This is the thermal resistance which describes the effect of output stage power dissipation in input stage temperature rise.

As an example of how θ_{JI} would be applied, we will calculate the limits with $V_{PS} = 40V$ and $R_L = 250\Omega$.

Power Dissipation:

at 20mA output: 20mA [40V−(20mA × 250Ω)] = 700mW
at 4mA output: 4mA [40V−(4mA × 250Ω)] − 156mW

Thermal Resistance: $\theta_{JI} = 60°C/W$

Input Stage Temperature Rise:

at 20mA output: 700mW × 60°C/W = 42°C
at 4mA output: 156mW × 60°C/W = 9.4°C

Thus under these conditions when the output changes from 4mA to 20mA the input stage temperature changes 42°C − 9.4°C = 32.6°C. The maximum input stage offset change will depend on the particular grade specification:

A Grade (1μV/°C max) = 32.6μV
B Grade (0.5μV/°C max) = 16.3μV

The amount of error that this offset voltage represents depends on how large the full scale input voltage is. It is worse, of course, for small input voltages. Table I shows the error as a percentage of full scale and in terms of output current (% FS error × 16mA FS output span).

TABLE I. Maximum Errors Due to Thermal Feedback
$V_{PS} = 40V$, $R_L = 250\Omega$.

	10mV FS	100mV FS	1V FS
A Grade	0.326% (52.2μA)	0.0326% (5.22μA)	0.0033% (0.522μA)
B Grade	0.163% (26.1μA)	0.0163% (2.61μA)	0.0016% (0.261μA)

HOW TO REDUCE ERRORS

Lower V_{PS}

The errors can be reduced by lowering the voltage at the XTR100 line terminals. The errors in the example above represent a fairly demanding condition of maximum voltage ($V_{PS} = 40V$) and minimum resistance ($R_L = 250\Omega$). If the voltage is lowered to 24V, then a 4mA to 20mA output change causes a change in input stage temperature of 17.3°C and the errors in Table I are reduced by a factor of 17.3°C/32.6°C = 0.53. (Note that this is different than the decrease in the voltage itself: 24/40 = 0.6.)

Raise Resistance

If the load or line resistance is raised the output power dissipation will also be reduced. If $R_L = 400\Omega$ (400/250 = 1.6), the change in output temperature is 29.2°C as the output changes from 4mA to 20mA (still with V_{PS} = 40V) and the errors in Table I are reduced by a factor of 29.2°C/32.6°C = 0.9.

Heat Sink

Heat sinking the package will reduce both θ_{JA} and θ_{JI}. The following is information on small-finned heat sinks that are attached with an epoxy heat sink adhesive (AHAM-985). The three models are 0.75″ × 0.4″ × 0.21″.

Model 141
AHAM
27901 Front St.
Rancho, CA 92390
(714) 676-4151

Models 141 and 142
Heat Sink Plus
28715 Via Montezuma
Temecula, CA 92390
(714) 676-3031

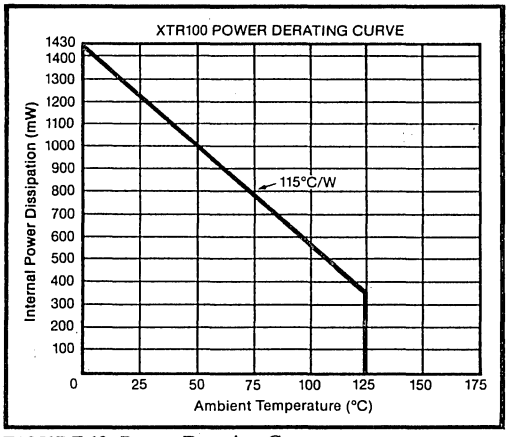


FIGURE 18. Power Derating Curve.

GENERAL RECOMMENDATIONS HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove the static-generating materials, such as untreated plastics, from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% is recommended).

BURR-BROWN®

XTR101

FOR A COMPLETE
DATA SHEET,
SEE PDS-627

Precision, Low Drift 4mA to 20mA TWO-WIRE TRANSMITTER

FEATURES

- INSTRUMENTATION AMPLIFIER INPUT
  - Low Offset Voltage, 30μV max
  - Low Voltage Drift, 0.75μV/°C max
  - Low Nonlinearity, 0.01% max
- TRUE TWO-WIRE OPERATION
  - Power and Signal on One Wire Pair
  - Current Mode Signal Transmission
  - High Noise Immunity
- DUAL MATCHED CURRENT SOURCES
- WIDE SUPPLY RANGE, 11.6V to 40V
- −40°C to +85°C SPECIFICATION RANGE
- SMALL 14-PIN DIP PACKAGE

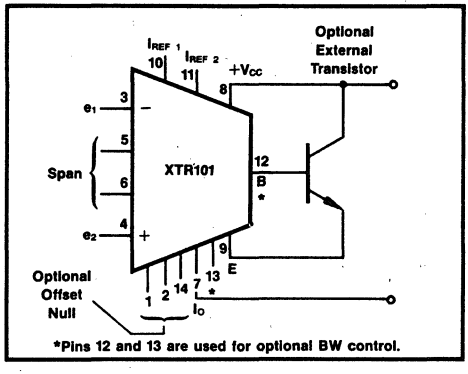
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  - Pressure Transmitters
  - Temperature Transmitters
  - Millivolt Transmitters
- RESISTANCE BRIDGE INPUTS
- THERMOCOUPLE INPUTS
- RTD INPUTS
- CURRENT SHUNT (mV) INPUTS
- PRECISION DUAL CURRENT SOURCES
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR101 is a microcircuit, 4mA to 20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage-controlled output current source, and dual-matched precision current reference. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTDs, thermistors, and strain gauge bridges. State-of-the-art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications. In addition the optional external transistor allows even higher precision.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers. Also, the XTR101 is generally very useful for low-noise, current-mode signal transmission.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, +V_{CC} = 24VDC, R_L = 100Ω with external transistor connected unless otherwise noted.

PARAMETER	CONDITIONS/DESIGNATION	XTR101AG MIN	XTR101AG TYP	XTR101AG MAX	XTR101BG MIN	XTR101BG TYP	XTR101BG MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS								
Current	Linear Operating Region	4		20	•		•	mA
	Derated Performance	3.8		22	•		•	mA
Current Limit			28	38		•	•	mA
Offset Current Error	I_{OS}, I_O = 4mA		±3.9	±10		±2.5	±6	µA
vs Temperature	$\Delta I_{OS}/\Delta T$		±10.5	±20		±8	±15	ppm, FS/°C
Full Scale Output Current Error	Full Scale = 20mA		±20	±40		±15	±30	µA
Power Supply Rejection		110	135		•	•		dB
Power Supply Voltage	V_{CC}, pins 7 and 8, compliance[1]	+11.6		+40	•		•	VDC
Load Resistance	At V_{CC} = +24V, I_O = 20mA			600			•	Ω
	At V_{CC} = +40V, I_O = 20mA			1400			•	Ω
SPAN								
Output Current Equation	R_S in Ω, e_1 and e_2 in V		$i_O = 4mA + [0.016Ω + (40/R_S)](e_2 - e_1)$					
Span Equation	R_S in Ω			$S = [0.016Ω + (40/R_S)]$				A/V
vs Temperature	Excluding TCR of R_S		±30	±100		•	•	ppm/°C
Untrimmed Error[2]	ε_{SPAN}	−5	−2.5	0	•	•	•	%
Nonlinearity	$\varepsilon_{NONLINEARITY}$			0.01			•	%
Hysteresis			0			•		%
Dead Band			0			•		%
INPUT CHARACTERISTICS								
Impedance: Differential			0.4 ‖ 3			•		GΩ ‖ pF
Common-Mode			10 ‖ 3			•		GΩ ‖ pF
Voltage Range, Full Scale	$\Delta e = (e_2 - e_1)$ [3]	0		1	•		•	V
Offset Voltage	V_{OS}		±30	±60		±20	±30	µV
vs Temperature	$\Delta V_{OS}/\Delta T$		±0.75	±1.5		±0.35	±0.75	µV/°C
Bias Current	I_B		60	150		•	•	nA
vs Temperature	$\Delta I_B/\Delta T$		0.30	1		•	•	nA/°C
Offset Current	I_{OSI}		10	±30		•	±20	nA
vs Temperature	$\Delta I_{OSI}/\Delta T$		0.1	0.3		•	•	nA/°C
Common-Mode Rejection[4]	DC	90	100		•	•		dB
Common-Mode Range	e_1 and e_2 with respect to pin 7	4		6	•		•	V
CURRENT SOURCES								
Magnitude			1			•		mA
Accuracy	V_{CC} = 24V, $V_{PIN\ 8} - V_{PIN\ 10,\ 11}$ = 19V, R_2 = 5kΩ, Figure 5		±0.06	±0.17		±0.025	±0.075	%
vs Temperature			±50	±80		±30	±50	ppm/°C
vs V_{CC}			±3			•		ppm/V
vs Time			±8			•		ppm/month
Ratio Match	Tracking							
Accuracy	$1 - I_{REF\ 1}/I_{REF\ 2}$		±0.014	±0.06		±0.009	±0.04	%
vs Temperature				±15			10	ppm/°C
vs V_{CC}			±10			•		ppm/V
vs Time			±1			•		ppm/month
Output Impedance		10	20		•	•		MΩ
TEMPERATURE RANGE								
Specification		−40		+85	•		•	°C
Operating		−55		+125	•		•	°C
Storage		−55		+165	•		•	°C

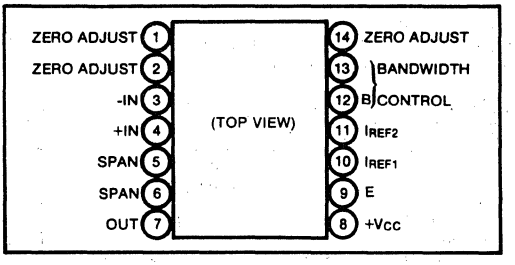
*Same as XTR101AG.

NOTES: (1) See Typical Performance Curves. (2) Span error shown is untrimmed and may be adjusted to zero. (3) e_1 and e_2 are signals on the −IN and +IN terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR101A and XTR101B grades respectively. 2mV FS is also possible with the B grade, but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise. (4) Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed. See Application Information section.

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC}	40V
Input Voltage, e_1 or e_2	$\geq V_{OUT}, \leq +V_{CC}$
Storage Temperature Range, ceramic	−55°C to +165°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration	Continuous $+V_{CC}$ to I_{OUT}
Junction Temperature	+165°C

PIN DESIGNATIONS

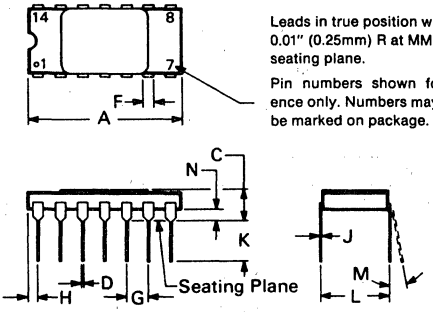


MECHANICAL

G Package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.009	.060	0.23	1.52

Hermetic DIP



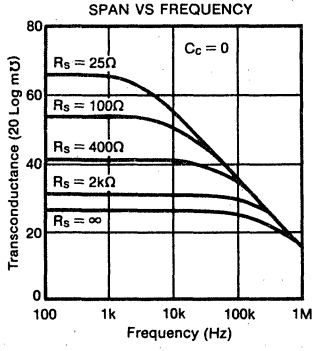
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

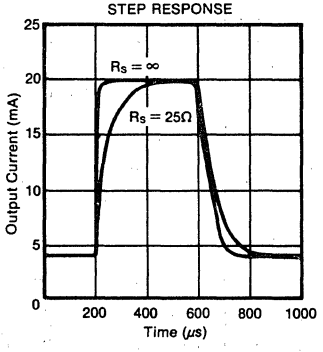
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, $+V_{CC}$ = 24VDC unless otherwise noted)

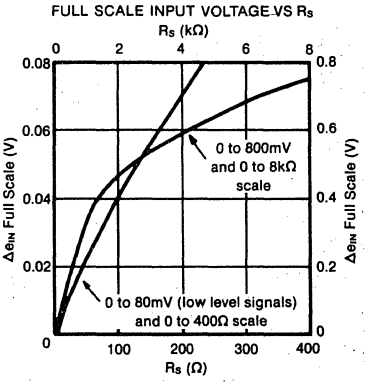
SPAN VS FREQUENCY



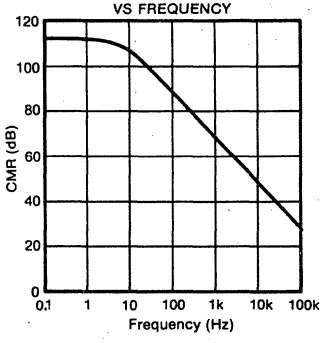
STEP RESPONSE



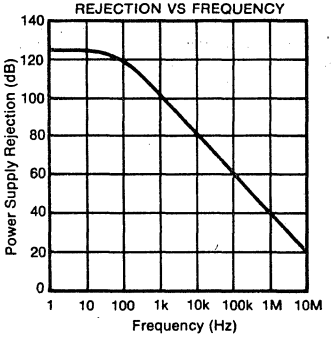
FULL SCALE INPUT VOLTAGE VS R_S



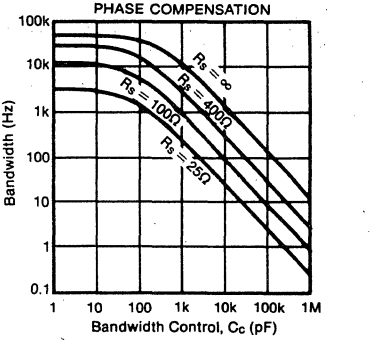
COMMON-MODE REJECTION VS FREQUENCY

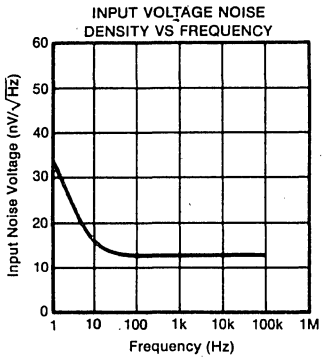


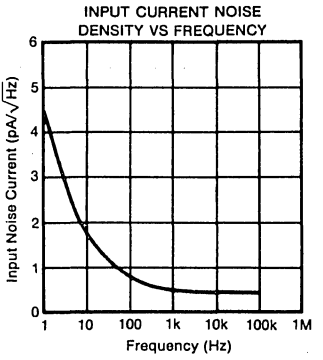
POWER SUPPLY REJECTION VS FREQUENCY

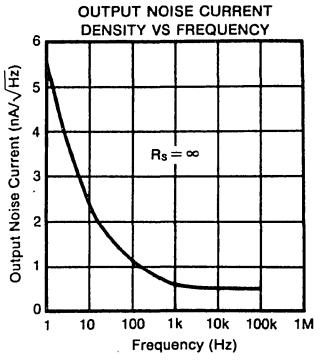


BANDWIDTH VS PHASE COMPENSATION









THEORY OF OPERATION

A simplified schematic of the XTR101 is shown in Figure 1. Basically the amplifiers, A_1 and A_2, act as a single power supply instrumentation amplifier controlling a current source, A_3 and Q_1. Operation is determined by an internal feedback loop. e_1 applied to pin 3 will also appear at pin 5 and similarly e_2 will appear at pin 6. Therefore the current in R_S, the span setting resistor, will be $I_S = (e_2 - e_1)/R_S = e_{IN}/R_S$. This current combines with the current, I_3, to form I_1. The circuit is configured such that I_2 is 19 times I_1. From this point the derivation of the transfer function is straightforward but lengthy. The result is shown in Figure 1.

Examination of the transfer function shows that I_O has a lower range-limit of 4mA when $e_{IN} = e_2 - e_1 = 0V$. This 4mA is composed of 2mA quiescent current exiting pin 7 plus 2mA from the current sources. The upper range limit of I_O is set to 20mA by the proper selection of R_S based on the upper range limit of e_{IN}. Specifically R_S is chosen for a 16mA output current span for the given full scale input voltage span; i.e., $(0.016\text{Ʊ} + 40/R_S)(e_{IN}$ full scale$) = 16mA$. Note that since I_O is unipolar e_2 must be kept larger than e_1; i.e., $e_2 \geq e_1$ or $e_{IN} \geq 0$. Also note that in order not to exceed the output upper range limit of 20mA, e_{IN} must be kept less than 1V when $R_S = \infty$ and proportionately less as R_S is reduced.

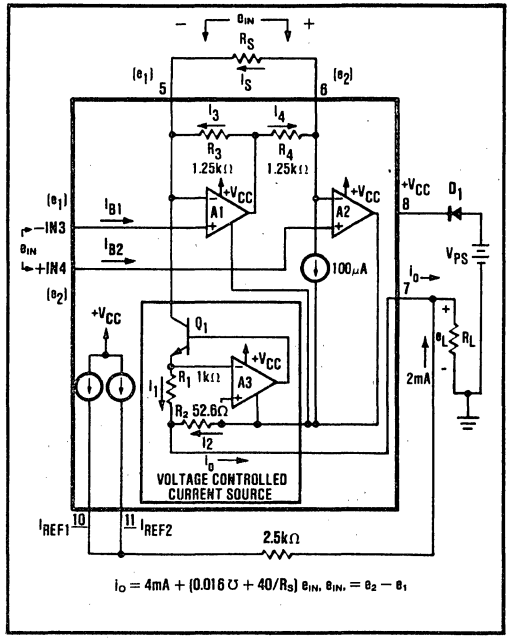


FIGURE 1. Simplified Schematic of the XTR101.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection of the XTR101 is shown in Figure 1. A difference voltage applied between input pins 3 and 4 will cause a current of 4mA to 20mA to circulate in the two-wire output loop (through R_L, V_{PS}, and D_1). For applications requiring moderate accuracy, the XTR101 operates very cost-effectively with just its internal drive transistor. For more demanding applications (high accuracy in high gain) an external NPN transistor can be added in parallel with the internal one. This keeps the heat out of the XTR101 package and minimizes thermal feedback to the input stage. Also in such applications where e_{IN} full scale is small (<50mV) and R_{SPAN} is small (<150Ω), caution should be taken to consider errors from the external span circuit plus high amplification of offset drift and noise.

OPTIONAL EXTERNAL TRANSISTOR

The optional external transistor, when used, is connected in parallel with the XTR101's internal transistor. The purpose is to increase accuracy by reducing heat change inside the XTR101 package as the output current spans from 4mA to 20mA. Under normal operating conditions, the internal transistor is never completely turned off as shown in Figure 2. This maintains frequency stability with varying external transistor characteristics and wiring capacitance. The actual "current sharing" between internal and external transistors is

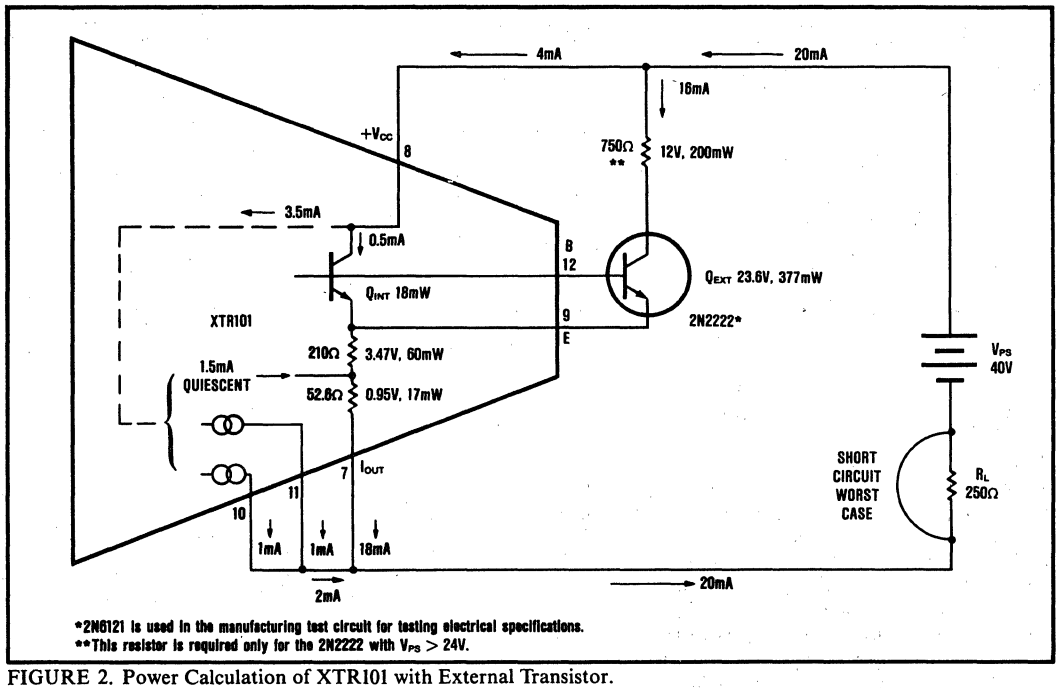


FIGURE 2. Power Calculation of XTR101 with External Transistor.

dependent on two factors: (1) relative geometry of emitter areas and (2) relative package dissipation (case size and thermal conductivity). For best results, the external device should have a larger base emitter area and smaller package. It will, upon turn on, take about [0.95 (I_O − 3.3mA)]mA. However, it will heat faster and take a greater share after a few seconds.

Although any NPN of suitable power rating will operate with the XTR101, two readily available transistors are recommended for accuracy improvement:

1. 2N2222 in the TO-18 package. For power supply voltages above 24V, a 750Ω, 1/2W resistor should be connected in series with the collector. This will limit the power dissipation to 377mW under the worst-case conditions shown in Figure 2. Thus the 2N2222 will safely operate below its 400mW rating at the upper temperature of +85°C. Heat sinking the 2N2222 will result in greatly reduced accuracy improvement and is not recommended.
2. 2N6121 in the TO-220 package. This transistor will operate over the specified temperature and output voltage range without a series collector resistor. Heat sinking the 2N6121 will result in slightly less accuracy improvement. It can be done, however, when mechanical constraints require it.

ACCURACY WITH AND WITHOUT EXTERNAL TRANSISTOR

The XTR101 has been tested in a circuit using a 2N6121 external transistor. The relative difference in accuracy with and without an external transistor is shown in Figure 3. Notice that a dramatic improvement in offset voltage change with supply voltage is evident for any value of load resistor.

MAJOR POINTS TO CONSIDER WHEN USING THE XTR101

1. The leads to R_S should be kept as short as possible to reduce noise pick-up and parasitic resistance.
2. $+V_{CC}$ should be bypassed with a 0.01μF capacitor as close to the unit as possible (pin 8 to 7).
3. Always keep the input voltages within their range of linear operation, +4V to +6V (e_1 and e_2 measured with respect to pin 7).
4. The maximum input signal level ($e_{IN_{FS}}$) is 1V with $R_S = \infty$ and proportionally less as R_S decreases.
5. Always return the current references (pins 10 and 11) to the output (pin 7) through an appropriate resistor. If the references are not used for biasing or excitation, connect them together to pin 7. Each reference must have between 0V and $+(V_{CC} - 4V)$ with respect to pin 7.
6. Always choose R_L (including line resistance) so that the voltage between pins 7 and 8 ($+V_{CC}$) remains within the 11.6V to 40V range as the output changes between the 4mA to 20mA range (see Figure 4).
7. It is recommended that a reverse polarity protection diode (D_1 in Figure 1) be used. This will prevent damage to the XTR101 caused by a momentary (e.g., tran-

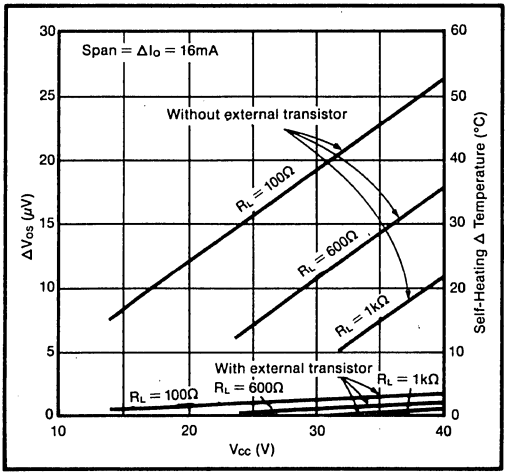


FIGURE 3. Thermal Feedback Due to Change in Output Current.

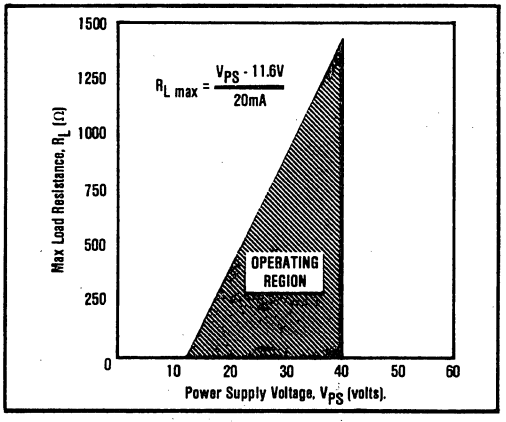


FIGURE 4. Power Supply Operating Range.

sient) or long term application of the wrong polarity of voltage between pins 7 and 8.

8. Consider PC board layout which minimizes parasitic capacitance, especially in high gain.

SELECTING R_S

R_{SPAN} is chosen so that a given full scale input span $e_{IN_{FS}}$ will result in the desired full scale output span of ΔI_{OFS},

$$[(0.016\mho) + (40/R_S)]\,\Delta e_{IN} = \Delta I_O = 16\text{mA}.$$

Solving for R_S:

$$R_S = \frac{40}{\Delta I_O/\Delta e_{IN} - 0.016\mho} \qquad (1)$$

For example, if $\Delta e_{IN_{FS}} = 100\text{mV}$ for $\Delta I_{O_{FS}} = 16\text{mA}$,

$$R_S = \frac{40}{(16\text{mA}/100\text{mV}) - 0.016} = \frac{40}{0.16 - 0.016} = \frac{40}{0.144}$$
$$= 278\Omega$$

See Typical Performance Curves for a plot of R_S vs $\Delta e_{IN_{FS}}$. Note that in order not to exceed the 20mA upper range limit, e_{IN} must be less than 1V when $R_S = \infty$ and proportionately smaller as R_S decreases.

BIASING THE INPUTS

Because the XTR operates from a single supply both e_1 and e_2 must be biased approximately 5V above the voltage at pin 7 to assure linear response. This is easily done by using one or both current sources and an external resistor R_2. Figure 5 shows the simplest case—a floating voltage source e'_2. The 2mA from the current sources flows through the 2.5kΩ value of R_2 and both e_1 and e_2 are raised by the required 5V with respect to pin 7. For linear operation the constraint is

$$+4\text{V} \le e_1 \le +6\text{V}$$
$$+4\text{V} \le e_2 \le +6\text{V}$$

Figure 6 shows a similar connection for a resistive transducer. The transducer could be excited either by one (as shown) or both current sources.

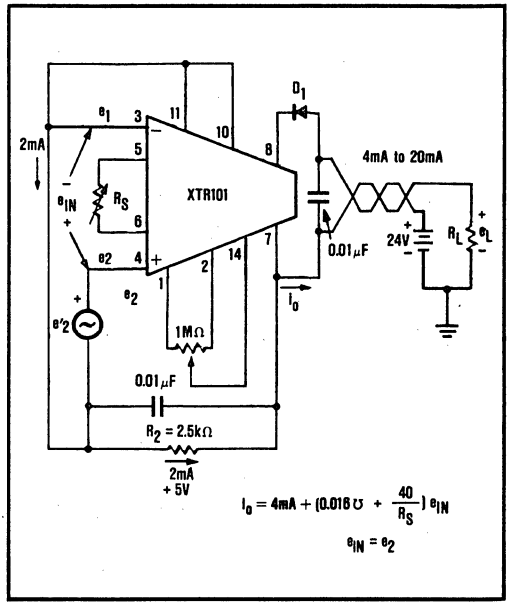


FIGURE 5. Basic Connection for Floating Voltage Source.

CMV AND CMR

The XTR101 is designed to operate with a nominal 5V common-mode voltage at the input and will function properly with either input operating over the range of 4V to 6V with respect to pin 7. The error caused by the 5V CMV is already included in the accuracy specifications. If the inputs are biased at some other CMV then an input offset error term is (CMV − 5)/CMRR; CMR is in dB, CMRR is in V/V.

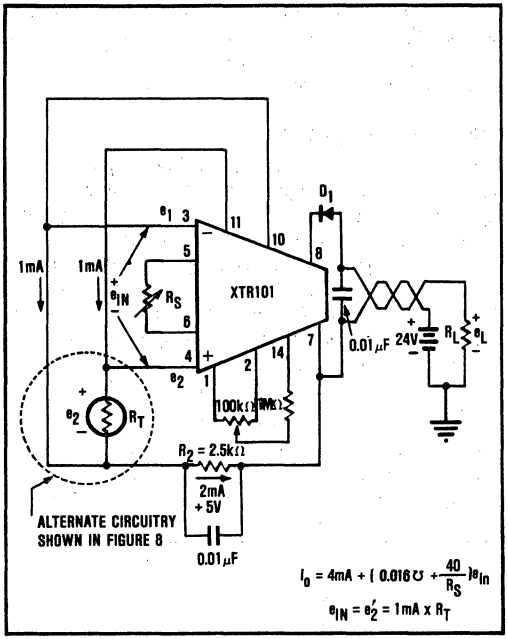


FIGURE 6. Basic Connection for Resistive Source.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (input signal elevation) or elevated zero range (input signal suppression). This is easily accomplished with the XTR101 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figures 7 and 8 (a). In this example the sensor voltage is derived from R_T (a thermistor, RTD or other variable resistance element) excited by one of the 1mA current sources. The other current source is used to create the elevated zero range voltage. Figures 8 (b), (c) and (d) show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments. Note: It is not recommended to use the optional offset voltage null (pins 1, 2, and 14) for elevation/suppression. This trim capability is used only to null the amplifier's input offset voltage. In many applications the already low offset voltage (typically 20μV) will not need to be nulled at all. Adjusting the offset voltage to nonzero values will disturb the voltage drift by ±0.3μV/°C per 100μV of induced offset.

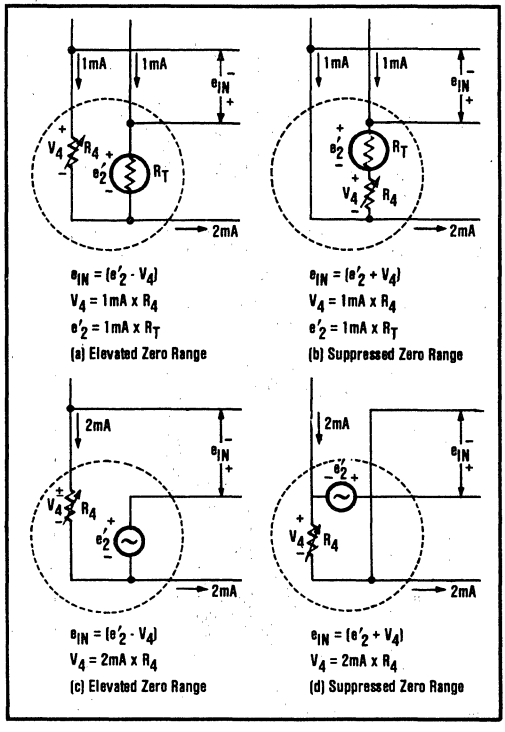


FIGURE 8. Elevation and Suppression Circuits.

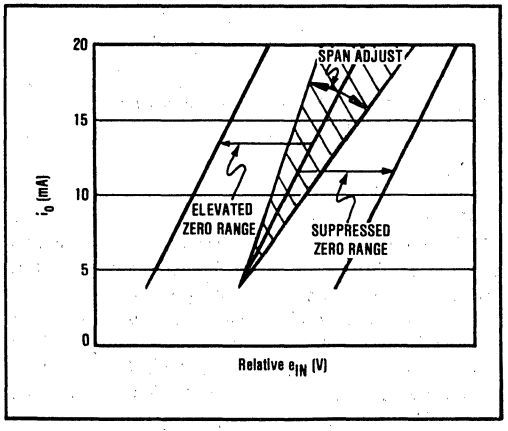


FIGURE 7. Elevation and Suppression Graph.

APPLICATION INFORMATION

The small size, low offset voltage and drift, excellent linearity, and internal precision current sources, make the XTR101 ideal for a variety of two-wire transmitter applications. It can be used by OEMs producing different types of transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus the XTR101 is, in general, very suitable for individualized and special purpose applications.

EXAMPLE 1

RTD Transducer shown in Figure 9.

Given a process with temperature limits of +25°C and +150°C, configure the XTR101 to measure the tempera-

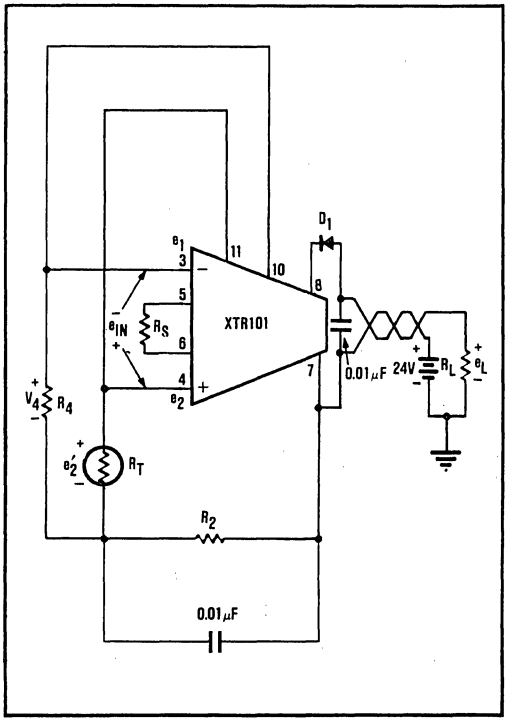


FIGURE 9. Circuit for Example 1.

ture with a platinum RTD which produces 100Ω at 0°C and 200Ω at +266°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C.

COMPUTING R_S:

The sensitivity of the RTD is $\Delta R/\Delta T = 100\Omega/266°C$. When excited with a 1mA current source for a 25°C to 150°C range (i.e., 125°C span), the span of e_{IN} is 1mA × (100Ω/266°C) × 125°C = 47mV = Δe_{IN}.

$$\text{From equation 1, } R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{IN}} - 0.016\mho}$$

$$R_S = \frac{40}{\frac{16mA}{47mV} - 0.016\mho} = \frac{40}{0.3244} = 123.3\Omega$$

Span adjustment (calibration) is accomplished by trimming R_S.

COMPUTING R_4:

$$\text{At } +25°C,\ e_2' = 1mA\ (R_T + \Delta R_T)$$
$$= 1mA\ [100\Omega + (\frac{100\Omega}{266°C} \times 25°C)]$$
$$= 1mA\ (109.4\Omega)$$
$$= 109.4mV$$

In order to make the lower range limit of 25°C correspond to the output lower range limit of 4mA, the input circuitry shown in Figure 9 is used.

e_{IN}, the XTR101 differential input, is made 0 at 25°C

$$\text{or } e_{2\,25°C}' - V_4 = 0$$
$$\text{thus, } V_4 = e_{2\,25°C}' = 109.4mV$$
$$R_4 = \frac{V_4}{1mA} = \frac{109.4mV}{1mA} = 109.4\Omega$$

COMPUTING R_2 AND CHECKING CMV:

At +25°C, $e_2' = 109.4mV$

At +150°C, $e_2' = 1mA\ (R_T + \Omega R_T)$

$$= 1mA\ [100\Omega + (\frac{100\Omega}{266°C} \times 150°C)]$$
$$= 156.4mV$$

Since both e_2' and V_4 are small relative to the desired 5V common-mode voltage, they may be ignored in computing R_2 as long as the CMV is met.

$$R_2 = 5V/2mA = 2.5k\Omega$$
$$\left.\begin{aligned} e_2\ \text{min} &= 5V + 0.1094V \\ e_2\ \text{max} &= 5V + 0.1564V \\ e_1 &= 5V + 0.1094V \end{aligned}\right\} \text{ The +4V to +6V CMV requirement is met.}$$

EXAMPLE 2

Thermocouple Transducer shown in Figure 10.

Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the XTR101 to measure the temperature with a type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, V_{R6}, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At a typical ambient of +25°C this is 1.28mV (obtained from standard thermocouple tables with reference junction of 0°C). Transmit 4mA for T_1 = 0°C and 20mA for T_1 = +1000°C. Note: $e_{IN} = e_2 - e_1$ indicates that T_1 is relative to T_2.

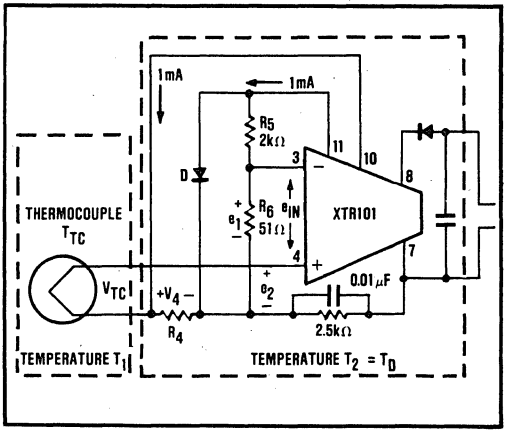


FIGURE 10. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

ESTABLISHING R_S:

The input full scale span is 58mV ($\Delta e_{IN_{FS}} = 58mV$).

R_S is found from equation (1)

$$R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{IN}} - 0.016\mho}$$

$$= \frac{40}{\frac{16mA}{58mV} - 0.016\mho} = \frac{40}{0.2599} = 153.9\Omega$$

SELECTING R_4:

R_4 is chosen to make the output 4mA at $T_{TC} = 0°C$ ($V_{TC} = -1.28mV$) and $T_D = +25°C$ ($V_D = 0.6V$). A circuit is shown in Figure 10.

V_{TC} will be $-1.28mV$ when $T_{TC} = 0°C$ and the reference junction is at $+25°C$. e_1 must be computed for the condition of $T_D = +25°C$ to make $e_{IN} = 0V$.

$$V_{D_{25°C}} = 600mV$$
$$e_{1_{25°C}} = 600mV\ (51/2051) = 14.9mV$$
$$e_{IN} = e_2 - e_1 = V_{TC} + V_4 - e_1$$

With $e_{IN} = 0$ and $V_{TC} + -1.28mV$,

$$V_4 = e'_1 + e_{IN} - V_{TC}$$
$$= 14.9mV + 0V - (-1.28mV)$$
$$1mA\ (R_4) = 16.18mV$$
$$R_4 = 16.18\Omega$$

COLD JUNCTION COMPENSATION:

The temperature reference circuit is shown in Figure 11.

The diode voltage has the form

$$V_D = \frac{KT}{q} \ln \frac{I_{DIODE}}{I_{SAT}}$$

Typically at $T_2 = +25°C$, $V_D = 0.6V$ and $\Delta V_D/\Delta T = -2mV/°C$. R_5 and R_6 form a voltage divider for the diode voltage V_D. The divider values are selected so that the gradient $\Delta V_D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At $+25°C$ this is approximately $52\mu V/°C$ (obtained from standard thermocouple table); therefore,

$$\Delta V_{TC}/\Delta T = \Delta V_D/\Delta T \left(\frac{R_6}{R_5 + R_6}\right) \quad (2)$$

$$52\mu V/°C = 200\mu V/°C \left(\frac{R_6}{R_5 + R_6}\right)$$

R_5 is chosen as $2k\Omega$ to be much larger than the resistance of the diode. Solving for R_6 yields 51Ω.

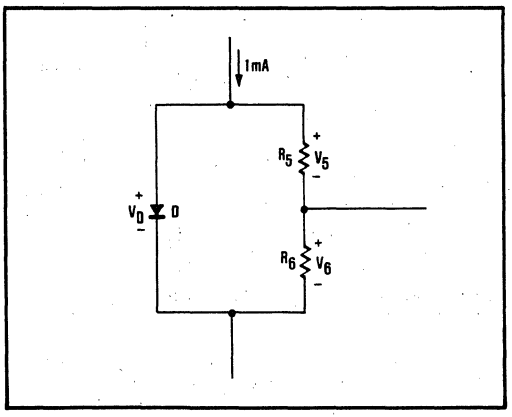


FIGURE 11. Cold Junction Compensation Circuit.

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to either limit when the thermocouple impedance goes very high. The circuits of Figures 16 and 17 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the + input (large impedance) will cause I_O to go to its lower range limit value (about 3.8mA). If up scale indication is desired the circuit of Figure 18 should be used. When the TC opens the output will go to its upper range limit value (about 25mA or higher).

OPTIONAL INPUT OFFSET VOLTAGE TRIM

The XTR101 has provisions for nulling the input offset voltage associated with the input amplifiers. In many applications the already low offset voltages ($30\mu V$ max for the B grade, $60\mu V$ max for the A grade) will not need to be nulled at all. The null adjustment can be done with a potentiometer at pins 1, 2, and 14 as shown in Figures 5 and 6. Either of these two circuits may be used. NOTE: It is not recommended to use this input offset voltage nulling capability for elevation or suppression. See the Signal Suppression and Elevation section for the proper techniques.

OPTIONAL BANDWIDTH CONTROL

Low-pass filtering is recommended where possible and can be done by either one of two techniques shown in Figure 12. C_2 connected to pins 3 and 4 will reduce the bandwidth with a cutoff frequency given by,

$$f_{CO} = \frac{15.9}{(R_1 + R_2 + R_3 + R_4)\ (C_2 + 3pF)}$$

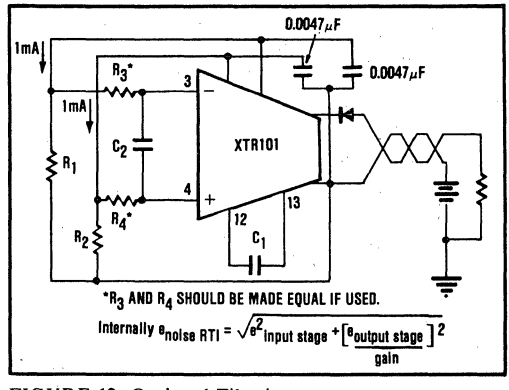


FIGURE 12. Optional Filtering.

This method has the disadvantage of having f_{CO} vary with R_1, R_2, R_3, R_4, and it may require large values of R_3 and R_4. The other method, using C_1, will use smaller values of capacitance and is not a function of the input resistors. It is, however, more subject to nonlinear distortion caused by slew rate limiting. This is normally not a problem with the slow signals associated with most process control transducers. The relationship between C_1 and f_{CO} is shown in the Typical Performance Curves.

APPLICATION CIRCUITS

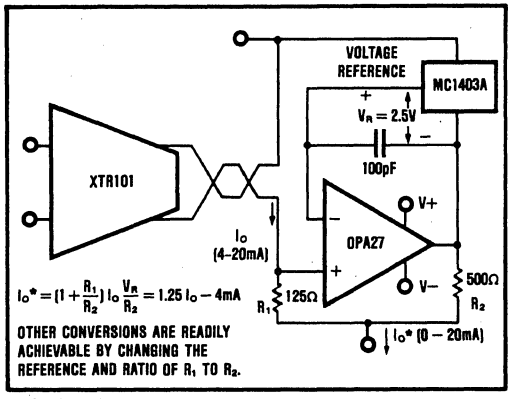


FIGURE 13. 0mA to 20mA Output Converter.

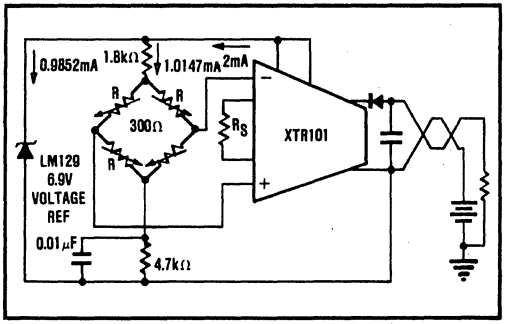


FIGURE 14. Bridge Input, Voltage Excitation.

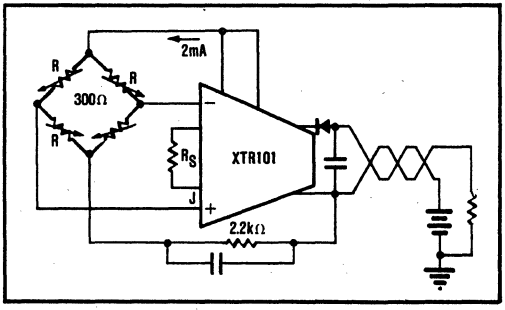


FIGURE 15. Bridge Input, Current Excitation.

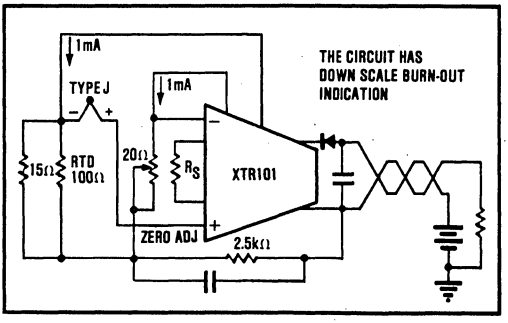


FIGURE 16. Thermocouple Input with RTD Cold Junction Compensation.

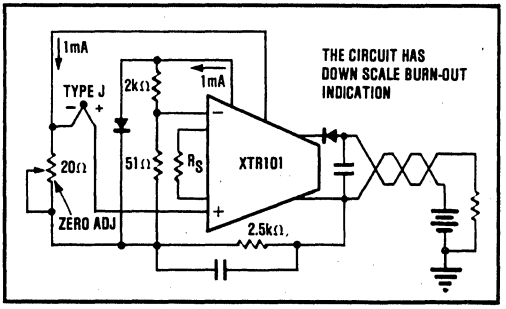


FIGURE 17. Thermocouple Input with Diode Cold Junction Compensation.

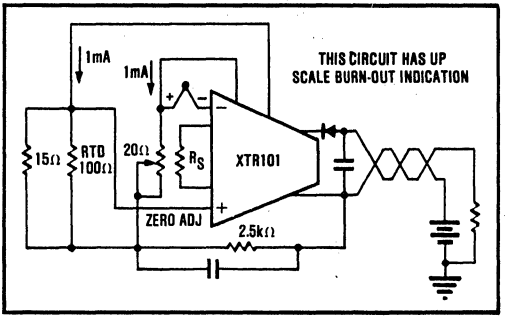


FIGURE 18. Thermocouple Input with RTD Cold Junction Compensation.

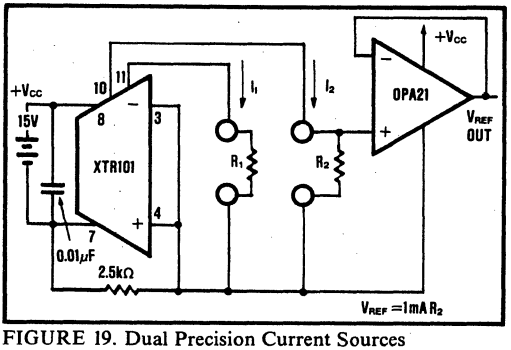


FIGURE 19. Dual Precision Current Sources Operated From One Supply.

BURR-BROWN®

XTR110

PRECISION VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER

FEATURES

- 4mA TO 20mA TRANSMITTER
- SELECTABLE INPUT/OUTPUT RANGES:
  0V to +5V, 0V to +10V Inputs
  0mA to 20mA, 5mA to 25mA Outputs
  Other Ranges
- 0.005% MAX NONLINEARITY, 14 BIT
- PRECISION +10V REFERENCE OUTPUT
- SINGLE SUPPLY OPERATION
- CURRENT SOURCING TO COMMON
- WIDE SUPPLY RANGE, 13.5V TO 40V

APPLICATIONS

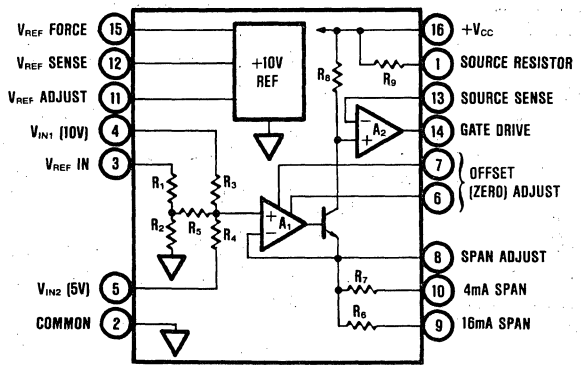
- INDUSTRIAL PROCESS CONTROL
- PRESSURE/TEMPERATURE TRANSMITTERS
- CURRENT-MODE BRIDGE EXCITATION
- GROUNDED TRANSDUCER CIRCUITS
- CURRENT SOURCE REFERENCE FOR DATA ACQUISITION
- PROGRAMMABLE CURRENT SOURCE FOR TEST EQUIPMENT
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR110 is a monolithic precision voltage-to-current converter. It can convert standard 0V to +10V or 0V to +5V inputs into 4mA to 20mA, or 5mA to 25mA outputs. The required external MOS transistor keeps heat outside the XTR110 package to optimize performance under all output conditions.

A precision +10V reference output can drive 10mA. An external transistor can be added for more current, e.g. 33mA for 300Ω bridges.

The XTR110 is a key data acquisition component, designed for high noise immunity current-mode transmission. It is also ideal as a precision programmable current source for transducer circuits and test equipment.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{CC} = +24V and R_L = 250Ω† unless otherwise specified.

PARAMETER	CONDITIONS	XTR110AG/XTR110KP MIN	XTR110AG/XTR110KP TYP	XTR110AG/XTR110KP MAX	XTR110BG MIN	XTR110BG TYP	XTR110BG MAX	UNITS
TRANSMITTER								
Transfer Function			$I_O = 10\ [(V_{REF}IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}$					
Input Range: V_{IN1}	Specified performance	0		+10	*		*	V
V_{IN2}	Specified performance	0		+5	*		*	V
Current, I_O	Specified performance[1]	4		20	*		*	mA
	Derated performance[1]	0		40	*		*	mA
Nonlinearity	16mA/20mA span[2]		0.01	0.025		0.002	0.005	% of span
Offset Current, I_{OS}	I_O = 4mA[1]							
Initial	[1]		0.2	0.4		0.02	0.1	% of span
vs Temp	[1]		0.0003	0.005		*	0.003	% of span/°C
vs Supply, V_{CC}	[1]		0.0005	0.005		*	*	% of span/V
Span Error	I_O = 20mA							
Initial	[1]		0.3	0.6		0.05	0.2	% of span
vs Temp	[1]		0.0025	0.005		0.0009	0.003	% of span/°C
vs Supply, V_{CC}	[1]		0.003	0.005		*	*	% of span/V
Output Resistance	From drain of FET (Q_{EXT})[3]		$10 \times 10^{[9]}$			*		Ω
Input Resistance	V_{IN1}		27			*		kΩ
	V_{IN2}		22			*		kΩ
	V_{REF} IN		19			*		kΩ
Dynamic Response								
Settling Time	To 0.1% of span		15			*		µsec
	To 0.01% of span		20			*		µsec
Slew Rate			1.3			*		mA/µsec
VOLTAGE REFERENCE								
Output Voltage		+9.95	+10	+10.05	+9.98	*	+10.02	V
vs Temp			35	50		15	30	ppm/°C
vs Supply, V_{CC}	Line regulation		0.0002	0.005		*	*	%/V
vs Output Current	Load regulation		0.0005	0.01		*	*	%/mA
vs Time			100			*		ppm/1k hrs
Trim Range		−0.100		+0.25	*		*	V
Output Current	Specified performance	10			*			mA
POWER SUPPLY								
Input Voltage, V_{CC}		+13.5		+40	*		*	V
Quiescent Current	Excluding I_O		3	4.5		*	*	mA
TEMPERATURE RANGE								
Specification: AG, BG		−40		+85	*		*	°C
KP		0		+70				°C
Operating: AG, BG		−55		+125	*		*	°C
KP		−25		+85				°C

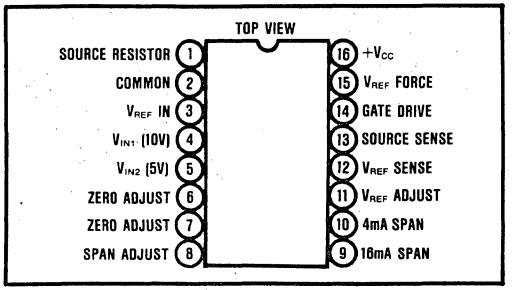
* Specification same as AG/KP grades. † Specifications apply to the range of R_L shown in Typical Performance Curves.

NOTES: (1) Including internal reference. (2) Span is the change in output current resulting from a full-scale change in input voltage. (3) Within compliance range limited by ($+V_{CC}$ − 2V) $+V_{DS}$ required for linear operation of the FET. (4) For V_{REF} adjustment circuit see Figure 4. (5) For extended I_{REF} drive circuit see Figure 8.

ABSOLUTE MAXIMUM RATINGS

Power Supply, $+V_{CC}$ 40V
Input Voltage, $V_{IN\ 1}$, $V_{IN\ 2}$, $V_{REF\ IN}$ ..... $+V_{CC}$
Storage Temperature Range: A, B ..... −55°C to +125°C
K ..... −40°C to +85°C
Lead Temperature (soldering, 10sec) ..... 300°C
Output Short Circuit Duration, Gate Drive and V_{REF} Force ..... Continuous to common and $+V_{CC}$
Output Current Using Internal 50Ω Resistor 40mA

PIN CONFIGURATION



ORDERING INFORMATION

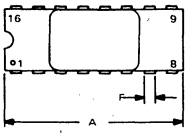
XTR110 X G

Basic model number

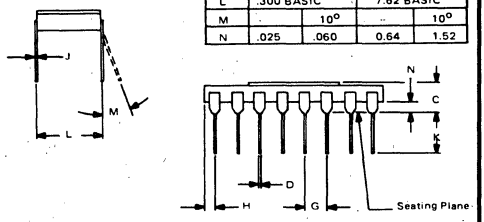
Performance grade code
A, B: −40°C to +85°C
K: 0°C to +70°C

Package code
G: 16-pin hermetic DIP
P: 16-pin plastic DIP

MECHANICAL



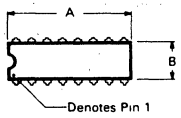
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52



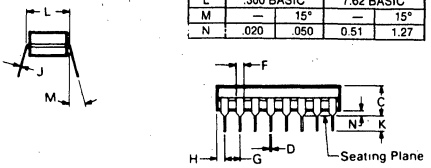
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

PLASTIC DUAL-IN-LINE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.760	.885	19.30	22.48
B	.220	.280	5.59	7.11
C	0.12	.200	0.12	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	.76	2.41
J	.008	.015	0.20	0.38
K	.100	—	2.54	—
L	.300 BASIC		7.62 BASIC	
M	—	15°	—	15°
N	.020	.050	0.51	1.27

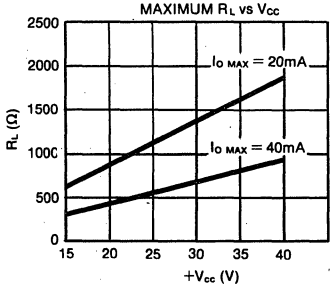


NOTE:
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

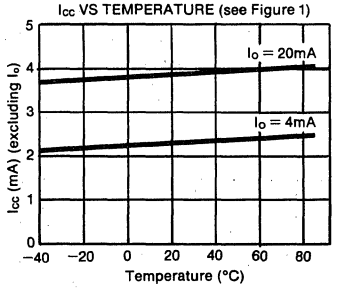
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = 24VDC, R_L = 250Ω unless otherwise noted.

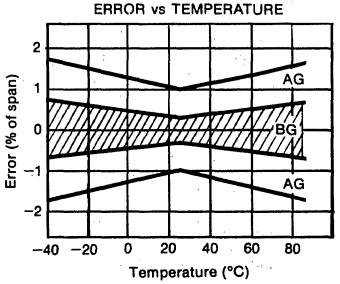
MAXIMUM R_L vs V_{CC}



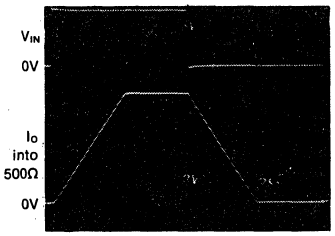
I_{CC} VS TEMPERATURE (see Figure 1)



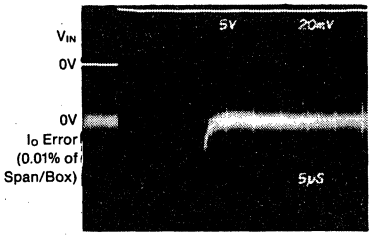
TOTAL OUTPUT ERROR vs TEMPERATURE



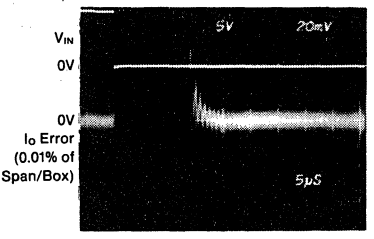
PULSE RESPONSE



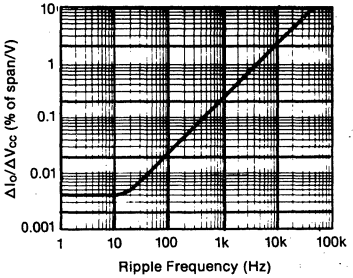
SETTLING TIME WITH POS V_{IN} STEP



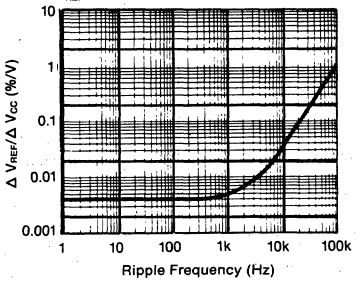
SETTLING TIME WITH NEG V_{IN} STEP



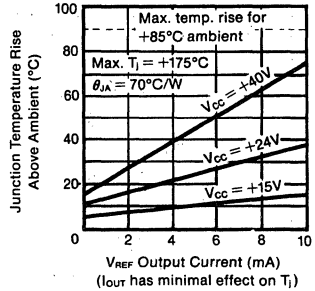
I_O POWER SUPPLY REJECTION vs FREQUENCY



V_{REF} LINE REGULATION vs FREQUENCY



JUNCTION TEMPERATURE RISE vs V_{REF} OUTPUT CURRENT



THEORY OF OPERATION

The XTR110 is designed to convert a high level input voltage into a positive output current.

A block diagram of the XTR110 is shown in Figure 1. The circuit contains four main functional blocks: (1) a precision resistor divider network (R_1–R_5), (2) a voltage-to-current converter (A_1, Q_1, R_6, R_7), (3) a current-to-current converter (A_2, R_8, R_9, Q_{EXT}), and (4) a precision +10V reference.

The precision divider network sums three input voltages to the noninverting input of A_1. These are V_{IN1} (10V full scale), V_{IN2} (5V full scale), and V_{REF} IN (for offsetting).

In the voltage-to-current converter, the op amp, A_1, forces its input voltage across the span setting resistors, R_6 and R_7. Since Q_1 is a high gain Darlington, base current error is negligible and all current flows to the current-to-current converter (into R_8). The transfer function including input divider is as follows:

$$I_{R8} = [(V_{REF}\ IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}$$

where R_{SPAN} is the resistance from Q_1 emitter to common.

The current-to-current converter is the output section of the XTR110 transmitter. The voltage across the 500Ω resistor (R_8) is forced across the 50Ω resistor (R_9) by A_2 and the external MOSFET (Q_{EXT}). Since no current flows in the gate of the MOSFET, all current is delivered to the output. This current (I_{OUT}) is ten times the internal current through R_8. Use of the external transistor keeps power out of the precision IC to maintain accuracy.

The overall transfer function for the XTR110 transmitter is:

$$I_O = 10[(V_{REF}\ IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}.$$

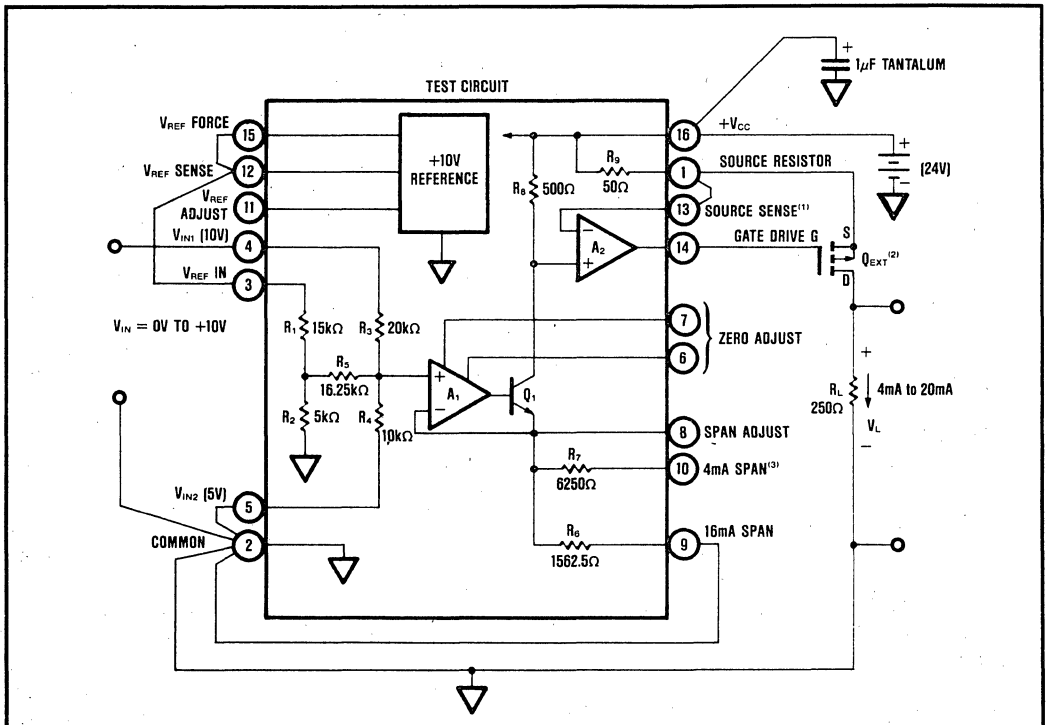
For output currents beyond 40mA an external resistor can be used in place of R_9.

The +10V reference provides input offsetting, e.g. 4mA offset for the 4ma to 20mA output configuration. The reference can deliver 10mA and is protected from shorts to common. Higher current can be provided for other applications by using an external NPN transistor connected to the sense and force pins.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection of the XTR110 is the standard 0V to +10V input; 4mA to 20mA output configuration is shown in Figure 1.



NOTES: (1) To maintain accuracy, make a separate direct connection between pins 1 and 13. (2) Q_{EXT} is any P-channel enhancement-mode power MOSFET with appropriate voltage and power rating. PNP bipolar transistors can be used with slight degradation in end-point accuracy and linearity. For recommended devices see section on external transistor. (3) For 20mA span, strap 4mA and 16mA pins together to common.

FIGURE 1. Block Diagram of the XTR110 in Basic Connection: 0V to +10V in, 4mA to 20mA out.

$+V_{CC}$ may originate at the XTR110 site or may be brought in as part of a three-wire twisted line. Be sure to use sufficient bypassing close to the XTR110 on the $+V_{CC}$ line.

EXTERNAL TRANSISTOR

Connections to the MOSFET are gate drive (pin 14) and source resistor (pin 1). To eliminate errors due to resistance in the connection between pin 1 and the source of the external transistor, connect pin 13 directly to pin 1 as shown in Figure 1.

The output of A2, pin 14, is intended to drive a MOSFET or PNP external pass transistor, and for that reason, is atypical of op amp outputs. The output stage can be visualized as a 300μA current source in parallel with an NPN collector. The NPN is the active element that, through feedback, determines where the gate drive should be set. It is capable of sinking over 15mA.

External MOSFET

The XTR110 can operate with a variety of output transistors having appropriate breakdown voltage and power rating which is influenced by package type. Some general observations on package thermal characteristics are listed in Table I.

TABLE I. External Transistor Package Type and Dissipation.

Package Type	Allowable Power Dissipation
TO-92	Lowest: Use minimum supply and at +25°C.
TO-237	Acceptable: Trade-off supply and temperature.
TO-39	Good: Adequate for majority of designs.
TO-220	Excellent: For prolonged maximum stress.
TO-3	Overkill: If nothing else is available.

Maximum power dissipation of the external transistor can be derived from the derating curve. It can also be calculated from the thermal characteristics using the equation below:

$$P_A = P_D - (T_A - 25)/\theta_{JA}$$

P_A = Power to be dissipated at T_A
T_A = Maximum ambient temperature
P_D = Maximum continuous power dissipation at +25°C ($I_D V_{DS}$)
θ_{JA} = Junction to ambient thermal resistance

(Refer to the manufacturer's data sheet for required numbers.)

Table II shows suitable MOSFET output transistors.

Summary of points to consider for selecting the transistor are:

1. Power rating—Equal to 1.5 × P_A if possible, or at least equal to P_A.
2. Drain-source breakdown—Greater than maximum expected V_{DS}. This includes any additional voltage that may exist between the transmitter and receiver grounds.
3. Gate-source breakdown—Greater than $+V_{CC}$, because V_{CC} will be applied gate-to-source, under the condition of an open drain line (V_{GATE} then = 0V). Most MOSFETS will tolerate only 20V, but a zener (12V or more) connected gate-to-source will clamp the junction and remain off during normal operation.

TABLE II. Available P-Channel MOSFETs.

Manufacturer	Part No.	BV_{DSS}*	BV_{GS}*	Package
Ferranti	ZVP1304A	−40V	20V	TO-92
	ZVP1304B	−40V	20V	TO-39
	ZVP1306A	−60V	20V	TO-92
	ZVP1306B	−60V	20V	TO-39
International Rectifier	IRF9513	−60V	20V	TO-220
Motorola	MTP8P08	−80V	20V	TO-220
RCA	RFL1P08	−80V	20V	TO-39
	RFT2P08	−80V	20V	TO-220
Siliconix (preferred)	VP0300B	−30V	40V	TO-39
	VP0300L	−30V	40V	TO-92
	VP0300M	−30V	40V	TO-237
	VP0808B	−80V	40V	TO-39
	VP0808L	−80V	40V	TO-92
	VP0808M	−80V	40V	TO-237
Supertex	VP1304N2	−40V	20V	TO-220
	VP1304N3	−40V	20V	TO-92
	VP1306N2	−60V	20V	TO-220
	VP1306N3	−60V	20V	TO-92

*BV_{DSS}—Drain-source breakdown voltage. BV_{GS}—Gate-source breakdown voltage.

External PNP Transistor

A PNP bipolar transistor can also be used for the output but it will result in a slight drop in end-point accuracy and linearity. A TN2905 in a TO-237 package performs adequately. The end point shifts can be calculated if the beta of the PNP is known. The offset shift is I_{OS}/beta and the span shift is I_{SPAN}/beta. For example, if the transistor's beta is 250 and the output range is 4mA to 20mA, the calculations are as follows:

$dI_{OS} = 4mA/250 = 16\mu A$ (0.1% of span)
$dI_{SPAN} = 16mA/250 = 64\mu A$ (0.4% of span)

The offset error can be corrected by using the offset correction circuitry of Figure 5. The span error due to base current loss can be compensated by connecting an external resistor, R_{PAD}, in parallel with the internal resistor as shown in Figure 2. R_{PAD} can be calculated with the following formula:

$$R_{PAD} = 50 \text{ (beta + 1)}$$

Any span error due to the XTR110 itself can be corrected with the span adjust circuitry of Figure 5. Use a nominal beta to calculate the value of R_{PAD} if individual transistor measurements are not made. There should be enough range in the span adjust circuit to compensate for normal tolerances.

Small nonlinearity degradation (0.01% typical at $24V_{CC}$) results from changes in beta caused by changes in power as collector current varies from 4mA to 20mA. A heat sink can be added to minimize the heat dissipation effect.

A Darlington configuration (two separate PNPs) can also be used with no degradation in end-point accuracy and linearity. A 0.047μF capacitor across pins 13 and 14 is required for stability as shown in Figure 3. Single-

packaged Darlingtons with internal bleeder resistors are not recommended since they will severly degrade accuracy.

To select a bipolar transistor, follow the same points as for MOSFETs. Note, however, the base-emitter breakdown is not considered because this junction is forward biased should the collector open.

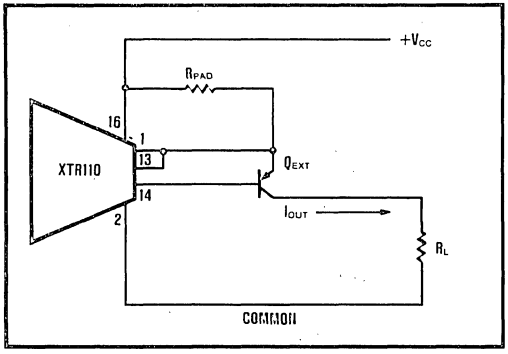


FIGURE 2. PNP Output Transistor (R_{PAD} corrects for span error caused by beta).

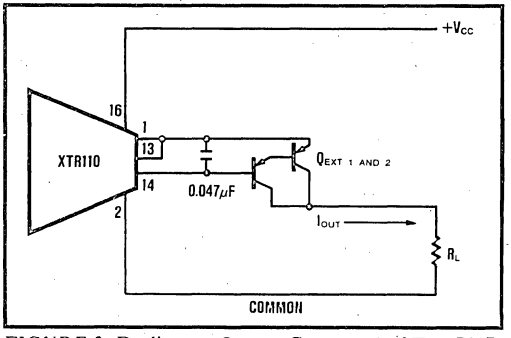


FIGURE 3. Darlington Output Composed of Two PNP Transistors.

COMMONS

Careful attention should be directed toward proper connection of the commons. All commons should be joined at one point as close to pin 2 of the XTR110 as possible. The exception is the I_{OUT} return. It can be returned to any place where it will not modulate the common at pin 2.

VOLTAGE REFERENCE

The reference voltage is accurately regulated at pin 12 (V_{REF} sense). To preserve accuracy, any load including pin 3 should be connected to this point.

The circuit in Figure 4 shows coarse and fine adjustment of the voltage reference.

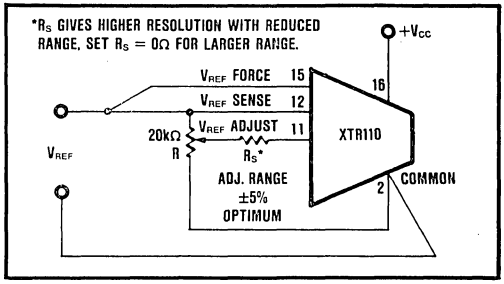


FIGURE 4. Optional Adjustment of Reference Voltage.

OFFSET (ZERO) ADJUSTMENT

The offset current can be adjusted by using the potentiometer, R_1, shown in Figure 5. The procedure is to set the input voltage to zero and then adjust R_1 to give 4mA at the output. For spans starting at 0mA, the following special procedure is recommended: set the input to a small nonzero value and then adjust R_1 to the proper output current. When the input is zero the output will be zero. Figures 6 and 7 show graphically how offset is adjusted.

SPAN ADJUSTMENT

The span is adjusted at the full-scale output current using the potentiometer, R_2, shown in Figure 5. This adjustment is interactive with the offset adjustment, and a few iterations may be necessary. For the circuit shown, set the input voltage to +10V full scale and then adjust R_2 to give 20mA full-scale output. Figures 6 and 7 show graphically how span is adjusted.

The values of R_2, R_3, and R_4 for adjusting the span are determined as follows: choose R_4 in series to slightly decrease the span; then choose R_2 and R_3 to increase the span to be adjustable about the center value.

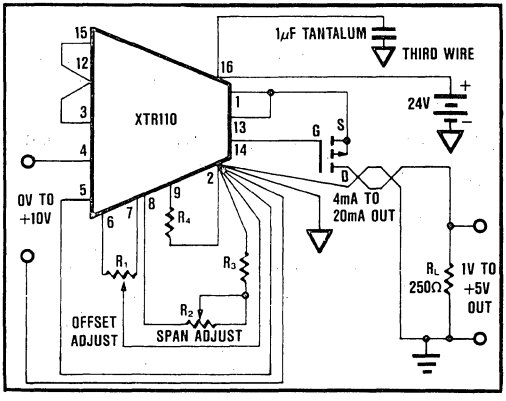


FIGURE 5. Offset and Span Adjustment Circuit for 0V to +10V Input, 4mA to 20mA Output.

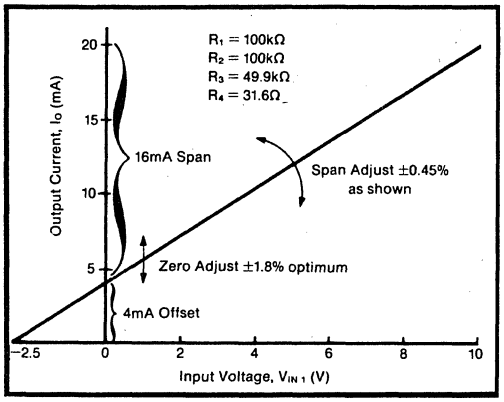


FIGURE 6. Zero and Span of 0V to +10V Input, 4mA to 20mA Output Configuration (see Figure 5).

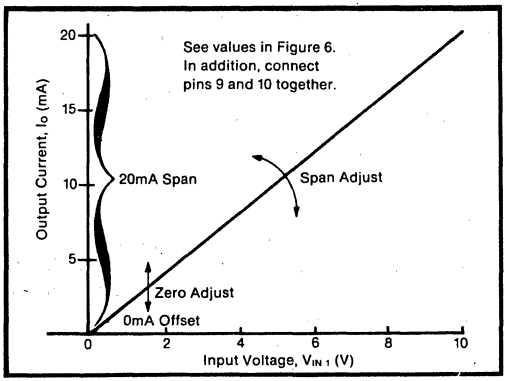


FIGURE 7. Zero and Span of 0V to +10V_{IN}, 0mA to 20mA Output Configuration (see Figure 5).

ERROR CALCULATIONS

Errors can be calculated by considering these key parameters:

1. Offset Current (Initial, vs Temperature, vs Supply)
2. Span Error (Initial, vs Temperature, vs Supply)
3. Nonlinearity

Lower errors can readily be obtained by externally adjusting the initial offset and span errors to zero (see Performance Curves).

EXTENDED REFERENCE CURRENT DRIVE

The current drive capability of the XTR110's internal reference is 10mA. This can be extended if desired by adding an external NPN transistor shown in Figure 8.

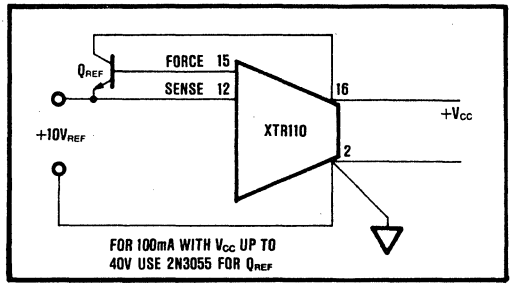


FIGURE 8. Extended Reference Current Drive.

LOW TEMPERATURE COEFFICIENT (TC) OPERATION

Although the precision resistors in the XTR110 track within 1ppm/°C, the output current depends upon the absolute temperature coefficient of any one of the resistors, R_6, R_7, R_8, and R_9. Since the absolute TC of the resistors is 20ppm/°C, maximum, the TC of the output current can have 20ppm/°C drift. For low TC operation, zero TC resistors can be substituted for either the span resistors (R_6 or R_7) or for the source resistor (R_9) but not both.

EXTENDED SPAN

For spans beyond 40mA, the internal 50Ω resistor (R_9) may be replaced by an external resistor connected between pins 13 and 16.

Its value can be calculated as follows:

$$R_{EXT} = R_9\ (Span_{OLD}/Span_{NEW})$$

Since the internal thin-film resistors have a 20% absolute value tolerance, measure R_9 before determining the final value of R_{EXT}. Self-heating of R_{EXT} can cause nonlinearity. Therefore, choose one with a low TC and adequate power rating. See Figure 14 for application.

STANDARD CURRENT RANGES OR SPANS

Table III shows the pin connections for standard XTR110 current ranges.

TABLE III. Pin Connections for Standard Ranges.

Input Range (V)	Output Range (mA)	Pin 3	Pin 4	Pin 5	Pin 9	Pin 10
0 - 10	0 - 20	Com	Input	Com	Com	Com
2 - 10	4 - 20	Com	Input	Com	Com	Com
0 - 10	4 - 20	+10V Ref	Input	Com	Com	Open
0 - 10	5 - 25	+10V Ref	Input	Com	Com	Com
0 - 5	0 - 20	Com	Com	Input	Com	Com
1 - 5	4 - 20	Com	Com	Input	Com	Com
0 - 5	4 - 20	+10V Ref	Com	Input	Com	Open
0 - 5	5 - 25	+10V Ref	Com	Input	Com	Com

TYPICAL APPLICATIONS

The XTR110 is ideal for a variety of applications requiring high noise immunity current-mode signal transmission. The precision +10V reference is convenient and can be exciting for bridges and transducers. Selectable ranges make it very useful as a precision programmable current source. The compact design and low price of the XTR110 allow versatility with a minimum of external components and design engineering expense.

Figures 9 through 16 show typical applications of the XTR110.

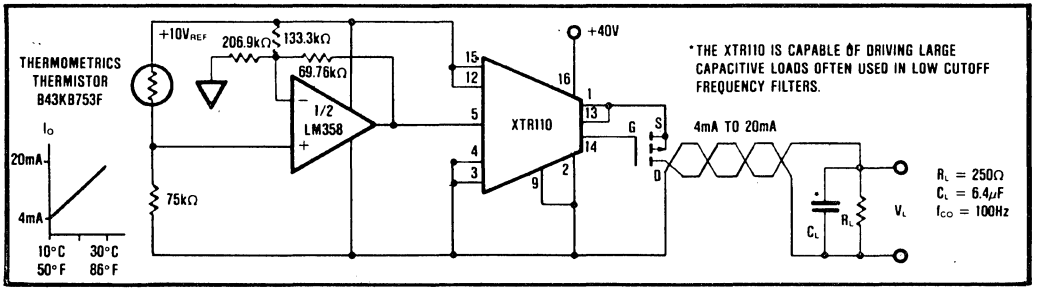


FIGURE 9. 4mA to 20mA Single-Supply Thermistor Transmitter for Energy Management Systems.

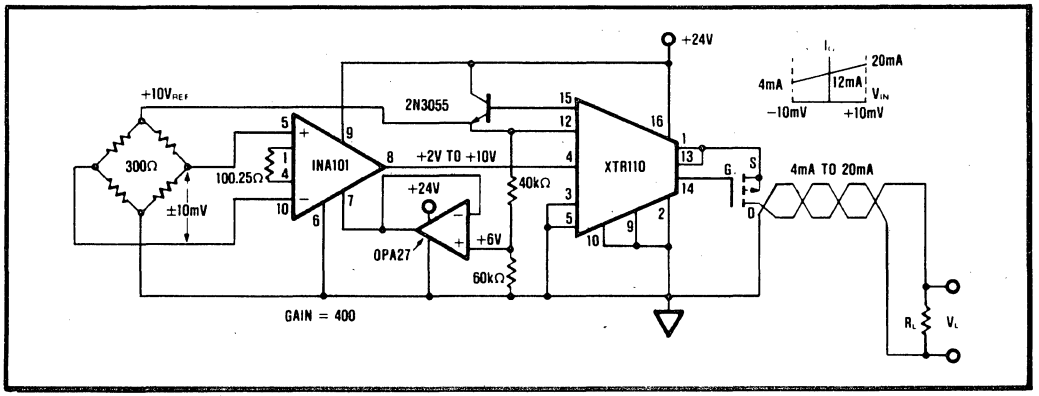


FIGURE 10. 4mA to 20mA Single-Supply Bridge Transmitter.

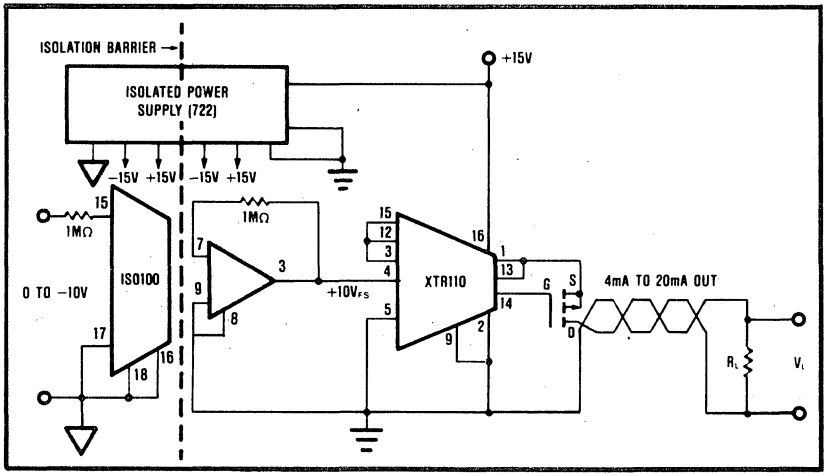


FIGURE 11. Isolated 4mA to 20mA Channel

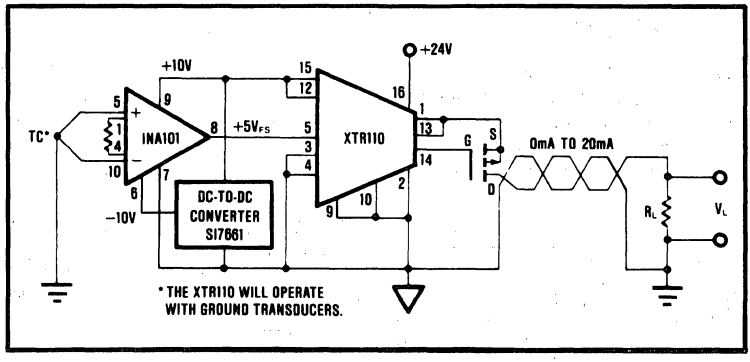


FIGURE 12. 0mA to 20mA Single-Supply Thermocouple Transmitter.

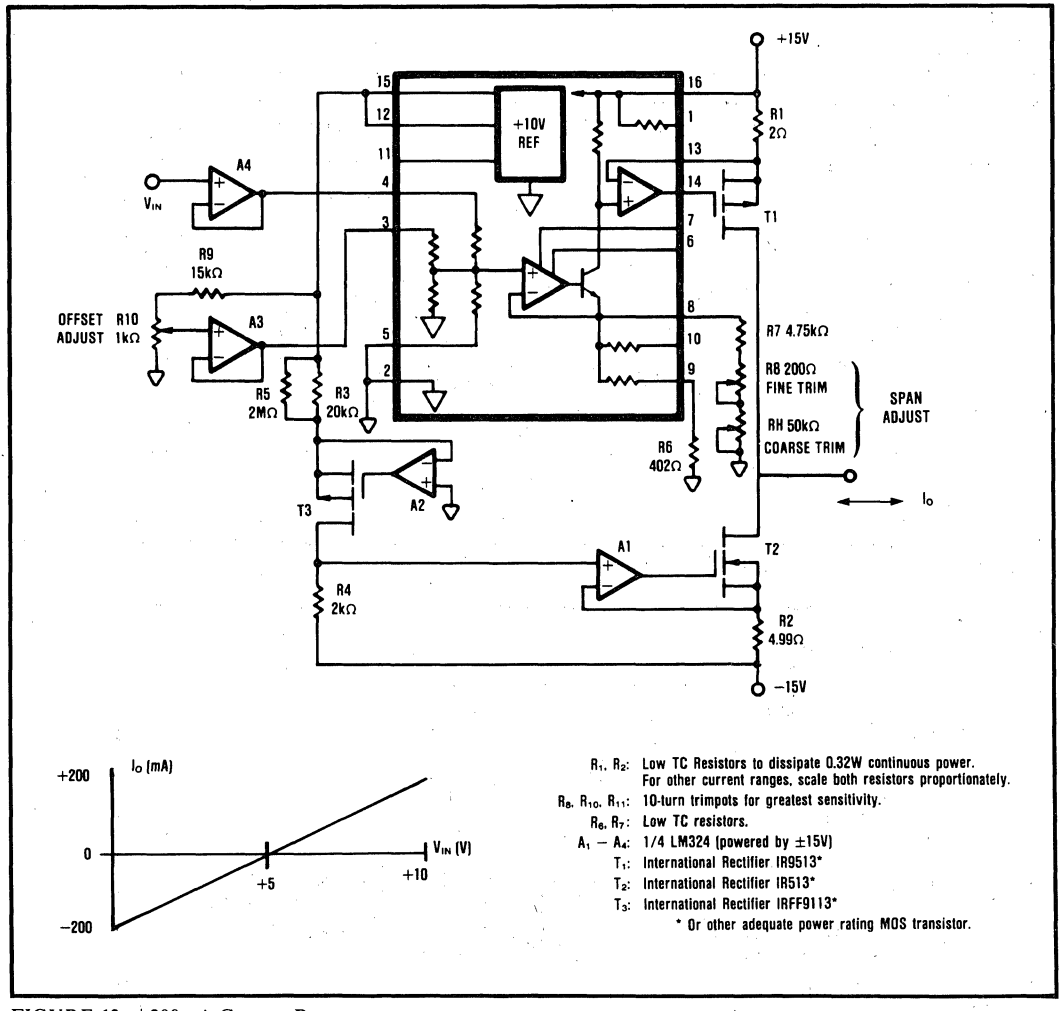


FIGURE 13. ±200mA Current Pump.

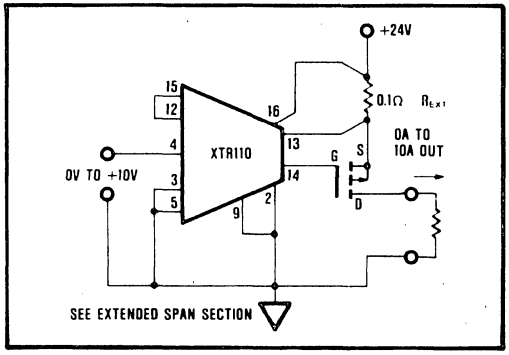


FIGURE 14. 0A to 10A High Current Voltage-to-Current Converter.

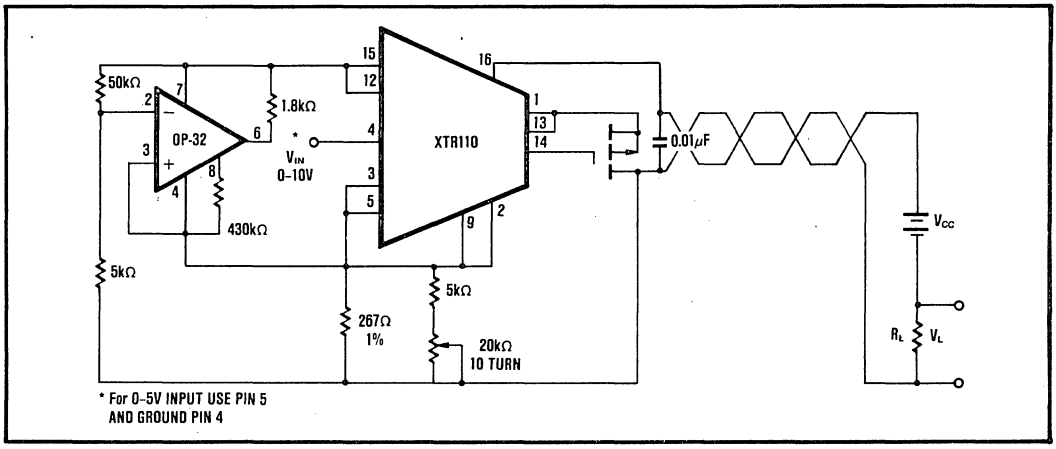


FIGURE 15. High Level Input 4ma to 20mA Two-Wire Transmitter.

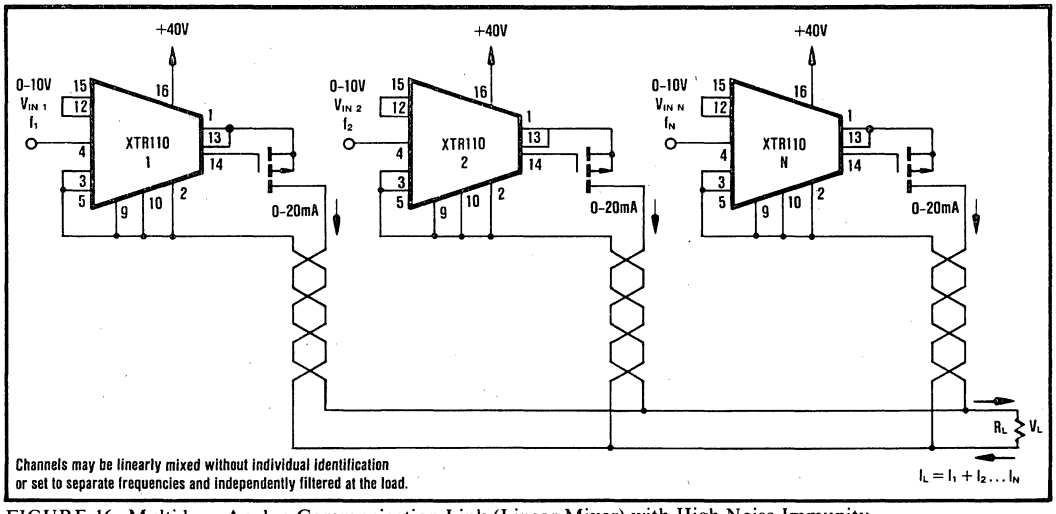


FIGURE 16. Multidrop Analog Communication Link (Linear Mixer) with High Noise Immunity.

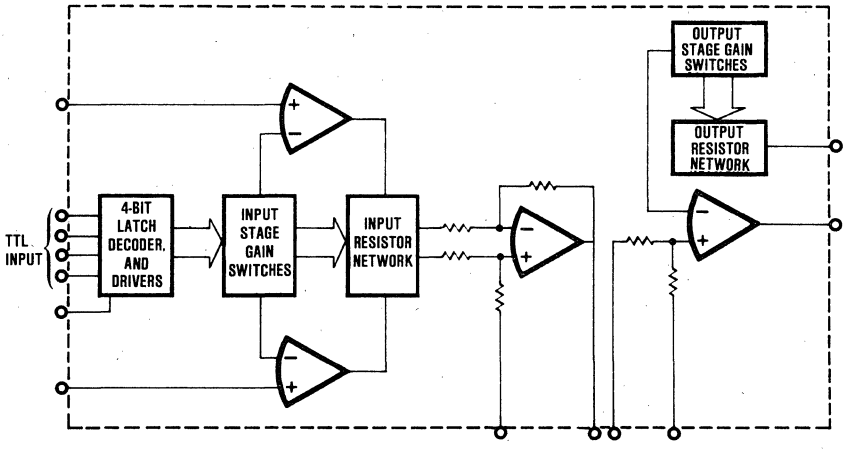
BURR-BROWN®

3606

Digitally Controlled Programmable Gain INSTRUMENTATION AMPLIFIER

FEATURES

- 11 BINARY GAINS - 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024V/V
- 4-BIT TTL GAIN CONTROL
- EXCELLENT GAIN NONLINEARITY 0.01% max at G = 1024V/V
- LOW GAIN ERRORS - 0.02% max
- LOW GAIN DRIFT - 10ppm/°C max
- LOW VOLTAGE DRIFT 1μV/°C max RTI, G = 1024V/V
- HIGH CMR - 110dB min, G = 1024V/V
- HIGH INPUT IMPEDANCE - 10 x $10^9\Omega$
- LOW OFFSET VOLTAGE 22μV max RTI, G = 1024V/V 2mV max RTI, G = 1V/V



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DESCRIPTION

The 3606 is a self-contained, Programmable Gain Instrumentation Amplifier (PGIA) whose gain can be changed in 11 binary weighted steps from 1 to 1024V/V. The gain control is accomplished through a 4-bit TTL input.

The PGIA function allows the user to deal with wide dynamic range signals while maintaining high system resolution. For example: when used with a 10-bit A to D converter in a "floating point" system, the 2^{10} gain range of the 3606, plus the 2^{10} range of the converter produces a total system resolution of 2^{20} (|| 1,000,000:1).

Desirable characteristics of a high performance instrumentation amplifier are offered by the 3606: high input impedance (10GΩ), excellent gain nonlinearity (0.01% max, G = 1024V/V; 0.02% max, G = 1V/V), high common-mode rejection (100dB min, G≥ 4V/V), low gain error (0.02% max with no trimming required), low gain temperature coefficient (10ppm/°C max), and low offset voltage drift vs temperature (1μV/°C max, RTI, G = 1024).

Added to these outstanding instrumentation amplifier characteristics is the ability to change 3606's gain under control of a 4-bit TTL input word. An important characteristic of the 3606 PGIA is its low change in offset plus laser trimming minimized this change to a maximum of ±25mV with no external adjustments. With two simple offset adjustments the change can be limited to less than 2mV (1mV typ) at the output over the entire 1V/V to 1024V/V gain range.

A simplified schematic of the 3606 is shown in Figure 1. The circuit consists of a variable gain high input impedance voltage follower input stage (A1 and A2) followed by a unity gain difference amplifier (A3) with a variable gain output stage (A4).

Common-mode voltage is derived for active guard drive to improve system common-mode rejection. Two-pole, low-pass filtering can easily be implemented on the output stage to reduce noise bandwidth and improve system signal-to-noise operation. A latch function is provided to inhibit gain changes while the digital gain control input is changed.

Burr-Brown's instrumentation grade monolithic operational amplifiers, high stability precision thin-film resistor networks and advanced laser-trimming techniques are used by the 3606 to achieve a performance, size and cost combination never before achieved in a PGIA. It is available in a 32-pin dual-in-line package in either ceramic or metal (hermetic) configurations.

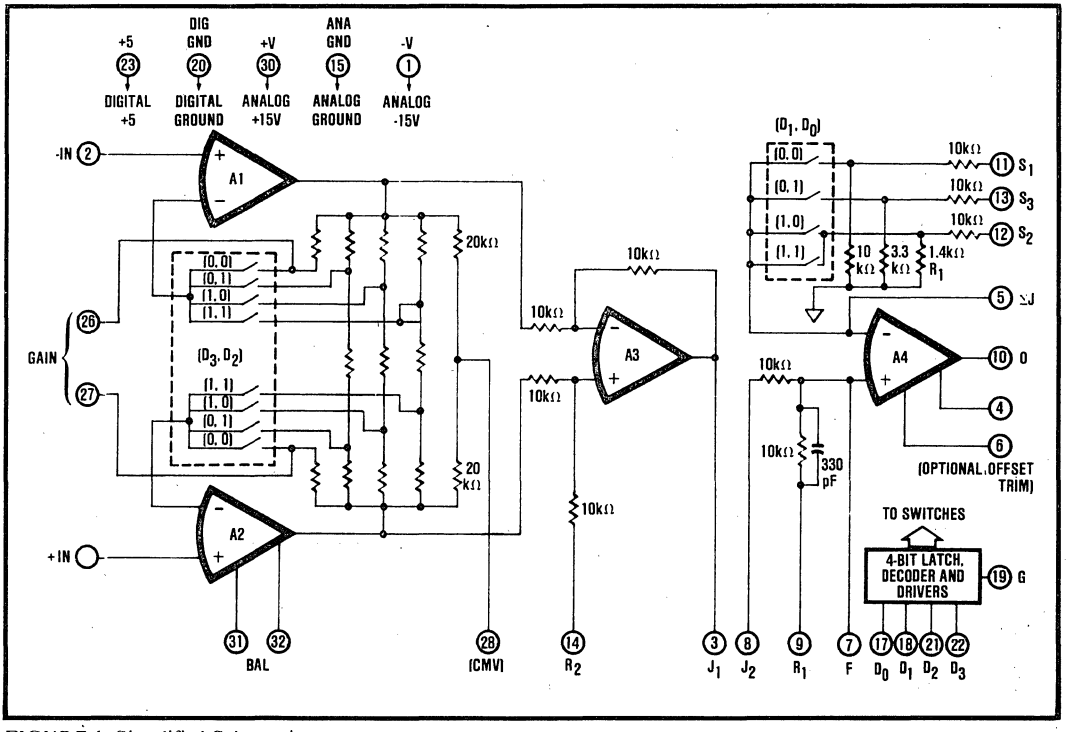


FIGURE 1. Simplified Schematic.

SPECIFICATIONS

ELECTRICAL

Typical at +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	3606A[1] MIN	3606A[1] TYP	3606A[1] MAX	3606B[1] MIN	3606B[1] TYP	3606B[1] MAX	UNITS
GAIN, G[2]								
Inaccuracy	G = 1 to 1024, I_O = 1mA		±0.02	±0.05		±0.01	±0.02	%
Nonlinearity[3]	G = 1 to 16		0.001	0.002		*	*	%(5)
	G = 32 to 128		0.003	0.004		*	*	%
	G = 256 to 1024		0.005	0.01		*	*	%
Drift vs Temperature	G = 1 to 1024		±5	±10		*	*	ppm/°C
vs Time	G = 1 to 1024		±0.01					%/1000 hrs
RATED OUTPUT								
Voltage	I_O = ±5mA	±10	±12		*	*		V
Current	V_O = ±10V	±5	±10		*	*		mA
Impedance			0.05			*		Ω
INPUT CHARACTERISTICS								
Absolute Max Voltage	No damage			±V_{CC}			*	V
Common-Mode Voltage Range	Linear operation	±10	±10.5		*	*		V
Differential Impedance			10 || 3			*		10^9Ω || pF
Common-Mode Impedance			10 || 3			*		10^9Ω || pF
OFFSET VOLTAGE, RTO[4]								
Initial at +25°C[5]			±(0.02G +1)	±(0.04G +2)		±(0.01G +1)	±(0.02G +2)	mV
vs Temperature	-25°C to +85°C		(±0.0015G ±0.03G_2)	(±0.003G ±0.05G_2)		(±0.0005G ±0.01G_2)	(±0.001G ±0.02G_2)	mV/°C
vs Time			(±0.001G ±0.01G_2)			*		mV/mo
vs Supply			(±0.002G ±0.04G_2)			*		mV/V
vs Gain[6]	With trimming		±1	±2		*	*	mV
INPUT BIAS CURRENT								
Initial	+25°C		±15	±50		±5	±20	nA
vs Temperature	-25°C to +85°C		±0.3			*		nA/°C
vs Supply Voltage			±0.1			*		nA/V
INPUT DIFFERENCE CURRENT								
Initial	+25°C		±15	±50		±5	±20	nA
vs Temperature	−25°C to +85°C		±0.5			*		nA/°C
vs Supply Voltage			±0.1			*		nA/V
INPUT NOISE								
Voltage	R_{SOURCE} ≤ 5kΩ							
0.01Hz to 10Hz	G = 1024		1.4			*		μV, p-p
10Hz to 1kHz			1.0			*		μV, rms
Current								
0.01Hz to 10Hz			70			*		pA, p-p
10Hz to 1kHz			20			*		pA, rms
COMMON-MODE REJECTION								
DC, 1kΩ Source Imbalance								
G = 1, 2		80	90		90	100		dB
G = 4 to 6		90	100		100	110		dB
G = 32 to 1024		100	114		110	114		dB
60Hz, 1kΩ Source Imbalance								
G = 1, 2		80	86		*	*		dB
G = 4 to 16		90	96		*	*		dB
G = 32 to 1024		100	106		*	*		dB
DYNAMIC RESPONSE								
±3dB Response	Small Signal							kHz
G = 1			100			*		kHz
G = 32 to 128			40			*		kHz
G = 256 to 1024			10			*		kHz
±1% Response	Small Signal							
G = 1			40			*		kHz
G = 32 to 128			8			*		kHz
G = 256 to 1024			3			*		kHz
Slew Rate	G = 1	0.2	0.5		*	*		V/μsec
Settling Time	G = 128							
to 1%			75			*		μsec
to 0.1%			100			*		μsec
to 0.01%			200			*		μsec

ELECTRICAL (CONT)

Typical at +25°C, unless otherwise noted.

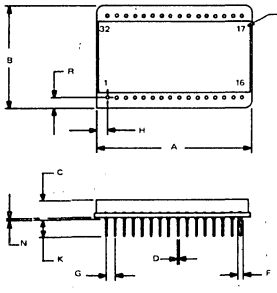
PARAMETER	CONDITIONS	3606A[1] MIN	3606A[1] TYP	3606A[1] MAX	3606B[1] MIN	3606B[1] TYP	3606B[1] MAX	UNITS
LOGIC VOLTAGES								
"0" Level[7]			0	+0.4		*	*	V
"1" Level[7]		+2.4	+5.0		*	*		V
Absolute Max	No damage			+7			*	V
ANALOG SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range, Derated Performance		±8		±18	*		*	VDC
Current, quiescent			±10	±20		*	*	mA
DIGITAL SUPPLY								
Rated Voltage			+5			*		VDC
Voltage Range		+4.5		+5.5	*		*	VDC
Current, quiescent			10			*		mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Storage		-40		+100	*		*	°C

*Specifications same as 3606A.

NOTES:
1. Specify 3606AG or 3606BG for ceramic package and 3606AM or 3606BM for metal package—see below.
2. $G = G_1 \times G_2$.
3. Nonlinearity is the maximum peak deviation from the best straight-line as a percent of full scale peak-to-peak output.
4. RTO = Referred To Output. May be referred to input by dividing by gain G.
5. May be adjusted to zero.
6. Trimmed according to Figure 8.
7. All digital inputs are 1 TTL unit load.

MECHANICAL

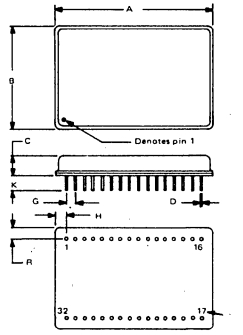
"G" PACKAGE



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

NOTE:
LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.

"M" PACKAGE



NOTE
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

Pin numbers shown for reference only. Numbers may not be marked on package.

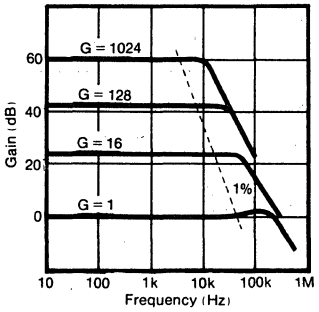
PIN DESIGNATIONS

PIN NO.	DESIG.	FUNCTION	PIN NO.	DESIG.	FUNCTION
1	-V	-15V Analog Supply	17	D_0	Digital Input, LSB
2	-IN	Inverting Input	18	D_1	Digital Input, next LSB
3	J_1	Output of A_3	19	G	Latch
4	(None)	Optional A_4 Offset Trim	20	DIG GND	Digital Ground
5	ΣJ	Summing Junction of A_4	21	D_2	Digital Input, next MSB
6	(None)	Optional A_4 Offset Trim	22	D_3	Digital Input, MSB
7	F	Low-Pass Filter Pin	23	+5	+5 Digital Supply
8	J_2	Input to A_4	24	(None)	No Internal Connection
9	R_1	Output Reference	25	(None)	No Internal Connection
10	O	Output	26	Gain	Optional External Gain
11	S_1	Sense G = 1	27	Gain	Optional External Gain
12	S_2	Sense G = 4	28	(None)	Input CMV
13	S_3	Sense G = 2	29	+IN	Noninverting Input
14	R_2	Output Reference	30	+V	+15V Analog Supply
15	ANA GND	Analog Ground	31	BAL	Optional Input Stage
16	(None)	No Internal Connection	32	BAL	Offset Null

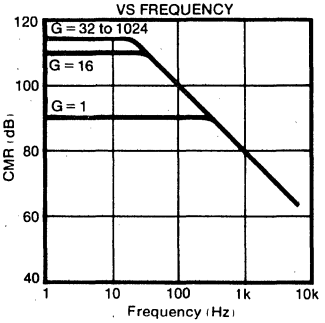
TYPICAL PERFORMANCE CURVES

Typical at +25°C unless otherwise noted.

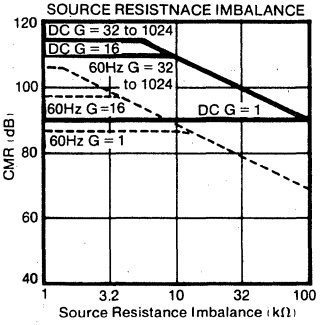
SMALL SIGNAL FREQUENCY RESPONSE



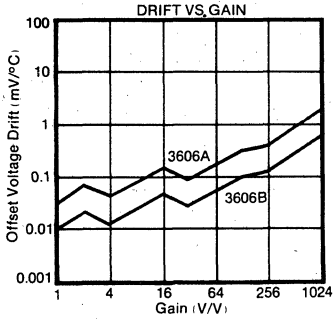
COMMON-MODE REJECTION VS FREQUENCY



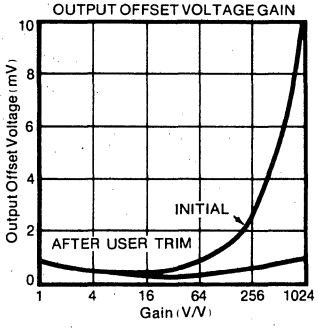
COMMON-MODE REJECTION VS SOURCE RESISTNACE IMBALANCE



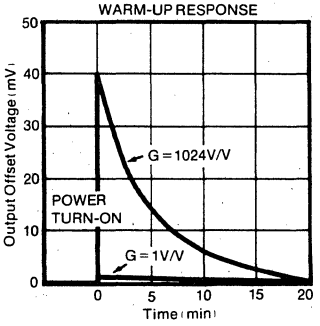
OUTPUT OFFSET VOLTAGE DRIFT VS GAIN



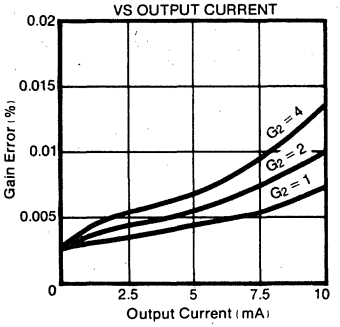
OUTPUT OFFSET VOLTAGE GAIN



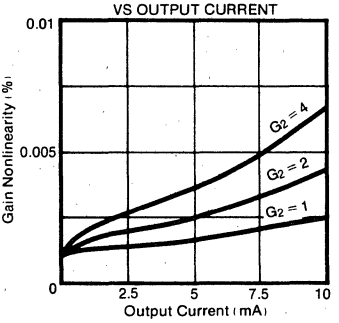
WARM-UP RESPONSE



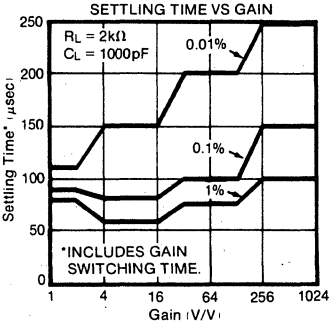
OUTPUT STAGE GAIN ERROR VS OUTPUT CURRENT



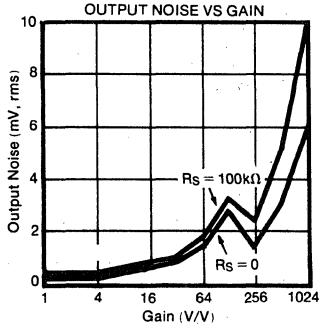
OUTPUT STAGE GAIN NONLINEARITY VS OUTPUT CURRENT



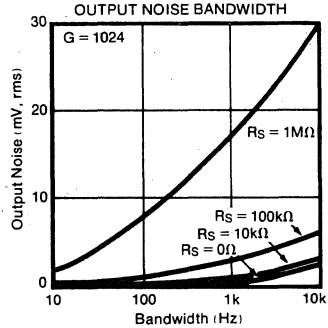
SETTLING TIME VS GAIN



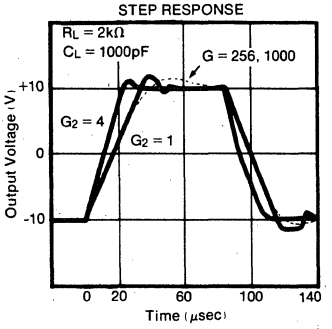
WIDEBAND OUTPUT NOISE VS GAIN



OUTPUT NOISE BANDWIDTH



STEP RESPONSE



INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Figure 2 shows the proper analog and digital power supply connections. The analog supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible. Because the amplifier is direct-coupled it must have a ground return path for the bias currents associated with the amplifier inputs at pins 2 and 29. If the ground return path is not inherent in the signal source (floating source) it must be provided externally. The ground return resistance (R_{GR}) should be kept as low as practical. An upper limit of approximately 50MΩ is established by the input bias currents of the amplifier and its common-mode voltage.

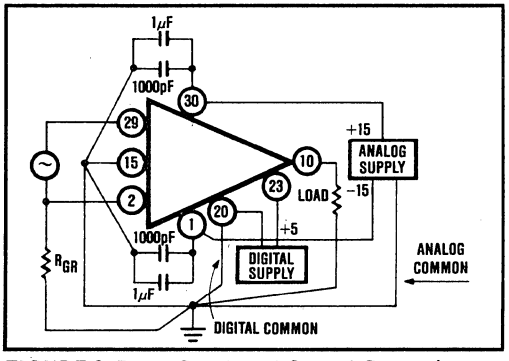


FIGURE 2. Power Supply and Ground Connections.

SIGNAL CONNECTIONS

Basic signal connections are shown in Figure 3. The connection to pin 14 completes the difference amplifier of A_3 (see Figure 1). The 3 to 8 jumper connects the output stage. The pin 9 connection provides a divide-by-two attenuator for the A_4 stage. This is necessary to limit the signal on the output stage switches to maintain signal linearity. The pin 11, 12 and 13 connections to pin 10 close the feedback loop around A_4.

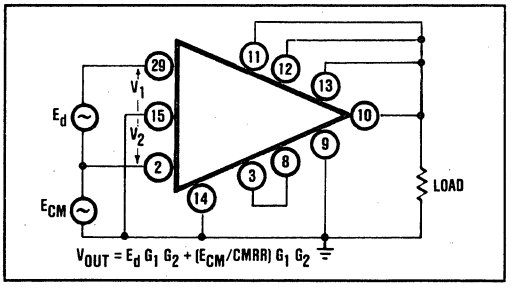


FIGURE 3. Basic Signal Connections.

In the equation shown in Figure 3, G_1 is the input stage gain and G_2 is the output stage gain. CMRR is the common-mode rejection ratio [CMR (in dB) = 20 log CMRR (in V/V)]. Common-mode voltage shown as E_{CM} is actually the average of the two voltages appearing at the two inputs (pins 29 and 2) with respect to pin 15 (V_1 and V_2).

GAIN SETTING

Gain is determined by a 4-bit digital word applied to the input D_0 through D_3 (see Figure 1). Pin 19 provides a latch function for the inputs. When pin 19 is a logic 0, changes on the D_0 through D_3 inputs are inhibited. Pin 19 should be at +5V if the latch is not used.

A gain state truth table is shown in Table I. Gains are determined by the resistor networks shown in Figure 1. For the state D_3, D_2 = 0, 0, the input stage gain is a function of the gain setting resistor R_G connected between pins 26 and 27. If gains of 1, 2 and 4 are desired, no connection should be made to pins 26 and 27 and the resistance across these pins should be kept high with respect to 40kΩ (> 400MΩ).

Gain accuracy is established by laser-trimming the thim-film resistor networks during assembly. No external, user trimming is required.

OUTPUT OFFSET

Output offset may be varied by either of two methods shown in Figure 4. Sources at pin 9 and pin 14 apply voltages to the noninverting inputs of A_4 and A_3 respectively (see Figure 1). Since the output stage gain occurs after these points, the output voltage bias established with V_{R1} and V_{R2} will vary with the output gain, G_2. Sources connected at pins 9 and 14 must have resistances low with respect to 10kΩ in order not to disturb gain accuracy and common-mode rejection.

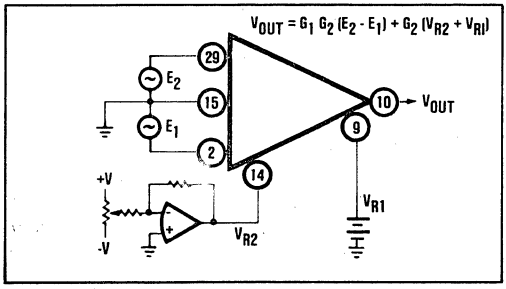


FIGURE 4. Output Offsetting.

LOW-PASS FILTER

For low frequency signals, system performance may be improved by reducing noise bandwidth in the amplifier. This may be accomplished with the addition of one or two external capacitors as shown in Figure 5. C_2 is connected to a 10k/10k attenuator and C_1 is connected as a feedback element across A4 (see Figures 1 and 5). The transfer function is:

$$\frac{V_O}{V_{IN}} = \left[\frac{10 \times 10^3}{100 \times 10^6\, S\,(C_2 + 330 \times 10^{-12}) + 20 \times 10^3}\right]\left[1 + \frac{10 \times 10^3}{10 \times 10^3\, R_1\, SC_1 + R_1}\right]$$

TABLE I. Gain State Truth Table.

Digital Inputs (G_1)		(G_2)		G_1 (A_1 and A_2) (Pins 2 & 29 to 3)	G_2 (A_4) (Pin 8 to Pin 10)	$G_1 \cdot G_2$ (R_G* = ∞)	$G_1 \cdot G_2$ (R_G* ≠ ∞)
D_3	D_2	D_1	D_0				
0	0	0	0	1 + 40k R_G	1	1	1(1 + 40k R_G)
0	0	0	1		2	2	2(1 + 40k R_G)
0	0	1	0		4	4	4(1 + 40k R_G)
0	0	1	1		4	4	4(1 + 40k R_G)
0	1	0	0	4	1	4	4
0	1	0	1		2	8	8
0	1	1	0		4	16	16
0	1	1	1		4	16	16
1	0	0	0	32	1	32	32
1	0	0	1		2	64	64
1	0	1	0		4	128	128
1	0	1	1		4	128	128
1	1	0	0	256	1	256	256
1	1	0	1		2	512	512
1	1	1	0		4	1024	1024
1	1	1	1		4	1024	1024

*R_G connected between pins 26 and 27.

The first term is a first order filter. The second term is more complex. R_1 varies with the output stage gain - 1.4k for $G_2 = 4$ (see Figure 1). The "1 + ..." nature of the transfer function prevents a true first order filter rolloff.

For most applications, the first order low-pass filter obtained by C_2 provides sufficient filtering. The value C_2 required for a desired cutoff frequency (f_2 in Hz) is obtained by the equation shown in Figure 5.

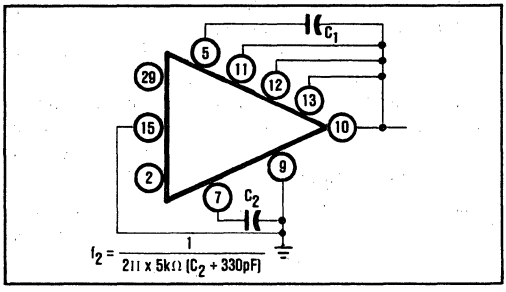


FIGURE 5. Low-Pass Filter Connections.

LARGER OUTPUT CURRENT

The output current rating of the 3606 is a minimum of ±5mA. The linearity of the gain is affected by output current. See Typical Performance Curves. Optimum linearity is achieved with $I_O \leq$ 1mA, $I_O \leq$ 5mA is acceptable. Above 5mA it may be desirable to use a power or current booster as shown in Figure 6. Burr-Brown's 3329 will provide ±100mA output while Burr-Brown's 3553 will supply ±200mA. When either booster is placed inside the feedback loop as shown, the booster's offset voltage produces no significant errors since it is divided by the open-loop gain of the output stage.

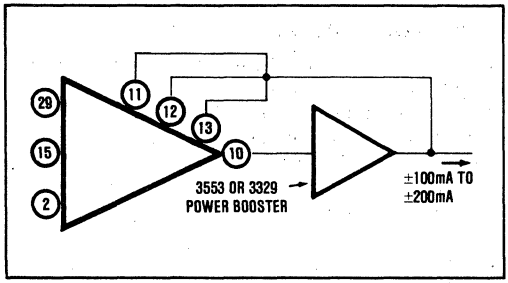


FIGURE 6. Output Current Booster.

GUARD DRIVE CONNECTIONS

Use of the guard drive connection shown in Figure 7 can improve system common-mode rejection when the distributed capacitance of the input lines is significant. The common-mode voltage which appears on the input lines and on pins 29 and 2 is computed by the 3606 [(V_1 + V_2)/2] and appears at pin 28. It is then fed back to the shield so that the voltage across the distributed capacitances is minimized. This reduces the common-mode current and improves common-mode rejection. The operational amplifier in the voltage follower configuration is used to supply more current than can be obtained from the 20k resistors connected internally to pin 28 (see Figure 1).

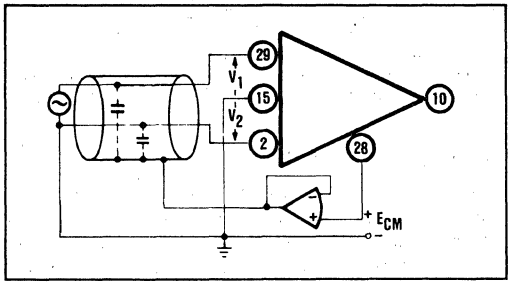


FIGURE 7. Guard Drive Connections.

OFFSET TRIM

Offset voltages of the 3606 are reduced by laser-trimming during assembly. This reduces the initial offset voltage and the offset voltage change with gain change to levels that are acceptable for most applications. For more critical applications the offset voltages can be externally

nulled to zero. The following steps should be followed (see Figure 8).

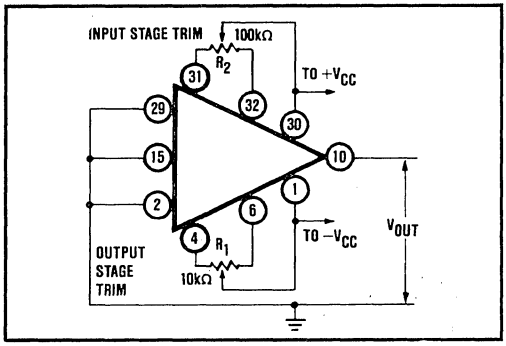


FIGURE 8. Optional Offset Trim.

1. Adjust both R_1 and R_2 to mid-range.
2. Set the gain to minimum (1V/V).
3. Adjust R_1 to make V_{OUT} equal zero.
4. Set the gain to maximum (1024V/V).
5. Adjust R_2 to make V_{OUT} equal zero.

By using this technique, the change in output offset voltage caused by a gain change of 1V/V to 1024V/V may be reduced to, typically 1mV instead of 10mV with no external trimming. Trimming may cause the offset voltage drift vs temperature to increase slightly.

APPLICATIONS

A typical application of 3606 in a microcomputer based data acquisition system is shown in the block diagram below.

The purpose of this system is to be able to acquire data from a specific analog input channel, suitably condition it (amplify it and convert it to digital form) and store it or transmit it for further processing.

Initially the Microcomputer loads the RAM (random access memory) with the required coding for various desired gains via Data Bus. The coding associates the gain state truth table for 3606 with corresponding address locations in the computer memory. So when the computer puts out an instruction to multiplex a specific analog input channel through the multiplexer via the Address Bus, the RAM also receives the same address information and puts out corresponding gain code to the PGIA 3606. The 3606 amplifies the multiplexed signal by the programmed gain value, and outputs it to S/H (sample and hold). The S/H holds the output value when it receives the control signal from the computer and the A/D converts it and outputs it to the computer via the Data Bus under computer control.

The PGIA 3606 allows the system user to modify and reprogram gain values for different analog input channels merely by changing the software computer program. Since different dedicated instruments are not required for various input channels, the PGIA also saves space and overall system costs.

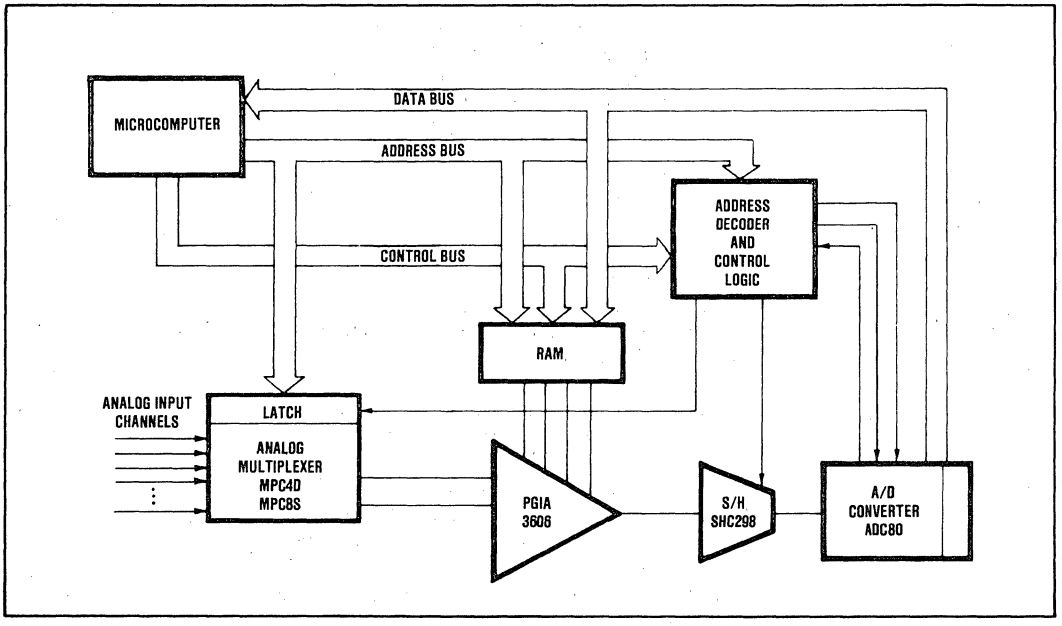


FIGURE 9. Use of 3606 in Data Acquisition System.

BURR-BROWN®

3627

High Accuracy Unity-Gain DIFFERENTIAL AMPLIFIER

FEATURES

- LOW COST
- EASY TO USE
- COMPLETELY SELF-CONTAINED
- HIGH ACCURACY
  - Gain Error, 0.005%
  - Nonlinearity, 0.0005%
  - CMR, 106dB
- NO TRIMMING REQUIRED

DESCRIPTION

The 3627 is a high accuracy committed-gain differential amplifier. It consists of a high quality monolithic operation amplifier, a low drift thin-film resistor network and laser-trimmed offset circuitry - all inside a single integrated circuit package.

The fact that the 3627 is completely self-contained in a TO-99 package has several user benefits:

The total performance is guaranteed as a single component.

No gain adjustments are required.

No offset trimming is required.

The whole circuit, including the gain setting resistors and offset trim circuitry, is protected by the environmentally rugged hermetically sealed package.

The total amplifier function is very small in size (0.108 square inches of area and 0.025 cubic inches of volume).

The 3627 is offered in two grades; the 3627AM and the 3627BM. They differ only in common-mode rejection (94dB typ. vs 106dB typ.) and offset voltage drift ($15\mu V/^{\circ}C$ typ. vs $10\mu V/^{\circ}C$ typ.)

The 3627 offers excellent total performance with no fuss and a very-low total installed cost.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and ±15VDC power supply unless otherwise noted.

MODELS	3627AM	3627BM
GAIN		
Gain Equation	G = 1V/V(1)	
Gain Error	±0.01%, max (±0.005% typ)	
Gain Nonlinearity(2)	±0.001%, max (±0.0005% typ)	
Gain Temp. Coefficient, max	±0.0005%/°C (5ppm/°C)	
Gain Temp. Coefficient, typ	±0.0002%/°C (2ppm/°C)	
OUTPUT		
Rated Output, min	±10V at ±5mA	
Rated Output, typ	±12V at ±10mA	
Output Impedance	0.01Ω	
INPUT		
Input Impedance		
Differential	50kΩ	
Common-mode	50kΩ	
Input Voltage Range		
Differential	±20V	
Common-mode	±20V	
Common-mode Rejection, DC to 60Hz		
CMR, at 25°C	90dB, min (94dB, typ)	100dB, min (106dB, typ)
CMR, -25°C to +85°C	80dB, min (90dB, typ)	86dB, min (94dB, typ)
OFFSET AND NOISE		
Offset Voltage, RTO(4)(5)		
at 25°C	250μV, max (100μV, typ)	
vs Temperature, μV/°C	30, max (15, typ)	20, max (10, typ)
vs Supply	20μV/V	
vs Time	20μV/mo	
Noise Voltage, RTO(4)(6)		
0.01Hz to 10Hz	2μV, p-p	
10Hz to 100Hz	1.5μV, rms	
DYNAMIC RESPONSE		
Small Signal, ±1% Flatness	5kHz min (8kHz, typ)	
Small Signal, ±3dB Flatness	0.8MHz min (1.2MHz, typ)	
Full Power Bandwidth	14kHz min (18kHz, typ)	
Slew Rate	0.6V/μsec min (1V/μsec, typ)	
Settling Time, 0.1% (±10mV)	20μsec	
Settling Time, 0.01% (±1mV)	50μsec	
POWER SUPPLY		
Rated Voltage	±15VDC	
Voltage Range	±5VDC to ±18VDC	
Quiescent Supply Current	±2mA	
TEMPERATURE RANGE		
Specifications, min	-25°C to +85°C	
Operation	-55°C to +125°C	
Storage	-65°C to +150°C	

NOTES:

1. Connected as unity-gain amplifier. Several other configurations are possible. See the figures in Discussion and Typical Applications.
2. Nonlinearity is the maximum peak deviation from the best straightline as a percent of full scale peak-to-peak output.
3. With zero source impedance unbalance.
4. Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifiers offset voltage and noise voltage.
5. Includes effects of amplifiers' input bias currents.
6. Includes effects of amplifiers' input current noise.

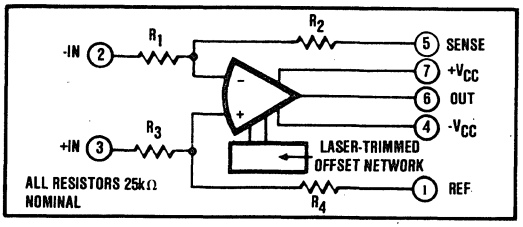
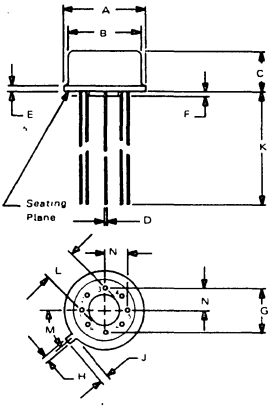


FIGURE 1. Simplified Circuit Diagram.

MECHANICAL

TO-99

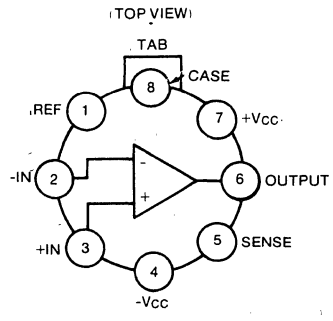


NOTE
Leads in true position within .010" (.25mm) R @ MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	-	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

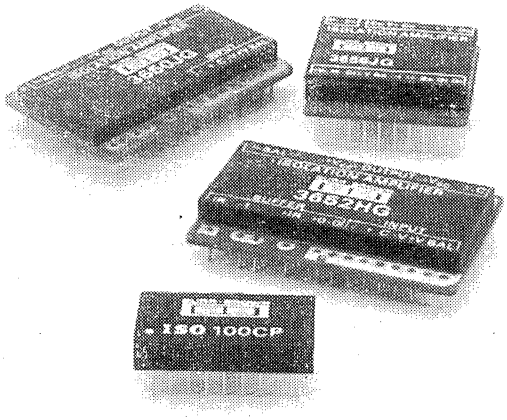
Pin material and plating compostion conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CONNECTION DIAGRAM



See Figure 1 for circuit diagram.

ISOLATION AMPLIFIERS



WHAT IS AN ISOLATION AMPLIFIER?

An isolation amplifier is a device with the primary function of providing ohmic isolation (break the ohmic continuity of electrical signal) between the input signal/circuitry and the output of the amplifiers. It usually consists of an input operational amplifier or instrumentation amplifier followed by a unity-gain isolation stage. The sole purpose of the unity-gain isolation stage is to completely isolate the input from the output of the device. Ideally, the ohmic continuity of the input signal is broken (at the isolation barrier) yet accurate signal transfer without any attenuation is achieved across the unity-gain isolation stage. An important feature of an isolation amplifier is that it has a completely floating input which helps eliminate cumbersome connections to source ground in several applications.

Figures 1 and 2 show typical isolation amplifier applications. The isolation-mode voltage V_{iso} is the voltage which exists across the isolation barrier. The contribution of the output referred error caused by V_{iso} is (V_{iso}/IMRR) x Gain where IMRR is the Isolation Mode Rejection Ratio. V_{sig} is the differential input signal and V_{cm} is the common-mode voltage. The "Leakage Current" is the current which flows across the isolation barrier with some specified isolation voltage applied between the input and the output.

CHARACTERISTICS OF ISOLATION AMPLIFIERS

The following is a discussion of some of the characteristics and terms unique to isolation amplifiers.

Common-mode Voltage and Isolation Voltage - Some manufacturers (other than Burr-Brown) treat common-mode voltage and isolation voltages synonymously in describing the use and/or specifications of isolation amplifiers. It is important to understand the significance of these terms and the difference between them.

When the input common is grounded, the input signal V_d (see Figure 1) can be floated by the amount V_{cm} above the input ground. V_{cm} is the common-

mode voltage (CMV) and is generally ±10V, limited by the CMV rating of the input stage amplifier. In applications involving higher systems common-mode voltages, input common terminal is not grounded and the common-mode voltages are referenced across the isolation barrier to the output common terminal.

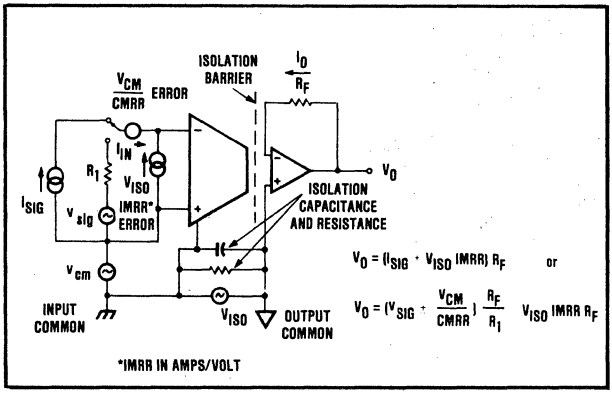


FIGURE 1. Typical Isolation Amplifier, Current (Input) Mode.

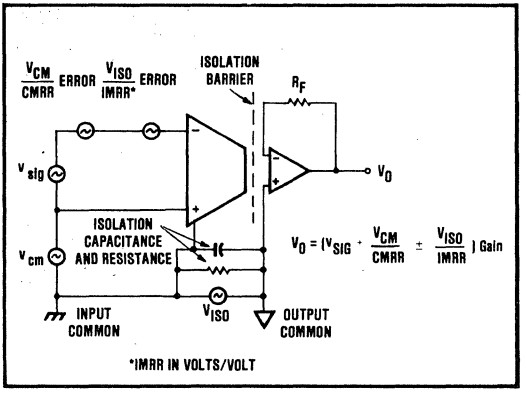


FIGURE 2. Typical Isolation Amplifier, Voltage (Input) Mode.

The isolation voltage V_{iso} as shown in Figure 1 is the potential difference between the input common and the output common terminals. The isolation voltage rating describes the amount of voltage that the isolation barrier can withstand without breakdown. This feature of the isolation amplifier allows two distinct ground connections to be made when necessary. It allows the isolation amplifier to be used in applications involving very-high common-mode voltages and in applications of breaking ground loops.

Many applications involve a large "system common-mode voltage." In such applications, the isolation amplifier's input common terminal is not connected to any ground but the output common terminal is connected to the system ground. In such a case, the term V_{cm} shown in Figures 1 and 2 becomes negligible and V_{iso} determines the safe limit for the system common-mode voltage. In this manner, the isolation amplifier can accommodate common-mode voltages of 2000V or more.

Common-mode Rejection and Isolation Rejection - Isolation-mode rejection (IMR) is another term which some other manufacturers refer to as common-mode rejection (CMR). The above discussion on the common-mode voltage and isolation voltage helps recognize the difference between CMR and the IMR. The CMR is the measure of the input stage amplifier's ability to reject common-mode input signals (common-mode with reference to the output common) while transmitting the differential signal across the isolation barrier. The isolation-mode rejection ratio (IMRR) is defined by the equation shown in Figures 1 and 2. Thus, understanding the IMR capability of isolation amplifiers allows their meaningful use in applications requiring very high common-mode rejection ratios such as 100dB to 140dB.

Isolation Voltage Ratings, Test Voltage - It is important to understand the significance of the continuous derated isolation voltage specification and its relationship to the actual test voltage applied to the unit. Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated minimum specification?" There are several rules of thumb used throughout the industry to establish this relationship. For most isolation amplifiers, Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.* Where the real voltages are well defined or where the isolation voltage is not continuous the user may chose to use a less conservative derating to establish a specification from the test voltage.

APPLICATIONS OF ISOLATION AMPLIFIERS

When one or more of the following conditions/requirements are present in an application, an isolation amplifier would generally be the right choice as a signal conditioning device:

- When ohmic isolation between the signal source and the output is a requirement (isolation impedance between the input and the output $>$ 10MΩ).
- When excellent common-mode noise and voltage rejection is a requirement (CMR $>$ 100dB).
- When it is necessary to process signals in the presence of, or riding on, high common-mode voltages (CMV $\gg$ 10V).

In general, most applications can be broadly categorized into the following four types:

- Amplifying and measuring low level signals in the presence of high common-mode voltages.
- Breaking ground loops and/or eliminating source ground connections. The isolation amplifier provides full floating input, eliminating the need for connections to source ground, and thus allows two-wire hook-up to the signal sources.
- Providing an interface between medical patient monitoring equipment and the transducer/devices which may be in physical contact with the patients. Such applications require high isolation voltage levels and very-low leakage currents.
- Providing isolation protection to electronic instruments/equipment. Large common-mode voltages occasionally cause hazardous electronic faults. Low leakage currents and high isolation voltage capability of isolation amplifiers help protect instruments against damage caused by such faults.

Isolation amplifier performance requirements vary significantly, depending on the type of requirement. In applications where bandwidth and speed of response are more important than gain accuracy and linearity, the optically-coupled amplifiers will be the best choice. For applications where gain accuracy and linearity are key parameters, Burr-Brown's family of transformer-coupled amplifiers are the suitable choice.

*Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS 1-109 and ICS 1-111.

SELECTION GUIDE

Description	Model	Isolation Voltage (V) Continuous, peak	Isolation Voltage (V) Pulse/Test, peak	Isolation Mode Rejection, min. DC (dB)	Isolation Mode Rejection, min. 60Hz (dB)	Leakage Current at Test Voltage (μA)	Isolation Impedance (Ω)	Isolation Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ. (%)	Voltage Drift, (±μV/°C) max	Bias Current, max	±3dB Freq. (kHz)	External Isolation Power Required	Temp. Range [1]	Package	Page
TRANSFORMER COUPLED AMPLIFIERS																	
Low Drift[2]	3450	±500	±2000	160	120	1	10^{12}	16	±0.005	±0.0015	100	50nA	1.5	No	Com	Module	3-19
Low Bias FET	3451	±500	±2000	160	120	1	10^{12}	16	±0.025	±0.005	100	25pA	2.5	No	Com	Module	3-19
	3452	±2000	±5000	160	120	1	10^{12}	16	±0.025	±0.005	100	10pA	2.5	No[4]	Com	Module	3-19
	3455	[3]	[3]	160	120	[3]	10^{12}	16	±0.025	±0.005	100	20pA	2.5	No[4]	Com	Module	3-19
Highest Isolation Voltage	3656AG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	25 + (500/G_1)	100nA	30	No	Ind	DIP	3-29
	3656BG	±3500	±8000	160	125	0.5	10^{12}	6	±0.05	±0.03	5 + (1000/G_1)	100nA	30	No	Ind	DIP	3-29
	3656HG	±3500	±8000	160	125	0.5	10^{12}	6	±0.15	±0.03	200 + (1000/G_1)	100nA	30	No	Com	DIP	3-29
	3656JG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	50 + (750/G_1)	100nA	30	No	Com	DIP	3-29
	3656KG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	10 + (350/G_1)	100nA	30	No	Com	DIP	3-29
OPTICALLY COUPLED AMPLIFIERS																	
Balanced Current Input	3650HG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	25	10nA	15	Yes[6]	Ind	DIP	3-21
	3650JG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.1	±0.03	10	10nA	15	Yes[6]	Ind	DIP	3-21
	3650KG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.05	±0.02	5	10nA	15	Yes[6]	Ind	DIP	3-21
	3650MG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	100	10nA	15	Yes[6]	Ind	DIP	3-21
Balanced FET Input	3652HG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	50	50nA	15	Yes	Ind	DIP	3-21
	3652JG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.1	±0.05	25	50nA	15	Yes	Ind	DIP	3-21
	3652MG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	100	50nA	15	Yes	Ind	DIP	3-21
Low Drift Wide Bandwidth	ISO100AP	750	2500	146[6]	108[6]	0.3	10^{12}	2.5	0.4	0.1	10[6]	10nA	60	Yes	Ind	DIP	3-6
	ISO100BP	750	2500	146[6]	108[6]	0.3	10^{12}	2.5	0.1	0.01	4[6]	10nA	60	Yes	Ind	DIP	3-6
	ISO100CP	750	2500	146[6]	108[6]	0.3	10^{12}	2.5	0.07	0.02	4[6]	10nA	60	Yes	Ind	DIP	3-6

NOTES: (1) Com = 0°C to +70°C; Ind = −25°C to +85°C. (2) Bipolar. (3) Isolation voltage tested at 2500V, rms, 60Hz; leakage current tested for 2μA max at 240V, rms, 60Hz. (4) ±15V at ±15mA isolated power available to power external circuitry. (5) At 240V/60Hz. (6) R_{IN} = 10k, Gain = 100.

GLOSSARY OF TERMS & DEFINITIONS
Isolation Amplifiers

ISOLATION AMPLIFIER

A device which provides ohmic isolation (breaks ohmic continuity of an electric signal) between the input and the output of the device. Method of coupling may be thermal, magnetic, optical, or any means other than direct ohmic coupling. Such a device allows the input circuit to be referenced separately and independent of the output circuitry.

ISOLATION BARRIER

A barrier or region between the input and the output stage of an isolatiom amplifier, where the signal transfer is achieved between the input and the output.

ISOLATION IMPEDANCE

The effective impedance between the input common terminal and the output common terminal. It is the impedance of the isolation barrier. (It is usually specified as a typical parameter. Leakage current is related to isolation impedance and is usually specified with a maximum limit.)

ISOLATION-MODE REJECTION (IMR)

The IMR is the measure of an isolation amplifier's ability to reject common-mode input signals (common-mode with reference to the output common), while transmitting the differential signal across the isolation barrier. It is the voltage or current that must be applied to the input to force the output to zero when V_{iso} is present.

For voltage input mode:

$$IMRR = \frac{V_{o\ error\ ISO}/G}{V_{iso}} \text{ with } V_o = 0$$

For current input mode:

$$IMRR = \frac{I_{o\ error\ ISO}}{V_{iso}} \text{ with } V_o = 0\ (I_o = 0)$$

ISOLATION VOLTAGE

The potential difference between the input stage common and output stage common terminals of an isolation amplifier.

ISOLATION VOLTAGE RATING

The amount of voltage that can be impressed between the input common and the output common terminals (across the isolation barrier) without resulting in breakdown.

LEAKAGE CURRENT

The current that flows between the input common terminal and the output common terminal (across the isolation barrier) with a specified voltage applied across it. (It is usually 100% tested and specified with a maximum limit.)

BURR-BROWN®

ISO100

Miniature
Low Drift - Wide Bandwidth
ISOLATION AMPLIFIER

FEATURES

- EASY TO USE, SIMILAR TO AN OP AMP
  $V_{OUT}/I_{IN} = R_F$, Current Input
  $V_{OUT}/V_{IN} = R_F/R_{IN}$, Voltage Input
- 100% TESTED FOR BREAKDOWN
  750V Continuous Isolation Voltage
- ULTRA-LOW LEAKAGE, 0.3μA, max, at 240V/60Hz
- WIDE BANDWIDTH, 60kHz
- LOW COST
- 18-PIN DIP PACKAGE

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer sensing
  (thermocouple, RTD, pressure bridges)
  4mA to 20mA loops
  Motor and SCR control
  Ground loop elimination
- BIOMEDICAL MEASUREMENTS
- TEST EQUIPMENT
- DATA ACQUISITION

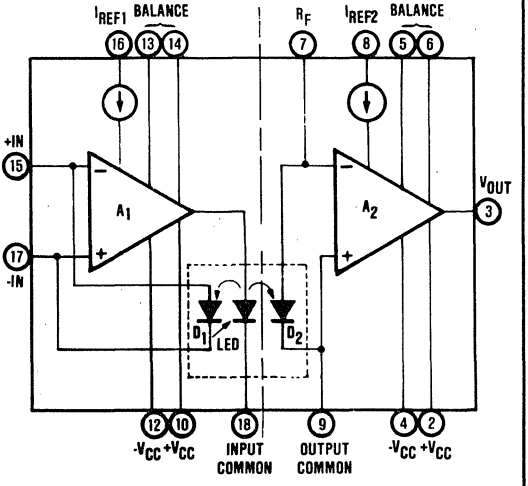
DESCRIPTION

The ISO100 is a miniature low cost optically-coupled isolation amplifier. High accuracy, linearity, and time-temperature stability are achieved by coupling light from an LED back to the input (negative feedback) as well as forward to the output. Optical components are carefully matched and the amplifier is actively laser-trimmed to assure excellent tracking and low offset errors.

The circuit acts as a current-to-voltage converter with a minimum of 750V (2500V test) between input and output terminals. It also effectively breaks the galvanic connection between input and output commons as indicated by the ultra-low 60Hz leakage current of 0.3μA at 240V. Voltage input operation is easily achieved by using one external resistor.

Versatility along with outstanding DC and AC performance provide excellent solutions to a variety of challenging isolation problems. For example, the ISO100 is capable of operating in many modes, including: noninverting (unipolar and bipolar) and inverting (unipolar and bipolar) configurations. Two precision current sources are provided to accomplish bipolar operation. Since these are not required for unipolar operation, they are available for external use (see Applications section).

Designs using the ISO100 are easily accomplished with relatively few external components. Since V_{OUT} of the ISO100 is simply $I_{IN}R_{OUT}$, gains can be changed by altering one resistor value. In addition, the ISO100 has sufficient bandwidth (DC to 60kHz) to amplify most industrial and test equipment signals.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±V_{CC} = 15VDC unless otherwise noted.

PARAMETER	CONDITIONS	ISO100AP			ISO100BP			ISO100CP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION											
Voltage,											
Rated Continuous, AC peak or DC[1]		750			•			•			V
Test Breakdown, DC	10sec	2500			•			•			V
Rejection[2] DC			5			•			•		pA/V
	R_{IN} =10kΩ, Gain = 100		146			•			•		dB
AC	60Hz, 480V, R_F = 1MΩ		400			•			•		pA/V
	R_{IN} = 10kΩ, Gain = 100		108			•			•		dB
Impedance			10^{12} || 2.5			•			•		Ω || pF
Leakage Current	240V, rms, 60Hz			0.3			•			•	μA, rms
OFFSET VOLTAGE (RTI)											
Input Stage (V_{OSI})											
Initial Offset				500			300			200	μV
vs Temperature				5			2			2	μV/°C
vs Input Power Supplies				105			•			•	dB
vs Time			1			•			•		μV/kHr
Output Stage (V_{OSO})											
Initial Offset				500			300			200	μV
vs Temperature				5			2			2	μV/°C
vs Output Power Supplies				105			•			•	dB
vs Time			1			•			•		μV/kHr
Common-Mode Rejection Ratio[2]	60Hz, R_F = 1MΩ		3			•			•		nA/V
	R_{IN} = 10kΩ, Gain = 100		90			•			•		dB
Common-Mode Range		±10			•			•			V
REFERENCE CURRENT SOURCES											
Magnitude											
Nominal		10.5	12	12.5	•	•	•	•	•	•	μA
vs Temperature				300			300			150	ppm/°C
vs Power Supplies			0.3	3		•	•		•	•	nA/V
Matching											
Nominal			50			•			•		nA
vs Temperature			150			•			•		ppm/°C
vs Power Supplies			0.3			•			•		nA/V
Compliance Voltage		-10		+15	•		•	•		•	V
Output Resistance			2×10^9			•			•		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	Gain = 1V/μA		60			•			•		kHz
Full Power Bandwidth	Gain = 1V/μA, V_O = ±10V		5			•			•		kHz
Slew Rate		0.22	0.31		•	•		•	•		V/μsec
Settling Time	0.1%		100			•			•		μsec
TEMPERATURE RANGE											
Specification		-25		+85	•		•	•		•	°C
Operating		-40		+100	•		•	•		•	°C
Storage		-55		+100	•		•	•		•	°C
UNIPOLAR OPERATION											
GENERAL PARAMETERS											
Input Current Range											
Linear Operation		-20		-0.02	•		•	•		•	μA
Without Damage		-1		+1	•		•	•		•	mA
Input Impedance			0.1			•			•		Ω
Output Voltage Swing	R_L = 2kΩ, R_F = 1MΩ	-10		0	•		•	•		•	V
Output Impedance	DC, open-loop		1200			•			•		Ω
GAIN	$V_O = R_F (I_{IN})$										
Initial Error (Adjustable To Zero)			2	5		1	2		1	2	% FS
vs Temperature			0.03	0.07		0.01	0.05		0.005	0.03	%/°C
vs Time			0.05			•			•		%/kHr
Nonlinearity[3]			0.1	0.4		0.03	0.1		0.02	0.07	%
CURRENT NOISE	I_{IN} = 0.2μA										
0.01Hz to 10Hz			20			•			•		pA, p-p
10Hz			1			•			•		pA/√Hz
100Hz			0.7			•			•		pA/√Hz
1kHz			0.65			•			•		pA/√Hz
INPUT OFFSET CURRENT (I_{OS})											
Initial Offset			1	10		•	•		•	•	nA
vs Temperature			0.05			•			•		nA/°C
vs Power Supplies			0.1			•			•		nA/V
vs Time			100			•			•		pA/kHr

ELECTRICAL (CONT)

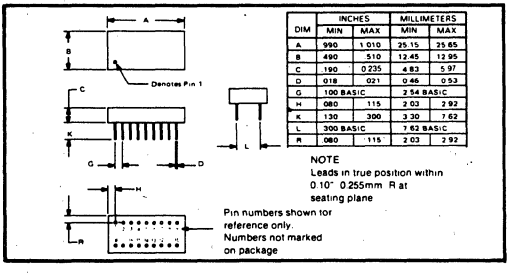
PARAMETER	CONDITIONS	ISO100AP			ISO100BP			ISO100CP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES											
Input Stage											
Voltage (rated performance)			±15			•			•		V
Voltage (derated performance)		±7		±18	•		•	•		•	V
Supply Current	I_{IN} = -0.02µA		±1.1	±2		•	•		•	•	mA
	I_{IN} = -20µA		+8, -1.1	+13, -2		•	•		•	•	mA
Output Stage											
Voltage (rated performance)			±15			•			•		V
Voltage (derated performance)		±7		±18	•		•	•		•	V
Supply Current	V_O = 0		±1.1	±2		•	•		•	•	mA
Short Circuit Current Limit				±40			•			•	mA
BIPOLAR OPERATION											
GENERAL PARAMETERS											
Input Current Range											
Linear Operation		-10		+10	•		•	•		•	µA
Without Damage		-1		+1	•		•	•		•	mA
Input Impedance			0.1			•			•		Ω
Output Voltage Swing	R_L = 2kΩ, R_F = 1MΩ	-10		+10	•		•	•		•	V
Output Impedance			1200			•			•		Ω
GAIN	$V_O = R_F (I_{IN})$										
Initial Error (Adjustable To Zero)			2	5		1	2		1	2	% of FS
vs Temperature			0.03	0.07		0.01	0.05		0.005	0.03	%/°C
vs Time			0.05			•			•		%/kHr
Nonlinearity (3)			0.1	0.4		0.03	0.1		0.02	0.07	%
CURRENT NOISE	I_{IN} = 0.2µA										
0.01Hz to 10Hz			1.5			•			•		nA, p-p
10Hz			17			•			•		pA/√Hz
100Hz			7			•			•		pA/√Hz
1kHz			6			•			•		pA/√Hz
INPUT OFFSET CURRENT (I_{OS}, bipolar)(4)											
Initial Offset			40	200		20	70		10	35	nA
vs Temperature				3			2			1	nA/°C
vs Power Supplies				0.7			•			•	nA/V
vs Time			250			•			•		pA/kHr
POWER SUPPLIES											
Input Stage											
Voltage (rated performance)			±15			•			•		V
Voltage (derated performance)		±7		±18	•		•	•		•	V
Supply Current	I_{IN} = +10µA		+2, -1.1	+3,-2		•	•		•	•	mA
	I_{IN} = -10µA		+8, -1.1	+13,-2		•	•		•	•	mA
Output Stage											
Voltage (rated performance)			±15			•			•		V
Voltage (derated performance)		±7		±18	•		•	•		•	V
Supply Current	V_O = 0		±1.1	±2		•	•		•	•	mA
Short Circuit Current Limit				±40			•			•	mA

* Same as ISO100AP.

NOTES:

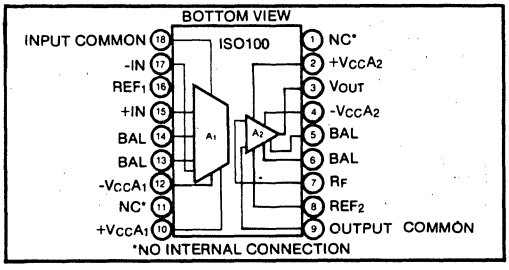
1. See Typical Performance Curves for temperature effects.
2. See Theory of Operation section for definitions. For dB see Ex. 2, CM and HV errors.
3. Nonlinearity is the peak deviation from a "best fit" straight line expressed as a percent of full scale output.
4. Bipolar offset current includes effects of reference current mismatch and unipolar offset current.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	990	1 010	25.15	25 65
B	490	510	12 45	12 95
C	190	0 235	4 83	5 97
D	018	021	0 46	0 53
G	100 BASIC		2 54 BASIC	
H	080	115	2 03	2 92
K	130	300	3 30	7 62
L	300 BASIC		7 62 BASIC	
R	080	115	2 03	2 92

PIN CONFIGURATION



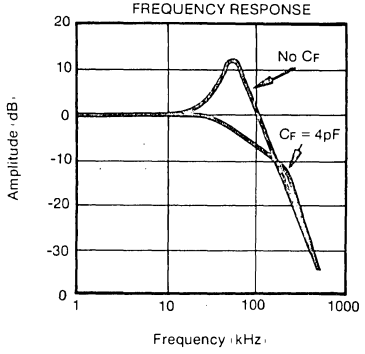
ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±18V
Isolation Voltage	2500V
Input Current	±1mA
Storage Temperature Range	-55°C to +100°C
Lead Temperature soldering 10 seconds	+300°C
Output Short-circuit Duration	Continuous to ground

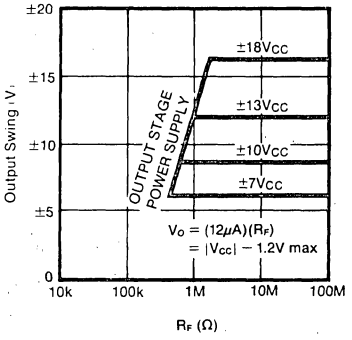
TYPICAL PERFORMANCE CURVES

T_A = +25°C, ±V_{CC} = 15VDC unless otherwise noted

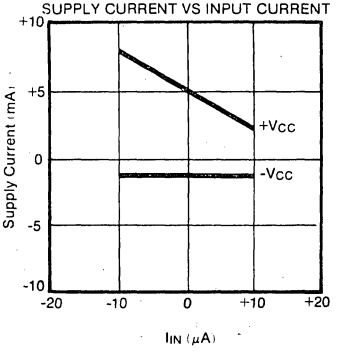
SMALL SIGNAL FREQUENCY RESPONSE



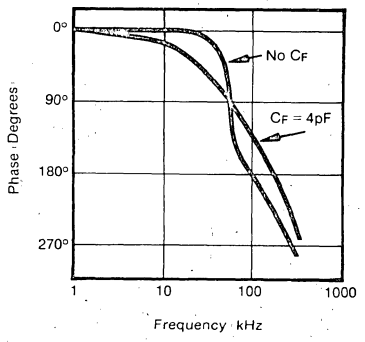
BIPOLAR OUTPUT SWING VS R_F



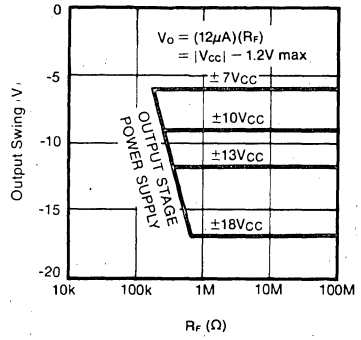
BIPOLAR INPUT STAGE SUPPLY CURRENT VS INPUT CURRENT



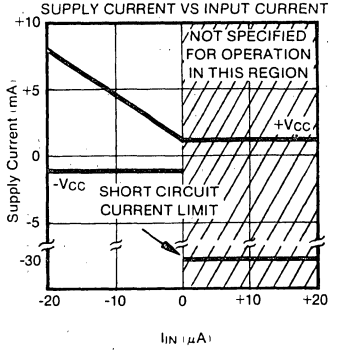
PHASE SHIFT VS FREQUENCY



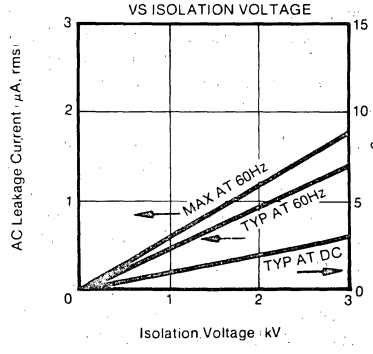
UNIPOLAR OUTPUT SWING VS R_F



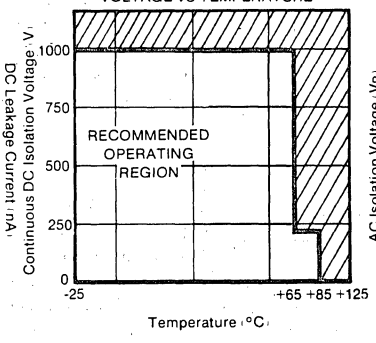
UNIPOLAR INPUT STAGE SUPPLY CURRENT VS INPUT CURRENT



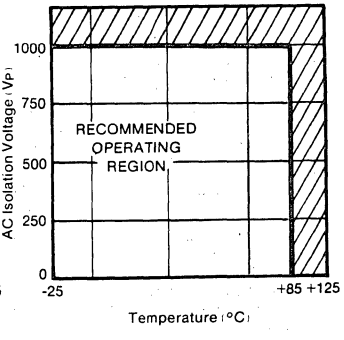
ISOLATION LEAKAGE CURRENT VS ISOLATION VOLTAGE

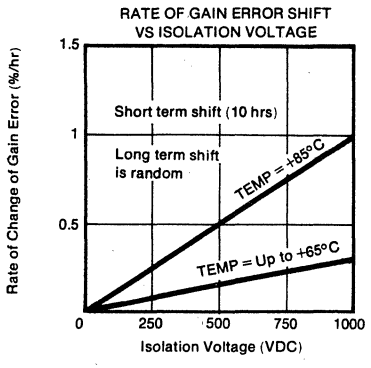


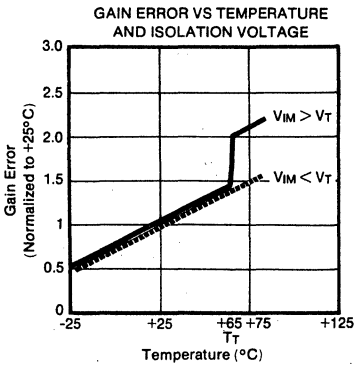
CONTINUOUS DC ISOLATION VOLTAGE VS TEMPERATURE



AC ISOLATION VOLTAGE VS TEMPERATURE







NOTES:
V_T and T_T approximate the threshold for the indicated gain shift. This is caused by the properties of the optical cavity.
T_T ≈ +65°C, V_T ≈ 200VDC. Shift does not occur for AC voltages.

V_{IM} = Isolation-mode Voltage
V_T = Threshold Voltage
T_T = Threshold Temperature

THEORY OF OPERATION

The ISO100 is fundamentally a unity gain current amplifier intended to transfer small signals between electrical circuits separated by high voltages or different references. In most applications an output voltage is obtained by passing the output current through the feedback resistor (R_F).

The ISO100 uses a single light emitting diode (LED) and a pair of photodiode detectors, coupled together, to isolate the output signal from the input.

Figure 1 shows a simplified diagram of the amplifier. I_{REF1} and I_{REF2} are required only for bipolar operation, to generate a midscale reference. The LED and photodiodes (D1 and D2) are arranged such that the same amount of light falls on each photodiode. Thus, the currents generated by the diodes match very closely. As a result, the transfer function depends upon optical match, rather than absolute performance. Laser-trimming of the components improves matching and enhances accuracy, while negative feedback improves linearity. Negative feedback around A1 occurs through the optical path formed by the LED and D1. The signal is transferred across the isolation barrier by the matched light path to D2.

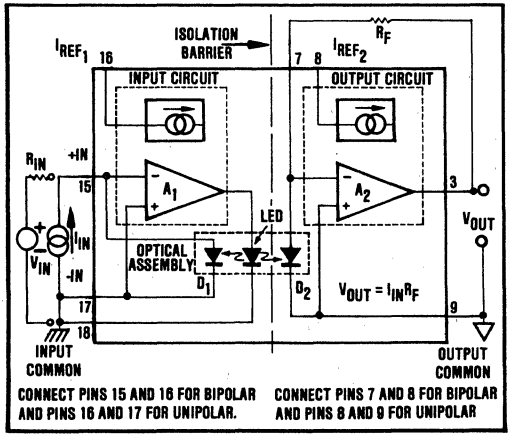


FIGURE 1. Simplified Block Diagram of the ISO100.

The overall ISO amplifier is noninverting (a positive going input produces a positive going output).

INSTALLATION AND OPERATING INSTRUCTIONS

UNIPOLAR OPERATION

In Figure 1, assume a current, I_{IN}, flows out of the ISO100 (I_{IN} must be negative in unipolar operation). This causes the voltage at pin 15 to decrease. Because the amplifier is inverting, the output of A1 increases, driving current through the LED. As the LED light output increases, D1 responds by generating an increasing current. The current increases until the sum of the currents in and out of the input node (-Input to A_1) is zero. At that point the negative feedback through D1 has stabilized the loop, and the current I_{D1} equals the input current plus the bias current. As a result no bias current flows in the source. Since D1 and D2 are matched ($I_{D1} = I_{D2}$), I_{IN} is replicated at the output via D2. Thus, A1 functions as a unity-gain current amplifier, and A2 is a current-to-voltage converter, as described below.

Current produced by D2 must either flow into A2 or R_F. Since A2 is designed for low bias current (≈10nA) almost all of the current flows through R_F to the output. The output voltage then becomes;

$$V_O = (I_{D2})\ R_F = (I_{D1} \pm I_{OS})\ R_F \approx -(-I_{IN})\ R_F = I_{IN}R_F, \quad (1)$$

where, I_{OS} is the difference between A1 and A2 bias currents. For input voltage operation I_{IN} can be replaced by a voltage source (V_{IN}) and series resistor (R_{IN}) since the summing node of the op amp is essentially at ground. Thus, $I_{IN} = V_{IN}/R_{IN}$.

Unipolar operation does have some constraints, however. In this mode the input current must be negative so as to produce a positive output voltage from A1 to turn the LED on. A current more negative than 20nA is necessary to keep the LED turned on and the loop stabilized. When this condition is not met the output may be indeterminant. Many sensors generate unidirectional signals, e.g., photoconductive and photodiode devices, as well as some applications of thermocouples. However, other applications do require bipolar operation of the ISO100.

BIPOLAR OPERATION

To activate the bipolar mode, reference currents as shown in Figure 1, are attached to the input nodes of the op amps. The input stage stabilizes just as it did in unipolar operation. Assuming $I_{IN} = 0$, the photodiode has to supply all the I_{REF1} current. Again, due to symmetry, $I_{D1} = I_{D2}$. Since the two references are matched, the current generated by D2 will equal I_{REF2}. This results in no current flow in R_F, and the output voltage will be zero. When I_{IN} either adds or substracts current from the input node, the current D1 will adjust to satisfy $I_{D1} = I_{IN} + I_{REF1}$. Because I_{REF1} equals I_{REF2} and I_{D1} equals I_{D2}, a current equal to I_{IN} will flow in R_F. The output voltage is then $V_O = I_{IN}R_F$. The range of allowable I_{IN} is limited. Positive I_{IN} can be as large as I_{REF1} (10.5μA, min). At this point, D1 supplies no current and the loop opens. Negative I_{IN} can be as large as that generated by D1 with maximum LED output (recommended 10μA, max).

DC ERRORS

Errors in the ISO100 take the form of offset currents and voltages plus their drifts with temperature. These are shown in Figure 2.

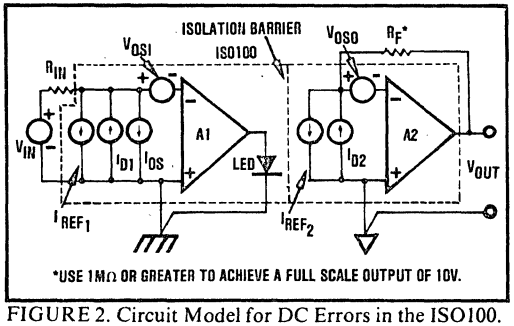


FIGURE 2. Circuit Model for DC Errors in the ISO100.

A1 and A2: are assumed to be ideal amplifiers.

V_{OSO} and V_{OSI}: are the input offset voltages of the output and input stage, respectively. V_{OSO} appears directly at the output, but, V_{OSI} appears at the output as

$$V_{OSI}\frac{R_F}{R_{IN}},$$

see equation (2).

I_{OS}: is the offset current. This is the current at the input necessary to make the output zero. It is equal to the combined effect of the difference between the bias currents of A1 and A2 and the matching errors in the optical components, in the unipolar mode.

I_{REF1} and I_{REF2}: are the reference currents that, when connected to the inputs, enable bipolar operation. The two currents are trimmed, in the bipolar mode, to minimize the $I_{OS\ bipolar}$ error.

I_{D1} and I_{D2}: are the currents generated by each photodiode in response to the light from the LED.

A_e: is the gain error.

$A_e = |\text{Ideal gain}/\text{Actual gain}| - 1$

The output then becomes:

$$V_{OUT} = R_F\left[\left(\frac{V_{IN} \pm V_{OSI}}{R_{IN}} - I_{REF1} \pm I_{OS}\right)(1 + A_e) + I_{REF2}\right] \pm V_{OSO} \quad (2)$$

The total input referred offset voltage of the ISO100 can be simplified in the unipolar case by assuming that $A_e = 0$ and $V_{IN} = 0$:

$$V_{OUT} \approx R_F\left[\frac{\pm V_{OSI}}{R_{IN}} \pm I_{OS\ unipolar}\right] \pm V_{OSO} \quad (3)$$

This voltage is then referred back to the input by dividing by R_F/R_{IN}.

$$V_{OS\ (RTI)} = (\pm V_{OSI}) \pm R_{IN}\ (I_{OS\ unipolar}) + V_{OSO}/(R_F/R_{IN}) \quad (4)$$

Example 1: (Refer to Figure 2 and Electrical Specifications Table)

Given:
$$I_{OS\ bipolar} = +35nA$$
$$R_{IN} = 100k\Omega$$
$$R_F = 1M\Omega\ (\text{gain} = 10)$$
$$V_{OSI} = +200\mu V$$
$$V_{OSO} = +200\mu V$$

Find: The total offset voltage error referred to the input and output when $V_{IN} = 0V$.

V_{OS} total RTI

$= \{[\pm V_{OSI} \pm R_{IN}\ (I_{OS\ bipolar}) - R_{IN}\ (I_{REF\ 1})]$
$[1 + A_e] + R_{IN}\ I_{REF\ 2}\} \pm V_{OSO}/(R_F/R_{IN})$

$= \{[+200\mu V + 100k\Omega\ (35nA) - 100k\Omega\ (12.5\mu A)]$
$[1.02] + 100k\Omega\ (12.5\mu A)\} +$
$200\mu V/(1M\Omega/100k\Omega)$

$= \{[0.2mV + 3.5mV - 1.25V]$
$[1.02] + 1.25V\} + 0.02mV$

$= -21.2mV$

V_{OS} total RTO

$= V_{OS}$ total RTI $\times R_F/R_{IN}$

$= -21.2mV \times 10$

$= -212mV$

Note: This error is dominated by $I_{OS\ bipolar}$ and the reference current times the gain error (which appears as an offset). The error for unipolar operation is much lower. The error due to offset current can be zeroed using circuits shown in Figures 6 and 7. The gain error is adjusted by trimming either R_F or R_{IN}.

COMMON-MODE AND HIGH VOLTAGE ERRORS

Figure 3 shows a model of the ISO100 that can be used to analyze common-mode and high voltage behavior.

Definitions of CMR and IMR

I_{OS} is defined as the input current required to make the ISO100's output zero. CMRR and IMRR in the ISO100 are expressed as conductances. CMRR defines the relationship between a change in the applied common-mode voltage (V_{CM}) and the change in I_{OS} required to maintain the amplifier's output at zero:

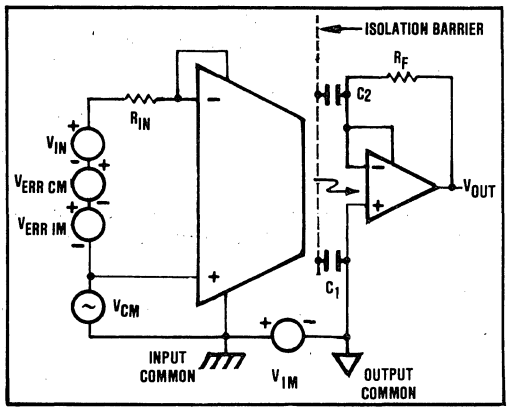


FIGURE 3. High Voltage Error Model.

$$\text{CMRR (I-mode)} = \Delta I_{OS}/\Delta V_{CM} \text{ in nA/V} \quad (5)$$

$$\text{CMRR (V-mode)} = \left[\frac{\Delta I_{OS}}{\Delta V_{CM}}\right] R_{IN} = \frac{\Delta V_{ERR\ CM}}{\Delta V_{CM}} \text{ in V/V} \quad (6)$$

IMRR defines the relationship between a change in the applied isolation mode voltage (V_{IM}) and the change in I_{OS} required to maintain the amplifier's output at zero:

$$\text{IMRR (I-mode)} = \frac{\Delta I_{OS}}{\Delta V_{IM}} \text{ in pA/V} \quad (7)$$

$$\text{IMRR (V-mode)} = \left[\frac{\Delta I_{OS}}{\Delta V_{IM}}\right] R_{IN} = \frac{\Delta V_{ERR\ IM}}{\Delta V_{IM}} \text{ in V/V} \quad (8)$$

CMRR & IMRR in V/V are a function of R_{IN}.

V_{IM} is the voltage between input common and output common.

V_{CM} is the common-mode voltage (noise that is present on both input lines, typically 60Hz).

V_{ERR} is the equivalent error signal, applied in series with the input voltage, which produces an output error identical to that produced by application of V_{CM} and V_{IM}.

CMRR and IMRR are the common-mode and isolation-mode rejection ratios, respectively.

TOTAL CAPACITANCE (C_1 and C_2) is distributed along the isolation barrier. Most of the capacitance is coupled to low impedance or noncritical nodes and affects only the leakage current. Only a small capacitance (C_2) couples to the input of the second stage, and contributes to IMRR.

Example 2: Refer to Figure 3 and Electrical Specification Table)

Given: V_{CM} = 1VAC peak at 60Hz, V_{IM} = 200VDC, CMRR = 3nA/V, IMRR = 5pA/V, R_{IN} = 100kΩ, R_F = 1MΩ (Gain = 10)

Find: The error voltage referred to the input and output when V_{IN} = 0V

$$V_{ERR\ RTI} = (V_{CM})(CMRR)(R_{IN}) + (V_{IM})(IMRR)(R_{IN})$$
$$= 1V\ (3nA/V)\ (100k\Omega) + 200V\ (5pA/V)(100k\Omega)$$
$$= 0.3mV + 0.1mV$$
$$= 0.4mV$$

$$V_{ERR\ RTO} = V_{ERR\ RTI}\ (R_F/R_{IN})$$
$$= 0.4mV\ (10)$$
$$= 4mV \text{ (with DC IMRR)}$$

(Note: This error is dominated by the CMRR term)

For purposes of comparing CMRR and IMRR directly with dB specifications, the following calculations can be performed:

$$\text{CMRR in V/V} = \text{CMRR (I-mode)}(R_{IN})$$
$$= 3nA/V\ (100k) = 0.3mV/V$$

$$\text{CMR} = 20\ \text{LOG}\ (0.3mV/V) = -70dB \text{ at } 60Hz$$

$$\text{IMRR in V/V} = \text{IMRR (I-mode)}(R_{IN}) = 5pA/V(100k\Omega) = 0.5\mu V/V$$

$$\text{IMR} = 20\ \text{LOG}\ (0.5 \times 10^{-6} V/V) = -126dB \text{ at DC}$$

Example 3:

In Example 2, V_{IM} is an AC signal at 60Hz and

$$\text{IMRR} = \frac{400pA}{V}$$

$$V_{ERR\ RTI} = V_{ERR\ CM} + V_{ERR\ IM}$$
$$= 0.3mV + 200V\ (400pA/V)(100k\Omega)$$
$$= 8.3mV$$
$$V_{ERR\ RTO} = 83mV \text{ (with AC IMRR)}$$

Example 4:

Given: Total error RTO from Examples 1 and 3 as 378mV worst case

Find: Percent error of +10V full scale output

$$\%\ \text{Error} = \frac{V_{ERR\ total}}{V_{FS}} \times 100$$
$$= \frac{378mV}{10V} \times 100$$
$$= 3.78\%$$

NOISE ERRORS

Noise errors in the unipolar mode are due primarily to the optical cavity. When the full 60kHz bandwidth is not needed, the output noise of the ISO100 can be limited by either a capacitor, C_F, in the feedback loop or by a low-pass filter following the output. This is shown in Figure 4. Noise in the bipolar mode is due primarily to the reference current sources, and can be reduced by the low-pass filters shown in Figure 5.

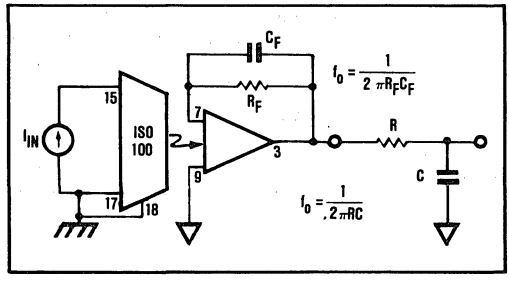


FIGURE 4. Two Circuit Techniques for Reducing Noise in the Unipolar Mode.

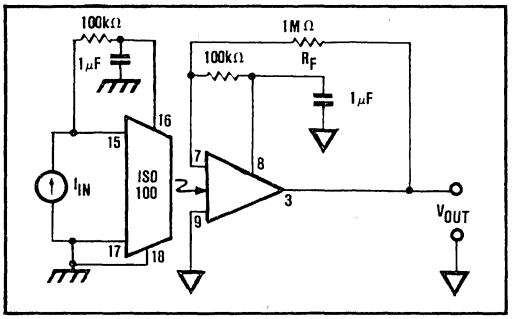


FIGURE 5. Circuit Technique for Reducing Noise from The Current Sources in the Bipolar-Mode.

OPTIONAL ADJUSTMENTS

There are two major sources of offset error: offset voltage and offset current. V_{OSI} and V_{OSO} of the input and output amplifiers can be adjusted independently using external potentiometers. An example is shown in Figure 17. Note that V_{OSO} (500μV, max) appears directly at the output, but V_{OSI} appears at the output multipled by gain (R_F/R_{IN}). In general, V_{OS} is small compared to the effect of I_{OS} (see Example I). To adjust for I_{OS} use a circuit which intentionally unbalances the offset in one direction and then allows for adjustment back to zero.

Figure 6 shows how to adjust unipolar errors at zero input. The unipolar amplifier can be used down to zero input if it is made to be "slightly bipolar." By sampling the reference current with R_5 and R_6 the minimum current required to keep the input stage in the linear region of operation can be established. R_7 and R_8 are adjusted to cancel the offset created in the input stage. This brings the output to zero, when the input is zero. Although the amplifier can now operate down to zero input voltage, it has only a small portion of the current drain and noise that the true bipolar configuration would have.

Adjusting the bipolar errors is illustrated in Figure 7. Each of the errors are adjusted in turn. With V_{IN} = "open,", I_{OS} is trimmed by adjusting R_{10} to make the output zero. R_G is then adjusted to trim the gain error. The effects of offset voltage are removed by adjusting R_{14}.

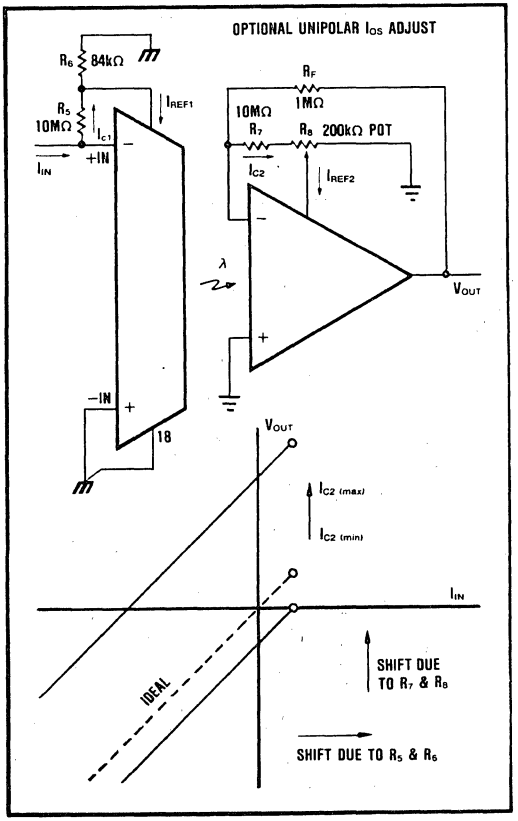


FIGURE 6. Adjusting the Unipolar Amplifier Errors at Zero Input.

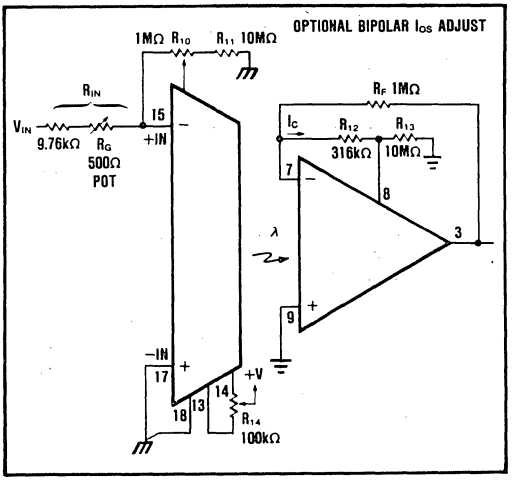


FIGURE 7. Adjusting the Bipolar Errors.

BASIC CIRCUIT CONNECTIONS

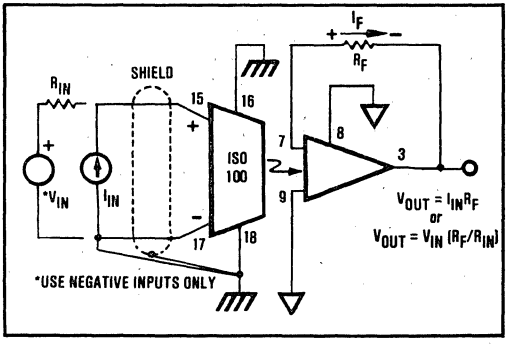


FIGURE 8. Unipolar Noninverting.

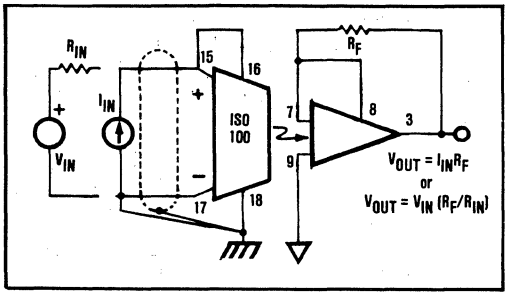


FIGURE 9. Bipolar Noninverting.

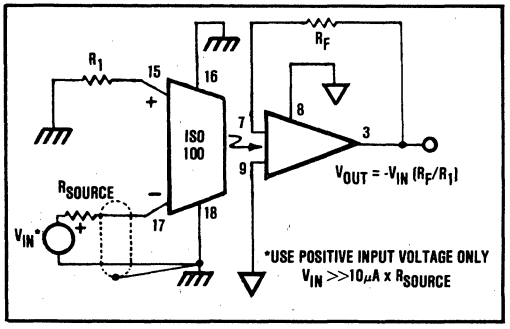


FIGURE 10. Unipolar Inverting.

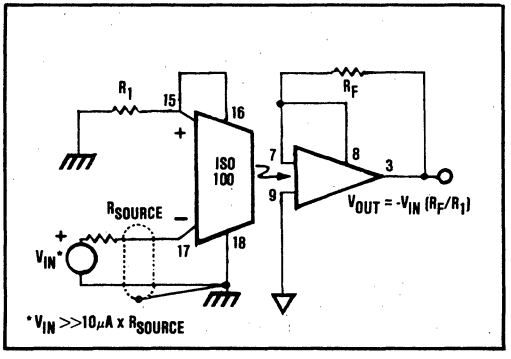


FIGURE 11. Bipolar Inverting.

APPLICATION INFORMATION

The small size, low offset and drift, wide bandwidth, ultra-low leakage, and low cost, make the ISO100 ideal for a variety of isolation applications. The basic mode of operation of the ISO100 will be determined by the type of signal and application.

Major points to consider when designing circuits with the ISO100.

1. Input Common (pin 18) and -IN (pin 17) should be grounded through separate lines. The Input Common can carry a large DC current and may cause feedback to the signal input
2. Use shielded or twisted pair cable at the input, for long lines.
3. Care should be taken to minimize external capacitance across the isolation barrier.
4. The distance across the isolation barrier, between external components, and conductor patterns, should be maximized to reduce leakage and arcing.
5. Although not an absolute requirement, the use of conformally-coated printed circuit boards is recommended.
6. When in the unipolar mode, the reference currents (pins 8 and 16) must be terminated. I_{IN} should be greater than 20nA to keep internal LED on.
7. The noise contribution of the reference currents will cause the bipolar mode to be noisier than the unipolar mode.
8. The maximum output voltage swing is determined by I_{IN} and R_F.

$$V_{SWING} = I_{IN_{max}} \times R_F$$

9. A capacitor (about 3pF) can be connected across R_F to compensate for peaking in the frequency response. The peaking is caused by the pole generated by R_F and the capacitance at the input of the output amplifier.

Figures 12 through 17 show applications of the ISO100.

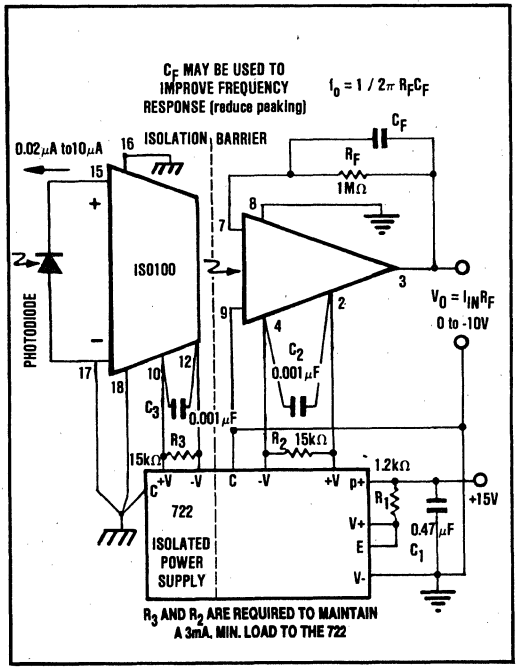
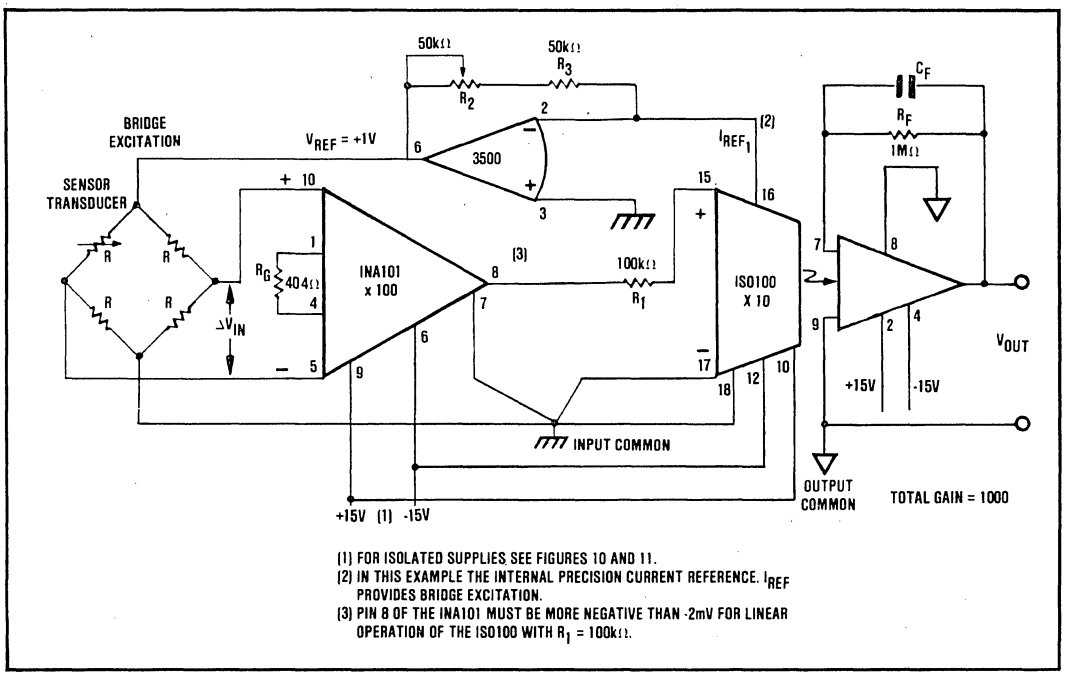


FIGURE 12. Two-Port Isolation Photodiode Amplifier Unipolar.



(1) FOR ISOLATED SUPPLIES SEE FIGURES 10 AND 11.
(2) IN THIS EXAMPLE THE INTERNAL PRECISION CURRENT REFERENCE. I_{REF} PROVIDES BRIDGE EXCITATION.
(3) PIN 8 OF THE INA101 MUST BE MORE NEGATIVE THAN -2mV FOR LINEAR OPERATION OF THE ISO100 WITH R_1 = 100kΩ.

FIGURE 13. Precision Bridge Isolation Amplifier (Unipolar).

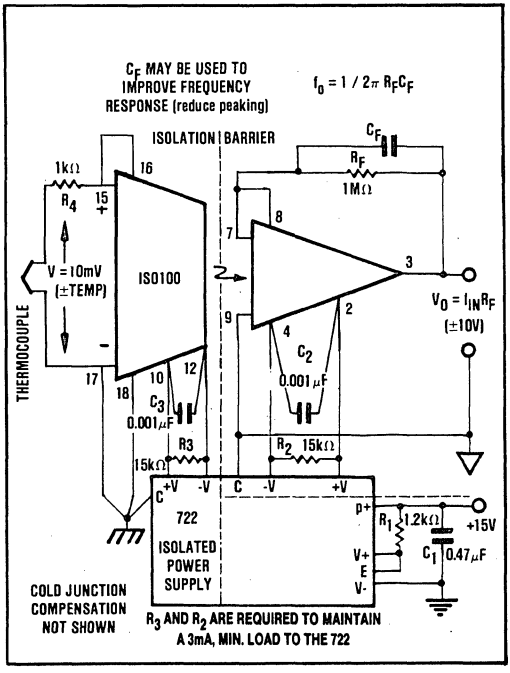


FIGURE 14. Three-Port Isolation Thermocouple Amplifier (Bipolar).

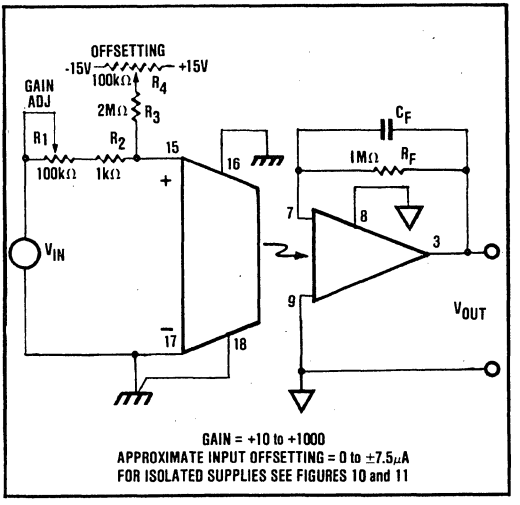


FIGURE 15. Isolated Test Equipment Amplifier (Unipolar with Offsetting).

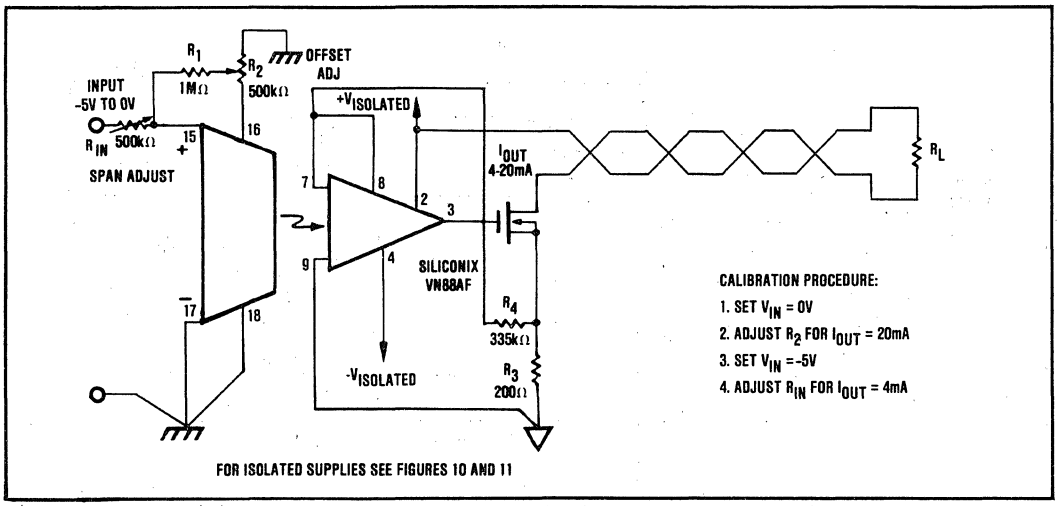


FIGURE 16. Isolated 4mA to 20mA Transmitter (Example of an isolated voltage controlled current source).

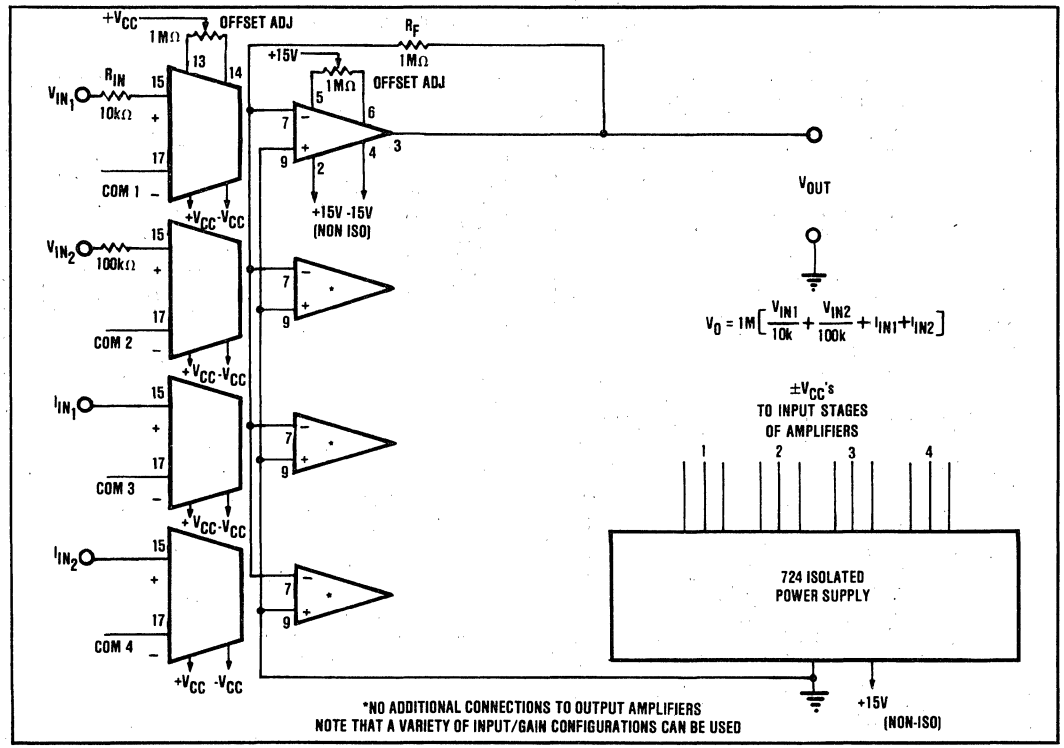


FIGURE 17. Four-Port Isolated Summing Amplifier (Unipolar).

EMI SHIELD

DESCRIPTION

The 100MS is an epoxy encapsulated electromagnetic electrostatic interference (EMI) shield for use with circuits where sensitivity to EMI is critical. It was designed to attenuate EMI by converting electromagnetic field energy into heat that is absorbed by the shield and by shunting electrostatic fields to common. The 100MS may be used in applications to either confine or exclude EMI. Its cavity was designed for 28.45mm x 28.45mm x 7.24mm, 20-pin hybrid packages. The shields in the cover and base plate are in two separate halves to maintain the electrical isolation between the adjacent rows of pins of the module it encloses. Because of the spacing between the shield halves and the epoxy flow holes, the 100MS provides a partial, but adequate low reluctance path for electromagnetic flux. The 100MS is well suited for use with isolation modules such as the Burr-Brown 3656, 722, and 724.

ASSEMBLY INSTRUCTIONS

Assemble the base plate to the module by pushing the pins of the module through the beveled holes in the base plate until the base plate and bottom of the module are in contact with each other. Place the cover over the module so the tabs are aligned and fit into the slots in the base plate. Bend the four wide shield soldering tabs protruding from the cover to make contact with the bare metal on the base plate. Solder these four tabs to insure the integrity of their connection to the base plate.

The 100MS and the module it contains are mounted and secured to a printed circuit board (PCB) by soldering the two narrow PCB solder tabs to the appropriate common. The PCB solder tab closest to the input side of the module should be soldered to the input common. The other tab should be soldered to the output common. Figure 2 illustrates the assembly of the 100MS.

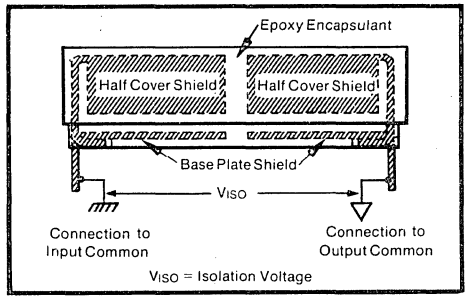


FIGURE 1. Cross-Sectional Side View of 100MS.

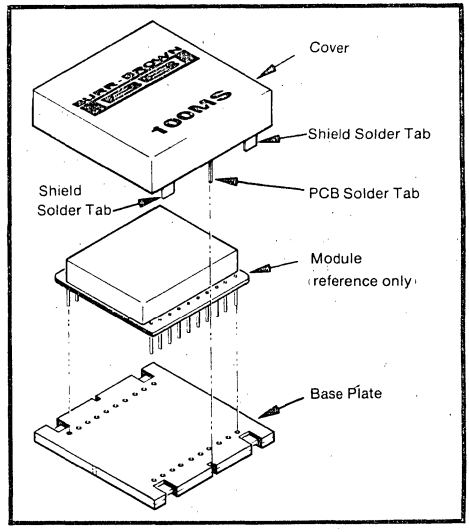


FIGURE 2. Assembly Diagram.

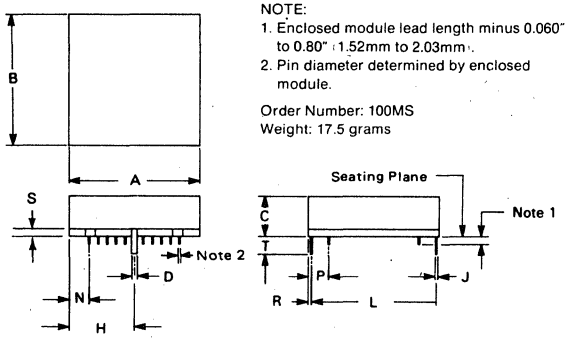
SPECIFICATIONS

ELECTRICAL - Specifications apply between solder tabs.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Isolation Voltage					
Rated Continuous, DC		3500			VDC
Rated Continuous, AC		2000			V, rms
Test	10 seconds	8000			VDC
Capacitance			5		pF
Resistance			10^{10}		Ω
Leakage Current	120V, 60Hz		0.23		μA

NOTE: Temperature changes (ΔT/Δt) greater than 1°C per minute below 0°C and long term storage above 100°C are not recommended.

MECHANICAL



NOTE:
1. Enclosed module lead length minus 0.060" to 0.80" (1.52mm to 2.03mm).
2. Pin diameter determined by enclosed module.

Order Number: 100MS
Weight: 17.5 grams

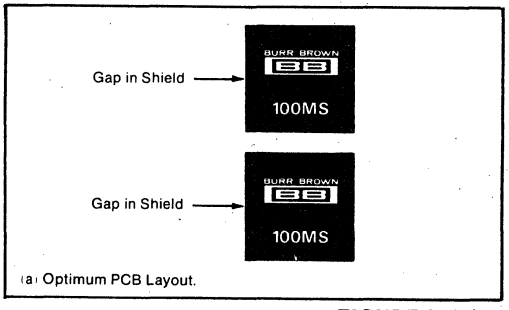
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.320	1.380	33.53	35.05
B	1.320	1.380	33.53	35.05
C	.350	.450	8.89	11.43
D	.040	.060	1.02	1.52
H	.600	.700	15.24	17.78
J	.015	.025	0.38	0.64
L	1.180	1.280	29.97	32.51
N	.150	.250	3.81	6.35
P	.150	.250	3.81	6.35
R	.015	.055	0.38	1.40
T	.130	.230	3.30	5.84
S	.060	.080	1.52	2.03

APPLICATIONS INFORMATION

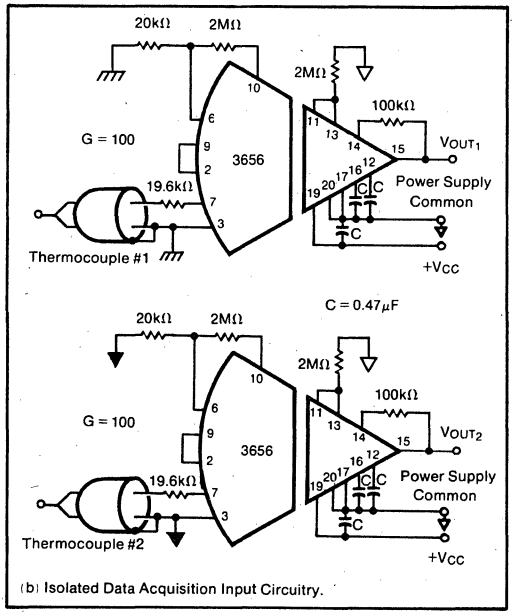
MULTIPLE DEVICE ORIENTATION

A typical application for the 100MS is shown in Figure 3. Using multiple devices within 30mm of each other can cause them to interact by forming beat frequency interference outputs. The 100MS can reduce this interference by as much as a factor of 200:1 depending on the distance between the devices and their relative orientation.

Minimum EMI results when the gaps of both shields are paralleled as in Figure 3a.



(a) Optimum PCB Layout.



(b) Isolated Data Acquisition Input Circuitry.

FIGURE 3. Orientation for Minimum EMI.

BURR-BROWN®

3450
3451
3452
3455

Precision Linear ISOLATION AMPLIFIERS

FEATURES

- 2000V ISOLATION (3452)
- 160dB ISOLATION-MODE REJECTION
- DIFFERENTIAL INPUT
- 0.005% GUARANTEED GAIN LINEARITY (3450)
- 1μV/°C INPUT VOLTAGE DRIFT(3450)
- 20pA INPUT BIAS CURRENT (3452)
- PRECISION WIRE-WOUND RESISTORS FOR LONG TERM STABILITY
- LOW INTERFERENCE PICKUP - PW MODULATION

APPLICATIONS

- GROUND-LOOP ELIMINATION
- OFF-GROUND SIGNAL MEASUREMENTS
- MEDICAL INSTRUMENTATION
- PATIENT MONITORING
- INDUSTRIAL PROCESS CONTROL
- DATA ACQUISITION
- HIGH VOLTAGE MEASUREMENTS
- FAULT PROTECTION

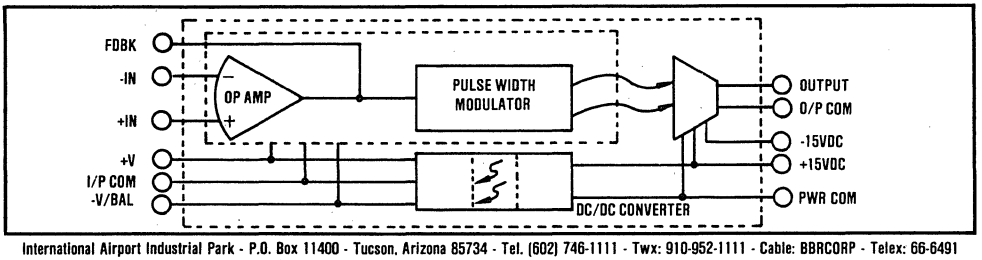
DESCRIPTION

The models 3450, 3451, and 3452 are operational amplifiers with the unique feature of having the output completely isolated from the input. This is accomplished by a high accuracy modulation demodulation stage which isolates the input from the output by $10^{12}\Omega$ in parallel with 12pF of coupling capacitance and provides gain linearity and stability far superior to that offered by ordinary isolation amplifiers.

These devices differ from other isolation amplifiers in several respects. They are true differential input operational amplifiers whereas other commercially available isolation amplifiers are simple unity-gain isolators or are capable of a few fixed gains. Thus they can be connected in all of the common op amp feedback circuits such as summing, inverting, differentiating, etc.

The 3452 differs from the 3450 and 3451 in that it has higher isolation voltage (2000V vs 500V) and has isolated ±15VDC power available at the input.

The 3450 and 3451 differ from each other primarily in their input stage characteristics. The 3450 has a low drift (1μV °C) bipolar transistor input stage while the 3451 has a low bias current (25pA)FET transistor input stage. The 3455 is identical to the 3452 except for additional isolation specifications more well suited for medical applications.



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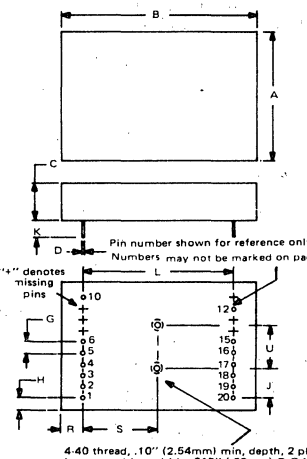
SPECIFICATIONS

ELECTRICAL

Typical at 25°C and ±15VDC unless otherwise noted.

MODEL	3450	3451	3452/3455[1]	UNITS
INPUT[2]				
Open-Loop Gain, min	94	88	94	dB
Input Offset Voltage at 25°C[3], max	±0.55	±20	±0.30	mV
vs Temperature, max	±1.0	±50	±5.0	µV/°C
vs. Supply	±50	±50	±25	µV/V
vs. Time	±10	±100		µV/mo
Input Bias Current at 25°C, max	±50	-0.025	-0.02	nA
vs Temperature, max	±0.5	doubles/10°C		nA/°C
vs. Supply	±0.2	±0.001		nA/V
Input Offset Current at 25°C	±30, max	±0.002		nA
vs Temperature max	±0.3	doubles/10°C		nA/°C
vs. Supply	±0.1	±0.0005		nA/V
Input Impedance				
Differential	10^7	10^{11}		Ω
Common-mode[4]	5×10^9 ‖ 10	10^{11} ‖ 10		Ω ‖ pF
Input Noise				
Voltage, 0.01Hz to 10Hz	0.8	2	4	µV, p-p
10Hz to 1kHz	1.2	3	2	µV, rms
Current, 0.01Hz to 10Hz	30	0.3	0.3	pA, p-p
10Hz to 1kHz	50	0.6	0.6	pA, rms
Input Voltage Range				
Common-mode[4] (operating), min		±10		V
Differential (w/o damage), min		±15		V
Common-mode Rejection[4] at 10V	100	80	90	dB
Isolated Power Available				
Voltage	--	--	±15 +0, -10%	V
Current, max	--	--	±10	mA
Ripple at 100kHz	--	--	100	mV, p-p
ISOLATION				
Gain (without trimming), max[3] 1V/V	±0.1	±0.5		%
vs Temperature, max	±10	±50		ppm/°C
Nonlinearity[5] at ±10V, max/typ	±.005/±0.0015	±0.025/±.005	±0.025/±.005	%
Frequency Response, -3dB (see Fig. 9)	1.5	2.5		kHz
Settling Time				
to 0.01%		5		msec
to 0.1%		1		msec
Isolation Impedance[6]		10^{12} ‖ 16		Ω ‖ pF
Isolation Leakage Current				
at 240V/60Hz, max		2.5[6]		µA
Isolation-mode Rejection[6]				
DC, min		160		dB
60Hz, min		120		dB
Isolation Voltage[6]				
Rated; continuous, min	±500	±2000		V, pk
Test Voltage[7]	±2000	±5000		V, pk[11]
OUTPUT				
Output Voltage, min		±10		V
Output Current, min		±5		mA
Output Impedance, DC		0.2		Ω
Output Noise				
0.01Hz to 10Hz		7		µV, p-p
10Hz to 1kHz		25		µV, rms
Output Offset Voltage at 25°C[3], max	±2	±5	±5	mV
vs Temperature, max		±100		µV/°C
vs. Supply		±500		µV/V
vs. Time		±100		µV/mo
Input Power Requirements				
Voltage		±14 to ±16		VDC
Current, quiescent, max		+30/-5		mA
Current, full load, max	+35/-10		+55/-10	mA[8]
TEMPERATURE RANGE				
Specification		-25 to +85		°C
Storage		-55 to +125		°C
Operating		-25 to +85		°C

MECHANICAL



NOTE:
Leads in true position within .015" (.38mm) R @ MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.250	2.310	57.15	58.67
B	3.480	3.510	87.63	89.15
C	.650	.710	16.51	18.03
D	.038	.042	0.97	1.07
G	.200 BASIC		5.08 BASIC	
H	.200	.300	5.08	7.62
J	.525 BASIC		13.34 BASIC	
K	.170	.350	4.32	8.89
L	2.700 BASIC		68.58 BASIC	
R	.350	.450	8.89	11.43
S	1.350 BASIC		34.29 BASIC	
U	.750 BASIC		19.05 BASIC	

MATERIAL: Black Plastic
WEIGHT: 100g (3.5 oz.)
MATING CONNECTOR: 4400MC

NOTES:
1. The 3455 is identical to the 3452 except for two additional specifications. Each unit is tested to withstand a 2500V, rms, 60Hz sine wave isolation voltage (Ref. Dielectric Withstand Voltage, paragraph 31.11 of UL544). Each unit is specified at a maximum leakage current of 2µA with 240V, rms, 60Hz isolation voltage (Ref. Leakage Current, paragraph 27.5 of UL544).
2. For 3450 and 3451 current drawn from FDBK pin must be ≤ 5mA. For 3452 the sum of the current drawn from FDBK pin and either "-V/Bal" or "+V" pins (i.e., + or - isolated current) must be ≤ 11mA.
3. Errors may be trimmed to zero.
4. Common-mode parameters are measured at the +IN and -IN pins with respect to the I/P COM pin.
5. Nonlinearity is specified to be the peak deviation from a best straightline expressed as a percent of peak-to-peak full scale output.
6. Isolation-mode parameters are measured at the I/P COM pin with respect to the PWR COM pin and O/P COM pin.
7. All units 100% tested for 1µA max leakage current at test voltage.
8. Includes fully loaded input power.

BURR-BROWN®

3650
3652

Optically-Coupled Linear ISOLATION AMPLIFIERS

FEATURES

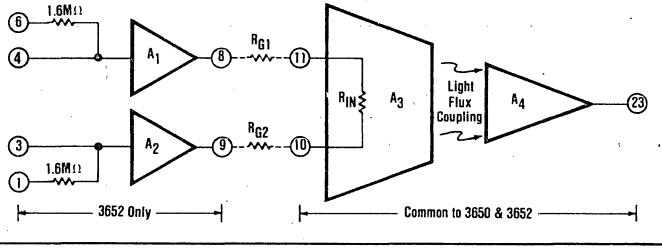
- BALANCED INPUT
- LARGE COMMON-MODE VOLTAGES
  - ±2000V Continuous
  - 140dB Rejection
- ULTRA LOW LEAKAGE
  - 0.35μA max at 240V/60Hz
  - 1.8pF Leakage Capacitance
- EXCELLENT GAIN ACCURACY
  - 0.05% Linearity
  - 0.05%/1000Hours Stability
- WIDE BANDWIDTH
  - 15kHz ±3dB
  - 1.2V/μsec Slew Rate

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- DATA ACQUISITION
- INTERFACE ELEMENT
- BIOMEDICAL MEASUREMENTS
- PATIENT MONITORING
- TEST EQUIPMENT
- CURRENT SHUNT MEASUREMENT
- GROUND-LOOP ELIMINATION
- SCR CONTROLS

DESCRIPTION

The 3650 and 3652 are optically coupled integrated circuit isolation amplifiers. Prior to their introduction commercially available isolation amplifiers had been modular or rack mounted devices using transformer coupled modulation demodulation techniques. Compared to these earlier isolation amplifiers the 3650 and 3652 have the advantage of smaller size, lower cost, wider bandwidth and integrated circuit reliability. Also, because they use a DC analog modulation technique as opposed to a carrier type technique, they avoid the problems of electromagnetic interference (both transmitted and received) that most of the modular isolation amplifiers exhibit.



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SPECIFICATIONS

ELECTRICAL

Typical at 25°C and ±15VDC supply voltages unless otherwise noted.

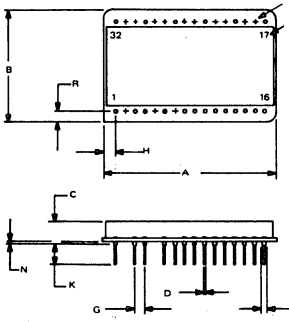
MODEL	3650MG/HG[1]	3650JG	3650KG	3652MG/HG[1]	3652JG
ISOLATION					
Isolation Voltage					
Rated Continuous, (min)			2000Vp or VDC		
Test Voltage, (min) 10sec duration			5000Vp		
Isolation-Mode Rejection, G = 10					
DC			140dB		
60Hz, 5000Ω source unbalance			120dB		
Leakage Current, 240V/60Hz			0.35μA, max		
Isolation Impedance					
Capacitance			1.8pF		
Resistance			$10^{12}\Omega$		
GAIN					
Gain Equation					
for current sources	$G_I = 10^6$ Volt/Amp			$G_I = 1.0057 \times 10^6$ Volt/Amp[2]	
for voltage sources	$G_V = \frac{10^6}{R_{G1} + R_{G2} + R_{IN}}$ V/V			$\frac{10^6}{R_{G1} + R_{G2} + R_{IN} + R_O}$ V/V	
Input Resistance, R_{IN}, max	25Ω			25Ω	
Buffer Output Impedance, R_O	Not applicable			90Ω ±30Ω	
Gain Equation Error, max[3]	1.5%	0.5%	0.5%	1.5%[4]	0.5%[4]
Gain Nonlinearity	±0.05% typ. ±0.2% max	±0.03% typ. ±0.1% max	±0.02% typ. ±0.05% max	±0.05% typ. ±0.2% max	±0.05% typ. ±0.1% max
Gain vs Temperature	300ppm/°C	100ppm/°C	50ppm/°C	300ppm/°C[4]	200ppm/°C[4]
Gain vs Time	±0.05%/1000hrs.			±0.05%/1000hrs.	
Frequency Response					
Slew Rate	0.7V/μsec min, 1.2V/μsec typ.				
±3dB Frequency	15kHz				
Settling Time					
to ±0.01%	400μsec				
to ±0.1%	200μsec				
INPUT STAGE[5]					
Input Offset Voltage					
at 25°C, max[3]	±5mV	±1mV	±0.5mV	±5mV	±2mV
vs Temperature, max	±25μV/°C	±10μV/°C	±5μV/°C	±50μV/°C	±25μV/°C
vs Supply	100μV/V			100μV/V	
vs Time	50μV/1000 hrs.			100μV/1000 hrs.	
Input Bias Current					
at 25°C	10nA typ, 40nA max			10pA typ, 50pA max	
vs Temperature	0.3nA/°C			doubles every +10°C	
vs Supply	0.2nA/V			1pA/V	
Input Offset Current				10pA	
vs Temperature	effects included			doubles every 10°C	
vs Supply	in output offset			1pA/V	
Input Impedance					
Differential	"R_{IN}" = 25Ω max			$10^{11}\Omega$	
Common-mode	$10^9\Omega$			$10^{11}\Omega$	
Input Noise					
Voltage, 0.05Hz to 100Hz	8μV, p-p			4μ, p-p	
10Hz to 10kHz	4μV, rms			5μV, rms	
Input Voltage Range					
Common-mode, linear operation,	±(|V| -5)V			±(|V| -5)	
w/o damage, at +,-	±V			±V	
at +I, -I	Not applicable [6]			±300V for 10msec[7]	
at +IR, -IR	Not applicable [6]			±3000V for 10msec[7]	
Differential, w/o damage, at +, -	±V			±V	
Differential, w/o damage, at +I, -I	Not applicable			±600V for 10msec[7]	
Differential, w/o damage, at +IR, -IR	Not applicable			±6000V for 10msec[7]	
Common-mode Rejection, 60Hz	90dB at 60Hz, 5kΩ imbalance			80dB at 60Hz, 5kΩ imbalance	
Power Supply (Input Stage Only)					
Voltage (at "+V" and "-V"	±8V to±18V			±8V to ±18V	
Current					
Quiescent	±1.2mA [8]			±3mA [8]	
with ±10V output[7]	+6.5mA or -6.5mA, typ			+8.5mA or -8.5mA, typ	
	+12mA or -12mA, max			+16mA or -16mA, max	

ELECTRICAL (cont)

MODEL	3650MG/HG[1]	3650JG	3650KG	3652MG/HG[1]	3652JG
OUTPUT STAGE					
Output Voltage, min		±10V		±10V	
Output Current, min		±5mA		±5mA	
Output Offset Voltage					
at 25°C max[3]	±25mV	±10mV	±10mV	±25mV	±10mV
vs Temperature, max	±900μV/°C	±450μV/°C	±300μV/°C	±900μV/°C	±450μV/°C
vs Supply		±500μV/V		±500μV/V	
vs Time		±1mV/1000hrs		±1mV/1000hrs	
Output Noise Voltage					
0.05Hz to 100Hz		50μV, p-p		50μV, p-p	
10Hz to 1kHz		65μV, rms		65μV, rms	
Power Supply (Output Stage Only)					
Voltage ("+V_{CC}" and "-V_{CC}")		±8V to ±18V			
Current					
Quiescent		±2.3mA typ, ±6mA max			
with ±5mA output, max		±11mA			
TEMPERATURE[9]					
Specification		0°C to 85°C			
Operating		-40°C to +100°C			
Storage		-55°C to +125°C			

1. All electrical and mechanical specifications of the 3650MG and 3652MG are identical to the 3650HG and 3652HG, respectively, except that the following specifications apply to the 3650MG and 3652MG: (a) Isolation test voltage duration incrased from 10sec minimum to 60sec minimum; (b) Input offset voltage at 25°C max: ±10mV; vs temp. max: ±100μV/°C; (c) Output offset voltage at 25°C max: ±50mV; vs temp. max: ±1.8mV/°C.
2. If used as 3650, see Installation and Operating Instructions.
3. Trimmable to zero.
4. Gain error terms specified for inputs applied through buffer amplifiers (i.e., ±1 or ±IR pins).
5. Input stage specifications at +1 and −1 inputs for 3652 unless otherwise noted.
6. Maximum safe input current at either input is 10mA.
7. Continuous rating is 1/3 pulse rating.
8. Load current is drawn from one supply lead at a time; other supply current at quiescent level. For 3652 add 0.2mA/V of positive CMV.
9. dT/dt > 1°C/minute below 0°C, and long-term storage above 100°C is not recommended. Also limit the repeated thermal cycles to be within the 0°C to +85°C temperature range.

MECHANICAL



"+" denotes missing pins.

Pin numbers shown for reference only Numbers may not be marked on package.

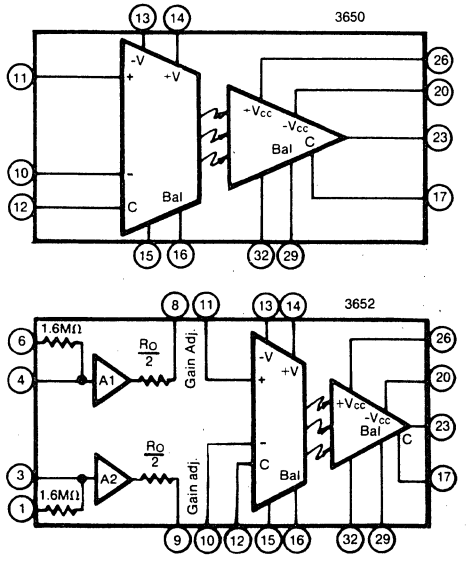
NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

ORDER NUMBER:
3650MG 3652MG
3650HG 3652HG
3650JG 3652JG
3650KG

MATERIAL: Alumina (ceramic)
WEIGHT: 14 grams (0.5 oz)
MATING CONNECTOR: 2302MC (set of two, 16-pin strips)

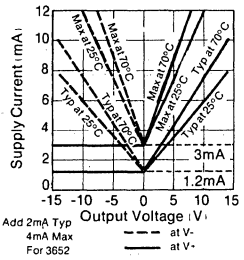
PIN CONNECTIONS



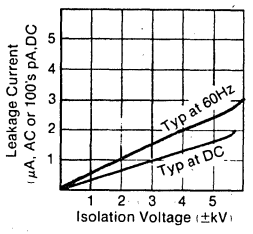
TYPICAL PERFORMANCE CURVES

Typical at 25°C and ±15VDC power supplies unless otherwise noted.

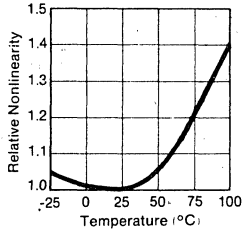
INPUT STAGE SUPPLY CURRENT VS. OUTPUT VOLTAGE



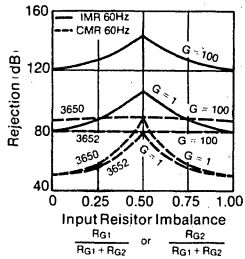
ISOLATION LEAKAGE CURRENT VS. ISOLATION VOLTAGE



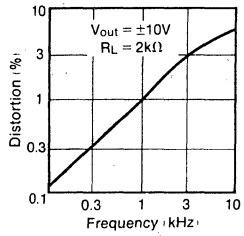
NORMALIZED LINEARITY VS. TEMPERATURE



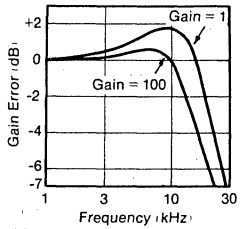
REJECTION VS. RESISTOR IMBALANCE



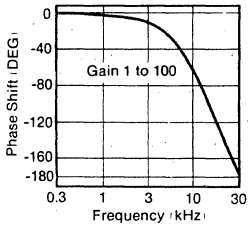
DISTORTION VS. FREQUENCY



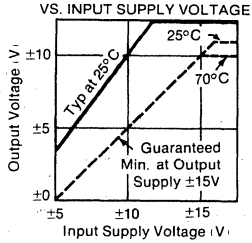
GAIN ERROR VS. FREQUENCY



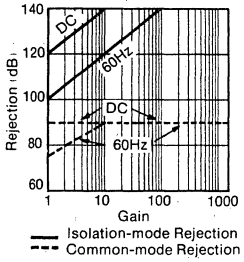
PHASE SHIFT VS. FREQUENCY



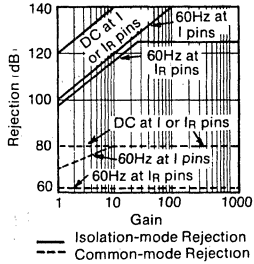
OUTPUT VOLTAGE SWING VS. INPUT SUPPLY VOLTAGE



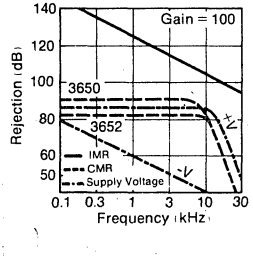
3650 COMMON-MODE AND ISOLATION-MODE REJECTION VS. GAIN



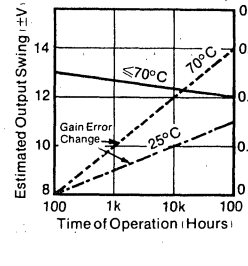
3652COMMON-MODE AND ISOLATION-MODE REJECTION VS. GAIN



REJECTION VS. FREQUENCY



OUTPUT VOLTAGE AND GAIN ERROR VS. TIME



DEFINITIONS

ISOLATION-MODE VOLTAGE, V_{ISO}

The isolation-mode voltage is the voltage which appears across the isolation barrier, i.e., between the input common and the output common. (See Figure 1.)

Two isolation voltages are given in the electrical specifications: "rated continuous" and "test voltage". Since it is impractical on a production basis to test a "continuous" voltage (infinite test time is implied), it is generally accepted practice to test at a significantly higher voltage for some reasonable length of time. For the 3650 and the 3652 the "test voltage" is equal to 1000V plus two times the "rated continuous" voltage. Thus, for a continuous rating of 2000V each unit is tested at 5000V.

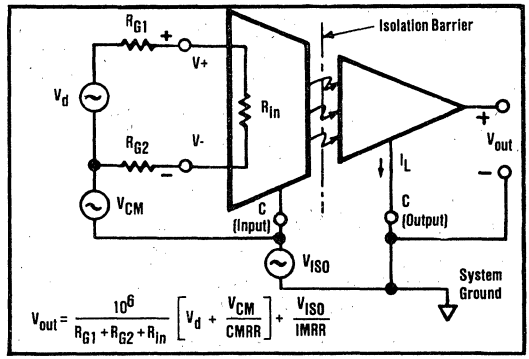


FIGURE 1. Illustration of Isolation-mode and Common-mode Specifications.

COMMON-MODE VOLTAGE, V_{CM}

The common-mode voltage is the voltage midway between the two inputs of the amplifier measured with respect to input common. It is the algebraic average of the voltage applied at the amplifiers' input terminals. In the circuit in Figure 5, $(V_+ + V_-)/2 = V_{CM}$. (Note: Many applications involve a large system "common-mode voltage." Usually in such cases the term defined here as "V_{CM}" is negligible and the system "common-mode voltage" is applied to the amplifier as "V_{ISO}" in Figure 1.)

ISOLATION-MODE REJECTION

The isolation-mode rejection is defined by the equation in Figure 1. The isolation-mode rejection is not infinite because there is some leakage across the isolation barrier due to the isolation resistance and capacitance.

NONLINEARITY

Nonlinearity is specified to be the peak deviation from a best straightline, expressed as a percent of peak-to-peak full scale output (i.e., ±10mV at 20V p-p ≈ 0.05%).

THEORY OF OPERATION

Prior to the introduction of the 3650 family optical isolation had not been practical in linear circuits. A single LED and photodiode combination, while useful in a wide range of digital isolation applications, has fundamental limitations - primarily nonlinearity and instability as a function of time and temperature.

The 3650 and 3652 use a unique technique to overcome the limitations of the single LED and photodiode isolator. Figure 2 is an elementary equivalent circuit for the 3650 which can be used to understand the basic operation without consideration the cluttering details of offset adjustment and biasing for bipolar operation.

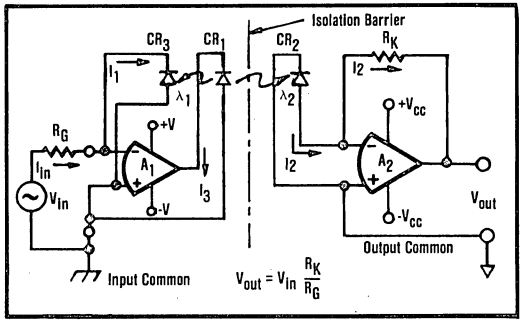


FIGURE 2. Simplified Equivalent Circuit of Linear Isolator.

Two matched photodiodes are used--one in the input (CR_3) and one in the output stage (CR_2) - - to greatly reduce nonlinearities and time - temperature instabilities. Amplifier A_1, LED CR_1, and photodiode CR_3 are used in a negative feedback configuration such that $I_1 = I_{in} \cdot R_G$ (where R_G is the user supplied gain setting resistor). Since CR_2 and CR_3 are closely matched and since they receive equal amounts of light from the LED CR_1 (i.e., $\lambda_1 = \lambda_2$), $I_2 = I_1 = I_{in}$. Amplifier A_2 is connected as a current-to-voltage converter with $V_{out} = I_2 R_K$ where R_K is an internal 1MΩ scaling resistor. Thus the overall transfer function is:

$$V_{out} = V_{in} \frac{10^6}{R_G}, \ (R_G \text{ in ohms})$$

This improved isolator circuit overcomes the primary limitations of the single LED and photodiode combination. The transfer function is now virtually independent of any degradation in the LED output as long as the two photodiodes and optics are closely matched*. Linearity is now a function of the accuracy of the matching and is further enhanced by the use of negative feedback in the input stage. Advanced laser trimming techniques are used to further compensate for residual matching errors.

*The only effect of decreased LED output is a slight decrease in full scale swing capability. See Typical Performance Curves.

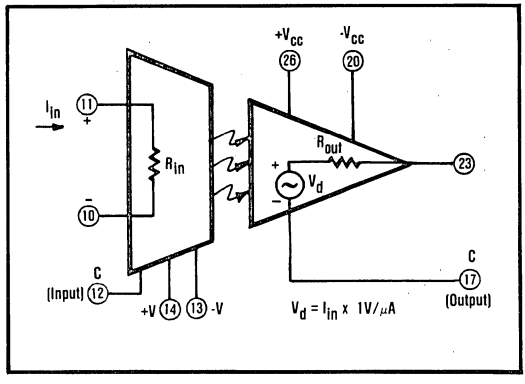


FIGURE 3. Simple Model of 3650.

A model of the 3650 suitable for simple circuit analysis is shown in Figure 3. The output is a current dependent voltage source, V_d, whose value depends on the input current. Thus, the 3650 is a transconductance amplifier with a gain of one volt per microamp. When voltage sources are used the input current is derived by using gain setting resistors in series with the voltage source (see Installation and Operating Instructions for details). R_{in} is the differential input impedance. The common-mode and isolation impedances are very high and are assumed to be infinite for this model.

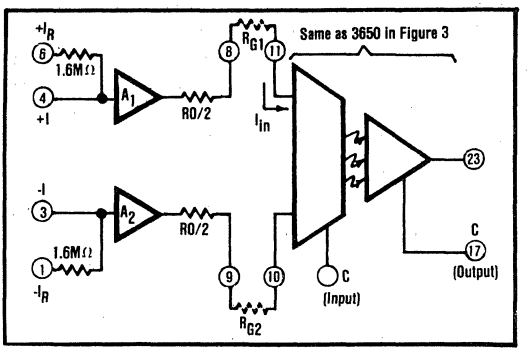


FIGURE 4. Simple Model of 3652.

A simplified model of the 3652 is shown in Figure 4. The isolation and output stages are identical to the 3650. Additional input circuitry consisting of FET buffer amplifiers and input protection resistors have been added to give higher differential and common-mode input impedance ($10^{11}\Omega$), lower bias currents (50pA) and overvoltage protection. The +IR and -IR inputs have a 10msec pulse rating of 6000V differential and 3000V common-mode (see Definitions for a discussion of common-mode and isolation-mode voltages.) The addition of the buffer amplifiers also creates a voltage-in voltage-out transfer function with the gain set by R_{G1} and R_{G2}.

INSTALLATION & OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

The power supply connections for the 3650 and 3652 are shown in Figure 5. When a DC/DC converter is used for isolated power it is placed in a parallel with the isolation barrier of the amplifier. This can lower the isolation impedance and degrade the isolation-mode rejection of the overall circuit. Therefore, a high quality, low leakage DC/DC converter such as the Burr-Brown Model 722 should be used.

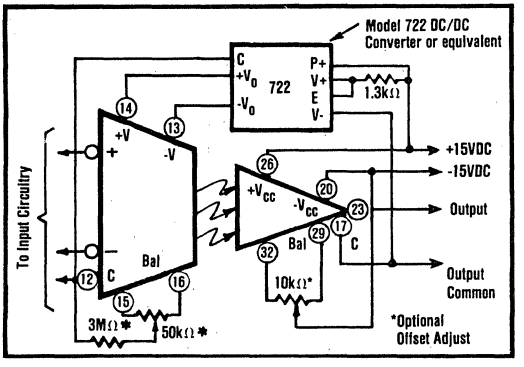


FIGURE 5. Power and Offset Adjust Connections.

OFFSET VOLTAGE ADJUSTMENTS

The offset nulling circuits are identical for the 3650 and 3652 and are shown in Figure 5. The offset adjust circuitry is optional and the units will meet the stated specifications with the BAL terminals unconnected. Provisions are available to null both the input and output stage offsets. If the amplifier is operated at a fixed gain, normally only one adjustment will be used; the output stage (10kΩ adjustment) for low gains and the input stage (50kΩ adjustment) for high gains.(>10).

Use the following procedure if it is desired to null both input and output components (for example, if the gain of the amplifier is to be switched). The input stage offset is first nulled (50kΩ adjustment) with the appropriate input signal pins connected to input common and the amplifier set at its maximum gain. The gain is then set to its minimum value and the output offset is nulled (10kΩ adjustment).

INPUT CONFIGURATIONS

Some possible input configurations for the 3650 and 3652 are shown in Figures 6a, 6b, 6c. Differential input sources are used in these examples. For situations with non-differential inputs the appropriate source term should be set to zero in the gain equations and replaced with a short in the diagrams.

Figure 6a shows the 3650 connected as a transconductance amplifier with input current sources. Voltage sources are shown in Figure 6b. In this case the voltages are converted to currents by R_{G1} and R_{G2}. As shown by the equations, they perform as gain setting resistors in the voltage transfer function. When a single voltage source is used it is recommended (but not essential) that the gain setting resistor remain split into two equal halves in order to minimize errors due to bias currents and common-mode rejection (see Typical Performance Curves).

Figure 6c illustrates the connections for the 3652 when the FET buffer amplifiers A_1 and A_2 are used. This configuration provides an isolation amplifier with high input impedance (both common-mode and differential) and good common-mode and isolation-mode rejection. It is a true isolated instrumentation amplifier which has many benefits for noise rejection when source impedance imbalances are present.

In the 3652 the voltage gain of the buffer amplifiers is slightly less than unity, but the gain of the output stage has been raised to compensate for this so that the overall transfer function from the ±I or ±IR inputs to the output is correct. It should be noted that A_1 and A_2 are buffer amplifiers. No summing can be done at the ±I or ±IR inputs. Figure 6c shows the +I and -I inputs used. If more input voltage protection is desired, then the +IR and −IR inputs should be used. This will increase the input noise due to the contribution from the 1.6MΩ resistors, but will provide additional differential and common-mode protection (10msec rating of 3kV).

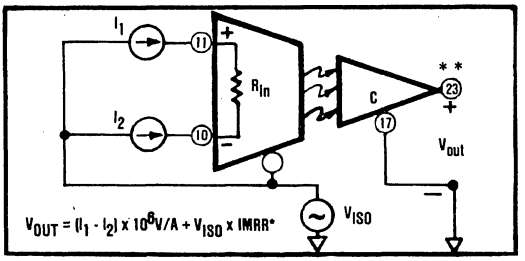


FIGURE 6a. 3650 With Differential Current Sources.

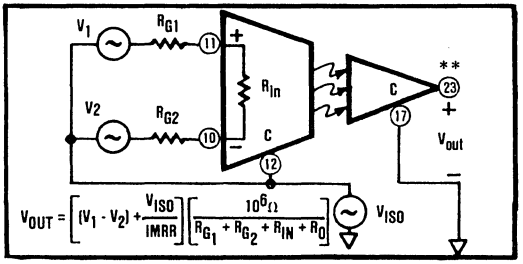


FIGURE 6b. 3650 With Differential Voltage Source.

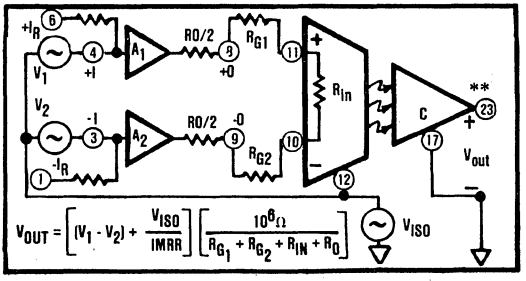


FIGURE 6c. 3652 with Differential Voltage Source.

*IMRR here is in pA V, typically 5pA V at 60Hz and 1pA V at DC.
**The offset adjustment circuitry and power supply connections have been omitted for simplicity. Refer to Figure 5 for details.

ERROR ANALYSIS

A model of the 3650 suitable for DC error analysis of offset voltage, voltage drift versus temperature, bias current, etc., is shown in Figure 7.

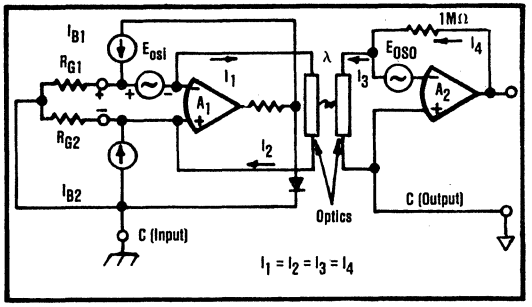


FIGURE 7. DC Error Analysis Model for 3650.

A_1 and A_2, the input and output stage amplifiers, are considered to be ideal. Separate external generators are used to model the offset voltages and bias currents. R_{in} is assumed to be small relative to R_{G1} and R_{G2} and is therefore omitted from the gain equation. The feedback configuration, optics and component matching are such that $I_1 = I_2 = I_3 = I_4$. A simple circuit analysis gives the following expression for the total output error voltage due to offset voltages and bias currents.

$$V_{out\text{-}total} = \frac{10^6}{R_{G1} + R_{G2}} \left[E_{osi} + (I_{B1} R_{G1} - I_{B2} R_{G2})\right] + E_{oso} \quad (1)$$

Offset current is defined as the difference between the two bias currents I_{B1} and I_{B2}. If $I_{B1} = I_B$ and $I_{B2} = I_B + I_{os}$, then, for $R_{G1} = R_{G2}$, $V_{out} - I_B = \frac{10^6 \cdot I_{os}}{2}$.

This component of error is not a function of gain and is therefore included as a part of E_{oso} specifications. The output errors due to the output stage bias current are also included in E_{oso}. This results in a very simple equation for the total error:

$$V_{out\text{-}total} = \frac{10^6 E_{osi}}{2R_{G1}} + E_{oso} \text{ (for } R_{G1} = R_{G2}). \quad (2)$$

In summary it should be noted that equation (2) should be used only when $R_{G1} = R_{G2}$. When $R_{G1} \neq R_{G2}$, equation (1) applies.

The effects of temperature may be analyzed by replacing the offset terms with their corresponding temperature gradient terms:

$V_{out} \rightarrow \Delta V_{out}$ ΔT, $E_{osi} \rightarrow \Delta E_{osi}$ ΔT, etc.

For a complete analysis of the effects of temperature, gain variations must also be considered.

OUTPUT NOISE

The total output noise is given by

$$E_n (RMS) = \sqrt{(E_{nI} G)^2 + (E_{nO})^2}$$

where E_n (RMS) = total output noise
E_{nI} = RMS noise of the input stage
E_{nO} = RMS noise of the output stage
$G = 10^6 (R_{G1} + R_{G2})$

E_{nO} includes the noise contribution due to the optics and the noise currents of the output stage. Errors created by the noise current of the input stage are insignificant compared to other noise sources and are therefore omitted.

COMMON-MODE and ISOLATION-MODE REJECTION

The expression for the output error due to common-mode and isolation mode voltage is:

$$V_{out} = G\left[\frac{V_{cm}}{CMRR} + \frac{V_{iso}}{IMRR}\right]$$

GUARDING & PROTECTION

To preserve the excellent inherent isolation characteristics of these amplifiers, the following recommended practice should be noted:

1. Use shielded, twisted pair of cable at the input as with any instrumentation amplifier;
2. Care sould be taken to minimize external capacitance. A symmetrical layout of external components to achieve balanced capacitance from the input terminals to output common will preserve high IMR;
3. External components and conductor patterns should be at a distance equal to or greater than the distance between the input and output terminals, to prevent HV breakdown.
4. Though not an absolute requirement, the use of laminated or conformally coated printed circuit boards is recommended.

APPLICATIONS

Figure 8 shows a system where isolation amplifiers (3650) are used to measure the armature current and the armature voltage of a motor.

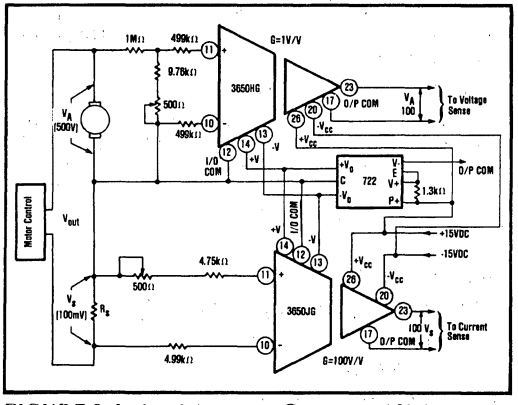


FIGURE 8. Isolated Armature Current and Voltage Sensor.

The armature current of the motor is converted to a voltage by the calibrated shunt R, and then amplifier (adjustable gain) and isolated by the 3650.

The armature voltage is sensed by the voltage divider (adjustable) shown and then amplified and isolated by the 3650.

The 3650 provides the advantage of accurate current measurement in the presence of high common-mode voltage. Both 3650's provide the advantage of isolating the motor ground from the control system ground. Isolated power is provided by an isolated DC DC converter (BB Model 722 or equivalent).

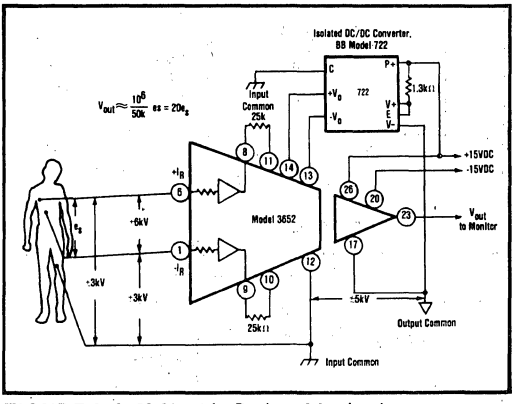


FIGURE 9. 3652 Used in Patient Monitoring Application (ECG, VCG, EMG Amplifier).

The 3652 is ideally suited for patient monitoring applications as shown in Figure 9. The fact that it is a true balanced input instrumentation amplifier with very high differential and common-mode inpedance means that it can greatly reduce the common-mode noise pick up due to imbalance in lead impedances that often appear in patient monitoring situations. The 3kV and 6kV shown in Figure 9 are the 10msec pulse ratings of the +IR and -IR inputs for the common-mode and differential input voltages with respect to input common. The rating of the isolation barrier is 2000V, pk continuous. The non-recurrent pulse rating of the isolation barrier is 5000V, pk since each unit is factory tested at 5000V, pk. If the isolation barrier is to be subjected to higher voltages a gas filled surge voltage protection device can be used. For multichannel operation, two 3562's can be powered by one Model 722 isolated DC/DC converter. The total leakage current for both channels at 240V/60Hz would still be less than 2μA.

The block diagram in Figure 10 shows the use of isolation amplifiers in SCR control application.

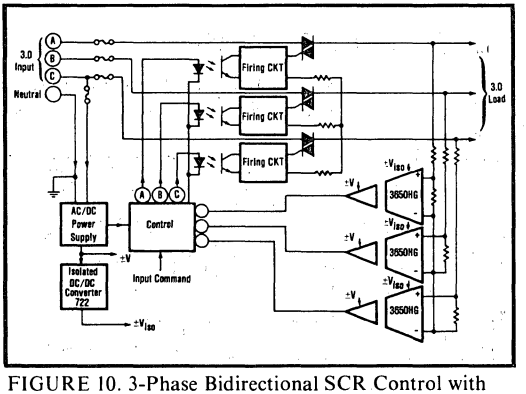


FIGURE 10. 3-Phase Bidirectional SCR Control with Voltage Feedback.

BURR-BROWN®

3656

Integrated Circuit - Transformer Coupled ISOLATION AMPLIFIER

FEATURES

- INTERNAL ISOLATED POWER
- 8000V ISOLATION TEST VOLTAGE
- 0.5μA MAX LEAKAGE AT 120V, 60Hz
- 3-PORT ISOLATION
- 125dB REJECTION AT 60Hz
- 1" x 1" x 0.25" CERAMIC PACKAGE

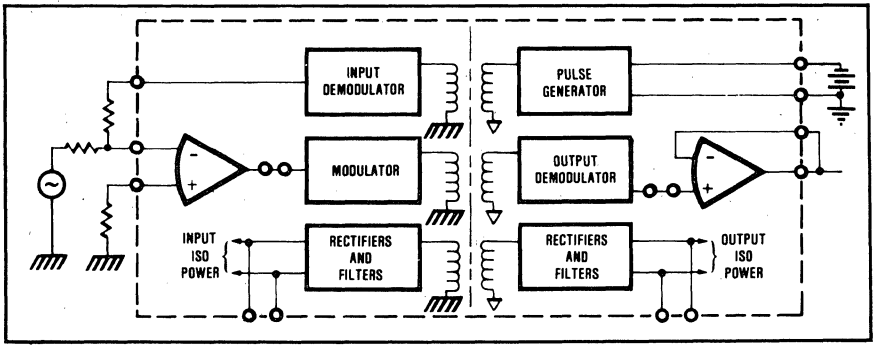
APPLICATIONS

- MEDICAL
  Patient monitoring and diagnostic instrumentation
- INDUSTRIAL
  Ground loop elimination and off-ground signal measurement
- NUCLEAR
  Input/output/power isolation

DESCRIPTION

The 3656 is the first amplifier to provide a total isolation function ... both signal and power isolation ... in integrated circuit form. This remarkable advancement in analog signal processing capability is accomplished by use of a patented modulation technique and minature hybrid transformer.

Versatility and performance are outstanding features of the 3656. It is capable of operating with three completely independent grounds (three-port isolation). In addition, the isolated power generated is available to power external circuitry at either the input or output. The uncommitted op amps at the input and the output allow a wide variety of closed-loop configurations to match the requirements of many different types of isolation applications.



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THEORY OF OPERATION

Details of the 3656 are shown in Figure 1. The external connections shown, place it in its simplest gain configuration - unity gain, noninverting. Several other amplifier gain configurations and power isolation configurations are possible. See Installation and Operating Instructions and Applications sections for details.

Isolation of both signal and power is accomplished with a single miniature toroid transformer with multiple windings. A pulse generator operating at approximately 750kHz provides a two-part voltage waveform to transformer T_1. One part of the waveform is rectified by diodes D_1 through D_4 to provide the isolated power to the input and output stages (+V, -V and V+, V-). The other part of the waveform is modulated with input signal information by the modulator operating into the V_2 winding of the transformer.

The modulated signal is coupled by windings W_6 and W_7 to two matched demodulators - one in the input stage and one in the output stage - which generate identical voltages at their outputs, pins 10 and 11 (voltages identical with respect to their respective commons, pins 3 and 17). In the input stage the input amplifier A_1, the modulator and the input demodulator are connected in a negative feedback loop. This forces the voltage at pin 6 (connect as shown in Figure 1) to equal the input signal voltage applied at pin 7. Since the input and the output demodulators are matched and produce identical output voltages, the voltage at pin 11 (referenced to pin 17, the output common) is equal to the voltage at pin 10 (referenced to pin 3, the input common). In the output stage, output amplifier A_2 is connected as a unity gain buffer, thus the output voltage at pin 15 equals the output demodulator voltage at pin 11. The end result is an isolated output voltage at pin 15 equal to the input voltage at pin 7 with no galvanic connection between them.

Several amplifier and power connection variations are possible:

1. The input stage may be connected in various operational amplifier gain configurations.
2. The output stage may be operated at gains above unity.
3. The internally generated isolated voltages which provide power to A_1 and A_2 may be overridden and external supply voltages used instead.

Versatility and its three independent isolated grounds allow simple solutions to demanding analog signal conditioning problems. See the Installation and Operating Instructions and Applications sections for details.

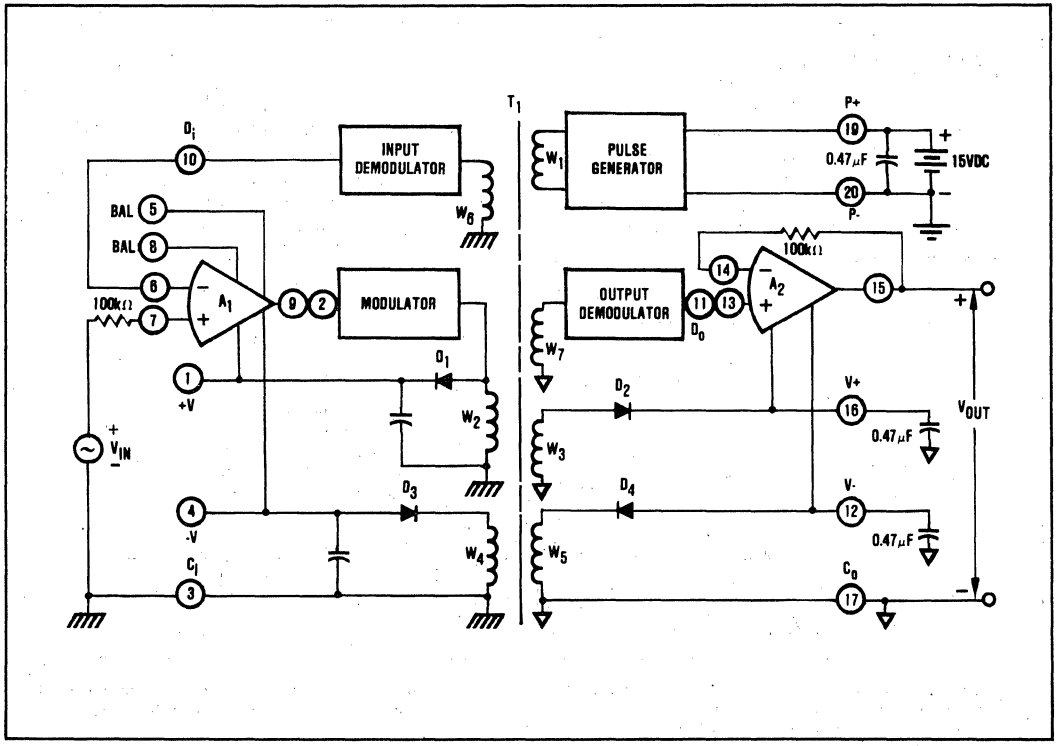


FIGURE 1. Block Diagram.

SPECIFICATIONS

ELECTRICAL

At +25°C, V± = 15VDC and 15VDC between P+ and P-, unless otherwise noted.

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG			UNITS
		MIN	TYP	MAX	
ISOLATION					
Voltage					
Rated Continuous(1), DC		3500 (1000)			VDC
Rate Continuous(2), AC		2000 (700)			V, rms
Test, 10sec(1)		8000 (3000)			VDC
Rejection	G_1 = 10V/V				
DC			160		dB
60Hz, < 100Ω in I/P Com(2)			125		dB
60Hz, 5kΩ in I/P Com(2)					
3656HG		108			dB
3656AG, BG, JG, KG		112			dB
Capacitance(1)			6.0 (6.3)		pF
Resistance(1)			10^{12} (10^{12})		Ω
Leakage Current	120V, 60Hz		0.28	0.5	μA
GAIN					
Equations	See Text				
Accuracy of Equations					
Initial(3) 3656HG	G < 100V/V			1.5	%
3656AG, JG, KG				1.0	%
3656BG				0.3	%
vs. Temperature 3656HG				480	ppm/°C
3656AG, JG				120	ppm/°C
3656BG, KG				60	ppm/°C
vs. Time			0.02 (1 + log khrs.)		%
Nonlinearity	$R_A + R_F = R_B \geq 2M\Omega$				
External Supplies used at					
pins 12 and 16, 3656HG	Unipolar or Bipolar Output			±0.15	%
3656AG, JG, KG				±0.1	%
3656BG				±0.05	%
Internal Supplies used for	Bipolar Output Voltage				
Output Stage	Swing, Full Load(4)		±0.15		%
OFFSET VOLTAGE(5)	RTI				
Initial(3), 3656HG	15V_P between P+ and P-			±(4 + 40/G_1)	mV
3656AG, JG				±(2 + 20/G_1)	mV
3656BG, KG				±(1 + 10/G_1)	mV
vs. Temperature, 3656HG				±(200 + 1000/G_1)	μV/°C
3656JG				±(50 + 750/G_1)	μV/°C
3656AG				±(25 + 500/G_1)	μV/°C
3656KG				±(10 + 350/G_1)	μV/°C
3656BG				±(5 + 350/G_1)	μV/°C
vs. Supply Voltage	Supply between P+ and P-				
3656HG				±(0.6 + 3.5/G_1)	mV/V
3656AG, BG, JG, KG				±(0.3 + 2.1/G_1)	mV/V
vs. Current(6)			±(0.1 + 10/G_1)	±(0.2 + (20/G_1))	mV/mA
vs. Time			±(10 + 100/G_1) x (1 + log khrs.)		μV
AMPLIFIER PARAMETERS	Apply to A1 and A2				
Bias Current(7)					
Initial				100	nA
vs. Temperature			0.5		nA/°C
vs. Supply			0.2		nA/V
Offset Current(7)			5	20	nA
Impedance	Common-mode		100 ‖ 5		MΩ ‖ pF
Input Noise Voltage	f_B = 0.05Hz to 100Hz		5		μV, p-p
	f_B = 10Hz to 10kHz		5		μV, rms
Input Voltage Range(8)					
Linear Operation	Internal Supply			±5	V
	External Supply			Supply -5V	V
Without Damage	Internal Supply			±8	V
	External Supply			Supply	V
Output Current	V_{OUT} = ±5V				
	±15V External Supply	±5			mA
	Internal Supply	±2.5			mA
	V_{OUT} = ±10V				
	±15V External Supply	±2.5			mA
	V_{OUT} = ±2V, $V_{P+, P-}$ = 8.5V				
	Internal Supply		±1		mA
Quiescent Current			150	450	μA

ELECTRICAL (CONT)

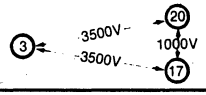
At +25°C, V± = 15VDC and 15VDC between P+ and P-, unless otherwise noted.

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG			UNITS
		MIN	TYP	MAX	
FREQUENCY RESPONSE					
±3dB Response	Small Signal		30		kHz
Full Power			1.3		kHz
Slew Rate	Direction measured at output	+0.1, -0.04			V/μsec
Settling Time	to 0.05%		500		μsec
OUTPUT					
Noise Voltage (RTI)	f_B = 0.05Hz to 100Hz		$\sqrt{(5)^2 + (22/G_1)^2}$		μV, p-p
	f_B = 10Hz to 10kHz		$\sqrt{(5)^2 + (11/G_1)^2}$		μV, rms
Residual Ripple[9]			5		mV, p-p
POWER SUPPLY IN	at P+, P-				
Rated Performance			15		VDC
Voltage Range[10]	Derated Performance	8.5		16	VDC
Ripple Current[9]			10	25	mA, p-p
Quiescent Current[11]	Average		14	18	mA, DC
Current vs. Load Current[12]	vs. Currents from +V, -V, V+, V-		0.7		mA/mA
ISOLATED POWER OUT	at +V, -V, V+, V- pins[13]				
Voltage, no load	15V between P+ and P-	8.5	9.0	9.5	V
Voltage, full load	±5mA (10mA sum) load[12]	7.0	8.0	9.0	V
Voltage vs. Power Supply	vs. Supply between P+ and P-		0.66		V/V
Ripple Voltage[9]					
No load			40		mV, p-p
Full load	±5mA load		80	200	mV, p-p
TEMPERATURE RANGE					
Specification 3656AG, BG		-25		+85	°C
3656HG, JG, KG		0		+70	°C
Operation[10]		-55		+100	°C
Storage[14]		-65		+125	°C

NOTES:

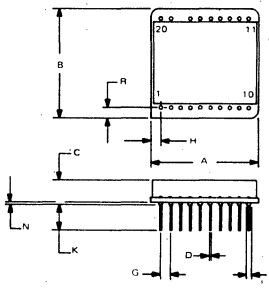
1. Ratings in parenthesis and between P- (pin 20) and O/P Com (pin 17). Other isolation ratings are between I/P Com and O/P Com or I/P Com and P-.

An example of the ratings for 3-port continuous isolation.



2. May be improved with proper shielding. See Performance Curves.
3. May be trimmed to zero.
4. If output swing is unipolar, or if the output is not loaded, specification same as if external supply were used.
5. Includes effects of A_1 and A_2 offset voltages and bias currents if recommended resistors used.
6. Versus the sum of all external currents drawn from V+, V-, +V, -V (= ISO).
7. Effects of A_1 and A_2 bias currents and offset currents are included in Offset Voltage specifications.
8. With respect to I/P Com (pin 3) for A_1 and with respect to O/P Com (pin 17) for A_2. CMR for A_1 and A_2 is 100dB, typical.
9. In configuration of Figure 3. Ripple frequency approximately 750kHz. Measurement bandwidth is 30kHz.
10. Decreases linearly from 16VDC at 85°C to 12VDC at 100°C.
11. Instantaneous peak current required from pins 19 and 20 at turn-on is 100mA for slow rising voltages (50msec) and 300mA for fast rises (50μsec).
12. Load current is sum drawn from +V, -V, V+, V- (= I_{ISO}).
13. Maximum voltage rating at pins 1 and 4 is ±18VDC; maximum voltage rating at pins 12 and 16 is ±18VDC.
14. Isolation ratings may degrade if exposed to 125°C for more than 1000 hours or 90°C for more than 50,000 hours.

MECHANICAL



CASE: Ceramic
MATING CONNECTOR: None
WEIGHT: 10 grams (0.35 oz.)

PINS: Pin material and plating composition to conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.080	1.120	27.43	28.45
B	1.080	1.120	27.43	28.45
C	.235	.300	5.97	7.62
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.350	3.81	8.89
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.100 BASIC		2.54 BASIC	

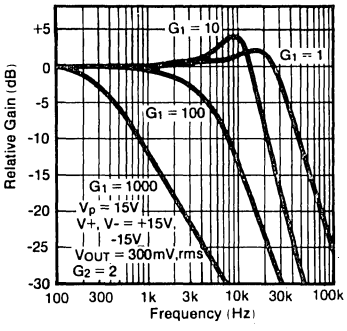
PIN DESIGNATIONS

1.	+V	11.	OUTPUT DEMOD
2.	MOD INPUT	12.	V-
3.	INPUT DEMOD COM	13.	A_2 NONINVERTING INPUT
4.	-V	14.	A_2 INVERTING INPUT
5.	BALANCE	15.	A_2 OUTPUT
6.	A_1 INVERTING INPUT	16.	V+
7.	A_1 NONINVERTING INPUT	17.	OUTPUT DEMOD COM
8.	BALANCE	18.	NO PIN
9.	A_1 OUTPUT	19.	P+
10.	INPUT DEMOD	20.	P-

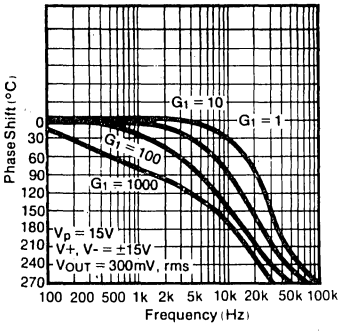
TYPICAL PERFORMANCE CURVES

All specifications typical at +25°C unless otherwise noted.

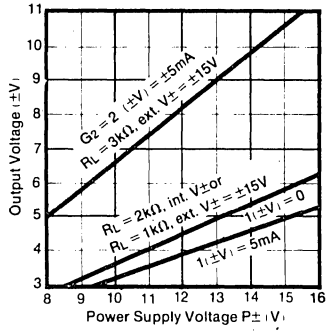
SMALL SIGNAL FREQUENCY RESPONSE



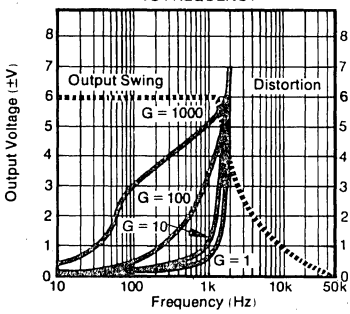
PHASE RESPONSE



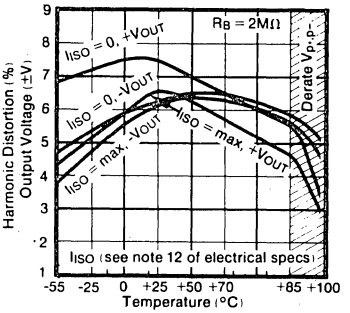
OUTPUT SWING VS SUPPLY VOLTAGE



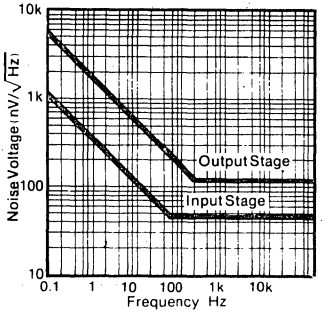
OUTPUT SWING AND DISTORTION VS FREQUENCY



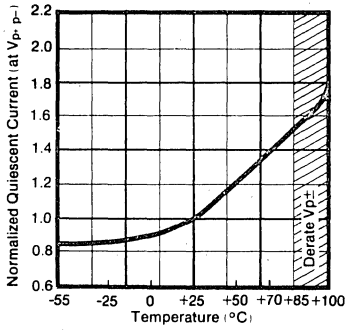
OUTPUT VOLTAGE SWING VS TEMPERATURE AND ISOLATED SUPPLY LOAD



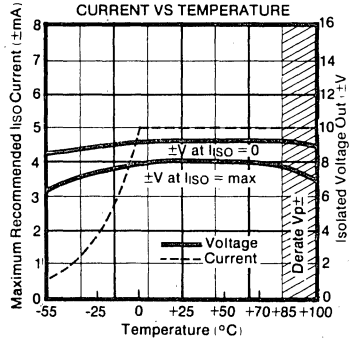
NOISE VOLTAGE VS FREQUENCY



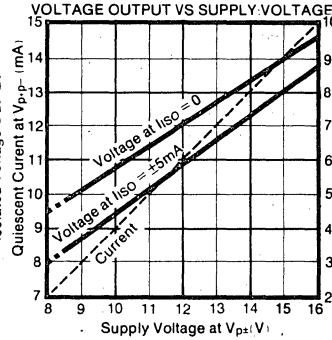
QUIESCENT CURRENT VS TEMPERATURE



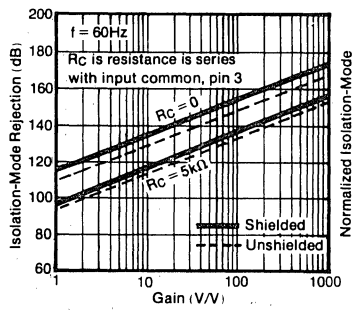
ISOLATED OUTPUT VOLTAGE AND CURRENT VS TEMPERATURE



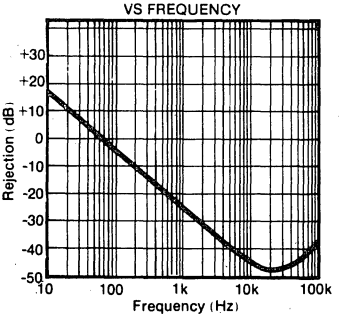
QUIESCENT CURRENT AND ISOLATED VOLTAGE OUTPUT VS SUPPLY VOLTAGE



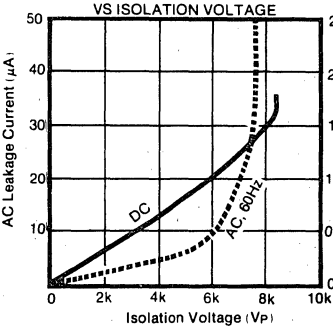
ISOLATION-MODE REJECTION VS GAIN



ISOLATION-MODE REJECTION VS FREQUENCY



AC AND DC LEAKAGE CURRENT VS ISOLATION VOLTAGE



INSTALLATION AND OPERATING INSTRUCTIONS

The 3656 is a very versatile device capable of being used in a variety of isolation and amplification configurations. There are several fundamental considerations that determine configuration and component value constraints:

1. Consideration must be given to the load placed on the resistance (pin 10 and pin 11) by external circuitry. Their output resistance is 100kΩ and a load resistor of 2MΩ or greater is recommended to prevent a voltage divider loading effect in excess of 5%.
2. Demodulator loadings should be closely matched so their output voltages will be equal. (Unequal demodulator output voltages will produce a gain error.) At the 2MΩ level, a matching error of 5% will cause an additional gain error of 0.25%.
3. Voltage swings at demodulator outputs should be limited to 5V. The output may be distorted if this limit is exceeded. This constrains the maximum allowed gains of the input and output stages. Note that the voltage swings at demodulator outputs are tested with 2MΩ load for a minimum of 5V.
4. Total current drawn from the internal isolated supplies must be limited to less than ±5mA per supply and limited to t total of 10mA. In other words, the combination of external and internal current drawn from the internal circuitry which feeds the +V, -V, V+ and V- pins should be limited to 5mA per supply (total current to +V, -V, V+ and V- limited to 10mA). The internal filter capacitors for ±V are 0.01μF. If more than 0.1mA is drawn to provide isolated power for external circuitry (see Figure 12), additional capacitors are required to provide adequate filtering. A minimum of 0.1μF/mA is recommended.
5. The input voltage at pin 7 (noninverting input to A_1) must not exceed the voltage at pin 4 (negative supply voltage for A_1) in order to prevent a possible lockup condition. A low leakage diode connected between pins 7 and 4, as shown in Figure 2, can be used to limit this input voltage swing.
6. Impedances seen by each amplifier's + and - input terminals should be matched to minimize offset voltages caused by amplifier input bias currents. Since the demodulators have a 100kΩ output resistance, the amplifier input not connected to the demodulator should also see 100kΩ.
7. All external filter capacitors should be mounted as close to the respective supply pins as is possible in order to prevent excessive ripple voltages on the supplies or at the output. (Optimum spacing is less than 0.5". Ceramic capacitors recommended.)

POWER AND SIGNAL CONFIGURATIONS

NOTE: Figures 2, 3 and 4 are used to illustrate both signal and power connection configurations. In the circuits shown, the power and signal configurations are independent so that any power configuration could be used with any signal configuration.

ISOLATED POWER CONFIGURATIONS

The 3656 is designed with isolation between the input, the output, and the power connections. The internally generated isolated voltages supplied to A_1 and A_2 may be overridden with external voltages greater than the internal supply voltages. These two features of 3656 provide a great deal of versatility in possible isolation and power supply hook-ups. When external supplies are applied, the rectifying diodes (D_1 through D_4) are reverse biased and the internal voltage sources are decoupled from the amplifiers (see Figure 1). Note that when external supplies are used, they must never be lower than the internal supply voltage.

Three-Port

The power supply connections in Figure 2 show the full three-port isolation configuration. The system has three separate grounds with no galvanic connections between them. The two external 0.47μF capacitors at pins 12 and 16 filter the rectified isolated voltage at the output stage. Filtering on the input stage is provided by internal capacitors. In this configuration continuous isolation voltage ratings are: 3500V between pins 3 and 17; 3500V between pins 3 and 19; 1000V between pins 17 and 19.

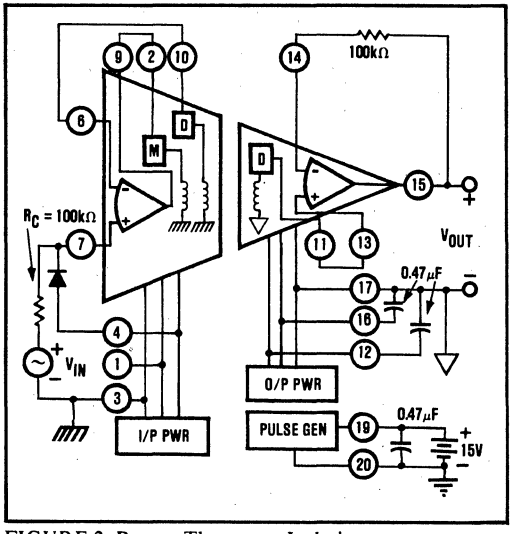


FIGURE 2. Power: Three-port Isolation;
Signal: Unity-gain Noninverting.

Two-Port - Bipolar Supply

Figure 3 shows two-port isolation which uses an external bipolar supply with its common connected to the output stage ground (pin 17). One of the supplies (either + or - could be used) provides power to the pulse generator (pins 19 and 20). The same sort of configuration is possible with the external supplies connected to the input stage. With the connection shown, filtering at pins 12 and 16 is not required. In this configuration continuous isolation voltage rating is: 3500VDC between pins 3 and 17; not applicable between pins 17 and 19; 3500VDC between pins 3 and 19.

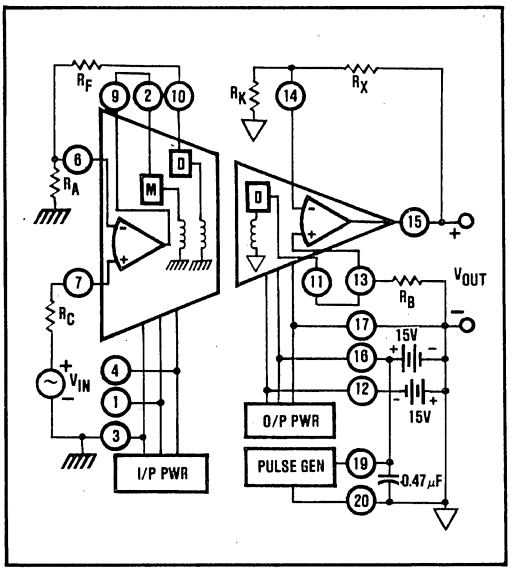


FIGURE 3. Power: Two-port, Dual Supply; Signal: Noninverting Gain.

Two-Port Single Supply

Figure 4 demonstrates two-port isolation using a single polarity supply connected to the output common (pin 17). The other polarity of supply for A_2 is internally generated (thus the filtering at pin 12). This isolated power configuration could be used at the input stage as well and either polarity of supply could be employed. In this configuration continuous isolation voltage rating is: 3500V between pins 3 and 17; 3500V between pins 3 and 19; not applicable between pins 17 and 19.

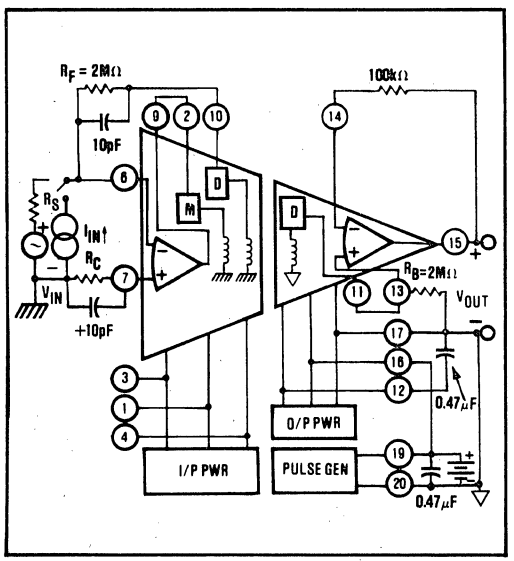


FIGURE 4. Power: Two-port, Single Supply; Signal: Inverting Gains.

SIGNAL CONFIGURATIONS

Unity Gain Noninverting

The signal path portion of Figure 2 shows the 3656 in its simplest gain configuration: unity gain noninverting. The two 100kΩ resistors provide balanced resistances to the inverting and noninverting inputs of the amplifiers. The diode prevents latch up in case the input voltage goes more negative than the voltage at pin 4.

Noninverting With Gain

The signal path portion of Figure 3 demonstrates two additional gain configurations: gain in the otuput stage and noninverting gain in the input stage. The following equations apply:

Total amplifier gain:

$$G = G_1 \bullet G_2 = V_{OUT}/V_{IN} \quad (1)$$

Input Stage:

$G_1 = 1 + (R_F/R_A)$ (Select G_1 to be less than 5V/full scale V_{In} to limit demodulator output to 5V) (2)

$R_A + R_F \geq 2M\Omega$ (Select to load input demodulator with at least 2MΩ) (3)

$$R_C = R_A \parallel (R_F + 100k\Omega) = \frac{R_A (R_F + 100k\Omega)}{R_A + R_F + 100k\Omega}$$

(Balance impedances seen by the + and - inputs of A_1 to reduce input offset caused by bias current) (4)

Output Stage:

$G_2 = 1 + (R_X/R_K)$ (Select ratio to obtain V_{OUT} between 5V and 10V full scale with V_{IN} at its maximum) (5)

$R_X \parallel R_K = 100k\Omega$ (Balance impedances seen by the + and - inputs of A_2 to reduce effect of bias current on the output offset) (6)

$R_B = R_A + R_F$ (Load output demodulator equal to input demodulator) (7)

Inverting Gain, Voltage or Current Input

The signal portion of Figure 4 shows two possible inverting input stage configurations: current and input and voltage input.

Input Stage:

For the voltage input case:

$G_1 = -R_F/R_S$ (Select G_1 to be less than 5V/full scale V_{IN} to limit the demodulator output voltage to 5V) (8)

$R_F = 2M\Omega$ (Select to load the demodulator with at least 2MΩ (9)

$$R_C = R_S \parallel (R_F + 100k\Omega) = \frac{R_S (R_F + 100k\Omega)}{R_S + R_F + 100k\Omega}$$

(Balance the impedances seen by the + and - inputs of A_1). (10)

For the current input case:

$$V_{OUT} = -I_{IN} R_F \bullet G_2 \quad (11)$$

$$R_C = R_F \quad (12)$$

R_F may be made larger than 2MΩ if desired. The 10pF capacitors are used to compensate for the input capacitance of A_1 and to insure frequency stability.

Output Stage:

The output stage is the same as shown in equations (5), (6), and (7).

Illustrative Calculations:

The maximum input voltage is 100mV. It is desired to amplify the input signal for maximum accuracy. Non-inverting output is desired.

Input Stage:

Step 1

G_1 max = 5V/ Max Input Signal = 5V/0.1V = 50V/V

With the above gain of 50V/V, if the input ever exceeds 100mV, it would drive the output to saturation. Therefore, it is good practice to allow reasonable input overrange.

So, to allow for 25% input overrange without saturation at the output, select;

$$G_1 = 40V/V$$

$$G_1 = 1 + (R_F + R_A) = 40$$

$$\therefore R_F/R_A = 39 \quad (13)$$

Step 2

$R_A + R_F$ forms a voltage divider with the 100kΩ output resistance of the demodulator. To limit the voltage divider loading effect to no more than 5%, $R_A + R_F$ should be chosen to be at least 2MΩ. For most applications, the 2MΩ should be sufficiently large for $R_A + R_F$. Resistances greater than 2MΩ may help decrease the loading effect, but would increase the offset voltage drift.

The voltage divider with $R_A + R_F = 2M\Omega$ is $2M\Omega/(2M\Omega + 100k\Omega) = 2/(2 + 0.1) = 95.2\%$, i.e., the percent loading is 4.8%.

Choose $R_A + R_F = 2M\Omega \quad (14)$

Step 3

Solving equations (13) and (14)

$R_A = 50k\Omega$ and $R_F = 1.95M\Omega$

Step 4

The resistances seen by the + and - input terminals of the input amplifier A_1 should be closely matched in order to minimize offset voltage due to bias currents.

$$\therefore R_C = R_A \parallel (R_F + 100k\Omega)$$
$$= 50k\Omega \parallel (1.95M\Omega + 100k\Omega)$$
$$\approx 49k\Omega$$

Output Stage:

Step 5

$$V_{OUT} = V_{IN\ MAX} \bullet G_1 \bullet G_2$$

As discussed in Step 1, it is good practice to provide 25% input overrange.

So we will calculate G_2 for 10V output and 125% of the maximum input voltage.

$$\therefore V_{OUT} = (1.25 \times 0.1)(G_1)(G_2)$$
$$\text{i.e., } 10V = 0.125 \times 40 \times G_2$$
$$\therefore G_2 = 10V/5V = 2V/V$$

Step 6

$$G_2 = 1 + (R_X/R_K) = 2.0$$
$$\therefore R_X/R_K = 1.0$$
$$\therefore R_X = R_K \quad (15)$$

Step 7

The resistance seen by the + input terminal of the output stage amplifier A_2 (pin 13) is the output resistance 100kΩ of the output demodulator. The resistance seen by the (-) input terminal of A_2(pin14)should be matched to the resistance seen by the + input terminal.

The resistance seen by pin 14 is the parallel combination of R_X and R_K.

$$\therefore R_X \parallel R_K = 100k\Omega$$
$$\text{i.e., } (R_X \bullet R_K/(R_X + R_K) = 100k\Omega$$
$$\text{i.e., } R_K/[1 + (R_K/R_X)] = 100k\Omega \quad (16)$$

Step 8

Solving equations (15) and (16) $R_K = 20k\Omega$ and $R_X = 200k\Omega$.

Step 9

The otuput demodulator must be loaded equal to the input demodulator.

$$\therefore R_B = R_A + R_F = 2M\Omega$$

(See equation (14) above in Step 2)

Use the resistor values obtained in Steps 3, 4, 8 and 9, and connect the 3656 as shown in Figure 3.

OFFSET TRIMMING

Figure 5 shows an optional offset voltage trim circuit. It is important that $R_A + R_F = R_B$.

CASE 1: Input and output stages in low gain, use output potentiometer (R_2) only. Input potentiometer (R_1) may be disconnected. For example, unity gain could be obtained by setting $R_A = R_B = 20M\Omega$, $R_C = 100k\Omega$, $R_F = 0$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 2: Input stage in high gain and output stage in low gain, use input potentiometer (R_1) only. Output potentiometer (R_2) may be disconnected. For example, $G_T = 100$ could be obtained by setting $R_F = 2M\Omega$, $R_B = 2M\Omega$ returned to pin 17, $R_A = 20k\Omega$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 3: When it is necessary to perform a two-stage precision trim (to maintain a very small offset change under conditions of changing temperature and changing gain in A_1 and A_2), use step 1 to adjust the input stage and step 2 for the output stage. Carbon composition resistors are acceptable but potentiometers should be stable.

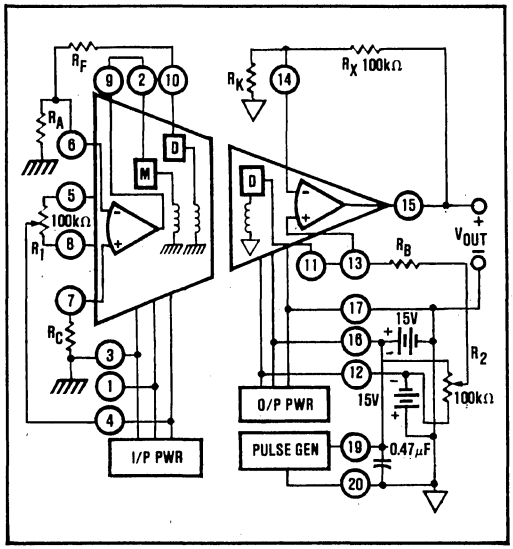


FIGURE 5. Optional Offset Voltage Trim.

Step 1: Input stage trim ($R_A = R_C = 20k\Omega$, $R_F = R_B = 20M\Omega$, $R_X = 100k\Omega$, $R_K = \infty$, R_2 disconnected); A_1 high, A_2 low gain. Adjust R_1 for 0V ±5mV or desired setting at V_{OUT}, pin 15.

Step 2: Output stage trim ($R_A = R_B = 20M\Omega$, $R_C = 100k\Omega$, $R_F = 0$, $R_X = 100k\Omega$, $R_K = \infty$, R_1 and R_2 connected); A_1 low, A_2 low gain. Adjust R_2 for 0V ±1mV or desired setting at V_{OUT}, pin 15 (±110mV approximate total range).

Note: Other circuit component values can be used with valid results.

APPLICATIONS

ECG AMPLIFIER

Although the features of the circuit shown in Figure 6 are important in patient monitoring applications, they may also be useful in other applications. The input circuitry uses an external, low quiescent current op amp (OPA21 type) powered by the isolated power of the input stage to form a high impedance instrumentation amplifier input (true three-wire input). R_3 and R_4 give the input stage amplifier of the 3656 a noninverting gain of 10 and an inverting gain of -9. R_1 and R_2 give the external amplifier a noninverting gain of 1 + 1/9. The inputs are applied to the noninverting inputs of the two amplifiers and the composite input stage amplifier has a gain of 10.

The 330kΩ, 1W, carbon resistors and diodes D_1 - D_4 provide protection for the input amplifiers from defibrillation pulses.

The output stage in Figure 6 is configured to provide a bandpass filter with a gain of 22.7 (68MΩ/3MΩ). The high-pass section (0.05Hz cutoff) is formed by the 1μF capacitor and 2MΩ resistor which are connected in series between the output demodulator and the inverting input of the output stage amplifier. The low-pass section (100Hz cutoff) is formed by the 68MΩ resistor and 22pF capacitor located in the feedback loop of the output stage. The diodes provide for quick recovery of the high-pass filter to overvoltages at the input. The 100kΩ pot and the 100MΩ resistor allow the output voltage to be trimmed to compensate for increased offset voltage caused by unbalanced impedances seen by the inputs of the output stage amplifier.

In many modern electrocardiographic systems, the

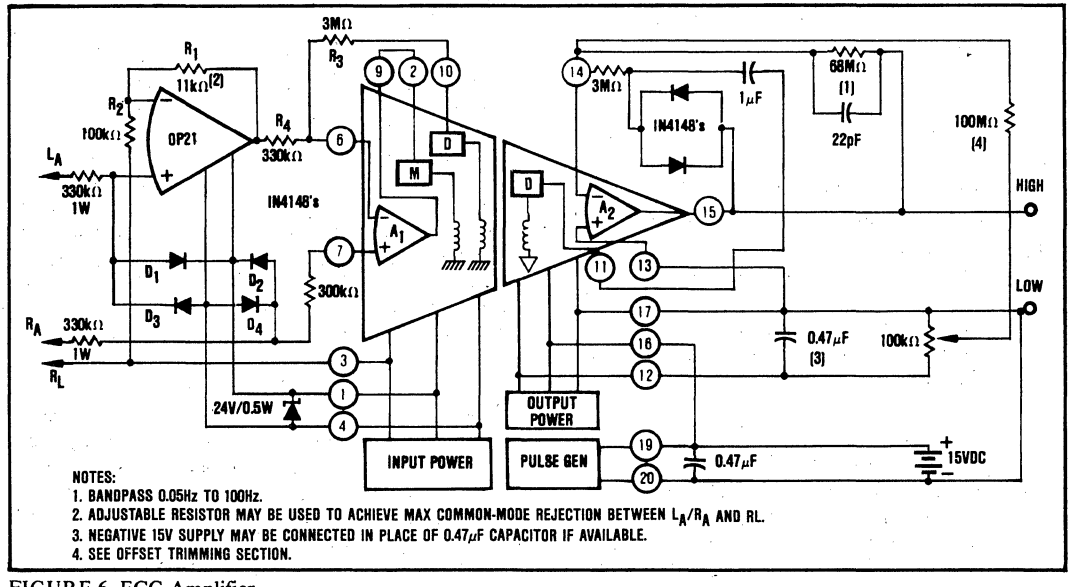


FIGURE 6. ECG Amplifier.

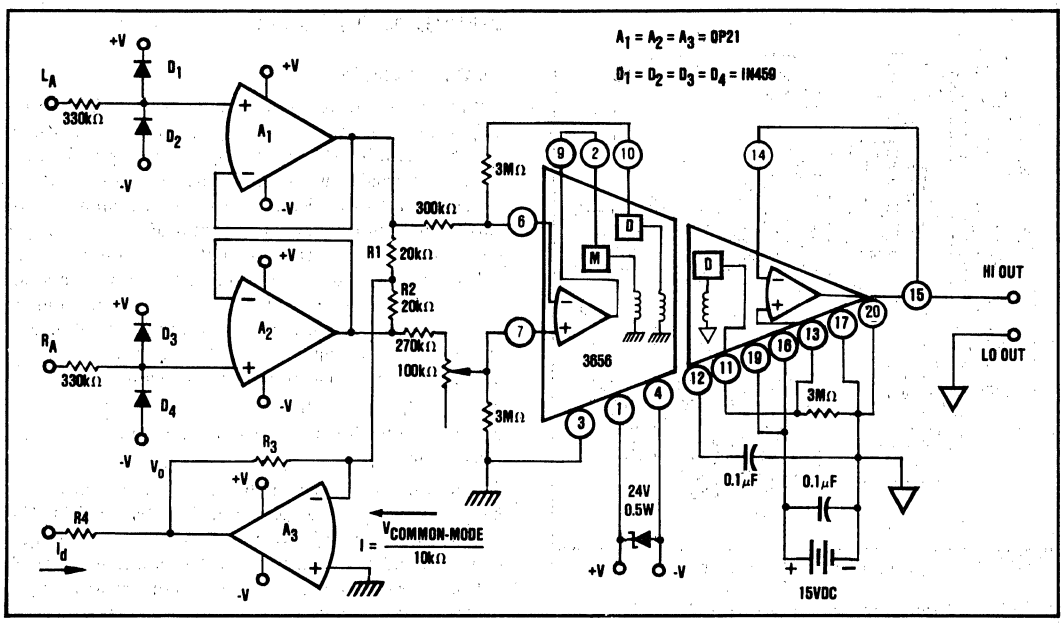


FIGURE 7. Driven Right-Leg ECG Amplifier.

patient is not grounded. Instead, the right-leg electrode is connected to the output of an auxiliary operational amplifier as shown in Figure 7. In this circuit, the common-mode voltage on the body is sensed by the two averaging resistors R_1 and R_2, inverted, amplified, and fed back to the right-leg through resistor R_4. This negative feedback drives the common-mode voltage to a low value. The body's displacement current i_d does not flow to ground, but rather to the output circuit of A_3. This reduces the pickup as far as the ECG amplifier is concerned and effectively grounds the patient.

The value of R_4 should be as large as practical to isolate the patient from ground. The resistors R_3 and R_4 may be selected by these equations:

$$R_3 = (R_1/2)\,(V_o/V_{CM}) \text{ and } R_4 = (V_{CM} - V_o)/i_d$$

$$(-10V \leqslant V_o \leqslant +10V \text{ and } -10V \leqslant V_{CM} \leqslant +10V)$$

where V_o is the output voltage of A_3 and V_{CM} is the common-mode voltage between the inputs L_A and R_A and the input common at pin 3 of the 3656.

This circuit has the added benefit of having higher common-mode rejection than the circuit in Figure 6 (approximately 10dB improvement).

BIPOLAR CURRENT OUTPUT

The three-port capability of the 3656 can be used to implement a current output isolation amplifier function, usually difficult to implement when grounded loads are involved. The circuit is shown in Figure 8 and the following equations apply:

$$G = I_{OUT}/V_{IN} = 1 + \frac{R_F}{R_A} \times \frac{R_2}{(R_1 + R_2) \cdot R_S}$$

$$I_{OUT} \leqslant \pm 2.5mA$$

$$V_L \leqslant \pm 4V \text{ (compliance)}$$

$$R_L \leqslant 1.6k\Omega$$

$$R_F + R_A = R_1 + R_2 \leqslant 2M\Omega$$

CURRENT OUTPUT - LARGER UNIPOLAR CURRENTS

A more practical version of the current output function is shown in Figure 9. If the circuit is powered from a source greater than 15V as shown,a three-terminal regulator should be used to provide 15V for the pulse generator (pins 19 and 20). The input stage is configured as a unity gain buffer, although other configurations such as current input could be used. The circuit uses the isolation feature between the output stage and the primary power supply to generate the output current configuration that can work into a grounded load. Note that the output transistors can only drive positive current into the load. Bipolar current output would require a second transistor and dual supply.

ISOLATED 4mA TO 20mA OUTPUT

Figure 10 shows the circuit of an expanded version of the isolated current output function. It allows any input voltage range to generate the 4mA to 20mA output excursion and is also capable of zero suppression. The "span" (gain) is adjusted by R_2 and the "zero" (4mA output for minimum input) is set by the 200kΩ pot in the output stage. A three-terminal 5V reference is used to provide a stable 4mA operating point. The reference is

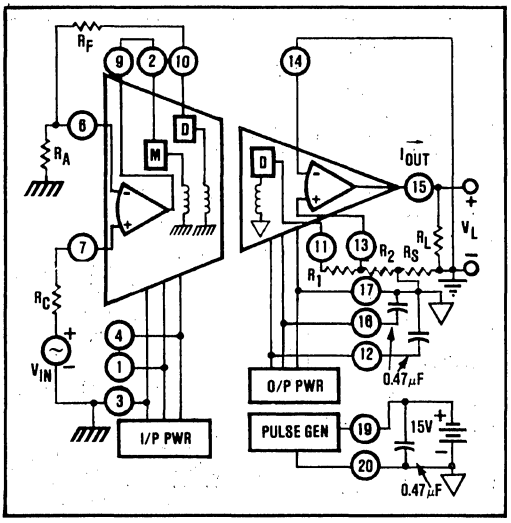


FIGURE 8. Bipolar Current Output.

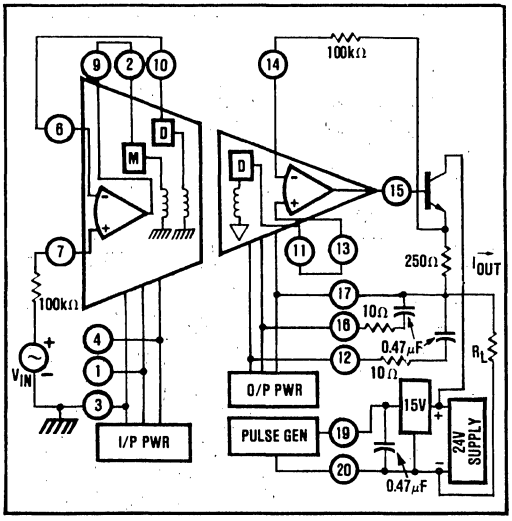


FIGURE 9. Isolated 1 to $5V_{IN}/4$ to 20mA I_{OUT}.

connected to insert an adjustable bias between the demodulator output and the noninverting input of the output stage.

DIFFERENTIAL INPUT

Figure 11 shows the proper connections for differential input configuration. The 3656 is capable of operating in this input configuration only for floating loads (i.e., the source V_{IN} has no connection to the ground reference established at pin 3). For this configuration the usual 2MΩ resistor used in the input stage is split into two halves, R_F and R_{F-}. The demodulator load (seen by pin 10 with respect to pin 3) is still 2MΩ for the floating load as shown. Notice pin 19 is common in Figure 11 whereas pin 20 is common in previous figures.

SERIES STRING SOURCE

Figure 12 shows a situation where a small voltage, which is part of a series string of other voltages, must be measured. The basic problem is that the small voltage to be measured is 500V above the system ground (i.e., a system common-mode voltage of 500V exists). The circuit converts this system CMV to an amplifier isolation mode voltage. Thus, the isolation voltage ratings and isolation-mode rejection specifications apply.

IMPROVED INPUT CHARACTERISTICS

In situations where it is desired to have better DC input amplifier characteristics than the 3656 normally provides it is possible to add a precision operational amplifier as shown in Figure 13. Here the instrumentation grade Burr-Brown 3510 is supplied from the isolated power of the input stage. The 3656 is configured as a unity-gain buffer. The gain of the 3510 stage must be chosen to limit its full scale output voltage to 5V and avoid overdriving the 3656's demodulators. Since the 3656 draws a

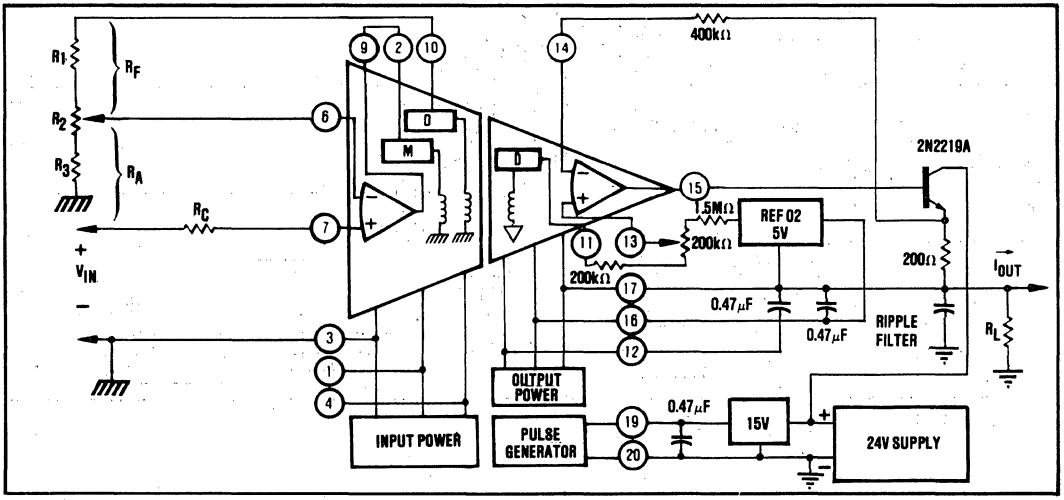


FIGURE 10. Isolated 4mA to 20mA I_{OUT}.

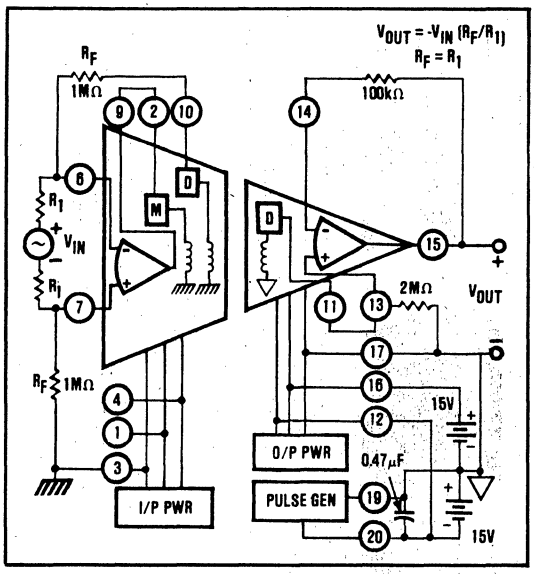


FIGURE 11. Differential Input, Floating Source.

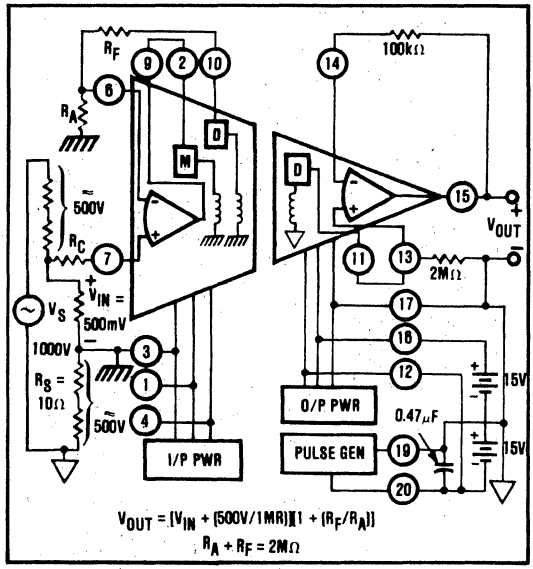


FIGURE 12. Series Source.

significant amount of supply current, extra filtering for the input supply is required as shown (2 x 0.47μF).

ELECTROMAGNETIC RADIATION

The transformer coupling used in the 3656 for isolation makes the 3656 a source of electromagnetic radiation unless it is properly shielded. Physical separation between the 3656 and sensitive components may not give sufficient attenuation by itself. In these applications the use of an electromagnetic shield is a must. A shield, Burr-Brown 100MS, is specially designed for use with the 3656 package. Note that the offset voltage appearing at pin 15 may change by 4mV to 12mV with use of the shield; however, this can be trimmed (see Offset Trimming section).

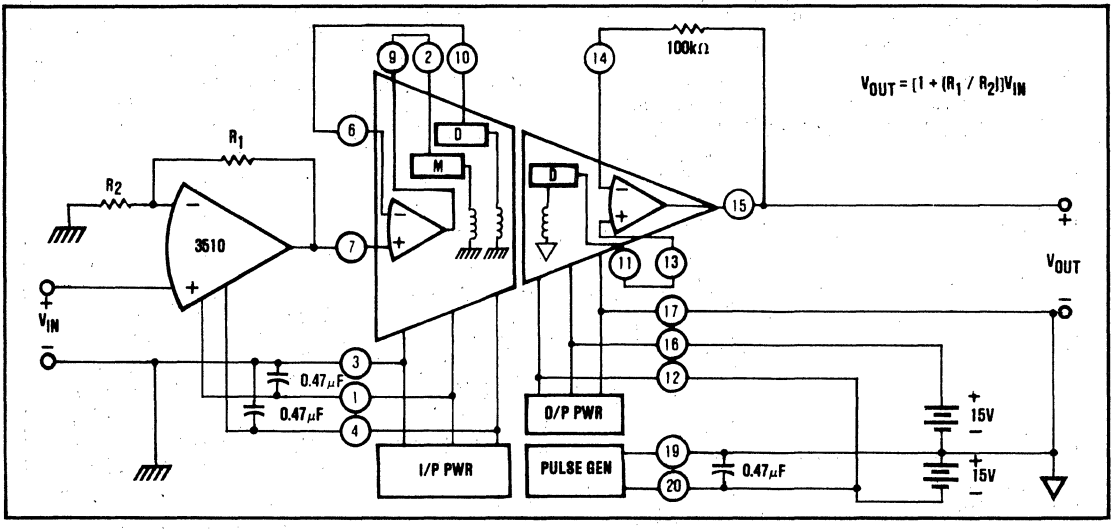
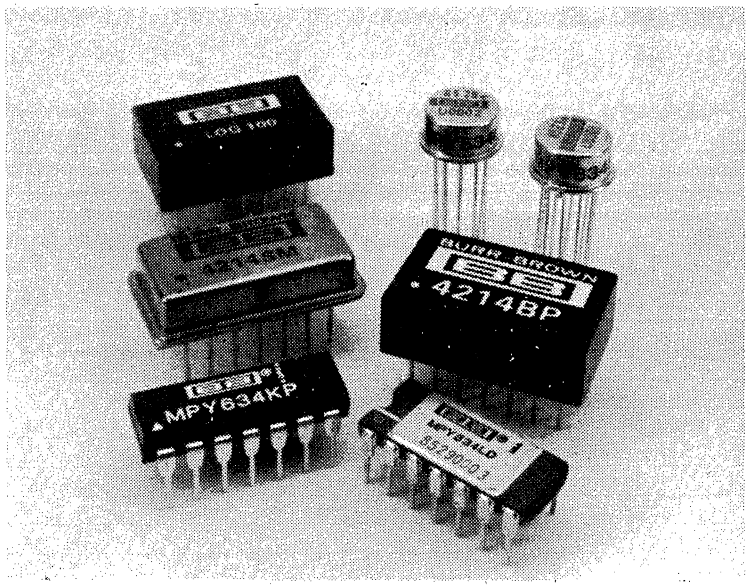


FIGURE 13. Isolator for Low-Level Signals.

ANALOG CIRCUIT FUNCTIONS



Analog circuits act as building blocks with which to perform a variety of instrumentation, computation, and control functions. They provide a broad range of versatile, proven, and ready to use computational function circuits for the designer to use in developing simple or complex systems. The analog circuit functions include multipliers, dividers, multifunction converters, true rms-to-DC converters, logarithmic amplifiers, voltage and window comparators, peak detectors, precision oscillators, and filters. The multifunction converter also provide multiply, divide, square root, exponentiate, roots, sine, cosine, arctangent, vector magnitude RMS-to-DC and logarithmic amplifier functions.

The availability of these relatively complex functions as precise, versatile, easy-to-use, low-cost building blocks has broadened the scope of practical analog circuit systems and greatly simplified analog circuit designs. The names of most analog circuit functions are self-explanatory and describe the main functions they perform.

The functions are used mostly for processing (handing) and/or conditioning of analog signals, and usually (though not always) for simulation of algebraic and/or trigonometrically expressed analog computations. The variety of applications these functions are effectively used for, are limited only by the designer's creative imagination. Some of the interesting applications where analog circuit functions have found wide acceptance are listed in the table on the following page.

Types of Applications	Recommended Analog Circuit Function
Analog simulation. Algebraic and trigonometric computations. Power series approximation, function fitting and linearizing Analog wave shaping.	Multiplier, Divider, Multifunction Converter, Logarithmic Amplifier, Oscillator.
VCO and AGC applications.	Multiplier, Divider.
Vector computation.	Multifunction Converter, Multiplier.
Power and energy measurements.	Multiplier, RMS-to-DC Converter.
Moduation and demodulation.	Multiplier, Divider.
Signal compression.	Logarithmic Amplifier.
Log-antilog-log ratio computations.	Logarithmic Amplifier.
Light-related measurements.	Logarithmic Amplifier.
Analog signal conditioning.	All circuit functions.
Instrumentation and control systems.	All circuit functions.
Variety of test equipment.	All circuit functions.
Transducer excitation	Oscillator.
Signal reference.	Oscillator.
Alarm circuits.	Voltage and Window Comparators.
Bang-bang control applications.	Voltage and Window Comparators.
Control of limit stops.	Voltage and Window Comparators.
Analog memory and peak detection.	Peak Detection.

SELECTION GUIDE

MULTIPLIERS/DIVIDERS

You can select accuracy from 0.25% to 2% max from this complete line of integrated circuit multipliers. Most provide full four-quadrant multiplication. All are laser-trimmed for accuracy—no trim pots are needed to meet specified performance. These compact models bring the cost of high performance down to acceptable levels.

MULTIPLIERS/DIVIDERS									
Model[1]	Transfer Function	Error at 25°C, max (%)	Temperature Coefficient (%/°C)	Feed-through (mV)	Offset Voltage (mV)	1% Bandwidth (kHz)	Temp Range [2]	Package	Page
MPY100A	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$	±2	0.017	100	50	70	Ind	TO-100	4-23
MPY100B	*	±1	0.008	30	10	70	Ind	TO-100	4-23
MPY100C	*	±0.5	0.008	30	7	70	Ind	TO-100	4-23
MPY100S	*	±0.5	0.025	30	7	70	MIL	TO-100	4-23
MPY534JH	*	±1.0	0.022	0.3%	5	3MHz	Com	TO-100	4-31
MPY534JD	*	±1.0	0.022	0.3%	5	3MHz	Com	DIP	4-31
MPY534KH	*	±0.5	0.015	0.15%	2	3MHz	Com	TO-100	4-31
MPY534KD	*	±0.5	0.015	0.15%	2	3MHz	Com	DIP	4-31
MPY534LH	*	±0.25	0.008	0.05%	2	3MHz	Com	TO-100	4-31
MPY534LD	*	±0.25	0.008	0.05%	2	3MHz	Com	DIP	4-31
MPY534SH	*	±1.0	0.02	0.3%	5	3MHz	MIL	TO-100	4-31
MPY534SD	*	±1.0	0.02	0.3%	5	3MHz	MIL	DIP	4-31
MPY534TH	*	±0.5	0.01	0.15%	2	3MHz	MIL	TO-100	4-31
MPY534TD	*	±0.5	0.01	0.15%	2	3MHz	MIL	DIP	4-31
MPY634AM	*	±1.0	0.022	0.3%	5	10MHz	Ind	TO-100	4-38
MPY634BM	*	±0.5	0.015	0.15%	2	10MHz	Ind	TO-100	4-38
MPY634SM	*	±1.0	0.02	0.3%	5	10MHz	MIL	TO-100	4-38
MPY634KP	*	±2.0	0.03	0.3%	25	10MHz	Ind	DIP	4-38
4203J	XY/10	2	0.04	50	20	40	Com	TO-100	4-97
4203K	*	1	0.04	50	20	40	Com	TO-100	4-97
4203S, (Q)	*	1	0.04	50	20	40	MIL	TO-100	4-97
4204J	XY/10	0.5	0.01	10	15	32	Ind	DIP	4-99
4204K	*	0.5	0.01	5	5	33	Ind	DIP	4-99
4204S, (Q)	*	0.25	0.02	5	5	33	MIL	DIP	4-99
4205J	$(X_1 - X_2)(Y_1 - Y_2)/10$	2	0.04	50	20	40	Com	TO-100	4-97
4205K	*	1	0.04	50	20	40	Com	TO-100	4-97
4205S, (Q)	*	1	0.04	50	20	40	MIL	TO-100	4-97
4206J	XY/10	0.5	0.01	10	15	33	Com	DIP	4-99
4206K	*	0.25	0.01	5	5	33	Com	DIP	4-99
4213AM, (Q)	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z$	1	0.008	30	10	70	Ind	TO-100	4-105
4213BM	*	0.5	0.008	30	7	70	Ind	TO-100	4-105
4213SM	*	0.5	0.008	30	7	70	MIL	TO-100	4-105
4213/MIL Series		See Military Products, section 12.							
4214AP	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z$	1	0.02	30	10	70	Ind	DIP	4-109
4214BP	*	0.5	0.02	30	7	70	Ind	DIP	4-109
4214RM	*	1	0.02	30	10	70	Ind	DIP	4-109
4214SM	*	0.5	0.02	30	7	70	Ind	DIP	4-109

*Same as model above.

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, section 12. (2) Com = 0°C to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

SPECIAL FUNCTIONS

This group of models offers many different functions that are the quick, easy way to solve a wide variety of analog computational problems. Most are in integrated circuit packages and are laser-trimmed for excellent accuracy.

SPECIAL FUNCTIONS						
Function	Model	Description	Comments	Temp Range [1]	Package	Page
Multifunction Converter	4302	$Y(Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	Plastic package.	Ind	DIP	4-111
	LOG100JP	K Log (I_1/I_2)	Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity.	Com	DIP	4-15
Logarithmic Amplifier	4127JG 4127KP	K Log (I_1/I_{REF})	A more versatile part which contains an internal reference and a current inverter. 1% and 0.5% accuracy.	Com Com	DIP DIP	4-90 4-90
$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)dt}$	4340	True rms-to-DC conversion based on a log-antilog computational approach.	Laser-trimmed, requires no external trimming for rated accuracy. Hermetically sealed in a metal package.	Ind	DIP	4-117
	4341	True rms-to-DC conversion based on a log-antilog computational approach.	Some external trimming required. Lower cost in plastic package. Pin compatible with 4340.	Ind	DIP	4-119
Peak Detector	4085BM 4085KG 4085SM	These are analog memory circuits which hold and provide read-out of a DC voltage equal to peak value of a complex input waveform.	Digital mode control provides reset capability and allows selection of peaks within a desired time interval. May be used to make peak-to-peak detector.	Com Ind MIL	DIP DIP DIP	4-82 4-82 4-82
Window Comparator	4115/04	Provides a window or dual limit for comparison. Unit has 3 inputs: one for a voltage that sets upper limit, one for a voltage that sets lower limit, and one for a signal input.	The 3 outputs are capable of sinking up to 200mA of current, indicating if the input voltage is above, below, or in the window.	Com	Module	4-88

NOTES: (1) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

DIVIDERS

The use of a special log/antilog committed divider design overcomes the major problem encountered when trying to use a multiplier in a divider circuit. Outstanding accuracy is maintained even at very low denominator voltages.

DIVIDERS									
Model	Transfer Function	Input Range	Accuracy, max, D = 250mV (%)	Temperature Coefficient (%/°C)	0.5% Bandwidth (kHz)	Rated Output, min	Temp Range[1]	Package	Page
DIV100HP	N/D 10	250mV	1.0	0.2	15	±10V, ±5mA	Ind	DIP	4-7
DIV100JP	N/D 10	to	0.5	0.2	15	±10V, ±5mA	Ind	DIP	4-7
DIV100KP	N/D 10	10V	0.25	0.2	15	±10V, ±5mA	Ind	DIP	4-7

NOTES: (1) Ind = −25°C to +85°C.

FREQUENCY PRODUCTS

This group of products consists of precision oscillators and active filters for both signal generation and attenuation. Both fixed frequency and user selected frequency units are available.

FREQUENCY PRODUCTS						
Function	Model	Description	Comments	Temp Range[1]	Package	Page
Oscillator	4023/25	Fixed-frequency (customer-specified, 10Hz to 20kHz) provides a low distortion, stable amplitude sine wave output.	Frequency stability vs temperature: 0.04%/°C max. Amplitude stability vs temperature: 0.02%/°C max.	Ind	Module	4-80
	4423	Very-low cost in plastic package. Provides resistor programmable quadrature outputs (sine and cosine wave outputs simultaneously available).	Frequency range: 0.002Hz to 20kHz. Frequency stability: 0.01%/°C. Quadrature phase error: ±0.1%.	Com	DIP	4-123
Universal Active Filter	UAF41 UAF21 UAF11	These filters provide a complex pole pair. Based on state variable approach, low-pass, high-pass and bandpass outputs are available.	Add only resistors to determine pole location (frequency and Q). Easily cascaded for complex filter responses.	Ind Ind Ind	DIP DIP DIP	4-68 4-60 4-60

NOTES: (1) Com = 0 to +70°C; Ind = −25°C to +85°C.

VOLTAGE REFERENCE

This product is a precision voltage reference which provides a +10V output. The output can be adjusted with minimal effect on drift or stability.

VOLTAGE REFERENCE								
				Power Supply				
Model	Output (V)	Minimum Output (mA)	Maximum Drift (ppm/°C)	(V)	(mA)	Temp Range[1]	Package	Page
REF10KM	+10.000 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	4-46
REF10JM	+10.000 ±0.005	10	2	+13.5/35	4.5	Com	TO-99	4-46
REF10SM	+10.000 ±0.005	10	3	+13.5/35	4.5	MIL	TO-99	4-46
REF10RM	+10.000 ±0.005	10	6	+13.5/35	4.5	MIL	TO-99	4-46
REF101KM	+10.000 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	4-52
REF101JM	+10.000 ±0.005	10	2	+13.5/35	4.5	Com	TO-99	4-52
REF101SM	+10.000 ±0.005	10	3	+13.5/35	4.5	MIL	TO-99	4-52
REF101RM	+10.000 ±0.005	10	6	+13.5/35	4.5	MIL	TO-99	4-52

NOTES: (1) Com = 0 to +70°C; MIL = −55°C to +125°C.

GLOSSARY OF TERMS & DEFINITIONS
Analog Circuit Functions

ABSOLUTE-VALUE CIRCUIT
A circuit that produces a unipolar output signal equal to the magnitude or absolute value of a bipolar input signal.

ACCURACY
The deviation from the ideal output voltage defined as a percent of full scale output voltage.

COMPARATOR
A device with two stable output states which signal if an input current or voltage has crossed a threshold. The threshold may be set by one or more other currents or voltages, either fixed or variable.

CREST FACTOR
The ratio of the peak value of a time-varying signal to its rms value.

CURRENT LIMITING
Limiting the output current supplied by a circuit for protection purposes.

FEEDBACK
The return of a portion of the output signal from a device to the input of the device.

FEEDTHROUGH
The input offset parameter applicable to multipliers. It is the output voltage when voltage is applied to one input of the multiplier and the other input is at zero.

FULL POWER FREQUENCY RESPONSE
The maximum frequency at which the output will swing full scale peak-to-peak voltage into a rated load without significant distortion of the output.

HYSTERESIS
The transfer response lag of comparators controlled by positive feedback and resulting in different trip points for the two directions of output transition.

LOGARITHMIC AMPLIFIER
An amplifier which develops an output voltage that is proportional to the logarithm of the input signal.

OUTPUT OFFSET
The output voltage when the inputs are grounded.

RMS
The root-mean-square value of a time-varying signal E(t) over a time period of T is

$$E_{rms} = \sqrt{1/T \int_o^T [E(t)]^2 \, dt}$$

RMS CONVERTER
A circuit that develops a DC output voltage equal in rms value to an input signal of arbitrary waveform.

SETTLING TIME
The time required for the output to respond to a step input and to settle within some specified error band around the output final value.

SLEW RATE
The maximum rate of change of an output voltage when supplying the rated output.

SMALL SCALE FREQUENCY RESPONSE
The -3dB output frequency for a small AC signal (normally 1V, p-p) input. For multipliers, one input may be held at +10VDC or -10VDC and the other input held at small AC signal.

WINDOW COMPARATOR
A compartor that detects levels within a set range or window rather than simply distinguishing between levels above and below a set point.

BURR-BROWN®

DIV100

ANALOG DIVIDER

FEATURES

- HIGH ACCURACY
  0.25% maximum error, 40:1 denominator range
- TWO-QUADRANT OPERATION
  Dedicated log-antilog technique
- EASY TO USE
  Laser-trimmed to specified accuracy - no external resistors needed
- LOW COST
- DIP PACKAGE

APPLICATIONS

- DIVISION
- SQUARE ROOT
- RATIOMETRIC MEASUREMENT
- PERCENTAGE COMPUTATION
- TRANSDUCER AND BRIDGE LINEARIZATION
- AUTOMATIC LEVEL - AND GAIN - CONTROL
- VOLTAGE CONTROLLED AMPLIFIERS
- ANALOG SIMULATION

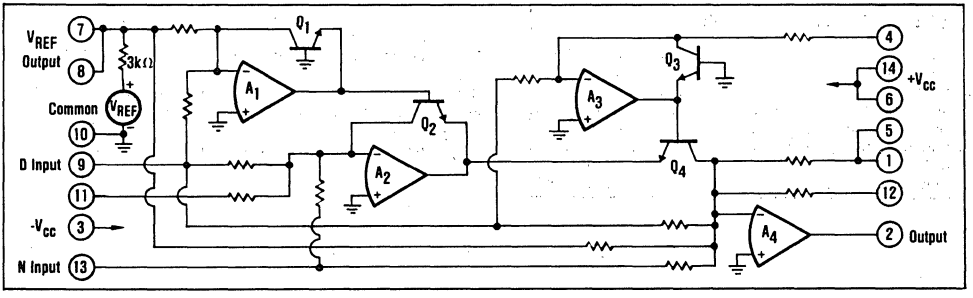
DESCRIPTION

The DIV100 is a precision two-quadrant analog divider offering superior performance over a wide range of denominator input. Its accuracy is nearly two orders of magnitude better than multipliers used for division. It consists of four operational amplifiers and logging transistors integrated into a single monolithic circuit and a laser-trimmed, thin-film resistor network. The electrical characteristics of these devices offer the user guaranteed accuracy without the need for external adjustment - the DIV100 is a complete, single package analog divider.

For those applications requiring higher accuracy than the DIV100 specifies the capability for optional adjustment is provided. These adjustments allow the user to set scale factor, feedthrough, and output-referred offsets for the lowest total divider error.

The DIV100 also gives the user a precision, temperature-compensated reference voltage for external use.

Designers of industrial process control systems, analytical instruments, or biomedical instrumentation will find the DIV100 easy to use and also a low cost, but highly accurate solution to their analog divider applications.



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SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

MODEL		DIV100HP			DIV100JP			DIV100KP			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSFER FUNCTION			V_O = 10N/D			*			*		
ACCURACY	$R_L \geq 10k\Omega$										
Total Error											
Initial	0.25V ≤ D ≤ 10V, N ≤ | D |		0.7	1.0		0.3	0.5		0.2	0.25	% FSO(1)
vs. Temperature	1V ≤ D ≤ 10V, N ≤ | D |		0.02	0.05(2)		*	*		*	*	% FSO/°C
	0.25V ≤ D ≤ 1V, N ≤ | D |		0.06	0.2(2)		*	*		*	*	% FSO/°C
vs. Supply	0.25V ≤ D ≤ 10V, N ≤ | D |		0.15			*			*		% FSO/%
Warm-up time to rated performance			5			*			*		Minutes
AC PERFORMANCE	D = +10V										
Small-Signal Bandwidth	-3dB		350			*			*		kHz
0.5% Amplitude Error	Small-Signal		15			*			*		kHz
0.57° Vector Error	Small-Signal		1000			*			*		Hz
Full-Power Bandwidth	V_O = ±10V, I_O = ±5mA		30			*			*		kHz
Slew Rate	V_O = ±10V, I_O = ±5mA		2			*			*		V/µsec
Settling Time	ϵ = 1%, ΔV_O = 20V		15			*			*		µsec
Overload Recovery	50% Output Overload		4			*			*		µsec
INPUT CHARACTERISTICS											
Input Voltage Range											
Numerator	N ≤ | D |	±10			*			*			V
Denominator	D ≥ +250mV	+10			*			*			V
Input Resistance	Either Input		25			*			*		kΩ
OUTPUT CHARACTERISTICS											
Full-Scale Output (FSO)		±10			*			*			V
Rated Output											
Voltage	I_O = ±5mA	±10			*			*			V
Current	V_O = ±10V	±5			*			*			mA
Current Limit											
Positive			15	20(2)		*			*		mA
Negative			19	23(2)		*			*		mA
OUTPUT NOISE VOLTAGE	N = 0V										
f_B = 10Hz to 10kHz											
D = +10V			370			*			*		µV, rms
D = +250mV			1			*			*		mV, rms
REFERENCE VOLTAGE CHARACTERISTICS	$R_L \geq 10M\Omega$										
Output Voltage											
Initial	At +25°C	6.3(2)	6.6	6.9(2)	*	*	*	*	*	*	V
vs. Supply			±25			*			*		µV/V
Temperature Coefficient			±50			*			*		ppm/°C
Output Resistance			3			*			*		kΩ
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			*			*		VDC
Operating Range	Derated Performance	±12		±20	*		*	*		*	VDC
Quiescent Current											
Positive Supply			5	7(2)		*	*		*	*	mA
Negative Supply			8	10(2)		*	*		*	*	mA
AMBIENT TEMPERATURE RANGE											
Specification		0		+70	*		*	*		*	°C
Operating Range	Derated Performance	-25		+85	*		*	*		*	°C
Storage		−40		+85	*		*	*		*	°C

*Same as DIV100H.

ABSOLUTE MAXIMUM RATINGS

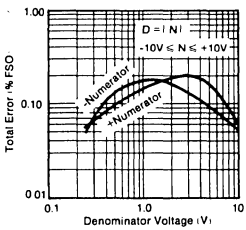
Supply	±20VDC
Internal Power Dissipation(3)	600mW
Input Voltage Range(4)	±20VDC
Storage Temperature Range	-55°C to +125°C
Operating Temperature Range	-25°C to +85°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-Circuit Duration(3)(5)	Continuous
Junction Temperature	175°C

NOTES:
1. FSO is the abbreviation for Full Scale Output.
2. This parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.
3. See General Information section for discussion.
4. For supply voltages less than ±20VDC, the absolute maximum input voltage is equal to the supply voltage.
5. Short-circuit may be to ground only. Rating applies to an ambient temperature of +38°C at rated supply voltage.

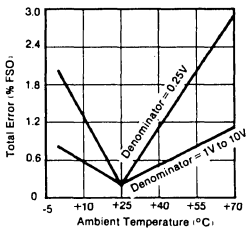
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.)

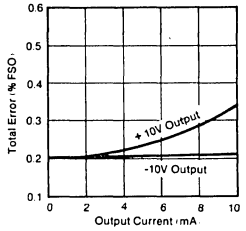
TOTAL ERROR VS DENOMINATOR VOLTAGE



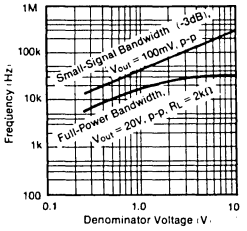
TOTAL ERROR VS AMBIENT TEMPERATURE



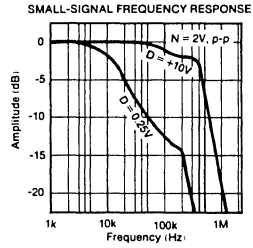
TOTAL ERROR VS OUTPUT CURRENT



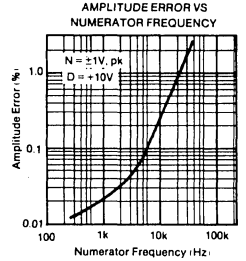
FREQUENCY RESPONSE VS DENOMINATOR VOLTAGE



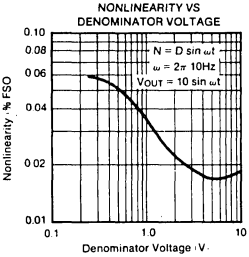
SMALL-SIGNAL FREQUENCY RESPONSE



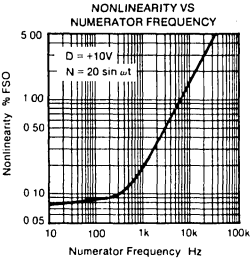
AMPLITUDE ERROR VS NUMERATOR FREQUENCY



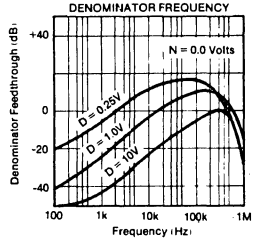
NONLINEARITY VS DENOMINATOR VOLTAGE



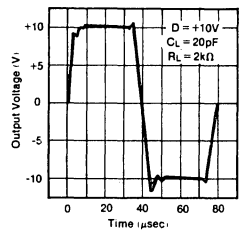
NONLINEARITY VS NUMERATOR FREQUENCY



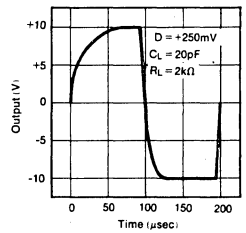
DENOMINATOR FEEDTHROUGH VS DENOMINATOR FREQUENCY



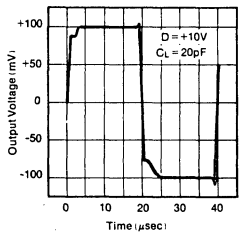
LARGE SIGNAL STEP RESPONSE



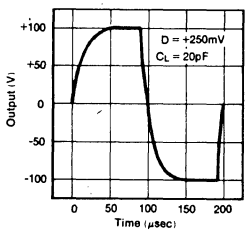
LARGE SIGNAL STEP RESPONSE



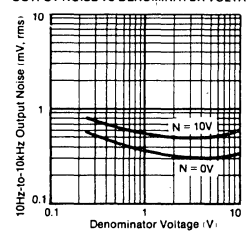
TRANSIENT RESPONSE



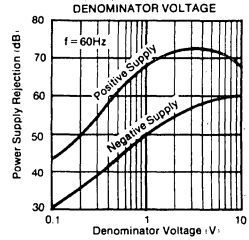
TRANSIENT RESPONSE



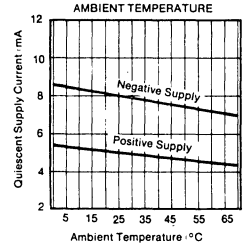
OUTPUT NOISE VS DENOMINATOR VOLTAGE



POWER SUPPLY REJECTION VS DENOMINATOR VOLTAGE

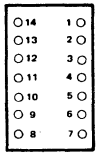


QUIESCENT CURRENT VS AMBIENT TEMPERATURE



PIN CONFIGURATION

1. Gain Error Adjust
2. Output
3. -V_{CC}
4. D Input Offset Adjust
5. Internally Connected to Pin 1
6. Internally Connected to Pin 14
7. Internally Connected to Pin 8
8. Reference Voltage
9. Denominator (D) Input
10. Common
11. N Input Offset Adjust
12. Output Offset Adjust
13. Numerator (N) Input
14. +V_{CC}

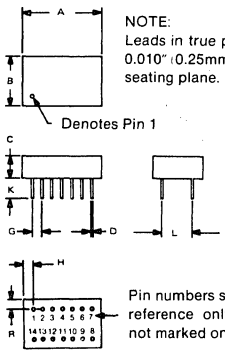


MECHANICAL

ORDER NUMBER: DIV100HP, DIV100JP, DIV100KP

CASE: Epoxy
WEIGHT: 2.7 Grams
CONNECTOR: 0145MC

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers are not marked on package.

DEFINITIONS

TRANSFER FUNCTION

The ideal transfer function for the DIV100 is:

$V_{out} = 10\ N/D$

where: N = Numerator input voltage
D = Denominator input voltage
10 = Internal scale factor

Figure 1 shows the operating region over the specified numerator and denominator ranges. Note that below the minimum denominator voltage (250mV) operation is undefined.

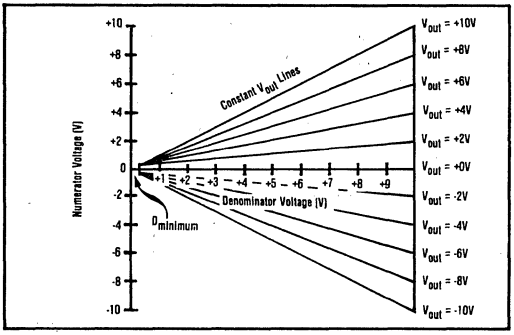


FIGURE 1. Operating Region.

ACCURACY

Accuracy is specified as a percentage of full-scale output (FSO). It is derived from the total error specification.

TOTAL ERROR

Total error is the deviation of the actual output from the ideal quotient 10N/D expressed in percent of FSO(10V); e.g., for the DIV100K:

$V_{out\ (actual)} = V_{out\ (ideal)} \pm$ total error,

where: Total error = 0.25% FSO = 25mV.

It represents the sum of all error terms normally associated with a divider: numerator nonlinearity, denomimator nonlinearity, scale-factor error, output-referred numerator and denominator offsets, and the offset due to the output amplifier. Individual errors are not specified because it is their sum that affects the user's application.

SMALL-SIGNAL BANDWIDTH

Small-signal bandwidth is the frequency the output drops to 70% (-3dB) of its DC value. The input signal must be low enough in amplitude to keep the divider's output from becoming slew-rate limited. A rule-of-thumb is to make the output voltage 100mV, p-p, when testing this parameter. Small-signal bandwidth is directly proportional to denominator magnitude as described in the Typical Performance Curves.

0.5% AMPLITUDE ERROR

At high frequencies the input-to-output relationship is a complex function that produces both a magnitude and vector error. The 0.5% amplitude error is the frequency at which the magnitude of the output drops 0.5% from its DC value.

0.57° VECTOR ERROR

The 0.57° vector error is the frequency at which a phase error of 0.01 radians occurs. This is the most sensitive measure of dynamic error of a divider.

LINEARITY

Defining linearity for a nonlinear device may seem unnecessary; however, by keeping one input constant the output becomes a linear function of the remaining input. The denominator is the input that is held fixed with a divider. Nonlinearities in a divider add harmonic distortion to the output in the amount of:

$$\text{Percent Distortion} \approx \frac{\text{Percent Nonlinearity}}{\sqrt{2}}$$

FEEDTHROUGH

Feedthrough is the signal at the output for any value of denominator within its rated range, when the numerator input is zero. Ideally the output should be zero under this condition.

GENERAL INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins to the power supply common. The connection of these capacitors should be as close to the DIV100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 1000pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the DIV100's output.

OVERLOAD PROTECTION

The DIV100 can be protected against accidental power supply reversal by putting a diode (1N4001, type) in series with each power supply line as shown in Figure 2. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off.

If this protection circuit is used, the accuracy of the DIV100 will be degraded by the power supply sensitivity specification. No other overload protection circuit is necessary. Inputs are internally protected against overvoltages and they are current-limited by at least a 10kΩ series resistor. The output is protected against short circuits to power supply common only.

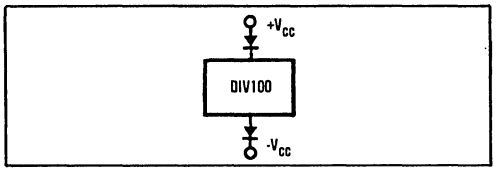


FIGURE 2. Overload Protection Circuit.

STATIC SENSITIVITY

No special handling is required. The DIV100 does not use MOS-type transitors. Furthermore, all external leads are protected by resistors against low energy electrostatic discharge (ESD).

INTERNAL POWER DISSIPATION

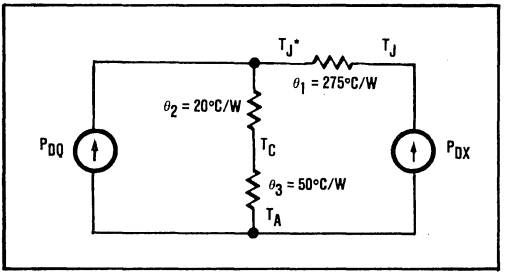


FIGURE 3. DIV100 Thermal Model.

Figure 3 is the thermal model for the DIV100 where:

P_{DQ} = Quiescent Power Dissipation
= $|+V_{CC}|\ I_{+QUIESCENT} + |-V_{CC}|\ I_{-QUIESCENT}$

P_{DX} = Worst case power dissipation in the output transistor
= $V_{CC}^2/4R_{LOAD}$ (for normal operation)
= $V_{CC}\ I_{(output\ limit)}$ (for short-circuit)

T_J = Junction Temperature (output loaded)
T_J* = Junction Temperature (no load)
T_C = Case Temperature
T_A = Ambient Temperature
θ = Thermal Resistance

This model is obviously not the simple one power source model that most linear device manufacturers give. It is, however, a more accurate model for a multidevice monolithic or hybrid integrated circuit.

The model in Figure 3 must be used in conjunction with the DIV100's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

As an example of how to use this model, consider this problem:

Determine the highest ambient temperature at which the DIV100 may be operated with a continuous short circuit to ground. $V_{CC} = \pm 15VDC$.

$P_{D(max)} = 600mW$. $T_{J(max)} = +175°C$.

$T_A = T_{J(max)} - P_{DQ}(\theta_2 + \theta_3) - P_{DX(short=circuit)}(\theta_1+\theta_2+\theta_3)$
$= 175°C - 18°C - 119°C = 38°C$

$P_{D(actual)} = P_{DQ} + P_{DX(short=circuit)} \leq P_{D(max)}$
$= 255mW + 345mW = 600mW$

The conclusion is that the device will withstand a short-circuit up to $T_A = +38°C$ without exceeding either the 175°C or 600mW absolute maximum limits.

LIMITING OUTPUT VOLTAGE SWING

The negative output voltage swing should be limited to ±11V, maximum, to prevent polarity inversion and possible system instability. This should be done by limiting the input voltage range.

THEORY OF OPERATION

The DIV100 is a log-antilog divider consisting of four operational amplifiers and four logging transistors integrated into a single monolithic circuit. Its basic principal of operation can be seen by an analysis of the circuit in Figure 4.

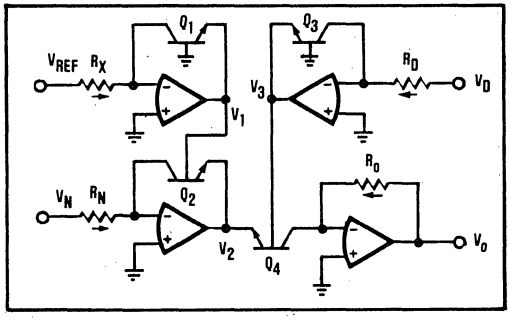


FIGURE 4. One-Quadrant Log-Antilog Divider

The logarithmic equation for a biopolar transistor is:

$$V_{BE} = V_T \ln (I_c/I_s), \quad (1)$$

where: $V_T = kT/q$
k = Boltzmann's constant = 1.381×10^{-23}
T = Absolute temperature in degrees Kelvin
q = Electron charge = 1.602×10^{-19}
I_c = Collector current
I_s = Reverse saturation current

Applying equation (1) to the four logging transistors gives:

For Q_1:
$V_{BE} = V_B - V_E = V_T[\ln(V_{REF}/R_X - \ln I_s]$

This leads to:
$V_1 = -V_T[\ln(V_{REF}/R_X - \ln I_s]$

For Q_2:
$V_1 - V_2 = V_T[\ln(V_N/R_N) - \ln I_S]$

For Q_3:
$V_3 = -V_T[\ln (V_D/R_D) - \ln I_S]$

We have now taken the logarithms of the input voltage V_{REF}, V_N, and V_D. Applying equation (1) to Q_4 gives:
$V_3 - V_2 = V_T [\ln (V_o/R_o) - \ln I_s]$.

Assume V_T and I_s are the same for all four transistors (a reasonable assumption with a monolithic IC). Solving

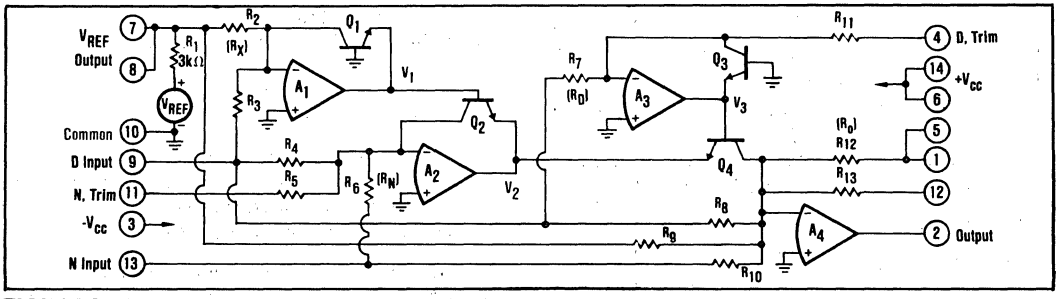


FIGURE 5. DIV100 Two-Quadrant Log-Antilog Circuit.

this last equation in terms of the previously defined variables and taking the antilogarithm of the result yields:

$$V_o = \frac{V_{REF}\, V_N\, R_o\, R_D}{V_D\, R_X\, R_N} \qquad (2)$$

In the DIV100 $V_{REF} = 6.6V$, $R_o = R_X = R_D$, and R_N is such that the transfer function is:

$$V_o = 10\ N\ D \qquad (3)$$

where: N = Numerator Voltage
D = Denominator Voltage

Figure 5 is a more detailed circuit diagram for the DIV100. In addition to the circuitry included in Figure 3, it also shows the resistors (R_3, R_4, R_8, R_9, and R_{10}) used for level-shifting. This converts the DIV100 to a two-quadrant divider.

The implementation of the transfer function is equation (3) is done using devices with real limitations. For example, the value of the D input must always be positive. If it isn't, Q_3 will no longer conduct, A_3 will become open loop, and its output and the DIV100 output will saturate. This limitation is further restricted in that if the D input is less than +250mV the errors will become substantial. It will still function, but its accuracy will be less.

Still another limitation is the value of the N input must always be equal to or less than the absolute value of the D input. From equation (3) it can be seen that if this limitation is not met V_o will try to be greater than the 10V output voltage limit of A_4.

A limitation that may not be obvious is the effect of source resistance. If the numerator or denominator inputs are driven from a source with more than 10Ω of output resistance, the resultant voltage divider will cause a significant output error. This voltage divider is formed by the source resistance and the DIV100 input resistance. With $R_{SOURCE} = 10\Omega$ and $R_{INPUT\ (DIV100)} = 25k\Omega$ an error of 0.04% results. This means that the best performance of the DIV100 is obtained by driving its inputs from operational amplifiers.

Note that the reference voltage is brought out to pins 7 and 8. This gives the user a precision, temperature-compensated reference for external use. Its open-circuit voltage is +6.6VDC, ±0.075V, typically. Its Thevenin equivalent resistance is 3kΩ. Since the output resistance is a relatively high value, an operational amplifier is necessary to buffer this source as shown in Figure 6. The external amplifier is necessary because current drawn through the 3kΩ resistor will effect the DIV100 scale factor.

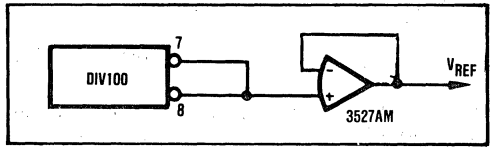


FIGURE 6. Buffered Precision Voltage Reference.

OPTIONAL ADJUSTMENTS

Figure 7 shows the connections to make to adjust the DIV100 for significantly better accuracy over its 40-to-1 denominator range.

The adjustment procedure is:

1. Begin with R_1, R_2, and R_3 set to their mid-position.
2. With |N| = D = 10.000V, ±1mV, adjust R_1 for $V_o = +10.000V$, ±1mV. This sets the scale factor.
3. Set D to the minimum expected denominator voltage. With N = D, adjust R_2 for $V_o = -10.000V$. This adjusts the output referred offset errors.
4. With D still at its minimum expected value, make N = D. Adjust R_3 for $V_o = 10.000V$. This adjusts the output referred offset errors.
5. Repeat steps 2-4 until the best accuracy is obtained.

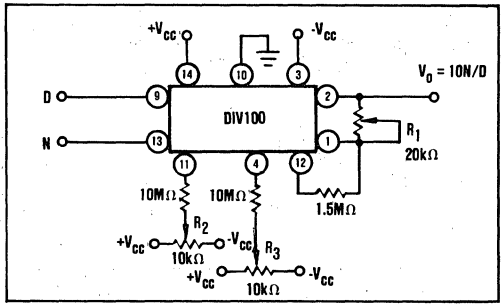


FIGURE 7. Connection Diagram for Optional Adjustments.

TYPICAL APPLICATIONS

CONNECTION DIAGRAM

Figure 8 is applicable to each application discussed in this section, except the square root mode.

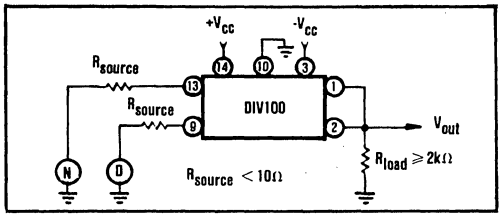


FIGURE 8. Connection Diagram - Divide Mode.

RATIOMETRIC MEASUREMENT

The DIV100 is useful for ratiometric measurements such as efficiency, elasticity, stress, strain, percent distortion, impedance magnitude, and fractional loss or gain. These ratios may be made for instantaneous, average, RMS, or peak values.

The advantage of using the DIV100 can be illustrated from the example shown in Figure 9.

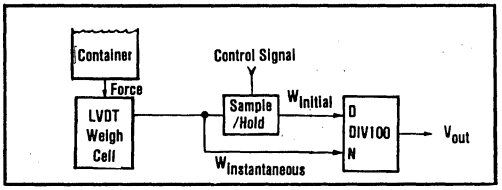


FIGURE 9. Weighing System - Fractional Loss.

The LVDT (Linear Variable Differential Transformer) weigh cell measures the force exerted on it by the weight of the material in the container. Its output is a voltage proportional to:

$$W = \frac{Fg}{a}$$

where: W = Weight of material
F = Force
g = Acceleration due to gravity
a = Acceleration (acting on body of weight W)

In a fractional loss weighing system the initial value of the material can be determined by the volume of the container and the density of the material. If this value is then held on the D-input to the DIV100 for some time interval, the DIV100 output will be a measure of the instantaneous fractional loss:

$$\text{Loss (L)} = W_{INSTANTANEOUS} / W_{INITIAL}$$

Note that by using the DIV100 in this application the common physical parameters of g and a have been eliminated from the measurement, thus eliminating the need for precise system calibration.

The output from a ratiometric measuring system may also be used as a feedback signal in an adaptive process control system. A common application in the chemical industry is in the ratio control of a gas and liquid flow as illustrated in Figure 10.

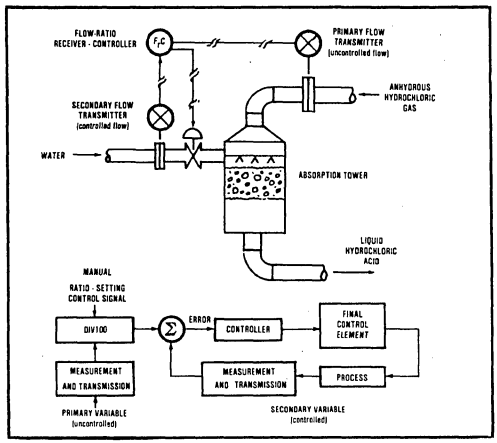


FIGURE 10. Ratio Control of Water to Hydrochloric Gas

PERCENTAGE COMPUTATION

A variation of the direct ratiometric measurements previously discussed is the need for percentage computation. In Figure 11 the DIV100 output varies as the percent deviation of the measured variable to the standard.

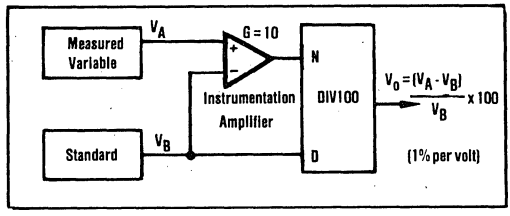


FIGURE 11. Percentage Computation.

TIME AVERAGING

The circuit in Figure 12 overcomes the fixed averaging interval and crude approximation of more conventional time averaging schemes.

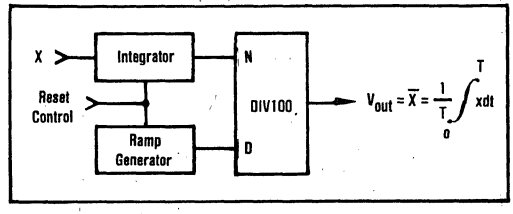


FIGURE 12. Time Averaging Computation Circuit.

BRIDGE LINEARIZATION

The bridge circuit in Figure 13 is fundamental to pressure, force, strain and electrical measurements. It can have one or more active arms whose resistance is a function of the physical quantity, property, or condition that is being measured; e.g., force of compression. For the sake of explanation the bridge in Figure 13 has only one active arm.

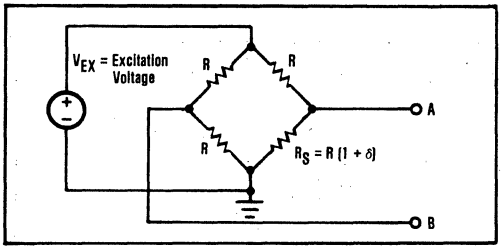


FIGURE 13. Bridge Circuit.

The differential output voltage V_{BA} is:

$$V_{BA} = V_B - V_A \quad \frac{-V_{EX}\delta}{2(2+\delta)},$$

a nonlinear function of the resistance change in the active arm. This nonlinearity limits the useful span of the bridge to perhaps ±10% variation in the measured parameter.

Bridge linearization is accomplished using the circuit in Figure 14. The instrumentation amplifier converts the differential output to a single-ended voltage needed to drive the divider. The voltage-divider string makes the numerator and denominator voltages:

$$N = \frac{-V_{EX}\delta\ R_{iN}}{(2R_1 + 3R_{iN})(2+\delta)}, \text{and,}$$

$$D = \frac{2\ V_{EX}\ R_{iD}}{(2R_1 + 3R_{iD})(2+\delta)}, \text{ respectively,}$$

where: R_{iN} = DIV100 numerator input resistance
R_{iD} = DIV100 denominator input resistance

Applying these voltages to the DIV100 transfer function gives:

$$V_o = 10N/D \quad \frac{(2R_1 + 3R_{iD})(R_{iN}\delta)\ 10}{(2R_1 + 3R_{iN})(2R_{iD})},$$

which reduces to:

$V_o = -5\delta$

if the divider's input resistances are equal.

The nonlinearity of the bridge has been eliminated and the circuit output is independent of variations in the excitation voltage.

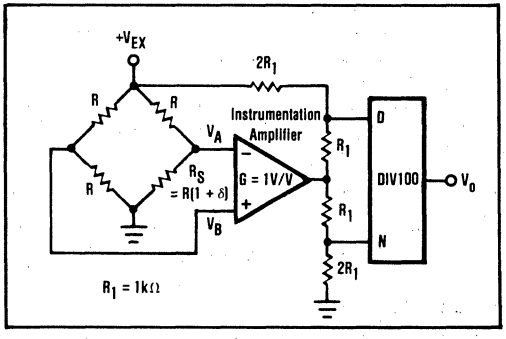


FIGURE 14. Bridge Linearization Circuit.

AUTOMATIC GAIN CONTROL

A simple AGC circuit using the DIV100 is shown in Figure 15. The numerator voltage may vary both positive and negative. The divider's output is half-wave rectified and filtered by D_1, R_3, and C_2. It is then compared to the DC reference voltage. If a difference exists the integrator sends a control signal to the denominator input to maintain a constant output, thus compensating for input voltage changes.

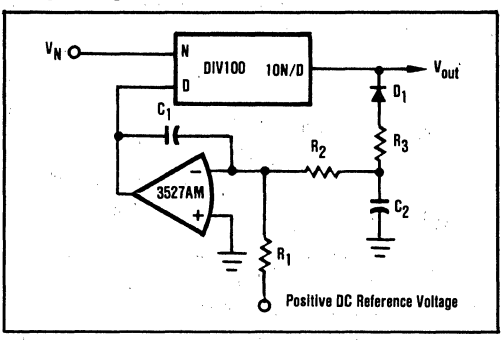


FIGURE 15. Automatic Gain Control Circuit.

VOLTAGE-CONTROLLED FILTER

Figure 16 shows how to use the DIV100 in the feedback loop of an integrator to form a voltage-controlled filter. The transfer function is:

$$\frac{V_{out(S)}}{V_{in(S)}} = \frac{K}{\tau S + 1}$$

where: $K = -R_2/R_1$

$$\tau = \frac{10\ R_2\ C}{V_{CONTROL}}$$

This circuit may be used as a single-pole low-pass active filter whose cutoff frequency is linearly proportional to the circuit's control voltage.

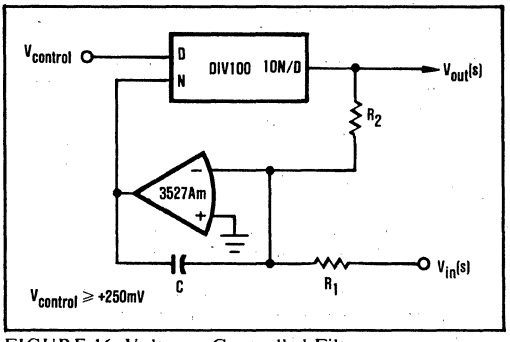


FIGURE 16. Voltage - Controlled Filter.

SQUARE ROOT

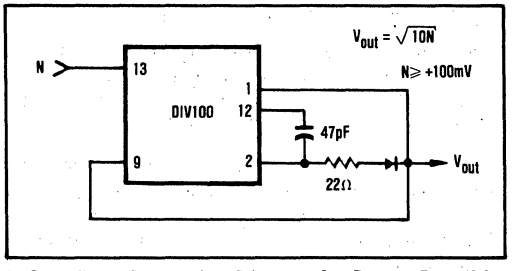


FIGURE 17. Connection Diagram for Square Root Mode.

BURR-BROWN®

LOG100

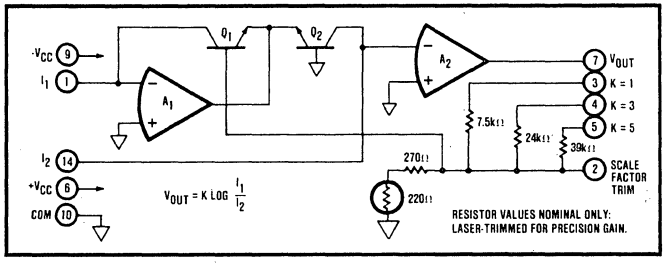
Precision
LOGARITHMIC AND LOG RATIO AMPLIFIER

FEATURES

- HIGH ACCURACY
  0.37% FSO max Total Error
  over 5 decades
- GOOD LINEARITY
  0.1% max Log Conformity
  over 5 decades
- EASY TO USE
  Pin-selectable Gains
  Internal Laser-trimmed Resistors
- WIDE INPUT DYNAMIC RANGE
  6 Decades, 1nA to 1mA

APPLICATIONS

- LOG, LOG RATIO AND ANTILOG COMPUTATIONS
- ABSORBANCE MEASUREMENTS
- DATA COMPRESSION
- OPTICAL DENSITY MEASUREMENTS
- DATA LINEARIZATION
- CURRENT AND VOLTAGE INPUTS



DESCRIPTION

The LOG100 uses advanced integrated circuit technologies to achieve high accuracy, ease of use, low cost, and small size. It is the logical choice for your logarithmic-type computations. The amplifier has guaranteed maximum error specifications over the full six-decade input range (1nA to 1mA) and for all possible combinations of I_1 and I_2. Total error is guaranteed so that involved error computations are not necessary.

The circuit uses a specially designed compatible thin-film monolithic integrated circuit which contains amplifiers, logging transistors, and low drift thin-film resistors. The resistors are laser-trimmed for maximum precision. FET input transistors are used for the amplifiers whose low bias currents (1pA typical) permit signal currents as low as 1nA while maintaining guaranteed total errors of 0.37% FSO maximum.

Because scaling resistors are self-contained, scale factors of 1V, 3V or 5V per decade are obtained simply by pin selections. No other resistors are required for log ratio applications. The LOG100 will meet its guaranteed accuracy with no user trimming. Provisions are made for simple adjustments of scale factor, offset voltage, and bias current if enhanced performance is desired.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

ELECTRICAL

SPECIFICATIONS

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	LOG100JP MIN	LOG100JP TYP	LOG100JP MAX	UNITS
TRANSFER FUNCTION			V_{OUT} = K Log (I_1/I_2)		
Log Conformity Error[1]	Either I_1 or I_2				
Initial	1nA to 100µA (5 decades)		0.04	0.1	%
	1nA to 1mA (6 decades)		0.15	0.25	%
Over Temperature	1nA to 100µA (5 decades)		0.002		%/°C
	1nA to 1mA (6 decades)		0.001		%/°C
K Range[2]			1, 3, 5		V/decade
Accuracy			0.3		%
Temperature Coefficient			0.03		%/°C
ACCURACY					
Total Error[3]	K = 1,[4] Current Input Operation				
Initial	I_1, I_2 = 1mA			±55	mV
	I_1, I_2 = 100µA			±30	mV
	I_1, I_2 = 10µA			±25	mV
	I_1, I_2 = 1µA			±20	mV
	I_1, I_2 = 100nA			±25	mV
	I_1, I_2 = 10nA			±30	mV
	I_1, I_2 = 1nA			±37	mV
vs Temperature	I_1, I_2 = 1mA		±0.20		mV/°C
	I_1, I_2 = 100µA		±0.37		mV/°C
	I_1, I_2 = 10µA		±0.28		mV/°C
	I_1, I_2 = 1µA		±0.033		mV/°C
	I_1, I_2 = 100nA		±0.28		mV/°C
	I_1, I_2 = 10nA		±0.51		mV/°C
	I_1, I_2 = 1nA		±1.26		mV/°C
vs Supply	I_1, I_2 = 1mA		±4.3		mV/V
	I_1, I_2 = 100µA		±1.5		mV/V
	I_1, I_2 = 10µA		±0.37		mV/V
	I_1, I_2 = 1µA		±0.11		mV/V
	I_1, I_2 = 100nA		±0.61		mV/V
	I_1, I_2 = 10nA		±0.91		mV/V
	I_1, I_2 = 1nA		±2.6		mV/V
INPUT CHARACTERISTICS (of amplifiers A_1 and A_2)					
Offset Voltage					
Initial			±0.7	±5	mV
vs Temperature			±80		µV/°C
Bias Current					
Initial			1	5[5]	pA
vs Temperature			doubles every 10°C		
Voltage Noise	10Hz to 10kHz, RTI		3		µV, rms
Current Noise	10Hz to 10kHz, RTI		0.5		pA, rms
AC PERFORMANCE					
3dB Response[6], I_2 = 10µA					
1nA	C_C = 4500pF		0.11		kHz
1µA	C_C = 150pF		38		kHz
10µA	C_C = 150pF		27		kHz
1mA	C_C = 50pF		45		kHz
Step Response[6]					
Increasing	C_C = 150pF				
1µA to 1mA			11		µsec
100nA to 1µA			7		µsec
10nA to 100nA			110		µsec
Decreasing	C_C = 150pF				
1mA to 1µA			45		µsec
1µA to 100nA			20		µsec
100nA to 10nA			550		µsec
OUTPUT CHARACTERISTICS					
Full Scale Output (FSO)		±10			V
Rated Output					
Voltage	I_{OUT} = ±5mA	±10			V
Current	V_{OUT} = ±10V	±5			mA
Current Limit					
Positive			12.5		mA
Negative			15		mA
Impedance			0.05		Ω
POWER SUPPLY REQUIREMENTS					
Rated Voltage			±15		VDC
Operating Range	Derated Performance	±12		±18	VDC
Quiescent Current			±7	±9	mA

ELECTRICAL (CONT'D)

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AMBIENT TEMPERATURE RANGE					
Specification		0		+70	°C
Operating Range	Derated Performance	−40		+85	°C
Storage		−40		+85	°C

NOTES:
1. Log Conformity Error is the peak deviation from the best-fit straight line of the V_{OUT} vs log I_{IN} curve expressed as a percent of peak-to-peak full scale output.
2. May be trimmed to other values. See Applications section.
3. The worst-case Total Error for any ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately.
4. Total Error at other values of K is K times Total Error for K = 1.
5. Guaranteed by design. Not directly measurable due to amplifier's committed configuration.
6. **3dB and transient response are a function of both the compensation capacitor and the level of input current. See Performance Curves.**

ABSOLUTE MAXIMUM RATINGS

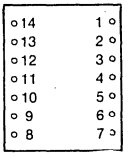
Supply	±18V
Internal Power Dissipation	600mV
Input Current	10mA
Input Voltage Range	±18V
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	175°C

SCALE FACTOR PIN CONNECTIONS

K, V/decade	Connections
5	5 to 7
3	4 to 7
1.9	4 and 5 to 7
1	3 to 7
0.85	3 and 5 to 7
0.77	3 and 4 to 7
0.68	3 and 4 and 5 to 7

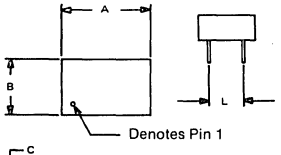
PIN CONFIGURATION

1. I_1 INPUT
2. SCALE FACTOR TRIM
3. K = 1
4. K = 3
5. K = 5
6. +V_{CC}
7. OUTPUT
8. NO INTERNAL CONNECTION
9. -V_{CC}
10. COMMON
11. NO INTERNAL CONNECTION
12. NO INTERNAL CONNECTION
13. NO INTERNAL CONNECTION
14. I_2 INPUT



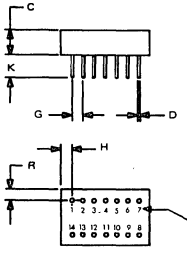
(Bottom View)

MECHANICAL



ORDER NUMBER: LOG100JP
CASE: Epoxy
WEIGHT: 2.7 grams
CONNECTOR: 0145MC

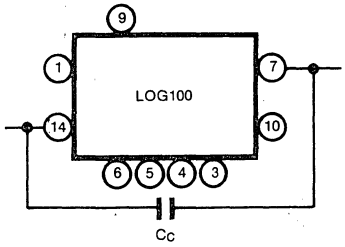
NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

Pin numbers shown for reference only. Numbers are not marked on package.

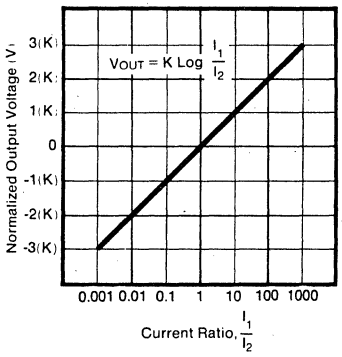
FREQUENCY COMPENSATION



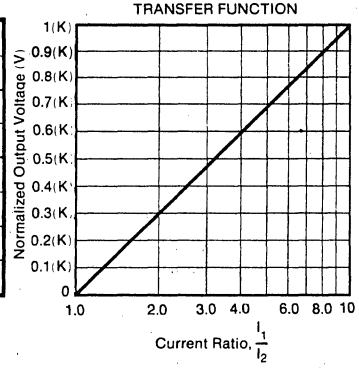
PERFORMANCE CURVES

(Typical at T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.)

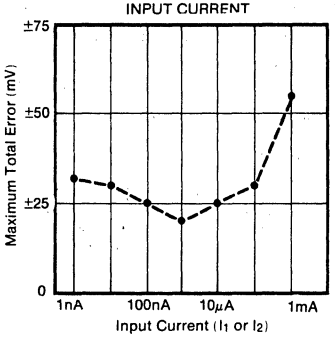
NORMALIZED TRANSFER FUNCTION



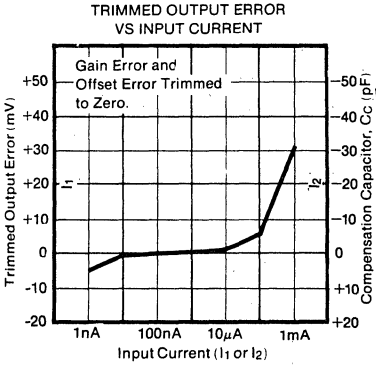
ONE CYCLE OF NORMALIZED TRANSFER FUNCTION



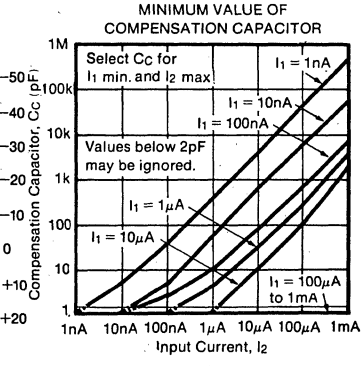
TOTAL ERROR VS INPUT CURRENT



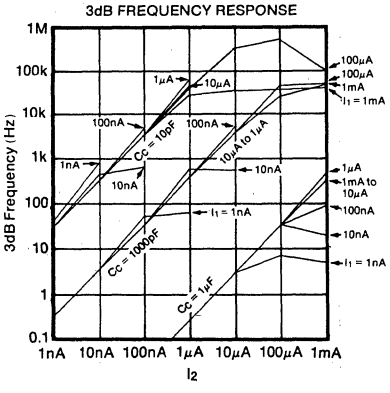
TRIMMED OUTPUT ERROR VS INPUT CURRENT



MINIMUM VALUE OF COMPENSATION CAPACITOR



3dB FREQUENCY RESPONSE



THEORY OF OPERATION

The base-emitter voltage of a bipolar transistor is

$$V_{BE} = V_T \ln \frac{I_c}{I_s} \quad \text{where:} \quad V_T = \frac{KT}{q} \qquad (1)$$

K = Boltzman's constant = 1.381×10^{-23}

T = Absolute temperature in degrees Kelvin

q = Electron charge = 1.602×10^{-19} Coulombs

I_c = Collector current

I_s = Reverse saturation current

From the circuit in Figure 1, we see that

$$V_{OUT}' = V_{BE_1} - V_{BE_2} \qquad (2)$$

Substituting (1) into (2) yields

$$V_{OUT}' = V_{T_1} \ln \frac{I_1}{I_{s_1}} - V_{T_2} \ln \frac{I_1}{I_{s_2}} \qquad (3)$$

If the transistors are matched and isothermal and $V_{T_1} = V_{T_2}$, then (3) becomes

$$V_{OUT}' = V_T \left[\ln \frac{I_1}{I_s} - \ln \frac{I_2}{I_s} \right] \qquad (4)$$

$$V_{OUT}' = V_T \ln \frac{I_1}{I_2} \quad \text{and since} \qquad (5)$$

$$\ln X = 2.3 \log_{10} X \qquad (6)$$

$$V_{OUT}' = n\, V_T \log \frac{I_1}{I_2} \qquad (7)$$

where $n = 2.3$ (8)

also

$$V_{OUT} = V_{OUT}' \frac{R_1 + R_2}{R_1} \qquad (9)$$

$$= \frac{R_1 + R_2}{R_1} n\, V_T \log \frac{I_1}{I_2} \qquad (10)$$

or

$$V_{OUT} = K \log \frac{I_1}{I_2} \qquad (11)$$

It should be noted that the temperature dependance associated with $V_T = KT/q$ is compensated by making R_1 a temperature sensitive resistor with the required positive temperature coefficient.

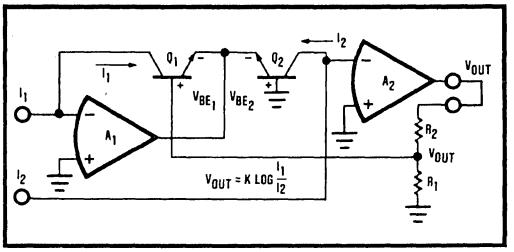


FIGURE 1. Simplified Model of Log Amplifier.

DEFINITION OF TERMS

TRANSFER FUNCTION

The ideal transfer function is $V_{OUT} = K \log \frac{I_1}{I_2}$

where

K = the scale factor with units of volts/decade

I_1 = numerator input current

I_2 = denominator input current.

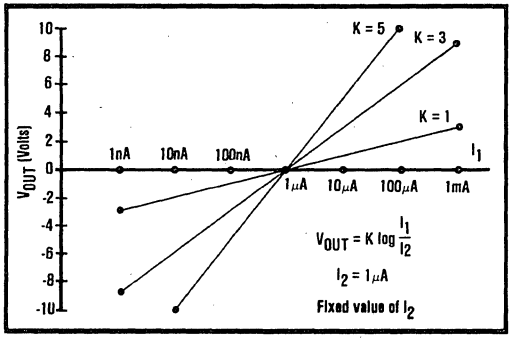


FIGURE 2. Transfer Function with Varying K and I_1.

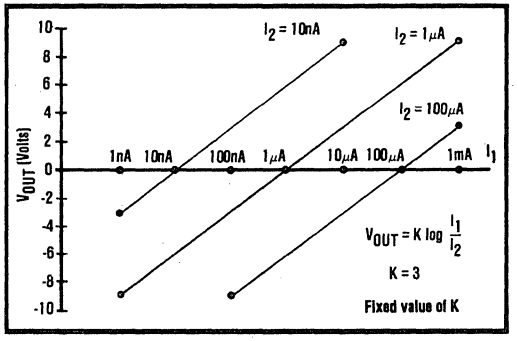


FIGURE 3. Transfer Function with Varying I_2 and I_1.

ACCURACY

Accuracy considerations for a log ratio amplifier are somewhat more complicated than for other amplifiers. The reason is that the transfer function is nonlinear and has two inputs, each of which can vary over a wide dynamic range. The accuracy for any combination of inputs is determined from the total error specification.

TOTAL ERROR

The total error is the deviation (expressed in mV) of the actual output from the ideal output of V_{OUT} = K log (I_1/I_2). Thus,

$V_{OUT\ (ACTUAL)} = V_{OUT\ (IDEAL)} \pm$ Total Error.

It represents the sum of all the individual components of error normally associated with the log amp when operated in the current input mode. The worst-case error for any given ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately.

Example

I_1 varies over a range of 10nA to 1μA and I_2 varies from 100nA to 10μA. What is the maximum error?

Table I shows the maximum errors for each decade combination of I_1 and I_2.

TABLE I. I_1/I_2 and Maximum Errors.

I_2 (max error)* \ I_1 (max error)*	10nA (30mV)	100nA (25mV)	1μA (20mV)
100nA (25mV)	0.1 (30mV)	1 (25mV)	10 (25mV)
1μA (20mV)	0.01 (30mV)	0.1 (25mV)	1 (20mV)
10μA (25mV)	0.001 (30mV)	0.01 (25mV)	0.1 (25mV)

*Maximum errors are in parenthesis.

Since the largest value of I_1/I_2 is 10 and the smallest is 0.001, K is set at 3V per decade so the output will range from +3V to -9V. The maximum total error occurs when I_1 = 10nA and is equal to K x 30mV. This represents a 0.75% of peak-to-peak FSO error $\frac{(3 \times 0.030)}{12} \times 100\% =$ 0.75% where the full scale output is 12V (from +3V to -9V).

ERRORS RTO AND RTI

As with any transfer function, errors generated by the function itself may be Referred-to-Output (RTO) or Referred-to-Input (RTI). In this respect log amps have a unique property:

Given some error voltage at the log amp's output, that error corresponds to a constant percent of the input regardless of the actual input level.

Refer to: Yu Jen Wong and William E. Ott, "Function Circuits: Design & Applications", McGraw-Hill Book, 1976.

LOG CONFORMITY

Log conformity corresponds to linearity when V_{OUT} is plotted versus I_1/I_2 on a semilog scale. In many applications log conformity is the most important specification. This is true because bias current errors are negligible (1pA compared to input currents of 1nA and above) and the scale factor and offset errors may be trimmed to zero or removed by system calibration. This leaves log conformity as the major source of error.

Log conformity error is defined as the peak deviation from the best-fit straight line of the V_{OUT} versus log (I_1/I_2) curve. This is expressed as a percent of peak-to-peak full scale output. Thus, the nonlinearity error expressed in volts over m decades is

$$V_{OUT\ (NONLIN.)} = K\ 2Nm \text{ volts} \quad (12)$$

where N is the log conformity error, in percent.

INDIVIDUAL ERROR COMPONENTS

The ideal transfer function with current input is

$$V_{OUT} = K \text{ Log } \frac{I_1}{I_2} \quad (13)$$

The actual transfer function with the major components of error is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{I_1 - I_{B_1}}{I_2 - I_{B_2}} \pm K\ 2Nm \pm V_{OS\ OUT} \quad (14)$$

The individual component of error is

ΔK = scale factor error (0.3%, typ)

I_{B_1} = bias current of A_1 (1pA, typ)

I_{B_2} = bias current of A_2 (1pA, typ)

N = log conformity error (0.05%, 0.1%, typ)

$V_{OS\ OUT}$ = output offset voltage (1mV, typ)

m = no. of decades over which N is specified: 0.05% for m = 5, 0.1% for m = 6

Example: what is the error with K = 3 when

$I_1 = 1\mu A$ and $I_2 = 100nA$

$$V_{OUT} = 3(1 \pm 0.003) \log \frac{10^{-6} - 10^{-12}}{10^{-7} - 10^{-12}} \pm 3(2)(0.0005)\ 5 \pm 1mV \quad (15)$$

$$\approx 3.009 \log \frac{10^{-6}}{10^{-7}} + 0.015 + 0.001 \quad (16)$$

$$= 3.009\ (1) + 0.015 + 0.001 \quad (17)$$

$$= 3.025 \text{ volts} \quad (18)$$

Since the ideal output is 3.000V the error as a percent of reading is

$$\% \text{ error} = \frac{0.025}{3} \times 100\% = 0.83\% \quad (19)$$

For the case of voltage inputs, the actual transfer function is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{\frac{V_1}{R_1} - I_{B_1} \pm \frac{E_{OS_1}}{R_1}}{\frac{V_2}{R_2} - I_{B_2} \pm \frac{E_{OS_2}}{R_2}} \pm K\ 2Nm \pm V_{OS\ OUT} \quad (20)$$

FREQUENCY RESPONSE

The 3dB frequency response of the LOG100 is a function of the magnitude of the input current levels and of the value of the frequency compensation capacitor. See Performance Curves for details.

The frequency response curves are shown for constant DC I_1 and I_2 with a small signal AC current on one of them.

The transient response of the LOG100 is different for increasing and decreasing signals. This is due to the fact that a log amp is a nonlinear gain element and has different gains at different levels of input signals. Frequency response decreases as the gain increases.

GENERAL INFORMATION

INPUT CURRENT RANGE

The stated input range of 1nA to 1mA is the range for specified accuracy. Smaller or larger input currents may be applied with decreased accuracy. Currents larger than 1mA result in increased nonlinearity. The 10mA absolute maximum is a conservative value to limit the power dissipation in the output stage of A_1 and the logging transistor. Currents below 1nA will result in increased errors due to the input bias currents of A_1 and A_2 (1pA typical). These errors may be nulled. See Optional Adjustments section.

FREQUENCY COMPENSATION

Frequency compensation for the LOG100 is obtained by connecting a capacitor between pins 7 and 14. The size of the capacitor is a function of the input currents as shown in the Performance Curves. For any given application the smallest value of the capacitor which may be used is determined by the maximum value at I_2 and the minimum value of I_1. Larger values of C_C will make the LOG100 more stable, but will reduce the frequency response.

SETTING THE REFERENCE CURRENT

When the LOG100 is used as a straight log amplifier I_2 is constant and becomes the reference current in the expression

$$V_{OUT} = K \log \frac{I_1}{I_{REF}} \quad (21)$$

I_{REF} can be derived from an external current source (such as shown in Figure 4) or it may be derived from a voltage source with one or more resistors.

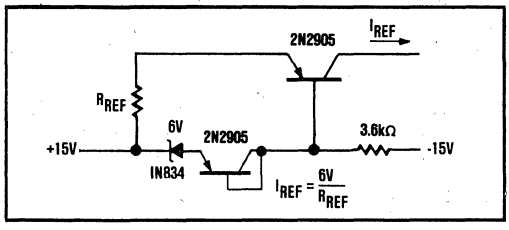


FIGURE 4. Temperature-Compensated Current Reference.

When a single resistor is used the value may be quite large when I_{REF} is small. If I_{REF} is 10nA and +15V is used

$$R_{REF} = \frac{15V}{10nA} = 1500M\Omega.$$

A voltage divider may be used to reduce the value of the resistor. When this is done one must be aware of possible errors caused by the amplifier's input offset voltage. This is shown in Figure 5.

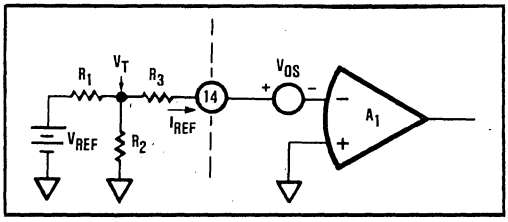


FIGURE 5. "T" Network for Reference Current.

In this case the voltage at pin 14 is not exactly zero, but is equal to the value of the input offset voltage of A_1 which ranges from zero to ±5mV. V_T must be kept much larger than 5mV in order to make this effect negligible. This concept also applies to pin 1.

OPTIONAL ADJUSTMENTS

The LOG100 will meet its specified accuracy with no user adjustments. If improved performance is desired the following optional adjustments may be made.

INPUT BIAS CURRENT

The circuit in Figure 6 may be used to compensate for the input bias currents of A_1 and A_2. Since the amplifiers have FET inputs with the characteristic bias current doubling every 10°C this nulling technique is practical only where the temperature is fairly stable.

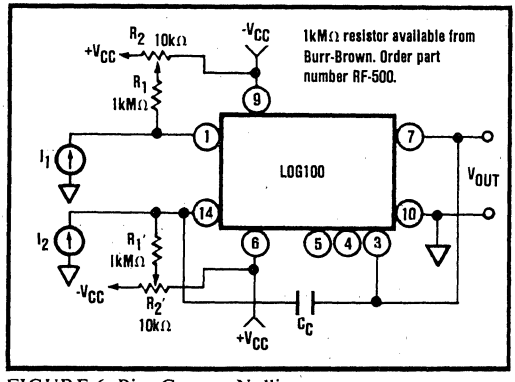


FIGURE 6. Bias Current Nulling.

OUTPUT OFFSET

The output offset may be nulled with the circuit in Figure 7. I_1 and I_2 are set equal at some convenient value in the range of 100nA to 100μA. R_1 is then adjusted for zero output voltage.

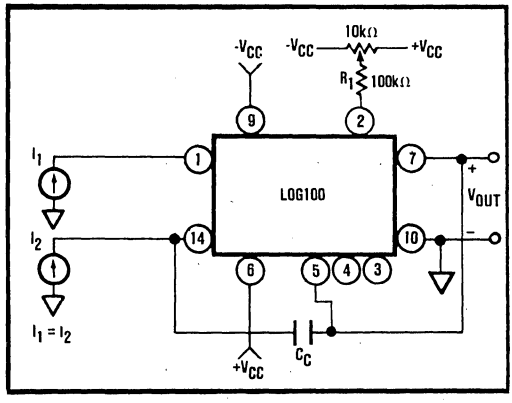


FIGURE 7. Output Offset Nulling.

ADJUSTMENTS OF SCALE FACTOR K

The value of K may be changed by increasing or decreasing the voltage divider resistor normally connected to the output, pin 7. To increase K put resistance in series between pin 7 and the appropriate scaling resistor pin (3, 4 or 5). To decrease K place a parallel resistor between pin 2 and either pin 3, 4 or 5.

APPLICATION INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins to the power supply common. The connection of these capacitors should be as close to the LOG100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 100pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the LOG100's output. This resistor will, of course, form a voltage divider with other resistive loads.

CIRCUIT PROTECTION

The LOG100 can be protected against accidental power supply reversal by putting a diode (1N4001 type) in series with each power supply line as shown in Figure 8. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off. If this protection circuit is used, the accuracy of the LOG100 will be degraded slightly by the voltage drops across the diodes as determined by the power supply sensitivity specification.

The LOG100 uses small geometry FET transistors to achieve the low input bias currents. Normal FET handling techniques should be used to avoid damage caused by low energy electrostatic discharge (ESD).

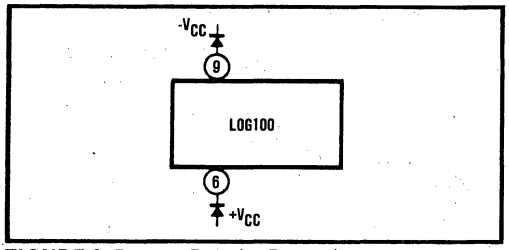


FIGURE 8. Reverse Polarity Protection.

LOG RATIO

One of the more common uses of log ratio amplifiers is to measure absorbance. A typical application is shown in Figure 9.

Absorbance of the sample is: $A = \log \frac{\lambda_1'}{\lambda_1}$ (22)

If $\lambda_2 = \lambda_1$ and D_1 and D_2 are matched $A \propto K \log \frac{I_1}{I_2}$. (23)

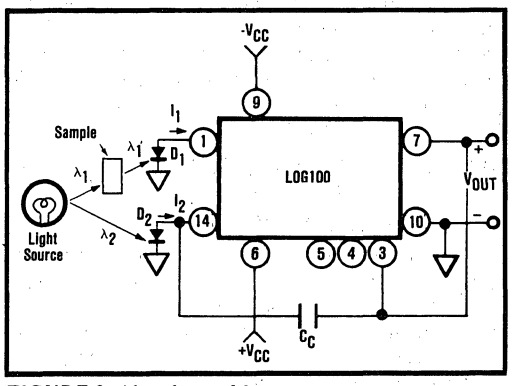


FIGURE 9. Absorbance Measurement.

DATA COMPRESSION

In many applications the compressive effects of the logarithmic transfer function is useful. For example, a LOG100 preceding an 8-bit analog-to-digital converter can replace a more expensive 20-bit converter.

SELECTING OPTIMUM VALUES OF I_2 AND K

In straight log applications (as opposed to log ratio) both K and I_2 are selected by the designer. In order to minimize errors due to output offset and noise it is normally best to scale the log amp to use as much of the ±10V output range as possible. Thus, with the range of I_1 from $I_{1\,MIN}$ to $I_{1\,MAX}$;

For $I_{1\,MAX}$ $+10V = K \log I_{1\,MAX}/I_2$ (24)

For $I_{1\,MIN}$ $-10V = K \log I_{1\,MIN}/I_2$ (25)

Addition of these two equations and solving for I_2 shows that its optimum value, $I_{2\,OPT}$, is the geometric mean of $I_{1\,MAX}$ and $I_{1\,MIN}$.

$$I_{2\,OPT} = \sqrt{I_{1\,MAX} \times I_{1\,MIN}} \quad (26)$$

$$K_{OPT} = \frac{10}{\log \frac{I_{1\,MAX}}{I_{2\,OPT}}} \quad (27)$$

Since K is selectable in discrete steps, use the largest value of K available which does not exceed K_{OPT}.

NEGATIVE INPUT CURRENTS

The LOG100 will function only with positive input currents (conventional current flow into pins 1 and 14). Some current sources (such as photomultiplier tubes) provide negative input currents. In such situations the circuit in Figure 10 may be used.

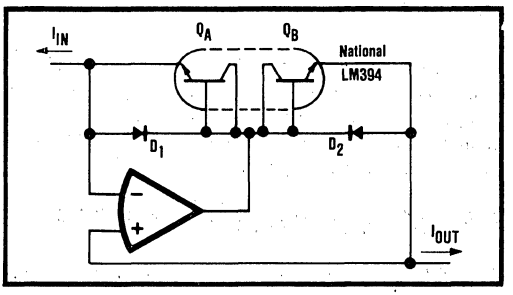


FIGURE 10. Current Inverter.

VOLTAGE INPUTS

The LOG100 gives the best performance with current inputs. Voltage inputs may be handled directly with series resistors, but the dynamic input range is limited to approximately three decades of input voltage by voltage noise and offsets. The transfer function of equation (20) applies to this configuration.

ANTILOG CONFIGURATION (an implicit technique)

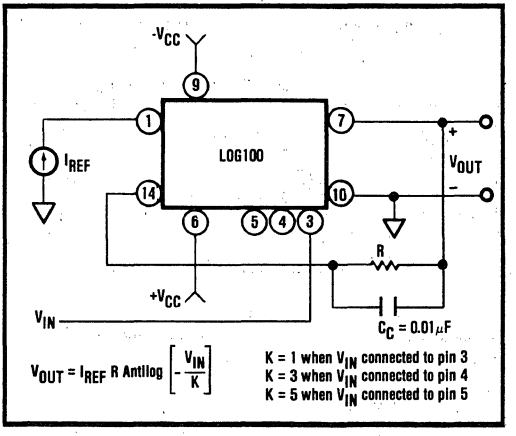


FIGURE 11. Connections for Antilog Function.

BURR-BROWN®

MPY100

MULTIPLIER-DIVIDER

FEATURES

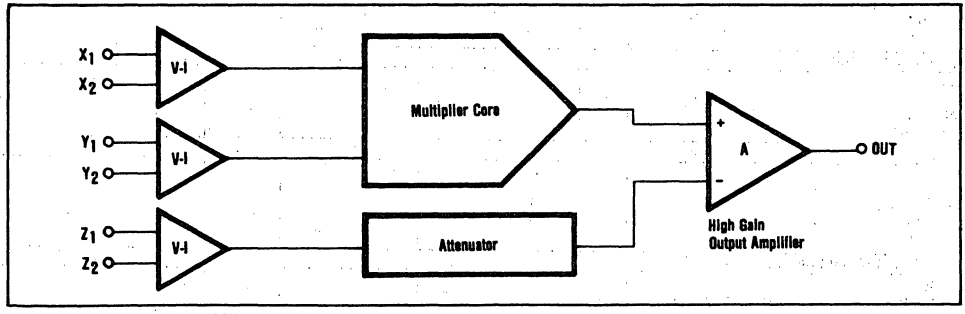
- LOW COST
- DIFFERENTIAL INPUT
- ACCURACY 100% TESTED AND GUARANTEED
- NO EXTERNAL TRIMMING REQUIRED
- LOW NOISE
  90μV, rms, 10Hz to 10kHz
- HIGHLY RELIABLE ONE-CHIP DESIGN
- DIP OR TO-100 TYPE PACKAGE
- WIDE TEMPERATURE OPERATION

APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOT
- LINEARIZATION
- POWER COMPUTATION
- ANALOG SIGNAL PROCESSING
- ALGEBRAIC COMPUTATION
- TRUE RMS-TO-DC CONVERSION

DESCRIPTION

The MPY100 multiplier-divider is a low cost precision device designed for general purpose application. In addition to four-quadrant multiplication, it also performs analog square root and division without the bother of external amplifiers or potentiometers. Laser-trimmed one-chip design offers the most in highly reliable operation with guaranteed accuracies. Because of the internal reference and pretrimmed accuracies the MPY100 does not have the restrictions of other low cost multipliers. It is available in both TO-100 and DIP ceramic packages.



MPY100 FUNCTIONAL BLOCK DIAGRAM

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_S$ = 15VDC unless otherwise noted.

MODEL		MPY100A			MPY100B/C			MPY100S			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
MULTIPLIER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$			*/*			•		
Total Error	-10V ≤ X, Y ≤ 10V										
Initial	T_A = +25°C			±2.0			±1.0/0.5			±0.5	% FSR
vs. Temperature	-25°C ≤ T_A ≤ +85°C		±0.017	±0.05		±0.008/0.008	±0.02/0.02				% FSR/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								±0.025	±0.05	% FSR/°C
vs. Supply(1)			±0.05			*/*			•		% FSR/%
Individual Errors											
Output Offset											
Initial	T_A = +25°C		±50	±100		±10/7	±50/25		±7	±50mV	mV
vs. Temperature	-25°C ≤ T_A ≤ +85°C		±0.7	±2.0		±0.7/0.3	±2.0/±0.7				mV/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								±0.3	±0.7	mV/°C
vs. Supply(1)			±0.25			*/*			•		mV/%
Scale Factor Error											
Initial	T_A = +25°C		±0.12			*/*			•		% FSR
vs. Temperature	-25°C ≤ T_A ≤ +85°C		±0.008			*/*					% FSR/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								±0.008		% FSR/°C
vs. Supply(1)			±0.05			*/*			•		% FSR/%
Nonlinearity											
X Input	X = 20V, p-p; Y = ±10VDC		±0.08			*/*			•		% FSR
Y Input	Y = 20V, p-p; X = ±10VDC		±0.08			*/*			•		% FSR
Feedthrough	f = 50Hz										
X Input	X = 20V, p-p; Y = 0		100			30/30			30		mV, p-p
Y Input	Y = 20V, p-p; X = 0		6			*/*			•		mV, p-p
vs. Temperature	-25°C ≤ T_A ≤ +85°C		0.1			*/*					mV, p-p/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								0.1		mV, p-p/°C
vs. Supply(1)			0.15			*/*			•		mV, p-p/%
DIVIDER PERFORMANCE											
Transfer Function	$X_1 > X_2$		$\frac{10(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			*/*			•		
Total Error (with	X = 10V										
external adjustments)	-10V ≤ Z ≤+10V		±1.5			±0.75/0.35			±0.35		% FSR
	X = 1V										
	-1V ≤ Z ≤ +1V		±4.0			±2.0/1.0			±1.0		% FSR
	+0.2V ≤ X ≤ +10V										
	-10V ≤ Z ≤ +10V		±5.0			±2.5/1.0			±1.0		% FSR
SQUARER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)^2}{10} + Z_2$			*/*			•		
Total Error	-10V ≤ X ≤ +10V		±1.2			±0.6/0.3			±0.3		% FSR
SQUARE-ROOTER PERFORMANCE											
Transfer Function	$Z_1 < Z_2$		$+\sqrt{10(Z_2 - Z_1)} + X_2$			*/*			•		
Total Error	1V ≤ Z ≤ 10V		±2			±1/0.5			±0.5		% FSR
AC PERFORMANCE											
Small-Signal Bandwidth			550			*/*			•		kHz
1% Amplitude Error	Small-Signal		70			*/*			•		kHz
1% (0.57°) Vector Error	Small-Signal		5			*/*			•		kHz
Full Power Bandwidth	$\|V_o\|$ = 10V, R_L = 2kΩ		320			*/*			•		kHz
Slew Rate	$\|V_o\|$ = 10V, R_L = 2kΩ		20			*/*			•		V/μsec
Settling Time	ε = ±1%, ΔV_o = 20V		2			*/*			•		μsec
Overload Recovery	50% Output Overload		0.2			*/*			•		μsec
INPUT CHARACTERISTICS											
Input Voltage Range											
Rated Operation		±10			*/*			•			V
Absolute Maximum				±Vcc			*/*			•	V
Input Resistance	X, Y, Z(2)		10			*/*			•		MΩ
Input Bias Current	X, Y, Z		1.4			*/*			•		μA
OUTPUT CHARACTERISTICS											
Rated Output											
Voltage	I_o = ±5mA	±10			*/*			•			V
Current	V_o = ±10V	±5			*/*			•			mA
Output Resistance	f = DC		1.5			*/*			•		Ω
OUTPUT NOISE VOLTAGE	X = Y = 0										
f_o = 1Hz			6.2			*/*			•		μV/√Hz
f_o = 1kHz			0.6			*/*			•		μV/√Hz
1/f Corner Frequency			110			*/*			•		Hz
f_B = 5Hz to 10kHz			60			*/*			•		μV, rms
f_B = 5Hz to 5MHz			1.3			*/*			•		mV, rms
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			*/*			•		VDC
Operating Range	Derated Performance	±8.5		±20	*/*		*/*	•		•	VDC
Quiescent Current			±5.5			*/*			*/*		mA

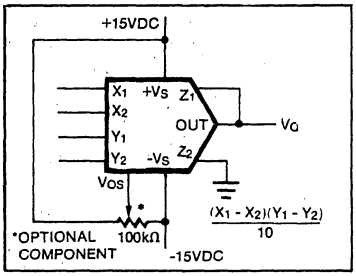
ELECTRICAL SPECIFICATIONS (CONT)

MODEL		MPY100A			MPY100B/C			MPY100S			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TEMPERATURE RANGE (Ambient)											
Specification	Derated Performance	-25		+85	*/*		*/*	-55		+125	°C
Operating Range		-55		+125	*/*		*/*	*		*	°C
Storage		-65		+150	*/*		*/*	*		*	°C

NOTES:
1. Includes effects of recommended null pots.
2. Z_2 input resistance is 10MΩ, typical, with V_{OS} pin open. If V_{OS} pin is grounded or used for optional offset adjustment, the Z_2 input resistance may be as low as 25kΩ.

*Same as MPY100A specification.
/ means B/C grades same as MPY100A specification.

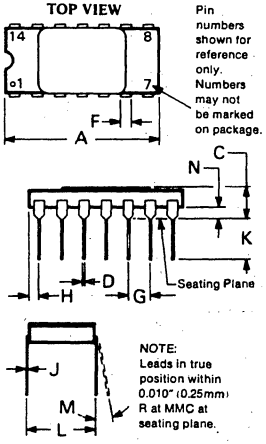
CONNECTION DIAGRAM



MECHANICAL

CERAMIC DUAL-IN-LINE PACKAGE

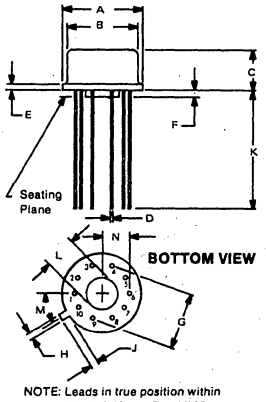
Order Number:
MPY100AG, MPY100BG
MPY100CG, MPY100SG



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.009	.060	0.23	1.52

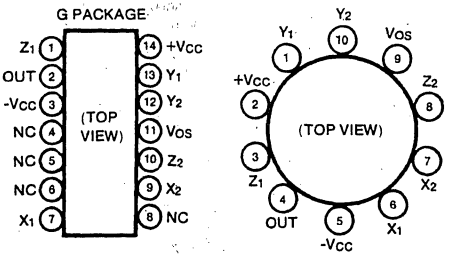
METAL CAN PACKAGE

Order Number:
MPY100AM, MPY100BM
MPY100CM, MPY100SM



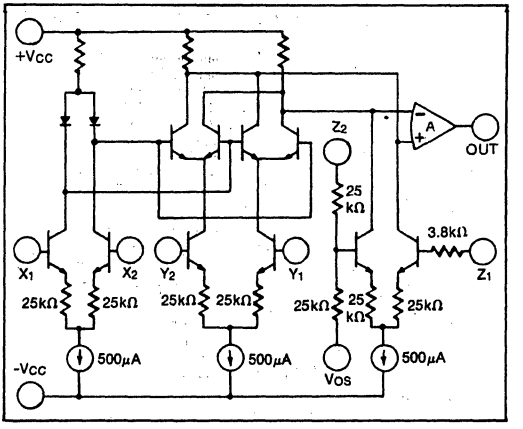
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	---	12.70	---
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

PIN CONFIGURATION



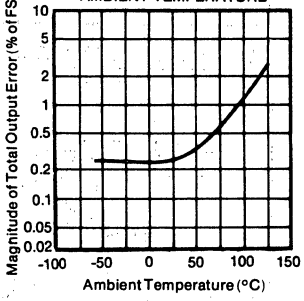
NOTES:
1. V_{OS} adjustment optional not normally recommended. V_{OS} pin may be left open or grounded.
2. All unused input pins should be grounded.

SIMPLIFIED SCHEMATIC

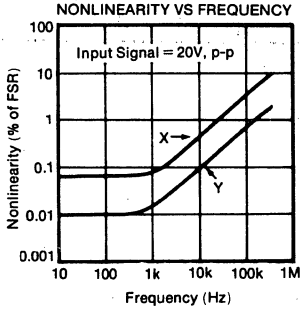


TYPICAL PERFORMANCE CURVES

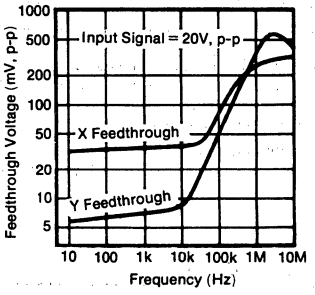
TOTAL ERROR VS AMBIENT TEMPERATURE



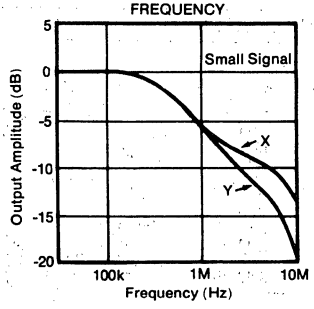
NONLINEARITY VS FREQUENCY



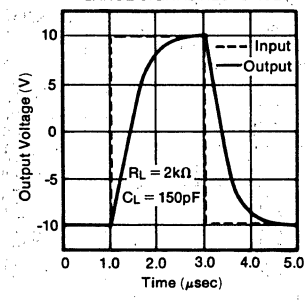
FEEDTHROUGH VS FREQUENCY



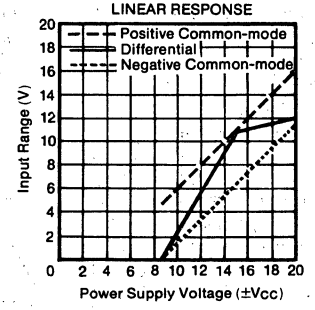
OUTPUT AMPLITUDE VS FREQUENCY



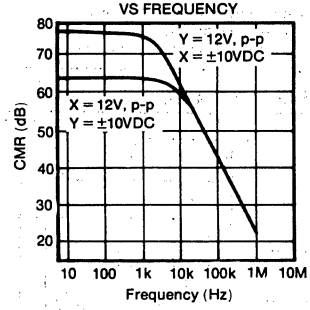
LARGE SIGNAL RESPONSE



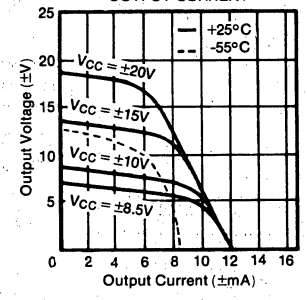
INPUT VOLTAGE FOR LINEAR RESPONSE



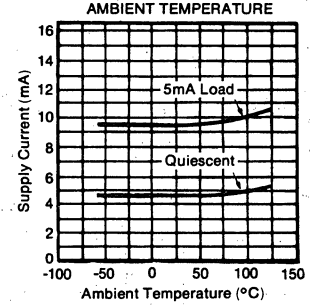
COMMON-MODE REJECTION VS FREQUENCY



OUTPUT VOLTAGE VS OUTPUT CURRENT



SUPPLY CURRENT VS AMBIENT TEMPERATURE



ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	500mW
Differential Input Voltage(2)	±40VDC
Input Voltage Range(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-circuit Duration(3)	Continuous
Junction Temperature	+150°C

NOTES:
1. Package must be derated on θ_{JC} = 15°C/W and θ_{JA} = 165°C/W for the metal package and θ_{JC} = 35°C/W and θ_{JA} = 220°C/W for the ceramic package.
2. For supply voltages less than ±20VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground only. Rating applies to +85°C ambient for the metal package and +65°C for the ceramic package.

APPLICATIONS INFORMATION

THEORY OF OPERATION

The MPY100 is a variable transconductance multiplier consisting of three differential voltage-to-current converters, a multiplier core and an output differential amplifier as illustrated in Figure 1.

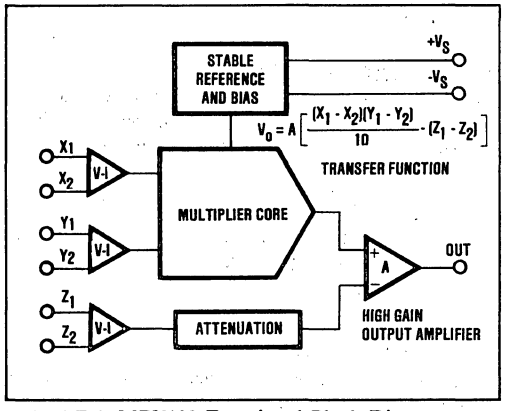


FIGURE 1. MPY100 Functional Block Diagram.

The basic principle of the transconductance multiplier can be demonstrated by the differential stage in Figure 2.

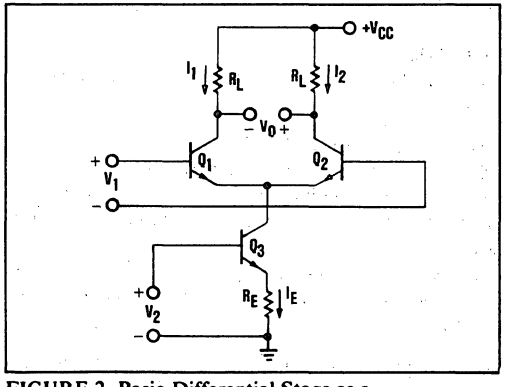


FIGURE 2. Basic Differential Stage as a Transconductance Multiplier.

For small values of the input voltage V_1 that are much smaller than V_T, the transistor's thermal voltage, the differential output voltage V_o is

$$V_o = g_m R_L V_i.$$

The transconductance g_m of the stage is given by:

$$g_m = I_E / V_T,$$

and is modulated by the voltage V_2 to give

$$g_m \approx V_2 / V_T R_E.$$

Substituting this into the original equation yields the overall transfer function

$$V_o \doteq g_m R_L V_1 = V_1 V_2 (R_L / V_T R_E)$$

which shows the output voltage to be the product of the two input voltages, V_1 and V_2.

Variations in I_E due to V_2 cause a large common-mode voltage swing in the circuit. The errors associated with this common-mode voltage can be eliminated by using two differential stages in parallel and cross-coupling their outputs as shown in Figure 3.

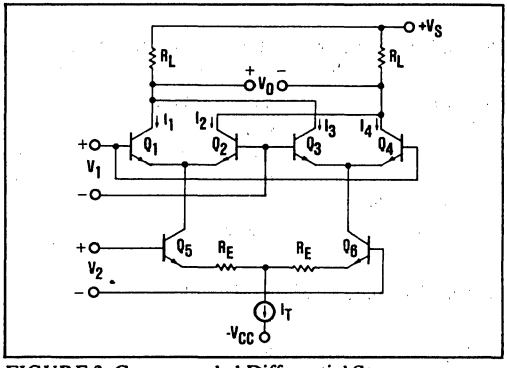


FIGURE 3. Cross-coupled Differential Stages as a Variable-transconductance Multiplier.

An analysis of the circuit in Figure 3 shows it to have the same overall transfer function as before:

$$V_o = V_1 V_2 (R_L / V_T R_E).$$

For input voltages larger than V_T the voltage-to-current transfer characteristics of the differential pair Q_1, Q_2 or Q_3 and Q_4 are no longer linear. Instead, their collector currents are related to the applied voltage V_1 as

$$\frac{I_1}{I_2} = \frac{I_3}{I_4} = e^{\frac{V_1}{V_T}}$$

The resultant nonlinearity can be overcome by developing V_1 logarithmically to exactly cancel the exponential relationship just derived. This is done by diodes D_1 and D_2 in Figure 4.

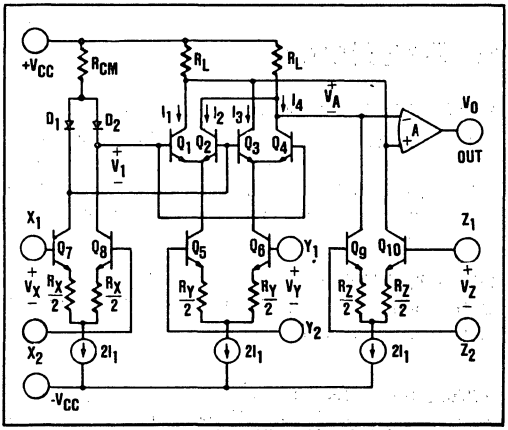


FIGURE 4. MPY100 Simplified Circuit Diagram.

The emitter degeneration resistors R_X and R_Y, in Figure 4, provide a linear conversion of the input voltages to differential current I_X and I_Y, where

$$I_X = V_X/R_X \text{ and } I_Y = V_Y/R_Y.$$

Analysis of Figure 4 shows the voltage V_A to be

$$V_A = (2R_L/I_I)(I_X I_Y).$$

Since I_X and I_Y are linearly related to the input voltages V_X and V_Y, V_A may also be written

$$V_A = KV_XV_Y$$

where K is a scale factor. In the MPY100, K is chosen to be 0.1.

The addition of the Z input alters the voltage V_A to

$$V_A = KV_XV_Y - V_Z.$$

Therefore, the output of the MPY100 is

$$V_o = A[KV_XV_Y - V_Z]$$

where A is the open-loop gain of the output amplifier. Writing this last equation in terms of the separate inputs to the MPY100 gives

$$V_o = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} - (Z_1 - Z_2)\right],$$

the transfer function of the MPY100.

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{EC}$ pins of the MPY100 to the power supply common. The connection of these capacitors should be as close to the MPY100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root mode for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the MPY100's output.

DEFINITIONS

TOTAL ERROR (Accuracy)

Total error is the actual departure of the multiplier output voltage from the ideal product of its input voltages. It includes the sum of the effects of input and output DC offsets, gain error and nonlinearity.

OUTPUT OFFSET

Output offset is the output voltage when both inputs V_X and V_Y are zero volts.

SCALE FACTOR ERROR

Scale factor error is the difference between the actual scale factor and the ideal scale factor.

NONLINEARITY

Nonlinearity is the maximum deviation from a best straightline (curve fitting on input-output graph) expressed as a percent of peak-to-peak full scale output.

FEEDTHROUGH

Feedthrough is the signal at the output for any value of V_X or V_Y within the rated range, when the other input is zero.

SMALL SIGNAL BANDWIDTH

Small signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value for a nominal output amplitude of 10% of full scale.

1% AMPLITUDE ERROR

The 1% amplitude error is the frequency the output amplitude is in error by 1%, measured with an output amplitude of 10% of full scale.

1% VECTOR ERROR

The 1% vector error is the frequency at which a phase error of 0.01 radians (0.57°) occurs. This is the most sensitive measure of dynamic error of a multiplier.

TYPICAL APPLICATIONS

MULTIPLICATION

Figure 5 shows the basic connection for four-quadrant multiplication.

The MPY100 meets all of its specifications without trimming. Accuracy can, however be improved over a limited range by nulling the output offset voltage using the 100kΩ optional balance potentiometer shown in Figure 5.

AC feedthrough may be reduced to a minimum by applying an external voltage to the X or Y input as shown in Figure 6.

Z_2, the optional summing input, may be used to sum a voltage into the output of the MPY100. If not used, this

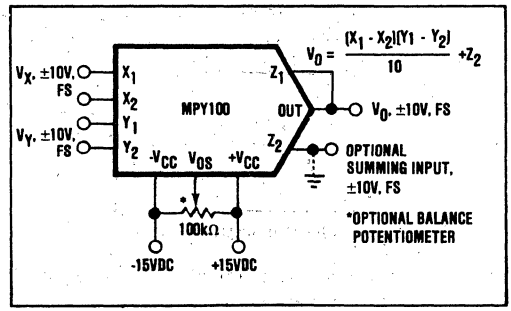


FIGURE 5. Multiplier Connection.

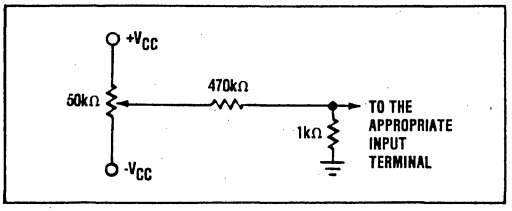


FIGURE 6. Optional Trimming Configuration.

terminal, as well as the X and Y input terminals, should be grounded. All inputs should be referenced to power supply common.

Figure 7 shows how to achieve a scale factor larger than the nominal 1/10. In this case, the scale factor is unity which makes the transfer function

$$V_o = KV_XV_Y = K(X_1 - X_2)(Y_1 - Y_2).$$

$$K = \frac{1 + (R_1/R_2)}{10}$$

$$0.1 \leq K \leq 1$$

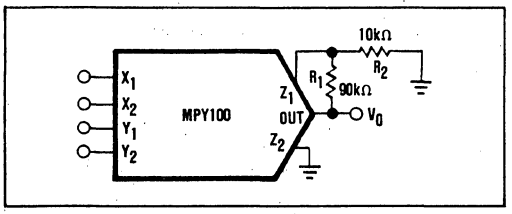


FIGURE 7. Connection For Unity Scale Factor.

This circuit has the disadvantage of increasing the output offset voltage by a factor of 10 which may require the use of the optional balance control as in Figure 1 for some applications. In addition, this connection reduces the small signal bandwidth to about 50kHz.

DIVISION

Figure 8 shows the basic connection for two-quadrant division. This configuration is a multiplier-inverted analog divider, i.e., a multiplier connected in the feedback loop of an operational amplifier. In the case of the MPY100 this operational amplifier is the output amplifier shown in Figure 1.

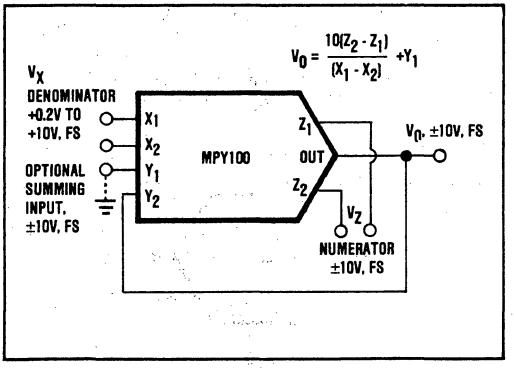


FIGURE 8. Divider Connection.

The divider error with a multiplier-inverted analog divider is approximately

$$\epsilon_{divider} = 10\,\epsilon_{multiplier}/(X_1 - X_2)$$

It is obvious from this error equation that divider error becomes excessively large for small values of $X_1 - X_2$. A 10-to-1 denominator range is usually the practical limit. If more accurate division is required over a wide range of denominator voltages, an externally generated voltage may be applied to the unused X-input (see Optional Trim Configuration). To trim, apply a ramp of +100mV to +1V at 100Hz to both X_1 and Z_1 if X_2 is used for offset adjustment, otherwise reverse the signal polarity, and adjust the trim voltage to minimize the variation in the output. An alternative to this procedure would be to use the Burr-Brown DIV100, a precision log-antilog divider.

SQUARING

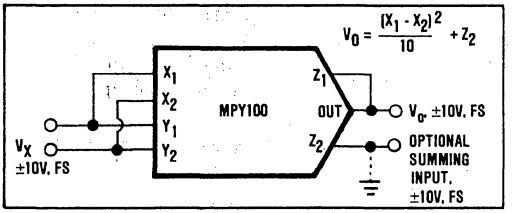


FIGURE 9. Squarer Connection.

SQUARE ROOT

Figure 10 shows the connection for taking the square root of the voltage V_Z. The diode prevents a latching condition which could occur if the input momentarily changed polarity. This latching condition is not a design flaw in the MPY100, but occurs when a multiplier is connected in the feedback loop of an operational amplifier to perform square root functions.

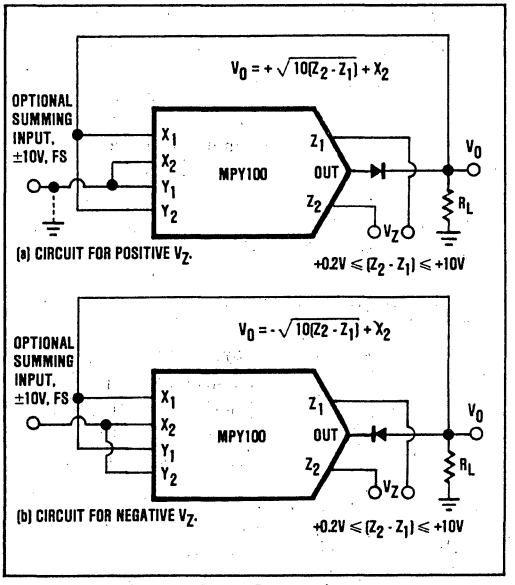


FIGURE 10. Square Root Connection.

The load resistance R_L must be in the range of $10k\Omega \leq R_L \leq 1M\Omega$. This resistance must be in the circuit as it provides the current necessary to operate the diode.

BRIDGE LINEARIZATION

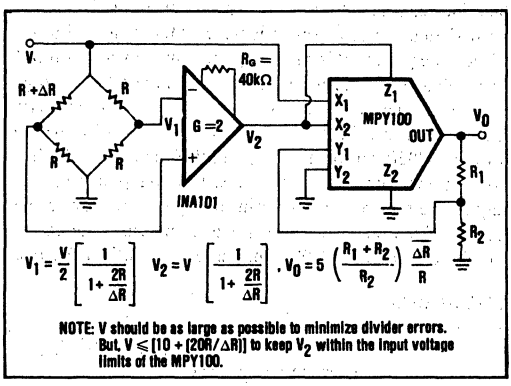


FIGURE 11. Bridge Linearization.

The use of the MPY100 to linearize the output from a bridge circuit makes the output V_o independent of the bridge supply voltage.

TRUE RMS-TO-DC CONVERSION

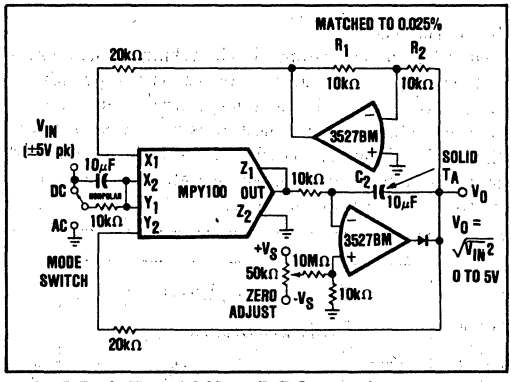


FIGURE 12. True RMS-to-DC Conversion.

The rms-to-DC conversion circuit of Figure 12 gives greater accuracy and bandwidth but with less dynamic range than most rms-to-DC converters.

PERCENTAGE COMPUTATION

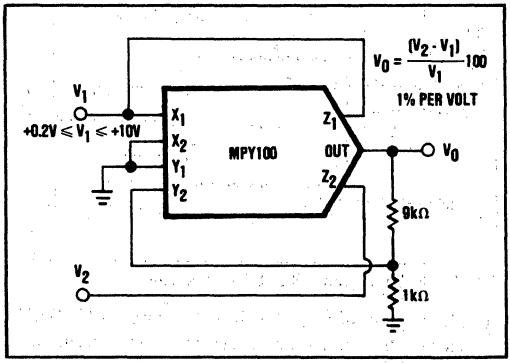


Figure 13. Percentage Computation.

The circuit of Figure 13 has a sensitivity of 1V/% and is capable of measuring 10% deviations. Wider deviation can be measured by decreasing the ratio of R_2/R_1.

SINE FUNCTION GENERATOR

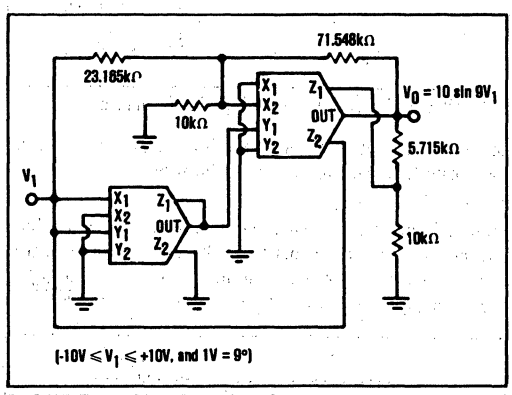


FIGURE 14. Sine Function Generator.

The circuit in Figure 14 uses implicit feedback to implement the following sine function approximation:

$$V_o = (1.5715V_1 - 0.004317V_1^3)/(1 + 0.001398V_1^2)$$
$$= 10 \sin (9V_1).$$

SINGLE-PHASE POWER MEASUREMENT

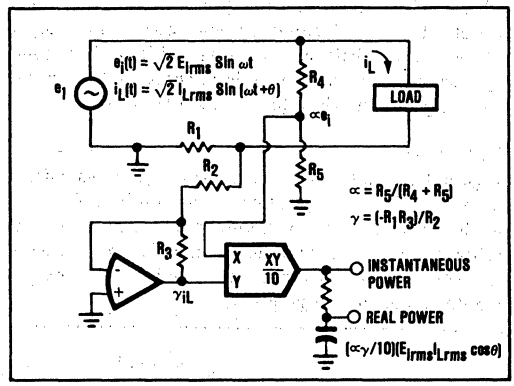


FIGURE 15. Single-Phase Instantaneous and Real Power Measurement.

MORE CIRCUITS

The theory and procedures for developing virtually any function generator or linearization circuit can be found in the Burr-Brown/McGraw Hill book "FUNCTION CIRCUITS - Design and Applications."

BURR-BROWN®

MPY534

Precision ANALOG MULTIPLIER

FEATURES

- ±0.25% MAX 4-QUADRANT ERROR
- WIDE BANDWIDTH: 1MHz MIN, 3MHz TYP
- ADJUSTABLE SCALE FACTOR: GAINS TO 100
- STABLE AND RELIABLE MONOLITHIC CONSTRUCTION
- LOW COST

APPLICATIONS

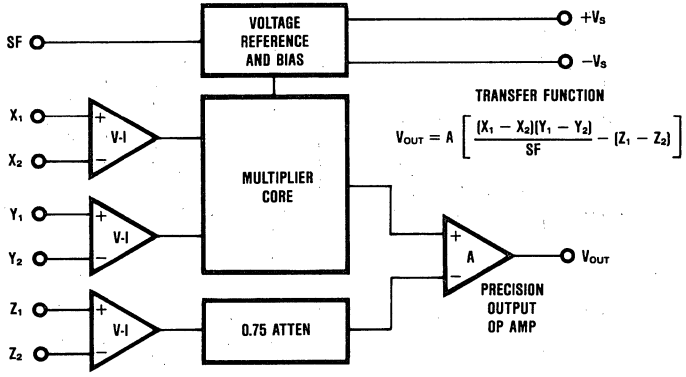
- PRECISION ANALOG SIGNAL PROCESSING
- VIDEO SIGNAL PROCESSING
- VOLTAGE CONTROLLED FILTERS AND OSCILLATORS
- MODULATION AND DEMODULATION
- RATIO AND PERCENTAGE COMPUTATION

DESCRIPTION

The MPY534 is a high accuracy, general purpose four-quadrant analog multiplier. Its accurately laser trimmed transfer characteristics make it easy to use in a wide variety of applications with a minimum of external parts and trimming circuitry. Its differential X, Y and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows accurate signal processing at higher frequencies suitable for video signal processing. It is capable of performing IF and RF frequency mixing, modulation and demodulation with excellent carrier rejection and very simple feedthrough adjustment.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user selected scale factors from 0.1 to 10 using external feedback resistors.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_S = ±15VDC unless otherwise specified.

MODEL	MPY534J			MPY534K			MPY534L			MPY534S			MPY534T			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
MULTIPLIER PERFORMANCE																
Transfer Function		*			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$			*			*			*		
Total Error[1]																
(−10V ≤ X, Y ≤ +10V)			±1.0			±0.5			±0.25			±1.0			*	%
T_A = min to max		±1.5			±1.0			±0.5				±2.0			±1.0	%
Total Error vs Temperature		±0.022			±0.015			±0.008				±0.02			±0.01	%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1			*			±0.25			*		%
Temperature Coefficient of Scaling Voltage		±0.02			±0.01			±0.005			±0.02				±0.005	%/°C
Supply Rejection (±15V ±1V)		*			±0.01			*			*			*		%
Nonlinearity:																
X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	±0.3		±0.10	±0.12		±0.4			*	*	%
Y (Y = 20V pk-pk, X = 10V)		*			±0.01	±0.1		±0.005	*		*			*	*	%
Feedthrough[3]																
X (Y Nulled, Y = 20V pk-pk, 50Hz)		±0.3			±0.15	±0.3		±0.05	±0.12		±0.3			*	*	%
Y (X Nulled, Y = 20V pk-pk, 50Hz)		*			±0.01	±0.1		±0.003	*		*			*	*	%
Output Offset Voltage		±5	±30		±2	±15		*	±10		±5	±30		*	*	mV
Output Offset Voltage Drift		200			100			*				500			300	µV/°C
DYNAMICS																
Small Signal BW, (V_{OUT} = 0.1V rms)	*	*		1	3		*	*		*	*		*	*		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		*			50			*			*			*		kHz
Slew Rate (V_{OUT} = 20V pk-pk)		*			20			*			*			*		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		*			2			*			*			*		µs
NOISE																
Noise Spectral Density: SF = 10V		*			0.8			*			*			*		$\mu V/\sqrt{Hz}$
Wideband Noise:																
f = 10Hz to 5MHz		*			1			*			*			*		mV/rms
f = 10Hz to 10kHz		*			90			*			*			*		µV/rms
OUTPUT																
Output Voltage Swing	*			±11			*			*			*			V
Output Impedance (f ≤ 1kHz)		*			0.1			*			*			*		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		*			30			*			*			*		mA
Amplifier Open Loop Gain (f = 50Hz)		*			70			*			*			*		dB
INPUT AMPLIFIERS (X, Y and Z)																
Signal Voltage Range																
Differential or Common-Mode		*			±10			*			*			*		V
Operating Differential		*			±12			*			*			*		V
Offset Voltage X, Y		±5	±20		±2	±10		*	*		±5	±20		*	*	mV
Offset Voltage Drift X, Y		100			50			*			100			*		µV/°C
Offset Voltage Z		±5	±30		±2	±15		*	±10		±5	±30		*	*	mV
Offset Voltage Drift Z		200			100			*				500			300	µV/°C
CMRR	60	80		70	90		*	*		60	80		*	*		dB
Bias Current		*	*		0.8	2.0		*	*		*	*		*	*	µA
Offset Current		*			0.1			0.05	0.2		*	2.0		*	2.0	µA
Differential Resistance		*			10			*			*			*		MΩ
DIVIDER PERFORMANCE																
Transfer Function ($X_1 > X_2$)		*			$10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$											
Total Error[1]																
(X = 10V, −10V ≤ Z ≤ +10V)		±0.75			±0.35			±0.2			±0.75			*		%
(X − 1V, −1V ≤ Z ≤ +1V)		±2.0			±1.0			±0.8			±2.0			*		%
(0.1V ≤ X ≤ 10V, −10V ≤ Z ≤ 10V)		±2.5			±1.0			±0.8			±2.5			*		%

*Specifications same as for MPY534K.

ELECTRICAL (CONT)

At T_A = +25°C and V_S = ±15VDC unless otherwise specified.

MODEL	MPY534J			MPY534K			MPY534L			MPY534S			MPY534T			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SQUARE PERFORMANCE																
Transfer Function		•		$\frac{(X_1 - X_2)^2}{10V} + Z_2$				•			•			•		
Total Error (−10V ≤ X ≤10V)		0.6			±0.3			±0.2			±0.6			•		%
SQUARE-ROOTER PERFORMANCE																
Transfer Function ($Z_1 \leq Z_2$)		•		$\sqrt{10V(Z_2 - Z_1)} + X_2$				•			•			•		
Total Error[1] (1V ≤ Z ≤ 10V)		±1.0			±0.5			±0.25			±1.0			±0.5		%
POWER SUPPLY																
Supply Voltage:																
Rated Performance		•			±15			•			•			•		VDC
Operating	•	•	•	±8		±18	•		•	•		±20	•		±20	VDC
Supply Current, Quiescent		•	•		4	6		•	•		•	•		•	•	mA
TEMPERATURE RANGE																
Operating	•		•	0		+70	•		•	−55		+125	−55		+125	°C
Storage	•		•	−65		+150	•		•	•		•	•		•	°C

*Specification same as for MPY534K.

NOTES: (1) Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV). (2) May be reduced to 3V using external resistor between −V_S and SF. (3) Irreducible component due to nonlinearity; excludes effect of offsets.

ABSOLUTE MAXIMUM RATINGS

Parameter	MPY534J, K, L	MPY534S, T
Power Supply Voltage	±18	±20
Power Dissipation	500mW	•
Output Short-Circuit to Ground	Indefinite	•
Input Voltage (all X, Y and Z)	±V_S	•
Operating Temperature Range	0°C to +70°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	•
Lead Temperature (10s soldering)	300°C	•

*Specification same as for MPY534K.

MPY534**

Grade Designation

J, K, L } 0 to 70°C

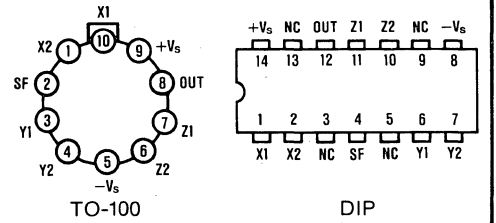
S, T } −55 to 125°C

Package Designation

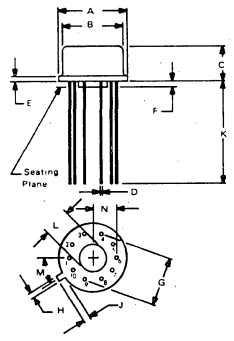
H = TO-100

D = DIP

PIN CONFIGURATION (TOP VIEW)



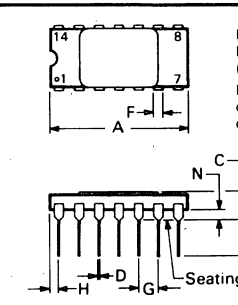
MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R at MMT at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05



NOTE:
Leads in true position within .010" (.25mm) R at MMT at seating plane.

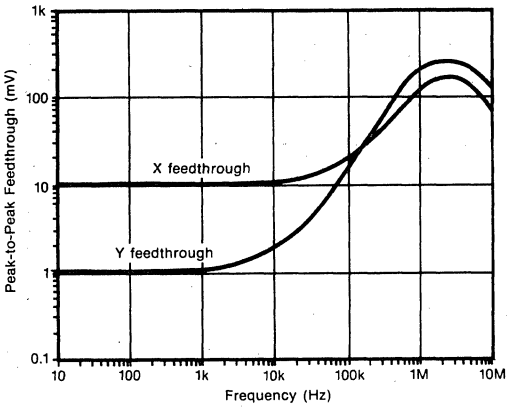
Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.009	.060	0.23	1.52

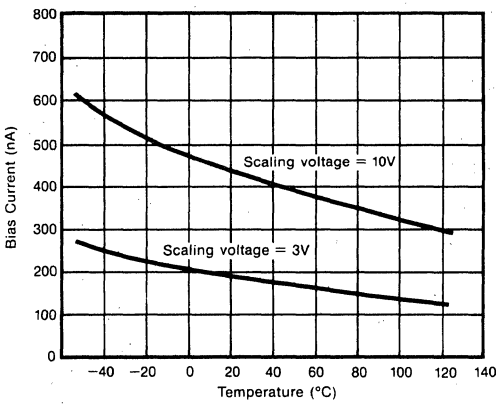
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

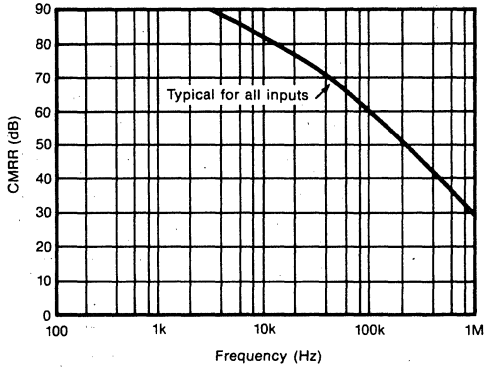
AC FEEDTHROUGH
VS FREQUENCY



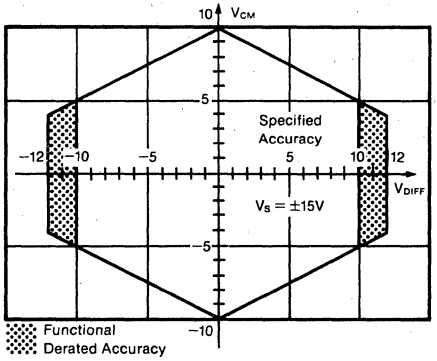
BIAS CURRENTS VS TEMPERATURE
(X, Y or Z inputs)



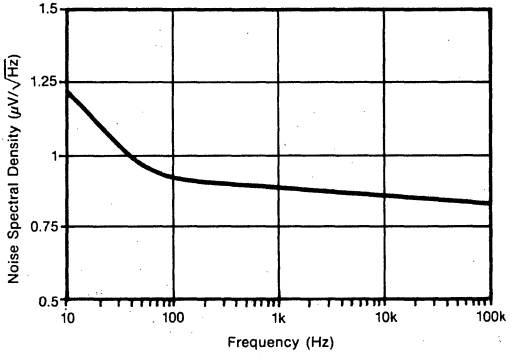
COMMON-MODE-REJECTION RATIO
VS FREQUENCY



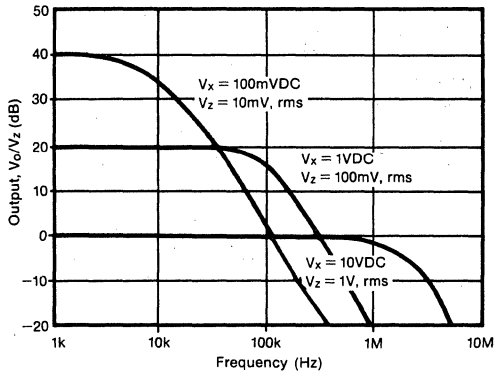
INPUT DIFFERENTIAL-MODE/
COMMON-MODE VOLTAGE

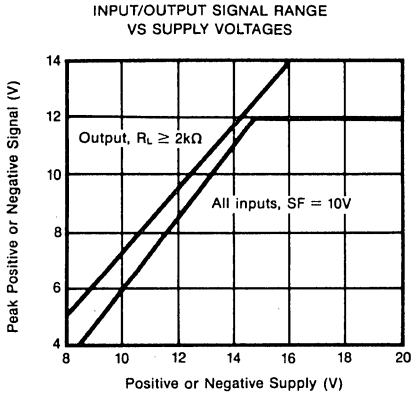


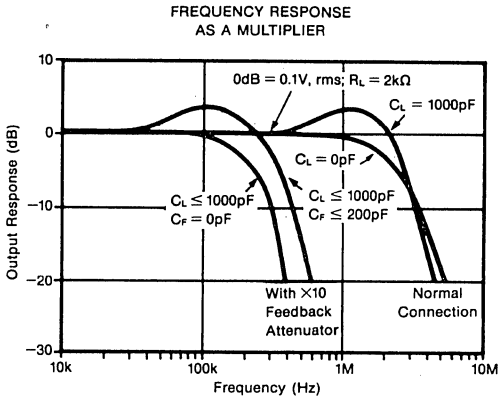
NOISE SPECTRAL DENSITY
VS FREQUENCY



FREQUENCY RESPONSE VS
DIVIDER DENOMINATOR INPUT VOLTAGE







THEORY OF OPERATION

The transfer function for the MPY534 is:

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right]$$

where:

A = Open-loop gain of the output amplifier (Typically 85dB at DC).

SF = Scale Factor. Laser-trimmed to 10V but adjustable over a 3V to 10V range using external resistor.

X, Y, Z are input voltages. Full-scale input voltage is equal to the selected SF. (Max input voltage = ±1.25 SF.)

An intuitive understanding of transfer function can be gained by analogy to an op amp. By assuming that the open-loop gain, A, of the output amplifier is infinite, inspection of the transfer function reveals that any V_{OUT} can be created with an infinitesimally small quantity within the brackets. Then, an application circuit can be analyzed by assigning circuit voltages for all X, Y and Z inputs and setting the bracketed quantity equal to zero. For example, the basic multiplier connection in Figure 1, $Z_1 = V_{OUT}$ and $Z_2 = 0$. The quantity within the brackets then reduces to:

$$\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (V_{OUT} - 0) = 0$$

This approach leads to a simple relationship which can be solved for V_{OUT}.

The scale factor is accurately factory-adjusted to 10V and is typically accurate to within 0.1% or less. The scale factor may be adjusted by connecting a resistor or potentiometer between pin SF and the $-V_S$ power supply. The value of the external resistor can be approximated by:

$$R_{SF} = 5.4k\Omega\left[\frac{SF}{10 - SF}\right]$$

Internal device tolerances make this relationship accurate to within approximately 25%. Some applications can benefit from reduction of the SF by this technique. The reduced input bias current and drift achieved by this technique can be likened to operating the input circuitry in a higher gain, thus reducing output contributions to these effects. Adjustment of the scale factor does not affect bandwidth.

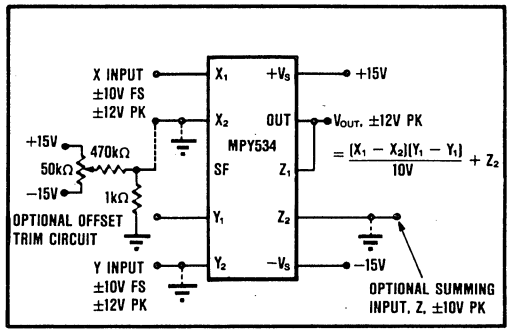


FIGURE 1. Basic Multiplier Connection.

The MPY534 is fully characterized at $V_S = \pm 15V$ but operation is possible down to ±8V with an attendant reduction of input and output range capability. Operation at voltages greater than ±15V allows greater output swing to be achieved by using an output feedback attenuator (Figure 2).

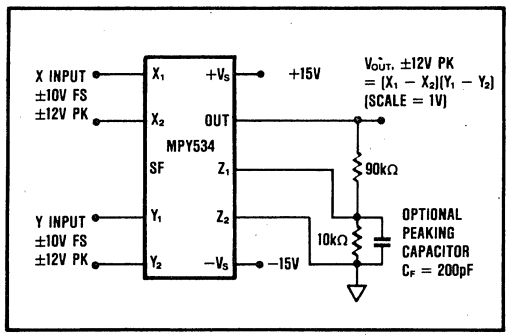


FIGURE 2. Connections for Scale-Factor of Unity.

BASIC MULTIPLIER CONNECTION

Figure 1 shows the basic connection as a multiplier. Accuracy is fully specified without any additional user trimming circuitry. Some applications can benefit from trimming one or more of the inputs. The fully differential inputs facilitate referencing the input quantities to the source voltage common terminal for maximum accuracy. They also allow use of simple offset voltage trimming circuitry as shown on the X input.

The differential Z input allows an offset to be summed in V_{OUT}. In basic multiplier operation the Z_2 input serves as the output voltage reference and should be connected to the ground reference of the driven system for maximum accuracy.

A method of changing (lowering) SF by connecting to the SF pin was discussed previously. Figure 2 shows another method of changing the effective SF of the overall circuit using an attenuator in the feedback connection to Z_1. This method puts the output amplifier in a higher gain and is thus accompanied by a reduction in bandwidth and an increase in output offset voltage. The larger output offset may be reduced by applying a trimming voltage to the high impedance input, Z_2.

The flexibility of the differential Z inputs allows direct conversion of the output quantity to a current. Figure 3 shows the output voltage differentially-sensed across a series resistor forcing an output-controlled current. Addition of a capacitor load then creates a time integration function useful in a variety of applications such as power computation.

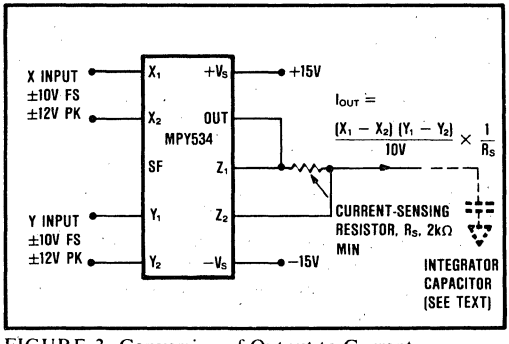


FIGURE 3. Conversion of Output to Current.

SQUARER CIRCUIT

Squarer operation is achieved by paralleling the X and Y inputs of the standard multiplier circuit. Inverted output can be achieved by reversing the differential input terminals of either the X or Y input. Accuracy in the squaring mode is typically a factor of two better than the specified multipler mode with maximum error occurring with small (less than 1V) inputs. Better accuracy can be achieved for small input voltage levels by using a reduced SF value.

DIVIDER OPERATION

The MPY534 can be configured as a divider as shown in Figure 4. High impedance differential inputs for the numerator and denominator are achieved at the Z and X inputs respectively. Feedback is applied to the Y_2 input, and Y_1 is normally referenced to output ground. Alternatively, as the transfer function implies, an input applied to Y_1 can be summed directly into V_{OUT}. Since the feedback connection is made to a multiplying input, the effective gain of the output op amp varies as a function of the denominator input voltage. Therefore the bandwidth of the divider function is proportional to the denominator voltage (see Typical Performance Curves).

Accuracy of the divider mode typically ranges from 0.75% to 2.0% for a 10 to 1 denominator range depending on device grade. Accuracy is primarily limited by input offset voltages and can be significantly improved by trimming the offset of the X input. A trim voltage of ±3.5mV applied to the "low side" X input (X_2 for positive input voltages on X_1) can produce similar accuracies over a 100 to 1 deonominator range. To trim, apply a signal which varies from 100mV to 10V at a low frequency (less than 500Hz) to both inputs. An offset sine wave or ramp is suitable. Since the ratio of the quantities should be constant, the ideal output would be a constant 10V. Using AC coupling on an oscilloscope, adjust the offset control for minimum output voltage variation.

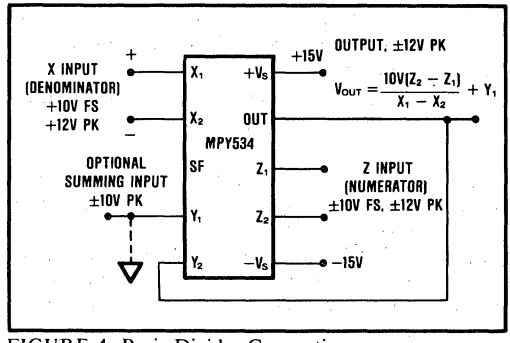


FIGURE 4. Basic Divider Connection.

SQUARE-ROOTER

A square-rooter connection is shown in Figure 5. Input voltage is limited to one polarity (positive for the connection shown). The diode prevents circuit latch-up

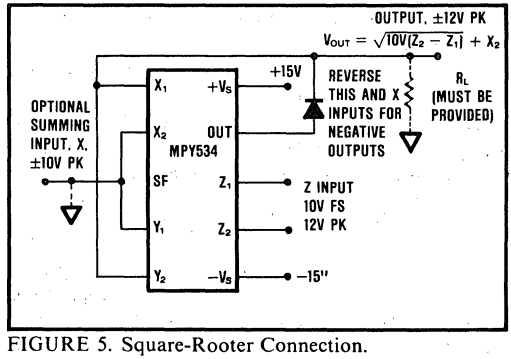


FIGURE 5. Square-Rooter Connection.

should the input go negative. The circuit can be configured for negative input and positive output by reversing the polarity of both the X and Y inputs. The output polarity can be reversed by reversing the diode and X input polarity. A load resistance of approximately 10kΩ must be provided. Trimming for improved accuracy would be accomplished at the Z input.

APPLICATIONS

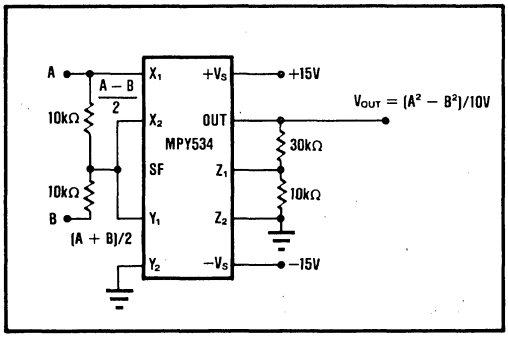


FIGURE 6. Difference-of-Squares.

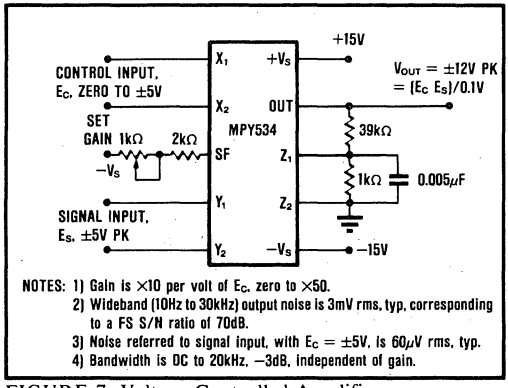


FIGURE 7. Voltage-Controlled Amplifier.

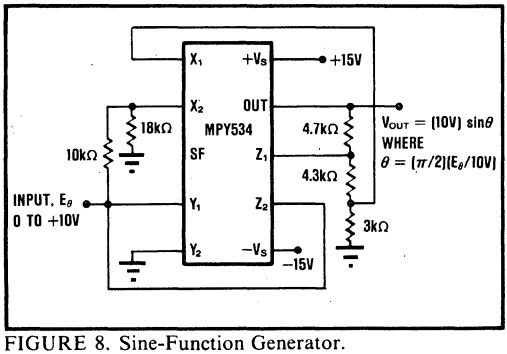


FIGURE 8. Sine-Function Generator.

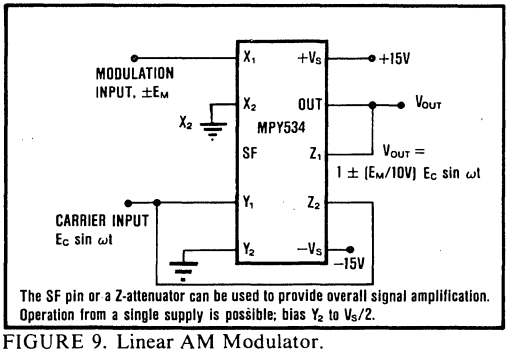


FIGURE 9. Linear AM Modulator.

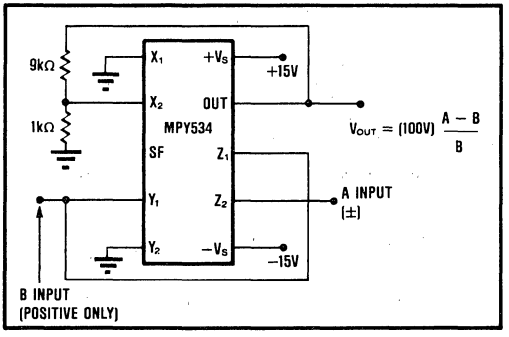


FIGURE 10. Percentage Computer.

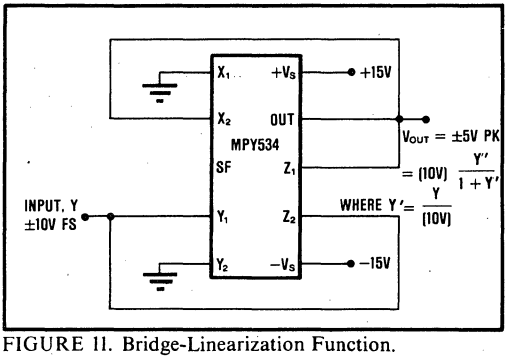


FIGURE 11. Bridge-Linearization Function.

BURR-BROWN®

MPY634

Wide Bandwidth PRECISION ANALOG MULTIPLIER

FEATURES

- WIDE BANDWIDTH: 10MHz TYP
- ±0.5% MAX 4-QUADRANT ERROR
- INTERNAL WIDE-BANDWIDTH OP AMP
- EASY TO USE
- LOW COST

APPLICATIONS

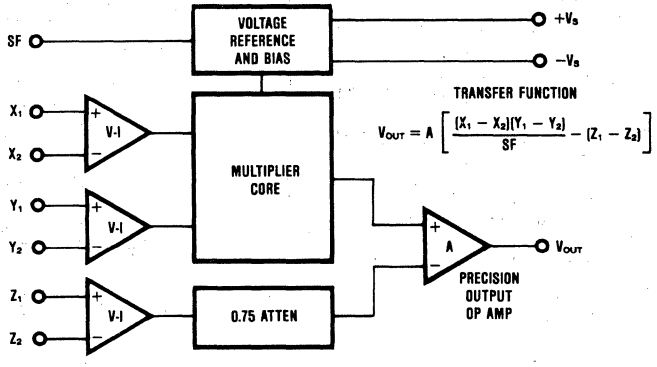
- PRECISION ANALOG SIGNAL PROCESSING
- MODULATION AND DEMODULATION
- VOLTAGE-CONTROLLED AMPLIFIERS
- VIDEO SIGNAL PROCESSING
- VOLTAGE-CONTROLLED FILTERS AND OSCILLATORS

DESCRIPTION

The MPY634 is a wide bandwidth, high accuracy, four-quadrant analog multiplier. Its accurately laser-trimmed multiplier characteristics make it easy to use in a wide variety of applications with a minimum of external parts, often eliminating all external trimming. Its differential X, Y, and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter, and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows signal processing at I.F., R.F., and video frequencies. The internal output amplifier of the MPY634 reduces design complexity compared to other high frequency multipliers and balanced modulator circuits. It is capable of performing frequency mixing, balanced modulation, and demodulation with excellent carrier rejection.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user-selected scale factors from 0.1 to 10 using external feedback resistors.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_S = ±15VDC unless otherwise specified.

MODEL	MPY634KP			MPY634AM			MPY634BM			MPY634SM			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
MULTIPLIER PERFORMANCE													
Transfer Function		•			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$			•			•		
Total Error[1]													
(−10V ≤ X, Y ≤ +10V)			±2.0			±1.0			±0.5			•	%
T_A = min to max		±2.5			±1.5			±1.0				±2.0	%
Total Error vs Temperature		±0.03			±0.022			±0.015				±0.02	%/°C
Scale Factor Error													
(SF = 10.000V Nominal)[2]		±0.25			±0.1			•			•		%
Temperature Coefficient of													
Scaling Voltage		±0.02			±0.01			±0.01			•		%/°C
Supply Rejection (±15V ±1V)		•			±0.01			•			•		%
Nonlinearity:													
X (X = 20V pk-pk, Y = 10V)		•			±0.4			0.2	±0.3		•		%
Y (Y = 20V pk-pk, X = 10V)		•			±0.01			•	±0.1		•		%
Feedthrough[3]													
X (Y Nulled, Y = 20V pk-pk, 50Hz)		±0.3			±0.3			±0.15	±0.3		•		%
Y (X Nulled, Y = 20V pk-pk, 50Hz)		•			±0.01			•	±0.1		•		%
Both Inputs (500kHz, 1V rms)													
Unnulled	40	50		45	55		•	60		•	•		dB
Nulled	55	60		55	65		60	70		•	•		dB
Output Offset Voltage		±50	±100		±5	±30		•	±15		•	•	mV
Output Offset Voltage Drift		•			±200			±100			•	±500	μV/°C
DYNAMICS													
Small Signal BW, Y Input													
(V_{OUT} = 0.1V rms)	6	•		6	10		8	•		6	•		MHz
1% Amplitude Error													
(C_{LOAD} = 1000pF)		•			100			•			•		kHz
Slew Rate (V_{OUT} = 20V pk-pk)		•			20			•			•		V/μs
Settling Time													
(to 1%, ΔV_{OUT} = 20V)		•			2			•			•		μs
NOISE													
Noise Spectral Density:													
SF = 10V		•			0.8			•			•		$\mu V/\sqrt{Hz}$
Wideband Noise:													
f = 10Hz to 5MHz		•			1			•			•		mV/rms
f = 10Hz to 10kHz		•			90			•			•		μV/rms
OUTPUT													
Output Voltage Swing	•			±11			•			•			V
Output Impedance (f ≤ 1kHz)		•			0.1			•			•		Ω
Output Short Circuit Current													
(R_L = 0, T_A = min to max)		•			30			•			•		mA
Amplifier Open Loop Gain													
(f = 50Hz)		•			85			•			•		dB
INPUT AMPLIFIERS (X, Y and Z)													
Signal Voltage Range													
Differential or Common-Mode		•			±10			•			•		V
Operating Differential		•			±12			•			•		V
Offset Voltage X, Y		±25	±100		±5	±20		±2	±10		•	•	mV
Offset Voltage Drift X, Y		200			100			50			•		μV/°C
Offset Voltage Z		±25	±100		±5	±30		±2	±15		•	•	mV
Offset Voltage Drift Z		•			200			100				500	μV/°C
CMRR	•	•		60	80		70	90		•	•		dB
Bias Current		•	•		0.8	2.0	•	•	•		•	•	μA
Offset Current		•			0.1			•			•	2.0	μA
Differential Resistance		•			10			•			•		MΩ
DIVIDER PERFORMANCE													
Transfer Function ($X_1 > X_2$)		•			$10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			•			•		
Total Error[1] untrimmed													
(X = 10V, −10V ≤ Z ≤ +10V)		1.5			±0.75			±0.35			±0.75		%
(X = 1V, −1V ≤ Z ≤ +1V)		4.0			±2.0			±1.0			•		%
(0.1V ≤ X ≤ 10V, −10V ≤ Z ≤ 10V)		5.0			±2.5			±1.0			•		%

ELECTRICAL (CONT)

At T_A = +25°C and V_S = ±15VDC unless otherwise specified.

MODEL	MPY634KP			MPY634AM			MPY634BM			MPY634SM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SQUARE PERFORMANCE													
Transfer Function		*		$\frac{(X_1 - X_2)^2}{10V} + Z_2$				*			*		
Total Error (−10V ≤ X ≤10V)		±1.2			±0.6			±0.3			*		%
SQUARE-ROOTER PERFORMANCE													
Transfer Function ($Z_1 \leq Z_2$)		*		$\sqrt{10V(Z_2 - Z_1)} + X_2$				*			*		
Total Error[1] (1V ≤ Z ≤ 10V)		±2.0			±1.0			±0.5			*		%
POWER SUPPLY													
Supply Voltage:													
Rated Performance		*			±15			*			*		VDC
Operating	*		*	±8		±18	*		*	*		±20	VDC
Supply Current, Quiescent		*	*		4	6		*	*		*	*	mA
TEMPERATURE RANGE													
Operating	*		*	−25		+85	*		*	−55		+125	°C
Storage	−40		+85	−65		+150	*		*	*		*	°C

*Specification same as for MPY634AM.

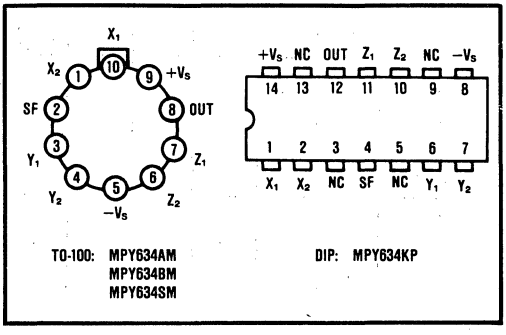
NOTES: (1) Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV). (2) May be reduced to 3V using external resistor between $-V_S$ and SF. (3) Irreducible component due to nonlinearity; excludes effect of offsets.

ABSOLUTE MAXIMUM RATINGS

Parameter	MPY634AM/BM/KP	MPY634SM
Power Supply Voltage	±18	±20
Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltage (all X, Y and Z)	±Vs	*
Operating Temperature Range	−25°C to +85°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature (10s soldering)	+300°C	*

* Specification same as for MPY634AM/BM/KP.

PIN CONFIGURATION (TOP VIEW)

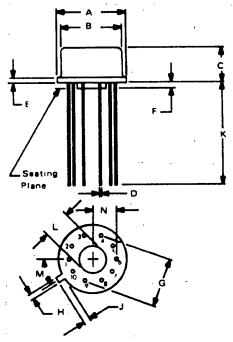


TO-100: MPY634AM, MPY634BM, MPY634SM

DIP: MPY634KP

MECHANICAL

METAL TO-100

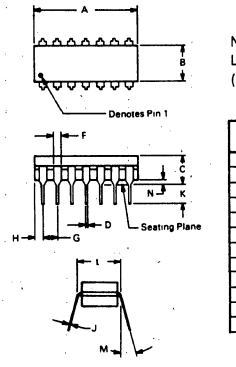


NOTE:
Leads in true position within .010" (.25mm) R at MMT at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	–	12.70	–
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

PLASTIC DUAL-IN-LINE



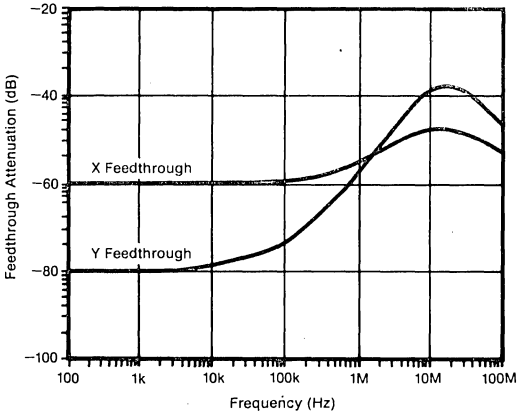
NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.660	.785	16.76	19.94
B	.220	.280	5.59	7.11
C	–	.200	–	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095		
J	.008	.015	0.20	0.38
K	.100	–	2.54	–
L	.300 BASIC		7.62 BASIC	
M	–	15°	–	15°
N	.020	.050	0.51	1.27

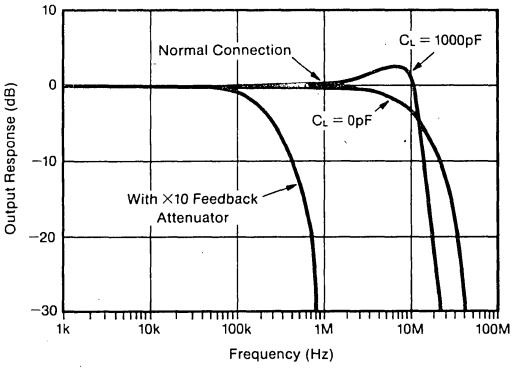
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

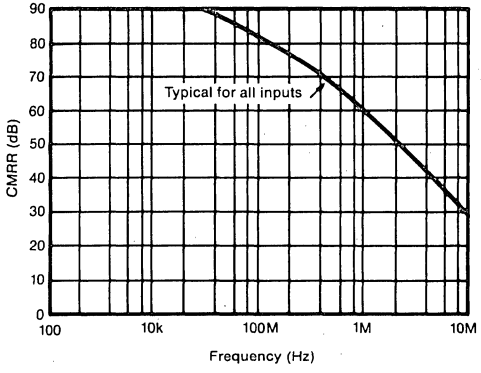
FEEDTHROUGH VS FREQUENCY



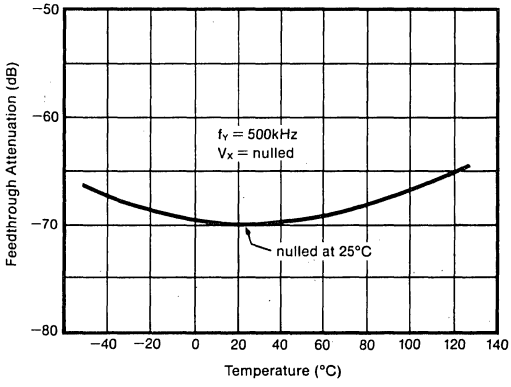
FREQUENCY RESPONSE AS A MULTIPLIER



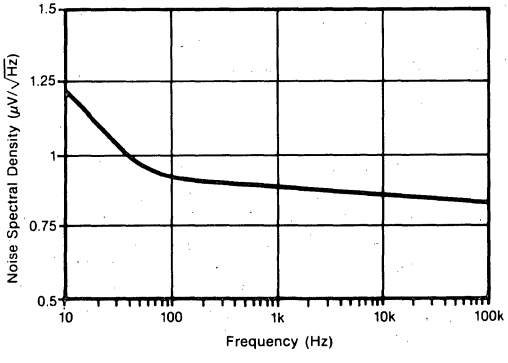
COMMON-MODE-REJECTION RATIO VS FREQUENCY



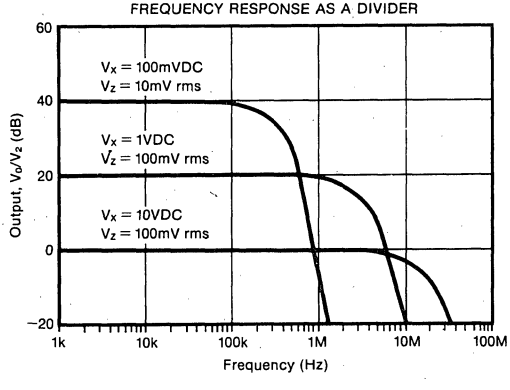
FEEDTHROUGH VS TEMPERATURE



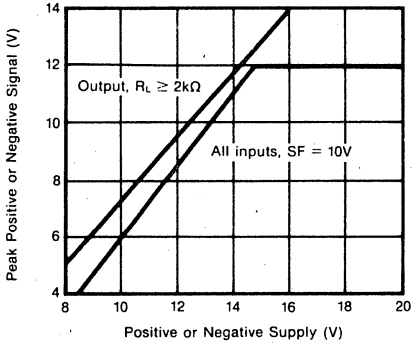
NOISE SPECTRAL DENSITY VS FREQUENCY



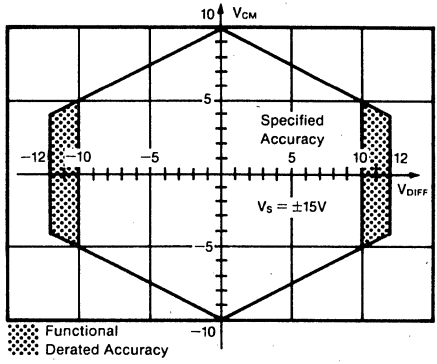
FREQUENCY RESPONSE AS A DIVIDER



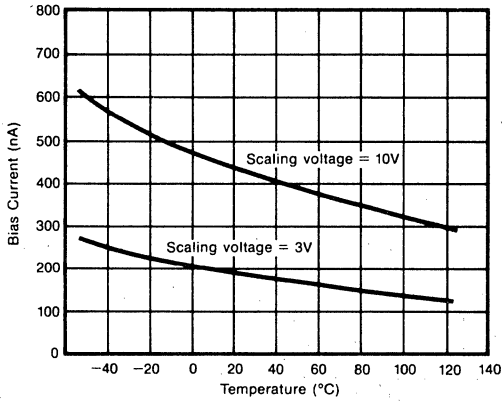
INPUT/OUTPUT SIGNAL RANGE
VS SUPPLY VOLTAGES



INPUT DIFFERENTIAL-MODE/
COMMON-MODE VOLTAGE



BIAS CURRENTS VS TEMPERATURE
(X, Y or Z inputs)



THEORY OF OPERATION

The transfer function for the MPY634 is:

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right]$$

where:

A = open-loop gain of the output amplifier (typically 85dB at DC).

SF = Scale Factor. Laser-trimmed to 10V but adjustable over a 3V to 10V range using external resistors.

X, Y, Z are input voltages. Full-scale input voltage is equal to the selected SF. (Max input voltage = ±1.25 SF.)

An intuitive understanding of transfer function can be gained by analogy to the op amp. By assuming that the open-loop gain, A, of the output operational amplifier is infinite, inspection of the transfer function reveals that any V_{OUT} can be created with an infinitesimally small quantity within the brackets. Then, an application circuit can be analyzed by assigning circuit voltages for all X, Y and Z inputs and setting the bracketed quantity equal to zero. For example, the basic multiplier connection in Figure 1, $Z_1 = V_{OUT}$ and $Z_2 = 0$. The quantity within the brackets then reduces to:

$$\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (V_{OUT} - 0) = 0$$

This approach leads to a simple relationship which can be solved for V_{OUT} to provide the closed-loop transfer function.

The scale factor is accurately factory-adjusted to 10V and is typically accurate to within 0.1% or less. The scale factor may be adjusted by connecting a resistor or potentiometer between pin SF and the $-V_S$ power supply. The value of the external resistor can be approximated by:

$$R_{SF} = 5.4k\Omega\left[\frac{SF}{10 - SF}\right]$$

Internal device tolerances make this relationship accurate to within approximately 25%. Some applications can benefit from reduction of the SF by this technique. The reduced input bias current, noise, and drift achieved by this technique can be likened to operating the input circuitry in a higher gain, thus reducing output contributions to these effects. Adjustment of the scale factor does not affect bandwidth.

The MPY634 is fully characterized at $V_S = \pm 15V$ but operation is possible down to $\pm 8V$ with an attendant reduction of input and output range capability. Operation at voltages greater than $\pm 15V$ allows greater output swing to be achieved by using an output feedback attenuator (Figure 1).

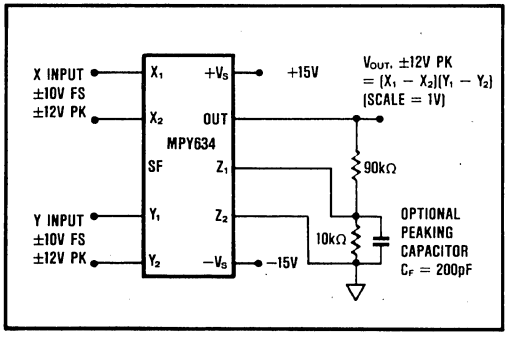


FIGURE 1. Connections for Scale-Factor of Unity.

As with any wide bandwidth circuit, the power supplies should be bypassed with high frequency ceramic capacitors. These capacitors should be located as near as practical to the power supply connections of the MPY634. Improper bypassing can lead to instability, overshoot, and ringing in the output.

BASIC MULTIPLIER CONNECTION

Figure 2 shows the basic connection as a multiplier. Accuracy is fully specified without any additional user-trimming circuitry. Some applications can benefit from trimming of one or more of the inputs. The fully differential inputs facilitate referencing the input quantities to the source voltage common terminal for maximum accuracy. They also allow use of simple offset voltage trimming circuitry as shown on the X input.

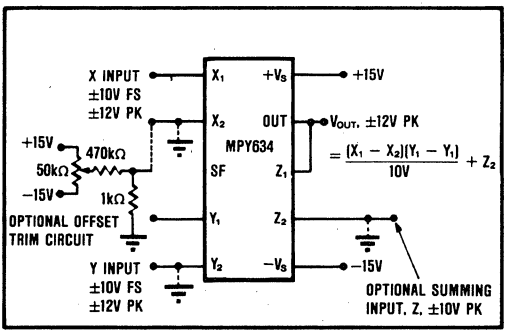


FIGURE 2. Basic Multiplier Connection.

The differential Z input allows an offset to be summed in V_{OUT}. In basic multiplier operation the Z_2 input serves as the output voltage ground reference and should be connected to the ground of the driven system for maximum accuracy.

A method of changing (lowering) SF by connecting to the SF pin was discussed previously. Figure 1 shows an alternative method of changing the effective SF of the overall circuit by using an attenuator in the feedback connection to Z_1. This method puts the output amplifier in a higher gain and is thus accompanied by a reduction in bandwidth and an increase in output offset voltage. The larger output offset may be reduced by applying a trimming voltage to the high impedance input, Z_2.

The flexibility of the differential Z inputs allows direct conversion of the output quantity to a current. Figure 3 shows the output voltage differentially-sensed across a series resistor forcing an output-controlled current. Addition of a capacitor load then creates a time integration function useful in a variety of applications such as power computation.

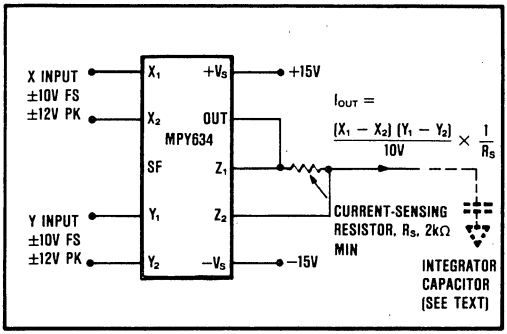


FIGURE 3. Conversion of Output to Current.

SQUARER CIRCUIT (FREQUENCY DOUBLER)

Squarer, or frequency doubler, operation is achieved by paralleling the X and Y inputs of the standard multiplier circuit. Inverted output can be achieved by reversing the differential input terminals of either the X or Y input. Accuracy in the squaring mode is typically a factor of two better than the specified multiplier mode with maximum error occurring with small (less than 1V) inputs. Better accuracy can be achieved for small input voltage levels by reducing the scale factor, SF.

DIVIDER OPERATION

The MPY634 can be configured as a divider as shown in Figure 4. High impedance differential inputs for the numerator and denominator are achieved at the Z and X inputs respectively. Feedback is applied to the Y_2 input, and Y_1 is normally referenced to output ground. Alternatively, as the transfer function implies, an input applied to Y_1 can be summed directly into V_{OUT}. Since the feedback connection is made to a multiplying input, the effective gain of the output op amp varies as a function of the denominator input voltage. Therefore, the bandwidth of the divider function is proportional to the denominator voltage (see Typical Performance Curves).

Accuracy of the divider mode typically ranges from 1.0% to 2.5% for a 10 to 1 denominator range depending on device grade. Accuracy is primarily limited by input offset voltages and can be significantly improved by trimming the offset of the X input. A trim voltage of

±3.5mV applied to the "low side" X input (X_2 for positive input voltages on X_1) can produce similar accuracies over a 100 to 1 deonominator range. To trim, apply a signal which varies from 100mV to 10V at a low frequency (less than 500Hz). An offset sine wave or ramp is suitable. Since the ratio of the quantities should be constant, the ideal output would be a constant 10V. Using AC coupling on an oscilloscope, adjust the offset control for minimum output voltage variation.

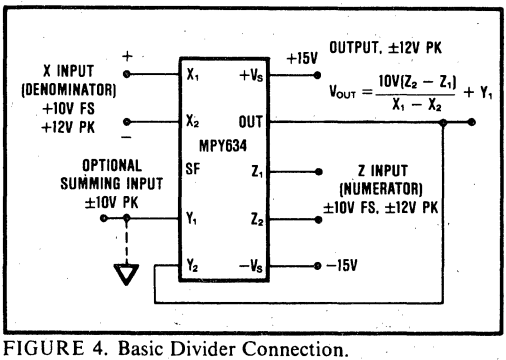


FIGURE 4. Basic Divider Connection.

SQUARE-ROOTER

A square-rooter connection is shown in Figure 5. Input voltage is limited to one polarity (positive for the connection shown). The diode prevents circuit latch-up should the input go negative. The circuit can be configured for negative input and positive output by reversing the polarity of both the X and Y inputs. The output polarity can be reversed by reversing the diode and X input polarity. A load resistance of approximately 10kΩ must be provided. Trimming for improved accuracy would be accomplished at the Z input.

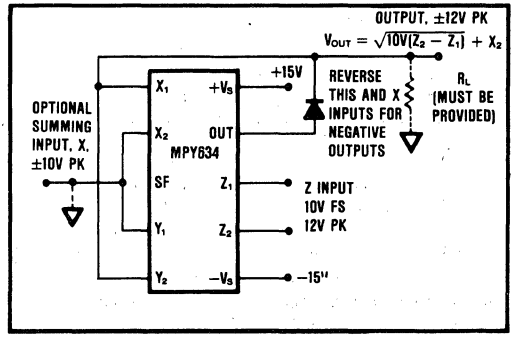


FIGURE 5. Square-Rooter Connection.

APPLICATIONS

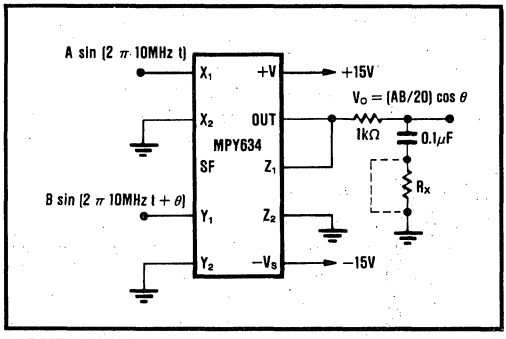


FIGURE 6. Phase Detector.

Multiplier connection followed by a low-pass filter forms phase detector useful in phase-locked-loop circuitry. R_X is often used in PLL circuitry to provide desired loop-damping characteristics.

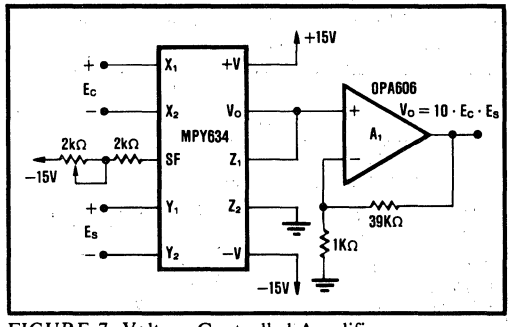


FIGURE 7. Voltage-Controlled Amplifier.

Minor gain adjustments are accomplished with the 1kΩ variable resistor connected to the scale factor adjustment pin, SF. Bandwidth of this circuit is limited by A_1, which is operated at relatively high gain.

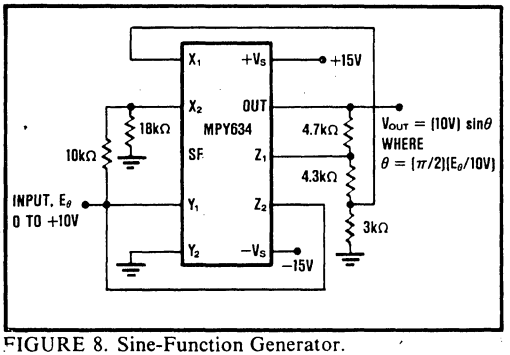


FIGURE 8. Sine-Function Generator.

With a linearly changing 0—10V input, this circuit's output follows 0° to 90° of a sine function with a 10V peak output amplitude.

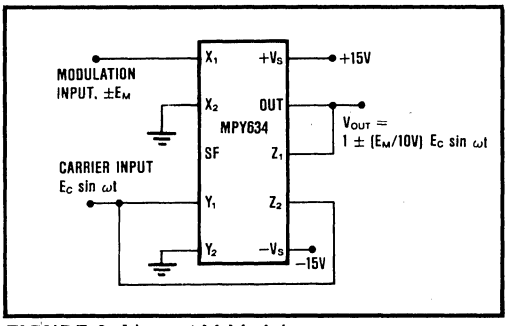
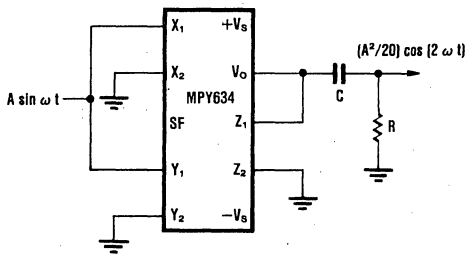
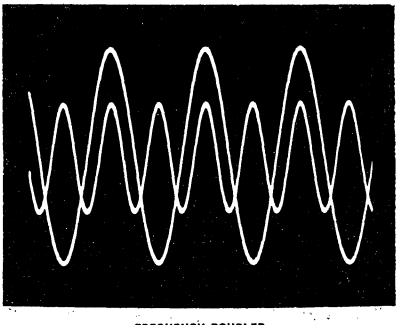


FIGURE 9. Linear AM Modulator.

By injecting the input carrier signal into the output through connection to the Z_2 input, conventional amplitude modulation is achieved. Amplification can be achieved by use of the SF pin, or Z attenuator (at the expense of bandwidth).

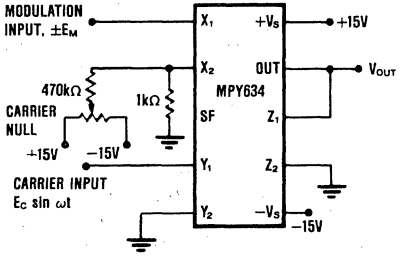


Squaring a sinusoidal input creates an output frequency of twice that of the input. The DC output component is removed by AC-coupling the output.

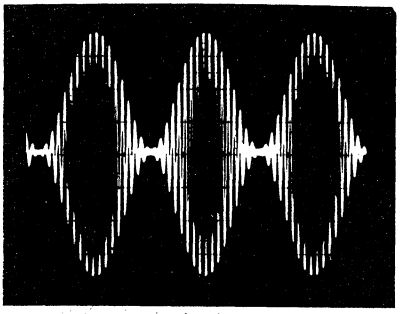


FREQUENCY DOUBLER
INPUT SIGNAL: 20V p-p, 200KHz
OUTPUT SIGNAL: 10V p-p, 400KHz

FIGURE 10. Frequency Doubler.



The basic multiplier connection performs balanced modulation. Carrier rejection can be improved by trimming the offset voltage of the modulation input. Better carrier rejection above 2MHz is typically achieved by interchanging the X and Y inputs (carrier applied to the X input).



CARRIER: $f_C = 2MHz$, AMPLITUDE = 1V rms
SIGNAL: $f_S = 120kHz$, AMPLITUDE = 10V peak

FIGURE 11. Balanced Modulator.

BURR-BROWN®

REF10

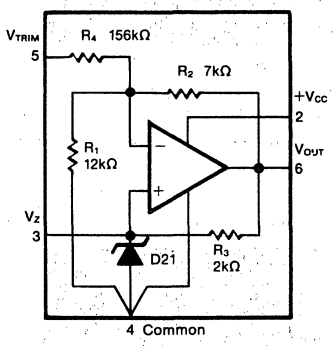
Precision VOLTAGE REFERENCE

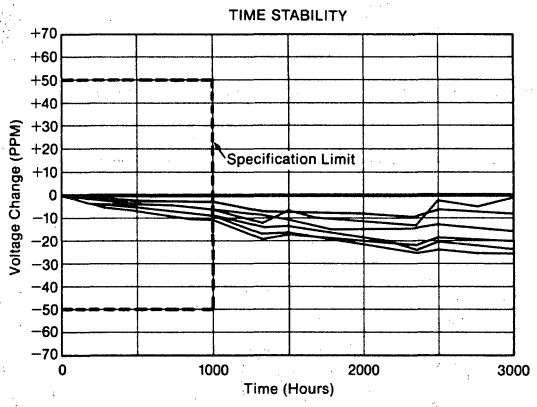
FEATURES

- +10.00V OUTPUT
- HIGH ACCURACY, ±0.005V untrimmed
- VERY-LOW DRIFT, 1ppm/°C max
- EXCELLENT STABILITY, 10ppm/1000hrs typ
- LOW NOISE, 6μV, p-p typ. 0.1Hz to 10Hz
- WIDE SUPPLY RANGE, up to 35V

APPLICATIONS

- PRECISION CALIBRATED VOLTAGE STANDARD
- TRANSDUCER EXCITATION
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT





DESCRIPTION

The REF10 is a precision voltage reference which provides a +10.00V output. The drift is laser-trimmed to 1ppm/°C max (KM grade) over the full specification range. This is in contrast to some references which guarantee drift over a limited portion of their specification temperature range. The REF10 achieves its precision without a heater. This results in low quiescent current, fast warm-up, excellent stability, and low noise.

The output can be adjusted with minimal effect on drift or stability. Single supply operation over 13.5V to 35V supply range and excellent overall specifications make the REF10 an ideal choice for the most demanding applications such as precision system standards, D/A and A/D references, transducer excitation etc.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

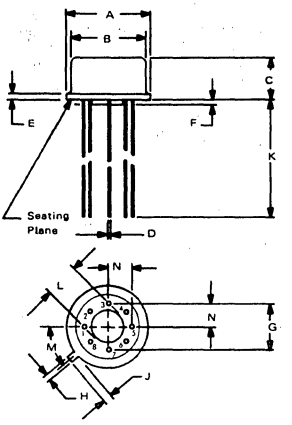
At T_A = +25°C and +15VDC power supply unless otherwise noted.

PARAMETER	CONDITION	REF10JM/KM/RM/SM MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE					
Initial	T_A = +25°C	9.995	10.000	10.005	V
Trim Range[1]		−0.100		+0.250	V
vs Temperature[2]: KM	0°C to +70°C			1	ppm/°C
JM	0°C to +70°C			3	ppm/°C
SM	−55°C to +125°C			3	ppm/°C
RM	−55°C to +125°C			6	ppm/°C
vs Supply (line regulation)	V_{CC} = 13.5 to 35V		0.001	0.002	%/V
vs Output Current (load regulation)	I_L = 0 to ±10mA		0.001	0.002	%/mA
vs Time[3]	T_A= +25°C		10	±50	ppm/1000 hrs
NOISE	0.1Hz to 10Hz		6	25	µV p-p
OUTPUT CURRENT	Source or Sink	±10			mA
INPUT VOLTAGE RANGE		13.5		35	V
QUIESCENT CURRENT	I_{OUT} = 0		4.5	6	mA
WARM-UP TIME	To 0.1%		10		µs
TEMPERATURE RANGE					
Specification: JM, KM		0		+70	°C
RM, SM		−55		+125	°C
Operating: JM, KM		−25		+85	°C
RM, SM		−55		+125	°C
Storage		−65		+125	°C

NOTES: (1) Trimming the offset voltage will affect the drift slightly. See Installation and Operating Instructions for details. (2) The "box method" is used to specify output voltage drift vs temperature. See the Discussion of Performance section. (3) Sample tested with power applied continuously.

MECHANICAL

TO-99 PACKAGE



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers not marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

WEIGHT: 1 gram

ORDERING INFORMATION

REF10 X M

Basic Model Number

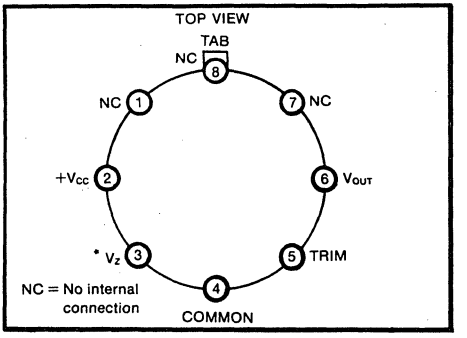
Performance Grade Code
- J, K: −0°C to +70°C
- R, S: −55°C to +125°C

Package Code
- TO-99

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Power Dissipation at +25°C	200mW
Operating Temperature Range	
REF10JM/KM	−25°C to +85°C
REF10RM/SM	−55°C to +125°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Short-Circuit Protection at +25°C to Common or +15VDC	Continuous

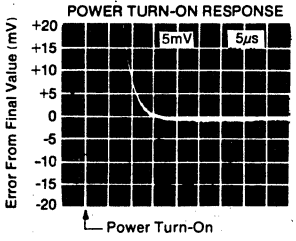
PIN CONFIGURATION



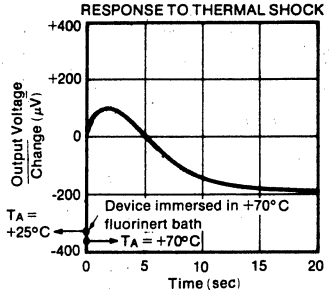
*Pin 3 is an unbuffered 6.3V output. Any load will affect the output voltage and drift. A load of 1µA on pin 3 will typically change the output voltage by 50µV and the drift by 0.1ppm/°C.

TYPICAL PERFORMANCE CURVES

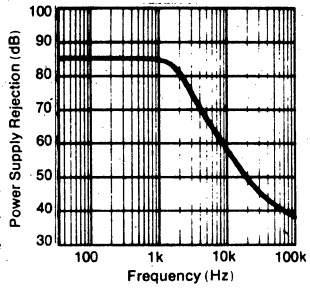
POWER TURN-ON RESPONSE



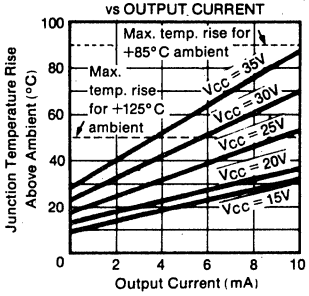
RESPONSE TO THERMAL SHOCK



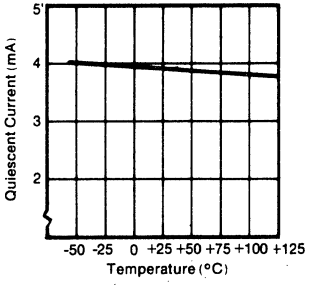
POWER SUPPLY REJECTION VS FREQUENCY



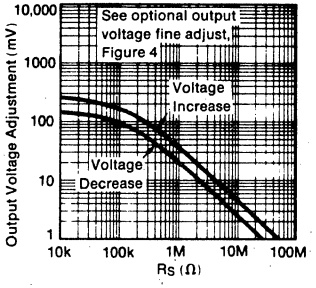
JUNCTION TEMPERATURE RISE vs OUTPUT CURRENT



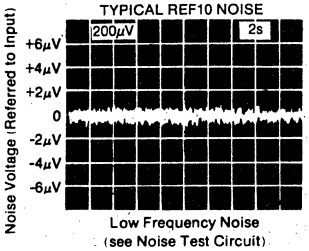
QUIESCENT CURRENT VS TEMPERATURE



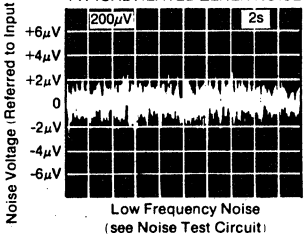
OUTPUT VOLTAGE ADJUSTMENT vs RS



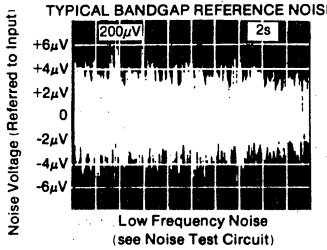
TYPICAL REF10 NOISE

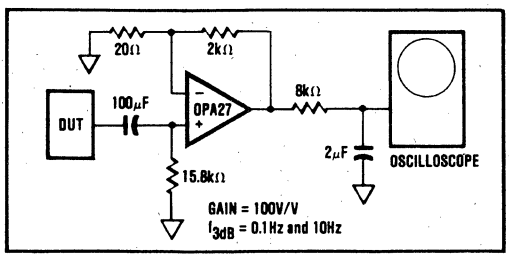


TYPICAL HEATED ZENER NOISE



TYPICAL BANDGAP REFERENCE NOISE





NOISE TEST CIRCUIT

THEORY OF OPERATION

The following discussion refers to the diagram on the first page.

In operation, approximately 6.3V is applied to the noninverting input of op amp A_1 by zener diode DZ_1. This voltage is amplified by A_1 to produce the 10.00V output. The gain is determined by R_1 and R_2: $G = (R_1 + R_2)/R_1$. R_1 and R_2 are actively laser-trimmed to produce an exact 10.00V output. The zener operating current is derived from the regulated output voltage through R_3. This feedback arrangement provides closely regulated zener current. R_3 is actively laser-trimmed to set the zener current to a level which results in low drift at the output of A_1. R_4 allows user-trimming of the output voltage by providing for a small external adjustment of amplifier gain. Since the TCR of R_4 closely matches the TCR of the gain setting resistors, the voltage trim has minimal effect on the drift of the reference.

DISCUSSION OF PERFORMANCE

The REF10 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the "butterfly method" and the "box method." The REF10 is specified with the more commonly used box method. The "box" is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

For the REF10 each J and K unit is tested at temperatures of 0°C, +25°C, +50°C, and +70°C and each R and S unit is tested at −55°C, −25°C, 0°C, +25°C, +50°C, +75°C, +100°C and +125°C. The minimum and maximum test voltages must meet this condition:

$$\left[\frac{(V_{OUT\ max} - V_{OUT\ min})/10V}{T_{high} - T_{low}}\right] \times 10^6 \leq \text{drift specification}$$

This assures the user that the variations of output voltage that occur as the temperature changes within the specification range T_{low} to T_{high} will be contained within a box whose diagonal has a slope equal to the maximum specified drift. Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{Upper\ Bound}$ and $V_{Lower\ Bound}$ (see Figure 1).

Figure 1 uses the REF10KM as an example. It has a drift specification of 1ppm/°C maximum and a specification temperature range of 0°C to +70°C. The "box" height (V_1 to V_2) is 700μV and upper bound and lower bound voltages are a maximum of 700μV away from the voltage at +25°C.

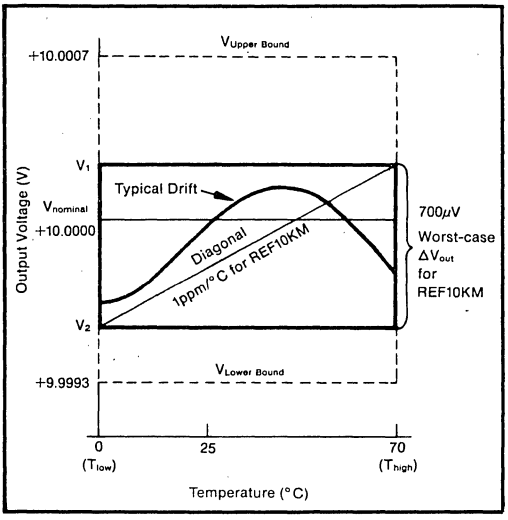


FIGURE 1. REF10KM Output Voltage Drift.

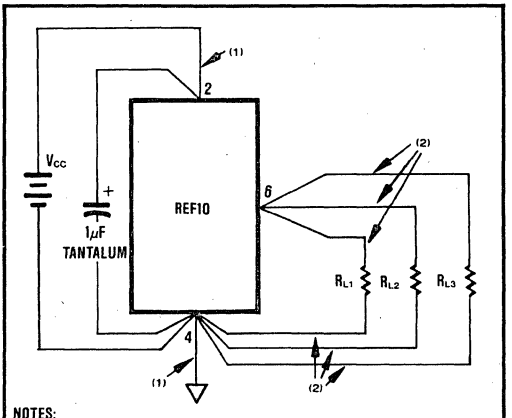
INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF10. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated being sure to minimize interconnection resistances.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figure 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.01ppm/°C



NOTES:
1. Lead resistances here of up to a few ohms have negligible effect on performance.
2. A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF10 Installation.

per mV of trimmed voltage. In the circuit in Figure 3 any mismatch in TCR between the two sections of the potentiometer will also affect drift but the effect of the ΔTCR is reduced by a factor of 40 by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a range of approximately +250mV to −100mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 156kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

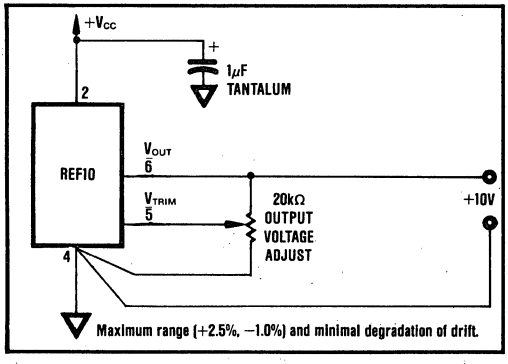


FIGURE 3. REF10 Optional Output Voltage Adjust.

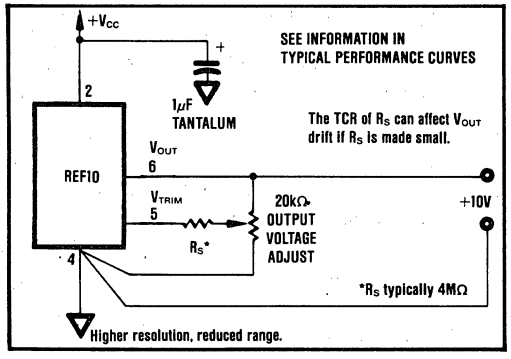


FIGURE 4. REF10 Optional Output Voltage Fine Adjust.

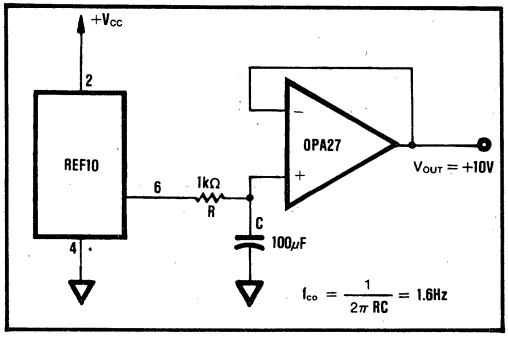


FIGURE 5. Precision Reference with Filtering.

APPLICATION INFORMATION

High accuracy, extremely-low drift, and small size make the REF10 ideal for demanding instrumentation and system voltage reference applications. Since no heater is required, low power supply current designs are readily achievable. Also the REF10 has lower output noise and much faster warm-up times than heated references, permitting high precision without extra power or additional supplies. It should be considered that operating any integrated circuit at an elevated temperature will reduce its MTTF.

A variety of application circuits are shown in Figures 5 through 11.

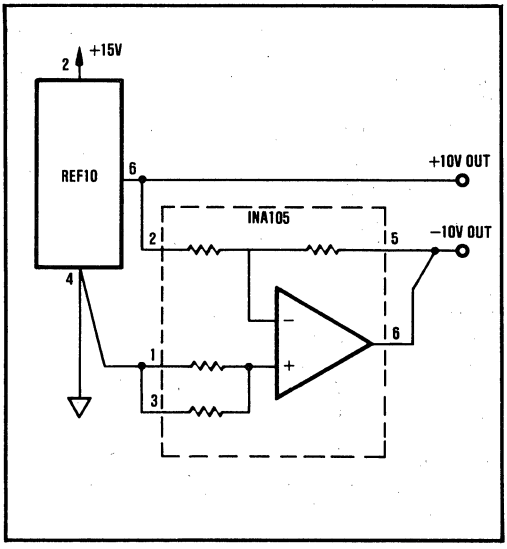


FIGURE 6. ±10V Reference.

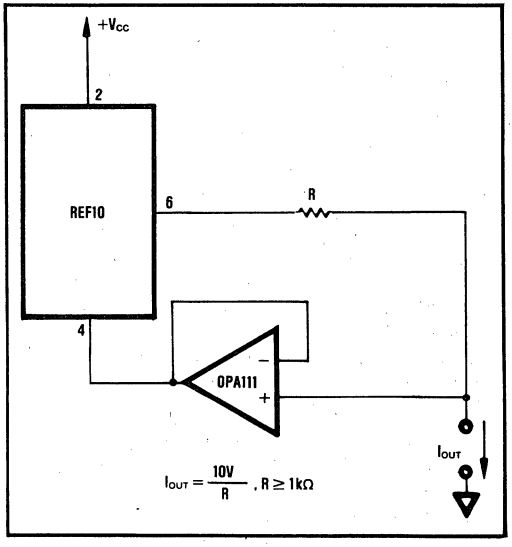


FIGURE 7. Positive Precision Current Source.

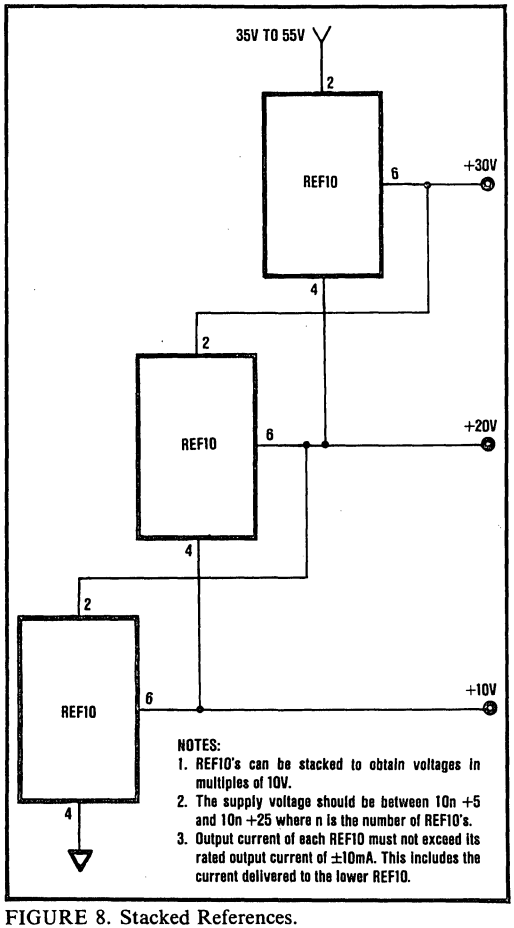


FIGURE 8. Stacked References.

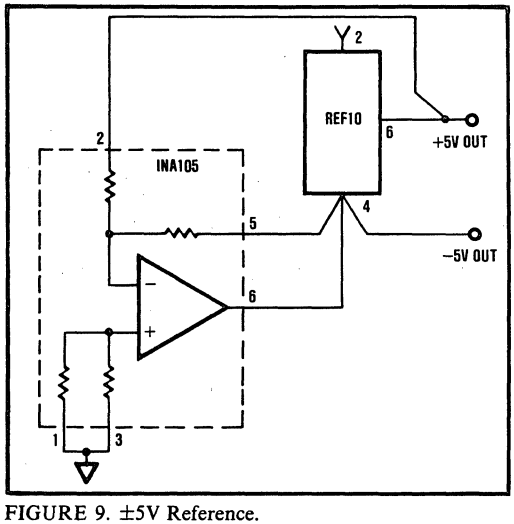


FIGURE 9. ±5V Reference.

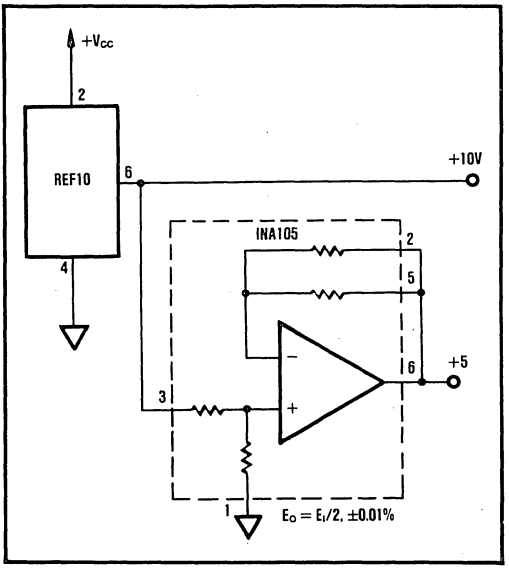


FIGURE 10. +5V and +10V Reference.

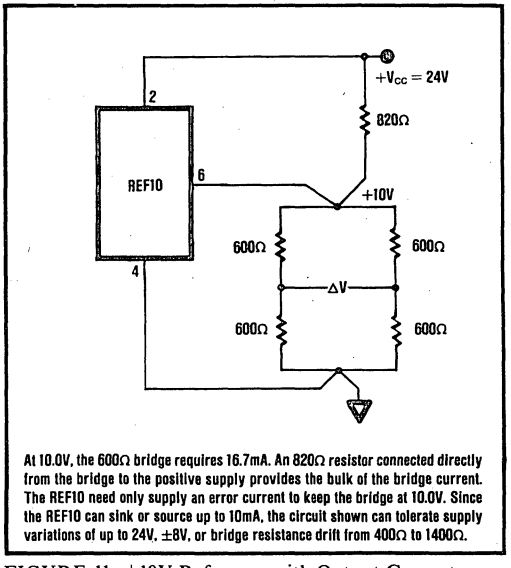


FIGURE 11. +10V Reference with Output Current Boost Using a Resistor to Drive a 600Ω Bridge.

BURR-BROWN®

REF101

Precision VOLTAGE REFERENCE

FEATURES

- +10.00V OUTPUT
- HIGH ACCURACY, ±0.005V
- VERY LOW DRIFT, 1ppm/°C max
- EXCELLENT STABILITY, 25ppm/1000hrs.
- LOW NOISE, 6μV, p-p typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE, up to 35V
- LOW QUIESCENT CURRENT, 6mA max
- USEFUL MATCHED RESISTOR PAIR INCLUDED

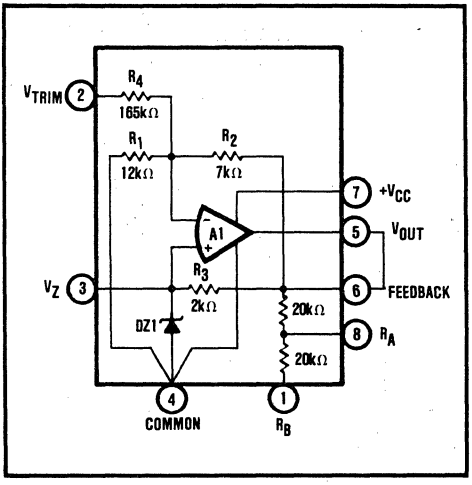
APPLICATIONS

- PRECISION CALIBRATED VOLTAGE STANDARD
- TRANSDUCER EXCITATION
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT

DESCRIPTION

The REF101 is a precision voltage reference which provides a +10.00V output. The drift is laser-trimmed to 1ppm/°C max (KM grade) over the full specification range. This is in contrast to some references which guarantee drift over a limited portion of their specification temperature range. The REF101 achieves its precision without a heater. This results in low quiescent current (4.5mA typ), fast warm-up (1msec to 0.1%), excellent stability (25ppm/1000hrs typ), and low noise (25μV, p-p max, 0.1Hz to 10Hz).

The output can be adjusted with minimal effect on drift or stability. Additionally, the REF101 contains a matched pair of user-accessible precision 20kΩ resistors which are useful in a variety of applications. Single supply operation over 13.5V to 35V supply range and excellent overall specifications make the REF101 an ideal choice for the most demanding applications such as precision system standards, D/A and A/D references, transducer excitation etc.



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PDS-485A

SPECIFICATIONS

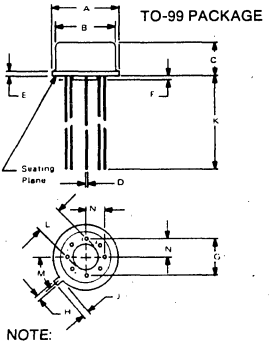
ELECTRICAL

At T_A = +25°C and +15VDC power supply unless otherwise noted.

PARAMETER	CONDITION	REF101JM/KM/RM/SM MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE					
Initial	T_A = +25°C	9.995	10.000	10.005	V
Trim Range[1]		-0.100		+0.250	V
vs Temperature[2]					
KM	0°C to +70°C			1	ppm/°C
JM	0°C to +70°C			2	ppm/°C
SM	-55°C to +125°C			3	ppm/°C
RM	-55°C to +125°C			6	ppm/°C
vs Supply (line regulation)	V_{CC} = 13.5 to 35V		0.00025	0.002	%/V
vs Output Current					
(load regulation)	I_L = 0 to ±10mA		0.00025[3]		%/mA
			0.001[4]	0.002[4]	%/mA
vs Time	T_A = +25°C		25		ppm/1000 hrs
NOISE	0.1Hz to 10Hz		6	25	µV p-p
OUTPUT CURRENT	Source or Sink	±10			mA
INPUT VOLTAGE RANGE		13.5		35	V
QUIESCENT CURRENT	I_{OUT} = 0		4.5	6	mA
WARM-UP TIME	To 0.1%		10		µsec
UNCOMMITTED RESISTORS					
Resistance			20		kΩ
Match			±0.01	±0.05	%
TCR			50		ppm/°C
TCR Tracking			2		ppm/°C
TEMPERATURE RANGE					
Specification					
JM, KM		0		+70	°C
RM, SM		-55		+125	°C
Operating					
JM, KM		-25		+85	°C
RM, SM		-55		+125	°C
Storage		-65		+125	°C

NOTES: (1) Trimming the offset voltage will affect the drift slightly. See Installation and Operating Instructions for details. (2) The "box method" is used to specify output voltage drift vs temperature. See the Discussion of Performance section. (3) Sourcing current. (4) Sinking current.

MECHANICAL



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers not marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	-	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

WEIGHT: 1 gram

ORDER: REF101JM, REF101KM
REF101RM, REF101SM

ORDERING INFORMATION

REF101 X M

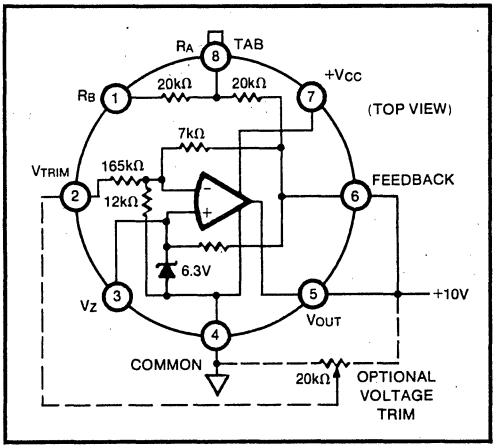
Basic Model Number
Performance Grade Code
- J, K -25°C to +85°C
- R, S -55°C to +125°C

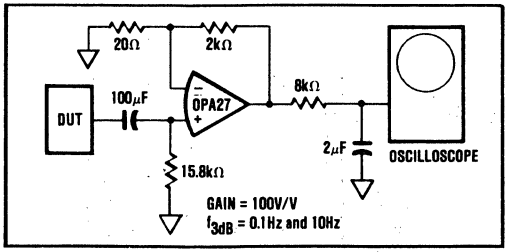
Package Code
- TO-99

ABSOLUTE MAXIMUM RATINGS

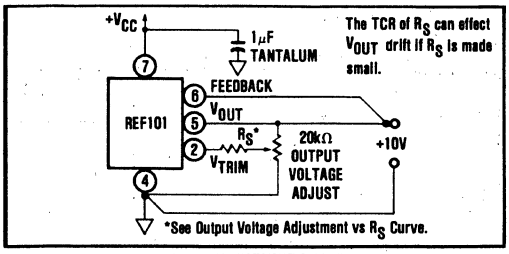
- Input Voltage 40V
- Power Dissipation at +25°C 200mW
- Operating Temperature Range
  - REF101JM/KM ..... -25°C to +85°C
  - REF101RM/SM ..... -55°C to +125°C
- Storage Temperature Range ..... -65°C to +125°C
- Lead Temperature (soldering, 10sec) ..... +300°C
- Short-Circuit Protection at +25°C
  - To Common or +15VDC ..... Continuous

PIN CONFIGURATION



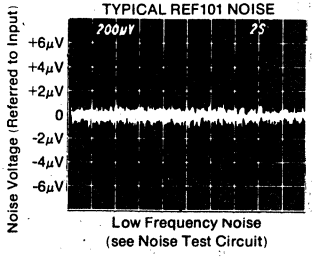


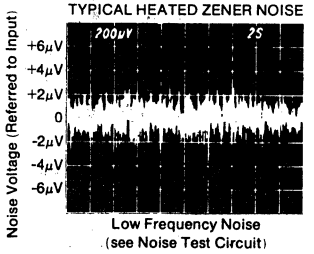
NOISE TEST CIRCUIT

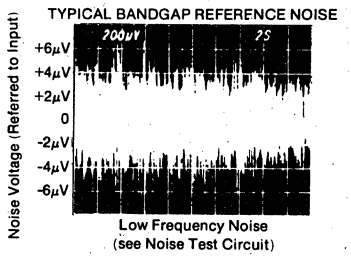


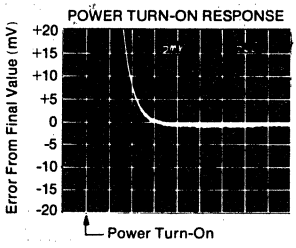
OPTIONAL OUTPUT VOLTAGE FINE ADJUSTMENT CIRCUIT.

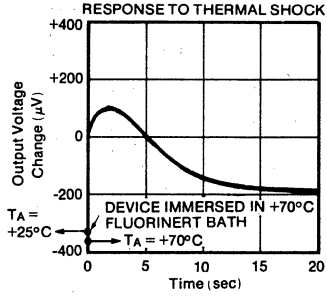
TYPICAL PERFORMANCE CURVES

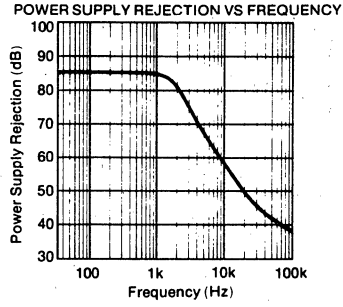


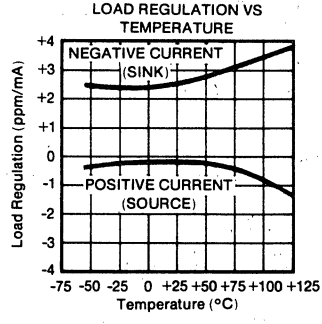


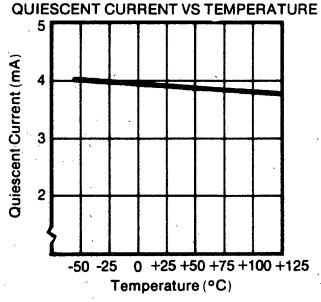


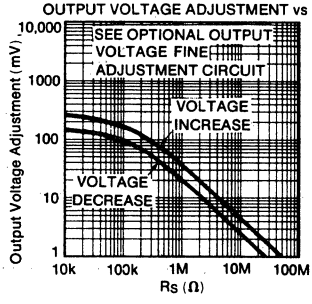


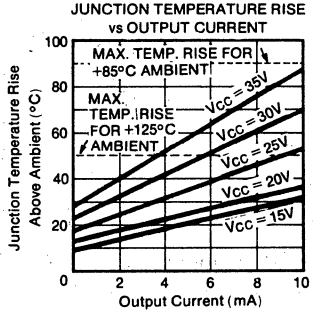












THEORY OF OPERATION

The following discussion refers to the diagram on the first page.

In operation, approximately 6.3V is applied to the noninverting input of op amp A_1 by zener diode DZ_1. This voltage is amplified by A_1 to produce the 10.00V output. The gain is determined by R_1 and R_2: $G = (R_1 + R_2)/R_1$. R_1 and R_2 are actively laser-trimmed to produce an exact 10.00V output. The zener operating current is derived from the regulated output voltage through R_3. This feedback arrangement provides closely regulated zener current. R_3 is actively laser-trimmed to set the zener current to a level which results in low drift at the output of A_1. The adjustment of output voltage and zener current is interactive and several iterations may be used to achieve the desired results. R_4 allows user-trimming of the output voltage by providing for a small external adjustment of amplifier gain. Since the TCR of R_4 closely matches the TCR of the gain setting resistors, the voltage trim has minimal effect on the drift of the reference.

DISCUSSION OF PERFORMANCE

The REF101 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry — the "butterfly method" and the "box method". Neither of these methods is entirely satisfactory in cases where the drift versus temperature is relatively nonlinear as is the case with most voltage references. The REF101 is specified with the more commonly used box method. The "box" is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

For the REF101 each J and K unit is tested at temperatures of 0°C, +25°C, +50°C, and +70°C and each R and S unit is tested at -55°C, -25°C, 0°C, +25°C, +50°C, +75°C, +100°C and +125°C. The minimum and maximum test voltages must meet this condition.

$$\left[\frac{(V_{OUT\ max} - V_{OUT\ min})/10V}{T_{high} - T_{low}}\right] \times 10^6 \leq \text{drift specification}$$

This assures the user that the variations of output voltage that occur as the temperature changes within the specification range T_{low} to T_{high} will be contained within a box whose diagonal has a slope equal to the maximum specified drift. Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{Upper\ Bound}$ and $V_{Lower\ Bound}$ (see Figure 1).

Figure 1 uses the REF101KM as an example. It has a drift specification of 1ppm/°C maximum and a specification temperature range of 0°C to +70°C. The "box" height (V_1 to V_2) is 700μV and upper bound and lower bound voltages are a maximum of 700μV away from the voltage at +25°C.

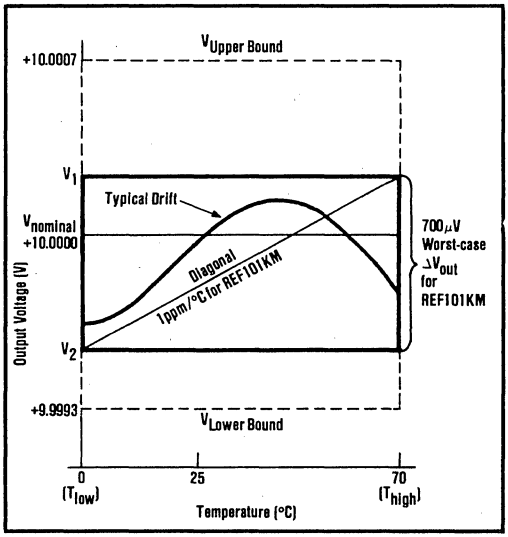
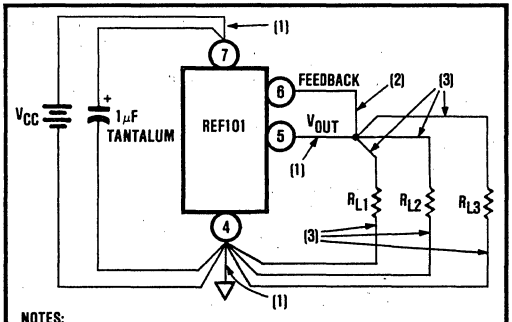


FIGURE 1. REF101KM Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF101. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated being sure to minimize interconnection resistances.



NOTES:
1. Lead resistances here of up to a few ohms have negligible effect on performance.
2. A relatively constant current of approx. 2mA at 50ppm/°C flows in this lead. 1Ω in this lead would introduce about 2mV error (adjustable to zero) with about 0.1ppm/°C drift at the output.
3. A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF101 Basic Circuit Connection.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.01ppm/°C per mV of trimmed voltage. In the circuit in Figure 3 any mismatch in TCR between the two sections of the potentiometer will also affect drift but the effect of the ΔTCR is reduced by a factor of 40 by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a range of approximately +250mV to -100mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 165kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

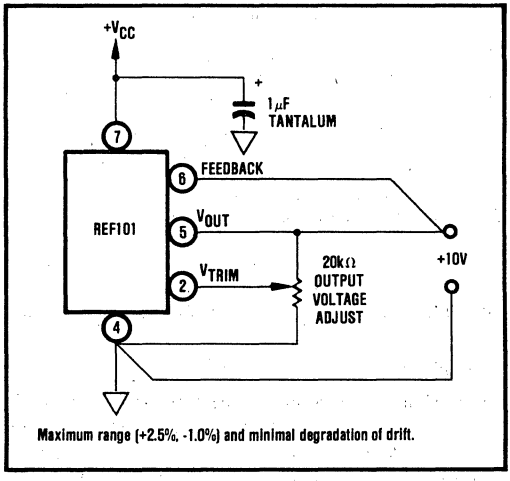


FIGURE 3. REF101 Optional Output Voltage Adjust.

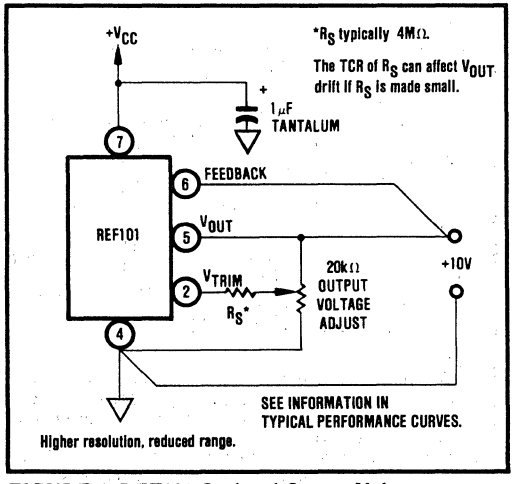


FIGURE 4. REF101 Optional Output Voltage Fine Adjust.

APPLICATION INFORMATION

High accuracy, extremely-low drift, and small size make the REF101 ideal for demanding instrumentation and system voltage reference applications. Since no heater is required, low power supply current designs are readily achievable. Also the REF101 has lower output noise and much faster warm-up times (1msec to 0.1%) than heated references, permitting high precision without extra power from additional supplies. It should be considered that operating any integrated circuit at an elevated temperature will reduce its MTTF.

A variety of application circuits are shown in Figures 5 through 19.

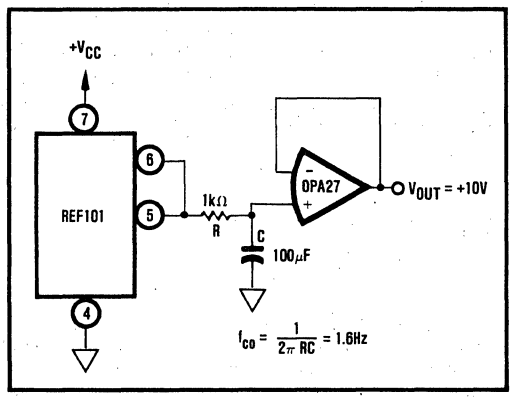


FIGURE 5. Precision Reference with Filtering.

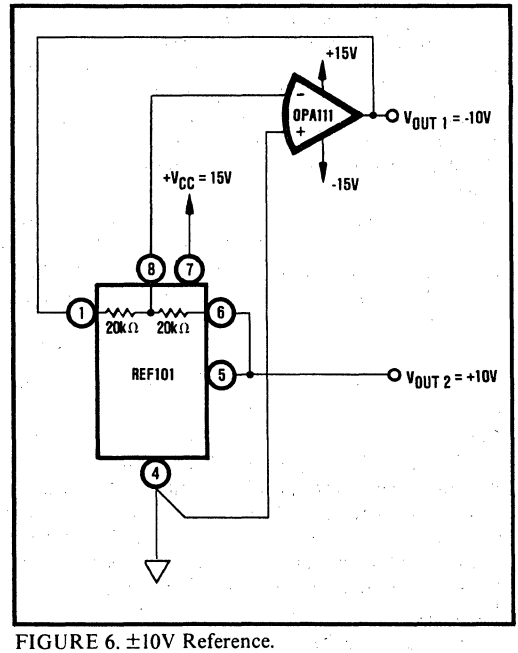


FIGURE 6. ±10V Reference.

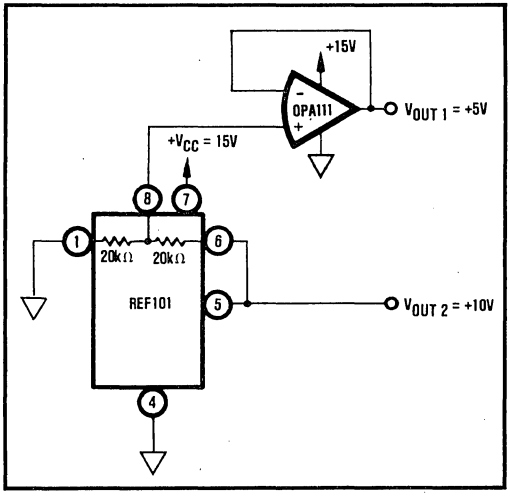


FIGURE 7. +10V and +5V Reference.

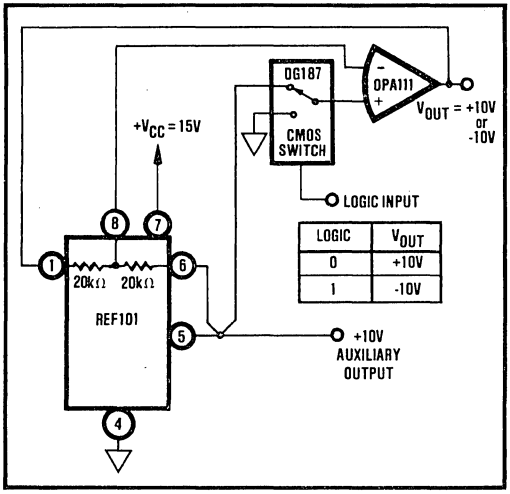


FIGURE 9. Digitally-Controlled Bipolar Precision Reference.

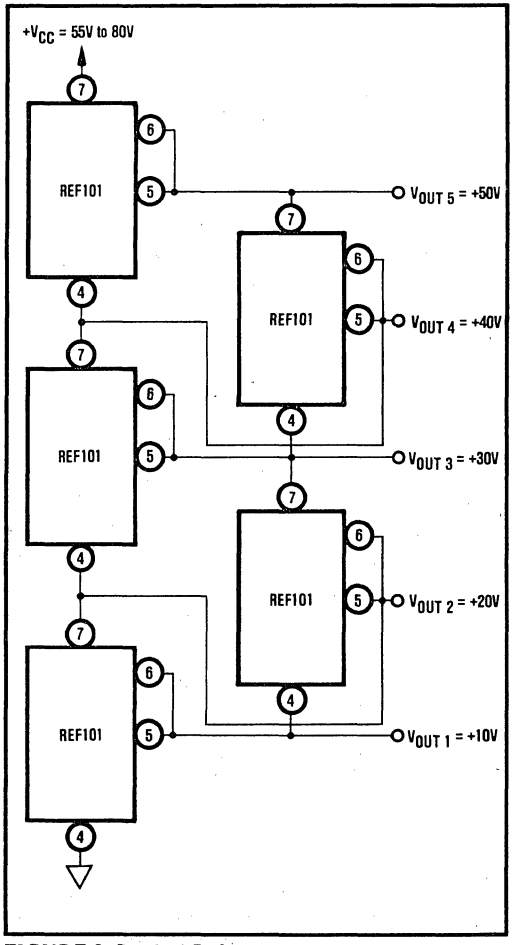


FIGURE 8. Stacked References.

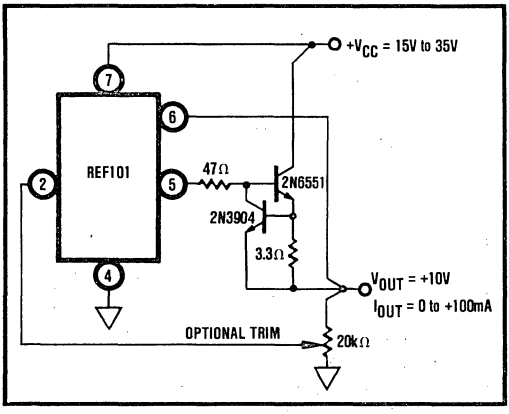


FIGURE 10. +10V Reference with Boosted Output Current to 100mA.

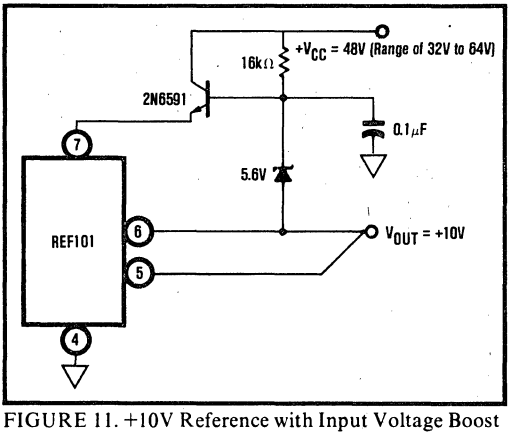


FIGURE 11. +10V Reference with Input Voltage Boost for 48V Operation.

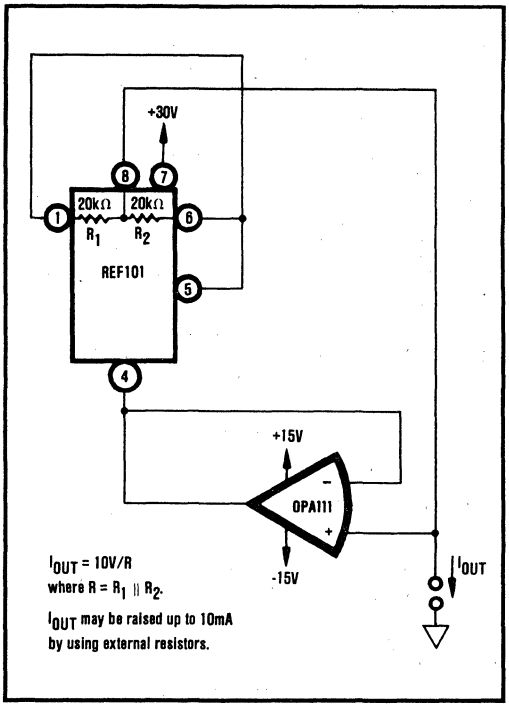


FIGURE 12. Positive Precision 1mA Current Source.

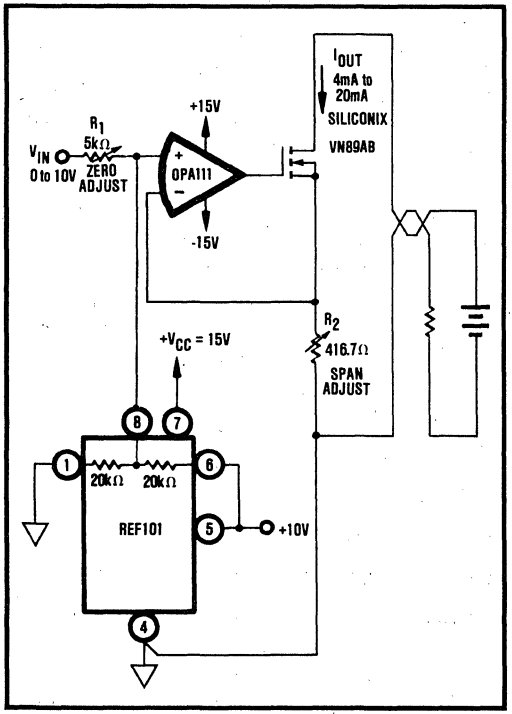


FIGURE 13. 4mA to 20mA Precision Current Transmitter.

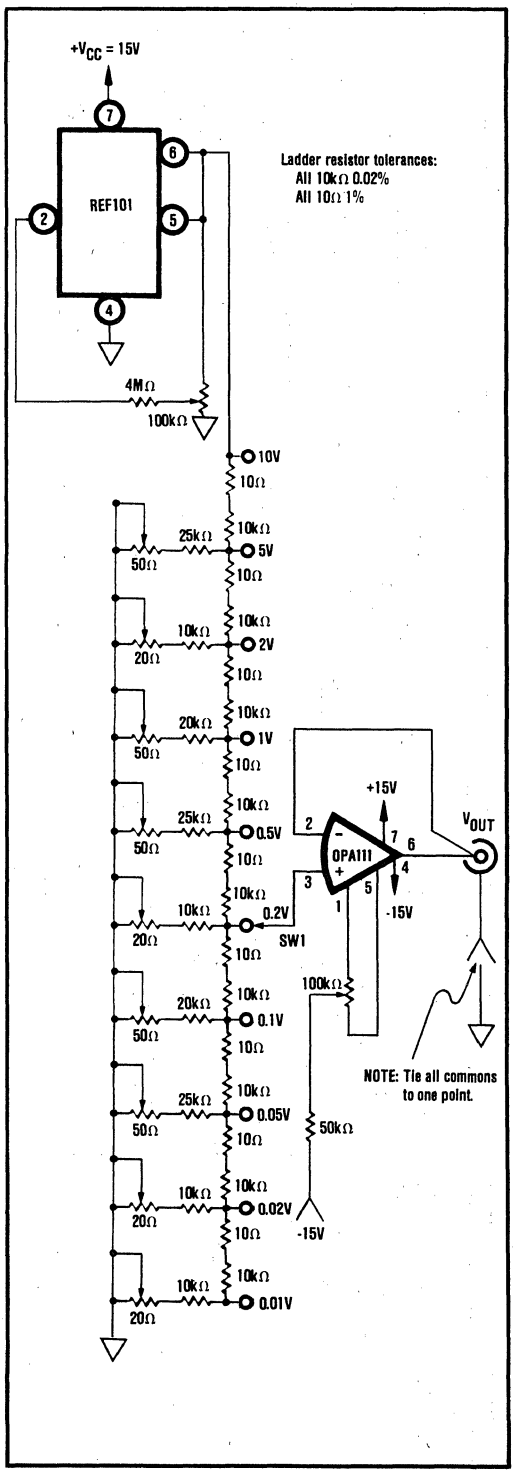


FIGURE 14. Precision Voltage Calibrator.

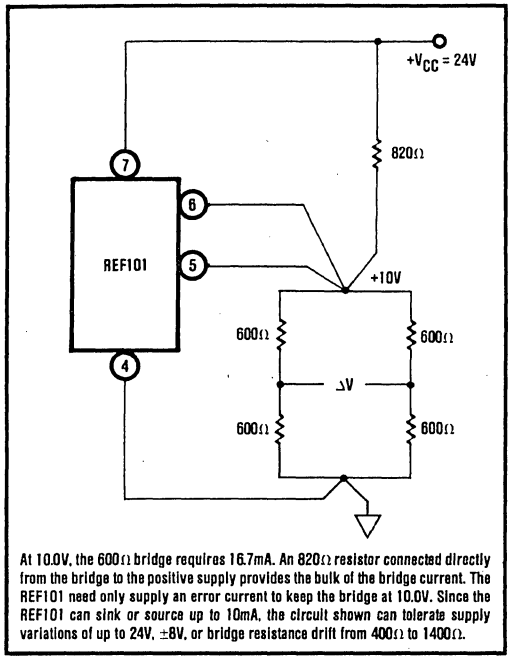


FIGURE 15. +10V Reference with Output Current Boost Using a Resistor to Drive a 600Ω Bridge.

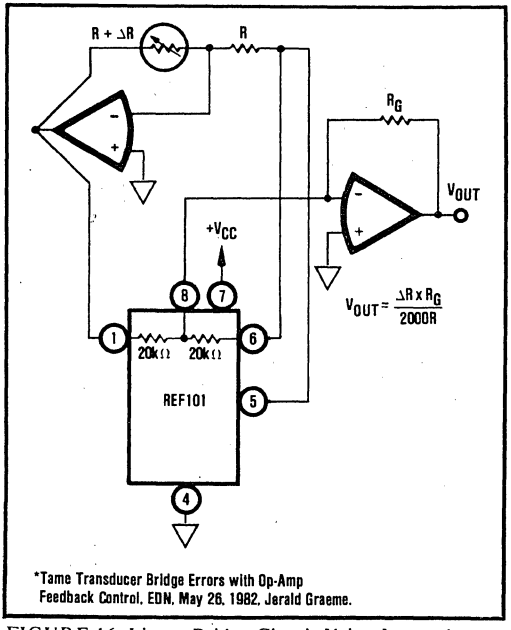


FIGURE 16. Linear Bridge Circuit Using Internal Precision Resistors of the REF101 as the Bridge Completion Network.

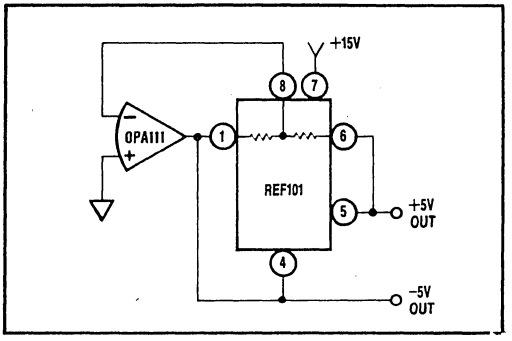


FIGURE 17. ±5V Reference.

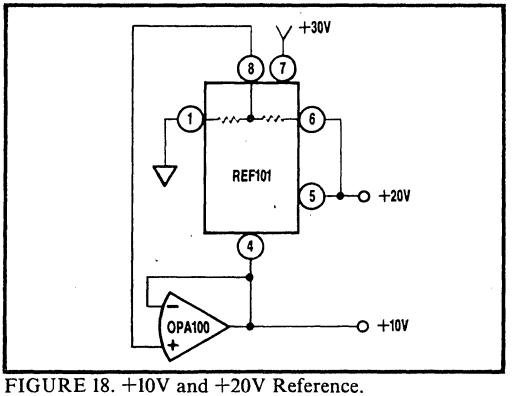


FIGURE 18. +10V and +20V Reference.

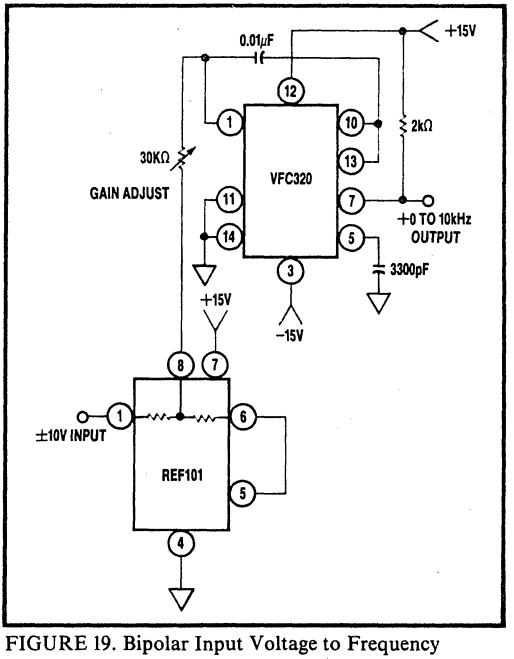


FIGURE 19. Bipolar Input Voltage to Frequency Converter.

BURR-BROWN®

UAF11
UAF21

UNIVERSAL ACTIVE FILTERS

FEATURES

- SAVES DESIGN TIME
  - User-tuneable frequency, Q-factor, gain
  - Calculate only three resistance values
  - Design directly from this data sheet
  - Completely characterized parameters
- IMPROVED PERFORMANCE
  - Wide frequency ranges
  - UAF11 - 0.001Hz to 20kHz
  - UAF21 - 0.001Hz to 200kHz
  - 1% frequency accuracy
  - Q range of 0.5 to 500
  - Reliable hybrid construction
  - NPO capacitors and thin-film resistors

APPLICATIONS

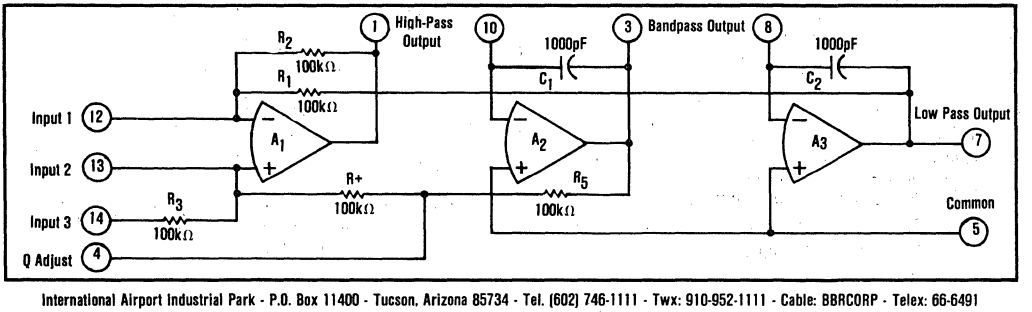
- FILTER CONFIGURATIONS
  - Butterworth
  - Bessel
  - Chebyschev
- FILTER FUNCTIONS
  - Low pass
  - High pass
  - Bandpass
  - Band reject

DESCRIPTION

The UAF11's and UAF21's are low cost universal active filters. These versatile units can easily be tailored to any active filter application using the extensive information provided in this data sheet. UAF's are excellent choices for use in communications equipment, test equipment (engine analyzers, aircraft and automotive test, medical test, etc.), servo systems, process control equipment, sonar and many others.

The UAF11's and UAF21's are complete two-pole active filters with the addition of four external resistors that provide the user easy control of the Q-factor, resonant frequency and gain. Any complex filter response can be obtained by cascading these units. Three separate outputs provide low-pass, high-pass, and bandpass transfer functions. A band-reject (notch) transfer function may be realized simply by summing the high-pass and low-pass outputs.

Since these UAF's are so versatile and flexible, they can be stocked by the user in quantity for use as building blocks whenever the requirement arises. This means instant availability and the UAF purchases may be made in volume to take advantage of quantity price discounts.



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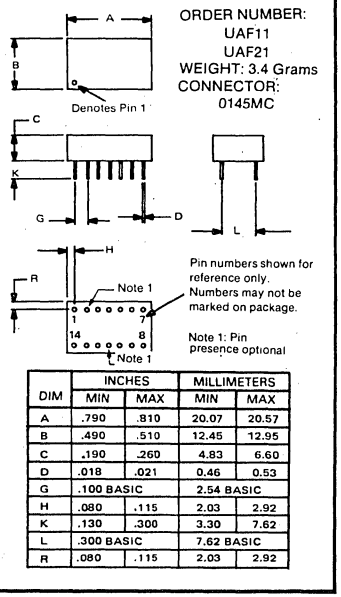
SPECIFICATIONS

ELECTRICAL

Typical at +25°C and with rated supply unless otherwise noted.

MODEL	UAF11	UAF21[1]	UNITS
INPUT			
Input Bias Current	±100	±15	nA
Input Voltage Range	±10	±10	V
Input Resistance	100k	100k	Ω
TRANSFER CHARACTERISTICS			
Frequency Range (f_o)	0.001 to 20k	0.001 to 200k	Hz
f_o Accuracy[2]	±1	±1	%
f_o Stability[3] (over temp. range)	±0.005	±0.005	%/°C
Q Range[4]	0.5 to 500	0.5 to 500	--
Q Stability[5]			
at f_o Q ≤ 10^4	±0.025	±0.01	%/°C
at f_o Q ≤ 10^5	±0.1	±0.025	%/°C
Gain Range	0.1 to 50	0.1 to 50	--
OUTPUT			
Slew Rate	0.6	6.0	V/μsec
Peak-to-Peak Output Swing[6]			
f_o ≤ 10kHz	20	20	V
f_o ≤ 20kHz	10	20	V
f_o ≤ 100kHz	2	20	V
Output Offset (at low-pass output with unity gain)	±10	±10	mV
Output Impedance	2	10	Ω
Noise[7]	200	200	μV, rms
Output Current[8]	10	10	mA
POWER SUPPLIES			
Rated Power Supplies	±15	±15	V
Power Supply Range[9]	±5 to ±18	±5 to ±18	V
Supply Current at ±15V (Quiescent)	±12, max	±12, max	mA
TEMPERATURE RANGE			
Specification: Epoxy	−25 to +85	−25 to +85	°C
Storage: Epoxy	−40 to +85	−40 to +85	°C

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

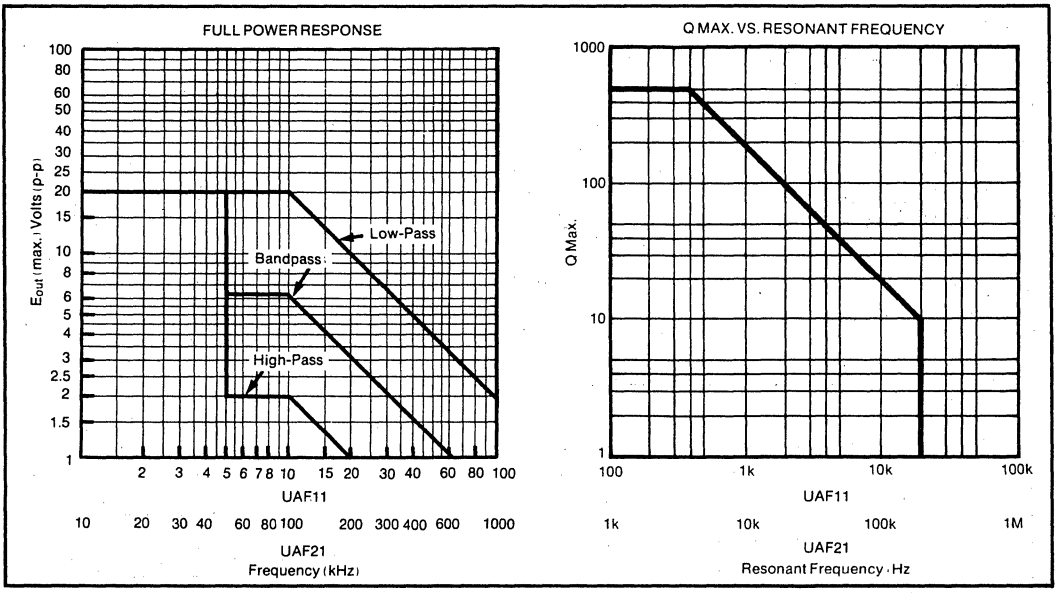
NOTES

1. The UAF21 includes two internal 0.002μF power supply capacitors.
2. Repeatability of f_o using 0.1% frequency determining resistors.
3. T.C.R. of external frequency determining resistors must be added to this figure.
4. Derated 50% from maximum - see Typical Performance Curves.
5. Q stability varies with both the value of Q and the resonant frequency f_o.
6. Low-pass output - see Typical Performance Curves.
7. Measured at the bandpass output with Q = 50 over DC to 50kHz.
8. The current required to drive R_{F1} and R_{F2} (external) as well as C_1 and C_2 must come from this current.
9. For supplies below ±10V, Q max will decrease slightly; filters will operate below ±5V.

PIN CONNECTIONS

Pin 1. High-Pass Output
Pin 2. Optional Pin
Pin 3. Bandpass Output
Pin 4. Q Adjust Point
Pin 5. Common
Pin 6. +Supply
Pin 7. Low-Pass Output
Pin 8. Frequency Adjust
Pin 9. -Supply
Pin 10. Frequency Adjust
Pin 11. Optional Pin
Pin 12. Input 1
Pin 13. Input 2
Pin 14. Input 3

TYPICAL PERFORMANCE CURVES



APPLICATIONS INFORMATION

TRANSFER FUNCTION

The UAF21 uses the state variable technique to produce a basic second order transfer function. The equation describing the three outputs available are:

$$T(\text{Low-Pass}) = \frac{A_{LP}\omega_o^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{Bandpass}) = \frac{A_{BP}(\omega_o/Q)s}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{High-Pass}) = \frac{A_{HP}\,s^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $\omega_o = 2\pi f_o$.

To obtain band reject characteristics the low-pass and high-pass outputs are summed to form a pair of $j\omega$ axis zeros:

$$T(\text{Band-Reject}) = \frac{A\,(s^2 + \omega_o^2)}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $A_{LP} = A_{HP} = A$.

The state variable approach uses two op amp integrators and a summing amplifier to provide simultaneous low-pass, bandpass and high-pass responses. One UAF is required for each two poles of low-pass or high-pass filters and for each pole-pair of bandpass or band-reject filters.

DESIGN PROCEDURE SUMMARY

These procedures give the design steps for the proper application of a UAF and for the selection of the external components. More detailed information on filter theory pertinent to some of the steps can be found in the reference sources listed in Table I.

TABLE I. Useful References.

1. Tobey, Gene, et al, Operational Amplifiers: Design and Applications, Chapter 8, McGraw-Hill Book Company, 1971.
2. Wong, Yu Jen, and William Ott: Function Circuits: Design and Applications, Chapter 6, McGraw-Hill Book Company, 1976.
3. Daniels, Richard W.: Approximation Methods for Electronic Filter Design, McGraw-Hill Book Company, 1974.
4. Zyerev, Anatol I.: Handbook of Filter Synthesis, John Wiley and Sons, 1967.
5. Temes, Gabor C., and Sanjit K. Mitra: Modern Filter Theory and Design, John Wiley and Sons, 1973.

Burr-Brown also manufactures a line of completely self-contained active filters called the ATF76 series. These are available in most popular transfer functions with from 2- to 8-pole responses. They contain all necessary components and do not require any user design effort.

DESIGN STEPS

1. Choose the type of function (low-pass, bandpass, etc.), type of response (Butterworth, Bessel, etc.), number of poles, and cutoff frequency based on the particular application.

   If the transfer function is band-reject see Band-Reject Transfer Function before proceeding to step 2.
2. Determine the normalized low-pass filter parameters (f_n and Q) based on the type of response and number of poles selected in step 1. See Normalized Low-Pass Parameters.
3. If the actual response desired is low-pass go to step 4. For other responses a transformation of variables must be made (low-pass to bandpass or low-pass to high-pass). See Low-Pass Transformation.

4. Determine the actual (denormalized) cutoff frequency, f_o, by multiplying f_n by the actual desired cutoff frequency. See Denormalization of Parameters.
5. Pick the desired UAF configuration (noninverting, inverting or bi-quad). See Configuration Selection Guide and UAF Configurations and Design Equations.
6. Decide whether to use design equations "A" or "B". See Design Equations "A" and "B".
7. Calculate R_{F1} and R_{F2}. See Natural Frequency and UAF Configurations and Design Equations.
8. Determine Q_P. See Q_P Procedure.
9. Select the desired gain for each UAF and calculate the corresponding R_G and R_Q. See Gain (A) and UAF Configurations and Design Equations.

BAND-REJECT TRANSFER FUNCTION

The band-reject is achieved by summing the high-pass and low-pass UAF outputs. Either of the configurations in Figures 2 and 3 can be used to provide the band-reject function if they are used as shown in Figure 1.

The 15kΩ resistor is adjusted for maximum rejection. The circuit in Figure 3 is applicable when using design equations "A" ($A_{LP} = A_{HP}$). When design equations "B" are used ($A_{LP} = 10A_{HP}$), the resistor at pin 7 must be 10 times the resistor at pin 1 to obtain equal pass-band gains above and below f_n.

In either case, the four external UAF resistors (R_G, R_Q, R_{F1} and R_{F2}) should be calculated for f_o and Q of the band-reject filter desired and for A_{LP} to equal the desired pass-band gain. An input constraint is that the input voltage times A_{BP} must not exceed the rated peak-to-peak voltage of the bandpass output, or clipping will result.

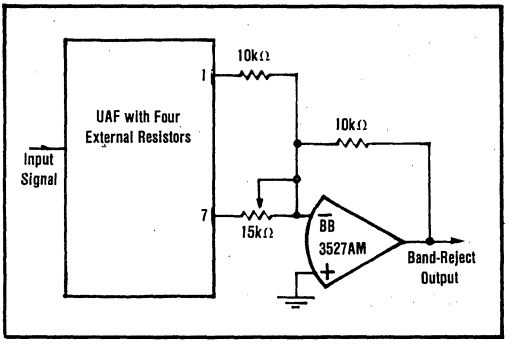


FIGURE 1. Band-Reject Configuration.

NORMALIZED LOW-PASS PARAMETERS

Usual active filter design procedure involves using normalized low-pass parameters. Table II is provided to assist in this step for the more common filter responses. Table III is a FORTRAN program which allows f_n and Q to be calculated for any desired ripple and number of poles for the Chebyschev response. Program inputs are the number of poles (N) and the peak-to-peak ripple (R). Program outputs are f_n and Q, which are used exactly as the values taken from Table II.

TABLE II. Low-Pass Filter Parameters.

Number	Butterworth		Bessel		Chebysev 0.5 dB Ripple		Chebysev 2 dB Ripple	
of Poles	f_n(1)	Q	f_n(1)	Q	f_n(2)	Q	f_n(2)	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	--	1.32475	--	0.626456	--	0.368911	--
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	--	1.50470	--	0.362320	--	0.218308	--
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982828	10.4616
7	1.0	--	1.68713	--	0.256170	--	0.155410	--
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.67658	0.237699	0.89236
	1.0	0.60134	1.85314	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.5308	0.990142	18.6873

1. -3dB frequency.
2. Frequency at which amplitude response passes through the ripple band.

TABLE III. Low-Pass Chebyschev Program.

```
      PI=3.1415926536
      COMPLEX P(10)
      READ 5, N, R
    5 FORMAT (I2,F8.6)
      A=SQRT(EXP(R/4.3429448)-1.)
      B=1./A
      AN=ALOG(B+SQRT(B**2.1.))
      AN=AN/FLOAT(N)
      J=MOD(N, 2)+N/2
      DO 10K=1, J
      RP=SINH(AN)*SIN(PI*FLOAT(2*K-1)/FLOAT(2*N))
      XIP=COSH(AN)*COS(PI*FLOAT(2*K-1)/FLOAT(2*N))
      WN=SQRT(RP**2+XIP**2)
      Q=-WN/(2*RP)
      P(K)=CMPLX(WN,Q)
      IF(MOD(N,2).NE.0.AND K.EQ.J)GO TO 15
      PRINT 20, P(K)
      GO TO 10
   15 F=REAL(P(K))
      PRINT 30, F
   10 CONTINUE
   20 FORMAT (2X"FN="E20.8"Q="E20.8)
   30 FORMAT (2X"FN = "E20.8)
      STOP
      END
```

NOTE: Language variations between computers may require modification of this program.

Note that for bandpass and high-pass filters complex conjugate pole pairs in the actual filter correspond to single poles in the normalized low-pass model. Thus four poles in Table II would correspond to four-pole pairs in a bandpass or high-pass filter.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents a simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. An external op amp and RC network can be used for this purpose.

The cutoff frequency determined by the Table II filter parameters is (1) the -3dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyschev filters passes through the maximum ripple band (to enter the stop band).

LOW-PASS TRANSFORMATION

Low-Pass to High-Pass

The following simple transformation may be used for high-pass filters:

$$f_n \text{ (high-pass)} = \frac{1}{f_n \text{ (low-pass)}}$$

$$Q \text{ (high-pass)} = Q \text{ (low-pass)}$$

Low-Pass to Bandpass

The low-pass to bandpass transformation to generate f_n (bandpass) and Q (bandpass) is much more complicated. It is tedious to do by hand but can be accomplished with the FORTRAN program given in Table IV. This program automates the tranformation

$$s = p/2 \pm \sqrt{(p/2)^2 - 1}.$$

TABLE IV. Low-Pass to Bandpass Transformation Program.

```
      COMPLEX P,S,U
      READ 5, FN, Q, QBP
    5 FORMAT (3F12.5)
      Y=FN*SQRT(1.-1(./(Q*2.))**2)
      X=-FN/Q*2.)
      P=CMPLX(X,Y)
      U=CONJG(P)
      DO 30 I=1,2
      S=P/(2*QBP)
      P=S**2-1.
      T=ATAN2(AIMAG(P),REAL(P))
      IF (T.GE.0.)GO TO 10
      T=2.*3.14159+T
   10 T=T/2.
      A=SQRT(CABS(P))*COS(T)
      B=SQRT(CABS(P))*SIN(T)
      S=S+CMPLX(A,B)
      FN=CABS(S)
      Q=-FN/(2.*REAL(S))
      PRINT 20,FN,Q
   20 FORMAT (2X"FN="F12.5"Q="F12.5)
      IF(AIMAG(U).EQ.0.)GO TO 40
   30 P=U
   40 STOP
      END
```

NOTE: Language variations between computers may require modification of this program.

Program Inputs

1. f_n - From Table II for the low-pass filter of interest
2. Q - From Table II
3. Q_{BP} - Desired Q of the bandpass filter

For filters with an odd number of poles a Q of 0.5 should be used where Q is not given in Table II. Enter 10^5 for Q when transforming zeros on the imaginary axis.

The program transforms each low-pass pole into a bandpass pole pair. Thus a three-pole low-pass input, would result in the pole positions for a three-pole pair bandpass filter requiring three UAF stages.

DENORMALIZATION OF PARAMETERS

Table II shows filter parameters for many 2- to 8-pole normalized low-pass filters. The Q and the normalized undamped natural frequency, f_n for each two-pole section are shown. The Q values do not have to be denormalized and may be used directly as described in the Design Procedure Summary. f_n must be denormalized by multiplying it by the desired cutoff frequency of the actual overall filter to obtain the required frequency, f_o for the design formulas. As an example, consider a 4-pole low-pass Bessel filter with a cutoff frequency of 1000Hz. The first stage would be designed to an f_o of 1432.41Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94Hz and Q of 0.80554. To combine the two stages into the composite filter the low-pass output of the first stage (pin 9) would be connected to the input resistors (R_G) of the second stage.

CONFIGURATION SELECTION GUIDE

It is possible to configure the UAF three different ways. Each configuration produces features that may or may not be desirable for a specific application. The selection guide in Table V is given to assist in determining the most advantageous configuration for a particular application.

UAF CONFIGURATIONS AND DESIGN EQUATIONS

Noninverting Configuration

For applications requiring a bandpass gain of 1V/V, the internal resistor R_3 may be used (input at pin 14) as the gain resistor R_G; thus, only three external resistors are needed to configure the filter.

To use equations "B" connect an 11kΩ resistor between pins 12 and 1. Use equations "B" for frequencies above 8kHz or when R_Q from equations "A" becomes a negative value.

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 10^9/\omega_o = 1.59 \times 10^8/f_o$
2. $A_{BP} = QA_{LP} = QA_{HP}$
3. $R_Q = 10^5/(2Q_p - A_{BP} - 1)$
4. $R_G = (2Q_p - A_{BP} + 1)\ 10^5/A_{BP}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 3.16 \times 10^8/\omega_o = 5.03 \times 10^7/f_o$
2. $A_{BP} = Q/3.16\ A_{LP} = 3.16Q\ A_{HP}$
3. $R_Q = 10^5/(3.48Q_p - A_{BP} - 1)$
4. $R_G = (3.48Q_p - A_{BP} + 1)\ 10^5/A_{BP}$

Inverting Configuration

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 10^9/\omega_o = 1.59 \times 10^8/f_o$
2. $A_{BP} = Q\ A_{LP} = Q\ A_{HP}$
3. $R_G = 10^5\ Q_P/A_{BP}$
4. $R_Q = 2 \times 10^5/(2Q_P + A_{BP} - 1)$

	NONINVERTING INPUT	INVERTING INPUT	BI-QUAD
Outputs Available	BP, LP and HP	BP, LP and HP	BP and LP
Inverted Outputs	BP	HP and LP	BP and LP
Q & Gain Independent of Frequency Resistors?	Yes	Yes	No
Type of Q Variation With Changes in R_F	Constant Q	Constant Q	Constant bandwidth
Other Advantages	May be used with only three external resistors (use internal R_3 as R_G)		R_G and R_Q are small at high frequencies
Parameter Limitations	$2Q_P - A_{BP} > 1$ ($f_o < 8kHz$) $3.48Q_P - A_{BP} > 1$ ($f_o > 8kHz$)	$2Q_P + A_{BP} > 1$ ($f_o < 8kHz$) $3.48Q_P + A_{BP} > 1$ ($f_o > 8kHz$)	None

Summary: The Bi-Quad filter is particularly useful as a bandpass filter if the filter bandwidth must be kept constant as the center frequency is varied. If Q must be kept constant (i.e., constant Q of a bandpass or maintaining constant response of a low-pass or high-pass) one of the other two configurations should be used. The Bi-Quad also has the advantage that R_G and R_Q are smaller than R_G and R_Q of the other two configurations (this is especially useful at high frequencies). The noninverting input configuration has the advantage that for $A_{BP} = 1$, $R_G = 100k\Omega$; therefore R_3 (internal) may be used so that only three external resistors are needed (R_{F1}, R_{F2}, R_Q).

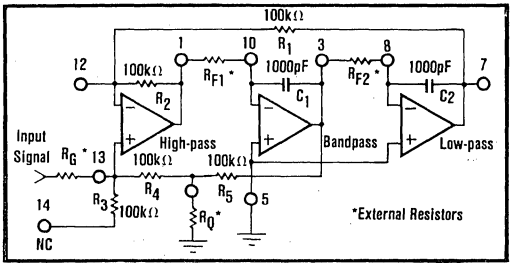


FIGURE 2. Noninverting Configuration.

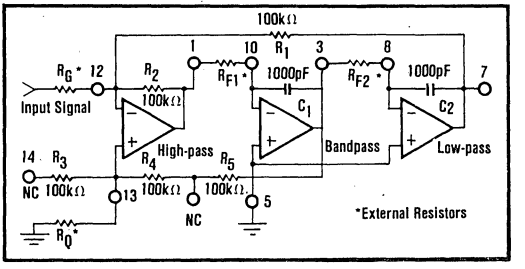


FIGURE 3. Inverting Configuration.

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5kHz$ (UAF11) or $50kHz$ (UAF21)

1. $R_{F1} = R_{F2} = 3.16 \times 10^8 / \omega_o = 5.03 \times 10^7 / f_o$
2. $A_{BP} = Q_P/3.16 = 3.16Q_P A_{HP}$
3. $R_G = 3.16 \times 10^4 Q_P A_{BP}$
4. $R_Q = 2 \times 10^5 (3.48Q_P + A_{BP} - 1)$

BI-QUAD Configuration

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5kHz$ (UAF11) or $50kHz$ (UAF21)

1. $R_{F1} = R_{F2} = 10^9 / \omega_o = 1.59 \times 10^8 / f_o$
2. $Q A_{LP} = A_{BP}$
3. $R_Q = Q_P R_{F1}$
4. $R_G = R_Q \cdot A_{BP}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5kHz$ (UAF11) or $50kHz$ (UAF21)

1. $R_{F1} = R_{F2} = 3.16 \times 10^8 / \omega_o = 5.03 \times 10^7 / f_o$
2. $Q A_{LP} = A_{BP}$
3. $R_Q = 3.16 Q_P R_{F1}$
4. $R_G = R_Q A_{BP}$

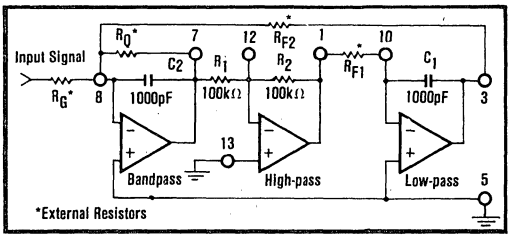


FIGURE 4. Bi-Quad Configuration.

Design Equations "A" and "B"

1. For f_o below 8kHz, either of equations "A" or "B" may be used.
2. For f_o above 8kHz, equations "B" must be used. If equations "A" were used above 8kHz, the filter could become unstable.
3. Equations "A" are for the UAF as it is supplied. When using equations "B", a 11kΩ resistor must be placed in parallel with R_2 (between pins 12 and 1).
4. The values of R_{F1} and R_{F2} calculated with equations "B" are approximately one-third of those calculated with equations "A". Thus there may be an advantage in using equations "B" at low frequencies. Using equations "B" would require use of one more resistor, but that would not alter or affect filter performance in any manner.
5. Using the negative gain values for A_{LP} or A_{HP} or A_{BP} could result in the negative values for resistors R_G and R_Q. So the absolute value of the gain should always be used in the equations.
6. Under some circumstances the value of R_Q using equations "A" will be negative. If this occurs, use design equations "B".

Natural Frequency (f_o)

1. f_o for each one pole-pair bandpass filter is the center frequency (f_C). f_C is defined as $f_C = \sqrt{f_1 f_2}$ where f_1 is the lower -3dB point and f_2 is the upper -3dB point of the pole-pair response.

2. To obtain f_o below 100Hz using practical resistor values, capacitors may be paralleled with C1 and C2 to reduce the size of R_{F1} and R_{F2}. If capacitors are added in parallel,

$$R_{F1}\text{ (new)} = R_{F2}\text{ (new)} = R_{F1}\text{ (old)}\ \frac{1000pF}{C + 1000pF}$$

where R_F (new) is the new lower value frequency resistor, C is the value of the two external capacitors placed across C1 and C2 (between pins 10 and 3 and pins 8 and 7 and R_{F1} (old) is the value calculated in the simplified design equations.

Q-Factor

1. For bandpass filters $Q = \frac{f_o}{3dB\text{ bandwidth}}$
2. When designing low-pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.

Qp Procedure

1. If the "f_o times Q" product is greater than 10^4 (or 10^5 for the UAF21), it is possible for the measured filter Q to be different from the calculated value of Q. This effect is the result of nonideal characteristics of operational amplifiers. It can be compensated for by introducing the parameter Q_P into the design equations.
2. Calculate the f_o Q product for the filter. If the product is above 10^4Hz (or 10^5 for the UAF21), locate the corresponding f_oQ_P product on the curve in Figure 5. Divide f_oQ_P by f_o to obtain Q_P. Use Q_P as indicated in the design equations. For f_oQ products below 10^4Hz (or 10^5 for the UAF21), $Q_P = Q$.

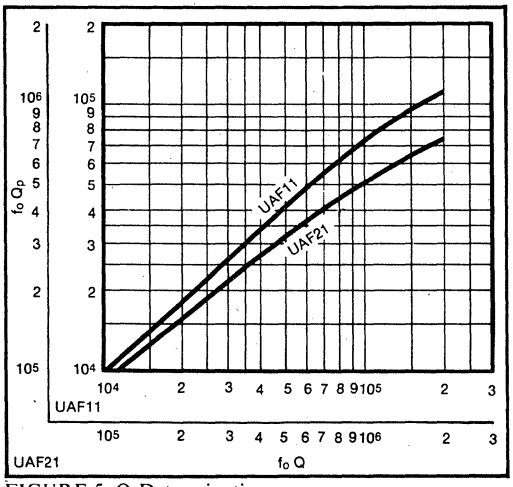


FIGURE 5. Q_PDetermination.

Gain (A)

1. The gain (V/V) of each filter section is:
   A_{LP} - for low-pass output - gain at DC
   A_{BP} - for bandpass output - gain at f_o
   A_{HP} - for high-pass output - gain at high frequencies.
2. Refer to the Typical Performance Curves for full power response. When selecting the gain, insure the limits of the curve are not exceeded for the desired voltage range.

DETAILED TRANSFER FUNCTION EQUATIONS

The following equations show the action of all the internal and external UAF filter components. They are not required for the regular design procedure but could be used if a detailed analysis is required.

NONINVERTING INPUT CONFIGURATION

1. $\omega_o^2 = R_2\ (R_1 R_{F1} C_1 R_{F2} C_2)$
2. $Q = \left[1 + \left(\frac{R_1}{R_G}\right)\left(\frac{R_1}{R_1 + R_2}\right)\right] \cdot (1 + 10^5\ R_Q) \sqrt{\frac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2}}$
3. $R_1 = 10^5 + 10^5\ R_Q\ (10^5 + R_Q)$
4. $Q\ A_{LP} = Q\ A_{HP}\ R_1\ R_2 = A_{BP}\sqrt{R_1 R_{F1} C_1\ (R_2 R_{F2} C_2)}$
5. $A_{HP} = 10^5\ (2 + 10^5\ R_Q)\ R_G$

INVERTING INPUT CONFIGURATION

1. $\omega_o^2 = R_2\ (R_1 R_{F1} C_1 R_{F2} C_2)$
2. $Q = R_P\ (1 + 2 \times 10^5\ R_Q) \sqrt{R_{F1} C_1 / (R_1 R_2 R_{F2} C_2)}$
3. $Q\ A_{LP} = Q\ R_1\ A_{HP}\ R_2 = A_{BP}\sqrt{R_1 R_{F1} C_1 / (R_2 R_{F2} C_2)}$
4. $A_{BP} = \sqrt{R_1 R_2 R_{F2} C_2 / (R_{F1} C_1)}\ Q\ R_G$
5. $1\ R_P = 1\ R_1 + 1\ R_2 + 1\ R_G$

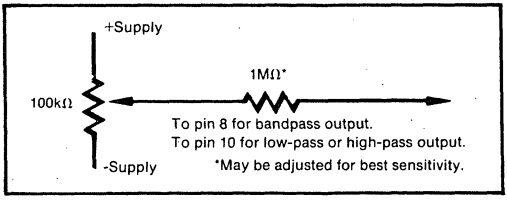
BI-QUAD CONFIGURATION

1. $\omega_o^2 = R_2\ (R_1 R_{F1} C_1 R_{F2} C_2)$
2. $Q = R_Q C_2\ \omega_o$
3. $Q\ A_{LP}\ (\omega_o R_1 C_2) = A_{HP} = R_Q\ R_G$

Offset Error Adjustment

DC offset errors will be minimized by grounding pin 5 through a resistor equal to 1/2 the value of R_{F1} or R_{F2}. The DC offset adjustment shown here may be used if required.

Offset errors will increase with increases in R_F.



Design Example

It is desired to design a 5-pole Bessel, Low-Pass Filter with $f_o = 3.3$kHz and $A_{LP} = 1$. We will use the UAF11 to implement this filter.

From Table II the following values of f_n and Q are obtained.

Complex Poles:
$f_n = 1.55876$
$Q = 0.56354$
$f_n = 1.75812$
$Q = 0.91652$

Simple Pole:
$f_n = 1.50470$

Using the above shown values of f_n and Q, we now will proceed to design the three stages of filter separately.

Any one of the three configurations can be used. We will select inverting configuration.

For Stage 1.

$f_o = 3.3kHz \times f_n = 3.3kHz \times 1.55876 = 5144Hz$

Since $f_o > 5kHz$, equations "B" would be used, thus an 11kΩ resistor must be connected between pins 12 and 1.

$$R_{F1} = R_{F2} = \frac{5.03 \times 10^7}{5144} = 9778\Omega$$

$f_oQ = 5144 \times 0.56354 = 2.9 \times 10^3$

$f_oQ < 10^4$, $\therefore Q_P = Q = 0.56354$

$$A_{BP} = \frac{Q_P}{3.16} \quad A_{LP} = \frac{0.56354}{3.16} \times 1 = 0.17834$$

$$R_G = \frac{3.16 \times 10^4 Q_P}{A_{BP}} = \frac{3.16 \times 10^4 \times 0.56354}{0.17834} = 99.85k\Omega$$

$$R_Q = \frac{2 \times 10^5}{3.48Q_P + A_{BP}-1} = \frac{2 \times 10^5}{3.48 \times 0.56354 + 0.17834 - 1} = 175.52k\Omega$$

For Stage 2.

$f_o = 3.3kHz \times f_n = 3.3kHz \times 1.75812 = 5802Hz$

Since $f_o > 5kHz$, equations "B" would again be used, and an 11kΩ resistor would be connected between pins 12 and 1 of the second UAF stage.

$$R_{F1} = R_{F2} = \frac{5.03 \times 10^7}{5802} = 8669\Omega$$

$f_oQ = 5802 \times 0.91652 = 5.32 \times 10^3$

$f_oQ < 10^4$, $\therefore Q_P = Q = 0.91652$

$$A_{BP} = \frac{Q_P}{3.16} \quad A_{LP} = \frac{0.91652}{3.16} \times 1 = 0.29004$$

$$R_G = \frac{3.16 \times 10^4 Q_P}{A_{BP}} = \frac{3.16 \times 10^4 \times 0.91652}{0.29004} = 99.86k\Omega$$

$$R_Q = \frac{2 \times 10^5}{(3.48 Q_P + A_{BP}-1)} = \frac{2 \times 10^5}{(3.48 \times 0.91652 + 0.29004 - 1)} = 80.66k\Omega$$

For Stage 3.

$f = 3.3kHz \times f_n = 3.3kHz \times 1.50470 = 4966Hz$

For the simple pole,

$$RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 4966} = 3.2049 \times 10^{-5}$$

3300pF (or any convenient value)

$$R = \frac{3.2049 \times 10^{-5}}{3300 \times 10^{-12}} = 9.71k\Omega$$

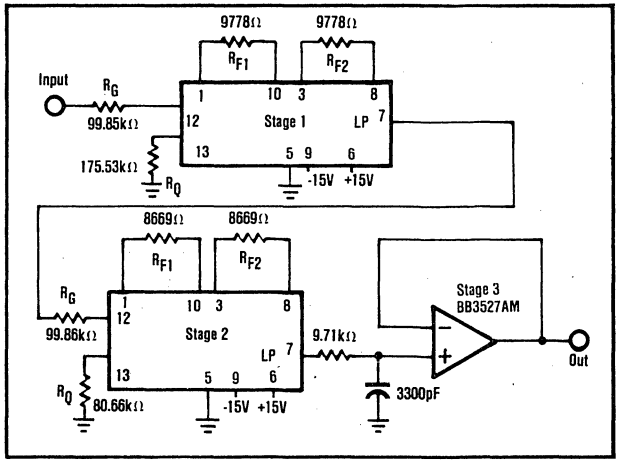


FIGURE 6. Overall Circuit.

BURR-BROWN®

UAF41

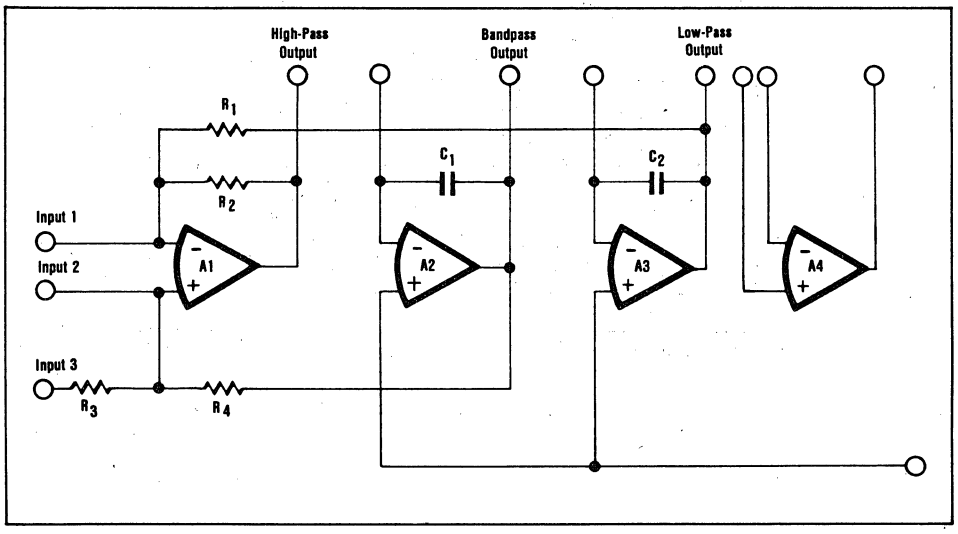
UNIVERSAL ACTIVE FILTER

FEATURES

- LOW COST
- SMALL SIZE
  Single wide DIP package
- FULLY CHARACTERIZED PARAMETERS
- HYBRID CONSTRUCTION
- IMPROVED PERFORMANCE
  1% frequency accuracy
  Q range of 0.5 to 500.
  NPO capacitors and thin-film resistors
  Uncommitted op amp included

BENEFITS

- SAVES PRINTED CIRCUIT BOARD SPACE
- SAVES DESIGN TIME
  Calculate only four resistance values
  Design directly from this data sheet
  Versatile building block for filter design
- HIGH RELIABILITY.
- HIGH STABILITY



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

The UAF41 is a versatile two-pole active filter. It uses a three operational amplifier double integrator feedback loop to generate a complex pole pair (two conjugate poles). The location of the poles in the complex plane (and thus the natural frequency and Q) are determined by external, user supplied resistors. Either three or four resistors are used depending on the particular configuration chosen.

The UAF41 produces three transfer functions simultaneously - low-pass, high-pass, and bandpass - which are available at three separate outputs. The fourth basic transfer function - the band-reject or notch - can be obtained simply by summing the high-pass and low-pass outputs using the uncommitted amplifier (A4) contained in the UAF41. The uncommitted op amp can also be used to add a single-pole response for complex filters requiring an odd number of poles.

More complex higher-order filters can readily be obtained by cascading UAF's. This is easily done with the UAF41 since the high input impedance and low output impedance associated with the operational amplifiers used prevents the series connected stages from interacting (e.g., no frequency pull due to following stage loading). This data sheet contains the design procedures for an easy selection of resistor values for the stagger tuning of cascaded stages.

The versatility of the UAF41 makes it a general purpose building block for a wide variety of active filter applications. Its universal nature, ease of use, small size, and low cost allows the user the convenience of keeping units on hand for immediate use whenever a filter requirement arises.

TRANSFER FUNCTION

The UAF41 uses the state variable technique to produce a basic second order transfer function. The equations describing the three outputs available are:

$$T(\text{Low-Pass}) = \frac{A_{LP}\omega_o^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{Bandpass}) = \frac{A_{BP}\,(\omega_o/Q)s}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{High-Pass}) = \frac{A_{HP}\,s^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

To obtain band-reject characteristics the low-pass and high-pass outputs are summed to form a pair of $j\omega$ axis zeros:

$$T(\text{Band-Reject}) = \frac{A\,(s^2 + \omega_o^2)}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $A_{LP} = A_{HP} = A$.

The state variable approach uses two op amp integrators (A2 and A3 in the simplified schematic below) and a summing amplifier (A1) to provide simultaneous low-pass, bandpass, and high-pass responses. One UAF41 is required for each two poles of low-pass or high-pass filters and for each pole-pair of bandpass or band-reject filters.

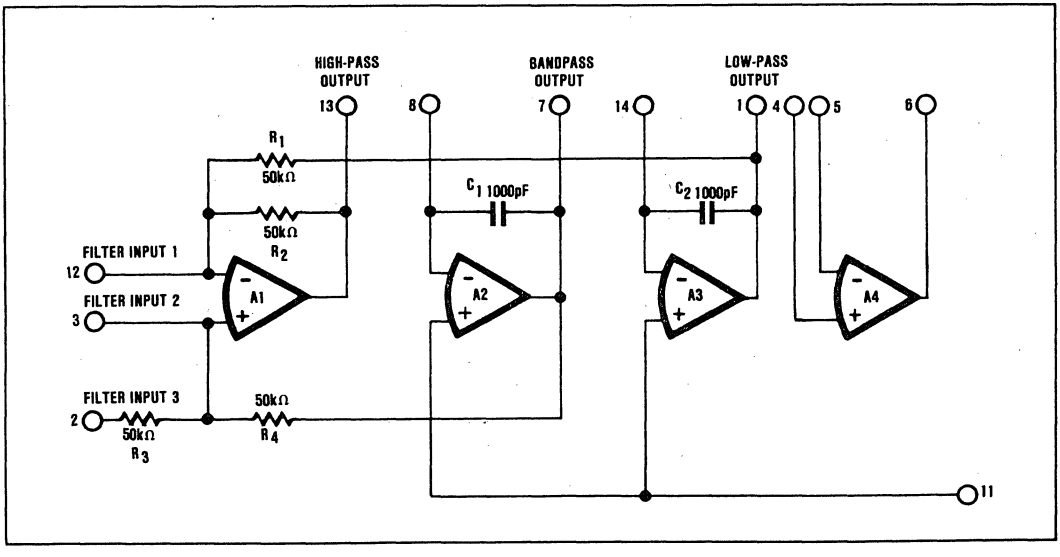


FIGURE 1. UAF41 Schematic.

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and with rated supply unless otherwise noted.

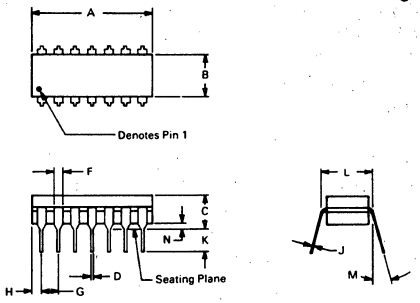
MODEL	UAF41
INPUT	
Input Bias Current	±40nA
Input Voltage Range	±10V
Input Resistance(1)	50kΩ
TRANSFER CHARACTERISTICS	
Frequency Range (f_o)	0.001Hz to 25kHz
f_o Accuracy(2), max	±1%
f_o Stability(3)	±0.002%/°C
Q Range(4)	0.5 to 500
Q Stability(5)	
@ f_o Q ≤ 10^4	±0.01%/°C
@ f_o Q ≤ 10^5	±0.025%/°C
Q Repeatability at f_o Q ≤ 10^5	±10%
Gain Range	0.1V/V to 50V/V
OUTPUT	
Peak-to-Peak Output Swing(6)	20V
Output Offset(7)	
(at L.P. output with unity gain)	±20mV
Output Impedance	1Ω
Noise(8)	200μV, rms
Output Current(9)	5mA
UNCOMMITTED AMP CHARACTERISTICS	
Input Offset Voltage	5mV
Input Bias Current	40nA
Input Impedance	1MΩ
Large Signal Voltage Gain	85dB
Output Current	5mA
POWER SUPPLIES	
Rated Power Supplies	±15VDC
Power Supply Range(10)	±5VDC to ±18VDC
Supply Current @ ±15V (Quiescent), max	7mA
TEMPERATURE RANGE	
Specification Temperature Range	-25°C to +85°C
Storage Temperature Range	-25°C to +85°C

NOTES:

1. For noninverting input configuration with A_{BP} * 1.
2. The tolerance of external frequency determining resistors must be added to this figure.
3. T.C.R. of external frequency determining resistors must be added to this figure.
4. See Performance Curves for Q_{max} vs F curve.
5. Q stability varies with both the value of Q and the resonant frequency f_o.
6. See Performance Curves for full power response curve.
7. $R_{F1} = R_{F2} < 100k\Omega$ at low-pass output with unity gain.
8. Measured at the bandpass output with Q @ 50 over DC to 50kHz.
9. The current required to drive R_{F1} and R_{F2} (external) as well as C1 and C2 must come from this current.
10. For supplies below ±10V, Q_{max} will decrease slightly; filters will operate below ±5V.

MECHANICAL

14-Pin Plastic DIP Package



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.660	.785	16.76	19.94
B	.220	.280	5.59	7.11
C	–	.200	–	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095		
J	.008	.015	0.20	0.38
K	.100	–	2.54	–
L	.300 BASIC		7.62 BASIC	
M	–	15°	–	15°
N	.020	.050	0.51	1.27

ROW SPACING: 7.63mm (0.300")
WEIGHT: 1.1 grams max

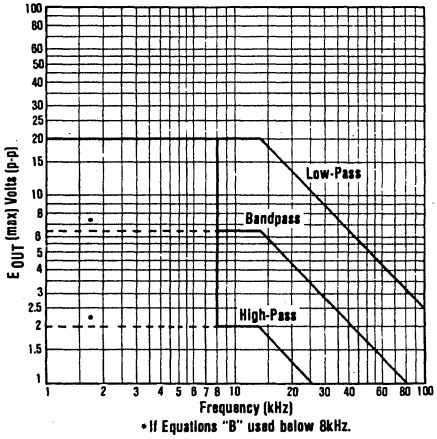
Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

PIN CONNECTIONS

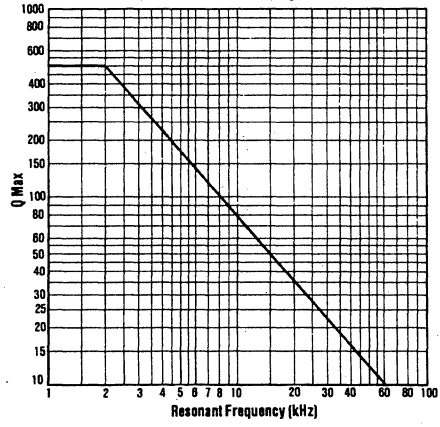
Pin 1 - LOW-PASS OUTPUT
Pin 2 - FILTER INPUT 3
Pin 3 - FILTER INPUT 2
Pin 4 - AUXILIARY AMP + INPUT
Pin 5 - AUXILIARY AMP - INPUT
Pin 6 - AUXILIARY AMP OUTPUT
Pin 7 - BANDPASS OUTPUT
Pin 8 - FREQUENCY ADJUST
Pin 9 - NEGATIVE SUPPLY
Pin 10 - POSITIVE SUPPLY
Pin 11 - COMMON
Pin 12 - FILTER INPUT 1
Pin 13 - HIGH-PASS OUTPUT
Pin 14 - FREQUENCY ADJUST

TYPICAL PERFORMANCE CURVES

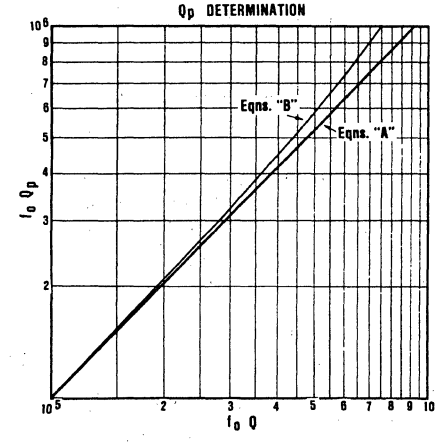
FULL POWER RESPONSE



Q MAX VS RESONANT FREQUENCY



Q_P DETERMINATION



DESIGN PROCEDURE SUMMARY

This summary gives the design steps for the proper application of UAF41s and for the selection of the external components. More detailed information on filter theory pertinent to some of the steps can be found in the reference sources listed on last page.

DESIGN STEPS:

1. Choose the type of function (low-pass, bandpass, etc.), type of response (Butterworth, Bessel, etc.), number of poles, and cutoff frequency based on the particular application.

   If the transfer function is band-reject see Band-Reject Transfer Function before proceeding to step 2.
2. Determine the normalized low-pass filter parameters (f_n and Q) based on the type of response and number of poles selected in step 1. See Normalized Low-Pass Parameters.
3. If the actual response desired is low-pass go to step 4. For other responses a transformation of variables must be made (low-pass to bandpass or low-pass to high-pass). See Low-Pass Transformation.
4. Determine the actual (denormalized) cutoff frequency, f_o, by multiplying f_n by the actual desired cutoff frequency. See Denormalization of Parameters.
5. Pick the desired UAF configuration (noninverting, inverting or bi-quad) see Configuration Selection Guide and UAF41 Configuration and Design Equations.
6. Decide whether to use design equations "A" or "B". See Design Equations "A" and "B".
7. Calculate R_{F1} and R_{F2}. See Natural Frequency and UAF Configurations and Design Equations.
8. Determine Q_P. See Q_P Procedure.
9. Select the desired gain for each UAF and calculate the corresponding R_G and R_Q. See Gain (A) and UAF41 Configurations and Design Equations.

NORMALIZED LOW-PASS PARAMETERS

Usual active filter design procedure involves using normalized low-pass parameters. Table I is provided to assist in this step for the more common filter responses. Table II is a BASIC program which allows f_n and Q to be calculated for any desired ripple and number of poles for the Chebyschev response. Consult the reference on last page for other information.

Note that for bandpass and high-pass filters, complex conjugate pole pairs in the actual filter correspond to single poles in the normalized low-pass model. Thus **four poles** in Table I would correspond to **four-pole pairs** (eight poles) in a bandpass or high-pass filter.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents a simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. The uncommitted internal op amp with an external RC network can be used for this purpose.

The cutoff frequency determined by the Table I filter parameters is (1) the -3dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyschev filters passes through the maximum ripple band (to enter the stop band). A filter that is designed as a low-pass filter will not give the corresponding response as a band-pass filter.

TABLE I. Low-Pass Filter Parameters.

NUMBER OF POLES	BUTTERWORTH		BESSEL		CHEBYSCHEV 0.5dB RIPPLE		CHEBYSCHEV 2dB RIPPLE	
	fn(1)	Q	fn(1)	Q	fn(2)	Q	fn(2)	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	----	1.32475	----	0.626456	----	0.368911	----
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	----	1.50470	----	0.362320	----	0.218308	----
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982828	10.4616
7	1.0	----	1.68713	----	0.256170	----	0.155410	----
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.67657	0.237699	0.89236
	1.0	0.60134	1.83514	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.5305	0.990142	18.6873

(1) -3 dB Frequency
(2) Frequency at which amplitude response passes through the ripple band.

NORMALIZED LOW-PASS CHEBYSCHEV

Table II gives a BASIC program for the determination of f_n and Q for a general normalized Chebyschev low-pass filter of any ripple and number of poles. Program inputs are the number of poles (N) and the peak-to-peak ripple (R). Program outputs are f_n and Q, which are used exactly as the values taken from Table I.

BAND-REJECT TRANSFER FUNCTION

The band-reject is achieved by summing the high-pass and low-pass UAF outputs. Either of the configurations in Figures 3 and 4 can be used to provide the band-reject function if they are used as shown in Figure 2.

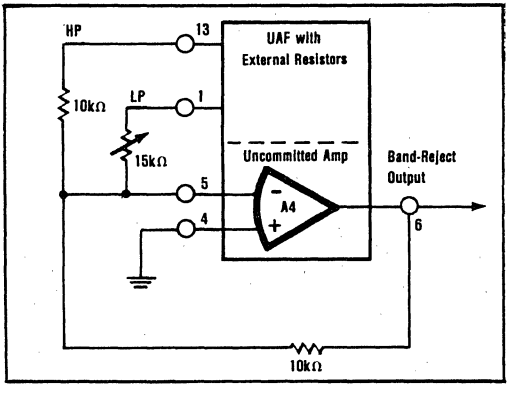
The 15kΩ resistor is adjusted for maximum rejection. The circuit in Figure 2 is applicable when using design equations "A" ($A_{LP} = A_{HP}$). When design equations "B" are used ($A_{LP} = 10A_{HP}$), the resistor at pin 1 must be 10 times the resistor at pin 13 to obtain equal pass-band gains above and below f_n.

In either case, the four external UAF resistors (R_G, R_Q, R_{F1} and R_{F2}) should be calculated for f_o and Q of the

band-reject filter desired and for A_{LP} to equal the desired pass-band gain. An input constraint is that the input voltage times A_{BP} must not exceed the rated peak-to-peak voltage of the bandpass output, or clipping will result. Note that the band-reject function is suitable only for a single UAF section. In a multi-section filter the inputs to successive stages are "preconditioned" by the preceding stages.

TABLE II. Low-Pass Chebyschev Program.

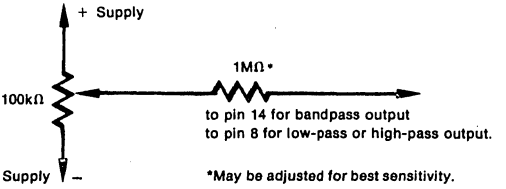
```
110 REM THIS IS A NORMALIZED LOW-PASS CHEBYSCHEV PROGRAM
120 REM BY BARRY A. EHRMAN
130 PRINT "NORMALLIZED CHEBYSCHEV"
140 PRINT "LOW-PASS FILTER"
150 PRINT
160 PRINT "BY BARRY A. EHRMAN"
170 PRINT
180 PRINT
185 PI=3.1415927
190 PRINT "NUMBER OF POLES?"
200 INPUT N
210 PRINT
220 PRINT "PEAK-TO -PEAK RIPPLE IN DB?"
230 INPUT R
240 PRINT
250 A=SQR(EXP(R/4.3429448)-1)
260 B=1/A
270 AN=LOG(B+SQR(B^2+1))
280 AN=AN/N
290 L=INT(N/2)
300 J=INT((N+1)/2)
310 FOR K=1 TO J
320 RP=((EXP(AN)-EXP(-AN))/2)*SIN(PI*((2*K)-1)/(2*N))
330 XIP=((EXP(AN)+EXP(-AN))/2)*COS(PI*((2*K)-1)/(2*N))
340 WN=SQR(RP^2+XIP^2)
350 Q=WN/(2*RP)
360 IF L<>J AND K=J THEN 410
370 PRINT "FN= ";WN
380 PRINT "Q = ";Q
390 PRINT
400 GOTO 430
410 PRINT "FN= ";WN
420 PRINT "Q =  RC POLE "
430 NEXT K
440 END
```



OFFSET ERROR ADJUSTMENT

DC offset errors will be minimized by grounding pin 3 through a resistor equal to 1/2 the value of R_{F1} or R_{F2}. The DC offset adjustment shown here may be used if required.

Offset errors will increase with increases in R_F.



LOW-PASS TRANSFORMATION

LOW-PASS TO HIGH-PASS

The following simple transformation may be used for high-pass filters:

$$f_n \text{ (high-pass)} = \frac{1}{f_n \text{ (low-pass)}}$$

$$Q \text{ (high-pass)} = Q \text{ (low-pass)}$$

LOW-PASS TO BANDPASS

The low-pass to bandpass transformation to generate f_n (bandpass) and Q (bandpass) is much more complicated. It is tedious to do by hand but can be accomplished with the BASIC program given in Table III. This program automates the transformation

$$s = p/2 \pm \sqrt{(p/2)^2 - 1}.$$

TABLE III. Low-Pass to Bandpass BASIC Transformation Program. (See last page of this PDS).

PROGRAM INPUTS:

1. f_n - From Table I for the low-pass filter of interest
2. Q - From Table I
3. Q_{BP} - Desired Q of the bandpass filter

For filters with an odd number of poles a Q of 0.5 should be used where Q is not given in Table I. Enter 10^5 for Q when transforming zeros on the imaginary axis.

The program transforms each low-pass pole into a bandpass pole pair. Thus a three-pole low-pass input, would result in the pole positions for a three-pole pair bandpass filter requiring three UAF stages.

DENORMALIZATION OF PARAMETERS

Table I shows filter parameters for many 2- to 8-pole normalized low-pass filters. The Q and the normalized undamped natural frequency, f_n for each two-pole section are shown. The Q values do not have to be denormalized and may be used directly as described in the Design Procedure Summary. f_n must be denormalized by multiplying it by the desired cutoff frequency of the actual overall filter to obtain the required frequency, f_o for the design formulas. As an example, consider a 4-pole low-pass Bessel filter with a cutoff frequency of 1000Hz. The first stage would be designed to an f_o of 1432.41Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94Hz and a Q of 0.80554. To combine the two stages into the composite filter the low-pass output of the first stage (pin 1) would be connected to the input resistors (R_G) of the second stage.

DESIGN EQUATIONS "A" AND "B"

1. For f_o below 8kHz, either of equations "A" or "B" may be used.
2. For f_o above 8kHz, equations "B" must be used. If equations "A" were used above 8kHz, the filter could become unstable.
3. Equations "A" are for the UAF as it is supplied. When using equations "B", a 5.49kΩ resistor must be placed in parallel with R_2 (between pins 12 and 13).
4. The values of R_{F1} and R_{F2} calculated with equations "B" are approximately one-third of those calculated with equations "A". Thus there may be an advantage in using equation "B" at low frequencies. Using equation "B" would require use of one more resistor, but that would not alter or affect filter performance in any manner.
5. Using the negative gain values for A_{LP} or A_{HP} or A_{BP} could result in the negative values for resistors R_G and R_Q. So the absolute value of the gain should always be used in the equations.

GAIN (A)

1. The gain (V/V) of each filter section is:
   A_{LP} - for low-pass output - gain at DC
   A_{BP} - for bandpass output - gain at f_o
   A_{HP} - for high-pass output - gain at high frequencies.
2. Refer to Performance Curves for full power response. When selecting the gain, insure that the limits of the curve are not exceeded for the desired voltage range.

NATURAL FREQUENCY (f_o)

1. f_o for each one pole-pair bandpass filter is the center frequency (f_C). f_C is defined as $f_C = \sqrt{f_1 f_2}$ where f_1 is the lower -3dB point and f_2 is the upper -3dB point of the pole pair response.
2. To obtain f_o below 100Hz using practical resistor values, capacitors may be paralleled with C1 and C2 to reduce the size of R_{F1} and R_{F2}. If capacitors are added in parallel,

$$R_{F1}\text{ (new)} = R_{F2}\text{ (new)} = R_{F1}\text{ (old)}\ \frac{1000\text{pF}}{C + 1000\text{pF}}$$

where R_F (new) is the new lower value frequency resistor, C is the value of the two external capacitors placed across C1 and C2 (between pins 7 and 8 and pins 1 and 14 and R_{F1} (old) is the value calculated in the simplified design equations.

Q-FACTOR

1. For bandpass filters $Q = \dfrac{f_o}{\text{3dB bandwidth}}$
2. When designing low-pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.
3. Q repeatability (Q change from unit-to-unit) is typically ±5% for f_oQ products less than 10^4. The Q repeatability error increases as the f_oQ product increases to approximately ±10% for f_oQ products near 10^5.

Q_P PROCEDURE

1. If the "f_o times Q" product is greater than 10^5, it is possible for the measured filter Q to be different from the calculated value of Q. This effect is the result of non-ideal characteristics of operational amplifiers. It can be compensated for by introducing the parameter Q_P into the design equations.
2. Calculate the f_oQ product for the filter. If the product is above 10^5Hz, locate the corresponding f_oQ_P product in the Performance Curves. Divide f_oQ_P by f_o to obtain Q_P. Use Q_P as indicated in the design equations. For f_oQ products below 10^5Hz, $Q_P = Q$.

CONFIGURATION SELECTION GUIDE

It is possible to configure the UAF41 three different ways. Each configuration produces features that may or may not be desirable for a specific application. This selection guide is given to assist in determining the most advantageous configuration for a particular application.

	NONINVERTING INPUT	INVERTING INPUT	BI QUAD
Outputs Available	BP, LP and HP	BP, LP and HP	BP and LP
Outputs Inverted with respect to the Input	BP	HP and LP	BP and LP
Q & Gain Independent of Frequency Resistors?	Yes	Yes	No
Type of Q Variation With Changes in R_F	Constant Q	Constant Q	Constant Bandwidth
Other Advantages	May eliminate one external resistor (use internal R_3 as R_G)		R_G and R_Q are small at high frequencies. Easy single-supply operation.
Parameter Limitations	$2Q_p - A_{BP} > 1$ (Eqns. "A") $3.48Q_p - A_{BP} > 1$ (Eqns. "B")	$2Q_p + A_{BP} > 1$ (Eqns. "A") $3.48Q_p + A_{BP} > 1$ (Eqns. "B")	No HP Output

Summary: The Bi-Quad filter is particulary useful as a bandpass filter if the filter bandwidth must be kept constant as the center frequency is varied. If Q must be kept constant (i.e., constant Q of a bandpass or maintaining a constant response of a low-pass or high-pass) one of the other two configurations should be used. The Bi-Quad also has the advantage that R_G and R_Q are smaller than with the other two configurations (this is especially useful at high frequencies). The noninverting input configuration has the advantage that for $A_{BP} = 1$, $R_G = 50k\Omega$; therefore R_3 (internal) may be used so that only three external resistors are needed (R_{F1}, R_{F2}, R_Q). For single supply operation of the UAF41 in bi-quad filters, bias pin 3 and pin 11 to 1/2 $+V_{CC}$.

UAF41 CONFIGURATIONS AND DESIGN EQUATIONS

NONINVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2. $A_{BP} = Q\,A_{LP} = Q\,A_{HP}$

3. $R_G = \frac{5.0 \times 10^4\, Q}{A_{BP}\, Q_P}$

4. $R_Q = \frac{5.0 \times 10^4}{2Q_P - \frac{A_{BP}\, Q_P}{Q} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o \geq 8kHz$

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2. $A_{BP} = \frac{Q}{3.16} A_{LP} = 3.16\,Q\,A_{HP}$

3. $R_G = \frac{5.0 \times 10^4\, Q}{A_{BP}\, Q_P}$

4. $R_Q = \frac{5.0 \times 10^4}{3.48Q_p - \frac{A_{BP}\, Q_P}{Q} - 1}$

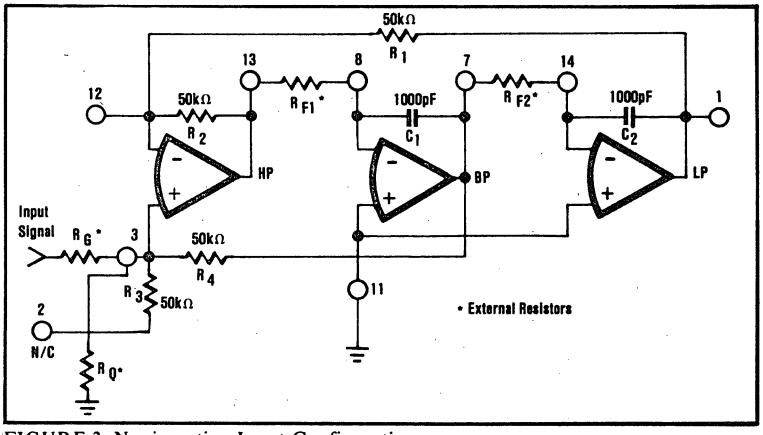


FIGURE 3. Noninverting Input Configuration.

INVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$
2. $A_{BP} = Q_P A_{LP} = Q_P A_{HP}$
3. $R_G = \frac{5.0 \times 10^4 Q_P}{A_{BP}}$
4. $R_Q = \frac{5.0 \times 10^4}{2Q_P + A_{BP} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o > 8$kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$
2. $A_{BP} = \frac{Q_P}{3.16} A_{LP} = 3.16\, Q_P\, A_{HP}$
3. $R_G = \frac{1.58 \times 10^4 Q_P}{A_{BP}}$
4. $R_Q = \frac{5.0 \times 10^4}{3.48 Q_P + A_{BP} - 1}$

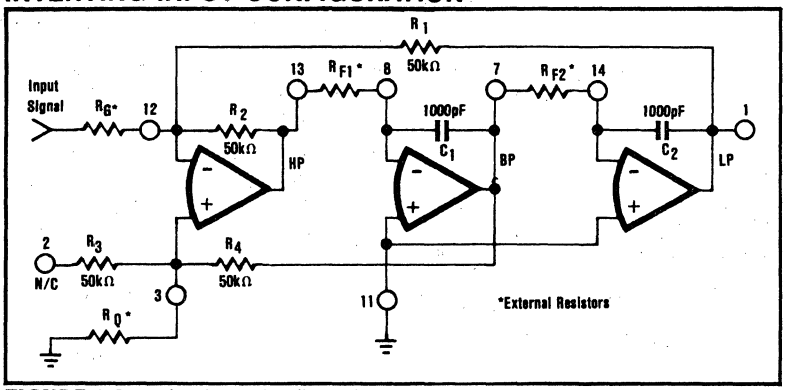


FIGURE 4. Inverting Input Configuration.

BI-QUAD CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$
2. $A_{BP} = Q\, A_{LP}$
3. $R_Q = Q_P R_{F1}$ *
4. $R_G = \frac{R_Q}{A_{BP}}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o > 8$kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$
2. $A_{BP} = 3.16\, Q\, A_{LP}$
3. $R_Q = 3.16\, Q_P\, R_{F1}$
4. $R_G = \frac{R_Q}{A_{BP}}$

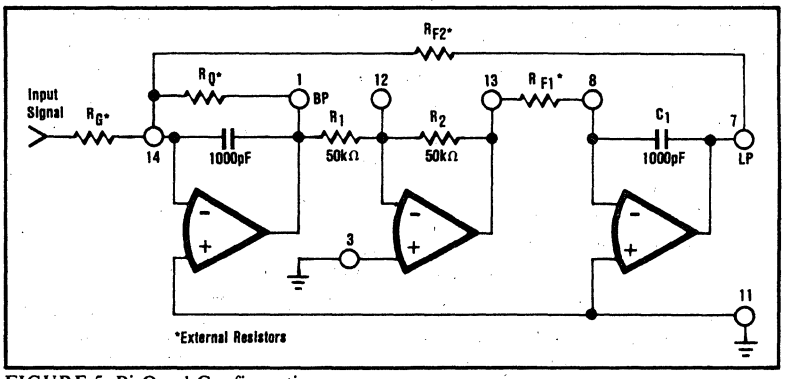


FIGURE 5. Bi-Quad Configuration.

† To use equations "B" connect a 5.49kΩ resistor between pins 12 and 13.
Equations "B" are also valid for frequencies below 8kHz.

DETAILED TRANSFER FUNCTION EQUATIONS

The following equations show the action of all the internal and external UAF41 filter components. They are not required for the regular design procedure but could be used if a detailed analysis is required.

NONINVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$
2. $Q = \frac{1 + \frac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \frac{R_2}{R_1}} \left(\frac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2}\right)^{1/2}$
3. $Q\, A_{LP} = Q\, A_{HP} \left(\frac{R_1}{R_2}\right) = A_{BP} \left(\frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$
4. $A_{LP} = \frac{1 + \frac{R_1}{R_2}}{R_G \left(\frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4}\right)}$
5. $A_{HP} = \frac{R_2}{R_1} A_{LP} = \frac{1 + \frac{R_2}{R_1}}{R_G \left(\frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4}\right)}$
6. $A_{BP} = \frac{R_4}{R_G}$

INVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$
2. $Q = \left(1 + \frac{R_4}{R_Q}\right) \frac{1}{\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}\right)} \left(\frac{R_{F1} C_1}{R_1 R_2 R_{F2} C_2}\right)^{1/2}$
3. $Q\, A_{LP} = Q\, A_{HP} \left(\frac{R_1}{R_2}\right) = A_{BP} \left(\frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$
4. $A_{LP} = \frac{R_1}{R_G}$
5. $A_{HP} = \frac{R_2}{R_1} A_{LP} = \frac{R_2}{R_G}$
6. $A_{BP} = \left(1 + \frac{R_4}{R_Q}\right) \frac{1}{R_G \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}\right)}$

BI-QUAD CONFIGURATION

1. $\omega_o^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$
2. $Q = R_Q C_2 \omega_o$
3. $A_{BP} = \frac{Q\, A_{LP}}{\omega_o R_{F2} C_2} = \frac{R_Q}{}$

ACTIVE FILTER DESIGN EXAMPLES USING THE DESIGN PROCEDURE OUTLINED IN DESIGN STEPS SECTION.

Example 1.

It is desired to design a three-pole, 0.5dB ripple, Chebyschev High-Pass Filter; the cutoff frequency f_c = 2kHz, Gain $A_{HP} = +1$.

Step 1.

The type of transfer function (high-pass), the type of response (Chebyschev), number of poles (3), and the cut off frequency (f_c) are chosen depending upon the particular application and are stated in the example.

Step 2.

Normalized low-pass filter parameters f_n and Q are obtained from Table I (or from program shown in Table II).

Complex Poles:
$f_n = 1.068853$
$Q = 1.7062$
Simple Pole:
$f_n = 0.626456$

Step 3.

Now, since the actual response desired is high-pass, the low-pass to high-pass transformation must be made as previously discussed in Low-Pass Transformation.

$$f_n \text{ (high-pass)} = \frac{1}{f_n \text{ (low-pass)}}, \quad Q_{HP} = Q_{LP}$$

∴ For Complex Poles:

$$f_n = \frac{1}{1.068853} = 0.935582$$

and Q = 1.7062

For Simple Pole: $f_n = \frac{1}{0.626456} = 1.596281$

Step 4.

Now, determine the actual (denormalized) frequency.
$f_o = f_c \times f_n = 2\text{kHz} \times 0.935582 = 1871.2\text{Hz}$

Step 5.

Refer to the Configuration Selection Guide. Since the gain required is positive, the HP output is not inverted with respect to the input. Therefore, the noninverting input configuration must be selected. Note that the HP output is not available with the Bi-Quad configuration.

Step 6.

Since $f_o < 8\text{kHz}$, Equations "A" would be used.

Step 7.

For the Complex Poles Stage of the filter, using the equations "A".

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{1871.2} = 85.08\text{k}\Omega$$

Step 8.

$f_o Q = 1871.2 \times 1.7062 = 3.19 \times 10^3$

$\therefore f_o Q < 10^5$

$\therefore Q_P = Q = 1.7062$

Step 9.

$A_{BP} = Q_P \times A_{HP} = 1.7062 \times 1 = 1.7062$

$$R_G = \frac{5.0 \times 10^4 \times 1.7062}{1.7062 \times 1.7062} = 29.3\text{k}\Omega$$

$$R_Q = \frac{5.0 \times 10^4}{2 \times 1.7062 - 1.7062 - 1} = 70.8\text{k}\Omega$$

The above obtained resistor values are for the complex pole pair of the first stage of the required active filter. The simple pole obtained as outlined below, using the uncommitted op amp in the UAF41 makes the second stage of the required filter.

For the simple pole f_n was obtained in step 3.

$f_n = 1.596281$

The actual (denormalized) frequency = $f_c \times f_n$

$= 2\text{kHz} \times 1.596281 = 3192.6\text{Hz}$

Now, $f = \frac{1}{2\pi RC}$

$$\therefore RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 3192.6} = 4.9851 \times 10^{-5}$$

Choosing C = 2200pF (or any convenient value),

$$R = \frac{4.9851 \times 10^{-5}}{2200 \times 10^{-12}} = 22.66\text{k}\Omega$$

Note:

R and/or C may be chosen in any convenient manner to obtain the desired RC product.

The overall circuit for the required filter is shown below:

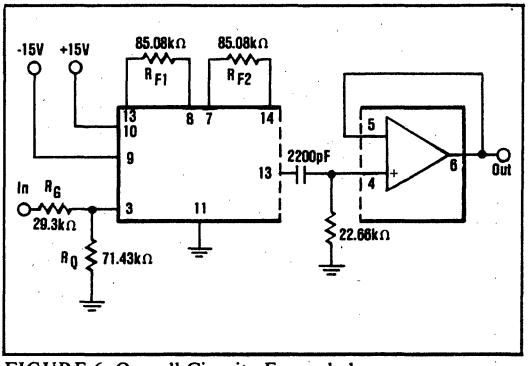


FIGURE 6. Overall Circuit - Example 1.

Example 2.

It is desired to design a 4-pole Butterworth, Bandpass Filter, with Q = 25, f_c = 19kHz and A_{BP} = 1.

Using the computer program shown in Table III, the following values of f_n and Q are obtained.

$$f_n = 1.0142435,\ Q = 35.36541$$

and

$$f_n = 0.9859565,\ Q = 35.35886$$

Using the above shown values of Q and f_n, we now will proceed to design the two stages of filter separately. Composite gain will be ≤1. Any one of the three configurations shown in the Configuration Selection Guide can be used. We will select the noninverting input configuration.

For Stage 1.

$f_o = 19kHz \times f_n = 19kHz \times 1.0142435 = 19270.6Hz$

Since $f_o > 8kHz$, equations "B" would be used.

$$R_{F1} = R_{F2} = \frac{5.033 \times 10^7}{19270.6} = 2.6118k\Omega$$

$f_oQ = 19270.6 \times 35.36541 = 6.815136 \times 10^5$

Since $f_oQ \geq 10^5$, locate the corresponding f_oQ_P from the Performance Curves.

Divide f_oQ_P by f_o to obtain Q_P.

Thus $Q_P = 48.78$

$$R_G = \frac{5.0 \times 10^4 \times 35.36541}{1 \times 48.78} = 36.25k\Omega$$

$$R_Q = \frac{5.0 \times 10^4}{3.48 \times 47.78 - \frac{48.78}{35.37} - 1} = 298.7\Omega$$

For Stage 2.

Following the same procedure as shown for Stage 1 above, the values shown below are obtained.

$f_oQ = 6.624 \times 10^5$, using the Performance Curves;

$Q_P = 48.04$

$R_{F1} = R_{F2} = 2.6867k\Omega$

$R_G = 36.8k\Omega$

and $R_Q = 303.4\Omega$

The overall circuit for the required filter is shown below.

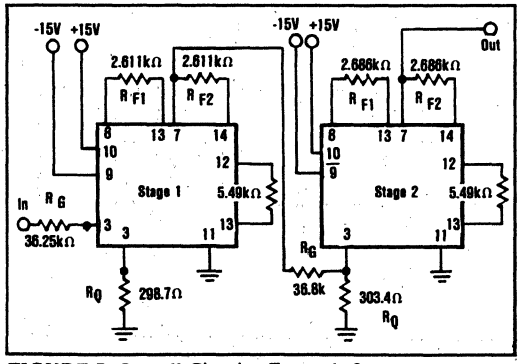


FIGURE 7. Overall Circuit - Example 2.

Example 3.

It is desired to design a 5-pole Bessel, Low-Pass Filter with f_c = 3.3kHz and A_{LP} = 1.

From Table I the following values of f_o and Q are obtained.

Complex Poles:

$f_n = 1.55876$
$Q = 0.56354$

$f_n = 1.75812$
$Q = 0.91652$

Simple Pole:

$f_n = 1.50470$

Using the above shown values of f_n and Q, we now will proceed to design the three stages of filter separately.

Any one of the three configurations can be used. We will select inverting configuration.

For Stage 1.

$f_o = 3.3kHz \times f_n = 3.3kHz \times 1.55876 = 5144Hz$

Since $f_o < 8kHz$, equations "A" would be used.

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{5144} = 30.95k\Omega$$

$f_oQ = 5144 \times 0.56354 = 2.9 \times 10^3$

$f_oQ < 10^5,\ \therefore Q_P = Q = 0.56354$

$A_{BP} = Q_P\ A_{LP} = 0.56354 \times 1 = 0.56354$

$$R_G = \frac{5 \times 10^4 \times 0.56354}{0.56354} = 50k\Omega$$

$$R_Q = \frac{5 \times 10^4}{2 \times 0.56354 + 0.56354 - 1} = 72.4k\Omega$$

For Stage 2.

$f_o = 3.3kHz \times f_n = 3.3kHz \times 1.75812 = 5802Hz$

Since $f_o > 8kHz$, equations "A" would be used.

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{5802} = 27.44k\Omega$$

$f_oQ = 5802 \times 0.91652 = 5.32 \times 10^3$

$f_oQ > 10^5,\ \therefore Q_P = Q = 0.91652$

$A_{BP} = Q_P\ A_{LP} = 0.91652 \times 1 = 0.91652$

$$R_G = \frac{5 \times 10^4 \times 0.91652}{0.91652} = 50k\Omega$$

$$R_Q = \frac{5 \times 10^4}{2 \times 0.91652 + 0.91652 - 1} = 28.58k\Omega$$

For Stage 3.

$f = 3.3kHz \times f_n = 3.3kHz \times 1.50470 = 4966Hz$

For the simple pole,

$$RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 4966} = 3.2049 \times 10^{-5}$$

3300pF (or any convenient value)

$$R = \frac{3.2049 \times 10^{-5}}{3300 \times 10^{-12}} = 9.71k\Omega$$

The overall circuit is shown below.

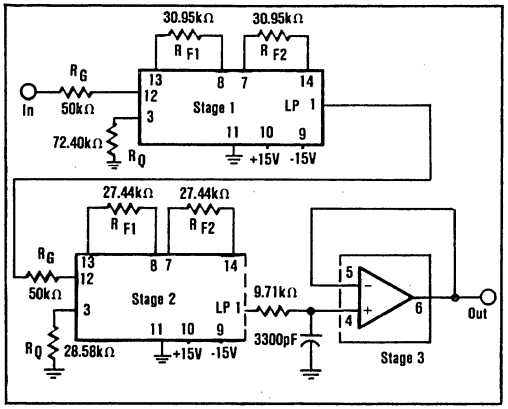


FIGURE 8. Overall Circuit - Example 3.

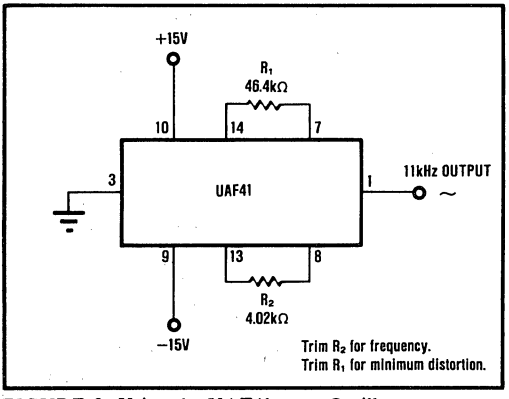


FIGURE 9. Using the UAF41 as an Oscillator.

USEFUL REFERENCES

1. G.E. Tobey, J.G. Graeme and L.P. Huelsman, Operational Amplifiers: Design and Applications, (Chapter 8) McGraw Hill Book Co., 1971.
2. Yu Jen Wong, William E. Ott, Function Circuits: Design and Applications, (Chapter 6) McGraw Hill Book Co., 1976.
3. Richard W. Daniels, Approximation Methods for Electronic Filter Design, McGraw Hill Book Co., 1974.
4. Anatol I. Zverev, Handbook of Filter Synthesis, John Wiley and Sons Inc., New York, N.Y., 1967
5. Gabor C. Temes, Sanjit K. Mitra, Modern Filter Theory and Design, John Wiley and Sons, New York, N.Y., 1973

TABLE III. Low-Pass to Bandpass BASIC Transformation Program.

```
 20  INPUT "FN, Q, AND Q(BANDPASS)";F,Q,QBP
 30  Y=F*SQR(1-(1/(2*Q))^2)
 40  X= -F/(2*Q)
 50  PX=X:PY=Y
 60  FOR I= 1 TO 2
 70  SX=PX/(2*QBP):SY=PY/(2*QBP)
 80  PX=(SX^2-SY^2)-1:PY=2*SX*SY
 90  T=ATN(PY/PX)
 95  T=T-3.1415926#
100  IF T >0 THEN 120
110  T = 2*3.1415926# + T
120  T=T/2
130  A=SQR(SQR(PX^2 + PY^2))*COS(T)
140  B=SQR(SQR(PX^2 + PY^2))*SIN(T)
150  SX=SX+A:SY=SY+B
160  F=SQR(SX^2 +SY^2)
170  Q= -F/(2*SX)
180  PRINT "FN=";F;"Q=";Q
190  IF Y=0 THEN 220
200  PX=X:PY= -Y
210  NEXT I
220  STOP
230  END
```

BURR-BROWN®

4023/25

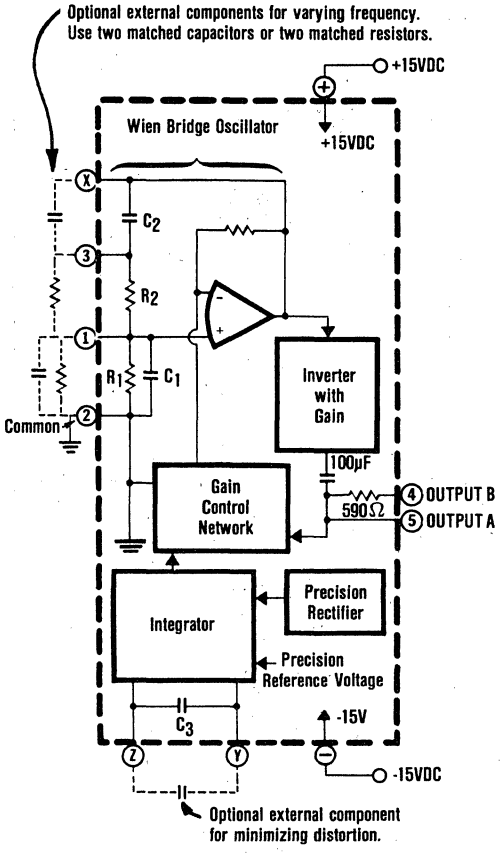
PRECISION OSCILLATOR

FEATURES

- FIXED FREQUENCY - 10Hz to 20kHz
- STABLE AMPLITUDE
- SINE WAVE OUTPUT
- LOW DISTORTION

DESCRIPTION

Model 4023/25 is an all solid-state, ultra-stable sine-wave oscillator. Both output amplitude and frequency are constant, and the stability of both with time and temperature variations is excellent. Internal high-performance Burr-Brown IC operational amplifiers are used to form a Wien bridge oscillator circuit and to regulate the output amplitude. The frequency of oscillation is within ±1% of the customer-specified value. If desired, external components may be added to trim the frequency to an exact value. Adding two external resistors will raise the output frequency and adding two external capacitors will lower the output frequency. With its small size, low distortion, and excellent frequency and amplitude stability, the Model 4023/25 is ideal for use as a reference oscillator in airborne or mobile equipment, special-purpose test equipment, and in telemetry systems. To order, specify Model 4023/25 and frequency.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

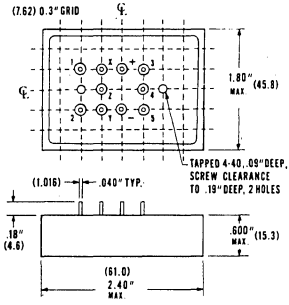
ELECTRICAL SPECIFICATIONS

Typical performance at 25°C and with rated supply unless otherwise noted.

FREQUENCY	
Range (1)	Customer specified, may be any value from 10 Hz to 20 kHz.
Accuracy	±1%, (May be trimmed by the user to less than ±1%)
Stability vs. Temperature	0.04%/°C (max.)
OUTPUT (3)	
Amplitude - Output A	6 Vrms
- Output B	3 Vrms (with 600 Ω load)
Amplitude Accuracy	±2%
Impedance - Output A	1 Ω
- Output B	600 Ω
Rated Load - Output A	1.2 k Ω
- Output B	600 Ω
Distortion (max.)	0.1%
AMPLITUDE STABILITY	
vs. Temperature (max.)	0.02%/°C
Noise and Jitter (max.)	0.02%
Long Term (max.)	0.1%
TEMPERATURE RANGE	
Operating, Rated Specifications	-25°C to +85°C
Storage	-55°C to +100°C
POWER REQUIREMENTS	
Rated Supply	±15 Vdc
Voltage Range at 25°C (2)	±12 Vdc to ±18 Vdc
Supply Drain (max.)	±40 mA

(1) To order, specify Model 4023/25 and frequency.
(2) The positive and negative supplies must be balanced within 2% of each other.
(3) The output may be taken from either Output A or Output B (not both).

MECHANICAL SPECIFICATIONS



Dimensions in millimeters are shown in parentheses.
Weight: 4 oz. maximum (120 grams)
Mating Connector: 1500MC (Optional)

OPERATING INSTRUCTIONS

With $R_1 = R_2$ and $C_1 = C_2$, the Wien-Bridge oscillator will provide a sine-wave oscillation of frequency:

$f_o = 1/2\pi RC$, where $R = R_1 = R_2$ and $C = C_1 = C_2$.

The frequency of oscillation, f_o, will be within ±1% of the nominal value specified by the customer. The frequency may be lowered by externally paralleling the internal capacitors C_1 and C_2; and the frequency may be raised by paralleling the internal resistors R_1 and R_2. The nominal values of C_1 and C_2 will be as follows:

Frequency f_o	C_1 and C_2
10Hz to 100Hz	0.1μF
101Hz to 1000Hz	0.01μF
1001Hz to 20kHz	0.001μF

It is important to pad both R_1 and R_2 or C_1 and C_2 by an equal amount to keep distortion within specifications.

If the frequency is lowered by a significant amount, it may be necessary to externally parallel the integrator capacitor C_3 to lower distortion of the output.

The range of frequency adjustment is approximately 2 decades (within 10kHz and 20kHz). For example, a 10Hz unit may be trimmed for a frequency of up to 1kHz or a 10kHz unit may be varied down to 100Hz. However, the distortion and amplitude stability specifications are guaranteed and tested only for the nominal frequency of oscillation. In general, the degradation in distortion and amplitude stability as the frequency is varied over a wide range is very small.

INSTALLATION

The Model 4023/25 is designed for installation on a flat mounting surface such as a chassis or printed circuit board. The gold-flashed pins may be hand or dip soldered; for plug-in installation, the Model 1500MC mating connector may be installed on the chassis. The unit may be secured to the mounting surface by means of two 4-40 machine screws inserted through the mounting surface not more than 3/16" into the tapped holes in the bottom.

Pin 1 and pin 3 must be shielded from external sources of electrical noise. The module is particularly sensitive to periodic noise near the resonant frequency. Also, if external bridge components are added to the Wien bridge terminals they must be physically near the 4023/25 module.

EXTERNAL CONNECTIONS

External connections are made to the gold-flashed pins on the unit. These connections include the Wien bridge, integrator feedback, output, and power supply termination and are made as follows:

Pin 1	Wien Bridge Terminals
Pin 2 Common	Wien Bridge Terminals
Pin 3	Wien Bridge Terminals
Pin X	
Pin 4	Output B
Pin 5	Output A
Pin Y	Integrator Feedback Terminals
Pin Z	Integrator Feedback Terminals
(+)	Positive Power, +15VDC
(-)	Negative Power, -15VDC

BURR-BROWN®

4085

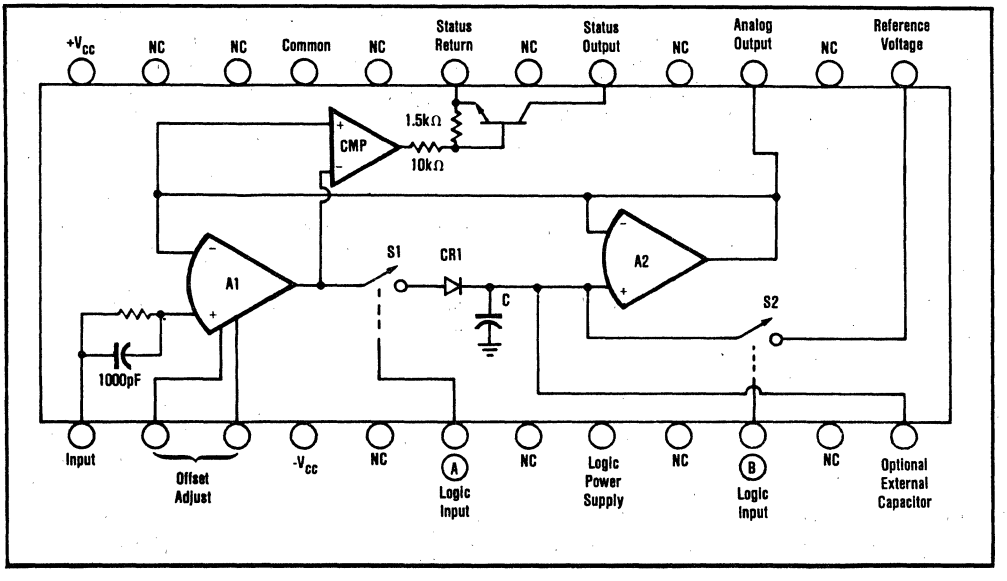
HYBRID MICROCIRCUIT PEAK DETECTOR

FEATURES:

- STORES TRANSIENT VOLTAGES
- COMPLETELY SELF-CONTAINED
- ACCURATE TO ±0.01%
- LOW DROOP ERRORS
- SMALL DIP PACKAGE

DESCRIPTION

The 4085 is a specialized sample/hold amplifier that tracks an input signal until a maximum amplitude is reached. That maximum value is held at the analog output, and the digital Status output indicates that a peak has been detected. The unit can then be commanded to hold that value, ignoring additional peaks, or reset to a user-specified reference voltage. The 4085 detects positive-going peaks from -10V to +10V and is available in a hermetic metal package and a low-cost ceramic package. Three models are available, specified for temperature ranges 0 to +70°C (4085KG), -25°C to +85°C (4085BM), and -55°C to +125°C (4085SM).



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specification at T_A = +25°C and ±15VDC and +5VDC power supplies unless otherwise noted.

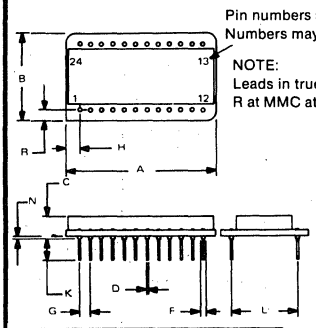
MODEL	4085 MIN	4085 TYP	4085 MAX	UNITS
ANALOG INPUT				
Signal Inputs				
Operating Range	±10	|Vcc|-3		V
Absolute Maximum Range			±Vcc	V
Input Offset Voltage (adjustable to zero)			2	mV
Input Offset Voltage Drift		15	50	µV/°C
Input Bias Current		15	50	pA
Input Resistance		1		GΩ
Input Capacitance		8		pF
DIGITAL INPUT				
Logic Levels				
Logic "1"	+2.4 at 50nA, max			V
Logic "0"			+0.8 at 100µA, max	V
Truth Table	Logic Input A		Logic Input B	
Peak Detect Mode	1		0	
Hold Mode	0		0	
Reset	0		1	
TRANSFER CHARACTERISTICS				
Voltage Gain		1.0		V/V
ACCURACY				
DC Voltage Gain Error			±0.01	% of FSR(1)
Dynamic Accuracy to 300Hz		±0.01	±0.02	% of FSR
Dynamic Accuracy to 100Hz			±0.01	% of FSR
Temperature Coefficient of Gain Error		±3		ppm/°C
Feedthrough			±0.05	% of Step
Droop (all units at T_A = +25°C)(2)			±0.06	mV/msec
T_A = +70°C, 4085KG			±0.5	mV/msec
T_A = +85°C, 4085BM			±1.2	mV/msec
T_A = +125°C, 4085SM			±12.0	mV/msec
Power Supply Sensitivity, ±Vcc			±0.005	%/% Supply Variation
Logic Supply			±0.005	%/% Supply Variation
DYNAMIC PERFORMANCE				
Acquisition Time (BM, SM)			500	µsec
Acquisition Time (KG)			800	µsec
Slew Rate		0.5		V/µsec
Charge Offset(3)		0.5	1	mV
Status Delay at 500Hz		0.7	1	msec
Status Delay at 100Hz		1.2	2	msec

MODEL	4085 MIN	4085 TYP	4085 MAX	UNITS
ANALOG OUTPUT				
Voltage Range	±10	|Vcc|-3		V
Output Current	5			mA
Output Resistance		0.2	0.5	Ω
Output Noise 10Hz to 100kHz		30		µV, rms
Output Load Capacitance	50	100		pF
STATUS OUTPUT				
Collector-emitter Voltage			+30	V
Collector Current			20	mA
DC Current Gain	50	100		mA/mA
V_{BE}		0.65		V
REFERENCE VOLTAGE				
Operating Range	±10	|Vcc|-3		V
Absolute Maximum Range			±Supply	V
Discharge Current(4)	5		30	mA
POWER SUPPLY REQUIREMENTS				
Rated Voltage		±15		V
Operating Range	±8		±18	V
Current Drain (I_{OUT} = 0			±20	mA
Rated Logic Supply Voltage(5)		+5.0 ±0.5		V
Logic Supply Current				
(Logic A & B high		3.0 ±0.3		mA
(Logic A & B = 0V		4.4 ±0.5		mA
TEMPERATURE RANGE				
Specification				
4085KG	0		+70	°C
4085BM	-25		+85	°C
4085SM	-55		+125	°C
Operating				
4085KG	-25		+85	°C
4085BM	-55		+90	°C
4085SM	-55		+125	°C
Storage				
4085KG	-30		+90	°C
4085BM	-60		+100	°C
4085SM	-60		+150	°C

NOTES:

1. FSR = Full Scale Range, 20V for the 4085.
2. Equation for droop: $\text{Droop (mV/msec)} = \dfrac{100\text{pA} \times 2^{\left(\frac{T - 25°C}{11}\right)}}{3300\text{pF} + C_{EXT}\text{ (pF)}}$
3. Charge Offset is the charge transferred from the holding capacitor when the 4085 is switched to the hold mode.
4. Any circuitry connected to the reference pin should be capable of sinking the desired discharge current of the internal 3300pF holding capacitor plus any external capacitor. The discharge current range is the current limit imposed by an internal FET switch. It does not imply that the I_{DSS} of external circuitry must be designed to limit current to this range.
5. Logic Supply, pin 8, may be connected to higher supply voltages for operation with MOS or CMOS logic. Refer to "Operating Instructions".

MECHANICAL



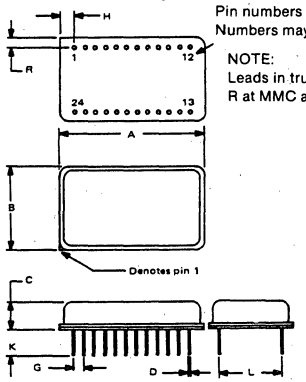
Pin numbers shown for reference only.
Numbers may not be marked on package.

NOTE:
Leads in true position .010" (0.25mm)
R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	002	.010	0.05	0.25
R	085	.105	2.16	2.67

ORDER NUMBER:
4085KG

CASE: Black Ceramic (alumina)
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz)



Pin numbers shown for reference only.
Numbers may not be marked on package.

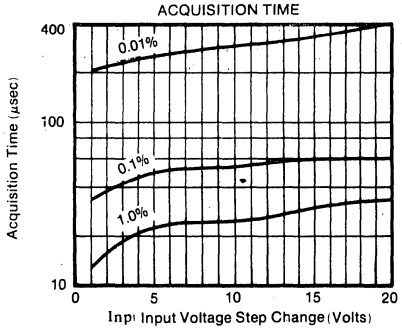
NOTE:
Leads in true position .010" (0.25mm)
R at MMC at seating plane.

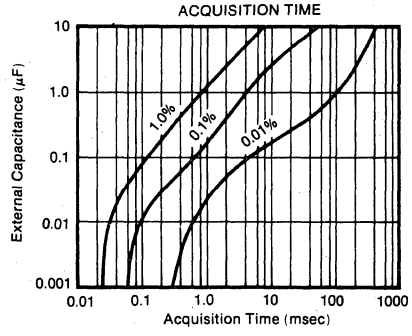
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

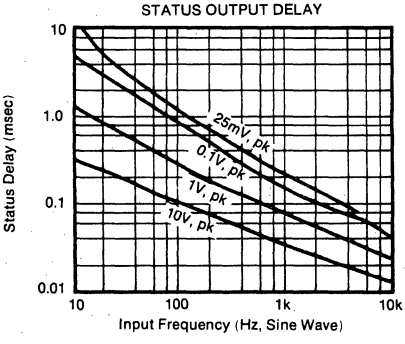
ORDER NUMBER:
4085BM
4085SM

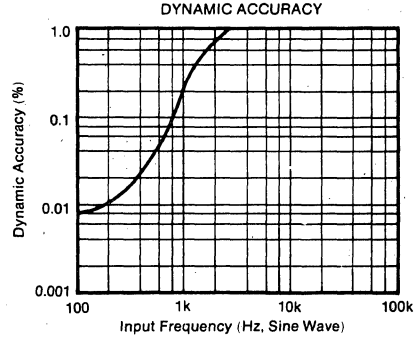
CASE: Kovar, Gold or Nickel plated
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz)

TYPICAL PERFORMANCE CURVES









THEORY OF OPERATION

In the Peak Detect Mode (S1 closed, S2 open), the analog output tracks the analog input until a peak value is reached. When the input voltage falls below the magnitude of the peak voltage, CR1 becomes reversed biased, and the feedback loop between A1 and A2 is broken. At this point, the status output transistor turns on and the magnitude of the peak voltage is held on the analog output. In the Hold Mode (S1 open, S2 open), the current charging path from the output of A1 to the capacitor is opened. The output voltage is equal to the voltage stored in the capacitor even though the input voltage may become larger than the peak voltage. In the Reset Mode (S1 open, S2 open), the voltage on the capacitor will charge to whatever voltage is applied to the reference voltage input. If both S1 and S2 are closed at the same time, the output of A1 will be connected to the reference voltage input through a low impedance. This represents an illegal mode of operation, but will cause no damage to the unit.

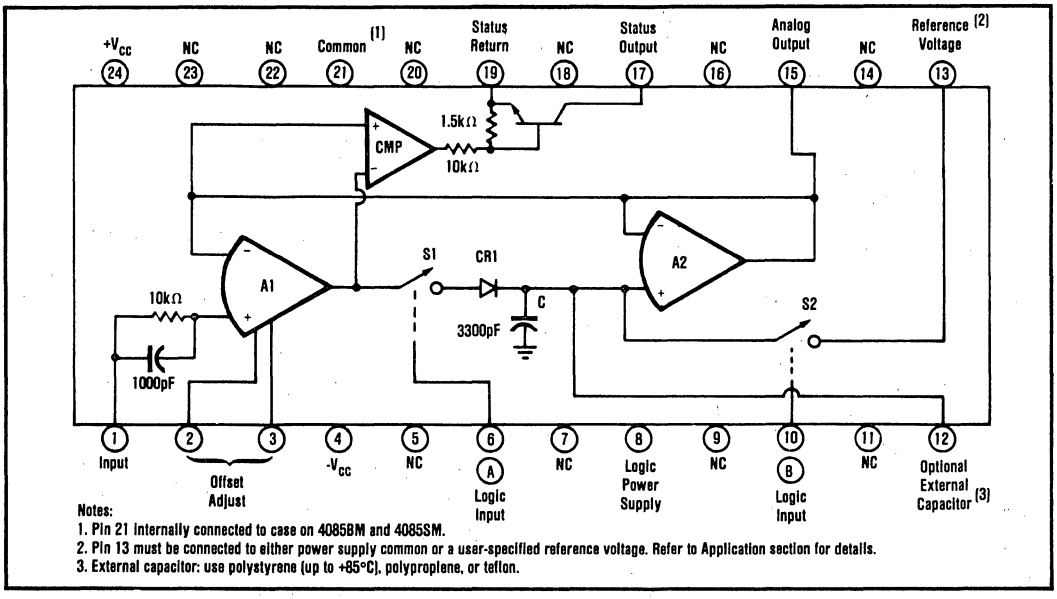


FIGURE 1. 4085 Functional Diagram and Pin Configuration.

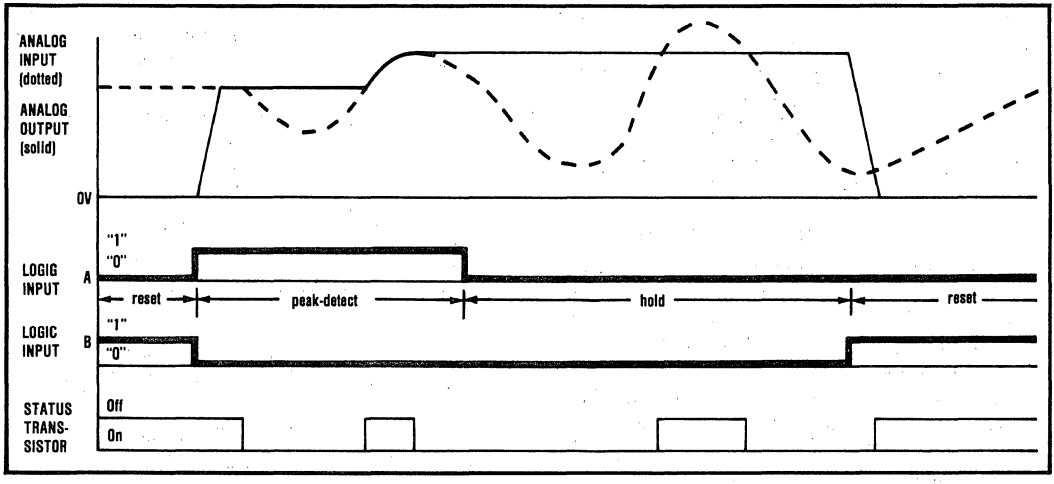


FIGURE 2. Timing Diagram For Peak-Detect Operation.

OPERATING INSTRUCTIONS

OFFSET VOLTAGE ADJUSTMENT

The ±2mV input offset voltage of the 4085 may be nulled to zero by using the circuit shown in Figure 3. With the 4085 in the Peak Detect Mode (logic input A = "1", logic input B = "0") apply zero volts to pin 1. Adjust the potentiometer until the output voltage is zero volts. Disconnect pin 12 after adjustment is made.

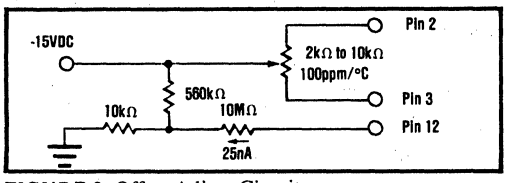


FIGURE 3. Offset Adjust Circuit.

POWER SUPPLY CONSIDERATIONS

The 4085 will operate as specified with power supplies from ±8VDC to ±18VDC. To minimize noise pickup, the supply inputs should be decoupled with 1μF tantalum capacitors located physically close to the unit.

DIGITAL INPUTS AND LOGIC SUPPLY

The digital inputs may be driven with TTL or CMOS logic. Pin 8 should be tied to the logic supply. The logic supply voltage (V_L) may also be provided by connecting pin 8 through a resistor of value R (kΩ) = 1.67 (V_{CC} -V_L)/V_L to the +V_{CC} ($V_{CC} \geq V_L$). The logic threshold voltage is equal to 0.4V_L - 0.7V.

INPUT FREQUENCY BANDWIDTH LIMITING

It is recommended that the input bandwidth be limited as much as possible by an RC section such as that shown in Figure 4. This is to limit noise spikes at the input that may cause erroneous readings. If detecting large pulse heights, a 5μsec time constant should be used. This will not degrade acquisition time or tracking accuracy for frequencies up to 500Hz. For input frequencies greater than 500Hz, a smaller time constant may be used.

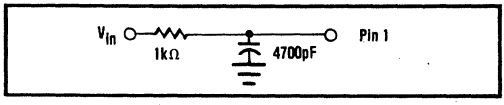


FIGURE 4. Input Bandwidth Limiting.

STATUS OUTPUT CHARACTERISTICS

The open-collector, open-emitter output transistor is a small signal, medium speed switching transistor similar to a 2N2222. To facilitate driving a variety of devices, the configuration of the status output has been left to the user's discretion.

The internal comparator shown in the block diagram (Figure 1) has an output characteristic as follows. Input signal track: $Z_{out} \approx \infty$; peak hold: V_{out} = +V_{CC} - 0.5V.

Several configurations are illustrated in Figures 5, 6, and 7. "Inverting" means logic "0" = peak has been detected. "Noninverting" means logic "1" = peak has been detected.

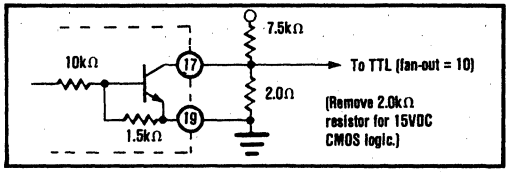


FIGURE 5. Inverting TTL (CMOS) Status Output.

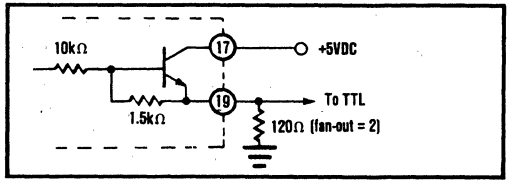


FIGURE 6. Noninverting TTL Status Output.

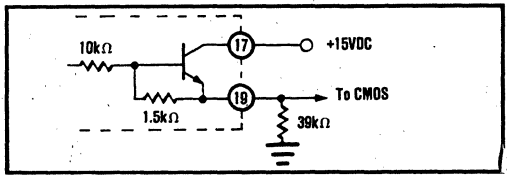


FIGURE 7. Noninverting CMOS Status Output.

DESIGNING IN HYSTERESIS

It may be desirable in some situations to have hysteresis in the circuit such that small peaks will not be detected, eliminating jitter in the Status output. This is possible through external components connected as shown in Figure 8. After a peak is detected, the input voltage must be slightly greater (determined by R1/R2) than the previous peak to cause the output to resume tracking the input. This hysteresis voltage is expressed by:

$$V_H = \frac{(V_{in} - V_E - 0.9V)\,R1}{R1 + R2}$$

The emitter voltage of the status transistor should be tied to a voltage sufficiently lower than the lowest expected peak to allow proper operation.

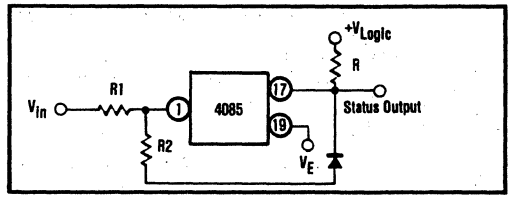


FIGURE 8. Hysteresis.

APPLICATIONS

PEAK CATCHER

This circuit detects and holds the first peak it encounters. After the first peak is detected, it automatically is switched to the Hold Mode. To reset the circuit for catching another peak, a 10μsec or longer positive logic pulse should occur at the Release Input. This will reset the peak detector to the desired voltage and put it in the peak-detect mode.

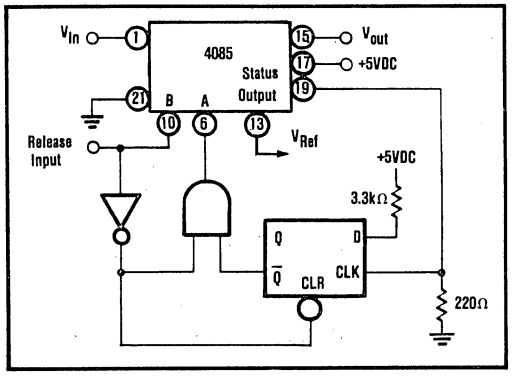


FIGURE 9. Peak Catcher.

NO-RIPPLE, FAST-SETTLING RMS-DC CONVERTER

If a waveform is known, the rms value of the signal may be computed from the peak value. In this circuit, the rms value is computed by the output amplifier from the peak value held by the 4085. The output in the circuit shown is updated manually. It may be updated automatically by replacing the switch circuit with an oscillator plus timing logic.

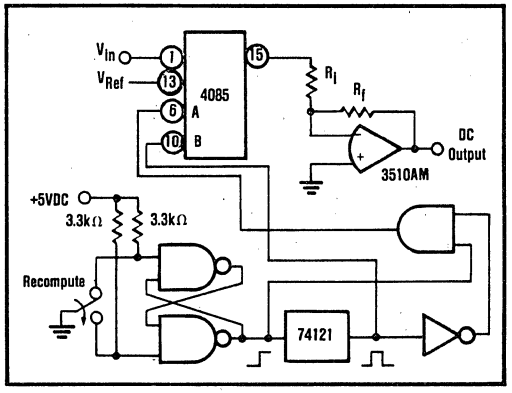


FIGURE 10. RMS-DC Converter.

INTERFACING TO A/D CONVERTER

Interfacing to an A/D converter is straightforward. The gating of the A/D converter command allows a conversion only if a peak has been detected and permits completion of each conversion. If a peak occurs while the A/D is converting, it will not be detected.

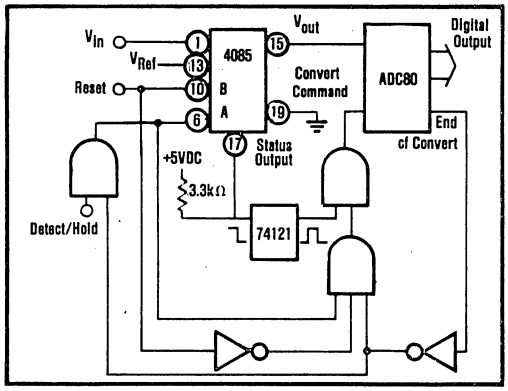


FIGURE 11. A/D Converter Interface.

PEAK-TO-PEAK DETECTOR

Figure 12 shows a circuit that will display the peak-to-peak voltage of an input waveform. The Status Output indicates that both positive and negative peaks have been detected and that the output is valid. The resistors around A3 should be matched to insure good common-mode rejection.

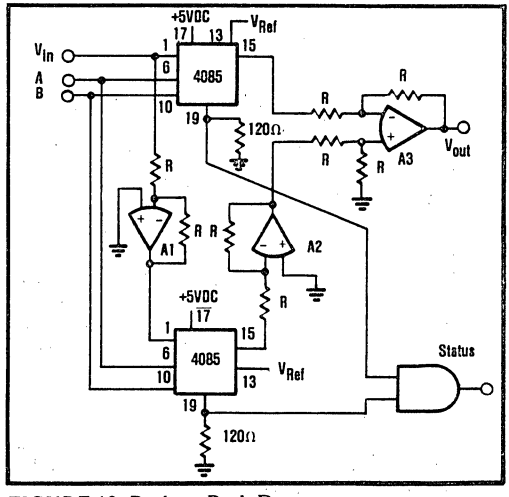


FIGURE 12. Peak-to-Peak Detector.

REFERENCE VOLTAGE

In the Reset Mode the voltage applied to pin 13 places an initial charge on the holding capacitor at the input to A2 (see Figure 1). This threshold voltage may be any value between positive and negative 10 volts. For most applications pin 13 will be tied to power supply common. This sets V_{Ref} to 0 volts. The 4085 will then capture peaks greater than 0 volts.

Pin 13 must be connected to either power supply common or to a user-specified reference voltage. If this connection is not made the 4085 will appear to have excessive droop.

BURR-BROWN®

4115/04

WINDOW COMPARATOR

FEATURES

- ADJUSTABLE LIMITS FOR "HIGH", "LOW", AND "GO"
- UP TO 200mA LOAD CAPABILITY (each output)
- INPUT PROTECTION

APPLICATIONS

- PRODUCTION LINE TESTING
- TEMPERATURE CONTROLS
- INDUSTRIAL ALARMS
- LEVEL DETECTORS/CONTROLS

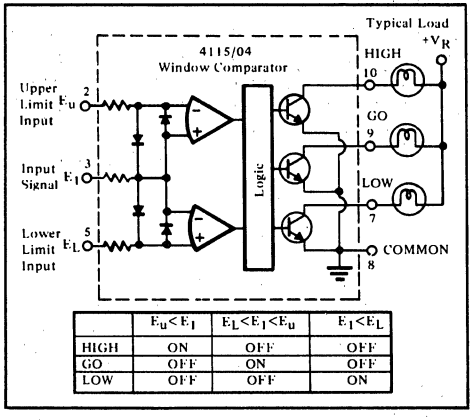
DESCRIPTION

Model 4115/04 is a hybrid IC window comparator in a double width DIP. The unit has three inputs - one for a voltage that sets the upper limit, another for a voltage that sets the lower limit, and a signal input. There are three mutually exclusive outputs - HIGH, LOW and GO. When an output is ON it will sink up to 200mA of current. This input diode protected device is designed to work with input voltages of up to ±10V, and will not be harmed by voltages to ±15V. The 4115/04 will drive a variety of loads including lamps, relays, MOS circuitry, and high noise immunity logic as well as DTL and TTL devices.

INSTALLATION

Separate connections should be made from each power supply common (+15VDC, -15VDC and V_R) to the 4115/04 common (pin 8).

To avoid unwanted pickup or chattering it may be necessary to include bypass capacitors from the ±15V supply pins (13 and 14) to the module common pin (8).



	$E_u < E_I$	$E_L < E_I < E_u$	$E_I < E_L$
HIGH	ON	OFF	OFF
GO	OFF	ON	OFF
LOW	OFF	OFF	ON

Model 4115/04 Transfer Characteristics.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

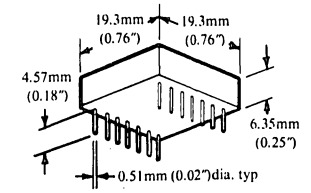
ELECTRICAL SPECIFICATIONS

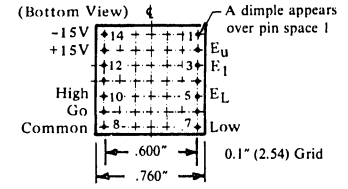
Typical performance at 25°C and with rated supply unless otherwise noted.

MODEL	4115 04	Units
INPUT		
All Inputs	±10V into 6kΩ (min)	
Maximum Safe Input	±15	V
ACCURACY		
D.C. Resolution (min)	±0.2	mV
Voltage Offset (referred to input)		
at 25°C (max)	±2	mV
vs Temperature (max)	±30	μV °C
Over Temperature Range (max)	±7	mV
vs Power Supply	±50	μV V
Switching Speed		
Total Switching Time at 30mV Overdrive	300	μsec
OUTPUT		
Impedance to COMMON from all Outputs		
OFF state	> 1	MΩ
ON state	3	Ω
Load Supply Voltage (V_R)	0 to +30	V
Load Current		
Steady State	+200	mA
Transient (absolute maximum)		
1 Second Duration	+400	mA
Saturation Voltage (V_{CE}) (max)		
at 200mA	0.7	V
TEMPERATURE RANGE		
Rated Specifications	-25 to +85	°C
Derated Performance	-40 to +85	°C
Storage	-55 to +100	°C
POWER SUPPLY REQUIREMENTS		
Rated Supply Voltage	±15	VDC
Derated Performance	-12 to ±18	VDC
Quiescent Drain (max)	±15	mA

To achieve best results use stable quiet reference sources and drive signal input from low impedance source. Noise and drift in input sources readily masks the inherently high resolution of the device.

MECHANICAL SPECIFICATIONS





WEIGHT: 0.24 oz. (6.80 grams)
MATERIAL: Black Exoxy
PIN: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
CONNECTOR: Fits any commercial dual-in-line connector.

BURR-BROWN ®

4127

LOGARITHMIC AMPLIFIER

FEATURES

- **ACCEPTS INPUT VOLTAGES OR CURRENTS OF EITHER POLARITY**
- **WIDE INPUT DYNAMIC RANGE**
  - **6 Decades of current**
  - **4 Decades of voltage**
- **VERSATILE**
  - **Log, antilog, and log ratio capability**
- **SMALL SIZE**
  - **Double wide DIP**
- **LOW COST**

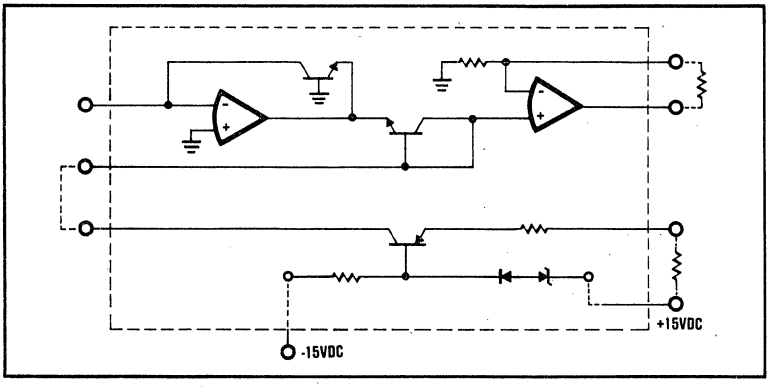
DESCRIPTION

Packaged in a ceramic double wide DIP, the 4127 is the first hybrid logarithmic amplifier that accepts signals of either polarity from current or voltage sources. A special purpose monolithic chip, developed specifically for logarithmic conversions, functions accurately for up to six decades of input current and four decades of input voltage. In addition, a newly developed current inverter and a precise internal reference allow pin programming of the 4127 as a logarithmic, log ratio, or antilog amplifier.

To further increase its versatility and reduce your system cost, the 4127 has an uncommitted operational amplifier in its package that can be used as a buffer, inverter, filter, or gain element.

The 4127 is available with initial accuracies (log conformity) of 0.5% and 1.0%, and operates over an ambient temperature range of -10°C to +70°C.

With its versatility and high performance, the 4127 has many applications in signal compression, transducer linearization, and phototube buffering. Manufacturers of medical equipment, analytical instruments, and process control instrumentation will find the 4127 a low cost solution to many signal processing problems.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

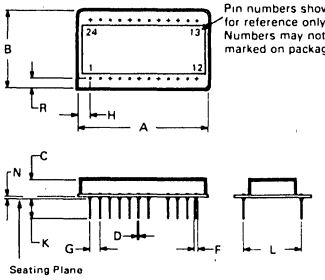
ELECTRICAL

Typical specifications at +25°C with rated supplies unless otherwise noted.

MODEL	4127KG	4127JG
ACCURACY(1), % of FSR		
Current Source Input: 1nA to 1mA	0.5% max	1% max
Voltage Input: 1mV to 10V	0.5% max	1% max
INPUT		
Current Source Input, Pin 4	+1nA to +1mA	
Current Source Input, Pin 7	-1nA to -1mA	
Reference Current Input, Pin 2	+1μA to +1mA	
Absolute Maximum Inputs	±10mA or ±Supply Volts	
OUTPUT		
Voltage	±10V	
Current	±5mA	
Impedance	10Ω	
FREQUENCY RESPONSE		
-3dB Small Signal at Current Input		
of 100μA	90kHz	
of 10μA	50kHz	
of 1μA	5kHz	
of 100nA	250Hz	
of 10nA	80Hz	
Step Response to within ±1% of		
Final Value (I_R = 1μA, A = 5)	10msec	
STABILITY		
Scale Factor Drift (ΔA/°C)	±0.0005A/°C	
Reference Current Drift (ΔI_R/°C)	±0.001 I_R/°C for $I_R \geq$ 1μA	
	±0.003 I_R/°C for 400nA < I_R < 1μA	
Input Offset Current Drift (ΔI_S/°C)	10pA at +25°C, Doubles Every 10°C	
Input Offset Voltage Drift	±10μV/°C	
Accuracy vs. Supply Variation		
Reference Current	±0.001I_R/V	
Input Offset Voltage	±300μV/V	
Input Noise - Current Input	1pA, rms, 10Hz to 10kHz	
Input Noise - Voltage Input	10μV, rms, 10Hz to 10kHz	
UNCOMMITTED OP AMP CHARACTERISTICS		
Input Offset Voltage	5mV	
Input Bias Current	40nA	
Input Impedance	1MΩ	
Large Signal Voltage Gain	85dB	
Output Current	5mA	
TEMPERATURE RANGE		
Specification	0°C to +60°C	
Operating	-10°C to +70°C	
Storage	-55°C to +125°C	
POWER SUPPLY REQUIREMENTS		
Rated Supply Voltages	±15VDC	
Supply Voltage Range	±14VDC to ±16VDC	
Supply Current Drain		
at Quiescent, max	±20mA	
at Full Load, max	±26mA	

NOTE:
1. Log conformity at 25°C.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

CASE: Ceramic
MATING CONNECTOR: 245MC
WEIGHT: 56 grams (2 oz.)
ORDER NUMBER: 4127KG
4127JG

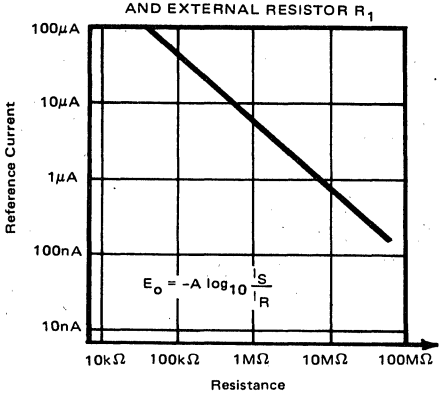
PIN CONNECTIONS

1. I_{REF} OUTPUT
2. I_{REF} INPUT
3. NO PIN PRESENT
4. +I INPUT *
5. CURRENT INVERTER OUTPUT *
6. NO PIN PRESENT
7. CURRENT INVERTER INPUT
8. NO PIN PRESENT
9. OP AMP +INPUT
10. OP AMP -INPUT
11. OP AMP OUTPUT
12. NO PIN PRESENT
13. MAKE NO CONNECTION
14. NEGATIVE SUPPLY
15. NO PIN PRESENT
16. NO PIN PRESENT
17. NO PIN PRESENT
18. LOG OUTPUT
19. GAIN ADJUST
20. NO PIN PRESENT
21. COMMON
22. POSITIVE SUPPLY
23. I_{REF} BIAS
24. NO PIN PRESENT

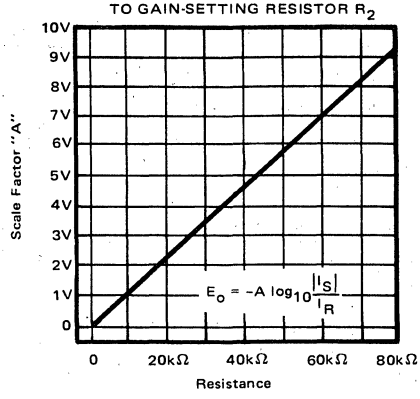
*Pins 4 and 5 are internally connected.

TYPICAL PERFORMANCE CURVES

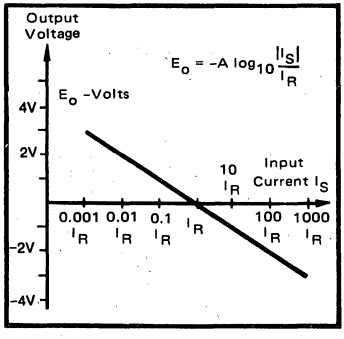
RELATIONSHIP OF REFERENCE CURRENT I_R AND EXTERNAL RESISTOR R_1



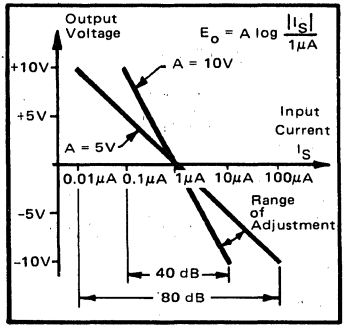
RELATIONSHIP OF SCALE FACTOR "A" TO GAIN-SETTING RESISTOR R_2



LOG RELATIONSHIP OF $\frac{|I_S|}{I_R}$ AND OUTPUT VOLTAGE IN TERMS OF "A"



RELATIONSHIP OF $\frac{|I_S|}{I_R}$ TO OUTPUT VOLTAGE FOR I_R = 1μA AND A = 5V AND 10V



DISCUSSION OF SPECIFICATIONS

ACCURACY

The deviation from the ideal output voltage defined as a percent of the full scale output voltage.

INPUT/OUTPUT RANGE

The log relationships of $-A \log \frac{I_S}{I_R}$ and $-A \log \frac{E_S}{I_R R}$ are subject to the constraints specified. The 4127 can be operated with inputs lower than those given, but the accuracy will be degraded.

FREQUENCY RESPONSE

The small-signal frequency response varies considerably with signal level and scaling, so the frequency response is specified under several different operating conditions.

STABILITY

The use of a monolithic transistor quad and low-drift op amps minimizes drift, but some drift remains in the scale-factor, reference current, and input offset. Input offset consists of a bias current plus the op amp input voltage offset divided by the signal source resistance. Also, there is some slight drift in conformity to the log function and in output amplifier offset, but this is generally negligible.

THEORY OF OPERATION

The 4127 is a complete logarithmic amplifier that can be pin-programmed to accept input currents or voltages of either polarity. By making use of the internal current inverter, reference current generator, log ratio element, and uncommitted op amp, you can generate a variety of logarithmic functions, including the log ratio of two signals, the logarithm of an input signal, or the antilog of an input signal. The unique FET-input current-inverting element removes the polarity limitations present in most conventional log amplifiers.

Utilizing the inherent exponential characteristics of transistor functions, the 4127 calculates accurate log functions for input currents from 1nA to 1mA, or input voltages from 1mV to 10V. Carefully matched monolithic quad transistors and temperature sensitive gain elements are used to produce a log amplifier with excellent temperature characteristics.

A functional diagram of the 4127 circuit is shown in Figure 1. In addition to the basic log amplifier, the 4127 contains a separate internal current source, a current inverter, and an uncommitted operational amplifier. The current inverter accurately converts negative input current to a positive current of equal magnitude.

The 4127 is capable of accurately logging input current over a 120dB range but to use this full range, good shielding practice must be followed. A current source input is, by definition, a high impedance source and is therefore subject to electrostatic pickups.

The input op amps A_1 and A_3 have FET input stages for low noise and very-low input bias current. The op amp A_1 will make the collector current of Q_1 equal to the signal input current I_S, and the collector current of Q_2 will be the reference input current I_R.

From the semiconductor junction characteristics, the base-to-emitter voltage will be

$$V_{BE} \approx \frac{m\,K\,T}{q} \ln \frac{I_C}{I_L}, \text{ where } I_C = \text{Collector current}$$

I_L = Reverse saturation current
q, m, K = Constants
T = Absolute temperature

$$\text{So } E_1 = -\frac{m\,K\,T_1}{q} \ln \frac{I_S}{I_{L1}} \quad \text{and } E_2 - E_1 = \frac{m\,K\,T_2}{q} \ln \frac{I_R}{I_{L2}}$$

If the transistors Q_1 and Q_2 are at the same temperature and have matched characteristics then

$$E_2 = \frac{m\,K\,T}{q}\left[\ln \frac{I_R}{I_L} - \ln \frac{I_S}{I_L}\right]$$

$$E_2 = \frac{-m\,K\,T}{q} \ln \frac{I_S}{I_R}$$

The output op amp A_2 provides a voltage gain of approximately $(R_T + R_2)/R_T$, and the value of $(mKT)/q$ is about 26mV at room temperature. Since resistor R_T varies with temperature to compensate for gain drift, the output voltage E_o expressed as a log will be

$$E_o = -A \log_{10} \frac{I_S}{I_R}$$

$$\text{where } A \approx \frac{R_T + R_2}{R_T}\,(26\text{ mV})\frac{1}{0.434}, \quad R_T \approx 520\Omega$$

The external resistor R_1 sets the reference current I_R and resistor R_2 sets the scale-factor "A". R_1 and R_2 must be trimmed to the desired values, but the approximate relationships are shown in Typical Performance Curves.

The relationship between the input current I_S and the output voltage E_o in terms of the externally adjusted parameters I_R and "A" is illustrated in Typical Performance Curves. This relationship is, of course, restricted to values of I_S between 1nA and 1mA and output voltages of less than ±10V.

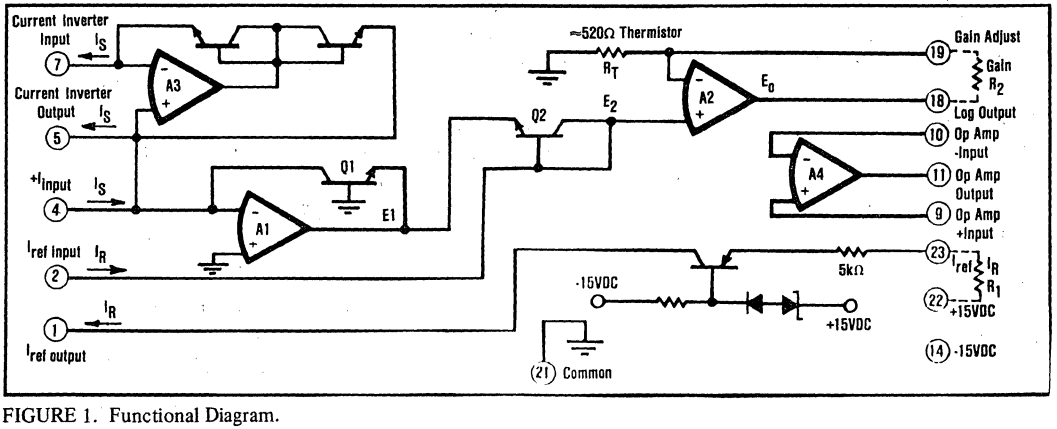


FIGURE 1. Functional Diagram.

CHOOSING THE OPTIMUM SCALE FACTOR AND REFERENCE CURRENT

To minimize the effects of output offset and noise, it is usually best to use the full ±10V output range. Once an output range of ±10V has been chosen, then "A" and I_R can be determined from the min/max of the input current I_S.

$$E_o = -A \log \frac{I_S}{I_R}, \text{ where } I_{min} < I_S < I_{max}$$

The output range of ±10V for an input range of I_{min} to I_{max} means that

$$+10 = -A \log \frac{I_{min}}{I_R} \text{ and } -10 = -A \log \frac{I_{max}}{I_R}$$

Adding these two equations together

$$\log \frac{I_{max} I_{min}}{I_R^2} = 0, \text{ or } I_R = \sqrt{I_{max} I_{min}}$$

The value for A can be found from:

$$10 = A \log \frac{I_{max}}{\sqrt{I_{max} I_{min}}}$$

In terms of the input current range for I_S, the values for I_R and A that will provide a full ±10V output swing are:

$$I_R = \sqrt{I_{max} I_{min}} \text{ and } A = \frac{10}{\log \frac{I_{max}}{I_R}}$$

Example: Assume that I_{min} is +10nA and I_{max} is +100μA.

This is an 80dB range.

$$I_R = \sqrt{I_{max} I_{min}} = \sqrt{(10^{-4})\ (10^{-8})} = 10^{-6}, \text{ or } 1\mu A.$$

$$\frac{I_{max}}{I_R} = \frac{10^{-4}}{10^{-6}} = 100$$

$$\log \frac{I_{max}}{I_R} = 2 \quad \text{So } A = 5$$

For an I_R of 1μA and A of 5,

$$E_o = -5 \log \frac{I_S}{1\mu A}$$

CONNECTION DIAGRAMS

Transfer function is $E_o = -A \log \frac{I_1}{I_R}$ where I_1 is a positive input current and I_R is the resistor-programmed internal reference current (see Figure 2).

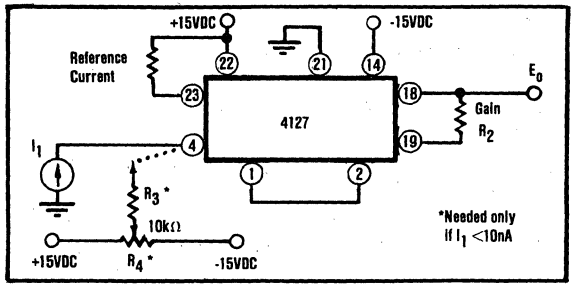


FIGURE 2. Transfer Function When I_1 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. Apply $I_1 = I_R$, adjust R_1 such that $E_o = 0$.
3. Apply $I_1 = I_{max}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $I_{1min} \geq$ 10nA. Otherwise, apply I_1 = 1nA, make R_3 = 1kMΩ* and adjust R_4 for the proper output voltage.

Transfer function is $E_o = -A \log \frac{|I_1|}{I_R}$ where I_1 is a negative input current and I_R is the resistor-programmed internal reference current (see Figure 3).

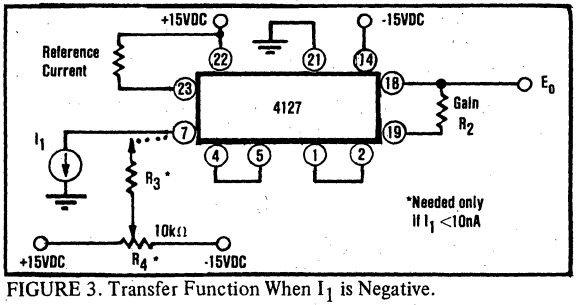


FIGURE 3. Transfer Function When I_1 is Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. Apply $|I_1| = I_R$ adjust R_1 such that $E_o = 0$.
3. Apply $|I_1| = I_{max}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $|I_{1min}| \geq$ 10nA. Otherwise, apply $|I_1|$ = 1nA, make R_3 = 1kMΩ* and adjust R_4 for the proper output voltage.

*Single resistor recommended. Voltage divider network difficult to use due to amplifier offset voltage. RF500-108, 1GΩ resistor available from Burr-Brown.

CONNECTION DIAGRAMS [CONT]

Transfer function is $E_0 = -A \log \frac{E_1}{R_4 I_R}$, where E_1 is a positive input voltage and I_R is the resistor-programmed internal reference current (see Figure 4).

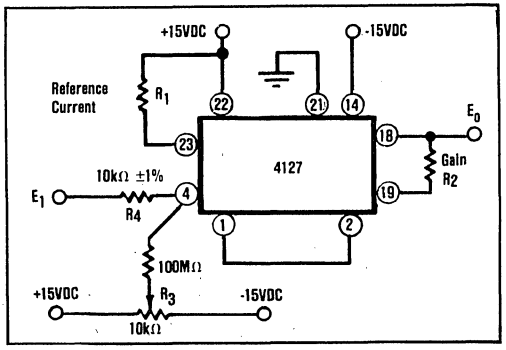


FIGURE 4. Transfer Function When E_1 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. Apply $E_1 = I_R$ (10kΩ), adjust R_1 such that $E_0 = 0$.
3. Apply $E_1 = E_{max}$, adjust R_2 for the proper output voltage.
4. Apply $E_1 = E_{min}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_0 = -A \log \frac{|E_1|}{R_4 I_R}$, where E_1 is a negative input voltage and I_R is the resistor-programmed internal reference current (see Figure 5).

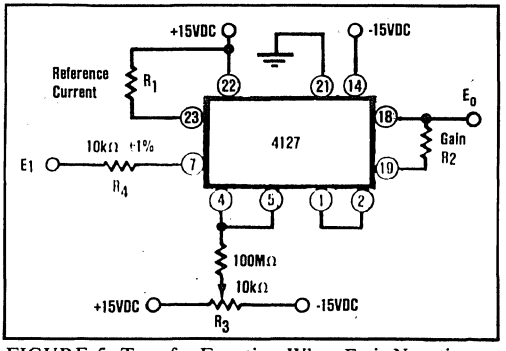


FIGURE 5. Transfer Function When E_1 is Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. Apply $|E_1| = I_R$ (10kΩ), adjust R_1 such that $E_0 = 0$.
3. Apply $|E_1| = E_{max}$, adjust R_2 for the proper output voltage.
4. Apply $|E_1| = E_{min}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_0 = -A \log \frac{|I_1|}{|I_2|}$ with I_1 and I_2 negative; $|I_1| \geq 1nA, |I_2| \geq 1\mu A$ (see Figure 6).

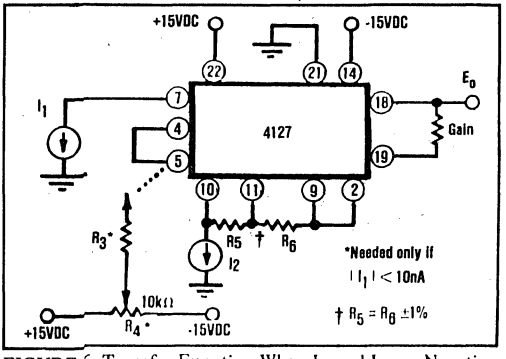


FIGURE 6. Transfer Function When I_1 and I_2 are Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if I_1 min $\geq$ 10nA, otherwise connect the R_3 and R_4 network, with R_4 = 10kΩ and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of ±5mV, it is not practical to use a T - network to replace R_3.

Transfer function is $E_0 = -A \log \frac{|I_1|}{I_2}$ with I_1 negative, I_2 positive; $|I_1| \geq 1nA$, $I_2 \geq 1\mu A$ (see Figure 7).

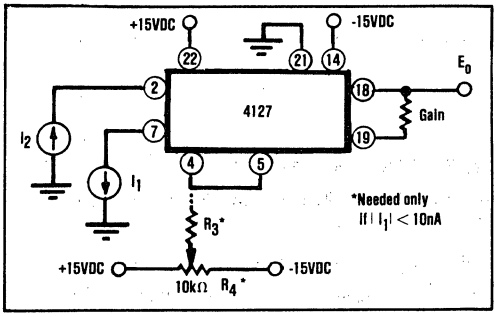


FIGURE 7. Transfer Function When I_1 is Negative, I_2 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if $|I_1|$min $\geq$ 10nA, otherwise connect the R_3 and R_4 network, with $R_4 = 10k\Omega$ and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm$5mV, it is not practical to use a T - network to replace R_3.

Transfer function is $E_0 = -A \log \frac{I_1}{I_2}$ with I_1 and I_2 positive; $I_1 \geq 1nA$, $I_2 \geq 1\mu A$ (see Figure 8).

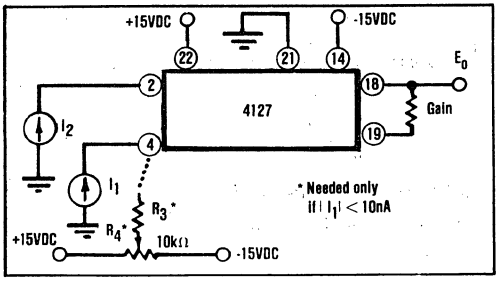


FIGURE 8. Transfer Function When I_1 and I_2 are Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if I_1 min $\geq$ 10nA, otherwise connect the R_3 and R_4 network, with $R_4 = 10k\Omega$ and $R_3 = 10^9\Omega$. Adjust R4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm$5mV, it is not practical to use a T - network to replace R_3.

ANTILOG OPERATION

The 4127 can also perform the antilog function. The output is connected through a resistor R_0 into the current input, pin 4. The input signal is connected through a gain resistor to pin 19 as shown in Figure 9.

These connections form an implicit loop for computing the antilog function. From the block diagram of Figure 1, the voltage at the inverting input of the output amplifier A2 must equal E_2, so

$$E_2 \approx \frac{R_T}{R_T + R_2} E_S, \quad R_T \approx 520\Omega$$

Since the output is connected through R_0 to pin 4, the current I_S will equal E_0/R_0 and E_2 will be

$$E_2 = -\frac{m K T}{q} \ln \frac{E_0}{R_0 I_R}$$

Combining expressions for E_2 gives the relationship

$$\frac{R_T}{R_T + R_2} E_S = -\frac{m K T}{q} \ln \frac{E_0}{R_0 I_R}$$

$$-\frac{E_S}{A} = \log \frac{E_0}{R_0 I_R}$$

where

$$A \approx \frac{R_T + R_2}{R_T} (26mV) \frac{1}{0.434}$$

$$E_0 = R_0 I_R \text{ Antilog} - \frac{E_S}{A}$$

Setting R_0 and I_R will set the scale factor. For example, an R_0 of 1MΩ and I_R of 1μA will give a scale factor of unity and

$$E_0 = \text{Antilog} - \frac{E_S}{A}$$

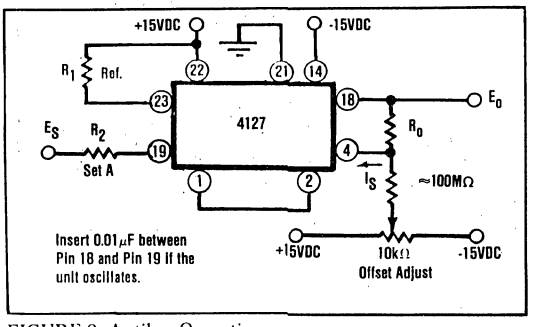


FIGURE 9. Antilog Operation.

BURR-BROWN®

4203
4205

Integrated Circuit
MULTIPLIER-DIVIDERS

FEATURES

- LASER-TRIMMED
  Requires No Adjustment
- GUARANTEED ACCURACY - 1% or 2%
- SELF-CONTAINED
  No Additional Amplifiers
- FAST SLEWING - 25V/μsec
- SMALL PACKAGE - TO-100

APPLICATIONS

- MULTIPLICATION, DIVISION, SQUARING, SQUARE ROOTS
- RMS MEASUREMENTS
- FREQUENCY DOUBLER
- BALANCED MODULATOR AND DEMODULATOR
- ELECTRONIC GAIN CONTROL
- FUNCTION GENERATOR AND LINEARIZING CIRCUITS
- PROCESS CONTROL SYSTEMS

DESCRIPTION

Burr-Brown Models 4203 and 4205 are integrated circuit multipliers designed for general purpose usage. In addition to four-quadrant multiplication they also perform division and square rooting of analog signals, requiring no additional amplifiers in performing the above functions. They are laser-trimmed prior to final packaging and are guaranteed to their rated accuracy with no external components. This is a distinct advantage from the standpoints of cost and reliability.

These multipliers contain their own zener-regulated references and, as a result, are much less sensitive to supply voltage variation than were earlier IC multipliers. The fast (25V/μsec) slew rate and 1MHz bandwidth are key performance factors for applications where delay phase shift must be minimized. Harmonic distortion of the 4203 and 4205 remain low for frequencies well above 100kHz, an important asset in modulation applications.

Other desirable features are hermetic TO-100 package (10-pin version of TO-99) and wide temperature range of operation. The 4203S and 4205S are specified for operation over the full MIL temperature range.

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SPECIFICATIONS

ELECTRICAL

Typical at +25°C with rated power supplies unless otherwise noted.
Percent specifications refer to % of full scale (10V).

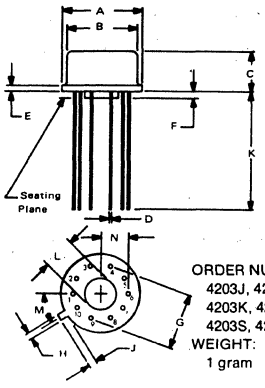
MODEL	4203J/4205J	4203K/4205K	4203S/4205S
OUTPUT FUNCTION 4203	XY/10		
4205	$(X_1 - X_2)(Y_1 - Y_2)/10$		
TOTAL ERROR*			
Internal Trim	2%, max	1%, max	1%, max
External Trim	1%	0.6%	0.6%
vs Temperature		0.04%/°C	
vs Supply		0.2%/%	
INDIVIDUAL ERRORS			
Output Offset at +25°C (X = Y = 0)	20mV	20mV	20mV, max
vs Temperature (Operating Range)		0.4mV/°C	
vs Supply		10mV/%	
Scale Factor Error	1%	0.6%	0.6%
vs Temperature (Operating Range)		0.04%/°C	
vs Supply		0.1%/%	
Nonlinearity			
X (X = 20V, p-p; Y = ±10VDC)	0.8%	0.5%	0.5%
Y (Y = 20V, p-p; X = ±10VDC)		0.2%	
Feedthrough at 50Hz			
X = 0, Y = 20V, p-p (Internal Trim)		50mV, p-p	
(External Trim)		20mV, p-p	
vs Temperature		1mV, p-p/°C	
Y = 0, X = 20V, p-p (Internal Trim)		50mV, p-p	
(External Trim)		20mV, p-p	
vs Temperature		2mV, p-p/°C	
AC PERFORMANCE			
Slew Rate		25V/μsec	
-3dB Small Signal Bandwidth		1MHz	
1% Amplitude Error		40kHz	
1% Vector Error (0.57° phase shift)		10kHz	
Settling Time (2% of final value, 20V, step)		1μsec	
Overload Recovery Time		3μsec	
OUTPUT NOISE (X = Y = 0)			
10kHz to 10MHz		3mV, rms	
10Hz to 10kHz		600μV, rms	
INPUT CHARACTERISTICS			
Input Voltage Range			
Rated Operation		±10V	
Absolute Max		±15V	
Input Impedance, X		10MΩ	
Y		10MΩ	
Z		36kΩ	
OUTPUT CHARACTERISTICS			
Rated Output		±10V at ±5mA	
Output Impedance		1Ω	
POWER SUPPLY REQUIREMENTS			
Rated Voltage		±15VDC	
Operating Range		±12VDC to ±18VDC	
Quiescent Current		±4.5mA	
TEMPERATURE RANGE			
Operating, Rated Performance	0°C to +70°C		-55°C to +125°C
Storage	-65°C to +150°C		

*Total error is a tested maximum at .25°C and represents the maximum allowed value for the sum of the individual errors.

MECHANICAL

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

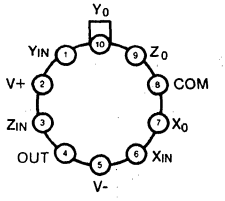
Pin numbers shown for reference only.
Numbers may not be marked on package.



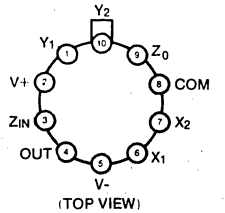
ORDER NUMBER:
4203J, 4205J
4203K, 4205K
4203S, 4205S
WEIGHT:
1 gram

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

CONNECTION DIAGRAM



(TOP VIEW)
4203



(TOP VIEW)
4205

BURR-BROWN®

4204
4206

ANALOG MULTIPLIER-DIVIDER

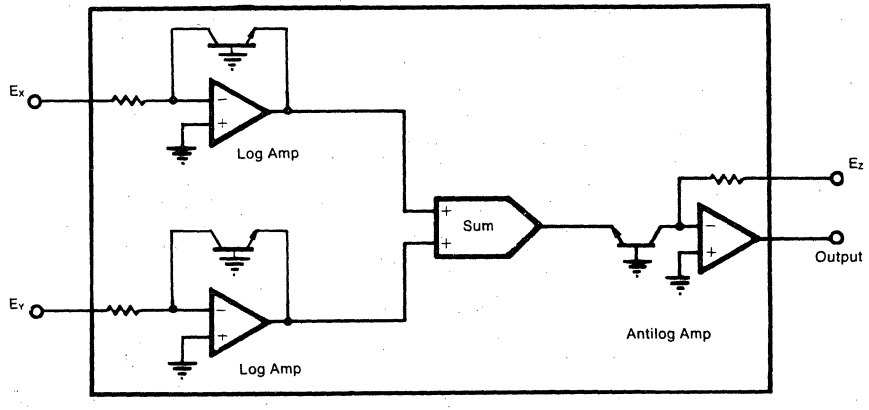
FEATURES

- HIGH TOTAL ACCURACY
  0.25% and 0.5% max, no external trims
  0.1% and 0.2% typ. with external trims
- LOW TEMPERATURE DRIFT
  100ppm/°C
- SMALL PACKAGE
  Dual-in-line metal or plastic
- LOW COST

DESCRIPTION

The 4204 and 4206 are four-quadrant analog multipliers offering high accuracy, low noise, and moderate bandwidth at low cost. They use the log/antilog technique and are internally laser-trimmed. Multiply mode accuracies of 0.25% and 0.5% max are guaranteed with no external components. By following the external trim procedure described in the Multiplication section, accuracies can be improved to 0.1% and 0.2% (typical). Accuracy specifications are verified at Burr-Brown by an automatic tester which scans the X-Y plane. Maximum error at any point in the plane is required to be less than the specified values.

The 4204 and 4206 also perform the divide function in two quadrants and the square root function in one quadrant with no external components required. Detailed instructions for these operations are given on the last page.



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SPECIFICATIONS

ELECTRICAL

Typical performance at +25°C with rated power supplies unless otherwise noted. Percent specifications refer to percent of full scale (10V)

MODEL	4204J, 4206J	4204K, 4206K	4204S
OUTPUT FUNCTION	E_X E_Y / 10	*	*
TOTAL ERROR (Multiply Mode)[1]			
Internal trim, max[2]	0.5% max	0.25% max	*
External trim, typ	0.2%	0.1%	0.1%
vs Temperature	0.01%/°C	*	0.02%/°C max
vs Supply	0.02%/%	*	*
INDIVIDUAL ERRORS (Multiply Mode)			
Output Offset X = Y = 0	15mV	5mV	5mV
Scale Factor Error	0.2%	0.1%	0.1%
Nonlinearity:			
X = 20V, p-p, Y = −10VDC	0.005%	*	*
Y = 20V, p-p, X = −10VDC	0.005%	*	*
X = 20V, p-p, Y = +10VDC	0.05%	*	*
X = 20V, p-p, X = +10VDC	0.05%		*
Feedthrough at 50Hz:			
X = 20V, p-p, Y = 0	10mV, p-p		5mV, p-p
Y = 20V, p-p, X = 0	10mV, p-p		5mV, p-p
AC PERFORMANCE			
Slew Rate	1V/μs	*	*
−3dB Small Signal Bandwidth	250kHz	*	*
1% Amplitude Error	33kHz	*	*
1% Vector Error (0.57° phase shift)	2.5kHz	*	*
Full Power Response	20kHz	*	*
OUTPUT NOISE X = Y = 0.0V			
DC to 10kHz	300μV, rms	*	*
INPUT CHARACTERISTICS			
Input Voltage:			
Maximum for Rated Specifications X, Y, Z	±10V	*	*
Maximum Safe Level X, Y, Z	±Supply	*	*
Input Impedance X/Y/Z	25kΩ/25kΩ/100kΩ	*	*
OUTPUT CHARACTERISTICS			
Rated Output: Voltage, min	±10V	*	*
Current, min	±5mA	*	*
Output Impedance	1Ω	*	*
POWER SUPPLY REQUIREMENTS			
Rated Supply	±15VDC	*	*
Operating Range	±14 to ±16V	*	*
Quiescent Current	+15mA, −8.5mA	*	*
TEMPERATURE RANGE, 4206			
Specification	0°C to +70°C	*	
Operating	−25°C to +85°C	*	
Storage	−55°C to +125°C	*	
TEMPERATURE RANGE, 4204			
Specification	−25°C to +85°C	*	−55°C to +125°C
Operating	−55°C to +125°C	*	*
Storage	−65°C to +125°C	*	*

*Same as for 4206J.

NOTES: (1) Total error is a tested maximum and does not represent a sum of the maximum individual errors as the maximum individual errors do not occur at the same X, Y operating point. (2) With output loading of 10kΩ or less.

PIN CONNECTIONS 4204

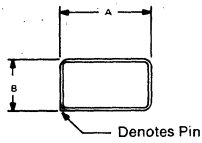
1 E_Z
2 Output
3 $-V_S$
4 Feedthrough Adjust
5 Make No Connection
6 Make No Connection
7 E_X
8 Internal Reference
9 Make No Connection
10 Ground
11 Feedthrough Adjust
12 Offset Adjust
13 E_Y
14 $+V_S$

PIN CONNECTIONS 4206

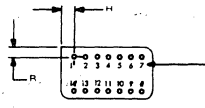
1 E_Z
2 Output
3 $-V_S$
4 Feedthrough Adjust
5 Make No Connection
6 Make No Connection
7 E_X
8 Internal Reference
9 Make No Connection
10 Ground
11 Feedthrough Adjust
12 Offset Adjust
13 E_Y
14 $+V_S$

MECHANICAL

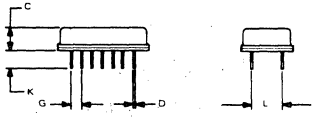
4204



NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

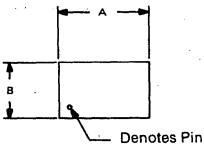


Pin numbers shown for reference only. Numbers are not marked on package.

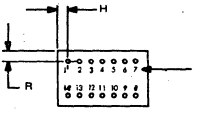


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

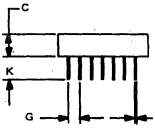
4206



NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

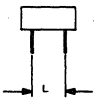


Pin numbers shown for reference only. Numbers are not marked on package.



PIN SPACING: 2.5mm (0.1")
ROW SPACING: 7.6mm (0.300")
WEIGHT: 3.4 grams (0.12 oz.)
CONNECTOR: 14-pin DIP 0145MC

Pin material and plating composition conform to Method 208 (solderability) of MIL-STD-202.

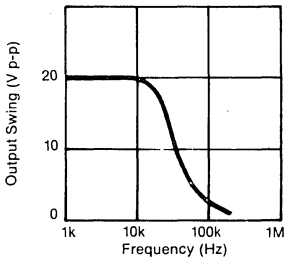


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.210	4.83	5.33
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

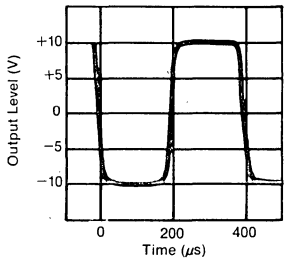
TYPICAL PERFORMANCE CURVES

At +25°C and ±15VDC.

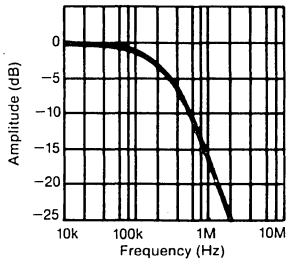
LARGE SIGNAL FREQUENCY RESPONSE



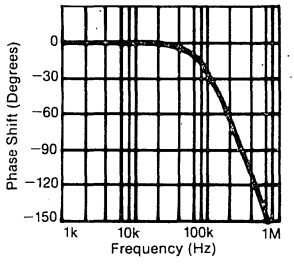
STEP RESPONSE



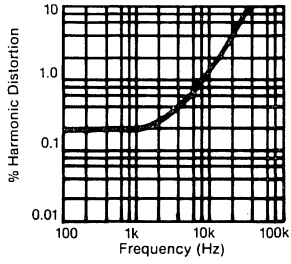
SMALL SIGNAL FREQUENCY RESPONSE



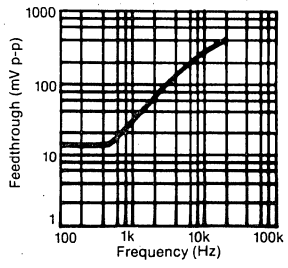
SMALL SIGNAL FREQUENCY RESPONSE



OUTPUT DISTORTION VS FREQUENCY



AC FEEDTHROUGH VS FREQUENCY



DISCUSSION OF PERFORMANCE CURVES

LARGE SIGNAL FREQUENCY RESPONSE

This response curve describes the output voltage capability of the 4204 and 4206 as a function of frequency. The measurement is made with one input at +10 or −10VDC, and with a sine wave applied at the other input. An output distortion of 0.5% is allowed.

STEP RESPONSE

Step response is measured with one input at +10 or −10VDC and with a 20Vp-p square wave applied at the other input.

SMALL SIGNAL FREQUENCY RESPONSE

These curves are the amplitude and phase response of the 4204 and 4206's transfer function, when one input is held at +10 or −10VDC. A sine wave signal is applied to the other input. Small signal response requires that the amplitude of the input sine wave be adjusted so that the output signal does not reach the slew rate limitation.

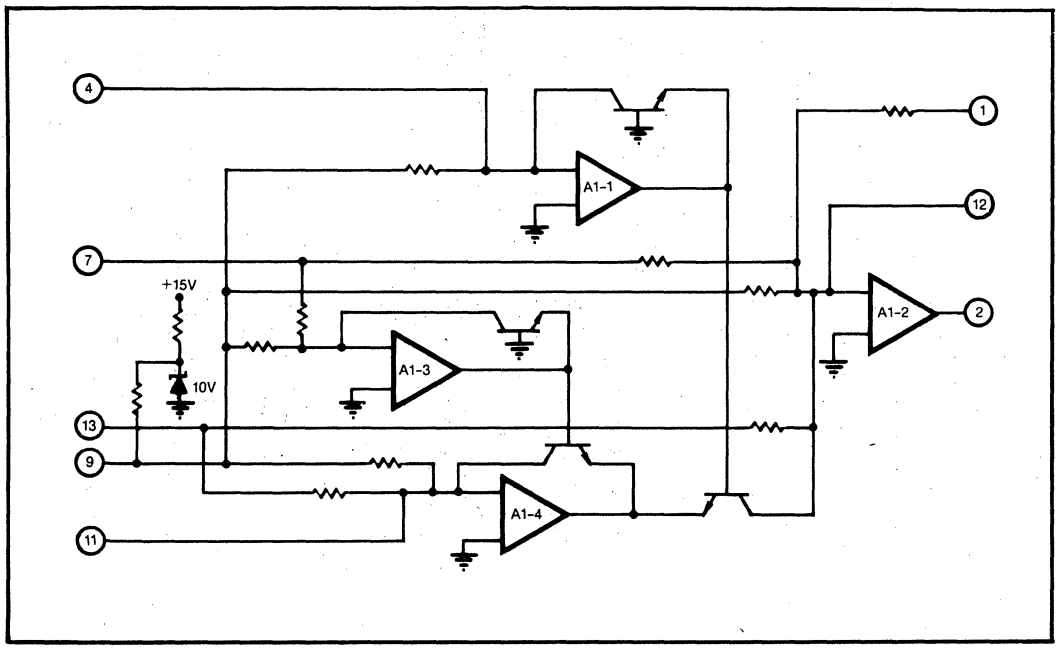
OUTPUT DISTORTION

The output distortion of the 4204 and 4206 is of most interest in modulator applications. The curve for Output Distortion characterizes this distortion with one input held at +10 or −10VDC. A sine wave is applied to the other input. The sine wave amplitude is held constant at 20Vp-p while frequency is varied.

AC FEEDTHROUGH

This variation of feedthrough as a function of frequency is illustrated in the curve above. One of the inputs is a zero while a 20Vp-p sine wave is applied at the other input. The output feedthrough generally has substantial harmonic content and is measured in millivolts, peak-to-peak.

THEORY OF OPERATION

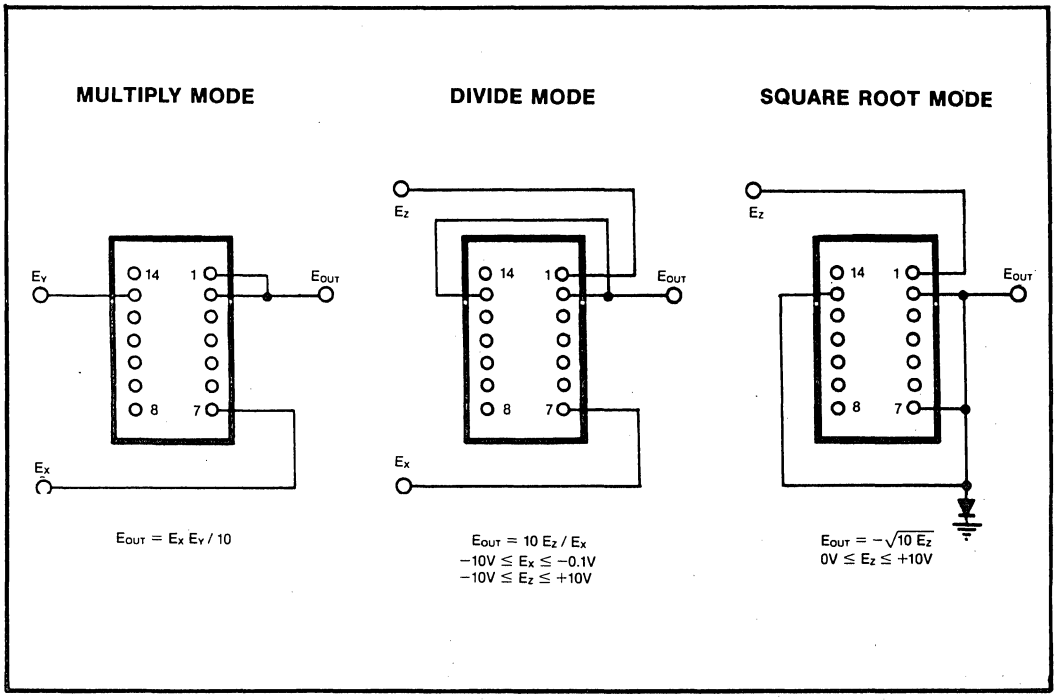


These products' log-antilog multiplication technique is based upon the logarithmic voltage-current relationship in a semiconductor junction. This action is shown by the simplified equation:

$$V_{BE} = (KT/q)\,(\ln I_C - \ln I_S)$$

where V_{BE} is the transistor's emitter-base voltage, I_C is the transistor collector current, I_S is the collector saturation current, K is Bolzmann's constant, q is the charge of one electron and T is the absolute temperature in degrees Kelvin. As can be seen from the equation, the logarithmic function is extremely temperature sensitive. The 4204 and 4206, however, have excellent temperature characteristics because the log and antilog circuitry have equal and opposite temperature drifts which cancel to a first order approximation. The log and antilog circuits will compensate each other to the extent that the various logging transistors are matched to each other. These transistors are placed adjacently on a monolithic chip to obtain the best possible matching, and so the best possible performance.

OPERATING MODES



ADJUSTMENTS

Although the products will achieve specified performance in the multiply mode with no external trimming, optimized performance can be achieved with external adjustments. The proper connections and the trim procedures are explained below.

The 4204 and 4206 will operate within specification with any combination of input signals. The best performance, however, will be obtained in the second, third, and fourth quadrants. That is, if four quadrant operations are not needed, the performance can be optimized by constraining operation to quadrants 2, 3 and 4 rather than 1.

MULTIPLICATION

Multiplication Trim Procedure (Figure 1)

1) Set $E_X = 0$ and apply a 10Vp-p sine wave (50Hz) to E_Y: Adjust R_1 for minimum output.
2) Set $E_Y = 0$ and apply a 10Vp-p sine wave (50Hz) to E_X: Adjust R_2 for minimum output.
3) Set $E_X = E_Y = 0$: Adjust R_3 for $E_{OUT} = 0.00V$.
4) Set $E_X = E_Y = +10.000V \pm 1mV$: Adjust R_4 for $E_{OUT} = +10.000V \pm 2mV$.

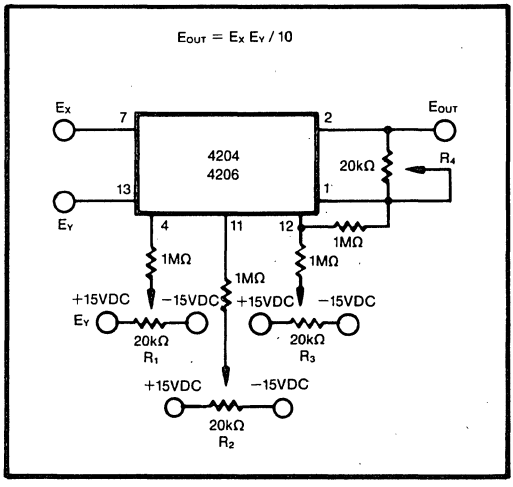


FIGURE 1. Multiplication Trim Procedure.

DIVISION

The 4204 and 4206 may be used as a two-quadrant divider without the need for an external operational amplifier. It should, however, be noted that the maximum output error is approximately given by

$$\text{divider error} \approx 10\varepsilon_M / E_X$$

where ε_M is the total error specification for the multiply mode. Obviously, divider error becomes excessively large for small values of E_X. A 10:1 denominator range is usually the practical limit. If accurate division is required over a wide dynamic range of denominator voltage, the Burr-Brown Model DIV100 is recommended (0.25% max., over a 40:1 range).

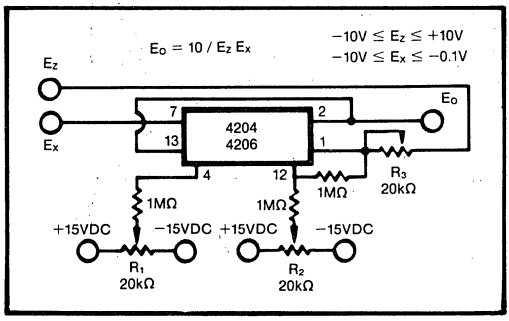


FIGURE 2. Division Trim Procedure.

Division Trim Procedure (Figure 2)

1) Set all potentiometers near mid-scale.
2) Set $E_Z = 0V$, $E_X \approx -10V$, adjust R_2 such that $E_O = 0.000V \pm 2mV$.
3) Set $E_X = E_Z = -10.000VDC \pm 2mV$, adjust R_3 such that $E_O = +10.000VDC \pm 2mV$.
4) Set $E_X = E_Z \approx$ minimum value required by application, adjust R_1 such that $E_O = +10.000VDC \pm 5mV$.
5) Repeat steps 2 through 4 if necessary.

SQUARE ROOT

The pin connections for the Square Root mode of operation are similar to those for division, except that the denominator input is connected to the output node. Errors in the Square root mode of operation become troublesome for small values of E_Z. However, the output error does not increase so rapidly as in the divide mode. The actual output for small values of E_Z is given approximately by

$$E_{OUT} \approx -\sqrt{10\,E_Z + 10\,\varepsilon_M}$$

where ε_M is the total error specifed for Multiply mode. This equation can be used to determine the feasibility of using either of these products as a square rooter for a given application. For operation over a much wider dynamic range, with improved accuracy, the Model 4302 multifunction converter is recommended.

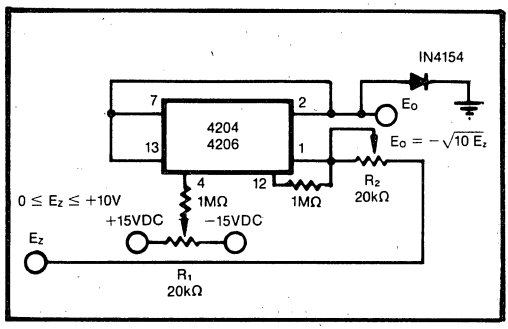


FIGURE 3. Square Root Trim Procedure.

Square Root Trim Procedure (Figure 3)

1) Set $E_Z = +10.000VDC \pm 2mV$, adjust R_2 such that $E_O = +10.000VDC \pm 2mV$.
2) Set $E_Z \approx$ minimum value required by application (E_{ZM}), adjust R_1 such that $E_O = -\sqrt{10\,E_{ZM}} \pm 2mV$.
3) Repeat steps 1 and 2 if necessary.

BURR-BROWN®

4213

For a /883B version of this product, see 4213/883B in the Military Products section.

MULTIPLIER-DIVIDER

FEATURES

- LOW COST
- DIFFERENTIAL INPUT
- ACCURACY 100% TESTED AND GUARANTEED
- LOW NOISE
  120μV, rms, 10Hz to 10kHz
- SELF-CONTAINED
  No additional amplifiers
- SMALL SIZE
  Hermetic TO-100 package
- WIDE TEMPERATURE OPERATION

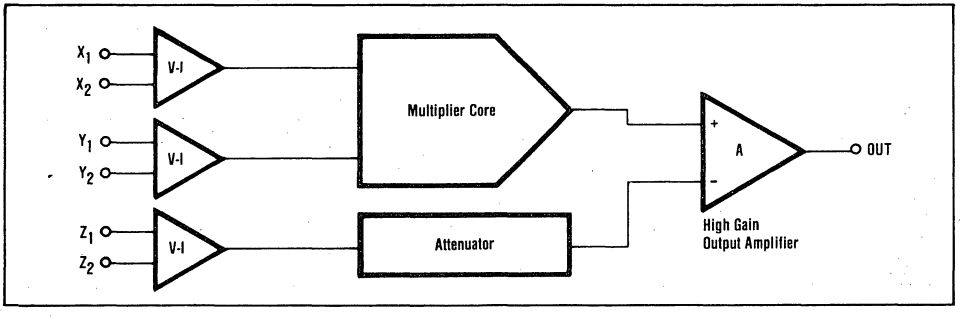
APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOT
- LINEARIZATION
- POWER COMPUTATION
- ANALOG SIGNAL PROCESSING
- ALGEBRAIC COMPUTATION
- TRUE RMS-TO-DC CONVERSION

DESCRIPTION

The 4213 multiplier-divider is a low cost precision device designed for general purpose application. In addition to four-quadrant multiplication, it also performs analog square root and division without the bother of external amplifiers. The 4213 is laser-trimmed to guarantee its rated accuracy with no external components. The internal zener regulated references make the 4213 much less sensitive to supply variation than earlier IC multipliers. Hermetic TO-100 package, wide operating temperature range, low output noise, and low cost are some of the desirable features of this versatile device.

4213 FUNCTIONAL DIAGRAM



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SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

MODEL		4213AM			4213BM			4213SM			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
MULTIPLIER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$			•			•		
Total Error	-10V ≤ X, Y ≤ 10V										
Initial	T_A = +25°C			±1.0			±0.5			±0.5	% FSR
vs Temperature	-25°C ≤ T_A ≤ +85°C		±0.008	±0.02		•	•		--	--	% FSR/°C
vs Temperature	-55°C ≤ T_A ≤ +125°C		--	--		--	--		±0.025	±0.05	% FSR/°C
vs Supply			±0.05			•			•		% FSR/%
Individual Errors											
Output Offset											
Initial	T_A = +25°C		±10	±50		±7	±25		±7	±25	mV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±0.7	±2.0		±0.3	±0.7		--	--	mV/°C
vs Temperature	-55°C ≤ T_A ≤ +125°C		--	--		--	--		±0.3	±0.7	mV/°C
vs Supply			±0.25			•			•		mV/%
Scale Factor Error											
Initial	T_A = +25°C		±0.12			•			•		% FSR
vs Temperature	-25°C ≤ T_A ≤ +85°C		±0.008			•			--		% FSR/°C
vs Temperature	-55°C ≤ T_A ≤ +125°C		--			--			±0.008		% FSR/°C
vs Supply			±0.05			•			•		% FSR/%
Nonlinearity											
X Input	X = 20V, p-p; Y = ±10VDC		±0.08			•			•		% FSR
Y Input	Y = 20V, p-p; X = ±10VDC		±0.01			•			•		% FSR
Feedthrough	f = 50Hz										
X Input	X = 20V, p-p; Y = 0		30			•			•		mV, p-p
Y Input	Y = 20V, p-p; X = 0		6			•			•		mV, p-p
vs Temperature	-25°C ≤ T_A ≤ +85°C		0.1			•			--		mV, p-p/°C
vs Temperature	-55°C ≤ T_A ≤ +125°C		--			--			0.1		mV, p-p/°C
vs Supply			0.15			•			•		mV, p-p/%
DIVIDER PERFORMANCE											
Transfer Function	$X_1 > X_2$		$\frac{10(Z_1 - Z_2)}{X_1 - X_2} + Y_2$			•			•		
Total Error with external adjustments	X = -10V										
	-10V ≤ Z ≤ +10V, X ≠ -1V		±0.75			±0.35			±0.35		% FSR
	-1V ≤ Z ≤ +1V, -10V ≤ X ≤ -0.2V		±2.0			±1.0			±1.0		% FSR
	-10V ≤ Z ≤ +10V		±5.0			±1.0			±1.0		% FSR
SQUARER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)^2}{10} + Z_2$			•			•		
Total Error	-10V ≤ X ≤ +10V		±0.6			±0.3			±0.3		% FSR
SQUARE-ROOTER PERFORMANCE											
Transfer Function	$Z_1 < Z_2$		$+\sqrt{10(Z_2 - Z_1)}$			•			•		
Total Error	1V ≤ Z ≤ 10V		±1			±0.5			±0.5		% FSR
AC PERFORMANCE											
Small-Signal Bandwidth	±3dB		550			•			•		kHz
1% Amplitude Error	Small Signal		70			•			•		kHz
1% 0.57° Vector Error	Small Signal		5			•			•		kHz
Full Power Bandwidth	$\|V_O\|$ = 10V, R_L = 2kΩ		320			•			•		kHz
Slew Rate	$\|V_O\|$ = 10V, R_L = 2kΩ		20			•			•		V/μsec
Settling Time	ε = ±1%, ΔVo = 20V		2			•			•		μsec
Overload Recovery	50% Output Overload		0.2			•			•		μsec
INPUT CHARACTERISTICS											
Input Voltage Range											
Rated Operation		±10			•			•			V
Absolute Maximum				±Vcc			•			•	V
Input Resistance	X, Y, Z(1)		10			•			•		MΩ
Input Bias Current	X, Y, Z		1.4			•			•		μA
OUTPUT CHARACTERISTICS											
Rated Output											
Voltage	I_O = ±5mA	±10			•			•			V
Current	V_O = ±10V	±5			•			•			mA
Output Resistance	f = DC		1.5			•			•		Ω
OUTPUT NOISE VOLTAGE	X = Y = 0										
f_O = 1Hz			40			•			•		$\mu V/\sqrt{Hz}$
f_O = 10kHz			1.0			•			•		$\mu V/\sqrt{Hz}$
1/f Corner Frequency			1060			•			•		Hz
f_B = 10Hz to 10kHz			125			•			•		μV, rms
f_B = 10Hz to 10MHz			3			•			•		mV, rms
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			•			•		VDC
Operating Range	Derated Performance	±8.5		±20	•		•	•		•	VDC
Quiescent Current			±5.5			•			•		mA

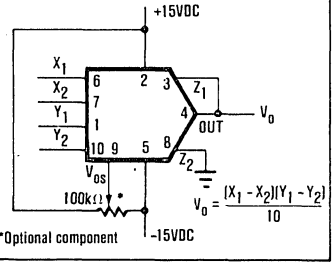
ELECTRICAL (CONT)

MODEL		4213AM			4213BM			4213SM			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TEMPERATURE RANGE (Ambient)											
Specification	Derated Performance	-25		+85	*		*	-55		+125	°C
Operating Range		-55		+125	*		*	*		*	°C
Storage		-65		+150	*		*	*		*	°C

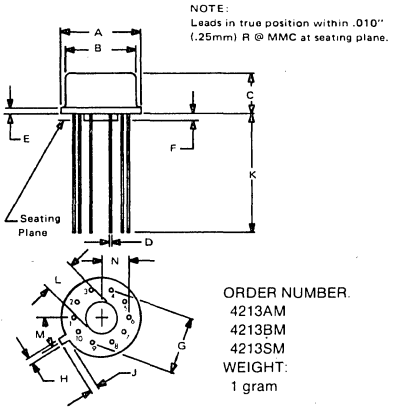
NOTES:
1. Z_2 input resistance is 10MΩ, typical, with Pin 9 open. If Pin 9 is grounded or used for optional offset adjustment, the Z_2 input resistance may be as low as 25kΩ.

*Same as 4213AM specification.

CONNECTION DIAGRAM



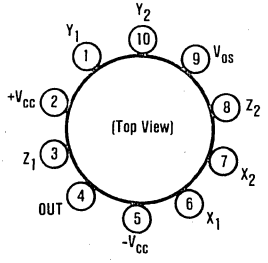
MECHANICAL



ORDER NUMBER:
4213AM
4213BM
4213SM
WEIGHT:
1 gram

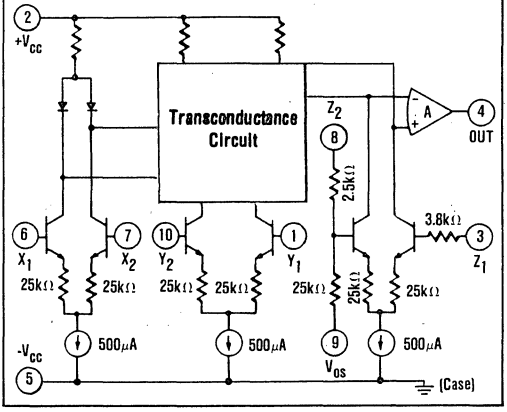
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

PIN CONFIGURATION



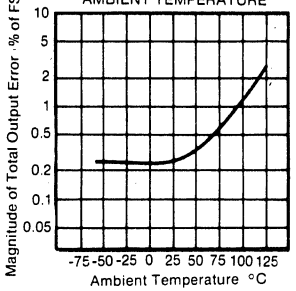
NOTES:
1. V_{os} adjustment optional not normally recommended. V_{os} pin may be left open or grounded.
2. All unused input pins should be grounded.
3. Pin 5 is connected to the case.

SIMPLIFIED SCHEMATIC

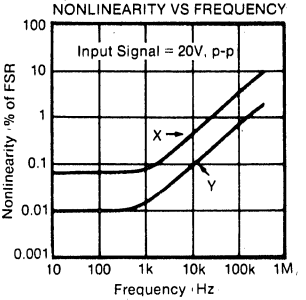


TYPICAL PERFORMANCE CURVES

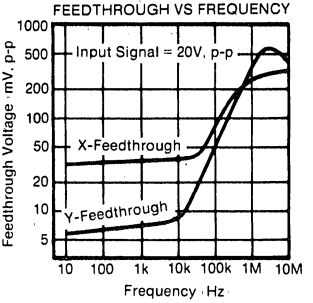
TOTAL ERROR VS AMBIENT TEMPERATURE



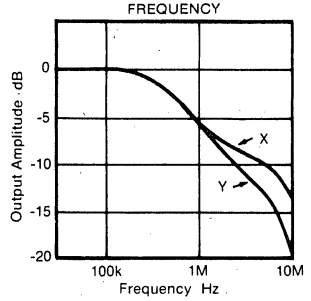
NONLINEARITY VS FREQUENCY



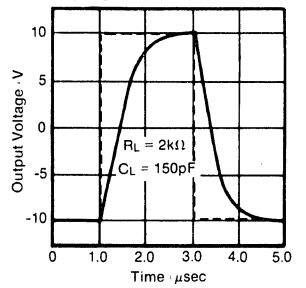
FEEDTHROUGH VS FREQUENCY



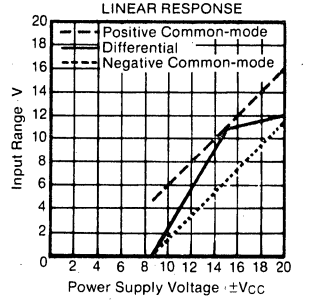
OUTPUT AMPLITUDE VS FREQUENCY



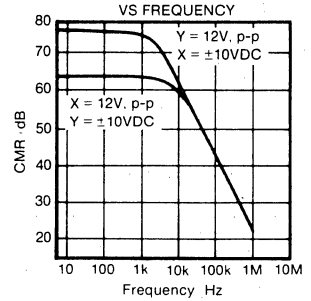
LARGE SIGNAL RESPONSE



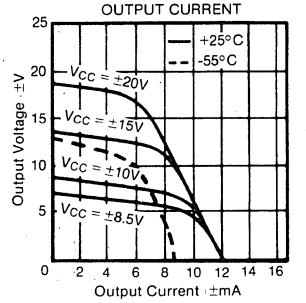
INPUT VOLTAGE FOR LINEAR RESPONSE



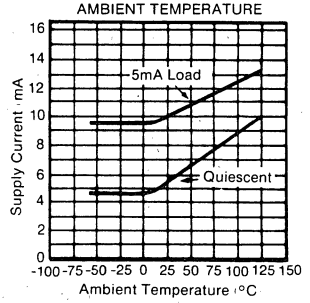
COMMON-MODE REJECTION VS FREQUENCY



OUTPUT VOLTAGE VS OUTPUT CURRENT



SUPPLY CURRENT VS AMBIENT TEMPERATURE



ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	500mW
Differential Input Voltage(2)	±40VDC
Input Voltage Range(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-circuit Duration(3)	Continuous
Junction Temperature	+150°C

NOTES:
1. Package must be derated based on: θ_{JC} = 55°C/W and θ_{JA} = 165°C/W.
2. For supply voltages less than ±20VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground only. Rating applies to +85°C ambient.

BURR-BROWN®

4214

MULTIPLIER - DIVIDER

FEATURES

- DIFFERENTIAL INPUTS
- LASER-TRIMMED
- GUARANTEED ACCURACY
  0.5% and 1%
- SELF-CONTAINED
  No additional parts required
- LOW NOISE
  120μV rms, 10Hz - 10kHz
- DIP PACKAGES

APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOTING
- ADAPTIVE CONTROL
- ALGEBRAIC COMPUTATION
- POWER COMPUTATION

DESCRIPTION

The 4214 family of multipliers are low cost integrated circuit multiplier/dividers designed for general purpose usage. In addition to four quadrant multiplication, they also perform division and square rooting of analog signals. They do not require use of additional amplifiers to perform these functions. The 4214 is laser-trimmed prior to final packaging and is guaranteed to its rated accuracy with no external components - a distinct advantage from standpoints of cost and reliability.

4214 contains its own zener regulated references and, as a result is much less sensitive to supply voltage variation than were earlier IC multipliers. The multipliers' output noise is only 120μV rms in a 10Hz to 10kHz bandwidth.

The unit is available in two 14 pin DIP packages. The plastic version ("P" package) is offered for minimum cost as is specified over the -25°C to +85°C range. The hermetic metal package ("M" package option) provides operation over the full -55°C to +125°C temperature range.

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ELECTRICAL SPECIFICATIONS

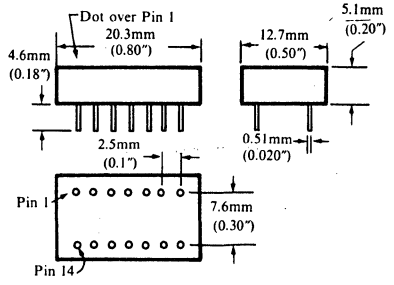
Typical performance at +25°C with rated power supplies unless otherwise noted.

MODEL	4214AP/RM[3]	4214BP/SM[3]
OUTPUT FUNCTION	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$	
TOTAL ERROR[1]		
Without Trimming	1% max	0.5% max
Error vs Temperature (-25°C to +85°C), (AP and BP)	0.008%/°C typ., 0.02%/°C max	
(-55°C to +125°C), (RM and SM)	0.025%/°C typ., 0.05%/°C max	
Error vs Supply	0.05%/%	
INDIVIDUAL ERRORS		
Output Offset	10mV typ	7mV typ
	50mV max	25mV max
vs Temperature	0.7mV/°C typ	0.3mV/°C typ
	2mV/°C max	0.7mV/°C max
vs Supply	0.25mV/%	
Scale Factor Error	0.12%	
vs Temperature	0.008%/°C	
vs Supply	0.05%/%	
Nonlinearity		
X(X = 20V p-p, Y = ±10VDC)	±0.08%	
Y(Y = 20V p-p, X = ±10VDC)	±0.01%	
Feedthrough at 50 Hz		
X = 20V p-p, Y = 0	30mV p-p	
Y = 20V p-p, X = 0	6mV p-p	
vs Temperature	0.1mV p-p/°C	
vs Supply	0.15mV p-p/%	
AC PERFORMANCE		
Small Signal ±3dB Flatness	610 kHz	
Small Signal ±1% Flatness	90 kHz	
Small Signal ±1% Vector Error (0.57° Phase Shift)	7.5 kHz	
Full Power Bandwidth	330 kHz	
Slew Rate	23V/μs	
Settling Time to 1% (20V step)	1.7μs	
OUTPUT NOISE (X = Y = 0)		
10 Hz to 10 kHz	120μV rms	
10 Hz to 10 MHz	700μV rms	
INPUT CHARACTERISTICS		
Input Voltage Range		
Rated Operation, min.	±10V	
Absolute max	±V$_s$	
Input Impedance, X, Y, Z[2]	10 MΩ	
Input Bias Current, X, Y, Z	1.4μA	
OUTPUT CHARACTERISTICS		
Rated Output	±10V at ±5mA min	
Output Impedance	1.5Ω	
POWER SUPPLY REQUIREMENTS		
Rated Voltage	±15V	
Operating Range	±8.5VDC to ±20VDC	
Quiescent Current	±5.5mA	
TEMPERATURE RANGE		
Rated Performance (specification) AP and BP	−25°C to +85°C	
RM and SM	−55°C to +125°C	
Operation	−55°C to +125°C	
Storage AP and BP	−40°C to +85°C	
RM and SM	−65°C to +150°C	

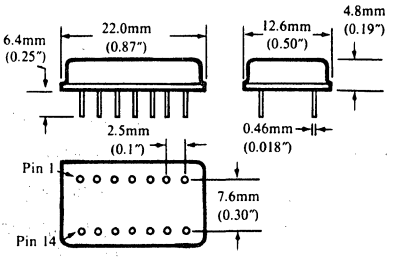
1. Total error is the maximum allowed value of the sum of the individual errors.
2. Z_2 input impedance is 10 MΩ typ with Pin 11 open circuit. If Pin 11 is grounded or used for optional offset adjustment the Z_2 input impedance may become as low as 25kΩ.
3. 4214RM and 4214SM will be available after May 15, 1978.

MECHANICAL

4214AP, 4214BP
Weight: 2.9 grams (0.10 oz.)

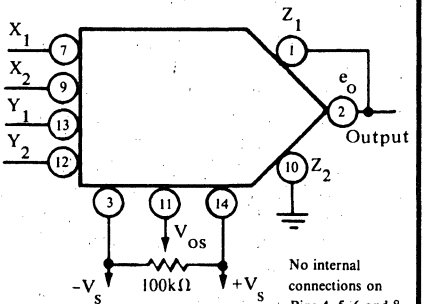


4214RM, 4214SM
Weight: 3.9 grams (0.13 oz.)



Connector: 0145MC (14-pin DIP)
Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

CONNECTION DIAGRAM



No internal connections on Pins 4, 5, 6 and 8.

$$e_o = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$$

NOTE: V_{os} adjustment optional, not normally recommended. Pin 11 may be left open or grounded.

BURR-BROWN®

4302

Low Cost MULTIFUNCTION CONVERTER

FEATURES

- LOW COST
- SMALL PACKAGE - Dual-in-line
- RELIABLE HYBRID CONSTRUCTION
- VERSATILE

FUNCTIONS	ACCURACY
MULTIPLY	±0.25%
DIVIDE	±0.25%
SQUARE	±0.03%
SQUARE ROOT	±0.07%
EXPONENTIATE	±0.15% (m = 5)
ROOTS	±0.2% (m = .2)
SINE θ	±0.5%
COSINE θ	±0.8%
TAN $^{-1}$ (Y/X)	±0.6%
$\sqrt{X^2 + Y^2}$	±0.07%

Typical accuracies expressed as a % of output full scale (+10VDC) at 25°C

DESCRIPTION

Burr-Brown's multifunction converter model 4302 is a low cost solution to many analog conversion needs. Much more than just another multiplier/divider, the 4302 out performs many analog circuit functions with a very high degree of accuracy at a very low total cost to the user.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-326D

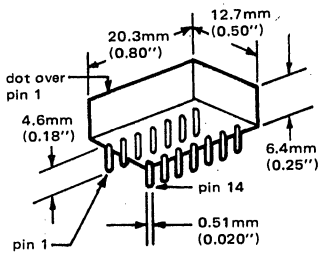
SPECIFICATIONS

Performance typical at 25°C and with rated supply unless otherwise noted.

ELECTRICAL

MODEL	4302
TRANSFER FUNCTION	$E_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$
RATED OUTPUT	
Voltage	+10.0 V
Current	5 mA
INPUT	
Signal Range	$0 \leq (V_X, V_Y, V_Z) \leq +10$ V
Absolute Maximum	$(V_X, V_Y, V_Z) \leq \pm 18$ V
Impedance (X/Y/Z)	100 kΩ/90 kΩ/100 kΩ
EXPONENT RANGE	
Roots ($0.2 \leq m < 1$)	$m = \frac{R_2}{R_1 + R_2}$ Refer to Functional Diagram below
Powers ($1 < m \leq 5$)	$m = \frac{R_1 + R_2}{R_2}$
($m = 1$)	$R_1 = 0\ \Omega$, R_2 not used
POWER REQUIREMENTS	
Rated Supply	±15 VDC
Range	±12 to ±18 VDC
Quiescent Current	±10 mA
TEMPERATURE RANGE	
Operating	−25°C to +85°C
Storage	−25°C to +85°C

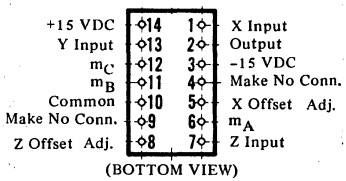
MECHANICAL



Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-pin DIP
0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

PIN CONNECTIONS

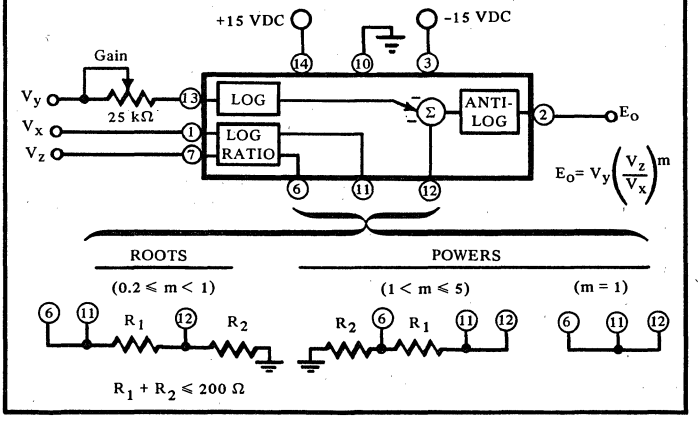


General specifications for the Model 4302 Multifunction Converter are presented on this page. These specifications characterize the 4302 as a versatile three input multifunction converter.

The following pages are applications oriented to help you apply the 4302 to your particular circuit function need. These pages contain dedicated circuit configurations in order to produce the functions of: multiplication, division, exponentiation, square rooting, squaring, sine, cosine, arctangent, and vector algebra.

It is the purpose of this product data sheet to enable you to apply the 4302 to your analog conversion needs quickly and efficiently.

4302 FUNCTIONAL DIAGRAM



Many of the following circuit configurations using the 4302 require a reference voltage for scaling purposes. The reference voltage is shown to be +15 VDC (+15 VDC REF.) since in most cases the +15 VDC power source for the 4302 has sufficient time and temperature related stability to achieve the specified typical accuracies.

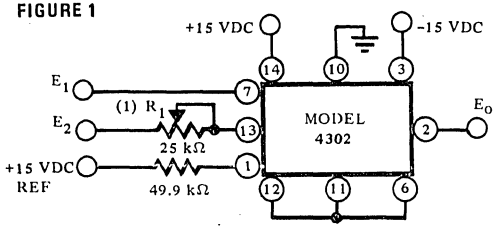
If the particular supplies which are available for powering the 4302 do not have the necessary stability for the required conversion accuracy, an additional +15 VDC precision supply may be required.

MULTIPLIER/DIVIDER FUNCTIONS

MULTIPLIER

In multiplier applications the 4302 provides high accuracy at a low cost. The 4302 accepts inputs up to +10 VDC and provides a typical accuracy of ±0.25% of full scale.

FIGURE 1



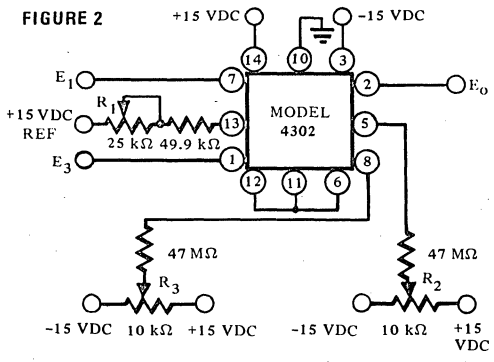
(1) Set R_1 so that with $E_1 = E_2 = +10.00$ VDC, $E_o = +10.00$ VDC.

Transfer Function	$E_o = +\frac{E_1 E_2}{10}$
ACCURACY	
Total Errors	
Typical at +25°C	±25 mV
Maximum at +25°C	±50 mV
(for input range)	$\begin{cases} 0.03V \leq E_1^* \leq 10\ V \\ 0.01\ V \leq E_2 \leq 10\ V \end{cases}$
vs. Temperature	±1 mV/°C
Offset Errors ($E_1 = E_2 = 0$)	
Output Offset (at 25°C)	±10 mV
vs. Temperature	±0.2 mV/°C
NOISE (10 Hz to 1 kHz)	100 μV rms
BANDWIDTH (E_1, E_2)	
Small Signal (-3 dB)	500 kHz
Full Output	60 kHz

DIVIDER

As a divider, the 4302 outperforms many of the multiplier/dividers on the market at a much lower cost. In the divider configuration the 4302 boasts a typical conversion accuracy of ±0.25% of full scale.

FIGURE 2



Transfer Function	$E_o = +10\ (E_1/E_3)$
ACCURACY	
Total Errors	
Typical at +25°C	±25 mV
Maximum at +25°C	±50 mV
(for $E_1 \leq E_3$ and input range)	$\begin{cases} 0.03V \leq E_1^* \leq 10\ V \\ 0.1\ V \leq E_3 \leq 10\ V \end{cases}$
vs. Temperature	±1 mV/°C
Offset Errors ($E_1 = 0$, $E_3 = +10$ V)	
Output Offset (at 25°C)	±10 mV
vs. Temperature	±1 mV/°C
NOISE (10 Hz to 1 kHz)	
$E_3 = +10$ V	100 μV rms
$E_3 = +0.1$ V	300 μV rms
BANDWIDTH (E_1, E_3)	
Small Signal (-3 dB)	500 kHz
Full Output ($E_3 = +10$ V)	60 kHz

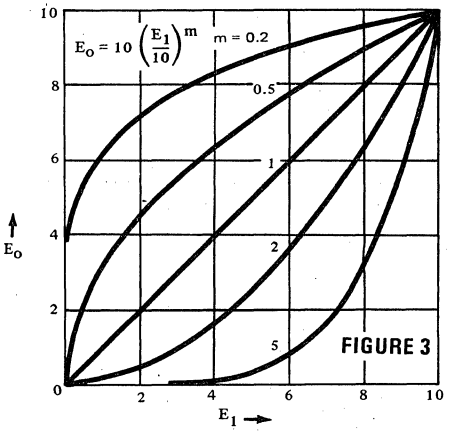
NOTES:
(1) Set R_1 so that with $E_1 = E_3 = +10.00$ VDC, $E_o = +10.00$ VDC.
(2) Set R_2 so that with $E_1 = E_3 = +0.10$ VDC, $E_o = +10.00$ VDC.
(3) Set R_3 so that with $E_1 = +0.01$ VDC and with $E_3 = +0.10$ VDC, $E_o = +1.00$ VDC.
(4) Repeat steps 1 through 3 as necessary to achieve the specified output voltages.

* The input voltage may be extended below 0.03V by connecting a 0.047 μF capacitor between pins 11 and 5, causing a slight reduction in bandwidth. (Multiply and Divide Modes).

EXPONENTIAL FUNCTIONS

Model 4302 may be used as exponentiator over a range of exponents from 0.2 to 5. The exponents 0.5 and 2, square rooting and squaring respectively, are often used functions and are treated below. Other values of exponents (m) may be useful in terms of linearization of nonlinear functions or simply for producing the mathematical conversions. Characteristics of m = 0.2 and m = 5 are presented on the right. For other values of m the curves presented in Figure 3 may be used to interpolate the error for a nonspecified value of m.

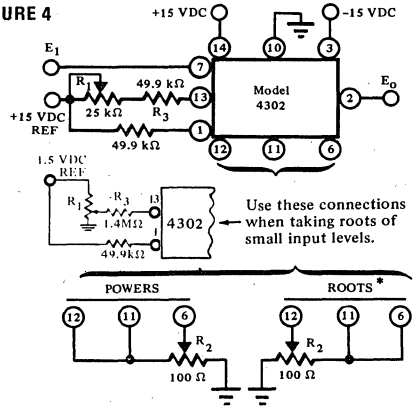
Transfer Function	$E_o = 10\left(\frac{E_1}{10}\right)^m$
Total Conversion Error (typical)	
m = 0.2	
0.5 VDC < $E_1 \leq$ 10 VDC	±2 m VDC
0.1 VDC < $E_1 \leq$ 0.5 VDC	±25 m VDC
m = 5	
1.0 VDC < $E_1 \leq$ 10 VDC	±15 m VDC
Exponent Range (continuous)	$0.2 \leq m \leq 5$
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC



Exponentiator Transfer Characteristics

NOTES:
(1) Connect a 100 Ω potentiometer as shown in Figure 4 for either roots ($0.2 \leq m < 1$) or powers ($1 < m \leq 5$).
(2) Set R_1 so that with $E_1 = +10.00$ VDC, $E_o = +10.00$ VDC.
(3) Select a + DC voltage level (E_1) such that the output voltage (E_o), as acted upon by the desired exponent, will not exceed +10.00 VDC. A level which is mid-range for input values of interest is an appropriate one to use. Set R_2 so that the output voltage (E_o) is the value expected for the chosen values of input (E_1) and exponent (m).

FIGURE 4



(4) Repeat steps (2) through (4) as necessary.

* When taking roots of smaller input levels, a modified transfer equation [$E_o = (10E_1)^m$] will provide improved conversion accuracy. To achieve this transfer function: 1) apply a +1.5 VDC REF in place of the +15 VDC REF shown in Figure 4., 2) make R_3 a 1.40 MΩ resistor, and rearrange R_1 and R_3 as 1.5VDC REF and 3) follow all notes except in note (2) apply +0.10VDC to pin 7 to set R_1 to $E_o = +1.00$VDC.

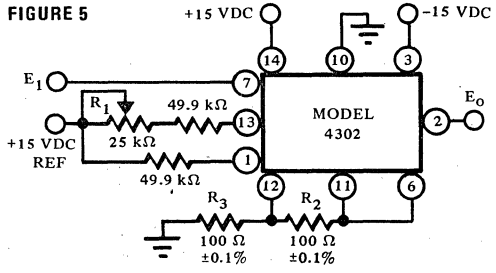
SQUARE ROOT

As a Square Rooter (m = 0.5), the 4302 provides a typical total conversion accuracy of ±0.07%. Refer to Figure 5 and notes for connections and adjustments respectively.

Transfer Function	$E_o = 10\sqrt{\frac{E_1}{10}}$
Total Conversion Error (Typical)	
0.5 VDC < E_1 ≤ 10 VDC	±7 mV
0.02 VDC < E_1 ≤ 0.5 VDC	±55 mV
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC

NOTES:
(1) Connect pins 12, 11, and 6 together. Set R_1 such that with $E_1 = +10.00$ VDC; $E_o = +10.00$ VDC.
(2) Connect 100 Ω resistors as shown in Figure 5.
(3) For greater conversion accuracy, R_2 & R_3 may be replaced by a potentiometer as shown in Figure 4.

FIGURE 5



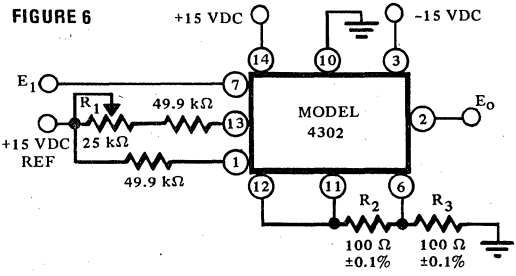
SQUARE

Configured as a Square Function Converter (m = 2), the 4302 produces high conversion accuracies of typically 0.03%. Please refer to Figure 6 and accompanying notes.

Transfer Function	$E_o = 10\left(\frac{E_1}{10}\right)^2$
Total Conversion Error (typical)	
0.1 VDC ≤ E_1 ≤ 10 VDC	±3 mV
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC

NOTES:
(1) Set R_1 such that with $E_1 = +10.00$ VDC, $E_o = +10.00$ VDC.
(2) Connect 100 Ω resistors as shown in Figure 6.
(3) For greater conversion accuracy R_2 & R_3 may be replaced by a potentiometer as shown in Figure 4.

FIGURE 6



TRIGONOMETRIC FUNCTIONS

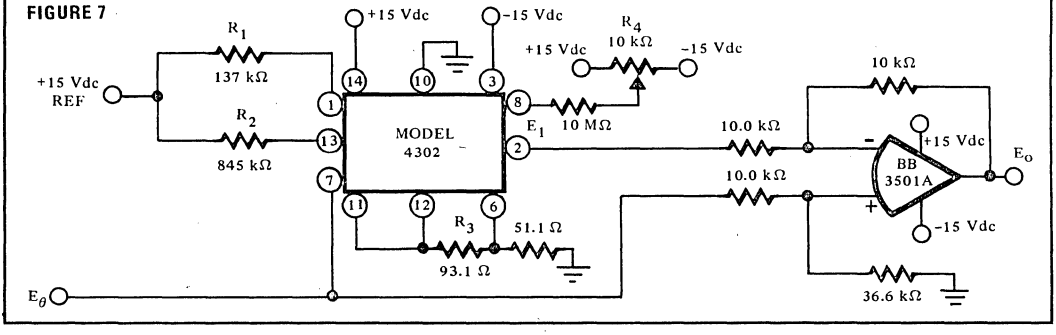
SINE

Sine functions can be accurately generated from input voltage levels representing angular displacement from 0 to 90°. Model 4302 configured as in Figure 7 will produce the sine power series approximations with modified coefficients to typically better than ±0.5% of full scale. In this circuit, the 4302 is scaled so that when $\theta = 0$, $E_O = 0$ VDC, and when $\theta = 90$, $E_O = 10$ VDC.

NOTES:
(1) Adjust R_4 if needed so that $E_1 < 1$ m VDC when $E_\theta = 0$.
(2) Adjust R_2 so that $E_1 = +0.8045$ VDC when $E_\theta = +5.00$ VDC.
(3) Adjust R_3 so that $E_1 = +5.709$ VDC when $E_\theta = +10.00$ VDC.
(4) Repeat steps (2) and (3) as necessary.

Transfer Function	$E_O = 10 \text{ Sin } 9E_\theta$
Power Series Approximation $E_O = 1.5708E_\theta - 1.5924\left(\frac{E_\theta}{6.366}\right)^{2.827}$	
Total Conversion Error (typical)	±50 mV
Input Voltage Range ($0 \leq \theta \leq 90^o$)	0 to +10 VDC
Output Voltage Range ($0 \leq \sin\theta \leq 1$)	0 to +10 VDC

FIGURE 7



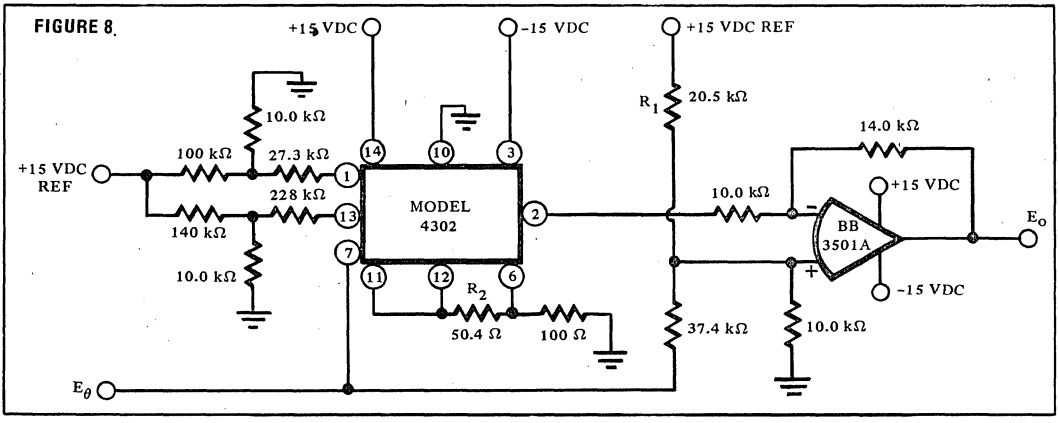
COSINE

Connected as in Figure 2, the Model 4302 will generate a cosine function of the input voltage. Typical accuracies of ±0.8% can be expected from this configuration.

NOTES:
(1) Adjust R_1 so that $E_O = +10.00$ VDC when $E_\theta = 0$.
(2) Adjust R_2 so that $E_O = 0$ when $E_\theta = +10.00$ VDC.

Transfer Function	$E_O = 10 \cos 9E_\theta$
Power Series Approximation $E_O = 10 + 0.3652\,E_\theta - 0.4276E^{1.504}$	
Total Conversion Error (typical)	±80 mV
Input Voltage Range ($0 \leq \theta \leq 90^o$)	0 VDC to +10 VDC
Output Voltage Range ($1 \leq \cos\theta \leq 0$)	+10 VDC to 0 VDC

FIGURE 8



ARCTANGENT

Model 4302 and the associated circuitry shown below will produce the inverse tangent of a ratio. This application is particularly well suited to conversion from rectangular coordinates to polar coordinates where

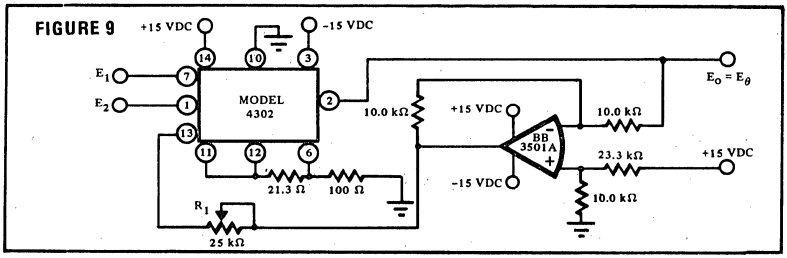
$$E_\theta = \tan^{-1}\frac{E_Y}{E_X}$$

The accuracy of conversion depends upon the levels of the input signals. Please refer to table at right.

Transfer Function	$E_o = \tan^{-1}\left(\frac{[E_1]}{[E_2]}\right)$
Power Series Approximation	$E_o = \frac{\left(\frac{[E_1]}{[E_2]}\right)^{1.2125}}{1+\left(\frac{[E_1]}{[E_2]}\right)^{1.2125}}(90^o)$
Total Conversion Error $2 < E_1, E_2 \leq 10$ VDC $0.1 < E_1, E_2 \leq 2$ VDC $0.03 < E_1, E_2 \leq 0.1$ VDC Input Voltage Range (E_1, E_2) Output Voltage Range $0 \leq E_\theta \leq 90^o$	 ±55 m VDC ±65 m VDC ±340 m VDC +0.01 VDC to +10 VDC 0 VDC to +9 VDC

NOTE:
(1) Set R_1 so that with $E_1 = E_2 = +10.00$ VDC, $E_o = +4.500$ VDC ±1 mVDC.

FIGURE 9



VECTOR MAGNITUDE FUNCTION

The model 4302 will produce the square root of the sum of the squares of two inputs. This function is companion to the arctangent of a ratio for the conversion of rectangular to polar coordinates.

Transfer Function	$E_o = \sqrt{E_1^2 + E_2^2}$
Input Voltage Range E_1 E_2	0 to +10VDC -10VDC to +10VDC
(refer to notes 1 and 2)	
Output Voltage Range	0 to +10VDC
Conversion Error	±7m VDC

NOTES:

1. Figure 10 shows one practical way to implement the transfer function $E_o=\sqrt{E_1^2+E_2^2}$ using 4302. It shows use of model 3501A op amp. Model 3501's rated output is ±10V. This limits the range of E_1 and E_2, such that the conditions $E_1 \leq \sqrt{100 - E_2}$ and $|E_2| \leq (5 - E_1^2/20)$ and $\sqrt{E_1^2 + E_2^2} \leq 10$ are always satisfied.
   (a) The above conditions imply, $0V \leq E_1 \leq 10V$ and $-5V \leq E_2 \leq 5V$.
   (b) The above conditions also imply that for applications where $E_1 = |E_2|$ the range would be limited to 4.142V max.
2. Use of model 3627 as shown in Figure 11 would directly substitute the eight 10kΩ resistors and the two model 3501A op amps. This would reduce the number of components needed to implement vector magnitude function and reduce overall cost.

FIGURE 10

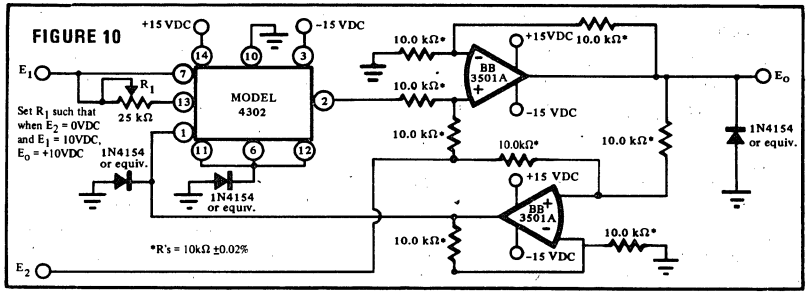
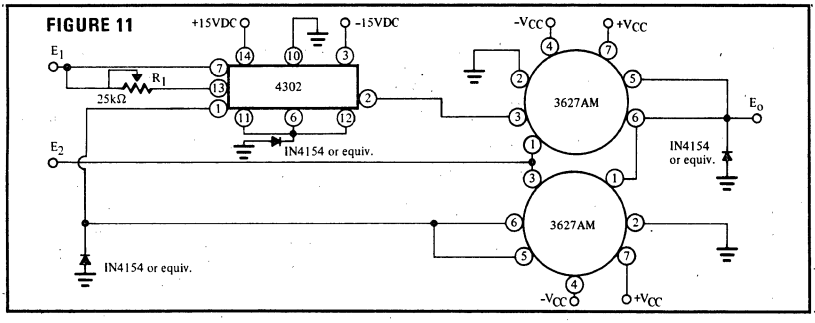


FIGURE 11



BURR-BROWN®

4340

TRUE RMS-TO-DC CONVERTER

FEATURES

- LOW COST
- HIGH ACCURACY
  ±0.3mV ±0.1% Reading
- HIGH INPUT IMPEDANCE - 5kΩ
- HERMETIC METAL PACKAGE

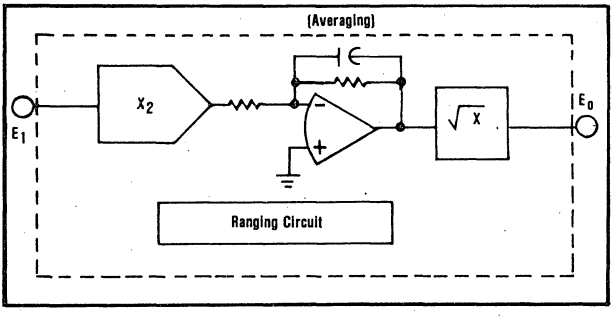
DESCRIPTION

The Burr-Brown Model 4340 is a true rms-to-DC converter featuring high performance, low cost, and a small hermetic package. The 4340 will compute the true rms value of a variety of signals applied to the input. The input signal may consist of complex AC waveforms as well as a DC voltage level. The output of the 4340 is a DC voltage, the amplitude of which is equal to the rms value of the input voltage.

The 4340 will accept input voltages from 0 to ±10V over a wide input frequency range. The conversion accuracy of the 4340 is specified in terms of error in millivolts plus a percent of reading, as a function of input signal level over an input frequency range.

The 4340 has an input impedance of 5kΩ and an output impedance of 1Ω. This product will supply up to 5mA of output current at a voltage of +10VDC. The input is fully protected for conditions of overvoltage up to the supply voltage. The output will withstand short-circuit to power supply common for an indefinite period of time.

The specified unadjusted performance characteristics of the 4340 are shown in the Electrical Specifications. Provision for the external adjustment of gain, voltage offset, DC reversal error, and frequency response performance allow the user to improve upon the specified conversion accuracies to the degree required by the user's application.



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SPECIFICATIONS

ELECTRICAL

Typical at 25°C with rated power supplies unless otherwise noted.

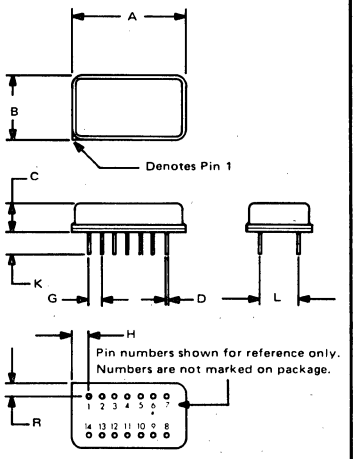
MODEL	4340
TRANSFER FUNCTION	E_O (DC) = $\sqrt{E_{IN}^2}$
INPUT	
Peak Voltage	±10VDC
Absolute Maximum Voltage	±Supply
Impedance	5kΩ
OUTPUT	
Voltage	0 to +10VDC
Current, min	+5mA
Impedance	1Ω
CONVERSION ACCURACY	
Total Unadjusted Error, max	
Input: 10mV, rms to 7V, rms	±2mV ±0.2% Reading
Input: 100Hz to 10kHz sine wave*	
Total Adjusted Error**	
Input: 10mV, rms to 7V, rms	±0.3mV ±0.1% Reading
Input: 50Hz to 20kHz*	
STABILITY	
Accuracy vs Temperature	±0.001% of FSR plus ±0.01% of reading per °C
Accuracy vs Supply	±0.001% of FSR plus ±0.01% of reading per %ΔV
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +125°C
POWER REQUIREMENTS	
Rated Voltage	±15VDC
Voltage Range	±14VDC to ±16VDC
Quiescent Current	±12mA

*Model 4340 will convert DC inputs. Lower frequency AC input signals will require the addition of external capacitors to preserve the accuracy.

**Performance with external trims and $C_L \geq 3\mu F$ and $20pF \leq C_H \leq 100pF$.

MECHANICAL

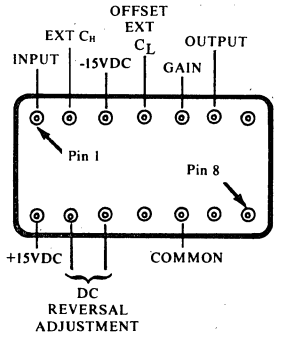
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

Pin material and plating composition meet method 2003 (solderability) of MIL-STD-883 (except for paragraph 3.2.1).

PIN CONNECTIONS



(BOTTOM VIEW)

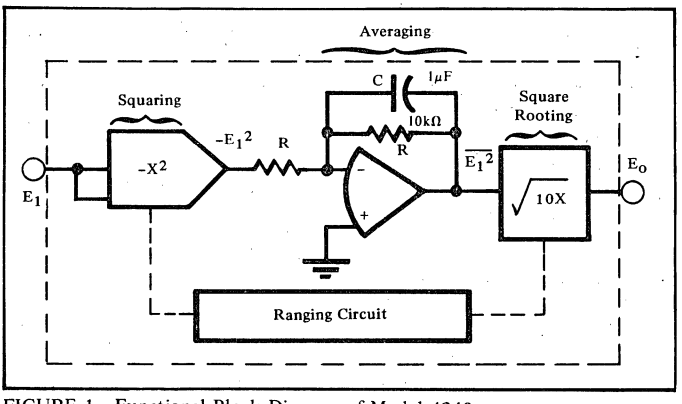


FIGURE 1. Functional Block Diagram of Model 4340.

BURR-BROWN®

4341

Low Cost
TRUE RMS-TO-DC CONVERTER

FEATURES

- LOW COST
- HIGH ACCURACY
  ±0.2% ±2mV
- HIGH RELIABILITY
  Hybrid construction

DESCRIPTION

The Burr-Brown Model 4341 RMS-to-DC Converter features low cost without sacrificing performance. The 4341 computes a DC voltage proportional to the true rms value of signals which may be complex waveforms, DC levels, or a combination of both.

The input and output are fully protected against overvoltages and short circuits. Provisions for the external adjustment of gain, offset voltage, DC-reversal error, and frequency response make the 4341 versatile enough to fill the majority of your applications.

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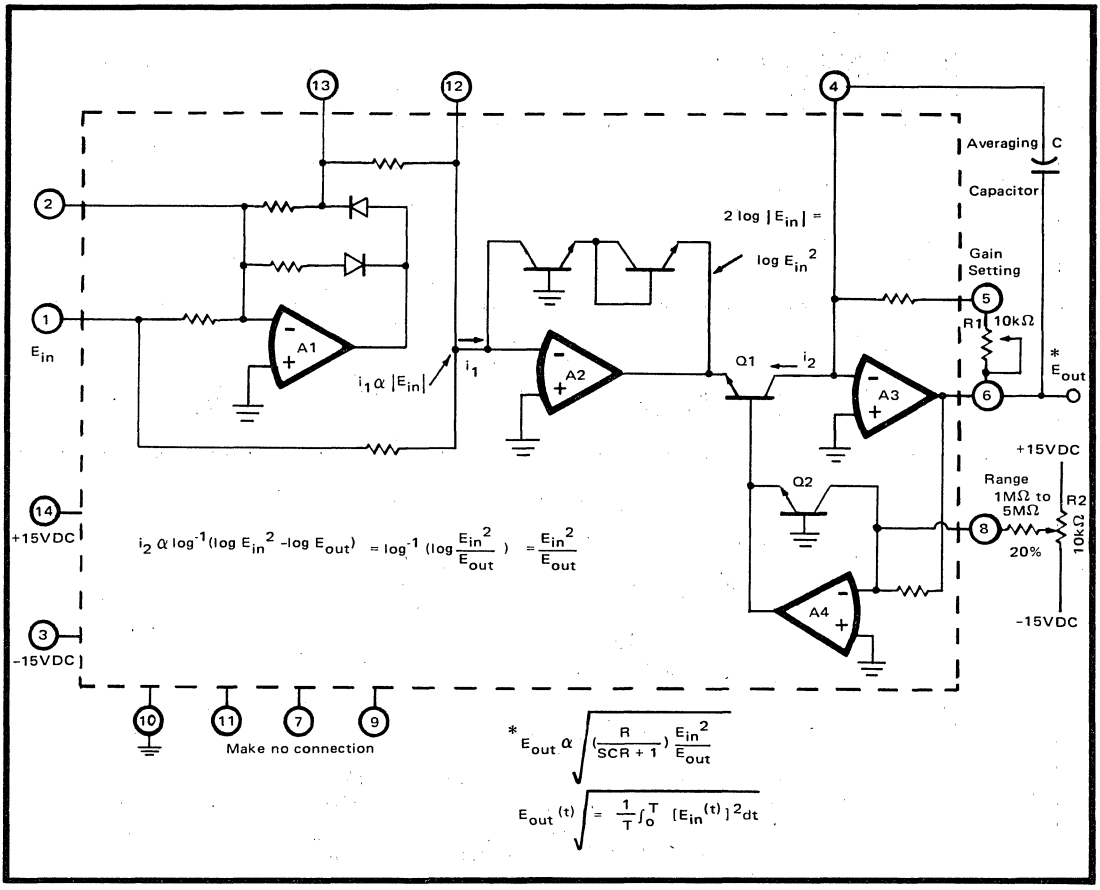


FIGURE 1. Simplified Schematic.

THEORY OF OPERATION

The true rms value of a time-varying signal E (t) over a time period T is

$$E_{rms} = \sqrt{1/T \int T/o\,[E(t)]^2\,dt}$$

The required operations are squaring, averaging and square rooting. A simplified schematic diagram of the 4341 is shown in Figure 1. The A1 circuit produces a current i_1 which is proportional to the rectified input voltage. The A2 circuit is a logarithmic amplifier which produces a voltage proportional to 2 log E_{in} or log E_{in}^2. The logarithmic gain of the A2 circuit is derived from the inherent exponential characteristics of transistor junctions. By using proprietary monolithic components, the circuit provides an accurate log function over many decades which is relatively insensitive to temperature variations. Amplifier A4 uses the same techniques as A2 to generate log E_{out}.

Transistor Q1 produces a collector current i_2 proportional to the antilog of its base-emitter voltage such that

$$i_2 \alpha \log^{-1} (\log E_{in}^2 - \log E_{out})$$
$$= \log^{-1} (\log E_{in}^2/E_{out}) = E_{in}^2/E_{out}$$

The A3 circuit which contains the external capacitor takes the time average of the i_2 signal and produces E_{out} which is directly proportional to the rms value of E_{in}.

Figures 2 and 3 show the effects of the external filter capacitor on ripple magnitude and response time. As the frequency of the input approaches DC, the 4341 begins to act like a full wave rectifier such that the output is the absolute value of the input. While the 4341 will accurately convert DC input voltages, the averaging capacitor must be made very large to minimize ripple at low frequencies.

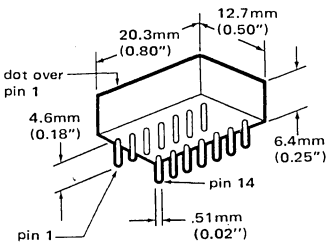
ELECTRICAL SPECIFICATIONS

Typical at 25°C with rated supply voltages, unless otherwise noted.

MODEL	4341
TRANSFER FUNCTION	$I_{out}(DC) = 1/T \int_0^T E_{in}^2(t)\,dt$
INPUT	
Peak Operating Voltage	±10V
Absolute Maximum Voltage	±Supply
Impedance	5kΩ
OUTPUT	
Voltage	0 to +10V
Current	+5mA, min
Resistance	1Ω, max
BANDWIDTH	
±1% of Theoretical Output	80kHz
-3dB	450kHz
CONVERSION ACCURACY[2]	
Input: 500mV, rms to 5.0V, rms Input: DC to 10kHz Sine Wave	±0.5% of Reading, max[1]
Input: 10mV, rms to 7V, rms Input: DC to 20kHz	±2mV ±0.2% Reading
STABILITY	
Accuracy vs. Temperature	±0.1mV ±0.01% of Reading/°C
Accuracy vs. Supply Voltage	±0.1mV ±0.01% of Reading/% of Supply Voltage Change
TEMPERATURE RANGE	
Operating	−25°C to +85°C
Storage	−40°C to +85°C
POWER REQUIREMENTS	
Rated Voltage	±15VDC
Voltage Range	±14VDC to ±16VDC
Quiescent Current	±12mA, typ., ±24mA, max

NOTES:
1. After standard trim procedure (see below).
2. Model 4341 will convert DC inputs. Lower frequency AC inputs require a large value of averaging capacitor to minimize ripple at output. (see Figure 2).

MECHANICAL



Row Spacing: 7.6mm (0.30")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-Pin DIP
0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

STANDARD TRIM PROCEDURE

If the 4341 is used to measure sine waves or distorted sine waves, only two trims are needed to achieve an accuracy of ±0.5% of reading from 500mV, rms to 5V, rms up to 10kHz. Refer to Figure 1.

1. Set E_{in} = 5.000V, rms ±0.02% and adjust R1 such that E_o = 5.000VDC ±2mV.
2. Set E_{in} = 500mV, rms ±0.02% and adjust R2 such that E_o = 500mVDC ±0.2mV.
3. Repeat Step 1.

CHOOSING THE AVERAGING CAPACITOR

A single-pole low-pass RC filter provides the averaging function. The time constant is 1/2 RC where R is 10kΩ when the 4341 is adjusted for unity gain. To select the best value of C, make a tradeoff between output ripple and response time. Figure 2 shows the ripple magnitude vs. frequency for several typical values of capacitor. Response time vs. capacitor value is shown in Figure 3. (Note that rise times and fall times are different for the same value of capacitor).

While the ripple magnitude for signals other than sine waves can be analytically determined, it is tedious. The fastest method of choosing C is to apply a representative input signal and observe the output for various value of C. C can be 100's of microfarads, but should have a leakage current less than 0.1μA to minimize gain errors. With very large values of C, the input signals with frequencies approaching DC level could be averaged. Since the output is always a positive voltage, C can be polar capacitor.

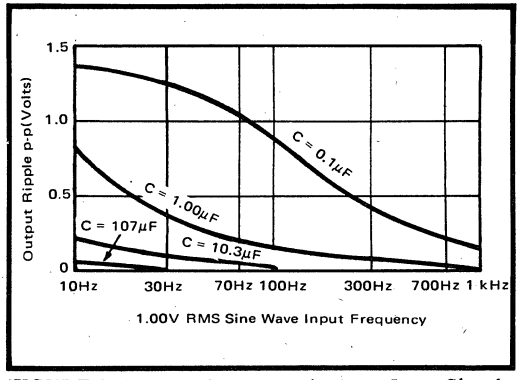


FIGURE 2. Output Ripple Magnitude vs. Input Signal Frequency.

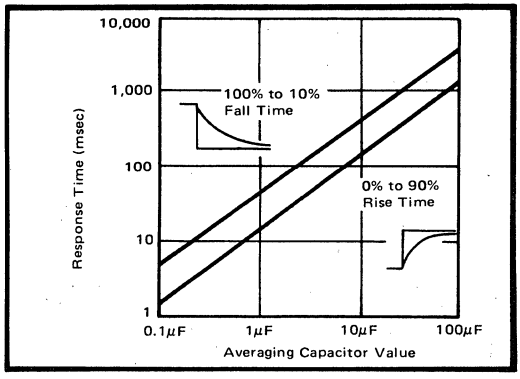


FIGURE 3. Response Time vs. Value of Averaging Capacitor.

EXPANDED TRIM PROCEDURE FOR GREATER ACCURACY

If the 4341 is used in applications to measure complex waveforms, the following expanded trim procedure is recommended. (Refer to Figure 4).

First set all potentiometers at mid turn position.

1. DC Reversal Error - Apply +10.000V ±1mV and -10.000V ±1mV to E_{in} alternatively, adjust R5 such that E_o readings are the same ±2mV.
2. Gain Adjustment - Apply E_{in} = +10.000VDC ±1mV, adjust R1 such that E_o = +10.000VDC ±1mV.
3. Input Offset - Apply +10.0mV ±0.1mV and -10.0mV ±0.1mV to E_{in}, adjust R4 such that E_o readings are the same ±0.1mV.
4. Offset - Ground E_{in}, adjust R3 such that E_o = 0 ±0.1mV. Repeat Step (3).
5. Low Level Accuracy - Apply E_{in} = +10.0mV ±0.1mV, adjust R2 such that E_o = +10.0mV ±0.1mV.

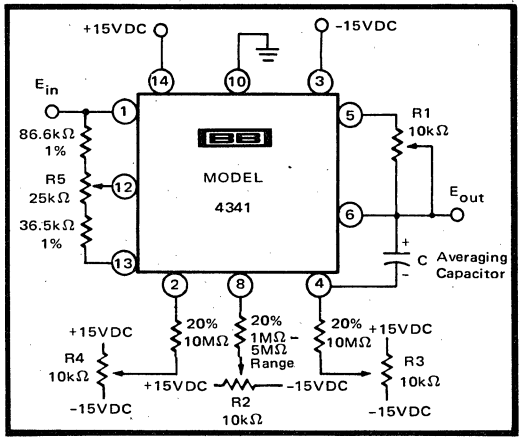


FIGURE 4. Expanded Trim Procedure (High Accuracy Applications).

NONUNITY GAINS

Gain values greater than unity can be achieved by inserting resistor R_x between pin 5 and pin 6. $R_x \simeq (A^2 - 1) \times 10k + 2k$ where A is the desired value of gain ($1 < A \leq 10$). (R_x is in ohms).

BURR-BROWN®

4423

PRECISION QUADRATURE OSCILLATOR

FEATURES

- SINE AND COSINE OUTPUTS
- RESISTOR-PROGRAMMABLE FREQUENCY
- WIDE FREQUENCY RANGE: 0.002Hz to 20kHz
- LOW DISTORTION: 0.2% max up to 5kHz
- EASY ADJUSTMENTS
- SMALL SIZE
- LOW COST

DESCRIPTION

The Model 4423 is a precision quadrature oscillator. It has two outputs 90 degrees out of phase with each other, thus providing sine and cosine wave outputs available at the same time. The 4423 is resistor programmable and is easy to use. It has low distortion (0.2% max up to 5kHz) and excellent frequency and amplitude stability.

The Model 4423 also includes an uncommitted operational amplifier which may be used as a buffer, a level shifter, or as an independent operational amplifier. The 4423 is packaged in a versatile, small, low-cost DIP package.

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SPECIFICATIONS

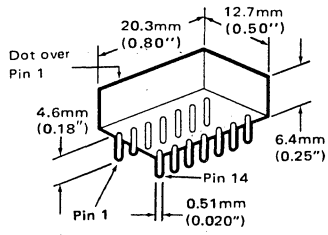
Specifications typical at 25°C and ±15VDC
Power Supply Unless Otherwise Noted.

ELECTRICAL

	MIN	TYP	MAX	UNITS
FREQUENCY				
Initial Frequency (no adjustments)	20.0k	20.5	21.0k	Hz
Frequency Range (using 2 R's only)	2k		20k	Hz
Frequency Range (using 2 R's and 2 C's)	.0.002		20k	Hz
Accuracy of Frequency Equation*		±1	±5	%
Stability vs Temperature		±50	±100	ppm/°C
Quadrature Phase Error		±0.1		degree
DISTORTION				
Sine Output (pin 1)				
0.002Hz to 5kHz			0.2	%
5kHz to 20kHz			0.5	%
Cosine Output (pin 7)				
0.002Hz to 5kHz		0.2		%
5kHz to 20kHz		0.8		%
Distortion vs Temperature		0.015		% °C
OUTPUT				
Amplitude (Sine)				
At 20 kHz	6.5	7	7.5	V rms
vs Temperature		0.05		%/°C
vs Supply		0.4		V/V
Output Current	1.5	5		mA
Output impedance			1	Ω
UNCOMMITTED OP AMP				
Input Offset Voltage		1.5		mV
Input Bias Current		275		nA
Input Impedance		1		MΩ
Open Loop Gain		90		dB
Output Current	5			mA
POWER SUPPLY				
Rated Supply Voltage		±15		VDC
Supply Voltage Range	±12		±18	VDC
Quiescent Current		±9	±18	mA
TEMPERATURE RANGE				
Specifications	0		+70	°C
Operation	-25		+85	°C
Storage	-55		+125	°C

* May be trimmed for better accuracy.

MECHANICAL



ROW SPACING - 7.6 (0.300")
WEIGHT - 3.4 gms (0.12 oz)
CONNECTOR - 14 pin DIP connector

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

PIN CONNECTIONS

1. E_1, Sine Output
2. Frequency Adjustment
3. Frequency Adjustment
4. +In, Uncommitted Op Amp
5. -In, Uncommitted Op Amp
6. Output, Uncommitted Op Amp
7. E_2, Cosine Output
8. Frequency Adjustment
9. $-V_{CC}$, -15VDC
10. $+V_{CC}$, +15VDC
11. Common
12. Frequency Adjustment
13. Frequency Adjustment
14. Frequency Adjustment

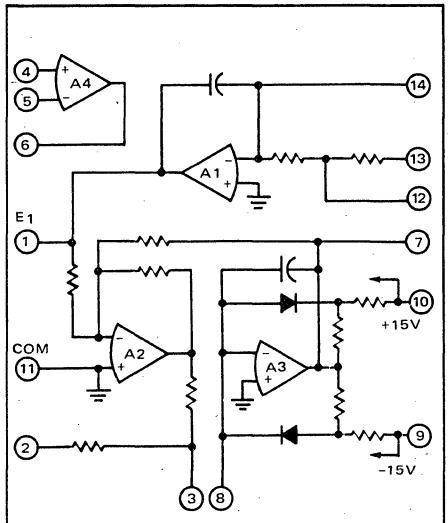


FIGURE 1. Equivalent Circuit.

TYPICAL PERFORMANCE CURVES

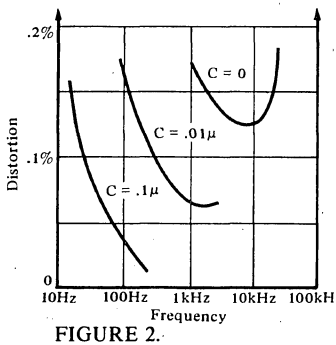


FIGURE 2.

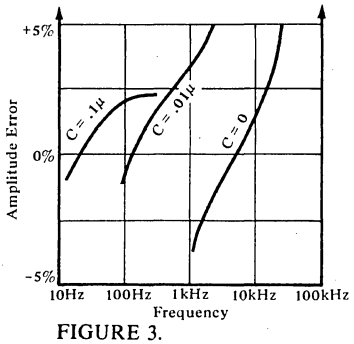


FIGURE 3.

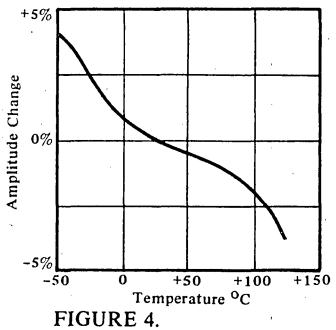


FIGURE 4.

EXTERNAL CONNECTIONS

1. 20 kHz Quadrature Oscillator

The 4423 does not require any external component to obtain a 20 kHz quadrature oscillator. The connection diagram is as shown in Figure 5.

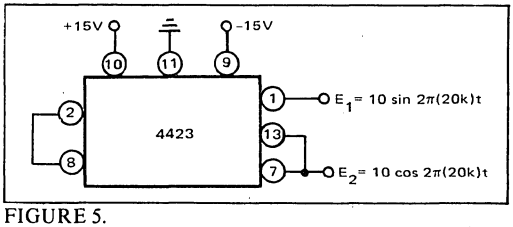


FIGURE 5.

2. Resistor Programmable Quadrature Oscillator

For resistor programmable frequencies in the 2 kHz to 20 kHz frequency range, the connection diagram is shown in Figure 6. Note that only two resistors of equal value are required. The resistor R can be expressed by,

$$R = \frac{3.785f}{42.05 - 2f}$$, R in kΩ, f in kHz

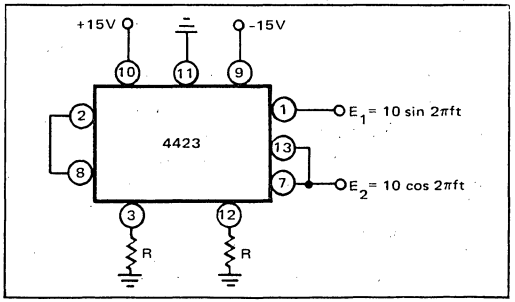


FIGURE 6.

3. Quadrature Oscillator Programmable to 0.002 Hz

For oscillator frequencies below 2000 Hz, use of two capacitors of equal value and two resistors of equal value as shown in Figure 7 is recommended. Connections shown in Figure 7 can be used to get oscillator frequency in the 0.002 Hz to 20 kHz range.

The frequency f can be expressed by:

$$f = \frac{42.05\ R}{(C + 0.001)(3.785 + 2R)}$$

where, f is in Hz
C is in μF
and R is in kΩ

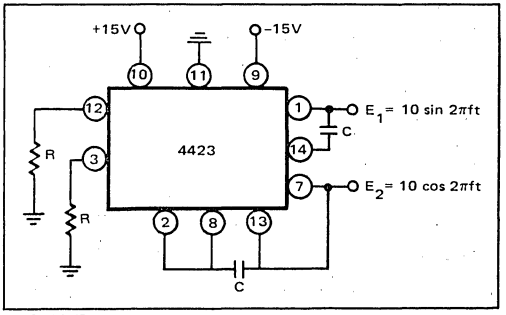


FIGURE 7.

For best results, the capacitor values shown in Table I should be selected with respect to their frequency ranges.

f	20 kHz to 2 kHz	2 kHz to 200 Hz	200 Hz to 20 Hz
C	0	0.01μF	0.1μF
20 Hz to 2 Hz	2 Hz to 0.2 Hz	0.2 Hz to 0.02 Hz	0.02 Hz to 0.002 Hz
1μF	10μF	100μF	1000μF

TABLE I.

After selecting the capacitor for a particular frequency the value of the required resistor can be obtained by using the resistor selection curve shown in Figure 8 or by the expression:

$$R = \frac{3.785f\ (C + 0.001)}{42.05 - 2f\ (C + 0.001)}$$

where,
R is in kΩ
f is in Hz
and C is in μF

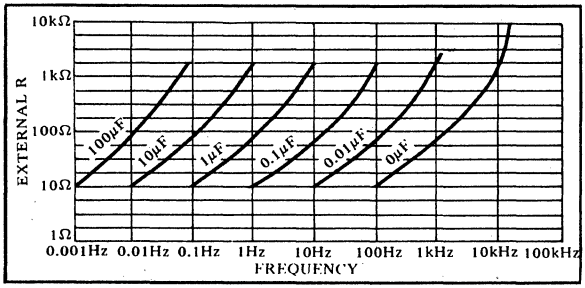


FIGURE 8.

The curves shown in Figure 8 are provided only as a nomographic design aid. The selection of capacitor values is not limited to the values shown in Figure 8. Any suitable combination of R and C values which satisfies the expression relating R, F and C as shown above, would work satisfactorily with the 4423.

NOTES ON TYPES OF CAPACITORS TO USE:

There are various kinds of capacitors available for use. There are polarized, also known as DC capacitors and non-polarized, also known as AC capacitors available. Of these two types, the polarized capacitors cannot be used with 4423 to set the frequencies.

Commonly available non-polarized capacitors include NPO ceramic, silver mica, teflon, polystyrene, polycarbonate, mylar, ceramic disc etc. A comparison is shown in Table II.

	Capacitance Range (μF)	Temperature Coefficients ppm/°C	Dissipation Factor (%)
NPO Ceramic	5pF - 0.1 μF	30	0.05
Silver Mica	5pF - 0.047 μF	60	0.05
Teflon	0.001 - 100 μF	200	0.01
Polystyrene	0.001 - 500 μF	100	0.03
Polycarbonate	0.001 - 1000 μF	90	0.08
Metalized Teflon	0.001 - 100 μF	60	0.1
Metalized Polycarbonate	0.001 - 1000 μF	10	0.4
Mylar	0.001 - 1000 μF	700	0.7
Metalized Mylar	0.001 - 2000 μF	700	1
Ceramic Disc	5pF - 0.5 μF	10,000	3

TABLE II.

For use with the 4423 oscillator, the choice of capacitors depends mainly on the user's application, error budget and cost budget. Note that the specifications of 4423 do not include the error contribution of the external components. The errors sourced by external components normally have to be added to the 4423 specifications.

As a general selection criteria we recommend the use of the above table. Start from the top of the list in the above table. If the capacitor is found unsuitable due to it being too large in size, too expensive, or is not easily available, then move down in the list for the next best selection. In any case do not choose or use any capacitors with dissipation factors greater than 1%. Such a capacitor would stop 4423 oscillation.

DISSIPATION FACTOR (DF)

A capacitor can be modeled by an ideal capacitor in parallel with an internal resistor whose value depends on its dissipation factor (DF). Mathematically, the internal resistor R is given by,

$$R = \frac{1}{2\pi f\, C(DF)}$$

where R is in Ω, f is the Hz, and C is in farads.

For example, the DF of ceramic disc capacitors is of the order of 3%, which for a 0.01 μF capacitor would look like having an internal resistor of 530kΩ at 1 kHz. 530 kΩ value resistor is small enough to stop the 4423 oscillator from oscillating.

Some capacitor manufacturers use the terms "Power Factor" (PF) or "Q Factor" (Q) instead of the term "Dissipation Factor". These terms are similar in meaning and are mathematically related by,

$$(PF) = \frac{(DF)}{\sqrt{1 + (DF)^2}} \quad ; \quad Q = \frac{1}{(DF)}$$

OSCILLATION AMPLITUDE

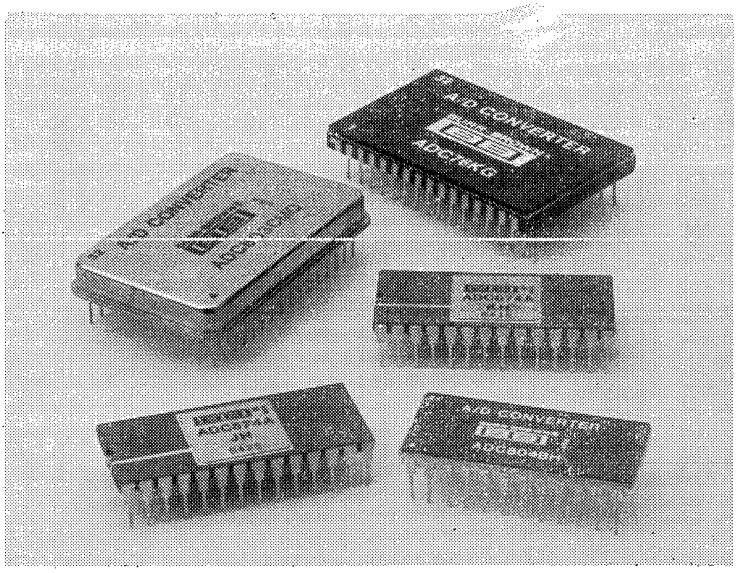
It takes a finite time to build up the amplitude of the oscillation to its final full scale value. There is a relationship between the amplitude build-up time and the frequency. The lower the frequency, the longer the amplitude build-up time. For example, typically it takes 250 seconds at 1 Hz, 30 seconds at 10 Hz, 4 seconds at 100 Hz, 400 milliseconds at 1 kHz, and 40 milliseconds at 10 kHz oscillator frequencies.

There are two methods available to shorten this normal amplitude build-up time. But there is also a relationship between the amplitude build-up time and distortion at final amplitude value. When the amplitude build-up time is shortened, the distortion can get worse.

One method to shorten the amplitude build-up time is to connect a resistor between pin 3 and pin 14. The lower this resistor is the shorter will be the time to build up amplitude of the oscillation, and worse will be the distortion of the output waveform. For example, a 100kΩ resistor would shorten the amplitude build up time from 15 seconds to 1 second at 20 Hz frequency, but the distortion could be degraded from tpically 0.05% to 0.5%.

The other method is to momentarily insert a 1kΩ resistor via a reset switch betwen pin 3 and pin 14. The amplitude of oscillation is built up instantaneously when the reset switch is pushed. There will be no degradation of distortion with this method since the 1kΩ resistor does not remain in the circuit continuously.

ANALOG-TO-DIGITAL CONVERTERS



The Burr-Brown analog-to-digital converter product line has a broad range of devices that enable the user to select the performance and price range ideally suited for the application. The high-performance 12-bit ADC80, which converts to 12-bit accuracy in 25μsec, was originated by Burr-Brown in 1975 and has become an industry standard. The recently introduced ADC803 is a 12-bit, 1.5μsec conversion time A/D converter that multiplies your system's throughput capabilities at the best price/performance ratio available. A high-resolution converter, the ADC76, converts 16 bits to $\pm$0.003% absolute accuracy in only 15μsec and is packaged in a 32-pin triple-wide dual-in-line package. Other performance categories are high-temperature (up to +200°C), and total harmonic distortion for digital recording of audio.

All devices are totally complete and fully specified, and have a track record of high reliability proven both in the field as well as in internal qualification testing.

SELECTION GUIDE

ANALOG-TO-DIGITAL CONVERTERS FOR INDUSTRIAL APPLICATIONS

These designs meet your most demanding applications. The successive approximation conversion technique permits 12-bit conversion times as short as 1μsec (ADC803CM), as well as the lowest cost 25μsec industry standard ADC80 and ADC574A and the 10μsec ADC84/85.

Other Burr-Brown industry standard high resolution A/D converters, ADC71 and ADC76, have recently been improved by utilizing higher levels of integration. This increases the reliability of the products and lowers their cost dramatically. This price/performance breakthrough opens the door to broad new application areas.

Burr-Brown has recently introduced a new standard of performance and packaging for 12-bit, 10MHz sampling rate, A/D converters with model ADC600K. As with most Burr-Brown developments, the ADC600K combines lower cost with performance improvements for maximum user benefit.

12-BIT ANALOG-TO-DIGITAL CONVERTERS

Description	Model[1]	Resolution (Bits)	Conversion Time, max (μsec)	Linearity Error, max (% of FSR)	Gain Drift, max (ppm/°C)	Zero Drift, max (ppm FSR/°C)	Input Ranges (V)	Temp Range[2]	Package	Page
Micro-Processor Interface, Low Cost, 574 Compatible	ADC574AJH	12	25	±0.024	±45[3]	±10U, ±10B[4]	±5, ±10, +10, +20	Com	24-pin DIP, Hermetic, Ceramic,	5-80
	ADC574AKH	12	25	±0.012	±25[3]	±5U, ±5B[4]		Com		5-80
	ADC574ASH	12	25	±0.024	±50[3]	±5U, ±10B[4]		MIL		5-80
	ADC574ATH	12	25	±0.012	±25[3]	±2.5U, ±5B[4]		MIL		5-80
	ADC674AJH	12	15	±0.024	±45[3]	±10U, ±10B[4]	±5, ±10, +10, +20	Com	24-pin DIP, Hermetic, Ceramic	5-93
	ADC674AKH	12	15	±0.012	±25[3]	±5U, ±5B[4]		Com		5-93
	ADC674ASH	12	15	±0.024	±50[3]	±5U, ±10B[4]		MIL		5-93
	ADC674ATH	12	15	±0.012	±25[3]	±2.5U, ±5B[4]		MIL		5-93
Low Cost, ADC80 Compatible	ADC80H-AH-12, (Q)	12	25	±0.012	±30	±3U typ, ±15B[5]	±2.5, ±5, ±10, +5, +10	Ind	32-pin DIP, Hermetic, Ceramic	5-64
Standard ADC80	ADC80AG-12	12	25	±0.012	±30	±3U typ, ±15B[5]	±2.5, ±5, ±10, +5, +10	Ind	32-pin DIP, Hermetic	5-56
High Speed	ADC84KG-12	12	10	±0.012	±30	±3U, ±15B typ[5]	±2.5, ±5, ±10 +5, +10	Com	32-pin DIP,	5-72
High Speed, Low Drift	ADC85-12, (Q)	12	10	±0.012	±15	±3U, ±7B typ[5]	±2.5, ±5, ±10, +5, +10	Ind	32-pin DIP, Hermetic, Metal	5-72
Serial Output, Small Package	ADC804BH, (Q)	12	17	±0.012	±30	±3U, ±15B typ[5]	±2.5, ±5, ±10, +5, +10	Ind	32-pin DIP, Hermetic, Ceramic	5-114
	ADC804SH, (Q)	12	17	±0.012	±30	±3U, ±15B typ[5]		Ind		5-114
Very High Speed	ADC803BM, (Q)	12	1.5	±0.020	±30	±7U, ±10B[5]	±5, ±10, −10 ±5, ±10, −10 ±5, ±10, −10	Ind	32-pin DIP, Hermetic, Metal	5-102
	ADC803CM, (Q)	12	1.5	±0.015	±30	±7U, ±10B[5]		Ind		5-102
	ADC803SM, (Q)	12	1.5	±0.015	±30	±7U, ±10B[5]		MIL		5-102
Wide Temp. −55°C to +200°C	ADC10HT	12	50	±0.012	±35	±2U, ±358[5]	±5, ±10, +10, +20	−55°C to +200°C	28-pin DIP, Hermetic, Ceramic	5-3

ULTRA-HIGH SPEED CONVERTERS

Analog-to-Digital	Model	Resolution (Bits)	Linearity Error, max (LSB)	Gain Drift, typ (ppm/°C)	Zero Drift, typ (ppm (FSR/°C)	Harmonic Distortion, DC to 1MHz	Sampling Rate	Temp Range [1]	Package	Page
Ultra-High Speed	ADC600K	12	1.25	±30	±50	70dB below FSR	10MHz	Com	Module	5-89

16-BIT ANALOG-TO-DIGITAL CONVERTERS

Description	Model[1]	Resolution (Bits)	Conversion Time, max (μsec)	Linearity Error, max (% of FSR)	Gain Drift, max (ppm/°C)	Zero Drift, max (ppm FSR/°C)	Input Ranges (V)	Temp Range[2]	Package	Page
High Resolution, High Accuracy	ADC73J	16	170	±0.0015	±10	±2U, ±5B[5]	±5, ±10, +10, +20	Com	Module	5-29
	ADC73K	16	170	±0.00075	±10	±2U, ±5B[5]		Com	Module	5-29
	ADC731J	16	170	±0.0015	±10	±2U, ±5B[5]	±5, ±10, +10, +20	Com	Module	5-29
	ADC731K	16	170	±0.00075	±10	±2U, ±5B[5]		Com	Module	5-29
High Resolution, Industry Standard Pinout	ADC71JG	16	50	±0.006	±15	±4U, ±10B[5]	±2.5, ±5, ±10, +5, +10, +20	Com	32-pin DIP, Ceramic	5-13
	ADC71KG	16	50	±0.003	±15	±4U, ±10B[5]		Com		5-13
	ADC72AM	16	50	±0.006	±15	±2U, ±10B[5]	±2.5, ±5, ±10, +5, +10, +20	Ind	32-pin DIP, Hermetic, Metal	5-21
	ADC72BM	16	50	±0.003	±15	±2U, ±10B[5]		Ind		5-21
	ADC72JM	16	50	±0.006	±20	±4U, ±10B[5]		Com		5-21
	ADC72KM	16	50	±0.003	±20	±4U, ±10B[5]		Com		5-21
	ADC76JG	16	15	±0.006	±15	±4U, ±10B[5]	±2.5, ±5, ±10 ±2.5, ±5, ±10	Com	32-pin DIP, Ceramic	5-40
	ADC76KG	16	15	±0.003	±15	±4U, ±10B[5]		Com		5-40
Military	See Military Products, section 12.									

NOTES: (1) "Q" indicates product available with screening for enhanced reliability. See High Reliability Screening, section 12. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) Full Scale Drift. (4) U = Unipolar Zero Drift, B = Bipolar Offset Drift. For ADC574A and ADC674A only, Bipolar Offset is defined at Bipolar Zero; that is, at 0V − ½LSB, rather than the more conventional definition at −Full Scale + 1/2LSB. (5) U = Unipolar Zero Drift, B = Bipolar Offset Drift.

PCM ANALOG-TO-DIGITAL CONVERTERS

Description	Model	Resolution (Bits)	Total Harmonic Distortion	Conversion Time, max (μsec)	Input Range (V)	Temp Range [1]	Dynamic Range (dB)	Package	Page
PCM Audio A/D Converter	PCM75KG	16	0.02% at −15dB	17	±2.5, ±5, ±10	Com	90	32-pin DIP, Ceramic	5-122
	PCM75JG	14[2]	0.05% at −15dB	15	±2.5, ±5, ±10	Com	90		5-122

NOTES: (1) Com = 0 to +70°C. (2) Can be operated at 16 bits.

BURR-BROWN®

ADC10HT

A Wide Temperature Range General Purpose 12-Bit ANALOG-TO-DIGITAL CONVERTER

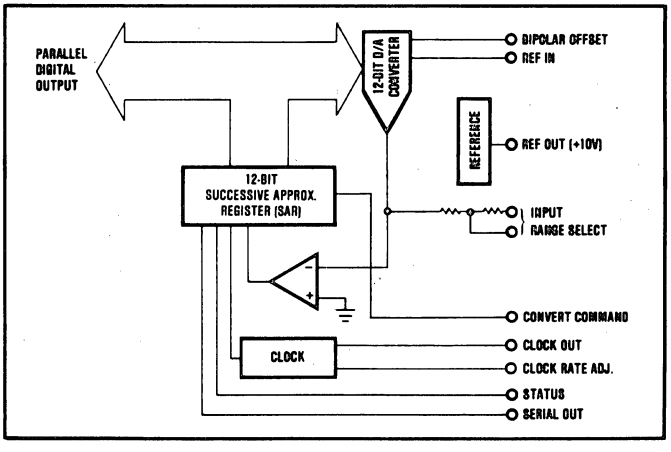
FEATURES

- -55° C to +200°C SPECIFICATIONS
- FULL 12-BIT RESOLUTION
- 50μsec MAX CONVERSION TIME
- NO MISSING CODES OVER FULL TEMPERATURE RANGE
- COMPLETE WITH INTERNAL CLOCK AND REFERENCE VOLTAGE
- SERIAL OUTPUT DATA AVAILABLE
- TTL AND +5V CMOS COMPATIBLE
- DUAL-WIDTH HERMETIC CERAMIC PACKAGE
- LOW POWER OPERATION WITH EXTERNAL REFERENCE (250mW)

DESCRIPTION

You'll find this general purpose, 12-bit, successive approximation A/D converter ideally qualified for circuits that must operate over wide temperature ranges. The ADC10HT incorporates state-of-the-art IC and laser-trimmed thin-film components. It is complete with an internal clock and reference voltage. Internal scaling resistors allow bipolar input voltage ranges of ±5V and ±10V. A pin is provided for serial output data. The ADC10HT is contained in a compact, dual width, 28-pin ceramic DIL package.

To assure consistent performance, 100% screening procedures are conducted on the ADC10HT at key points during its manufacture. Burn-in and temperature cycling are examples. A clean-room environment is maintained for assembly operations.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at rated power supply voltages and T_A = +25°C unless otherwise noted.

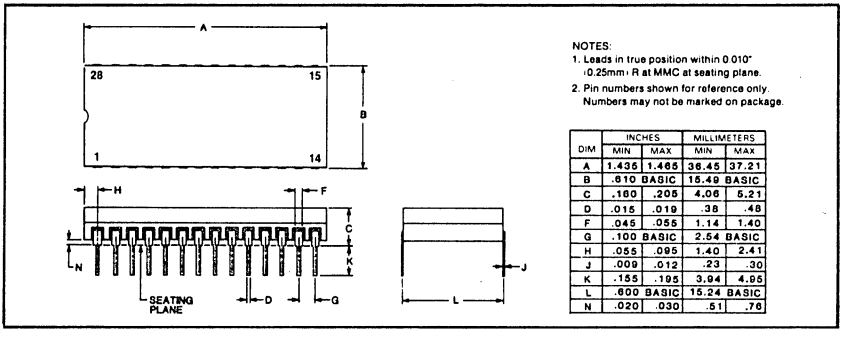
MODEL	ADC10HT			UNITS
	MIN	TYP	MAX	
RESOLUTION	12			Bits
INPUT				
ANALOG				
Voltage Ranges				
Unipolar		0 to +10, 0 to +20		V
Bipolar		±5, ±10		V
Impedance (direct input)				
0 to +10V, ±5V		5		kΩ
0 to +20V, ±10V		10		kΩ
DIGITAL(1)				
Convert Command Logic Loading		1		CMOS Load
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error(2)		±0.05	±0.2	%
Offset Error(2)				
Unipolar		±0.05	±0.2	% of FSR(3)
Bipolar		±0.05	±0.2	% of FSR
Linearity Error			±0.012	% of FSR
Inherent Quantization Error		±1/2		LSB
Differential Linearity Error		±0.012	±0.024	% of FSR
Total Unadjusted Error(4)				
+25°C		±0.10	±0.40	% of FSR
-55°C to +200°C		±0.30	±1.00	% of FSR
Total Adjusted Error(5)				
+25°C		±0.006	±0.012	% of FSR
-55°C to +200°C		±0.20	±0.60	% of FSR
Total Unadjusted Error(6)				
Exclusive of Reference				
+25°C		±0.10	±0.40	% of FSR
-55°C to +200°C		±0.20	±0.80	% of FSR
Total Adjusted Error(7)				
Exclusive of Reference				
+25°C		±0.006	±0.012	% of FSR
-55°C to +200°C		±0.15	±0.40	% of FSR
CONVERSION TIME		30	50	μsec
DRIFT (-55°C ≤ T_A ≤ +200°C)				
Gain				
With Internal Reference		±15	±35	ppm/°C
Exclusive of Reference		±5	±10	ppm/°C
Offset				
Unipolar		±2		ppm of FSR/°C
Bipolar				
With Internal Reference		±10	±35	ppm of FSR/°C
Exclusive of Reference		±4	±10	ppm of FSR/°C
Linearity		±0.5	±1.5	ppm of FSR/°C
No Missing Codes (Temp. Range				
-55°C to +200°C	12			Bits
OUTPUT				
DIGITAL DATA				
Parallel				
Output Codes(8)				
Unipolar		SB		
Bipolar(9)		OB, TC		
Output Drive	1			LSTTL Loads
Serial Data Code (NRZ) - SB, OB		SB, OB		
Output Drive	1			LSTTL Loads
Status		Logic "1" During Conversion		
Status Output Drive	1			LSTTL Loads
Internal Clock				
Output Drive	1			LSTTL Loads
Frequency		400		kHz

ELECTRICAL (CONT)

MODEL	ADC10HT			
	MIN	TYP	MAX	UNITS
POWER SUPPLIES AND REFERENCE				
Rated Voltage, V_{CC}	±14.5	±15	±15.5	VDC
V_{DD}	+4.75	+5	+5.25	VDC
Supply Drain, $+V_{CC}$ (10)		+15		mA
$-V_{CC}$ (10)		-30		mA
V_{DD}		+16		mA
Power Supply Sensitivity				
$\pm V_{CC}$		0.01	0.1	% of FSR/%V_{CC}
V_{DD}		0.01	0.1	% of FSR/%V_{DD}
Internal Reference Voltage	9.990	10.0	10.010	V
Max External Current with no Degradation of Specs		2		mA
Temperature Coefficient		±10		ppm/°C
TEMPERATURE RANGE				
Specification	-55		+200	°C
Operating	-55		+200	°C
Storage	-65		+210	°C

NOTES:
1. +5V CMOS compatible. Input current (low to high state) = 1μA max. Use pull-up resistor when driving convert command from TTL
2. Adjustable to zero (see Table II and Figures 5 and 6).
3. FSR means Full Scale Range. For example, unit connected for ±10V has a 20V FSR.
4. Includes Gain, Offset, and Linearity Errors (Bipolar Mode).
5. Gain and Offset Errors removed at +25°C (Bipolar Mode).
6. Includes Gain, Offset, and Linearity Errors with external +10.0V ±1mV reference, does not include Reference Drift (Bipolar Mode)
7. Gain and Offset Errors removed at +25°C with external +10.0V ±1mV reference, does not include Reference Drift (Bipolar Mode)
8. See Table I. SB - Straight Binary, OB - Offset Binary, TC - Two's Complement.
9. TC coding obtained by using $\overline{MSB}$ (pin 13) instead of MSB (pin 12).
10. May be reduced. See Low Power Operation.

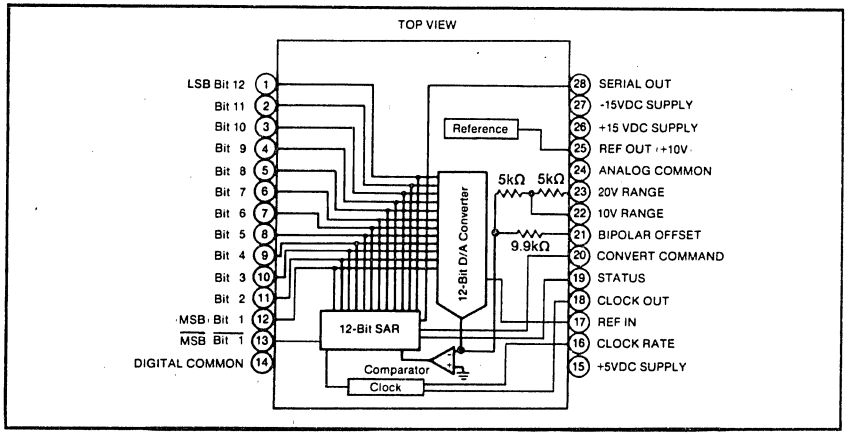
MECHANICAL



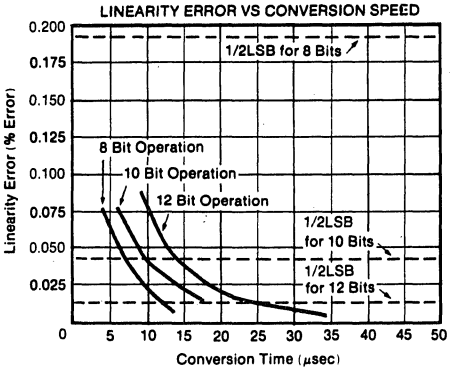
NOTES:
1. Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
2. Pin numbers shown for reference only. Numbers may not be marked on package.

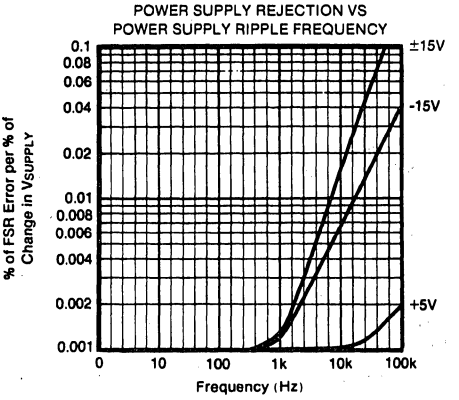
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	.38	.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.055	.095	1.40	2.41
J	.009	.012	.23	.30
K	.155	.195	3.94	4.95
L	.600 BASIC		15.24 BASIC	
N	.020	.030	.51	.76

CONNECTION DIAGRAM



TYPICAL PERFORMANCE CURVES





DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over range of the A/D converter is 1LSB, ±1/2LSB.

The ADC10HT is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also specifies that this converter will have no missing codes over the full operating temperature range.

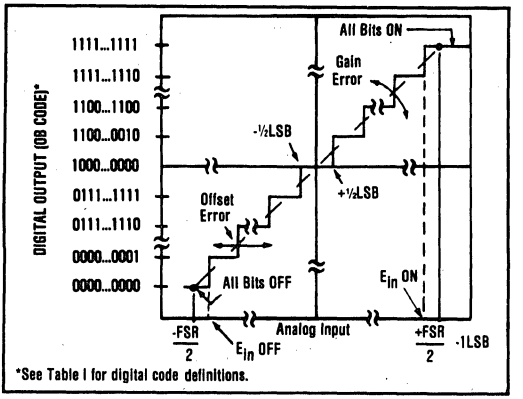


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 0110 0111 0110 exists.

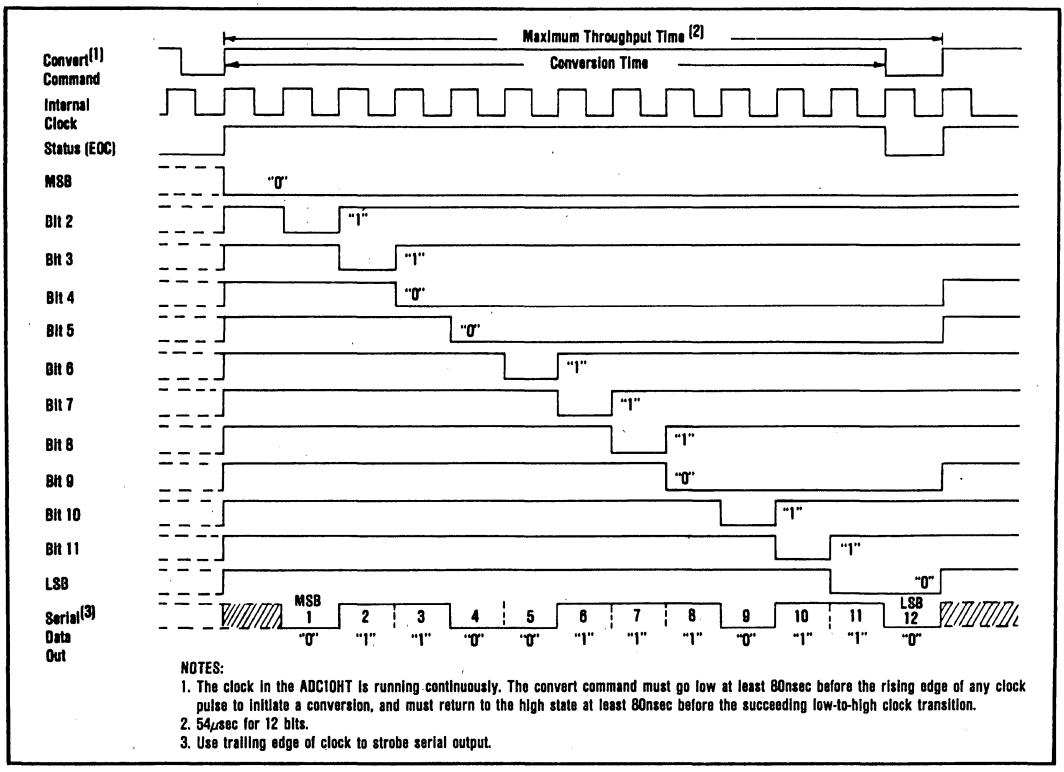


FIGURE 2. ADC10HT Timing Diagram.

DEFINITION OF DIGITAL CODES

Parallel Data

Two binary codes are available on the ADC10HT parallel output; they are straight binary (SB) for unipolar input signal ranges and offset binary (OB) for bipolar input signal ranges. Two's complement (TC) may be obtained by using $\overline{\text{MSB}}$ (pin 13).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 8-, 10- and 12-bit resolutions. Figure 3 shows the connections for 12-bit resolution, parallel data output, with ±10V input.

Serial Data

Two straight binary codes are available on the serial output line; they are SB and OB. The serial data is available only during conversion and appears with the MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the TC code.

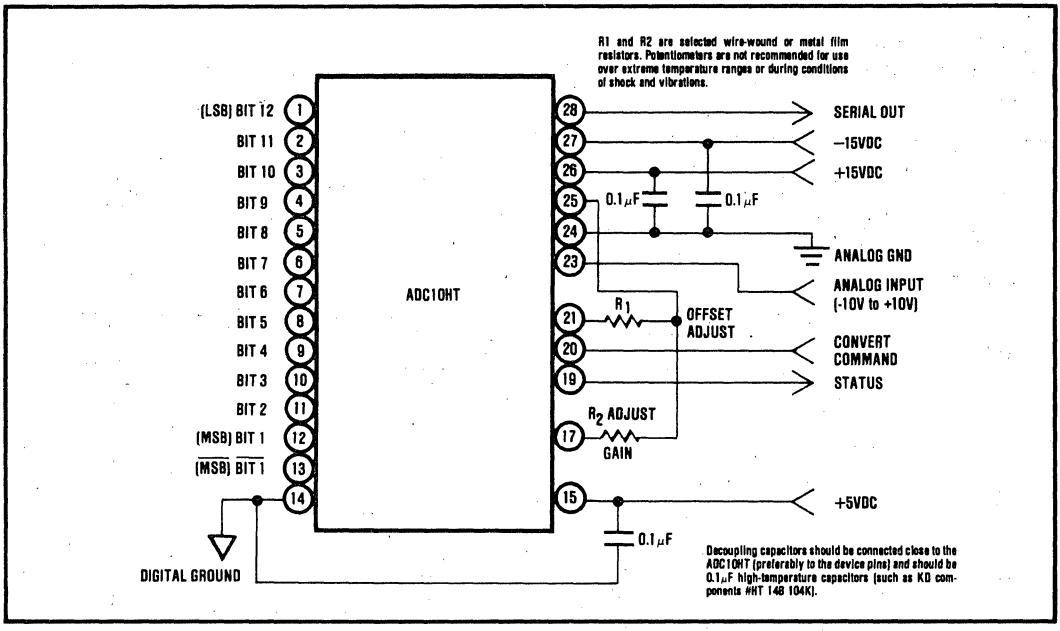


FIGURE 3. ADC10HT Connections for ±10V Analog Input, 12-Bit Resolution, and Serial or Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	Defined As:	±10V	±5V	0 to +10V	0 to +20V
Code Designation		OB(1) or TC(2)	OB(1) or TC(2)	SB(3)	SB(3)
One Least Significant Bit (LSB)	$FSR/2^n$	$20V/2^n$	$10V/2^n$	$10V/2^n$	$20V/2^n$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n = 10	19.53mV	9.77mV	9.77mV	19.53mV
	n = 12	4.88mV	2.44mV	2.44mV	4.88mV
Transition Values					
MSB LSB					
111...111(4)	+Full Scale	+10V - 3/2LSB	+5V - 3/2LSB	+10V - 3/2LSB	+20V - 3/2LSB
100...000	Mid Scale	0	0	+5V	+10V
000...001	-Full Scale	-10V + 1/2LSB	-5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

NOTES:
(1)OB = Offset Binary
(2)TC = Two's Complement - obtained by inverting the most significant bit. $\overline{MSB}$ (pin 13)
(3)SB = Straight Binary
(4)Voltages given are the nominal value for transition to the code specified

DISCUSSION OF SPECIFICATIONS

The ADC10HT is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion-speed effects on accuracy. This ADC is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory trimmed to typically ±0.05% of FSR at 25°C. These errors may be trimmed to zero as shown in Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC10HT power supply sensitivity is specified for ±0.01% of FSR/%V_{CC} for ±15V supplies and ±0.01% of FSR/%V_{DD} for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 4.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC10HT but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with high temperature mica or teflon capacitors as shown in Figure 4 to obtain noise free operation. These capacitors should be located close to the ADC.

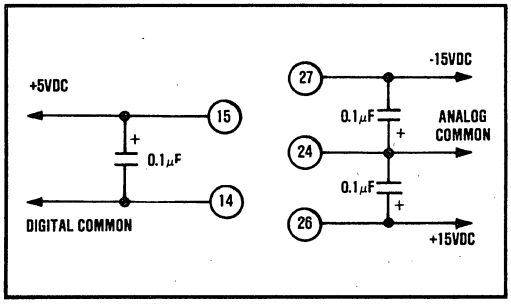


FIGURE 4. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 5 for circuit details.

TABLE II. ADC10HT Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 21 To Pin	Connect Pin 23 To	Connect Input Signal To Pin
±10V	OB or TC*	25**	Input Sig.	23
±5V	OB or TC*	25**	Open	22
0 to +10V	SB	Open	Open	22
0 to +20V	SB	Open	Input Sig.	23

*Obtained by using $\overline{MSB}$ (pin 13)

** If optional offset adjustment is not used connect a 25Ω ±0.1% resistor from pin 21 to pin 25 to obtain specified gain and offset errors.

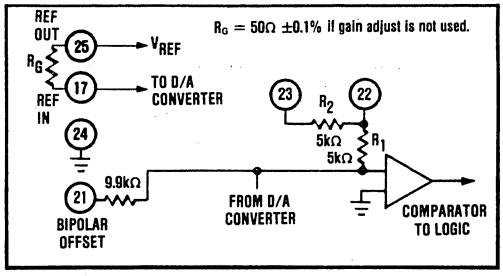


FIGURE 5. ADC10HT Input Scaling Circuit.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

A connection diagram for the ADC10HT in the ±10V input bipolar mode of operation is shown in Figure 3. The gain and offset adjustment resistors (R1 and R2) should be selected discrete metal-film or wirewound resistors and not potentiometers if optimum performance is required under high shock and vibration levels. The internal gain and offset errors are laser trimmed to within a maximum error of ±0.2% with 50Ω, 0.1% resistors in place of R1 and R2. Another possible approach in many applications is to simply remove the offset and gain errors with digital techniques after the A/D conversion has taken place. This approach can virtually eliminate the need for initial gain and offset adjustment and even the effects of gain and offset drift with time and temperature can often be removed. In some cases it may be desirable to use potentiometers.

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer or resistance substitution boxes as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all bits off E_{IN}^{OFF}.

Adjust the Offset potentiometer or resistor substitution boxes until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

GAIN - Connect the Gain adjust potentiometer or resistor substitution boxes as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

It is also possible to make the adjustments just described with potentiometers and then replace the resistive arms with discrete metal film or wire-wound resistors in order to make a system more rugged before subjecting it to harsh environments.

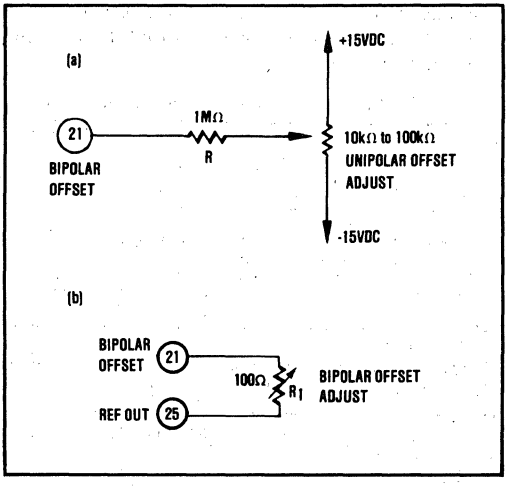


FIGURE 6. Optional Unipolar and Bipolar Offset Adjust Circuitry with ±0.4% of FSR Range of Adjustment.

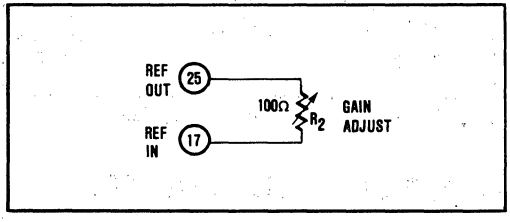


FIGURE 7. Optional Gain Adjust with ±0.4% Range of Adjustment.

CLOCK RATE CONTROL (OPTIONAL)

Faster Conversion

If adjustment of the clock rate is desired for faster conversion times, a resistor may be connected between Clock Rate (pin 16) and Clock Out (pin 18) as shown in Figure 8.

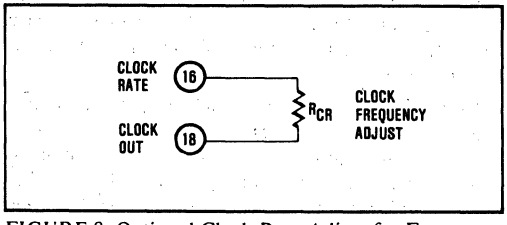


FIGURE 8. Optional Clock Rate Adjust for Faster Conversion Times.

Figure 9 shows the effect of clock rate control resistor (R_{CR}) on clock frequency. Figure 9 is based on a typical initial clock frequency of about 400kHz (conversion time of 30μsec for 12 bits). To determine the required clock frequency:

$$f_{clock} = \frac{\text{Bit Resolution}}{\text{Conversion Time}}$$

For example, if the ADC10HT is short cycled to 10-bit operation and a conversion time of 20μsec is required, then

$$f_{clock} = \frac{10}{20\mu\text{sec}} = 500\text{kHz}$$

from Figure 9 a clock rate resistor (R_{CR}) of about 40kΩ is required.

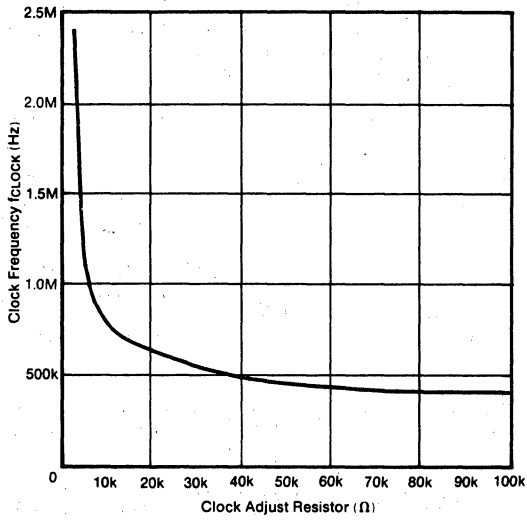


FIGURE 9. Clock Frequency vs Clock Rate Control Resistor (R_{CR}).

Slower Conversion

The conversion time can be decreased by connecting a capacitor from the Clock Rate pin to Digital Common (see Figure 10).

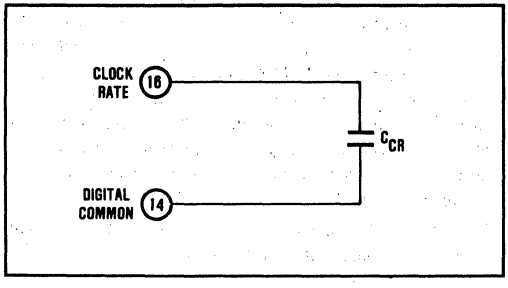


FIGURE 10. Optional Clock Rate Adjust for Slower Conversion Times.

Figure 11 shows the effect of the clock rate control capacitor on the clock frequency.

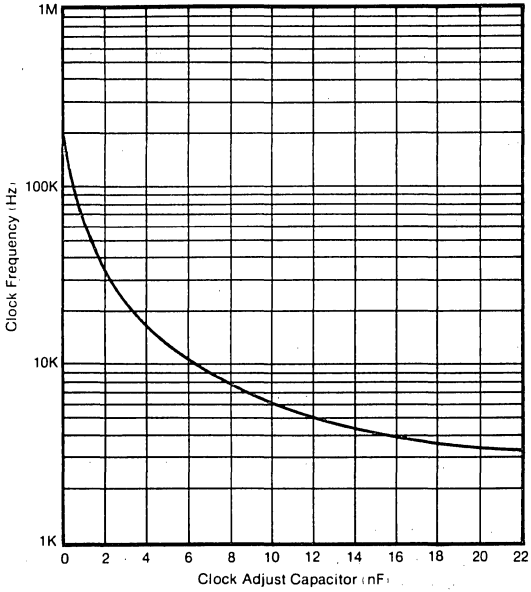


FIGURE 11. Clock Frequency vs Clock Rate Control Capacitor (C_{CR}).

The serial output data (pin 28) is synchronous with the internal clock. In some applications the clock frequency must be lowered to 3kHz or 4kHz so that the data can be transmitted over long distances. If 12-bit resolution is required, the conversion time for 4kHz is

$$\text{conversion time} = \frac{12 \text{ bits}}{4\text{kHz}} = 3\text{msec}$$

From Figure 11, a clock rate control capacitor, C_{CR}, of approximately 16nF is required.

In applications requiring such a slow conversion time, a low-pass filter should be used at the analog input to the ADC10HT.

SHORT-CYCLE AND CONTINUOUS CONVERSION OPERATION.

The ADC10HT may be operated at faster speeds for resolutions less than 12 bits by using the clock rate control feature. The conversion time can be further increased by using the short cycle circuit shown in Figure 12. Without this circuit, the status signal (pin 19) will always remain high for 13 clock pulses even if only 8 bits are being used. By connecting the short cycle input of the NAND gate to the n + 1 bit (connect to bit 9 for 8-bit operation, for example) the conversion will be completed and the status signal will go low after n + 1 clock pulses (9 pulses for 8-bit operation). It should be noted that with the circuit shown in Figure 12, the ADC10HT will operate in a continuous conversion mode, i.e., a new conversion will start on the n + 2 clock pulse without the need for an external convert command.

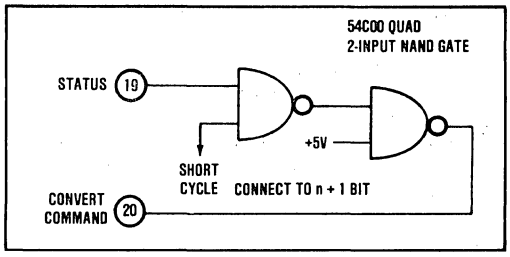


FIGURE 12. Short-Cycle Circuit which Provides for Lower Resolutions than 12 Bits with Faster Conversion Times and Continuous Conversions.

Table III indicates where to connect the short cycle input for 8-bit and 10-bit resolution and gives possible conversion time(s) obtainable by using this feature along with the clock rate pin.

TABLE III. Short Cycle Connections and Specifications for 8 to 12 Bit Resolutions.

Resolution (Bits)		12	10	8
Connect SHORT CYCLE to:		N/A	Pin 2	Pin 4
Conversion Time (μsec)(1)		24	10	6
Nonlinearity at +25°C (% of FSR)	ADC10HT	±0.012	±0.048	±0.1
	ADC10HT-1	±0.048	±0.048	±0.1

NOTE: (1) Adjust Conversion Time with Clock Rate Control resistor as shown in Figures 8 and 9.

For 12-bit operation and continuous conversion, simply connect status (pin 19) directly to convert command (pin 20).

OUTPUT DRIVE

Normally the ADC10HT logic outputs will drive two low power TTL loads or one LSTTL load. If long digital lines must be driven, external logic buffers are recommended. The digital outputs are connected directly to the internal CMOS successive-approximation-register and can drive +5V CMOS without the need for pull-up resistors.

HEAT DISSIPATION

The ADC10HT dissipastes approximately 750mW and the package has a case-to-case ambient thermal resistance (θ_{CA}) of 35°C/W. For optimum performance at +200°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the package can be achieved by using a silicone heat-sink compound.

LOW POWER OPERATION

The typical supply currents required by the ADC10HT under normal operating conditions are 15mA (+15V), 30mA (-15V), and 16mA (+5V). The average power required (P_D) is therefore

$P_D = |15\text{mA} \times 15\text{V}| + |30\text{mA} \times -15\text{V}| + |16\text{mA} \times 5\text{V}| = 755\text{mW}$.

Under certain operating conditions this power consumption can be reduced to as little as 250mW.

The ADC10HT is completely self-contained with an internal +10V reference voltage. The +15V supply is used only to supply power for the op amp current source and zener diode used in this reference. If an external reference is available, the +15V supply is not required and it can be removed. This reduces the P_D by 15mA x 15V = 225mW. The average P_D for the ADC10HT is therefore reduced to 530mW.

The major contributor to the power consumption is the -15V supply. As long as a +10V reference is used, the V- supply voltage must be between -13V and -16V. If, however, a lower voltage reference is used, this V- supply voltage can be reduced considerably which greatly reduces the power consumption. Lowering the reference voltage will, of course, lower the full scale input voltage by a proportional amount. For example, if the reference voltage is +5V, the full scale input voltage for the 10V range input (pin 22) will be +5V, instead of +10V with a +10V reference, in the unipolar mode of operation. Table IV indicates the minimum supply voltages and the typical power consumption obtained when using these supply voltages for various values of V_{REF}.

TABLE IV. Minimum Power Supply Voltages and Typical Power Consumption for Operation with External V_{REF}. (Note: +15V is not required if internal V_{REF} is not used.)

External V_{REF}	V_{DD} Logic (Pin 15)	$-V_{CC}$ (Pin 27) (Minimum)	Total Power Consumption (Typical)
+10V	+5V	-13V	470mW
+6.3V	+5V	-10V	300mW
+5V	+5V	-8V	250mW

LOW-POWER EXTERNAL REFERENCE

A simple external reference voltage can be made with a single resistor and a zener diode as shown in Figure 13. The power consumed by the reference is only about 75mW with $+V_{CC} = +10V$. The power supply sensitivity of this reference is approximately ±0.02% of FSR/%V_{CC}.

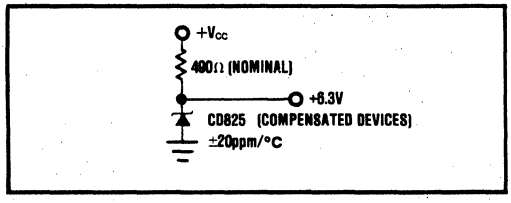


FIGURE 13. Simple +6.3V External Reference That Requires Only 75mW.

A very simple procedure can be used to obtain the lowest possible drift with this reference. First, vary the zener current from about 4mA to 11mA by changing either the bias voltage, $+V_{CC}$, or bias resistor, R_B, and plot V_Z versus I_Z as shown in figure 14. Next, heat the zener (the exact temperature is not important, but it should be near the desired operating temperature), and repeat the procedure. The point where the two curves cross is the zero-temperature-coefficient bias current. $+V_{CC}$ and/or R_B should then be adjusted accordingly for this optimum operating current.

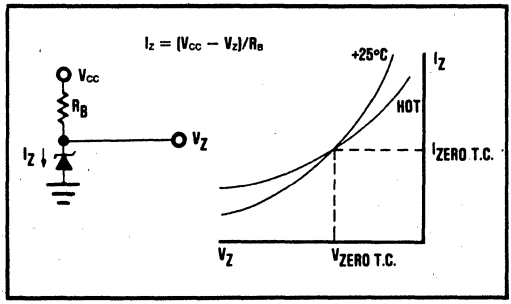


FIGURE 14. Simple Techniques for Obtaining a Low Drift Reference Voltage.

This procedure is also discussed in a Burr-Brown Application Note: "Squeeze High Performance out of Low-Cost Hybrid Data Converters, AN-86.

Other Application Notes

Burr-Brown also has other Application Notes of interest to the converter user. In particular:

"What Designers Should Know About Data Converter Drift," AN-89.

"Correcting Errors Digitally in Data Acquisition and Control," AN-101.

OPERATION WITH EXTERNAL CLOCK

Figure 15 shows the internal clock circuit of the ADC10HT. To operate with an external clock, first connect the Clock Rate Control (pin 16) to ground. This will shut off the internal clock and also turn off the open collector output transistor of the LM119 comparator. The Clock Out (pin 18) will then be in a "high" state (+5V) because of the 2kΩ pull-up resistor to +5V. Now simply use the Clock Out pin for the external clock input. Note that the external clock must have the capability of sinking 2.5mA when it is in the low state due to the 2kΩ pull-up resistor.

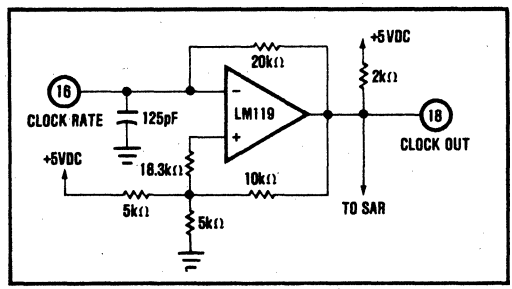


FIGURE 15. ADC10HT Internal Clock.

BURR-BROWN®

ADC71

16-Bit Hybrid
ANALOG-TO-DIGITAL CONVERTER

FEATURES:

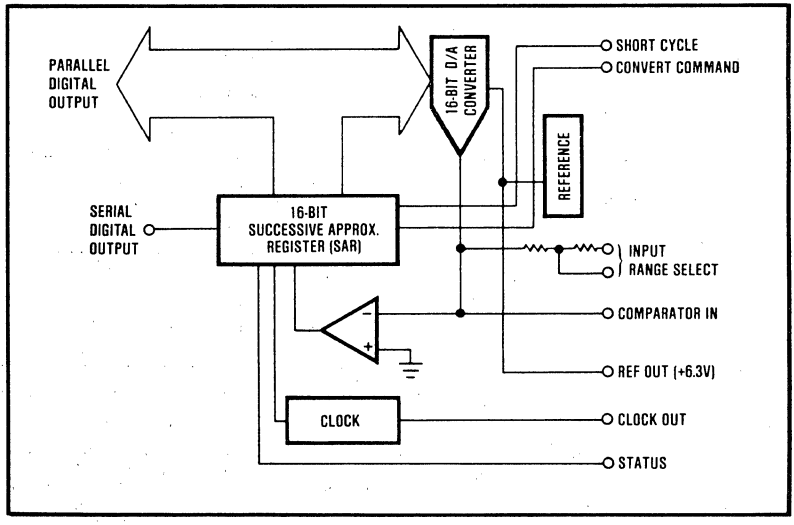
- 16-BIT RESOLUTION
- LINEARITY ERROR ±0.003%
- COMPACT DESIGN
  32-Pin Ceramic Package
- FAST CONVERSION SPEED
- LOW COST

DESCRIPTION

The ADC71 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The ADC71 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a convenient 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, and thin-film scaling resistors, which allows selection of analog input ranges of ±2.5V, ±5.0V, ±10.0V, 0 to +5.0V, 0 to +10V and 0 to +20V.

Data is available in parallel and serial form with corresponding clock and status output. All digital input and outputs are TTL compatible.

Power supply voltages are ±15VDC and +5VDC.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

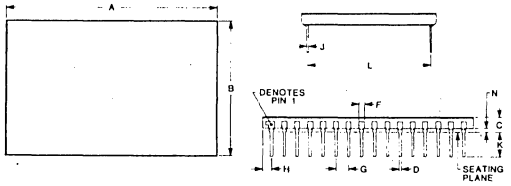
At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC71KG			ADC71JG			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
ANALOG INPUTS							
Voltage Ranges: Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10, 0 to +20			0 to +5, 0 to +10, 0 to +20		V
Impedance (Direct Input): 0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL INPUTS[1]							
Convert Command	Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading			1			1	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error		±0.1[2]	±0.2		±0.1[2]	±0.2	%
Offset: Unipolar		±0.05[2]	±0.1		±0.05[2]	±0.1	% of FSR[3]
Bipolar		±0.1[2]	±0.2		±0.1[2]	±0.2	% of FSR
Linearity Error			±0.003			±0.006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.003			±0.003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			0.003		% of FSR/%V_{CC}
+5VDC		0.001			0.001		% of FSR/%V_{CC}
CONVERSION TIME[4]							
14 Bits			50			50	μs
15 Bits			53.3			53.3	μs
16 Bits			56.7			56.7	μs
WARM-UP TIME	5			5			min
DRIFT							
Gain			±15			±15	ppm/°C
Offset: Unipolar		±2	±4		±2	±4	ppm of FSR/°C
Bipolar			±10			±10	ppm of FSR/°C
Linearity		±2	±3		±2	±3	ppm of FSR/°C
No Missing Codes Temp Range: KG (14-bit)	+10		+40				°C
JG (13-bit)				0		50	°C
OUTPUT							
DIGITAL DATA							
(All codes complementary)							
Parallel: Output Codes[5]							
Unipolar			CSB				
Bipolar			COB, CTC[6]				
Output Drive			2				TTL Loads
Status			Logic "1" during conversion				
Status Output Drive			2			2	TTL Loads
Internal Clock: Clock Output Drive			2			2	TTL Loads
Frequency		280			280		kHz
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Max External Current with No Degradation of Specs			±200			±200	μA
Temp Coefficient			±10			±10	ppm/°C
POWER SUPPLY REQUIREMENTS							
Power Consumption		550			550		mW
Rated Voltage: Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain: +15VDC		+15			+15		mA
−15VDC		−18			−18		mA
+5VDC		+10			+10		mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (derated specs)	−25		+85	−25		+85	°C
Storage	−55		+125	−55		+125	°C

NOTES: (1) DTL/TTL compatible, i.e., Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V, max. Logic "1" = 2.4V, min. (2) Adjustable to zero. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution; see "Additional Connections Required" section. (5) See Table I. CSB—Complementary Straight Binary, COB—Complementary Offset Binary, CTC—Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (Pin 1).

MECHANICAL

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	.180	.210	4.57	5.33
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.089	.106	2.26	2.69
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.900 BASIC		22.86 BASIC	
N	.015	.035	.38	.89

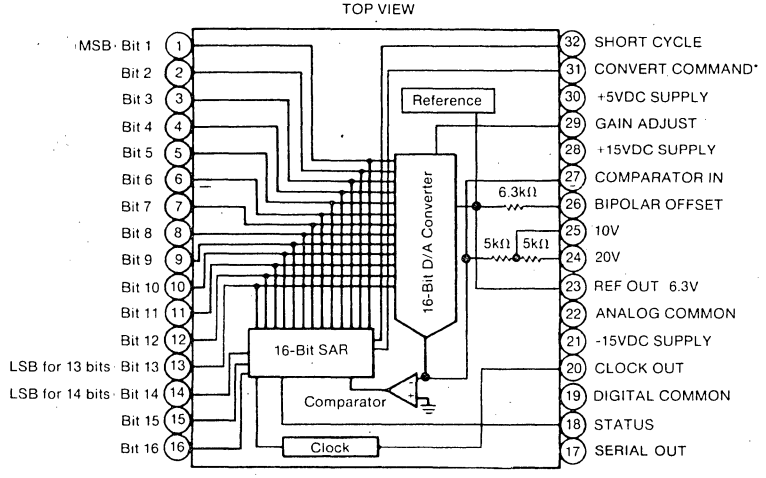


NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

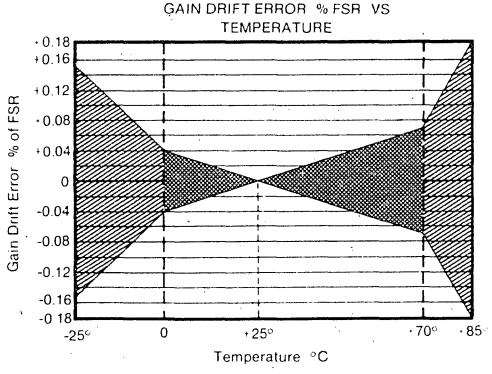
CASE: Ceramic
MATING CONNECTOR: 2302MC
WEIGHT: 13 grams (0.46 oz.)
HERMETICITY: Conforms to Method 1014, Condition C, Step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

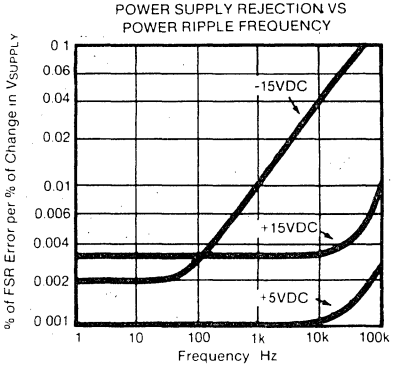
CONNECTION DIAGRAM



*If an external clock is used, connect the clock to pin 31 CONVERT COMMAND .

TYPICAL PERFORMANCE CURVES





DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2 LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

The ADC71 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that this converter will have no missing codes over a specified temperature range when short cycled for 14-bit operation.

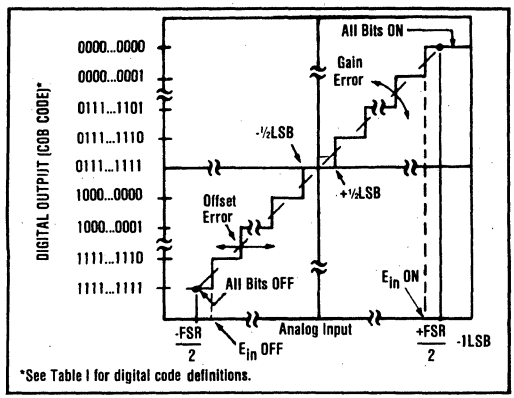


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram in Figure 2 assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output).

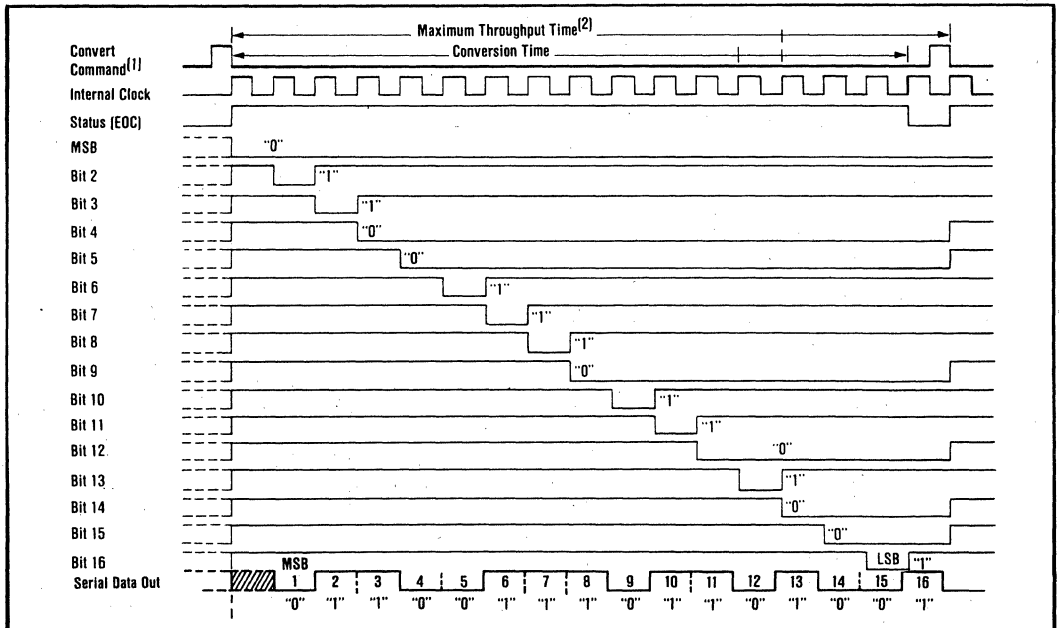


FIGURE 2. ADC71 Timing Diagram.

Figures 2a and 2b are timing diagrams showing the relationship of serial data to clock and valid data to status.

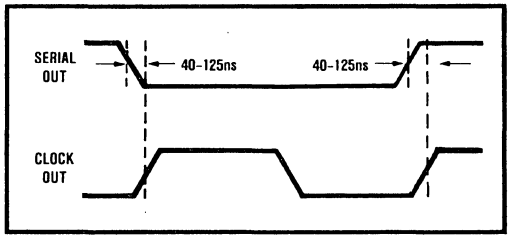


FIGURE 2a. Timing Relationship of Serial Data to Clock.

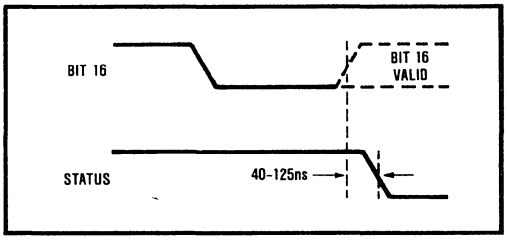


FIGURE 2b. Timing Relationship of Valid Data to Status.

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Two binary codes are available on the ADC71 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (Pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 3 shows the connections for 14-bit resolution, parallel data output, with ±10V input.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagrams of Figures 2 and 2a. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

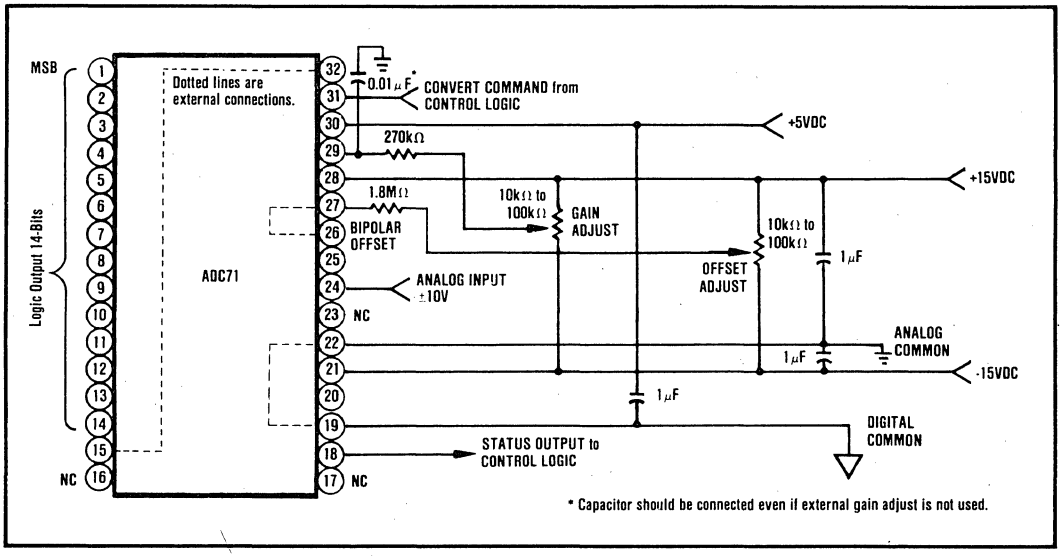


FIGURE 3. ADC71 Connections For: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
	n = 14	1.22mV	610μV	305μV	610μV	305μV	1.22mV
Transition Values							
MSB LSB							
000...000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

*COB = Complementary Offset Binary
**CTC = Complementary Two's Complement - obtained by inverting the most significant bit. MSB (Pin 1)
***CSB = Complementary Straight Binary
****Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC71 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC71 power supply sensitivity is specified for ±0.003% of FSR/%V_{CC}, for ±15V supplies and ±0.0015% of FSR/%V_{CC} for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 4.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC71 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (Pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum capacitors as shown in Figure 4 to obtain noise free operation. These capacitors should be located close to the ADC.

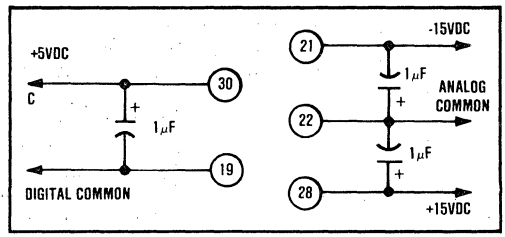


FIGURE 4. Recommended Power Supply Decoupling.

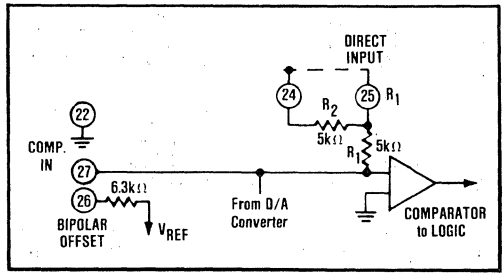


FIGURE 5. ADC71 Input Scaling Circuit.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 5 for circuit details.

TABLE II. ADC71 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB - Pin 1

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with .100ppm °C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and Pin 27 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

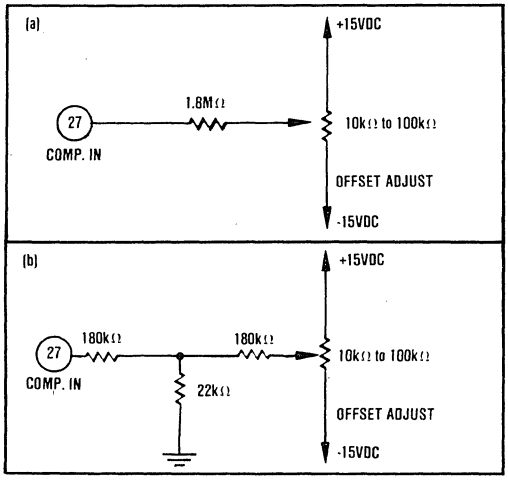


FIGURE 6. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range of Adjustment.

GAIN - Connect the Gain adjust potentiometer as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

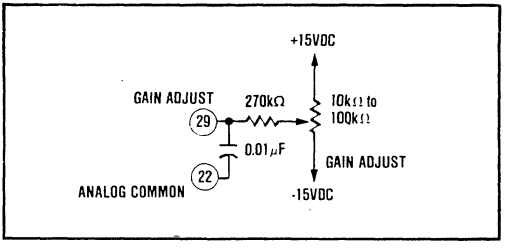


FIGURE 7. Connecting Optional Gain Adjust with a 0.2% Range of Adjustment.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

ADDITIONAL CONNECTIONS REQUIRED

The ADC71 may be operated at faster speeds for resolutions less than 14 or 13 bits, depending on the model selected, by connecting the Short Cycle Input, pin 32, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

TABLE III. Short Cycle Connections and Specifications for 12- to 14-Bit Resolutions.

Resolution Bits	14	13	12
Connect Pin 32 to	Pin 15	Pin 14	Pin 13
Maximum Conversion Speed μsec (1)	50	46.5	43
Maximum Nonlinearity at 25°C % of FSR	0.003(2)	0.006(3)	0.006(3)

NOTES: (1) Max. conversion time to maintain specified nonlinearity error. (2) ADC71KG only. (3) ADC71KG or ADC71JG.

OUTPUT DRIVE

Normally all ADC71 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

ORDERING INFORMATION

Model	Temperature	Package
ADC71KG	0°C to +70°C	Ceramic
ADC71JG	0°C to +70°C	Ceramic

BURR-BROWN®

ADC72

16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

FEATURES

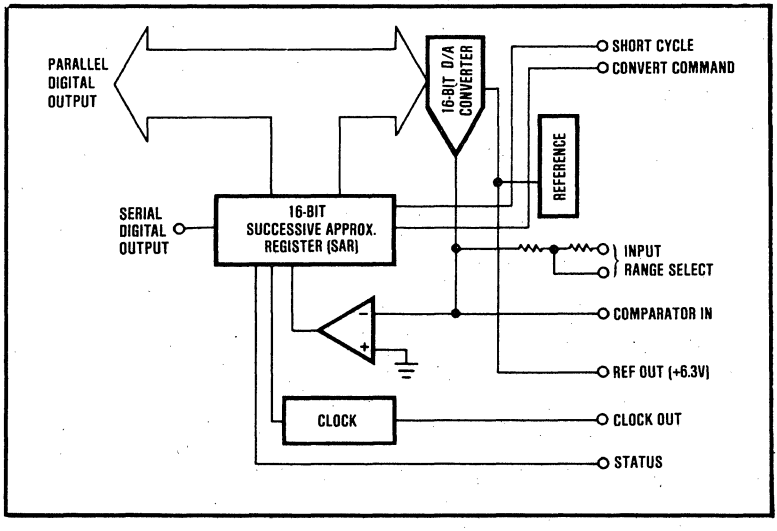
- 16-BIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- COMPACT DESIGN
  32-Pin Hermetic Metal Package
- FAST CONVERSION SPEED
  50μs Maximum
- LOW COST

DESCRIPTION

The ADC72 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. It uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a compact 32-pin metal dual-in-line package. The converter is complete with internal reference, clock, comparator, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Data is available in parallel and serial form with corresponding clock and status output. All digital input and outputs are DTL/TTL compatible.

Power supply voltages are ±15VDC and +5VDC.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

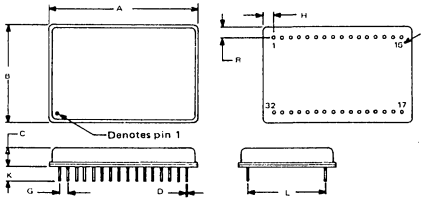
Typical at +25°C and rated power supplies unless otherwise noted.

MODEL	ADC72JM, KM			ADC72AM, BM			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
INPUT							
ANALOG							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10, 0 to +20			0 to +5, 0 to +10, 0 to +20		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL(1)							
Convert Command	Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading		1				1	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(2)		±0.1	±0.2		±0.1	±0.2	%
Offset Gain(2)							
Unipolar		±0.05	±0.1		±0.05	±0.1	% of FSR(3)
Bipolar		±0.1	±0.2		±0.1	±0.2	% of FSR
Linearity Error KM, BM			±0.003			±0.003	% of FSR
JM, AM			±0.006			±0.006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.003			±0.003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		±0.003			±0.003		% of FSR/%ΔVs
+5VDC		±0.001			±0.001		% of FSR/%ΔVs
CONVERSION TIME(4) (14 Bits)			50			50	μs
WARM-UP TIME	10			10			min
DRIFT							
Gain		±10	±20		±7	±15	ppm/°C
Offset							
Unipolar		±2	±4			±2	ppm of FSR/°C
Bipolar		±8	±10		±5	±10	ppm of FSR/°C
Linearity		±2	±3			±2	ppm of FSR/°C
No Missing Codes Temp Range							
JM, AM (13 bits)	0		+50	0		+50	°C
KM, BM (14 bits)	+10		+40	+10		+40	°C
OUTPUT							
DIGITAL DATA							
All codes complementary							
Parallel							
Output Codes(5)							
Unipolar			CSB				
Bipolar			COB, CTC(6)				
Output Drive			2				TTL Loads
Status			Logic "1" during conversion				
Status Output Drive			2			2	TTL Loads
Internal Clock							
Clock Output Drive			2			2	TTL Loads
Frequency		280			280		kHz
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Max External Current with No Degradation of Specs			±200			±200	μA
Temp Coefficient			±10			±5	ppm/°C
POWER SUPPLY REQUIREMENTS							
Power Consumption		550			550		mW
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Rated Voltage, Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain +15VDC		+15			+15		mA
Supply Drain -15VDC		−18			−18		mA
Supply Drain +5VDC		+10			+10		mA
TEMPERATURE RANGE							
Specification	0		+70	-25		+85	°C
Operating (derated specs)	-25		+85	-55		+85	°C
Storage	-55		+125	-55		+125	°C

NOTES:
1. DTL/TTL compatible, i.e., Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V, max. Logic "1" = 2.4V, min
2. Adjustable to zero.
3. FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR.
4. Conversion time may be shortened with "Short Cycle" set for lower resolution, see "Additional Connections Required" section.
5. See Table I. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.
6. CTC coding obtained by inverting MSB (Pin 1).

MECHANICAL

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56



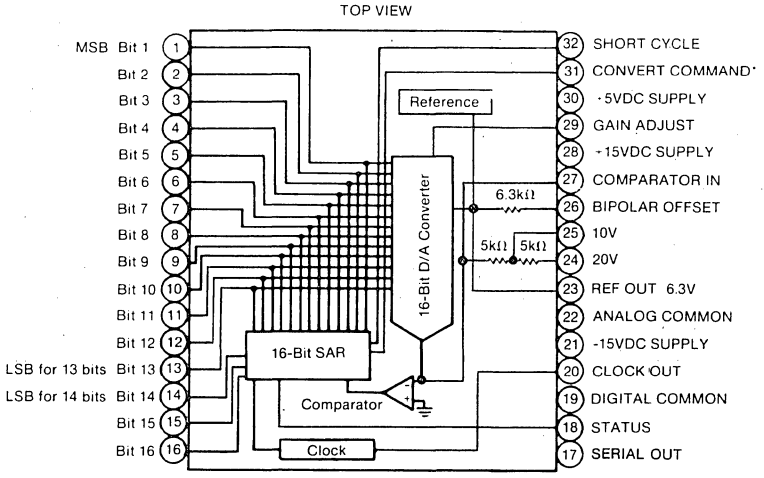
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

CASE: Nickel-plated kovar
MATING CONNECTOR: 2302MC
WEIGHT: 13 grams (0.46 oz.)

Contrasting glass seal or square corner denotes pin 1.

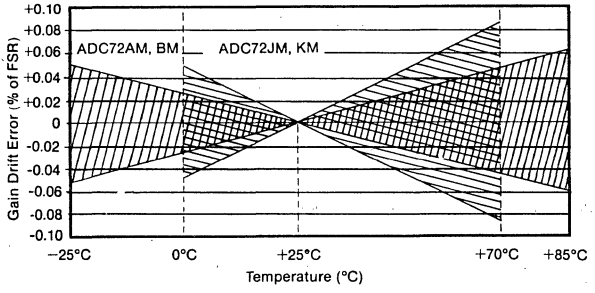
CONNECTION DIAGRAM



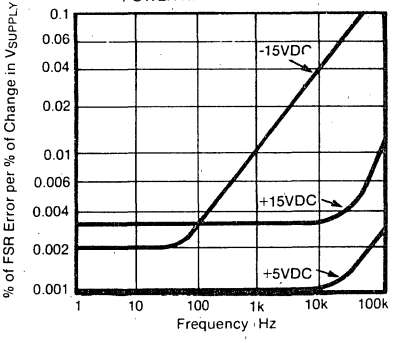
*If an external clock is used, connect the clock to pin 31 CONVERT COMMAND

TYPICAL PERFORMANCE CURVES

GAIN DRIFT ERROR (% OF FSR) VS TEMPERATURE



POWER SUPPLY REJECTION VS POWER RIPPLE FREQUENCY



DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A D converter is described by the transfer function shown in Figure 1. All successive approximation A D converters have an inherent Quantization Error of ±1 2 LSB. The remaining errors in the A D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

The ADC72 is also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that these converters will have no missing codes over a specified temperature range when short-cycled for 14-bit operation.

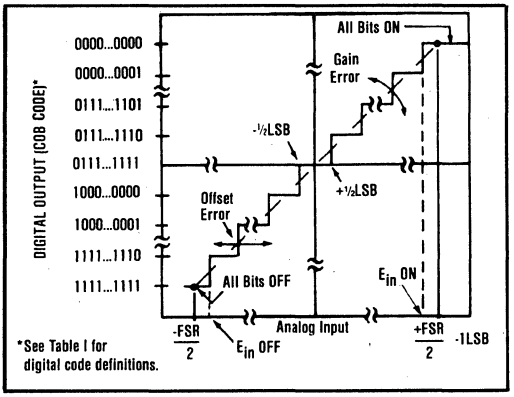


FIGURE 1. Input vs Output for an Ideal Bipolar A D Converter.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 2a and 2b are timing diagrams showing the relationship of serial data to clock and valid data to status.

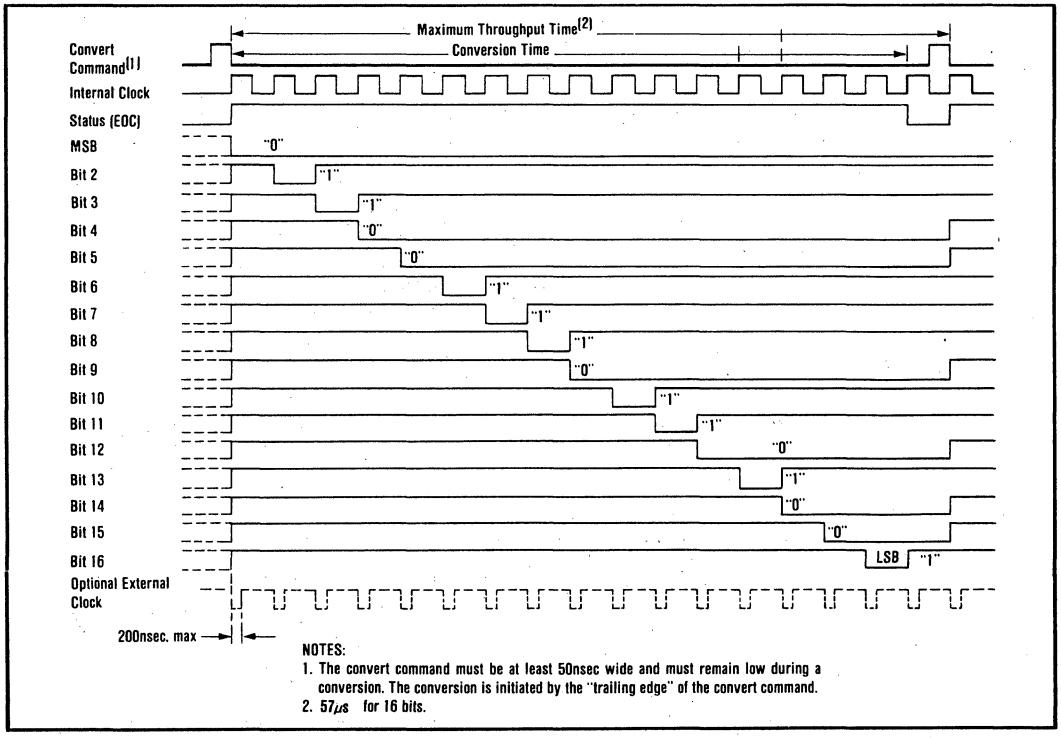


FIGURE 2. ADC72 Timing Diagram.

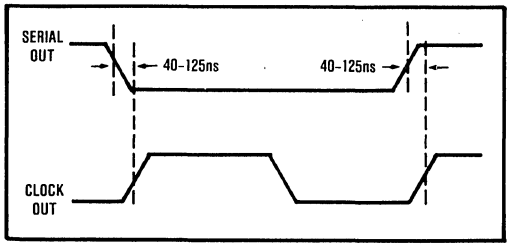


FIGURE 2a. Timing Relationship of Serial Data to Clock.

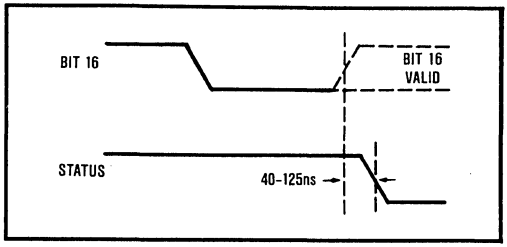


FIGURE 2b. Timing Relationship of Valid Data to Status.

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Two binary codes are available on the ADC72 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (Pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 3 shows the connections for 14-bit resolution, parallel data output, with ±10V output.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line: CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagrams of Figures 2 and 2a. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

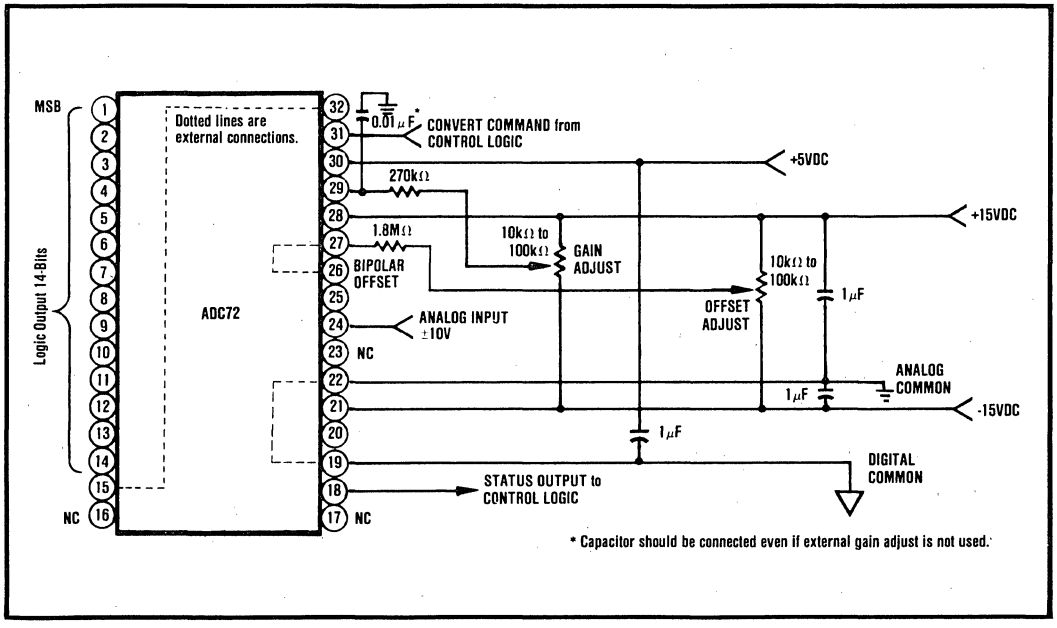


FIGURE 3. ADC72 Connections For: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary BIN Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit LSB	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
	n = 14	1.22mV	610μV	305μV	610μV	305μV	1.22mV
Transition Values MSB LSB							
000...000(4)	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

(1) COB = Complementary Offset Binary
(2) CTC = Complementary Two's Complement - obtained by inverting the most significant bit. MSB Pin 1
(3) CSB = Complementary Straight Binary
(4) Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC72 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC72 power supply sensitivity is specified for ±0.003% of FSR/%ΔV_S for ±15V supplies and ±0.001% of FSR/%ΔV_S for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 4.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC72 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF non-polarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (Pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

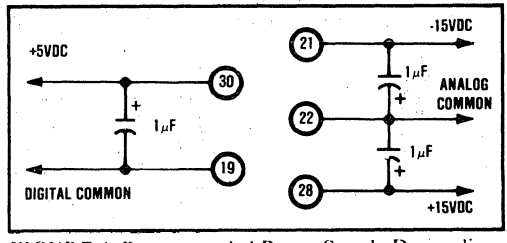


FIGURE 4. Recommended Power Supply Decoupling.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum capacitors as shown in Figure 4 to obtain noise free operation. These capacitors should be located close to the ADC.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 5 for circuit details.

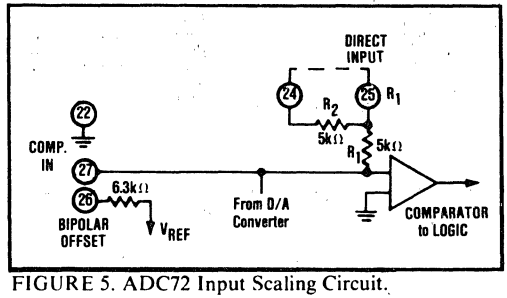


FIGURE 5. ADC72 Input Scaling Circuit.

TABLE II. ADC72 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB Pin 1

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and Pin 27 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 6. **Sweep the input through the end point transition voltage that should cause an output transition to all bits Off (E_{IN}^{OFF}).**

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

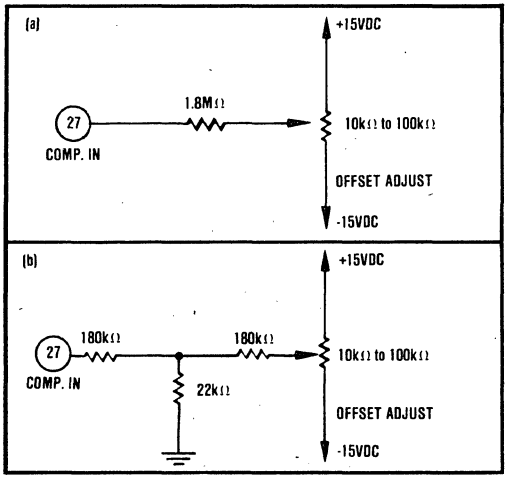


FIGURE 6. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range of Adjustment.

GAIN - Connect the Gain adjust potentiometer as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

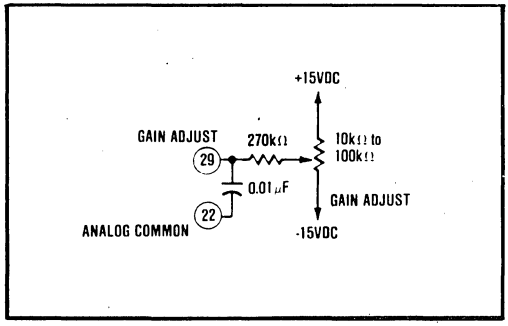


FIGURE 7. Connecting Optional Gain Adjust with a 0.2% Range of Adjustment.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

ADDITIONAL CONNECTIONS REQUIRED

The ADC72 may be operated at faster speeds for resolutions less than 14 or 13 bits, depending on the model selected, by connecting the Short-Cycle Input, pin 32, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

TABLE III. Short-Cycle Connections and Specifications for 12- to 14-Bit Resolutions.

Resolution (Bits)	16	14	13	12
Connect Pin 32 to	Open	Pin 15	Pin 14	Pin 13
Maximum Conversion Speed (μsec)(1)	57	50	46.5	43
Maximum Nonlinearity at 25°C (% of FSR)	0.003(2)	0.003(2)	0.006	0.006

NOTES:
1. Max. conversion time to maintain specified nonlinearity error.
2. BM and KM models only.

OUTPUT DRIVE

Normally all ADC72 logic outputs will drive 2 standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

HEAT DISSIPATION

The ADC72 dissipates approximately 550mW (typical) and the packages have a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above 70°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 8 for θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16 square inch (min.) area, this technique will allow operation to 85°C.

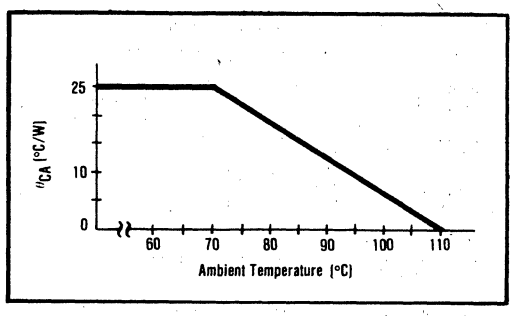


FIGURE 8. θ_{CA} Requirement Above 70°C.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	NONLINEARITY
ADC72JM	0°C to +70°C	±0.006% FSR
ADC72KM	0°C to +70°C	±0.003% FSR
ADC72AM	-25°C to +85°C	±0.006% FSR
ADC72BM	-25°C to +85°C	±0.003% FSR

BURR-BROWN®

ADC73
ADC731

True 16-Bit
ANALOG-TO-DIGITAL CONVERTER

FEATURES

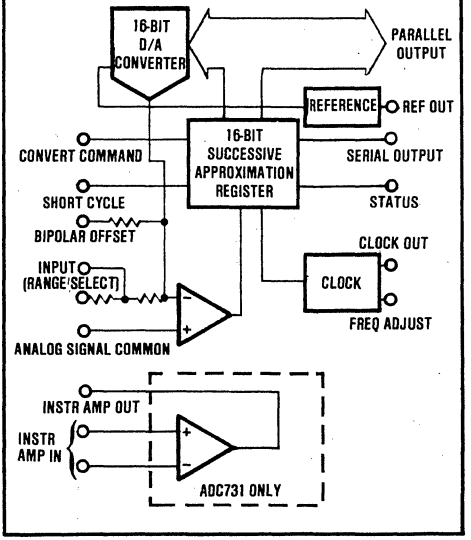
- 16-BIT RESOLUTION WITH TRUE 16-BIT ACCURACY
- LINEARITY ERROR OF LESS THAN ±0.00075% max (K model)
- OPTIONAL UNITY-GAIN INSTRUMENTATION AMPLIFIER INPUT (ADC731)
- FAST CONVERSION TIME - 170μsec max to ±0.00075% accuracy (K models)
- USER-SELECTED INPUT RANGES
- VERY-HIGH PERFORMANCE/PRICE RATIO

DESCRIPTION

The ADC73 and ADC731 are high quality, 16-bit successive approximation analog-to-digital converters that are linear to within ±0.0015% of full scale range (J models) or ±0.00075% of full scale range (K models). They combine state-of-the-art monolithic, hybrid, and discrete technologies to establish a new standard in value for true 16-bit A D converters. Complete with precision internal reference and comparator, ultra-stable clock, and unity-gain instrumentation amplifier input (ADC731), the ADC73 and ADC731 are ready to use. The user-selectable input ranges of ±5V, ±10V, 0 to +10V, and 0 to +20V, short-cycle capability for faster throughput rates, optional instrumentation amplifier input, binary or two's complement codes, parallel and serial outputs, and low price make this versatile converter suitable for a wide range of demanding applications.

Control signals and output data lines are TTL-compatible over the entire operating temperature range. Output data is available as a parallel word or a serial bit stream (MSB first) with corresponding clock and status outputs.

FUNCTIONAL DIAGRAM



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and rated power supplies unless otherwise noted.

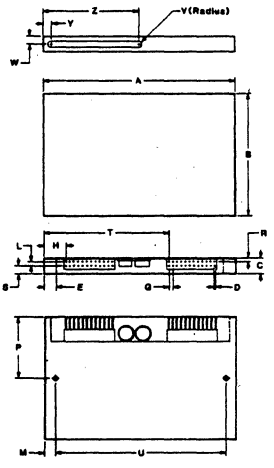
MODEL	ADC73J, ADC731J			ADC73K, ADC731K			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
INPUT CHARACTERISTICS							
ANALOG							
Voltage Ranges							
Bipolar		±5, ±10			*		V
Unipolar(1)		0 to +10, 0 to +20			*		V
Input Impedance, Direct Input							
0 to +10, ±5V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
Differential Amplifier (ADC731 only)							
Input Impedance, Differential		$10^{10} \parallel 3$			*		Ω ‖ pF
Common-mode		$5 \times 10^{9} \parallel 3$			*		Ω ‖ pF
Common-mode Voltage(2)		±(|Vcc| - 3)			*		V
CMRR ±10V input (3)		76			*		dB
DIGITAL (Convert Command)							
Pulse Width	200			*			nsec
Logic "1" Voltage	2.0			*			V
Current			20			*	μA
Logic "0" Voltage			0.8			*	V
Current			0.4			*	mA
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(4)		±0.001			*		%
Offset Error(4), Unipolar		±0.001			*		% of FSR
Bipolar		±0.001			*		% of FSR
Linearity Error(5)			±0.0015			±0.00075	% of FSR
Differential Linearity Error(5)		±0.0015	±0.003		±0.00075	±0.0015	% of FSR
Quantization Error			±0.00075			±0.00075	% of FSR
No Missing Codes Temperature Range	+15		+35			*	°C
Differential Ground Potential Error(6)							
Gain		0.01			*		LSB/mV
Offset		0.02			*		LSB/mV
Linearity		0.01			*		LSB/mV
Differential Linearity		0.02			*		LSB/mV
3σ Noise Full Scale (7)		150	300		*	*	μV, p-p
POWER SUPPLY SENSITIVITY							
Offset, +15VDC			±0.0005			*	% of FSR/%ΔV
-15VDC			±0.0001			*	% of FSR/%ΔV
+5VDC			±0.0007			*	% of FSR/%ΔV
Gain, +15VDC			±0.00035			*	% of FSR/%ΔV
-15VDC			±0.0012			*	% of FSR/%ΔV
+5VDC			±0.0004			*	% of FSR/%ΔV
CONVERSION TIME(8)		150	170		*	*	μsec
WARM-UP TIME (To rated accuracy)		15			*		minutes
TEMPERATURE DRIFT (Including Internal Reference)							
Gain			±10			*	ppm/°C
Offset, Unipolar			±2			*	ppm of FSR/°C
Bipolar			±5			*	ppm of FSR/°C
Linearity		±0.5	±2		*	*	ppm of FSR/°C
Differential Linearity		±0.5	±2		*	*	ppm of FSR/°C
LONG TERM STABILITY							
Gain Exclusive of Reference		±30			*		ppm/10^3 hr
Offset, Exclusive of Reference, Bipolar		±30			*		ppm of FSR/10^3 hr
Unipolar		±5			*		ppm of FSR/10^3 hr
Linearity		±3.7	±7.5		*	*	ppm of FSR/10^3 hr
Reference		±50			*		ppm/10^3 hr

ELECTRICAL (CONT)

MODEL	ADC73J, ADC731J			ADC73K, ADC731K			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS							
DIGITAL							
Data Codes (Positive True Logic)							
Parallel(9)		USB, BOB, BTC			•		
Serial (NRZ)(9)		USB, BOB			•		
Status		Logic "1" During Conversion			•		
Internal Clock							
Frequency		113			•		kHz
Clock Adjust Range		±20			•		%
Logic Levels							
Logic "1" Voltage	2.4			•			V
Current			0.4			•	mA
Logic "0" Voltage			0.4			•	V
Current			3.2			•	mA
INTERNAL REFERENCE							
Voltage	+5.9988	+6.0000	+6.0012	•	•	•	V
Source Current Available for External Loads	4.0			•			mA
Temperature Drift			±5			•	ppm/°C
POWER SUPPLY REQUIREMENTS							
Voltage, +15VDC	+14.5	+15	+15.5	•	•	•	V
-15VDC	-14.5	-15	-15.5	•	•	•	V
+5VDC	+4.75	+5	+5.25	•	•	•	V
Current, +15VDC		---	60		•	•	mA
-15VDC		---	65		•	•	mA
+5VDC		---	130		•	•	mA
POWER DISSIPATION		---	2.5		•	•	W
TEMPERATURE RANGE							
Specification	0		+70	•		•	°C
Storage	-55		+100	•		•	°C

NOTES:
1. Maximum input voltage of ADC731 differential buffer input is ±10V.
2. V_{CC} is value of supply voltage connected to +15V and -15V power supply pins.
3. See CMRR versus frequency performance curve.
4. Adjustable to zero with internal potentiometers. FSR = Full Scale Range.
5. As adjusted at the factory. Periodic recalibration is performed by following the adjustment procedure in the Installation and Operating Instructions.
6. Effect on output of DC voltage differential being present between analog and digital grounds. Measured with 10V Full Scale Range input and up to 175mVDC between grounds.
7. For 20V FSR input voltage. Noise is directly proportional to user-selected FSR.
8. Conversion time can be reduced to 120μsec. See Typical Performance Curves for accuracy versus conversion time. Conversion time and resolution may also be reduced by "short-cycling". See Installation and Operating Instructions.
9. BOB = Bipolar Offset Binary, USB = Unipolar Straight Binary, BTC = Bipolar Two's Complement.

MECHANICAL



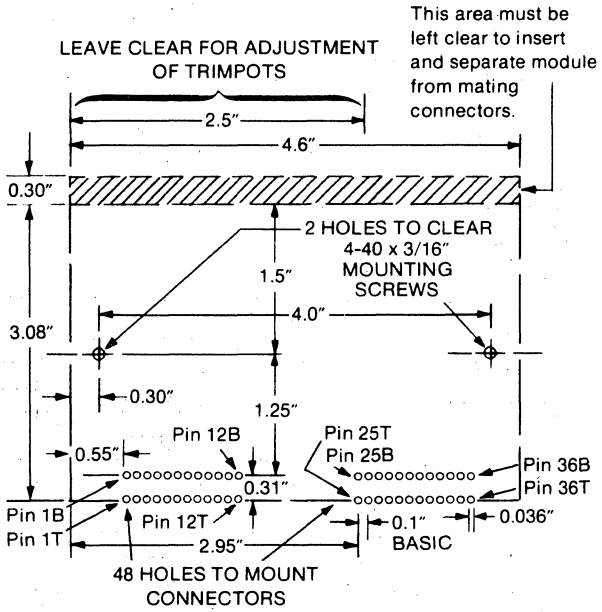
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.590	4.810	116.59	117.09
B	2.990	3.010	75.95	76.45
C	.380	.400	9.65	10.16
D	.022	.028	0.56	0.71
E	.290	.310	7.37	7.87
G	.100 BASIC		2.54 BASIC	
H	.540	.560	13.72	14.22
L	.100 BASIC		2.54 BASIC	
M	.290	.310	7.37	7.87
P	1.46	1.54	37.08	39.11
R	.180	.200	4.57	5.08
S	.090	.110	2.29	2.79
T	2.95	2.97	74.93	75.44
U	3.990	4.010	101.35	101.85
V	.065	.085	1.65	2.16
W	.140	.160	3.56	4.06
Y	.235	.255	5.97	6.48
Z	2.285	2.305	58.04	58.55

PIN DESIGNATIONS

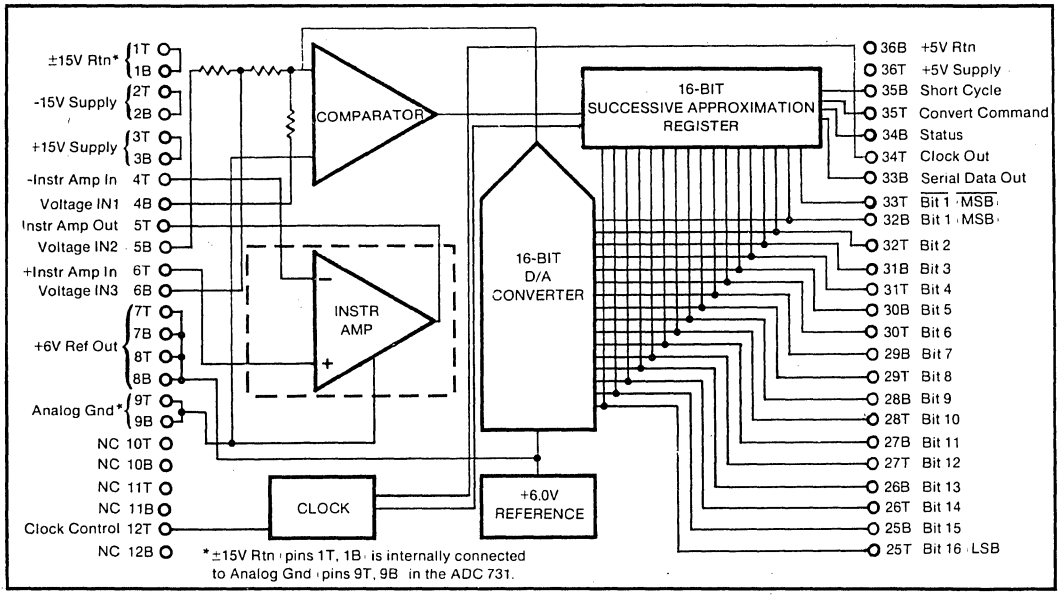
±15V Return(1)	1B	1T	±15V Return(1)	Bit 15	25B	25T	Bit 16 (LSB)
-15V Supply	2B	2T	-15V Supply	Bit 13	26B	26T	Bit 14
+15V Supply	3B	3T	+15V Supply	Bit 11	27B	27T	Bit 12
IN1	4B	4T	-Instr Amp Input	Bit 9	28B	28T	Bit 10
IN2	5B	5T	Instr Amp Output (ADC731 only(3))	Bit 7	29B	29T	Bit 8
IN3	6B	6T	+Instr Amp Input	Bit 5	30B	30T	Bit 6
NC(2)	7B	7T	NC(2)	Bit 3	31B	31T	Bit 4
+6V Ref Out	8B	8T	+6V Ref Out	Bit 1 (MSB)	32B	32T	Bit 2
Analog Gnd(1)	9B	9T	Analog Gnd(1)	Serial Out	33B	33T	Bit 1 (MSB)
NC	10B	10T	NC	Status Out	34B	34T	Clock Out
NC	11B	11T	NC	Short Cycle	35B	35T	Convert Command
NC	12B	12T	Clock Control	+5V Return	36B	36T	+5V Supply

NOTES:
1. ±15V Return (Pins 1T, 1B) is internally connected to Analog Gnd (Pins 9T, 9B) in ADC731.
2. Internally connected to Pins 8T, 8B.
3. Not internally connected on ADC73 models.

PC BOARD MOUNTING DETAILS
(component side)

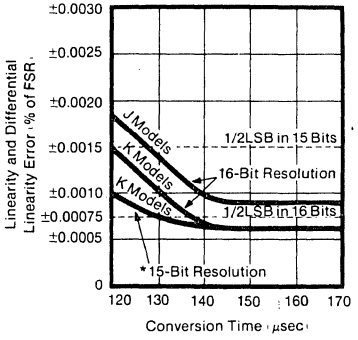


CONNECTION DIAGRAM



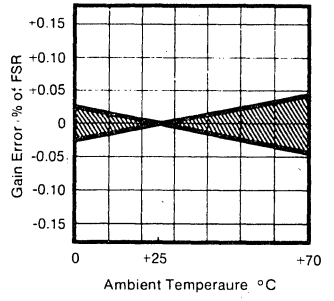
TYPICAL PERFORMANCE CURVES

LINEARITY AND DIFFERENTIAL LINEARITY ERROR VS CONVERSION TIME

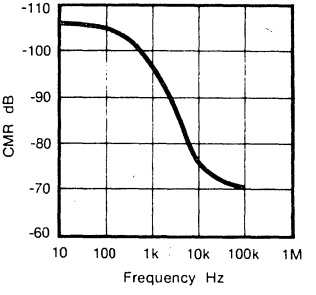


*Short-cycled to 15 Bits

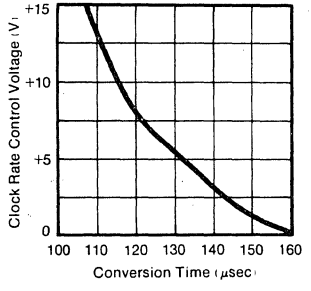
GAIN DRIFT VS AMBIENT TEMPERATURE



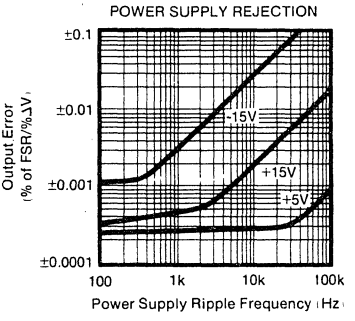
COMMON-MODE REJECTION OF DIFFERENTIAL INPUT BUFFER VS FREQUENCY



CLOCK RATE CONTROL VOLTAGE VS CONVERSION TIME



POWER SUPPLY REJECTION



DISCUSSION OF SPECIFICATIONS AND PERFORMANCE

ACCURACY

The accuracy of a successive approximation A D converter is described by the transfer function shown in Figure 1. All successive approximation A D converters have an inherent quantization error of ±1 2LSB. The remaining errors in the A D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and the scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including gain, offset, linearity, differential linearity, and power supply sensitivity. Initial gain and offset errors are adjusted to zero at the factory prior to shipment. Periodic recalibration may be performed by the user as needed. Gain drift over temperature rotates the transfer characteristic (Figure 1) about the zero or -FS point (all bits OFF) and offset drift shifts the transfer characteristic left or right. The linearity error has also been adjusted to within ±1 2LSB at the factory and, like gain and offset error, is user adjustable. Linearity error is the deviation of an actual bit transition from ideal transition value at any level over the range of the A D converter. A differential linearity error of ±1 2LSB means that the width of each bit step over the input range of the A/D converter is 1LSB±1/2LSB. The ADC73 and ADC731 are also guaranteed to have no missing codes from +15°C to +35°C.

TIMING CONSIDERATIONS

The timing diagram shown in Figure 2 illustrates by a specific example the timing of the A/D logic. It shows how an analog input voltage is converted to the output digital word 0110 0111 0110 1001.

DEFINITION OF DIGITAL CODES

The user may select one of three available codes for the ADC73 or ADC731 parallel output. They are unipolar straight binary (USB) for unipolar input ranges, bipolar offset binary (BOB), and bipolar two's complement (BTC) for bipolar input voltage ranges. Table I shows the LSB voltage, transition voltages and code definitions for each possible analog input signal range for 14-, 15-, and 16-bit resolutions.

Two serial data output codes are available, USB and BOB. The serial data is available as each bit is being converted with the MSB being output first. The serial data is synchronized with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition voltages shown in Table I also apply to the serial data output except for the BTC code.

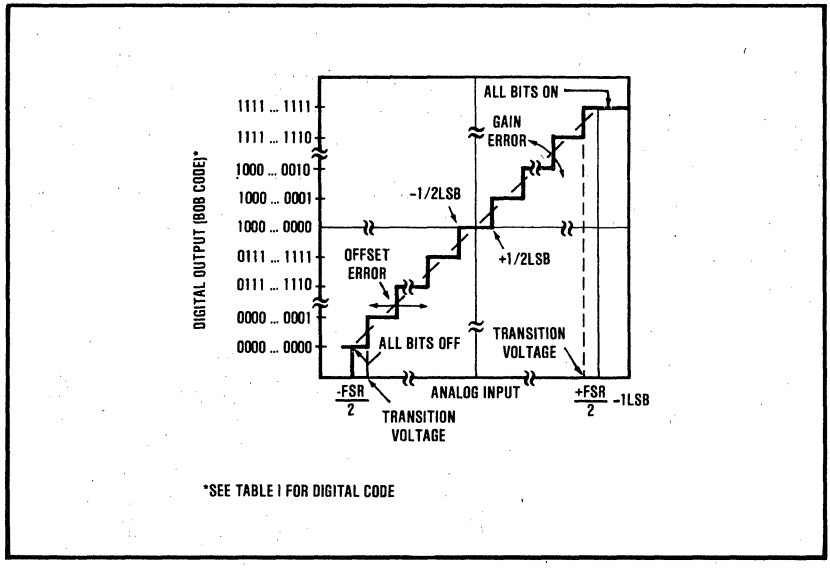
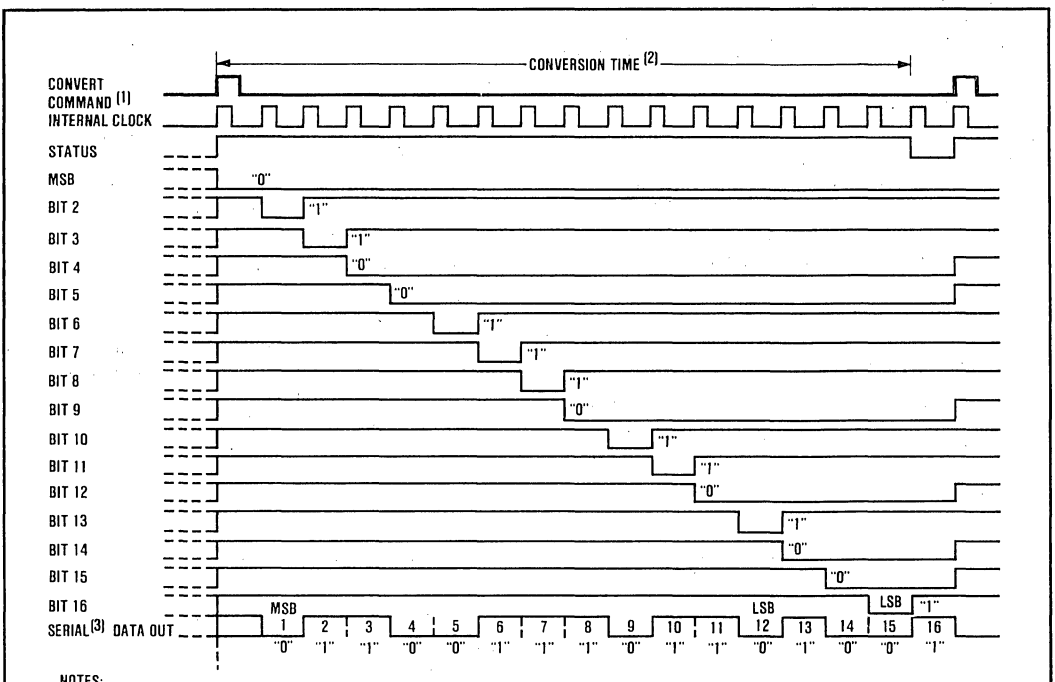


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.



NOTES:
1. The convert command must be at least 200nsec wide. The conversion is initiated by the "leading edge" of the convert command.
2. 170μsec maximum for 16 bits.
3. Use trailing (high to low) edge of clock to strobe each serial output bit.

FIGURE 2. ADC73 731 Timing Diagram.

TABLE I. Input Voltages, Transition Values, LSB Value and Code Definitions.

INPUT VOLTAGE - RANGE AND LSB VALUES					
Analog Input Voltage Range		10V	±5V	0 to +10V	0 to +20V
Code Designation		BOB(1) or BTC(2)	BOB(1) or BTC(2)	USB(3)	USB(3)
One Least Significant Bit LSB	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 14	1.22mV	610μV	610μV	1.22mV
	n = 15	610μV	305μV	305μV	610μV
	n = 16	305μV	153μV	153μV	305μV
Transition Values(4) MSB LSB					
1111 ... 1111	+Full Scale	+10V-3/2LSB	+5V-3/2LSB	+10V-3/2LSB	+20-3/2LSB
1000 ... 0000	Mid Scale	0±1/2LSB	0±1/2LSB	+5V±1/2LSB	+10±1/2LSB
0000 ... 0000	-Full Scale	-10V+1/2LSB	-5V+1/2LSB	0+1/2LSB	0+1/2LSB

1. BOB = Bipolar Offset Binary
2. BTC = Binary Two's Complement
3. USB = Unipolar Straight Binary
4. Nominal voltages for transition to code specified.

INSTALLATION AND OPERATING INSTRUCTIONS

MOUNTING

Mounting on a printed circuit board is accomplished using the female printed circuit connectors supplied with each A/D converter. Mount the A/D converter with two #4 external tooth lockwashers and two #4-40 machine screws. Refer to the mounting instructions. Be sure to leave clearance for screwdriver adjustment of the trim potentiometers.

PC LAYOUT CONSIDERATIONS

The metal case (ADC73 and ADC731) is connected internally to the ±15V Rtn pins (1B and 1T). Care must be taken to prevent other printed circuit conductors from making electrical contact with the case. In order to avoid ground loop paths, the case itself should not be connected to any other local power supply returns.

Coupling between digital signal paths and the analog inputs, IN1, IN2, IN3 and +Amp In and -Amp In (ADC731) should be minimized by careful layout separation and/or ground plane shielding.

In addition to the power supply connections, other connections to the A/D converter should be limited to digital inputs and outputs with a single digital common return path and the analog input.

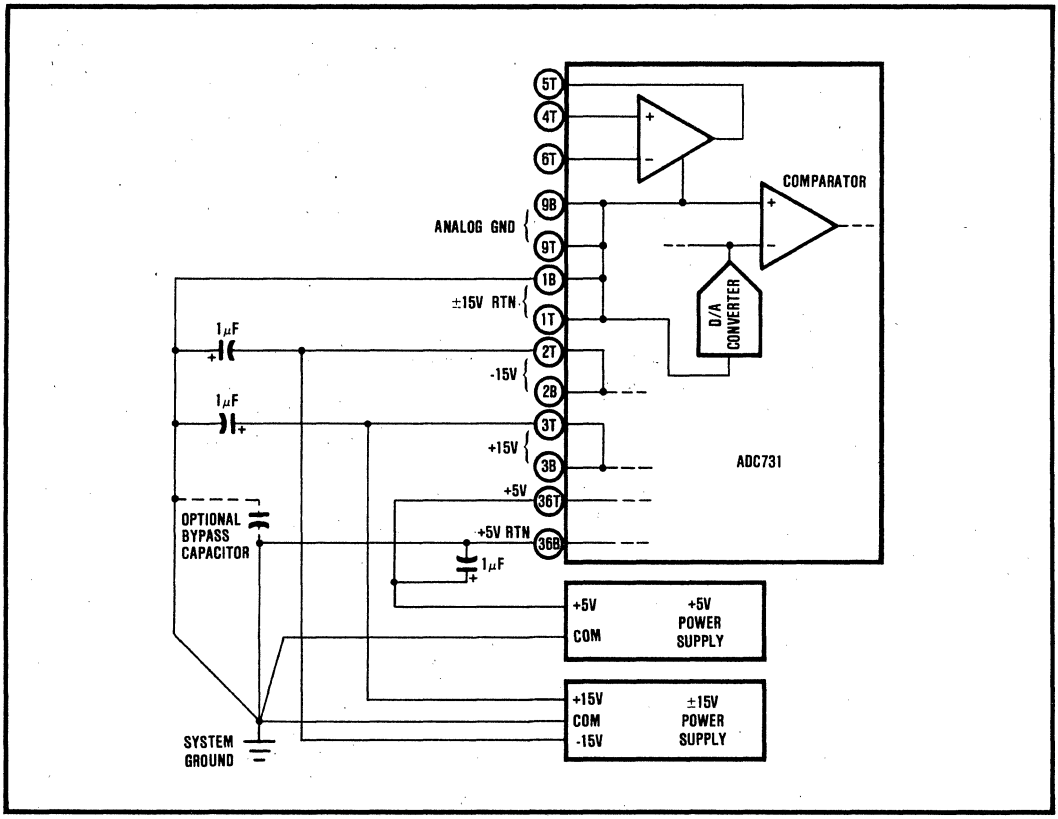


FIGURE 3. ADC731 Power Supply Connections.

POWER SUPPLY CONNECTIONS

ADC731

Analog Gnd (pins 9B, 9T) and ±15V Rtn (pins 1B, 1T) are connected together internally. ±15V Rtn and +5V Rtn (pin 36B) are not connected internally. These supply return lines should be connected together as close to the unit as possible. If ±15V Rtn and +5V Rtn are connected together at a system common point a significant distance from the pins, use a 0.01μF to 0.1μF nonpolarized bypass capacitor between these pins as close to the pins as possible. Refer to Differential Ground Potential Error in Electrical Specification table.

Power supply decoupling capacitors should be used as shown in Figure 3 and located as close as possible to the pins. Use 1μF tantalum or electrolytic capacitors. Parallel electrolytic capacitors with 0.01μF ceramic capacitors for best high frequency decoupling.

ADC73

Analog Gnd and ±15V Rtn pins are not connected internally on this model to permit a separate analog input signal return sense connection. Input signal connections are described in a following section.

Comments made for ADC731 power supply connections also apply to the ADC73. Refer to Figure 4.

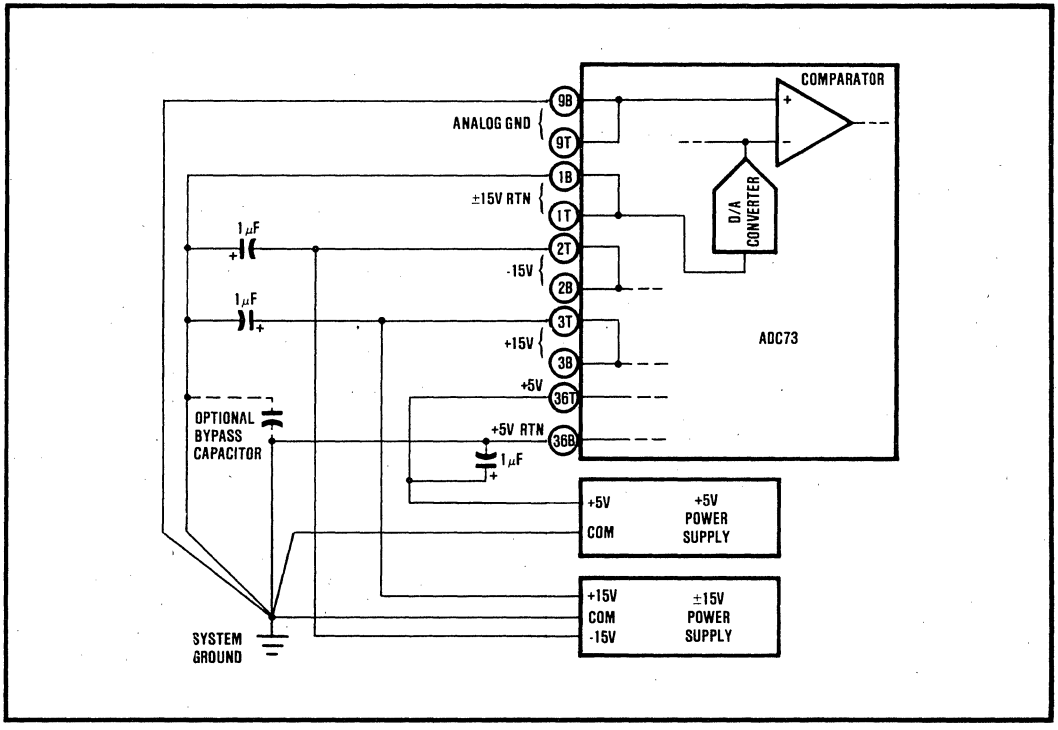


FIGURE 4. ADC73 Power Supply Connections.

SEPARATE POWER SUPPLIES

Because the effectiveness of high resolution A/D converters can be reduced by small amounts of noise, separate floating supplies may be needed for applications in environments with high electrical noise. These supplies and their return paths should be connected to the A/D converter only. Some experimentation with extra shielding and alternative return configurations may be necessary in extreme circumstances.

INPUT CONNECTIONS

ADC73

Analog input signals to ADC73 are connected directly to low impedance inputs (5kΩ and 10kΩ). The user may select unipolar or bipolar, 10V or 20V full scale ranges as illustrated in Figure 5.

ADC731

ADC731 has a precision high impedance differential input buffer. The user may select a unipolar range of 0 to +10V or bipolar ranges of ±5V or ±10V as illustrated in Figure 6. Note that signal input voltage V_{IN} plus the common-mode voltage is limited to ±10V for the bipolar connection and +10V for the unipolar connections.

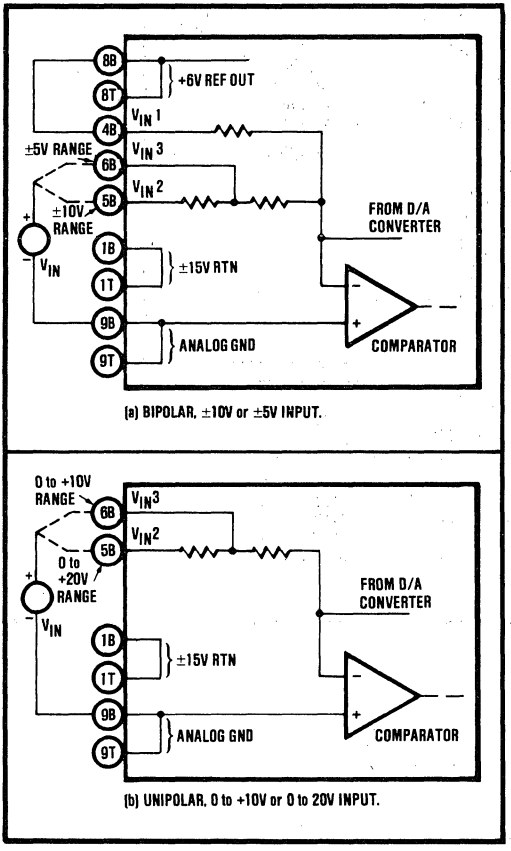


FIGURE 5. Signal Input Connections for ADC73.

CALIBRATION

The relative accuracy of ADC73 and ADC731 is adjusted to within specification at the factory. Offset and Gain may need to be adjusted after the A/D converter is installed and, after extended periods of time, recalibration will be necessary.

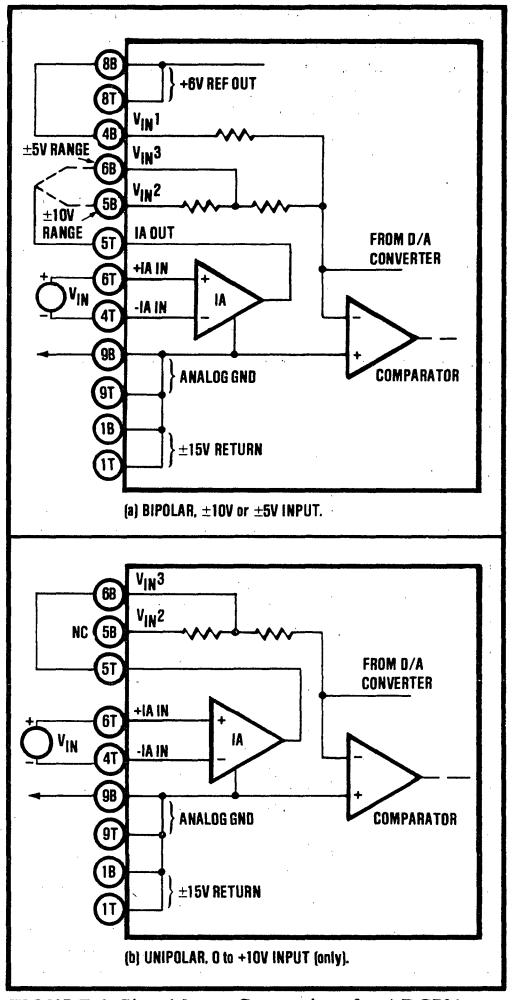


FIGURE 6. Signal Input Connections for ADC731.

Six potentiometers are built into the ADC73 and ADC731 for adjusting Offset (1 potentiometer), Gain (1 potentiometer), and Linearity (4 potentiometers). Linearity is adjusted in the first 4MSB's by adjusting the currents in bits 1(MSB), 2, 3, and 4. Refer to Table II for the transition voltages to be applied to the input appropriate to the input range being used. All input voltages should be set within ±10μV of the ideal voltage.

Procedure for full calibration (Offset, Linearity, and Gain):

1. Set the input voltage to the transition voltage for offset calibration. Adjust the Offset potentiometer until the transition to 0001_{16} from 0000_{16} occurs 50% of the time with repeated conversions.
2. Set the input to the transition voltage for the Gain Cal adjustment listed in Table II. Adjust the Gain potentiometer until the transition to $0FFF_{16}$ from $0FFE_{16}$ occurs 50% of the time with repeated conversions. If bit 4 should turn on such that the codes $1FFF_{16}$ and $1FFE_{16}$ occur, adjust potentiometer labeled bit 4 so that bit 4 (pin 31T) does not turn on.
3. Set the input to the bit 4 transition voltage of Table II. Adjust the potentiometer labeled bit 4 until the transition to 1001_{16} from 1000_{16} occurs 50% of the time with repeated conversions.
4. Set the input to the transition voltage for bit 3. Adjust potentiometer labeled bit 3 until the transition to 2001_{16} from 2000_{16} occurs 50% of the time with repeated conversions.
5. Set the input to the transition voltage for bit 2. Adjust the potentiometer labeled bit 2 until the transition to 4001_{16} from 4000_{16} occurs 50% of the time with repeated conversions.
6. Set the input to the transition voltage for bit 1. Adjust the potentiometer labeled bit 1 until the transition to 8001_{16} from 8000_{16} occurs 50% of the time with repeated conversions.
7. Set the input to the transition voltage for Gain calibration. Adjust the potentiometer labeled Gain until transition to $FFFF_{16}$ from $FFFE_{16}$ occurs 50% of the time with repeated conversions.

If adjusting only Offset and Gain, perform only steps 1 and 7, in that order.

TABLE II. Calibration Values for ADC73 and ADC731.

Input Voltage Range	0 to +10V	0 to +20V	±5V	±10V
POTENTIOMETER ADJUST Transition Codes(1)	Transition voltages for 16-bit resolution(2)			
Offset to 0001_{16} from 0000_{16}	0.000076V	0.000153V	-4.99924V	-9.999847V
Gain Cal(3) to $0FFF_{16}$ from $0FFE_{16}$	0.624771V	1.249542V	-4.375229V	-8.750458V
Bit 4 to 1001_{16} from 1000_{16}	0.625076V	1.250153V	-4.374924V	-8.7498747V
Bit 3 to 2001_{16} from 2000_{16}	1.250076V	2.500153V	-3.749924V	-7.499847V
Bit 2 to 4001_{16} from 4000_{16}	2.500076V	5.000153V	-2.499924V	-4.999847V
Bit 1 to 8001_{16} from 8000_{16}	5.000076V	10.000153V	0.000076V	0.000153V
Gain to $FFFF_{16}$ from $FFFE_{16}$	9.999771V	19.999542V	4.999771V	9.999542V

1. Positive true codes, Bipolar Offset Binary or Unipolar Straight Binary.
2. Voltages given are the nominal value for transition to the code shown.
3. This transition code used only prior to linearity error adjustment.

OPTIONAL CONVERSION TIME ADJUSTMENT

ADC73 and ADC731 may be operated at faster or slower conversion rates by connecting the Clock Control pin (12T) to a positive voltage between 0 and +15V as shown in Figure 7. The conversion time range is typically from 120μsec (12T at +15V) to 190μsec (12T tied to +15V Rtn), see Typical Performance Curves. If pin 12T is left open, the conversion time is typically 150μsec. Figure 7 illustrates the circuit used for conversion rate control. The potentiometer is a non-critical component.

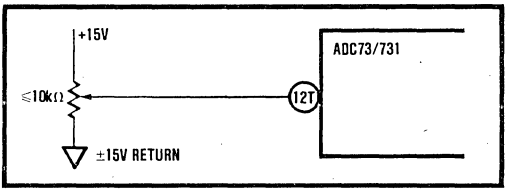


FIGURE 7. Clock Rate Control.

CHANGING RESOLUTION BY SHORT CYCLING

The ADC73 and ADC731 may be short cycled to lower resolutions and higher conversion rates by connecting the Short Cycle pin (35B) to the appropriate bit output as listed in Table III.

TABLE III. Connections for Short-Cycling Resolution Conversions.

Resolution (bits)	16	15	14	13	12
Connect pin 35B* to	Open	25T	25B	26T	26B
Connect pin 12T to	Open	Open	Open	Open	Open
Typical Conversion Time with pin 12T open μsec	150	141	132	123	114

*For resolutions less than 16 bits also connect pin 35B through a 2kΩ resistor to +5V

BURR-BROWN®

ADC76

16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

FEATURES

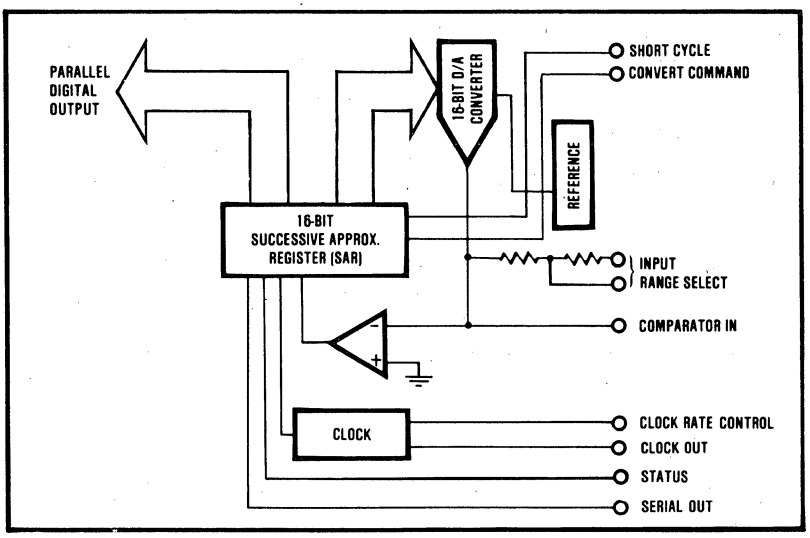
- 16-BIT RESOLUTION
- LINEARITY ERROR ±0.003% MAX (KG)
- COMPACT DESIGN
  32-Pin Ceramic Package
- LOW COST
- 15μs CONVERSION TIME (14-BIT)
- SERIAL AND PARALLEL OUTPUTS

DESCRIPTION

The ADC76 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The ADC76 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a convenient 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, serial output, and thin-film scaling resistors, which allows selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are DTL/TTL compatible.

Power supply voltages are ±15VDC and +5VDC.



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THEORY OF OPERATION

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

The ADC76 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that this converter will have no missing codes over a specified temperature range when short cycled for 14-bit operation.

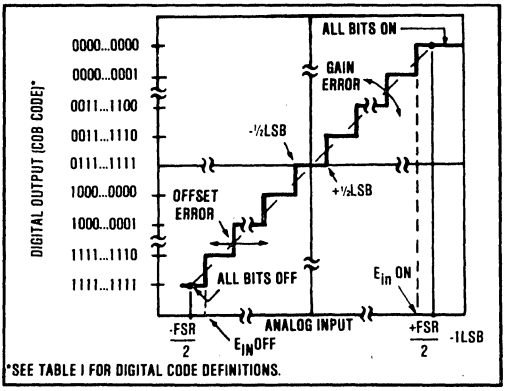


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram in Figure 2 assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 3 and 4 are timing diagrams showing the relationship of serial data to clock and valid data to status.

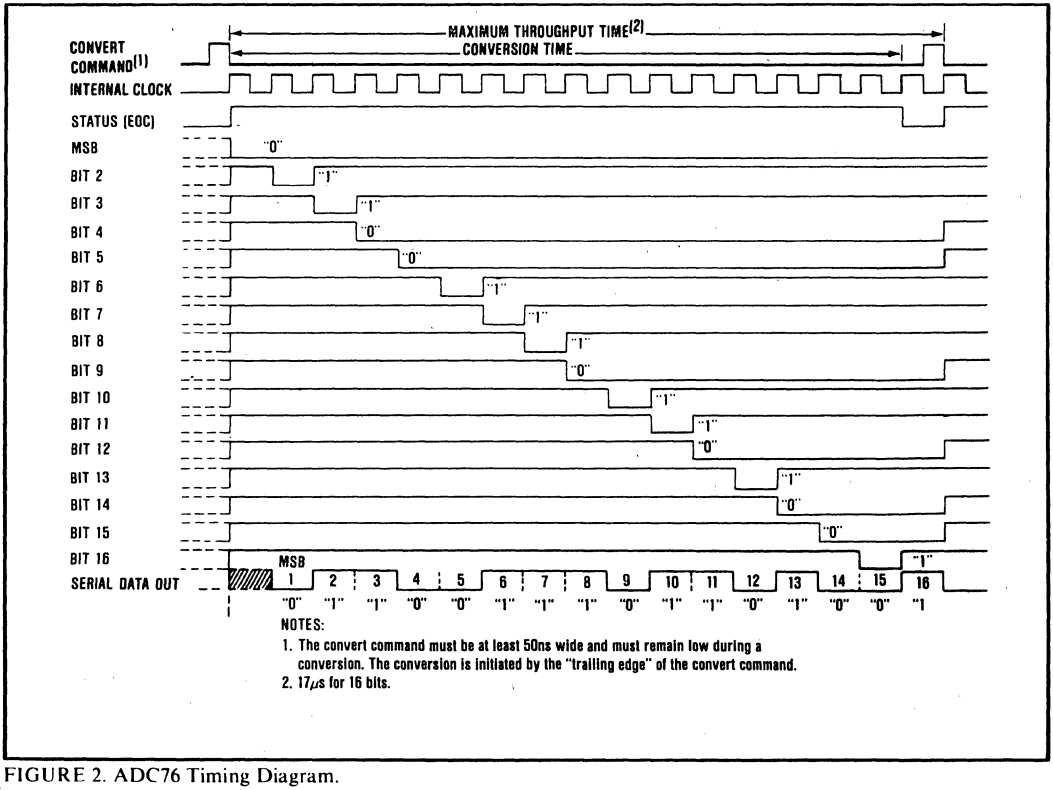


FIGURE 2. ADC76 Timing Diagram.

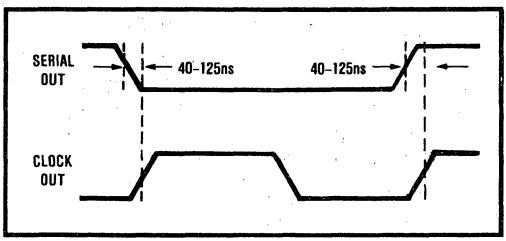


FIGURE 3. Timing Relationship of Serial Data to Clock.

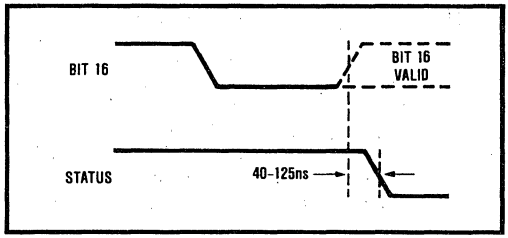


FIGURE 4. Timing Relationship of Valid Data to Status.

DIGITAL CODES

Parallel Data

Two binary codes are available on the ADC76 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 5 shows the connections for 14-bit resolution, parallel data output, with ±10V input.

Serial Data

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagrams of Figures 2 and 3. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

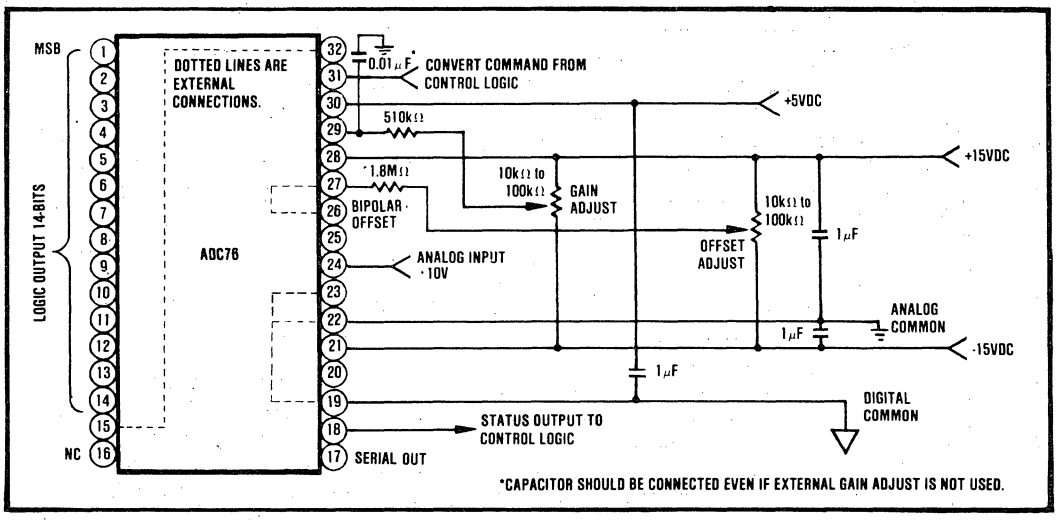


FIGURE 5. ADC76 Connections for: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
	n = 14	1.22mV	610μV	305μV	610μV	305μV	1.22mV
Transition Values							
MSB LSB							
000...000(4)	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

(1)COB = Complementary Offset Binary

(2)CTC = Complementary Two's Complement - obtained by inverting the most significant bit. MSB (pin 1).

(3)CSB = Complementary Straight Binary

(4)Voltages given are the nominal value for transition to the code specified.

SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC76KG			ADC76JG			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges: Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10, 0 to +20			*		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			*		kΩ
0 to +10V, ±5.0V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
DIGITAL INPUTS(1)							
Convert Command	Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading			1			*	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(2)		±0.1	±0.2		*	*	%
Offset Error: Unipolar(2)		±0.05	±0.1		*	*	% of FSR(3)
Bipolar(2)		±0.1	±0.2		*	*	% of FSR
Linearity Error			±0.003			±0.006	% of FSR
Inherent Quantization Error		±1/2			*		LSB
Differential Linearity Error		±0.003			*		% of FSR
Noise (3σ, p-p)		±0.003			*		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			*		% of FSR/%V_S
+5VDC		0.001			*		% of FSR/%V_S
CONVERSION TIME(4) (14 Bits)			15			*	μs
WARM-UP TIME	5			*			Min
DRIFT							
Gain			±15			*	ppm/°C
Offset: Unipolar		±2	±4		*	*	ppm of FSR/°C
Bipolar			±10			*	ppm of FSR/°C
Linearity		±2	±3		*	*	pm of FSR/°C
No Missing Codes Temp Range							
KG (14-bit)	+10		+40				°C
JG (13-bit)				0		50	°C

ELECTRICAL (CONT)

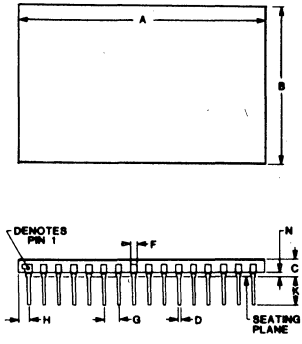
At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC76KG			ADC76JG			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT							
DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes[5]: Unipolar		CSB			•		
Bipolar		COB, CTC[6]			•		
Output Drive			2			•	TTL Loads
Serial Data Code (NRZ)		CSB, COB			•		
Output Drive			2			•	TTL Loads
Status		Logic "1" during conversion			•		
Status Output Drive			2			•	TTL Loads
Internal Clock: Clock Output Drive			2			•	TTL Loads
Frequency[7]	933		1400	•		•	kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		0.525			•		W
Rated Voltage: Analog	±14.5	±15	±15.5	•	•	•	VDC
Digital	+4.75	+5	+5.25	•	•	•	VDC
Supply Drain: +15VDC		+14			•		mA
−15VDC		−17			•		mA
+5VDC		+10			•		mA
TEMPERATURE RANGE							
Specification	0		+70	•		•	°C
Storage	−55		+125	•		•	°C

*Specification same as ADC76KG.

NOTES: (1) DTL/TTL compatible, i.e., Logic "0" = 0.8V, max, Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V, max, Logic "1" = 2.4V, min. (2) Adjustment to zero. See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Optional Conversion Time Adjustment" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to Bit 15, (pin 15) for 14-bit resolution. For resolutions less than 16 bits, pin 32 should also be tied to +5V through a 2kΩ resistor. (5) See Table I. CSB—Complementary Straight Binary, COB—Complementary Offset Binary, CTC—Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (pin 1). (7) Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz. See Figures 13 and 14 and Table III.

MECHANICAL



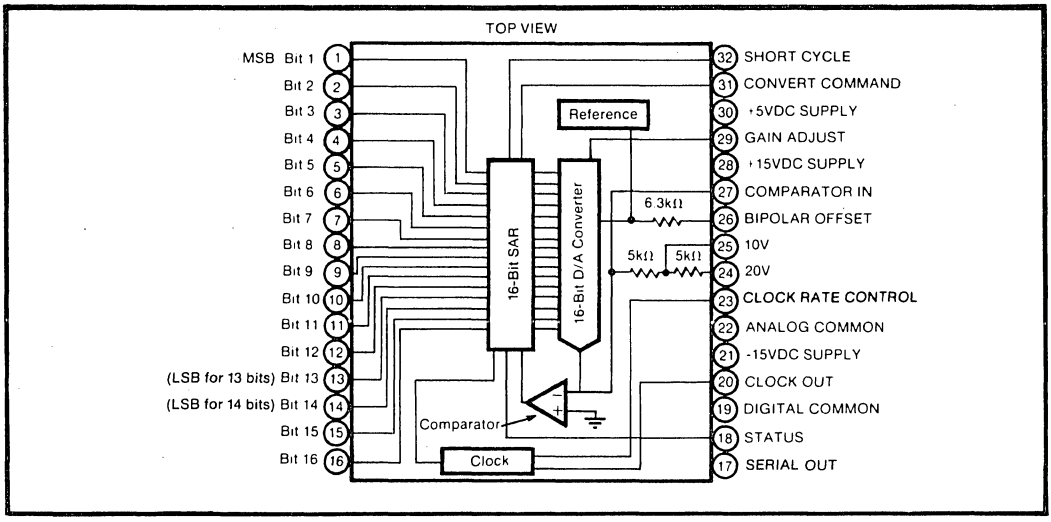
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	.180	.210	4.57	5.33
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.089	.106	2.26	2.69
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.900 BASIC		22.86 BASIC	
N	.015	.035	.38	.89

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

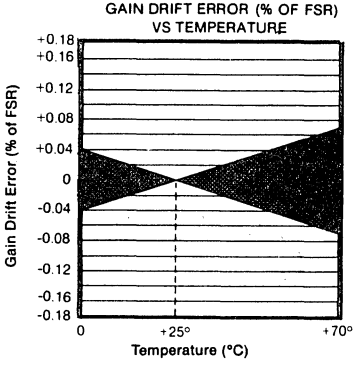
Pin numbers shown for reference only. Numbers may not be marked on package.

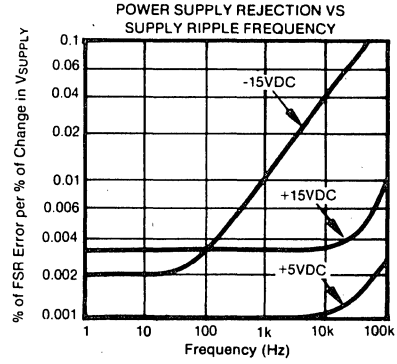
CASE: Ceramic
MATING CONNECTOR: 2302MC
WEIGHT: 13 grams (0.46 oz.)
HERMETICITY: Conforms to Method 1014, Condition C, Step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

CONNECTION DIAGRAM



TYPICAL PERFORMANCE CURVES





DISCUSSION OF SPECIFICATIONS

The ADC76 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10 and 11.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. The ADC76 power supply sensitivity is specified at ±0.003% of FSR/%V_S for the ±15V supplies and ±0.0015% of FSR/%V_S for the +5V supply. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 7.

LINEARITY ERROR

Linearity error is not adjustable and is the most meaningful indicator of A/D converter accuracy. Linearity is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter.

DIFFERENTIAL LINEARITY ERROR

Differential linearity describes the step size between transition values. A differential linearity error of ±0.003% of FSR indicates that the size of any step may not vary from the ideal step size by more than 0.003% of Full Scale Range.

ACCURACY VERSUS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC76 are shown in Figure 6.

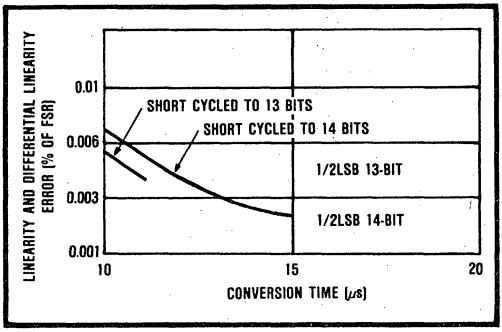


FIGURE 6. Linearity and Differential Linearity Versus Conversion Time.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC76, but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 7 to obtain noise free operation. These capacitors should be located close to the ADC.

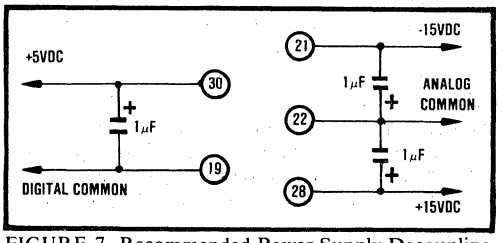


FIGURE 7. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 8 for circuit details.

TABLE II. ADC76 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB (pin 1).

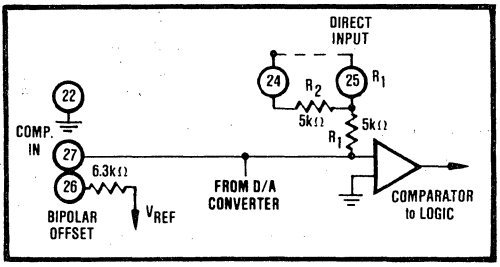


FIGURE 8. ADC76 Input Scaling Circuit.

OUTPUT DRIVE

Normally all ADC76 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

INPUT IMPEDANCE

The input signal to the ADC76 should be a low impedance, such as the output of an op amp to avoid any errors due to the relatively low input impedance of the ADC76.

If this impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the ADC76 as shown in Figure 9.

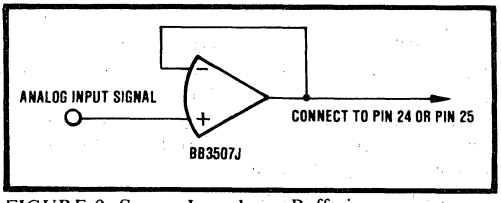


FIGURE 9. Source Impedance Buffering.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 10 and 11. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and

time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and pin 27 (Offset Adjust) may be left open if no external adjustment is required; however, pin 29 should always be bypassed with 0.01μF to Analog Common.

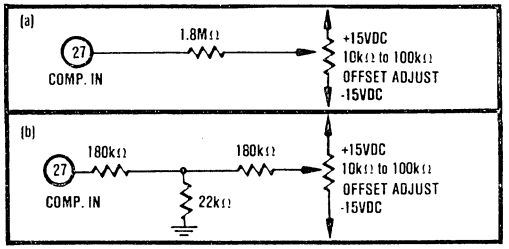


FIGURE 10. Two Methods of Connecting Optional Offset Adjust.

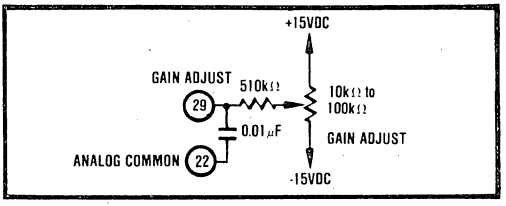


FIGURE 11. Connecting Optional Gain Adjust.

ADJUSTMENT PROCEDURE

Offset—Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 10. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}), Figure 1.

Adjust the Offset potentiometer until the actual end point transition voltage occurs at (E_{IN}^{OFF}). The ideal transition voltage values of the input are given in Table I.

Gain—Connect the Gain adjust potentiometer as shown in Figure 11. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at (E_{IN}^{ON}).

Table I details the transition voltage levels required.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

OPTIONAL CONVERSION TIME ADJUSTMENT

The ADC76 may be operated with faster conversion times for resolutions less than 14 bits by connecting the Short Cycle (pin 32) as shown in Table III. Typical conversion times for the resolution and connections are indicated.

TABLE III. Short Cycle Connections for 12- to 16-Bit Resolutions.

Resolution (Bits)	16	15	14	13	12
Connect Pin 32 to	Open	Pin 16	Pin 15	Pin 14	Pin 13
Typical Conversion Time	17μs	16μs	15μs	13μs	12μs

Clock Rate Control may be connected to an external multiturn trim potentiometer with a TCR of ±10ppm/°C or less as shown in Figure 12. The typical conversion time versus the Clock Rate Control voltage is shown in Figure 13. The effect of varying the conversion time and the resolution on Linearity Error and Differential Linearity Error is shown in Figure 6.

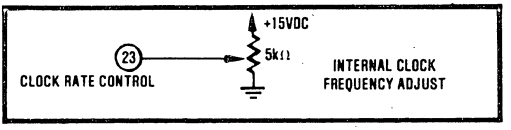


FIGURE 12. Clock Rate Control, Optional Fine Adjust.

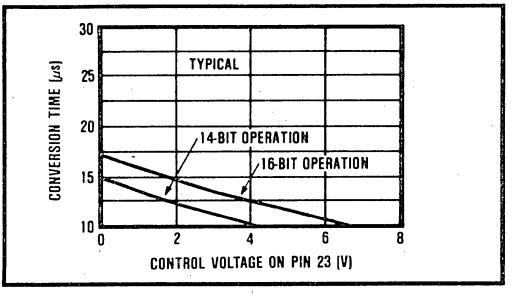


FIGURE 13. Conversion Time vs Clock Rate Control Voltage.

BURR-BROWN®

ADC76JM, KM
ADC76AM, BM

16-Bit Hybrid
ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 16-BIT RESOLUTION
- LINEARITY ERROR ±0.003% MAX (KM, BM)
- NO MISSING CODES GUARANTEED FROM 0°C TO +70°C
- 15μs CONVERSION TIME (14-BIT)
- SERIAL AND PARALLEL OUTPUTS
- COMPACT DESIGN
  32-pin Hermetic Metal Package
- LOW COST

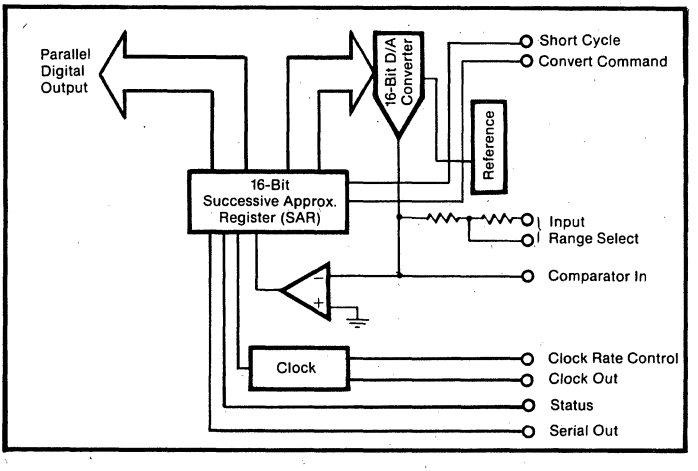
DESCRIPTION

The ADC76 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The ADC76 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a convenient 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, serial output, and thin-film scaling resistors, which allows selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Specified for operation over two temperature ranges: 0°C to +70°C (JM, KM) and −25°C to +85°C (AM, BM).

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are DTL/TTL-compatible.

Power supply voltages are ±15VDC and +5VDC.



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THEORY OF OPERATION

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

The ADC76 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that this converter will have no missing codes over a specified temperature range when short cycled for 14-bit operation.

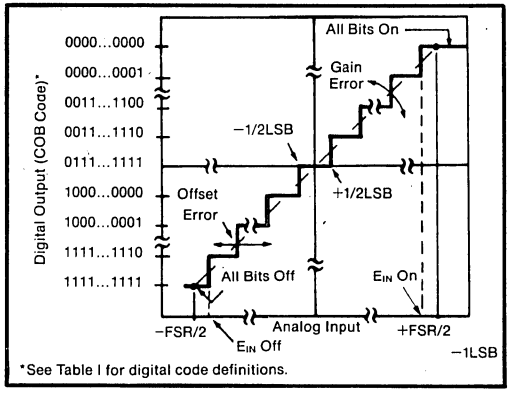
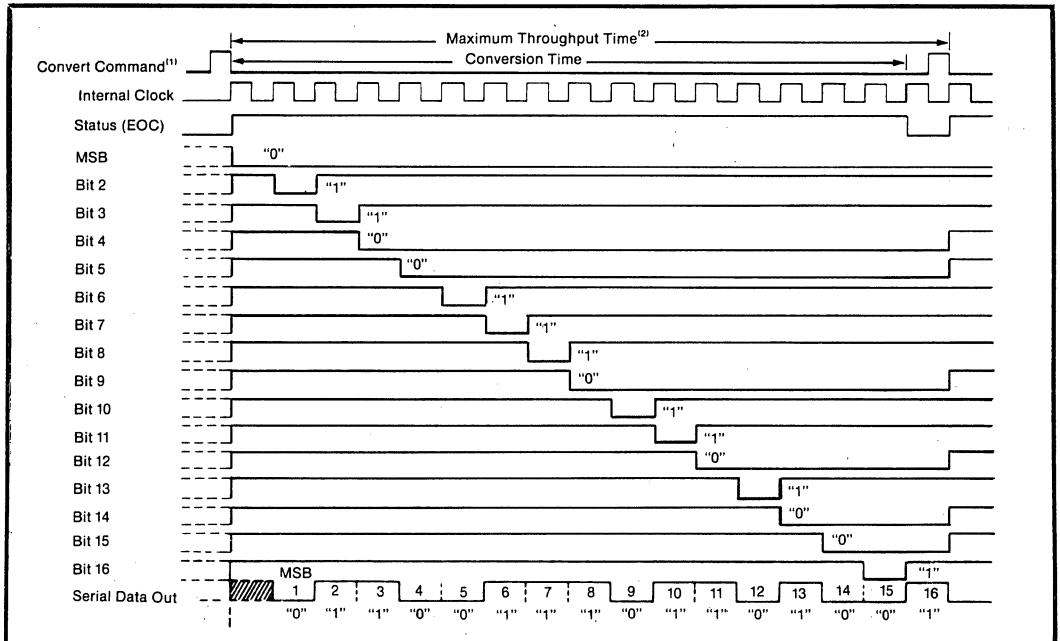


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram in Figure 2 assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 3 and 4 are timing diagrams showing the relationship of serial data to clock and valid data to status.



NOTES: (1) The convert command must be at least 50ns wide and must remain low during a conversion. The conversion is initiated by the "trailing edge" of the convert command.
(2) 17μs for 16 bits.

FIGURE 2. ADC76 Timing Diagram.

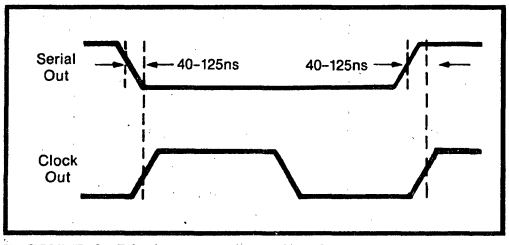


FIGURE 3. Timing Relationship of Serial Data to Clock.

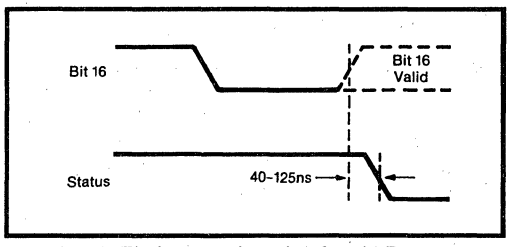


FIGURE 4. Timing Relationship of Valid Data to Status.

DIGITAL CODES

Parallel Data

Two binary codes are available on the ADC76 parallel output: they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 5 shows the connections for 14-bit resolution, parallel data output, with ±10V input.

Serial Data

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagrams of Figures 2 and 3. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

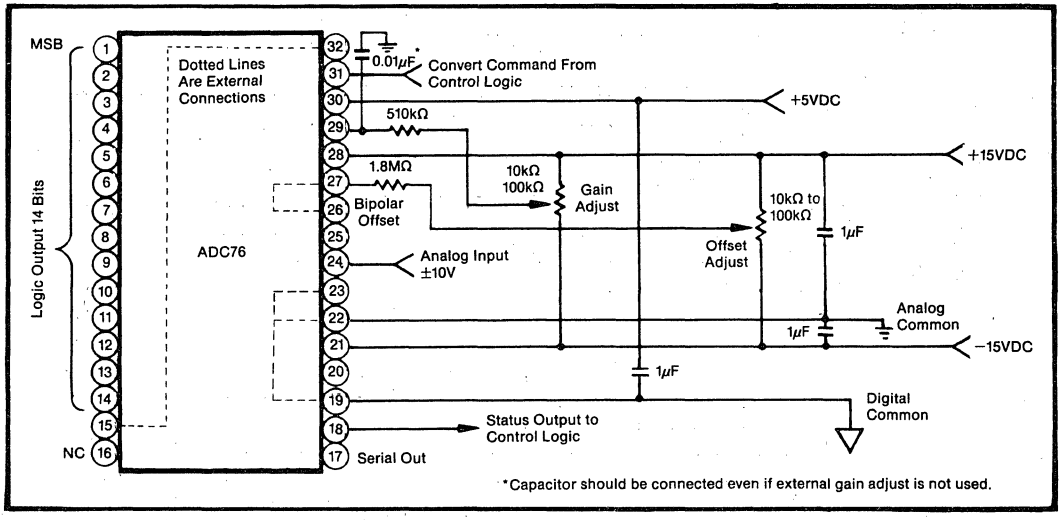


FIGURE 5. ADC76 Connections for: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
	n = 14	1.22mV	610μV	305μV	610μV	305μV	1.22mV
Transition Values							
MSB LSB							
000...000[4]	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

NOTES: (1) COB = Complementary Offset Binary.
(2) Complementary Two's Complement—obtained by inverting the most significant bit, MSB (pin 1).
(3) CSB = Complementary Straight Binary.
(4) Voltages given are the nominal value for transition to the code specified.

SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC76JM, KM			ADC76AM, BM			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges: Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10, 0 to +20			*		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			*		kΩ
0 to +10V, ±5.0V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
DIGITAL INPUTS[1]							
Convert Command		Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)					
Logic Loading			1			*	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error[2]		±0.1	±0.2		*	*	%
Offset Error: Unipolar[2]		±0.05	±0.1		*	*	% of FSR[3]
Bipolar[2]		±0.1	±0.2		*	*	% of FSR
Linearity Error: KM, BM			±0.003			*	% of FSR
JM, AM			±0.006			*	% of FSR
Inherent Quantization Error		±1/2			*		LSB
Differential Linearity Error		±0.003			*		% of FSR
Noise (3σ, p-p)		±0.003			*		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			*		% of FSR/%V_S
+5VDC		0.001			*		% of FSR/%V_S
CONVERSION TIME[4]							
14 Bits			15			*	μs
15 Bits			16			*	μs
16 Bits			17			*	μs
WARM-UP TIME	5				*		Min
DRIFT							
Gain			±15			*	ppm/°C
Offset: Unipolar		±2	±4		*	*	ppm of FSR/°C
Bipolar			±10			*	ppm of FSR/°C
Linearity		±2	±3		*	*	ppm of FSR/°C
No Missing Codes Temp Range							
KM, BM (14-bit)	0		+70	0		+70	°C
JM, AM (13-bit)	0		+70	−25		+85	°C

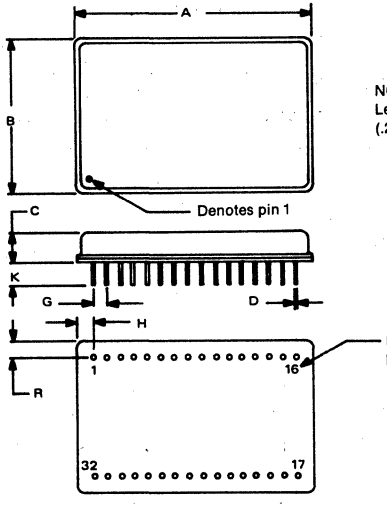
ELECTRICAL (CONT)

At +25°C and rated power supplies unless otherwise noted.

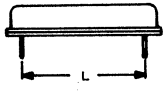
MODEL	ADC76JM, KM			ADC76AM, BM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT							
DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes[5]: Unipolar		CSB			•		
Bipolar		COB, CTC[6]			•		
Output Drive			2			•	TTL Loads
Serial Data Code (NRZ)		CSB, COB			•		
Output Drive			2			•	TTL Loads
Status		Logic "1" during conversion			•		
Status Output Drive			2			•	TTL Loads
Internal Clock: Clock Output Drive			2			•	TTL Loads
Frequency[7]	933		1400	•		•	kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		0.525			•		W
Rated Voltage: Analog	±14.5	±15	±15.5	•	•	•	VDC
Digital	+4.75	+5	+5.25	•	•	•	VDC
Supply Drain: +15VDC		+14			•		mA
−15VDC		−17			•		mA
+5VDC		+10			•		mA
TEMPERATURE RANGE							
Specification	0		+70	−25		+85	°C
Storage	−55		+125	•		•	°C

*Specification same as ADC76JM/KM.

NOTES: (1) DTL/TTL compatible, i.e., Logic "0" = 0.8V, max, Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V, max, Logic "1" = 2.4V, min. (2) Adjustment to zero. See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Optional Conversion Time Adjustment" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to Bit 15 (pin 15) for 14-bit resolution. For resolutions less than 16 bits, pin 32 should also be tied to +5V through a 2kΩ resistor. (5) See Table I. CSB—Complementary Straight Binary, COB—Complementary Offset Binary, CTC—Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (pin 1). (7) Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz. See Figures 12 and 13 and Table III.



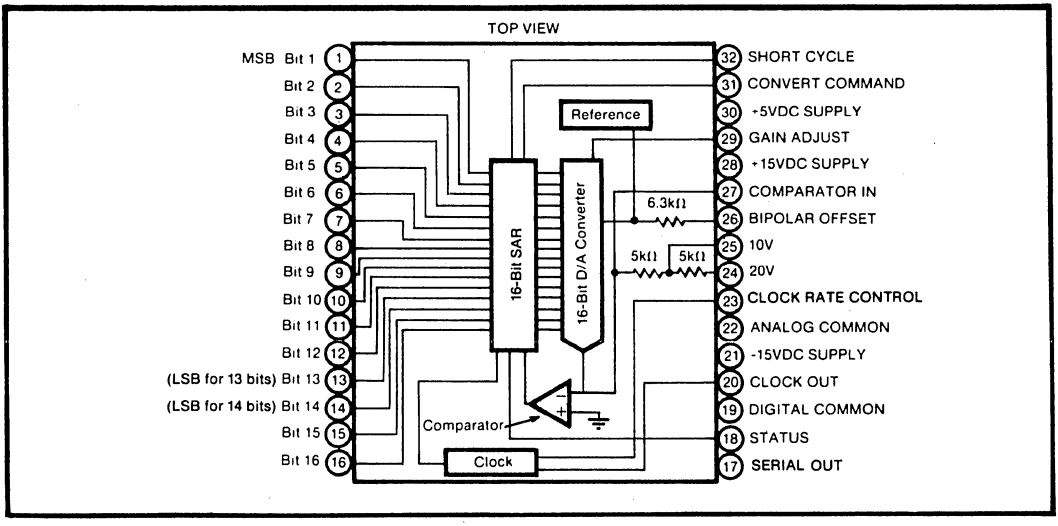
NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.



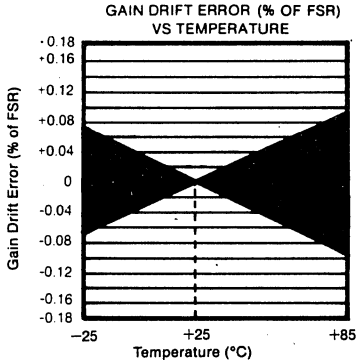
Pin numbers shown for reference only.
Numbers may not be marked on package.

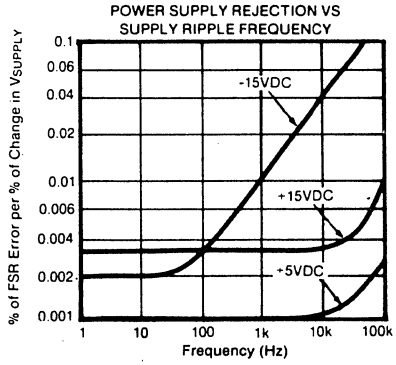
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

CONNECTION DIAGRAM



TYPICAL PERFORMANCE CURVES





DISCUSSION OF SPECIFICATIONS

The ADC76 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10 and 11.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. The ADC76 power supply sensitivity is specified at ±0.003% of FSR/%V_S for the ±15V supplies and ±0.0015% of FSR/%V_S for the +5V supply. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 7.

LINEARITY ERROR

Linearity error is not adjustable and is the most meaningful indicator of A/D converter accuracy. Linearity is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter.

DIFFERENTIAL LINEARITY ERROR

Differential linearity describes the step size between transition values. A differential linearity error of ±0.003% of FSR indicates that the size of any step may not vary from the ideal step size by more than 0.003% of Full Scale Range.

ACCURACY VERSUS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC76 are shown in Figure 6.

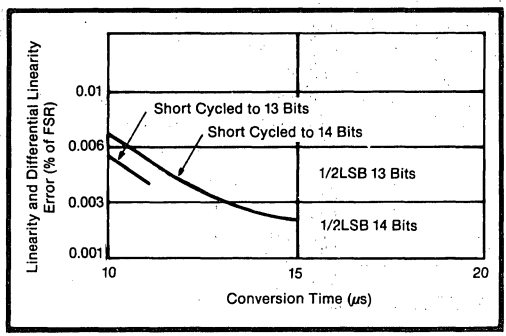


FIGURE 6. Linearity and Differential Linearity Versus Conversion Time.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC76, but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 7 to obtain noise free operation. These capacitors should be located close to the ADC.

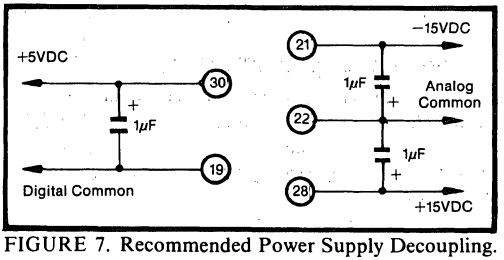


FIGURE 7. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 8 for circuit details.

TABLE II. ADC76 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB - pin 1.

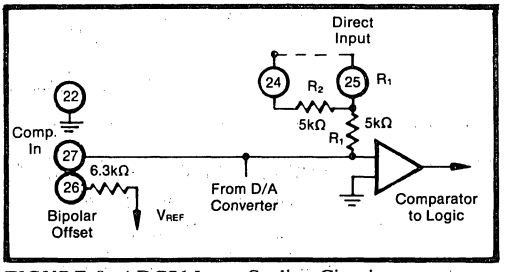


FIGURE 8. ADC76 Input Scaling Circuit.

OUTPUT DRIVE

Normally all ADC76 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

INPUT IMPEDANCE

The input signal to the ADC76 should be low impedance, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the ADC76.

If this impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the ADC76 as shown in Figure 9.

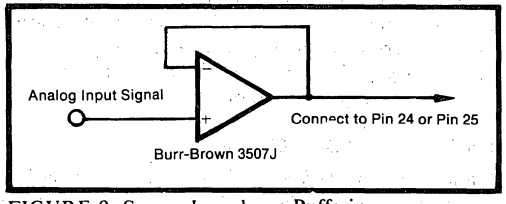


FIGURE 9. Source Impedance Buffering.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 10 and 11. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and

time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and pin 27 (Offset Adjust) may be left open if no external adjustment is required; however, pin 29 should always be bypassed with 0.01μF to Analog Common.

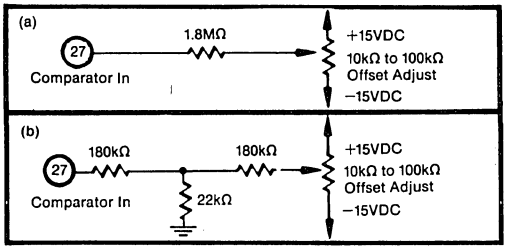


FIGURE 10. Two Methods of Connecting Optional Offset Adjust.

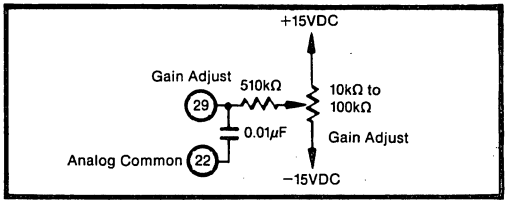


FIGURE 11. Connecting Optional Gain Adjust.

ADJUSTMENT PROCEDURE

Offset—Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 10. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}), Figure 1.

Adjust the Offset potentiometer Until the actual end point transition voltage occurs at (E_{IN}^{OFF}). The ideal transition voltage values of the input are given in Table I.

Gain—Connect the Gain adjust potentiometer as shown in Figure 11. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at (E_{IN}^{ON}).

Table I details the transition voltage levels required.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

OPTIONAL CONVERSION TIME ADJUSTMENT

The ADC76 may be operated with faster conversion times for resolutions less than 14 bits by connecting the Short Cycle (pin 32) as shown in Table III. Typical conversion times for the resolution and connections are indicated.

TABLE III. Short Cycle Connections for 12- to 16-Bit Resolutions.

Resolution (Bits)	16	15	14	13	12
Connect Pin 32 to	Open	Pin 16	Pin 15	Pin 14	Pin 13
Typical Conversion Time	17μs	16μs	15μs	13μs	12μs

Clock Rate Control may be connected to an external multiturn trim potentiometer with a TCR of ±10ppm/°C or less as shown in Figure 12. The typical conversion time versus the Clock Rate Control voltage is shown in Figure 13. The effect of varying the conversion time and the resolution on Linearity Error and Differential Linearity Error is shown in Figure 6.

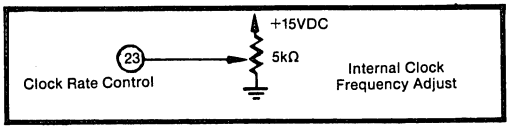


FIGURE 12. Clock Rate Control, Optional Fine Adjust.

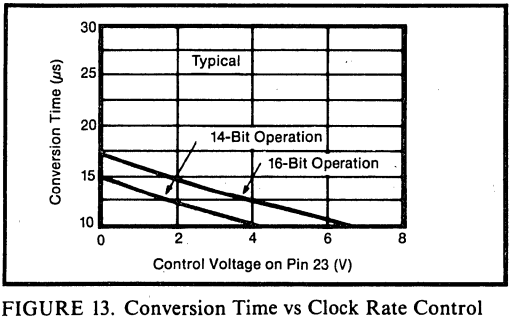


FIGURE 13. Conversion Time vs Clock Rate Control Voltage.

BURR-BROWN®

ADC80

General Purpose ANALOG-TO-DIGITAL CONVERTER

FEATURES

- INDUSTRY-STANDARD 12-BIT ADC
- LOW COST
- ±0.012% LINEARITY
- 25μs MAX CONVERSION TIME
- ±12V or ±15V OPERATION
- NO MISSING CODES −25°C to +85°C
- HERMETIC 32-PIN PACKAGE
- PARALLEL AND SERIAL OUTPUTS
- 595mW MAX DISSIPATION

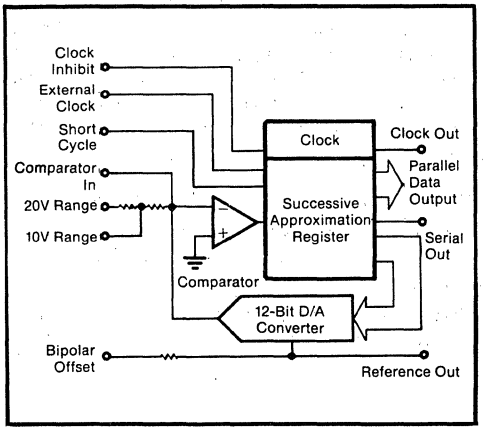
DESCRIPTION

The ADC80 is a 12-bit successive-approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom designed for freedom from latch-up and optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial endpoint accuracies of better than ±0.12% (±1/2LSB).

The maximum conversion time of 25μs makes the ADC80 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, the ADC80 may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher-speed operation.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike many ADC80-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise specified.

MODEL		ADC80AG			
		MIN	TYP	MAX	UNITS
RESOLUTION	ADC80AG-12, ADC80-AGZ-12[1]			12	Bits
	ADC80AG-10			10	Bits
INPUT					
ANALOG	Voltage Ranges: Unipolar		0 to +5, 0 to +10		V
	Bipolar		±2.5, ±5, ±10		V
	Impedance: 0 to +5V, ±2.5V	2.45	2.5	2.55	kΩ
	0 to +10V, +5V	4.9	5	5.1	kΩ
	±10V	9.8	10	10.2	kΩ
DIGITAL	Logic Characteristics (Over specification temperature range)				
	V_{IH} (Logic "1")	2.0		5.5	V
	V_{IL} (Logic "0")	−0.3		+0.8	V
	I_{IH} (V_{IN} = +2.7V)			−150	μA
	I_{IL} (V_{IN} = +0.4V)			500	μA
	Convert Command Pulse Width[2]	100		2000	ns
TRANSFER CHARACTERISTICS					
ACCURACY	Gain Error[3]		±0.1	±0.3	% of FSR[4]
	Offset Error[3]: Unipolar		±0.05	±0.2	% of FSR
	Bipolar		±0.1	±0.3	% of FSR
	Linearity Error: ADC80AG-12, ADC80AGZ-12			±0.012	% of FSR
	ADC80AG-10			±0.048	% of FSR
	Differential Linearity Error		±1/2	±3/4	LSB
	Inherent Quantization Error		±1/2		LSB
POWER SUPPLY SENSITIVITY					
11.4V ≤ ± V_{CC} ≤ 16.5V			±0.003	±0.009	% of FSR/%V_{CC}
+4.5V ≤ V_{DD} ≤ +5.5V			±0.002	±0.005	% of FSR/%V_{DD}
DRIFT	Total Accuracy, Bipolar[5]		±10	±23	ppm/°C
	Gain		±15	±30	ppm/°C
	Offset: Unipolar		±3		ppm of FSR/°C
	Bipolar		±7	±15	ppm of FSR/°C
	Linearity Error Drift		±1	±3	ppm of FSR/°C
	Differential Linearity over Temperature Range			±3/4	LSB
	No Missing Code Temperature Range	−25		+85	°C
	Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME[6]	ADC80AG-12, ADC80AGZ-12	15	22	25	μs
	ADC80AG-10	13	20	22	μs
OUTPUT					
DIGITAL (Bits 1-12, Clock Out, Status, Serial Out)					
Output Codes[7]					
Parallel: Unipolar			CSB		
Bipolar			COB, CTC		
Serial (NRZ)[8]			CSB, COB		
Logic Levels: Logic 0 (I_{SINK} ≤ 3.2mA)				+0.4	V
Logic 1 (I_{SOURCE} ≤ 80μA)		+2.4			V
Internal Clock Frequency			545		kHz
INTERNAL REFERENCE VOLTAGE					
Voltage		+6.2	+6.3	+6.4	V
Source Current Available for External Loads[9]		200			μA
Temperature Coefficient			±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS (For all models)					
Voltage: $\pm V_{CC}$		±11.4	±15	±16.5	V
V_{DD}		+4.5	+5.0	+5.5	V
Current: $+I_{CC}$			5	8.5	mA
$-I_{CC}$			21	26	mA
I_{DD}			11	15	mA
Power Dissipation ($\pm V_{CC}$ = 15V)			450	595	mW
Thermal Resistance, θ_{JA}			50		°C/W
TEMPERATURE RANGE (Ambient)					
Specification		−25		+85	°C
Operating (derated specs)		−55		+125	°C
Storage		−65		+150	°C

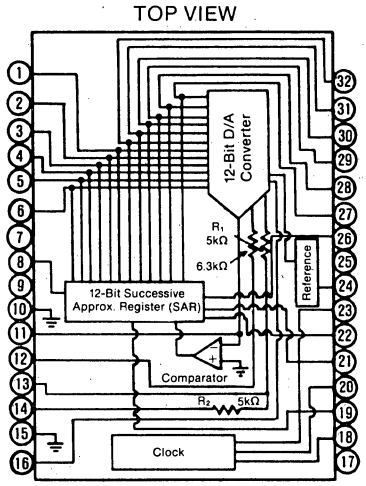
NOTES: (1) ADC80AGZ-12 is not recommended for new designs. Standard ADC80AG-12 now meets the extended power supply range of the ADC80AGZ-12. (2) Accurate conversion will be obtained with any convert command pulse width of greater than 100ns; however, it must be limited to 2μs (max) to assure the specified conversion time. (3) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (4) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc. (5) Includes drift due to linearity, gain, and offset drifts. (6) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time; see "Short Cycle Feature" section. (7) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table I for additional information. (8) NRZ means Non-Return-to-Zero coding. (9) External loading must be constant during conversion, and must not exceed 200μA for guaranteed specification.

CONNECTION DIAGRAM

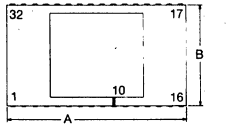
Pin 1 - Bit 6
Pin 2 - Bit 5
Pin 3 - Bit 4
Pin 4 - Bit 3
Pin 5 - Bit 2
Pin 6 - Bit 1(MSB)
Pin 7 - N/C *
Pin 8 - Bit 1 ($\overline{\text{MSB}}$)
Pin 9 - +5V Digital Supply
Pin 10 - Digital Common
Pin 11 - Comparator In
Pin 12 - Bipolar Offset
Pin 13 - R1 10V Range
Pin 14 - R2 20V Range
Pin 15 - Analog Common
Pin 16 - Gain Adjust

Pin 32 - Bit 7
Pin 31 - Bit 8
Pin 30 - Bit 9
Pin 29 - Bit 10 (LSB—10 Bits)
Pin 28 - Bit 11
Pin 27 - Bit 12 (LSB—12 Bits)
Pin 26 - Serial Out
Pin 25 - $-V_{CC}$
Pin 24 - Ref. Out (+6.3V)
Pin 23 - Clock Out
Pin 22 - Status
Pin 21 - Short Cycle
Pin 20 - Clock Inhibit
Pin 19 - External Clock
Pin 18 - Convert Command
Pin 17 - $+V_{CC}$

* +5V applied to pin 7 has no effect on circuit.

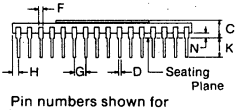


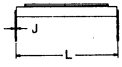
MECHANICAL



Leads in true position within .010" (.25MM) R at MMC at Seating Plane.

Seal ring is connected to Pin 10.





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

Pin numbers shown for reference only. Numbers may not be marked on package.

CASE: Ceramic, hermetic
MATING CONNECTOR: 2302MC
WEIGHT: 7.3gm (0.26oz)

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common ..... 0 to +16.5V
$-V_{CC}$ to Analog Common ..... 0 to −16.5V
V_{DD} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±0.5V
Logic Inputs (Convert Command, Clock In)
to Digital Common ..... −0.3V to V_{DD} +0.5V
Analog Inputs (Analog In, Bipolar Offset)
to Analog Common ..... ±16.5V
Reference Output ..... Indefinite Short to Common, Momentary Short to V_{CC}
Lead Temperature, Soldering ..... +300°C, 10s

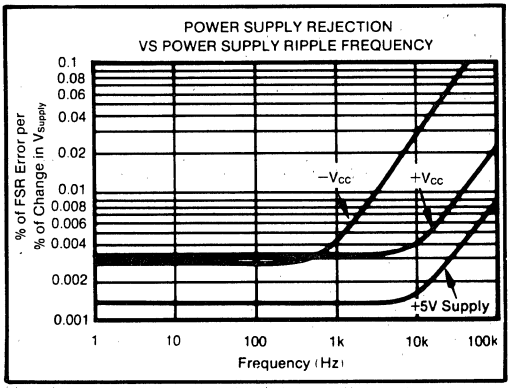
CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

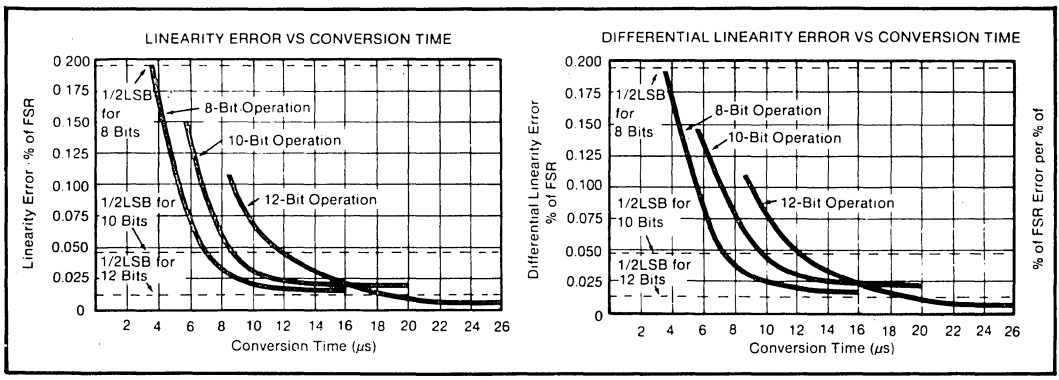
ORDERING INFORMATION

Model	Resolution (bits)
ADC80AG-10	10
ADC80AG-12	12
ADC80AG-12Q[1]	12
ADC80AGZ-12[2]	12

NOTES: (1) Q suffix indicates Environmental Screening; see Table IV for details. (2) ADC80AGZ-12 is not recommended for new designs. Standard ADC80AG-12 now meets the extended power supply range of the ADC80AG-12.

TYPICAL PERFORMANCE CURVES





DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a signficantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers.

The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1 which illustrates these relationships. A linearity specification which guarantees ±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and code definitions for each possible ADC80 analog input signal range are described in Table I.

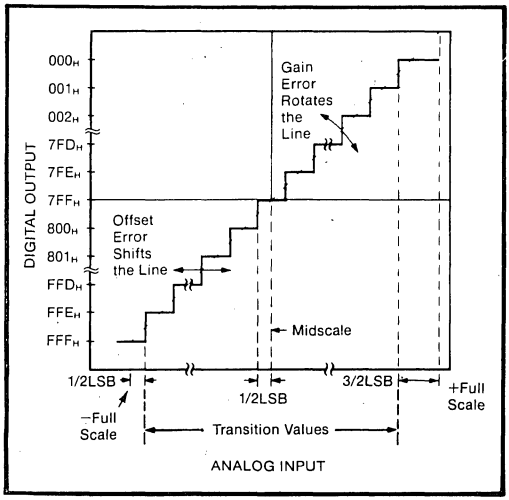


FIGURE 1. ADC80 Transfer Characteristic Terminology.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary Output	Input Voltage Range and LSB Values					
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB* or CTC**	COB or CTC	COB or CTC	CSB***	CSB
One Least Significant Bit (LSB)	FSR/2^n	20V/2^n	10V/2^n	5V/2^n	10V/2^n	5V/2^n
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
001_H to 000_H	+Full Scale	+10V − 3/2LSB	+5V − 3/2LSB	+2.5V − 3/2LSB	+ 10V − 3/2LSB	+5V − 3/2LSB
800_H to $7FF_H$	Mid Scale	0	0	0	+5V	+ 2.5V
FFF_H to FFE_H	−Full Scale	−10V + 1/2LSB	−5V + 1/2LSB	−2.5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

*COB = Complementary Offset Binary **CTC = Complementary Two's Complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.
***CSB = Complementary Straight Binary

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC80 input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. ADC80 is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC80 connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC80 follows this convention. Thus, bipolar offset error for the ADC80 is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

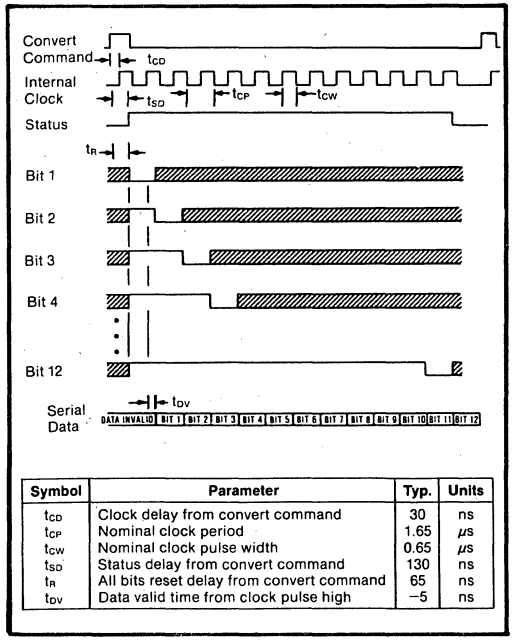
The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the Specification temperature range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC80 assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of course, results in a proportional change in all code transition values (i.e., a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

TIMING CONSIDERATIONS

Timing relationships of the ADC80 are shown in Figure 2. It should be noted that although the convert command pulse width must be between 100ns and 2μs to obtain the specified conversion time with internal clock, the ADC80 will accept longer convert commands with no loss of accuracy, assuming that the analog input signal is stable.



Symbol	Parameter	Typ.	Units
t_{CD}	Clock delay from convert command	30	ns
t_{CP}	Nominal clock period	1.65	μs
t_{CW}	Nominal clock pulse width	0.65	μs
t_{SD}	Status delay from convert command	130	ns
t_R	All bits reset delay from convert command	65	ns
t_{DV}	Data valid time from clock pulse high	−5	ns

FIGURE 2. ADC80 Timing Diagram (nominal values at +25°C with internal clock).

In this situation, the actual indicated conversion time (during which status is high) for 12-bit operation will be equal to approximately 1μs less than the sum of the factory-set conversion time and the length of the convert command. The code returned by the converter at the end of the conversion will accurately represent the analog input to the converter at the time the status returns to the

low state. In addition, although the initial state of the converter will be indeterminate when power is first applied, it is designed to time-out and be ready to accept a convert command within approximately 25μs after power-up, provided that either an external clock source is present or the internal clock is not inhibited.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse "n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the rising edge of the 13th clock pulse, and with valid output data ready to be read at that time. A new conversion may not be initiated until 50ns after the fall of the last clock pulse (pulse 13 for 12-bit operation).

Additional convert commands applied during conversion will be ignored.

DEFINITION OF DIGITAL CODES

Parallel Data

Three binary codes are available on the ADC80 parallel output; all three are complementary codes, meaning that logic "0" is true. The available codes are complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) and complementary two's complement (CTC) for bipolar input signal ranges. CTC coding is obtained by complementing bit 1 (the MSB) of the COB code; the complement of bit 1 is available on pin 8.

Serial Data

Two (complementary) straight binary codes are available on the serial output of the ADC80; as in the parallel case, they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values of Table I also apply to the serial data output, except that the CTC code is not available. All clock pulses available from the ADC80 have equal pulse widths to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC80, but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC80 as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC80 will be driving into a nominal DC input impedance of 2.5kΩ to 10kΩ depending upon the range selected. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC80 offers five standard input ranges: 0V to +5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. External padding resistors can be added to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range). Alternatively, the gain range of the converter may easily be increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by decreasing the value of the gain adjust series resistor in Figure 5.

TABLE II. ADC80 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

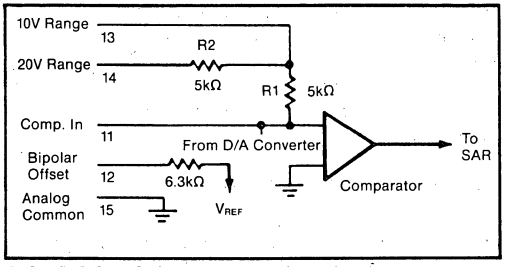


FIGURE 3. ADC80 Input Scaling Circuit.

CALIBRATION

Optional External Gain And Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC80 as shown in Figures 4 and 5 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These pots may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 16 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

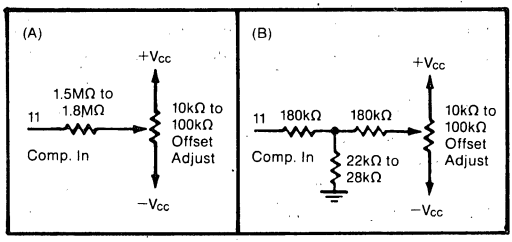


FIGURE 4. Two Methods of Connecting Optional Offset Adjust.

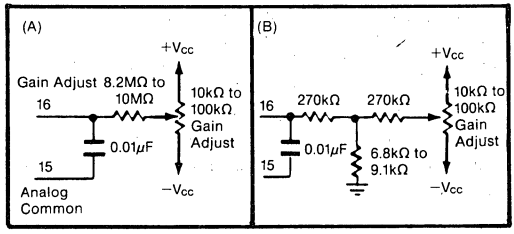


FIGURE 5. Two Methods of Connecting Optional Gain Adjust.

Adjustment Procedure

OFFSET—Connect the offset potentiometer as shown in Figure 4. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V +2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiometer until an output code is obtained which is alternating between FFE_H and FFF_H with approximately 50% occurrence of each of the two codes. In other words, the potentiometer is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 5. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V −7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiomter until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transitions to a precisely known value.

CLOCK OPTIONS

The ADC80 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with inexpensive TTL logic as shown in Figures 6 through 9. When operating with an external clock, the conversion time may be as short as 15μs (800kHz external clock frequency) with assured performance within specified limits. When operating with the internal clock, pin 19 (external clock input) and pin 20 (clock inhibit) may be left unconnected. No external pull-ups are required due to the inclusion of pull-up resistors in the ADC80. Pin 20 (clock inhibit) must be grounded for use with an external clock, which is applied to pin 19.

SHORT-CYCLE FEATURE

A short-cycle input (pin 21) permits the conversion to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applications not requiring full 12-bit resolution. In these situations, the short-cycle pin should be connected to the bit output pin of the next bit after the desired resolution. For example, when 10-bit resoltion is desired, pin 21 is connected to pin 28 (bit 11). In this example, the conversion cycle terminates and status is reset after the bit 10 decision. Short-cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times (with internal clock) are shown in Table III. Also shown are recommended minimum conversion times (external clock) for these conversion lengths to obtain the stated accuracies. The ADC80 is not factory-tested for these external clock conversion speeds and the product is not guaranteed to achieve the stated accuracies under these operating conditions; the recommended values are offered as an aid to the user.

TABLE III. Short-Cycle Connections and Conversion Times for 8-, 10-, and 12-Bit Resolutions—ADC80.

Resolution (Bits)	12	10	8
Connect pin 21 to	Pin 9 or NC	Pin 28	Pin 30
Maximum Conversion Time[1] Internal Clock (μs)	25	22	18
Minimum Conversion Time[1] External Clock (μs)	15	13	10
Maximum Linearity Error At +25°C (% of FSR)	0.012	0.048	0.20

NOTE: (1) Conversion time to maintain ±1/2LSB linearity error.

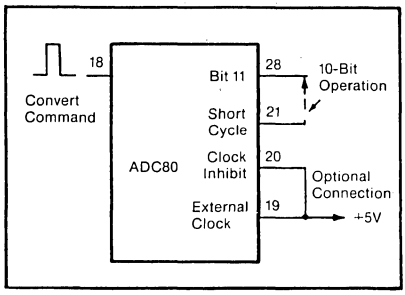


FIGURE 6. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

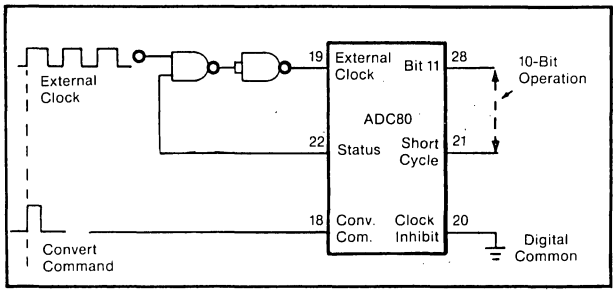


FIGURE 7. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

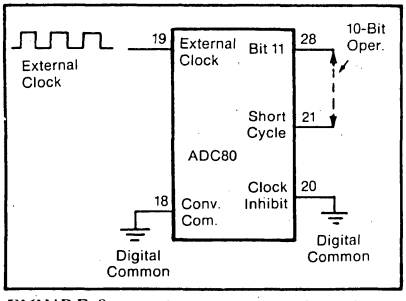


FIGURE 8. Continuous Conversion with External Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

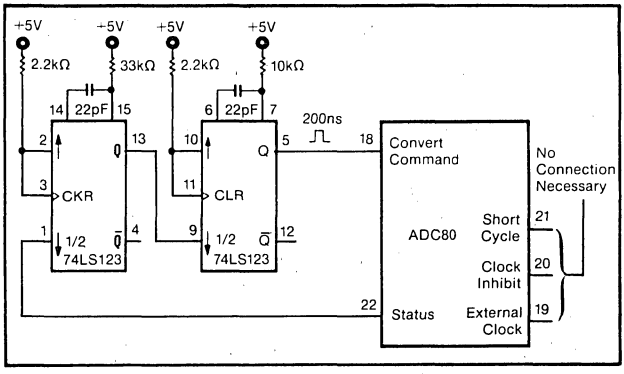


FIGURE 9. Continuous Conversion with 600ns between Conversions. (Circuit insures that conversion will start when power is applied.)

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table IV is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

TABLE IV. Screening Flow for ADC80AG-12Q.

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Electrical Test	Burr-Brown test procedure	
Burn-in	1015, B	160 hour, +125°C, steady-state
Hermeticity: Fine Leak Gross Leak	1014, A1 or A2 1014, C	5×10^{-7} atm cc/s bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	Burr-Brown QC5150	

BURR-BROWN®

ADC80H

General Purpose ANALOG-TO-DIGITAL CONVERTER

FEATURES

- PIN-COMPATIBLE WITH INDUSTRY STANDARD ADC80
- <600mW POWER DISSIPATION
- 15μsec CONVERSION TIME WITH EXTERNAL CLOCK
- 25μSEC MAXIMUM CONVERSION TIME
- ±0.012% INTEGRAL LINEARITY
- 12-BIT RESOLUTION
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- NO MISSING CODES −25°C TO +85°C
- PARALLEL AND SERIAL OUTPUTS
- 32-PIN HERMETIC PACKAGE

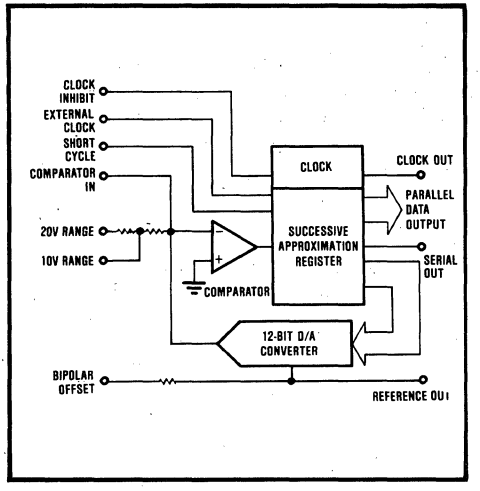
DESCRIPTION

The ADC80H is a 12-bit successive-approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom designed for freedom from latch-up and optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than ±0.012% (±1/2LSB). Like the industry standard ADC80, the ADC80H is completely specified for −25°C to +85°C operation.

The maximum conversion time of 25μsec makes the ADC80H ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, the ADC80H may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher-speed operation.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80H operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike other ADC80-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise specified.

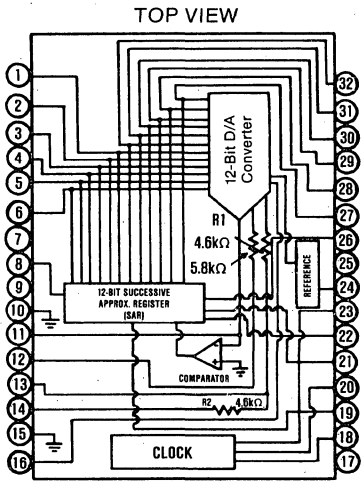
MODEL	ADC80H-AH-12			
	MIN	TYP	MAX	UNITS
RESOLUTION			12	Bits
INPUT				
ANALOG				
Voltage Ranges: Unipolar		0 to +5, 0 to +10		V
Bipolar		±2.5, ±5, ±10		V
Impedance: 0 to +5V, ±2.5V		2.3		kΩ
0 to +10V, +5V		4.6		kΩ
±10V		9.2		kΩ
DIGITAL				
Logic Characteristics (Over specification temperature range)				
V_{IH} (Logic "1")	2.0		5.5	V
V_{IL} (Logic "0")	−0.3		+0.8	V
I_{IH} (V_{IN} = +2.7V)			−150	μA
I_{IL} (V_{IN} =+0.4V)			500	μA
Convert Command Pulse Width[1]	100		2000	nsec
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error[2]		±0.1	±0.3	% of FSR[3]
Offset Error[2]: Unipolar		±0.05	±0.2	% of FSR
Bipolar		±0.1	±0.3	% of FSR
Linearity Error			±0.012	% of FSR
Differential Linearity Error			±3/4	LSB
Inherent Quantization Error		1/2		LSB
POWER SUPPLY SENSITIVITY				
+13.5V ≤ +V_{CC} ≤ +16.5V or +11.4V ≤ +V_{CC} ≤ +12.6V		±0.003	±0.009	% of FSR/%V_{CC}
−16.5V ≤ −V_{CC} ≤ −13.5V or −12.6V ≤ −V_{CC} ≤ −11.4V		±0.003	±0.009	% of FSR/%V_{CC}
+4.5V ≤ V_{DD} ≤ +5.5V		±0.002	±0.005	% of FSR/%V_{DD}
DRIFT				
Total Accuracy, Bipolar[4]		±10	±23	ppm/°C
Gain		±15	±30	ppm/°C
Offset: Unipolar		±3		ppm of FSR/°C
Bipolar		±7	±15	ppm of FSR/°C
Linearity Error Drift		±1	±3	ppm of FSR/°C
Differential Linearity over Temperature Range			±3/4	LSB
No Missing Code Temperature Range	−25		+85	°C
Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME[5]	15	22	25	μsec
OUTPUT				
DIGITAL(Bits 1-12, Clock Out, Status, Serial Out)				
Output Codes[6]				
Parallel: Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ)[7]		CSB, COB		
Logic Levels: Logic 0 (I_{sink} ≤ 3.2mA)			+0.4	V
Logic 1 (I_{source} ≤ 80μA)	+2.4V			V
Internal Clock Frequency		545		kHz
INTERNAL REFERENCE VOLTAGE				
Voltage	+6.2	+6.3	+6.4	
Source Current Available for External Loads[8]	200			μA
Temperature Coefficient		±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS				
Voltage, ±V_{CC}	±11.4	±15	±16.5	V
V_{DD}	+4.5	+5.0	+5.5	V
Current, +I_{CC}		5	8.5	mA
−I_{CC}		21	26	mA
I_{DD}		11	15	mA
Power Dissipation (±V_{CC} = 15V)		450	595	mW
TEMPERATURE RANGE (Ambient)				
Specification	−25		+85	°C
Storage	−65		+150	°C

NOTES: (1) Accurate conversion will be obtained with any convert command pulse width of greater than 100nsec; however, it must be limited to 2μsec (max) to assure the specified conversion time. (2) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustments" section. (3) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc. (4) Includes drift due to linearity, gain, and offset drifts. (5) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time; see "Short Cycle Feature" section. (6) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table I for additional information. (7) NRZ means non-return-to-zero coding. (8) External loading must be constant during conversion, and must not exceed 200μA for guaranteed specification.

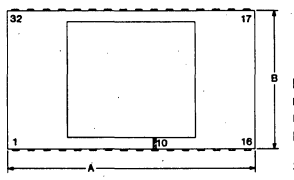
CONNECTION DIAGRAM

Pin 1 - Bit 6
Pin 2 - Bit 5
Pin 3 - Bit 4
Pin 4 - Bit 3
Pin 5 - Bit 2
Pin 6 - Bit 1(MSB)
Pin 7 - N/C
Pin 8 - Bit 1 (MSB)
Pin 9 - +5V Digital Supply
Pin 10 - Digital Common
Pin 11 - Comparator In
Pin 12 - Bipolar Offset
Pin 13 - R1 10V Range
Pin 14 - R2 20V Range
Pin 15 - Analog Common
Pin 16 - Gain Adjust

Pin 32 - Bit 7
Pin 31 - Bit 8
Pin 30 - Bit 9
Pin 29 - Bit 10
Pin 28 - Bit 11
Pin 27 - Bit 12 (LSB)
Pin 26 - Serial Out
Pin 25 - $-V_{CC}$
Pin 24 - Ref. Out (+6.3V)
Pin 23 - Clock Out
Pin 22 - Status
Pin 21 - Short Cycle
Pin 20 - Clock Inhibit
Pin 19 - External Clock
Pin 18 - Convert Command
Pin 17 - $+V_{CC}$



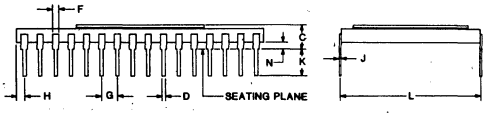
MECHANICAL



Leads in true position within .010" (.25MM) R at MMC at Seating Plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

S/R is connected to Pin 10.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

CASE: Ceramic, hermetic
MATING CONNECTOR: 2302MC
WEIGHT: 7.3gm (0.26oz)

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common	0 to +16.5V
$-V_{CC}$ to Analog Common	0 to −16.5V
V_{DD} to Digital Common	0 to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs (Convert Command, Clock In) to Digital Common	−0.3V to V_{DD} +0.5V
Analog Inputs (Analog In, Bipolar Offset) to Analog Common	±16.5V
Reference Output	Indefinite Short to Common, Momentary Short to V_{CC}
Power Dissipation	1000mW
Lead Temperature, Soldering	+300°C, 10sec
Thermal Resistance, θ_{JA}	60°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a significantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers.

The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1 which illustrates these relationships. A linearity specification which guarantees ±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

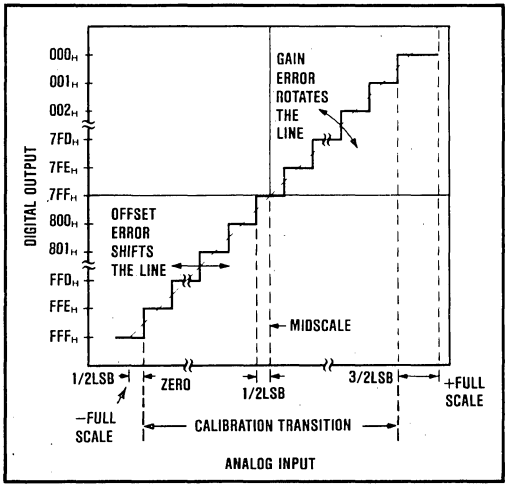


FIGURE 1. ADC80H Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and code definitions for each possible ADC80H analog input signal range are described in Table I.

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC80H input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is a definition of the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. ADC80H is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC80H connected for uniplolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC80H follows this convention. Thus, bipolar offset error for the ADC80H is

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	Input Voltage Range and LSB Values					
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB* or CTC**	COB or CTC	COB or CTC	CSB***	CSB
One Least Significant Bit (LSB)	FSR/2^n	20V/2^n	10V/2^n	5V/2^n	10V/2^n	5V/2^n
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
001_H to 000_H	+Full Scale	+10V − 3/2LSB	+5V − 3/2LSB	+2.5V − 3/2LSB	+ 10V − 3/2LSB	+5V − 3/2LSB
800_H to $7FF_H$	Mid Scale	0	0	0	+5V	+ 2.5V
FFF_H to FFE_H	−Full Scale	−10V + 1/2LSB	−5V + 1/2LSB	−2.5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

*COB = Complementary Offset Binary **CTC = Complementary Two's Complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.
***CSB = Complementary Straight Binary

defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the specification range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

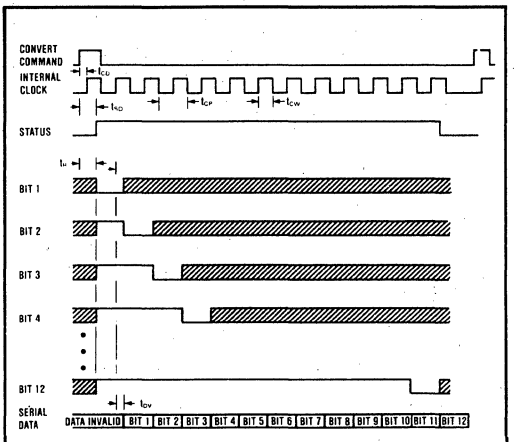
Electrical specifications for the ADC80H assume the application of the rated power supply voltages of+5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

TIMING CONSIDERATIONS

Timing relationships of the ADC80H are shown in Figure 2. It should be noted that although the convert command pulse width must be between 100nsec and 2μsec to obtain the specified conversion time with internal clock, the ADC80H will accept longer convert commands with no loss of accuracy, assuming that the analog input signal is stable.In this situation, the actual indicated conversion time (during which status is high) for 12-bit operation will be equal to approximately 1μsec less than the sum of the factory-set conversion time and the length of the convert command. The code returned by the converter at the end of the conversion will accurately represent the analog input to the converter at the time the convert command returns to the low state. In addition, although the initial state of the converter will be indeterminate when power is first applied, it is designed to time-out and be ready to accept a convert command within approximately 25μsec after power-up, provided that either an external clock source is present or the internal clock is not inhibited.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse "n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the rising edge of the 13th clock pulse, and with valid output data ready to be read at that time. A new conversion may not be initiated until 50nsec after the fall of the last clock pulse (pulse 13 for 12-bit operation).

Additional convert commands applied during conversion will be ignored.



Symbol	Parameter	Typ.	Units
t_{CD}	Clock delay from convert command	30	nsec
t_{CP}	Nominal clock period	1.65	μsec
t_{CW}	Nominal clock pulse width	0.65	μsec
t_{SD}	Status delay from convert command	130	nsec
t_R	All bits reset delay from convert command	65	nsec
t_{DV}	Data valid time from clock pulse high	−35	nsec

FIGURE 2. ADC80H Timing Diagram (nominal values at +25°C with internal clock).

DEFINITION OF DIGITAL CODES

Parallel Data

Three binary codes are available on the ADC80H parallel output; all three are complementary codes, meaning that logic "0" is true. The available codes are complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) and complementary two's complement (CTC) for bipolar input signal ranges. CTC coding is obtained by complementing bit 1 (the MSB) relative to its normal state for CSB or COB coding; the complement of bit 1 is available on pin 8.

Serial Data

Two (complementary) straight binary codes are available on the serial output of the ADC80H; as in the parallel case, they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values of Table I also apply to the serial data output, except that the CTC code is not available. All clock pulses available from the ADC80H have equal pulse widths to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC80H, but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC80H as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC80H will be driving into a nominal DC input impedance of 2.3kΩ to 9.2kΩ depending upon the range selected. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC80H offers five standard input ranges: 0V to +5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. Use of external padding resistors to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range) will require matching of the external fixed resistor values to individual devices, due to the large tolerance of the internal input resistors. Alternatively, the gain range of the converter may easily be increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by the decreasing the value of the gain adjust series resistor in Figure 5.

TABLE II. ADC80H Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

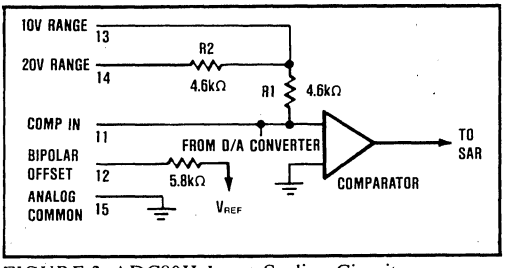


FIGURE 3. ADC80H Input Scaling Circuit.

CALIBRATION

Optional External Gain And Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC80H as shown in Figures 4 and 5 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These

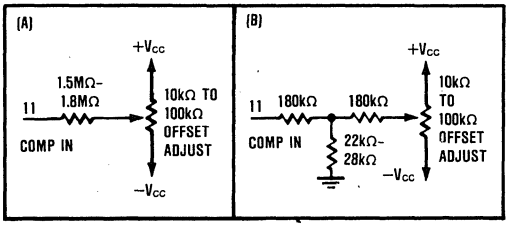


FIGURE 4. Two Methods of Connecting Optional Offset Adjust.

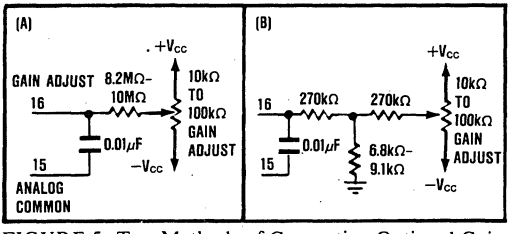


FIGURE 5. Two Methods of Connecting Optional Gain Adjust.

pots may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 16 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

Adjustment Procedure

OFFSET—Connect the offset potentiometer as shown in Figure 4. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V +2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiometer until an output code is obtained which is alternating between FFE_H and FFF_H with approximately 50% occurence of each of the two codes. In other words, the potentiometer is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 5. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V −7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiometer until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transition to a precisely known value.

CLOCK OPTIONS

The ADC80H is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with inexpensive TTL logic as shown in Figures 6 through 9. When operating with an external clock, the conversion time may be as short as 15μsec (800kHz external clock frequency) with assured performance within specified limits. When operating with the internal clock, pin 19 (external clock input) and pin 20 (clock inhibit) may be left unconnected. No external pull-ups are required due to the inclusion of pull-up resistors in the ADC80H. Pin 20 (clock inhibit) must be grounded for use with an external clock, which is applied to pin 19.

SHORT-CYCLE FEATURE

A short-cycle input (pin 21) permits the conversion to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applica-

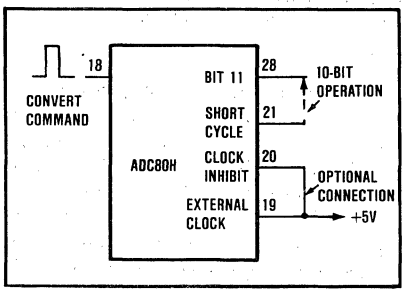


FIGURE 6. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

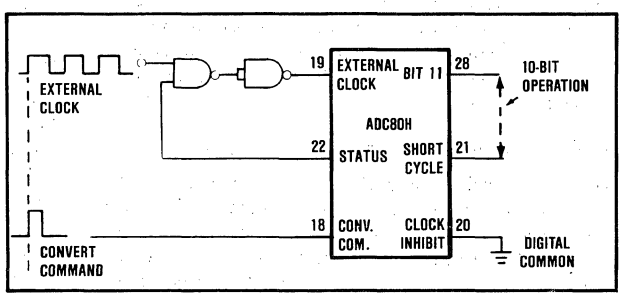


FIGURE 7. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

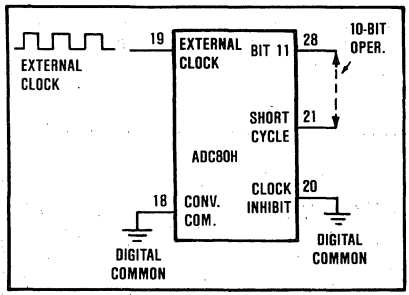


FIGURE 8. Continuous Conversion with External Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

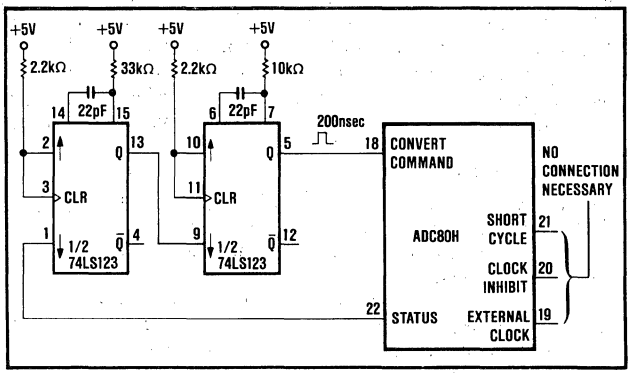


FIGURE 9. Continuous Conversion with 600nsec between Conversions. (Circuit insures that conversion will start when power is applied.)

tions not requiring full 12-bit resolution. In these situations, the short-cycle pin should be connected to the bit output pin of the next bit after the desired resolution. For example, when 10-bit resolution is desired, pin 21 is connected to pin 28 (bit 11). In this example, the conversion cycle terminates and status is reset after the bit 10 decision. Short-cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times (with internal clock) are shown in Table III. Also shown are recommended minimum conversion times (external clock) for these conversion lengths to obtain the stated accuracies. The ADC80H is not factory-tested for these external clock conversion speeds and the product is not guaranteed to achieve the stated accuracies under these operating conditions; the recommended values are offered as an aid to the user.

TABLE III. Short-Cycle Connections and Conversion Times for 8-, 10-, and 12-Bit Resolutions—ADC80H.

Resolution (Bits)	12	10	8
Connect pin 21 to	Pin 9 or NC	Pin 28	Pin 30
Maximum Conversion Time[1] Internal Clock (μsec)	25	22	18
Minimum Conversion Time[1] External Clock (μsec)	15	13	10
Maximum Linearity Error At +25°C (% of FSR)	0.012	0.048	0.20

NOTE: (1) Conversion time to maintain ±1/2LSB linearity error.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table IV is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

TABLE IV. Screening Flow for ADC80H-AH-12Q

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Electrical Test	Burr-Brown test procedure	
Burn-in	1015, B	160 hour, +125°C, steady-state
Hermeticity: Fine Leak Gross Leak	1014, A1 or A2 1014, C	5×10^{-7} atm cc/sec bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	Burr-Brown QC5150	

BURR-BROWN®

ADC84
ADC85

For a /883B version of this product, see DAC87/883B in the Military Products section.

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **COMPACT DESIGN - Self-contained with internal clock, comparator, reference, and input buffer amplifier 32-pin ceramic or hermetic metal package**
- **FAST CONVERSION SPEEDS**
  Provide Fast Signal Sampling Rates
  12-bits - 10μsec, 10-bits - 6μsec
  Faster conversion speeds obtainable with "Short-Cycling" and adjustable clock rate
- **LOW COST - ADC84KG-12**

DESCRIPTION

The ADC84 and ADC85 families of 10- and 12-bit analog-to-digital converters utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a compact 32-pin dual-in-line packages.

Complete with internal reference and input buffer amplifier, they offer versatility and performance formerly offered only in larger modular or rack-mount packages.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V. Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.012% (±1/2LSB).

The fast conversion speeds of 10μsec for 12-bit and 6μsec for 10-bit resolution make these ADC's excellent for a wide range of applications where system throughput sampling rates from 100kHz to 120kHz are required. In addition, they may be short cycled and the clock rate control may be used to obtain faster conversion speeds at low resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Power supply voltages are ±15VDC and +5VDC.

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DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC84 and ADC85 are also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that these converters will have no missing codes over a specified temperture range.

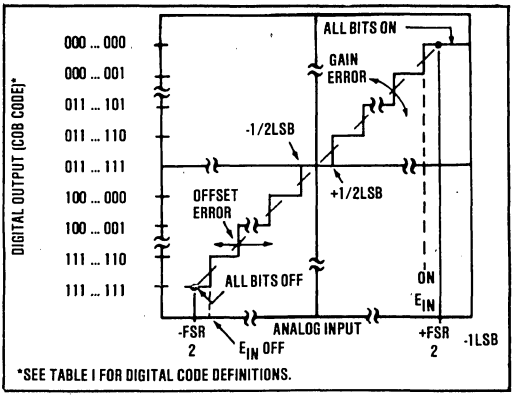


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram of the ADC's (see Figure 2) assumes an analog input such that the positive true digital word 100110001001 exists. The output will be complementary as shown in Figure 2 (011001110110 is the digital output).

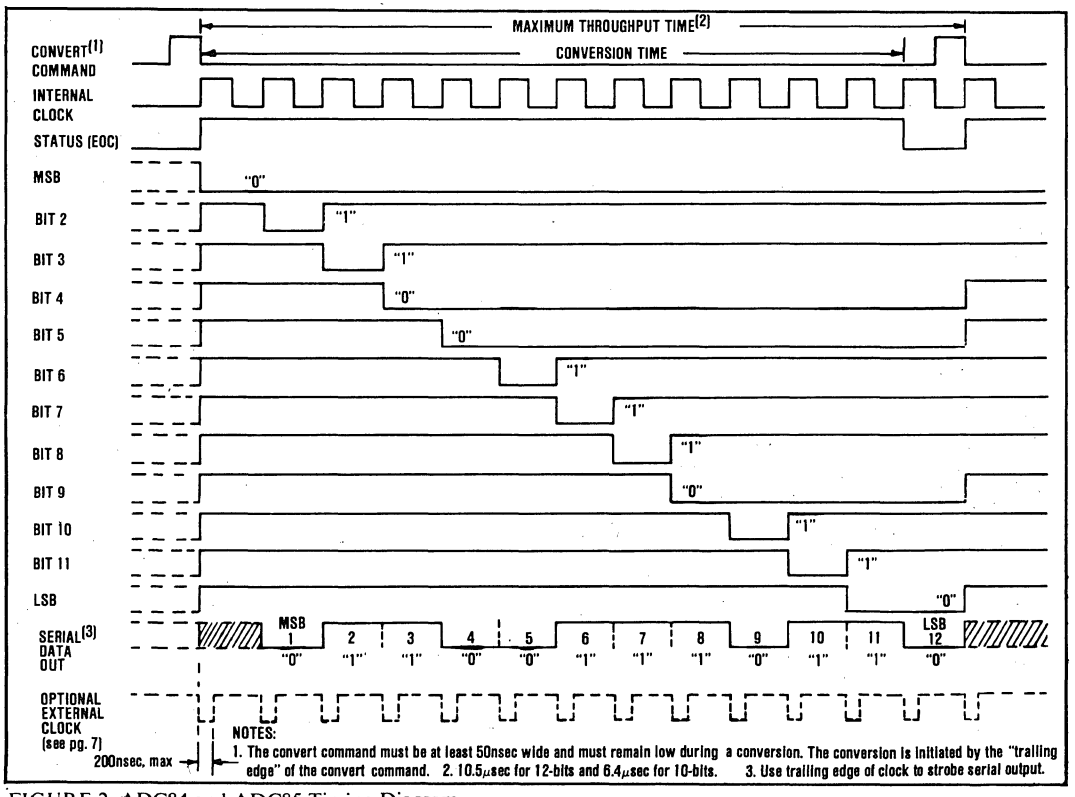


FIGURE 2. ADC84 and ADC85 Timing Diagram.

SPECIFICATIONS

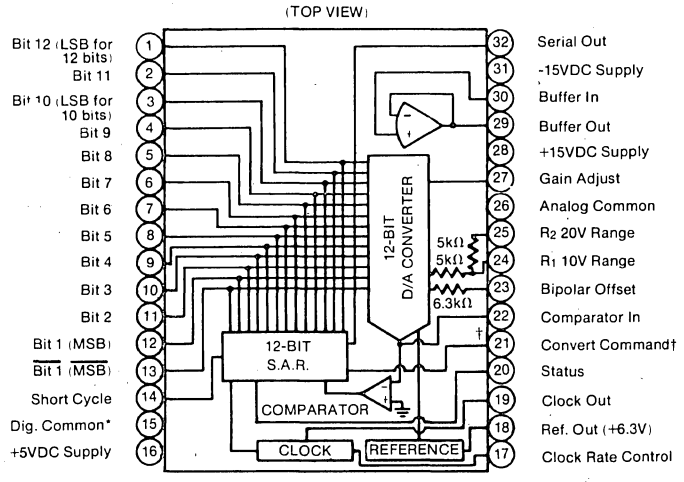
ELECTRICAL

Typical at +25°C and rated power supplies otherwise noted.

MODEL	ADC85		ADC85C		ADC84KG		UNITS
RESOLUTION	10	12	10	12	10	12	BITS
INPUT							
ANALOG INPUTS							
Voltages Ranges							
Bipolar	±2.5, ±5, ±10						V
Unipolar	0 to +5, 0 to +10						V
Impedance (Direct Input)							
0 to +5V, ±2.5V	2.5						kΩ
0 to +10V, ±5V	5						kΩ
±10V	10						kΩ
Buffer Amplifier							
Impedance, min	100						MΩ
Bias Current	50						nA
Settling Time							
to 0.01% for 20V step[1]	2						µsec
DIGITAL INPUTS[2]							
Convert Command	Positive pulse 50nsec wide, min. Trailing Edge "1" to "0" initiates conversion						
Logic Loading	1						TTL Load
External Clock	See External Clock paragraph						
TRANSFER CHARACTERISTICS							
ERROR							%
Gain Error	±0.1 (Adjustable to zero)						
Offset Error	Adjustable to zero						% of FSR[3]
Unipolar	±0.05						% of FSR
Bipolar	±0.1						% of FSR
Linearity Error, max[4]	±0.048	±0.012	±0.048	±0.012	±0.048	±0.012	% of FSR
Inherent Quantization Error	±1/2						LSB
Differential Linearity Error	±1/2						LSB
No Missing Codes	-25 to +85	0 to +70	0 to +70	0 to +70	0 to +70	0 to +70	°C
Power Supply Sensitivity							
±15VDC	±0.004						% of FSR/%V_S
+5VDC	±0.001						% of FSR/%V_S
DRIFT							
Specification Temperature Range	-25 to +85		0 to +70		0 to +70		°C
Gain, max	±20	±15	±40	±25		±30	ppm/°C
Offset							
Unipolar	±3	±3	±3	±3	±3	±3	ppm of FSR/°C
Bipolar	±10	±7	±20	±12	±15	±15	ppm of FSR/°C
Linearity, max	±3	±2	±3	±3	±3	±3	ppm of FSR/°C
Monotonicity	Guaranteed						
CONVERSION SPEED (max)[5][6]	6	10	6	10	6	10	µsec
OUTPUT							
DIGITAL DATA							
All codes complementary							
Parallel Output Codes[7]							
Unipolar	CSB						
Bipolar	COB, CTC						
Output Drive	2						TTL Loads
Serial Data Codes (NRZ)	CSB, COB						
Output Drive	2						TTL Loads
Status	Logic "1" during conversion						
Status Output Drive	2						TTL Loads
Internal Clock							
Clock Output Drive	2						TTL Loads
Frequency[6]	1.9	1.35	1.9	1.35	1.9	1.35	MHz
INTERNAL REF. VOLTAGE	6.3						V
Max External Current With no degradation of Specifications	200						µA
Tempco of Drift, max	±5	±5	±10	±10	±20	±20	ppm/°C
POWER REQUIREMENTS							
Rated Voltages	±15, +5						V
Range for Rated Accuracy	4.75 to 5.25 and ±14.5 to ±15.5						V
Supply Drain +15VDC	+45				+45		mA
-15VDC	-35				-35		mA
+5VDC	+120				+70		mA
TEMPERATURE RANGE							
Specification	-25 to +85		0 to +70		0 to +70		°C
Operating (derated specs)	-55 to +85 (110°C case Temp.						°C
Storage	-55 to +125		-55 to +125		-55 to +125		°C
PACKAGE (see Mechanical Specifications)	Metal (Hermetic)				Ceramic		

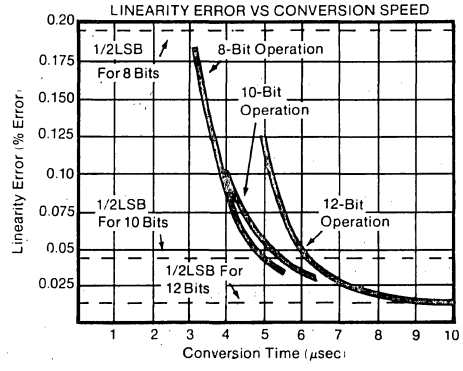
NOTES:
1. This settling time adds to conversion speed when buffer is connected to input.
2. DTL/TTL compatible; i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V, min for inputs. For digital outputs, Logic "0" = +0.4V max, Logic "1" = 2.4V, min.
3. FSR means Full Scale Range - for example, unit connected for ±10V range has 20V FSR.
4. Error shown is the same as ±1/2LSB max linearity error in % of FSR.
5. Conversion time may be shortened with "short cycle" set for lower resolution. See Table III.
6. Internal Clock is externally adjustable.
7. See Table II. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.

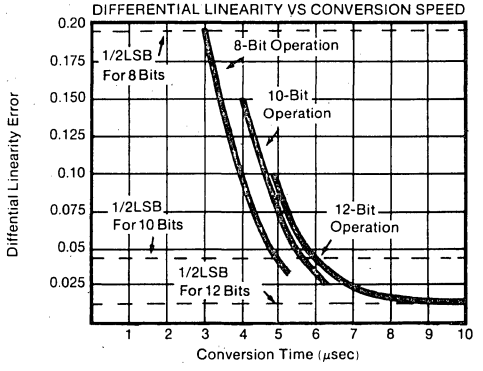
CONNECTION DIAGRAM

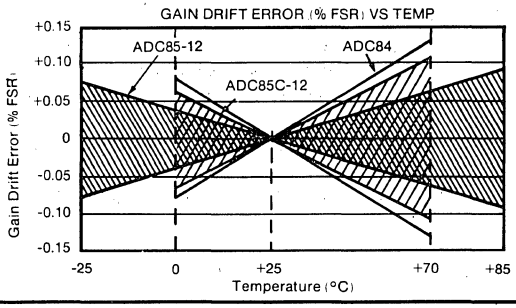


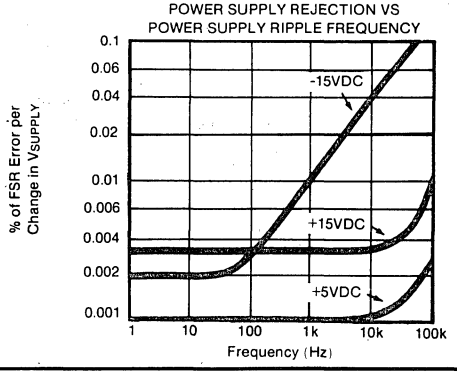
*Digital Common is internally connected to case. (ADC85 and ADC85C only)
† If an external clock is used, connect the clock to Pin-21 (conv. command). (See Figure 2 and External Clock paragraph).

TYPICAL PERFORMANCE CURVES









DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC84 and ADC85 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input singal ranges.

Table I describes the LSB, transition values and code definitions for each possible analog input signal range for 8-, 10-, and 12-bit resolutions.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES					
Analog Input Voltage Ranges	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB* or CTC***	COB* or CTC***	COB* or CTC***	CSB**	CSB**
One Least Significant Bit (LSB)	FSR	20V	10V	5V	10V	5V
	2^n	2^n	2^n	2^n	2^n	2^n
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values						
MSB LSB						
000 ... 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5 -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 ... 111	MIL Scale	0	0	0	+5V	+2.5V
111 ... 110	-Full Scale	-10V +1/2LSB	-5V + 1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB

*COB = Complementary Offset Binary
**CSB = Complementary Straight Binary
***CTC = Complementary Two's complement - obtained by using the complement of the most-significant bit (MSB). MSB is available on pin-13.
****Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC84 and ADC85 are specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors and conversion speed effects on accuracy. These ADC's are factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown on next page.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature; they are gain, offset and linearity drift. The worst-case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\epsilon g^2 + \epsilon o^2 + \epsilon e^2}$$

where ϵg = gain drift error (ppm/°C)
ϵo = offset drift error (ppm of FSR/°C)
ϵe = linearity error (ppm of FSR/°C)

For the ADC85-12 operating in the unipolar mode the total RSS drift is ±15.42ppm/°C and for bipolar operation the total RSS drift is ±16.7ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC84 and ADC85 are shown in Typical Performance Curves.

The conversion speeds are specified for a maximum linearity error of ±1/2LSB with the internal clock. Faster conversion speeds are possible (see Clock Rate Control Alternate Connections).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC84 and the ADC85 power supply sensitivity is specified for ±0.003% of FSR/%V_S for ±15VDC supplies and ±0.0015% of FSR/%V_S for +5VDC supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with these ADC's. See Layout Precautions and Power Supply Decoupling on next page.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC84 and ADC85, but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 3 to obtain noise free operation. These capacitors should be located close to the ADC. 1μF electrolytic type capacitors should be bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

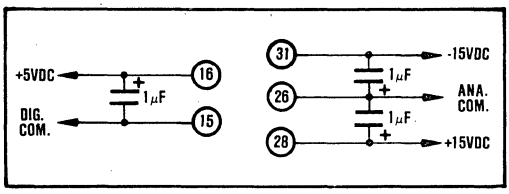


FIGURE 3. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 4 for circuit details.

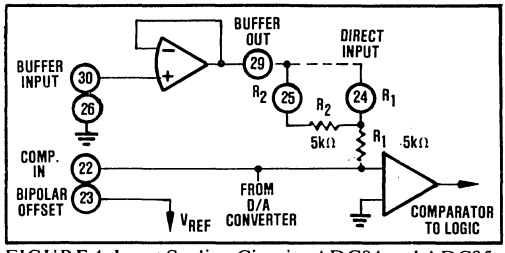


FIGURE 4. Input Scaling Circuit - ADC84 and ADC85.

TABLE II. ADC84 and ADC85 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Buffered Input* Connect Pin 29 To Pin	For Direct Input (see note) Connect Input Signal To Pin
			Input		
±10V	COB or CTC	22	Signal**	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0 to +5V	CSB	26	Pin 22	24	24
0 to +10V	CSB	26	Open	24	24

*Connect to Pin 29 or input signal as shown in next two columns.
**The input signal is connected to Pin 30 if the buffer amplifier is used.
NOTE: If the buffer amplifier is not used, the input Pin 30 must be grounded (Pin 26).

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 5 and 6. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 27 (Gain Adjust) should be bypassed with 0.01μF to reduce noise pickup and Pin 22 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

Offset - Connect the Offset potentiometer as shown in Figure 5. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

Gain - Connect the Gain adjust potentiometer as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition voltage to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

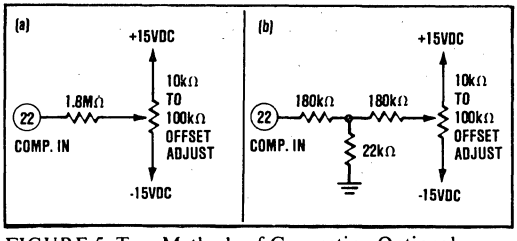


FIGURE 5. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range of Adjustment.

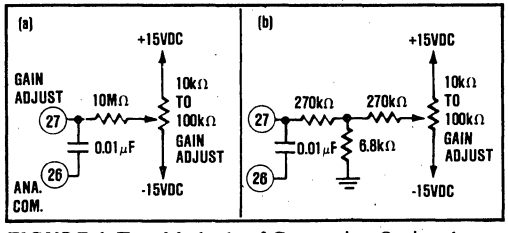


FIGURE 6. Two Methods of Connecting Optional Gain Adjust with a 0.6% Range of Adjustment.

CLOCK RATE CONTROL ALTERNATE CONNECTIONS

If adjustment of the Clock Rate is desired for faster conversion speeds, the Clock Rate Control may be connected to an external multiturn trim potentiometer with TCR of ±100ppm/°C or less as shown in Figures 7A and 7B. If the potentiometer is connected to -15VDC, conversion time can be increased as shown in Figure 8. If these adjustments are used, delete the connections shown in Table III for pin 17. See Typical Performance Curves for nonlinearity error vs. clock frequency, and Figure 8 for the effect of the control voltage on clock speed. Operation with clock rate control voltage of less than −1VDC is not recommended.

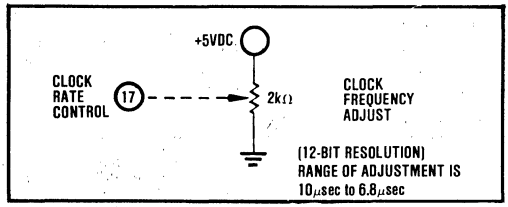


FIGURE 7A. 12-Bit Clock Rate Control Optional Fine Adjust.

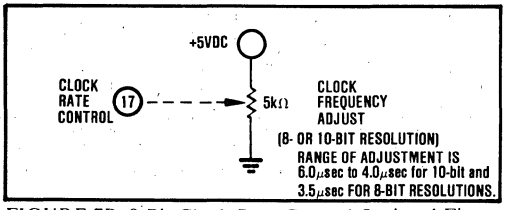


FIGURE 7B. 8-Bit Clock Rate Control Optional Fine Adjust.

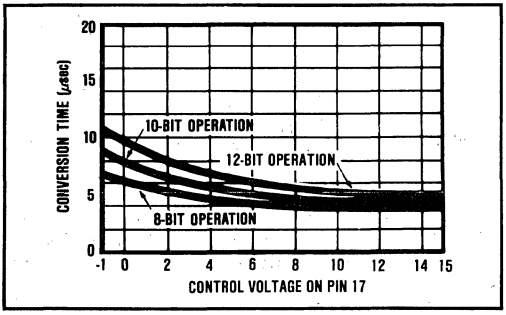


FIGURE 8. Conversion Time vs Clock Speed Control Voltage.

EXTERNAL CLOCK

If an external clock is used, connect the external clock to convert command, pin 21. The convert command shown in Figure 2 is not used. After each conversion is completed, a new conversion cycle will automatically start of the first falling edge of the external clock following the completion of conversion. The clock-out signal will remain as shown in Figure 2 even if an external clock is used. The external clock pulse must be a negative going pulse with a width between 100nsec and 200nsec as shown in Figure 2.

ADDITIONAL CONNECTIONS REQUIRED

The ADC84 and ADC85 may be operated at faster speeds for resolutions less than 12 bits by connecting the Short Cycle input, pin 14, as shown in Table III. Conversion speeds, linearity and resolution are shown for reference. Specifications for 10-bit units assume connections as shown below.

TABLE III. Short Cycle Connections and Specifications for 8- to 12-Bit Resolution.

RESOLUTION (Bits)	12	10	8
Connect Pin 17 to (1)	Pin 15	Pin 16	Pin 28
Connect Pin 14 to	Pin 16	Pin 2	Pin 4
Maximum Conversion Speed (μsec)(2)	10	6	4
Maximum Nonlinearity at 25°C (% of FSR)	0.012(3)	0.048(4)	0.20(4)

NOTES:
1. Connect only if clock rate control is not used.
2. Max. conversion speeds to maintain ±1/2LSB nonlinearity error.
3. 12-bit models only.
4. 10- or 12-bit models.

CONVERTER INITIALIZATION

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

OUTPUT DRIVE

Normally all ADC84 and ADC85 logic outputs will drive 2 standard TTL-loads; however, if long digital lines must be driven, external logic buffers are recommended.

HEAT DISSIPATION

The ADC84 and ADC85 dissipate approximately 1.2W and the packages have a case-to-ambient thermal resistance (Θ_{CA} should be lowered by a heat-sink or by forced air over the surface of the package). See Figure 9 for Θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat-sink compound. On a 0.062-inch thick PC card with 16 square-inch minimum area, this technique will allow operation to 85°C.

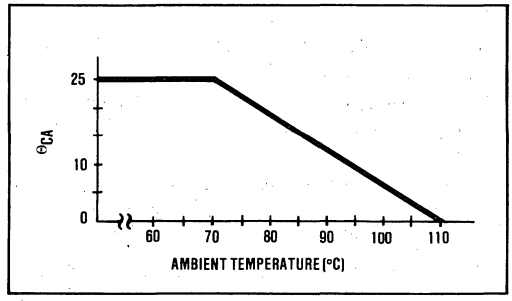


FIGURE 9. θ_{CA} Requirement Above 70°C.

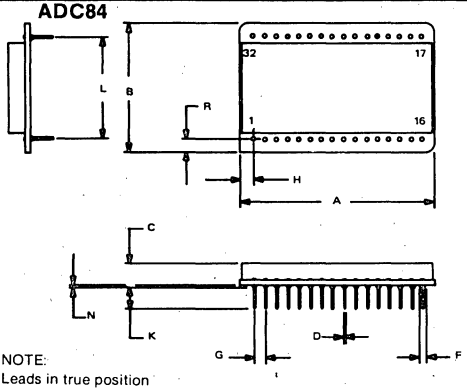
HIGH RELIABILITY A/D CONVERTERS

Each of the ADC85 models are available screened to the requirements of the Burr-Brown Q-Program, which consists of a sequence of thermal and mechanical stress procedures, plus a verification of package hermeticity. The diagram below illustrates the screening sequence which is applied to 100% of the Q-Screened A/D converters.

High Temp. Storage (MIL-STD-883)	Temperature Cycling (MIL-STD-883)	Hermeticity Gross Leak (MIL-STD-883)	Hermiticity Fine Leak (MIL-STD-883)	Burn-In (MIL-STD-883)	Centrifuge (MIL-STD-883)
Method 1008 Condition B +125°C 24 Hours	Method 1010 Condition B -55 to +25°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5×10^{-7}cc/sec	Method 1015 Condition D 168 Hours +70°C (ADC85C) +85°C (ADC85)	Method 2001 2,000 G Y_1 Axis

MECHANICAL

ADC84

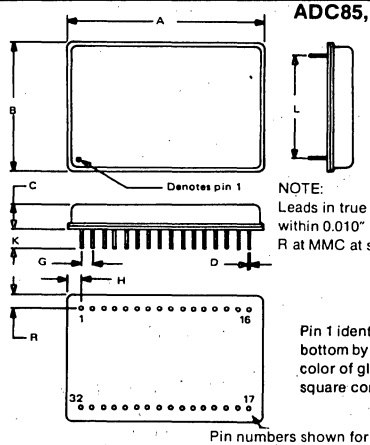


NOTE:
Leads in true position within 0.010" (0.255mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
CASE: Ceramic
MATING CONNECTOR: 2302MC
Set of two 16-pin strips
WEIGHT: 13 grams (0.46 oz.)

ADC85, ADC85C



NOTE:
Leads in true position within 0.010" (0.255mm) R at MMC at seating plane.

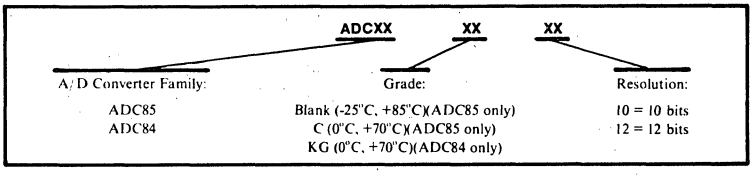
Pin 1 identified on bottom by contrasting color of glass or square corner.

Pin numbers shown for reference only. Numbers may not be marked on package.

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
CASE: Kovar, Nickel plated
MATING CONNECTOR: 2302MC
Set of two 16-pin strips
WEIGHT: 13 grams (0.46 oz.)

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

ORDERING INFORMATION



BURR-BROWN®

ADC574A

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE
- IMPROVED PERFORMANCE SECOND SOURCE FOR 574A-TYPE A/D CONVERTERS
  - 25μs Maximum Conversion Time
  - 150ns Bus Access Time
  - A_0 Input: Bus Contention During Read Operation Eliminated
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- NO MISSING CODES OVER TEMPERATURE
  - 0°C to +75°C: ADC574AJH, KH Grades
  - −55°C to +125°C: ADC574ASH, TH Grades

DESCRIPTION

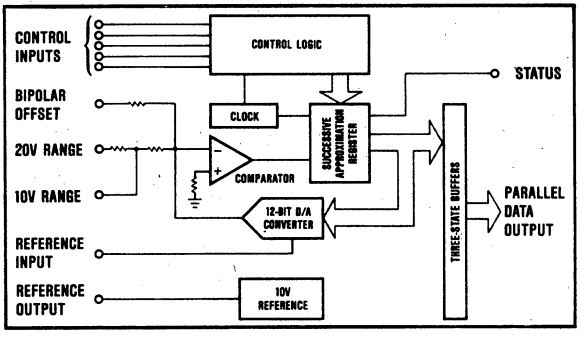
The ADC574A is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally-trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 20μs typical.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC574A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a hermetic 28-pin side-brazed ceramic DIP.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC574AJH, ADC574ASH			ADC574AKH, ADC574ATH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			•	Bits
INPUT							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			•		V
Bipolar		±5, ±10			•		V
Impedance: 0 to +10V, ±5V	3.7	5	6.3	•	•	•	kΩ
±10V, 0V to +20V	7.5	10	12.5	•	•	•	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2.4[1]		+5.5	•		•	V
Logic 0	−0.5		+0.8	•		•	V
Current, 0.0V ≤ V_{IN} ≤ 5.0V	−5	0.1	+5	•	•	•	μA
Capacitance		5			•		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			•	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error[2] (adjustable to zero)			±0.3			•	% of FS[3]
No Missing Codes Resolution	11			12			Bits
Inherent Quantization Error		±1/2			•		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	% of FS
S, T Grades			±1			•	% of FS
Full-Scale Calibration Error							
Without Initial adjustment[2]: J, K Grades			±0.5			±0.4	% of FS
S, T Grades			±0.8			±0.6	% of FS
Adjusted to zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution	11			12			Bits
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
−16.5V < V_{EE} < −13.5V or −12.6V < V_{EE} < −11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5.5V			±1/2			•	LSB
CONVERSION TIME[4]							
8-Bit Cycle	10	13	17	•	•	•	μs
12-Bit Cycle	15	20	25	•	•	•	μs
DRIFT							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Change over Temperature Range, All Grades			±2			±1	LSB
Bipolar Offset, All Grades			±10			±5	ppm/°C
Change over Temperature Range: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Change over Temperature Range: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
OUTPUT							
DIGITAL (DB_{11} − DB_0, STATUS)							
Over Temperature Range							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{sink} = 1.6mA)			+0.4			•	V
Logic 1 (I_{source} = 500μA)	+2.4			•			V
Leakage, Data Bits Only, High-Z State	−5	0.1	+5	•	•	•	μA
Capacitance		5			•		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10.1	•	•	•	V
Source Current Available for External Loads[5]	2.0			•			mA

ELECTRICAL (CONT)

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC574AJH, ADC574ASH			ADC574AKH, ADC574ATH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	*		*	V
V_{EE}	−11.4		−16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		11	15		*	*	mA
I_{EE}		21	28		*	*	mA
I_{LOGIC}		7	15		*	*	mA
Power Dissipation (±15V Supplies)		515	720		*	*	mW
TEMPERATURE RANGE (Ambient)							
Specification: J, K Grades	0		+75	*		*	°C
S, T Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

*Same specification as grade to the immediate left.

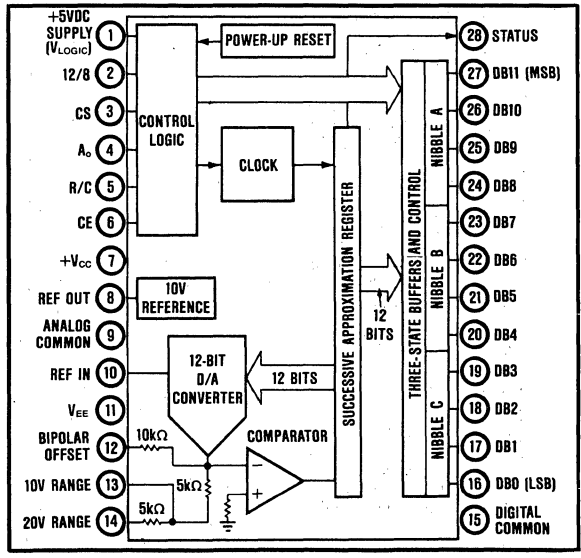
NOTES: (1) Although this guaranteed threshold is higher than the standard TTL guaranteed level (+2.0V), bus loading is much less. Typical input current is only 0.25% of a standard TTL load. (2) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C (see "Optional External Full Scale and Offset Adjustments" section). (3) FS in this specification table means Full-Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. Use of the term Full Scale for these specifications instead of Full-Scale Range is consistent with other vendors' 574 and 574A specification tables. (4) See "Controlling the ADC574A" section for detailed information concerning digital timing. (5) External loading must be constant during conversion. When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the reference output.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/8, R/C)
to Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$)
to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
REF OUT ..... Indefinite Short to Common, Momentary Short to V_{CC}
Chip Temperature: J, K, L Grades ..... +100°C
S, T, U Grades ..... +150°C
Power Dissipation 1000mW
Lead Temperature, Soldering ..... +300°C, 10sec
Thermal Resistance, θ_{JA} ..... 48°C/W

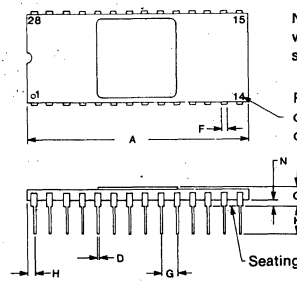
CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

CONNECTION DIAGRAM



MECHANICAL

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.386	1.414	35.20	35.92
C	.108	.166	2.74	4.22
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	- -	10°	- -	10°
N	.025	.060	0.64	1.52



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

CASE: Ceramic, hermetic
MATING CONNECTOR: 2803MC
WEIGHT: 4.8 grams (0.17oz.)

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 1).

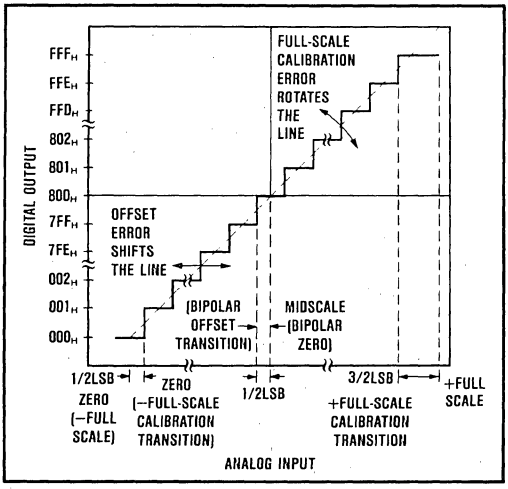


FIGURE 1. ADC574A Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of −10V is 2.44mV below the first code transition (000_H to 001_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Table I).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur.

ADC57A KH and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An ADC574A connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC574A specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC574A is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC574A assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply

TABLE I. Input Voltages, Transition Values, and LSB Values.

Binary (BIN) Output	Input Voltage Range and LSB Values				
Analog Input Voltage Range	Defined As:	±10V	±5V	0 to +10V	0 to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	$n = 8$	78.13mV	39.06mV	39.06mV	78.13mV
	$n = 12$	4.88mV	2.44mV	2.44mV	4.88mV
Output Transition Values					
FFE_H to FFF_H	+ Full-Scale Calibration	+10V − 3/2LSB	+5V − 3/2LSB	+10V − 3/2LSB	+20V − 3/2LSB
$7FFF_H$ to 800_H	Midscale Calibration (Bipolar Offset)	0 − 1/2LSB	0 − 1/2LSB	+5V − 1/2LSB	+10V −1/2LSB
000_H to 001_H	Zero Calibration (− Full-Scale Calibration)	−10V + 1/2LSB	−5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

voltage deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given otuput code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC574A, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. This single common path will typically carry about 1.5mA of current out of the converter. Code-dependent currents do not flow in analog (pin 9) or digital (pin 15) commons. DC currents that flow are typically +7mA in pin 9 and −5.5mA in pin 15.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC574A as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC574A will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC574A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustments are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48V (5mV LSB) input range, insert a 200Ω potentiometer in series with pin 13 for the 10.24V range, or a 500Ω potentiometer in series with pin 14 for the 20.48V range. Use a fixed 50Ω, 1% resistor for R_2 (Figures 2 and 3). Offset adjustment is still performed as described below. Full-scale adjustment is performed as described below but with adjustment performed using the input potentiometer instead of R_2.

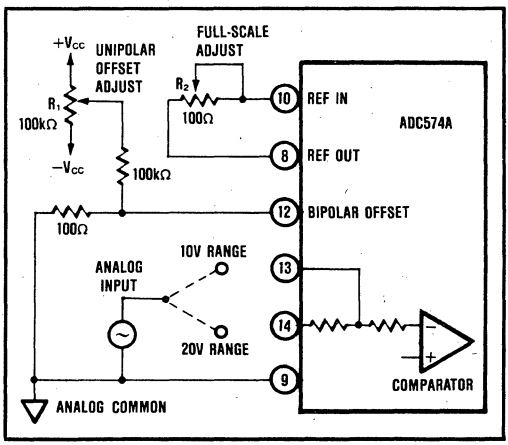


FIGURE 2. Unipolar Configuration.

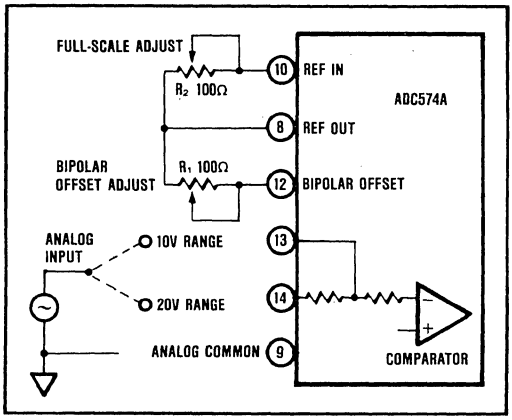


FIGURE 3. Bipolar Configuration.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC574A as shown in Figures 2 and 3 for unipolar and bipolar operation.

CALIBRATION PROCEDURE—UNIPOLAR RANGES

If adjustment of unipolar offset and full scale is not required, replace R_2 with a 50Ω, 1% metal film resistor and connect pin 12 to pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 2. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DBO ON (high). Adjust potentiometer R_1 until DBO is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1–DB11 are ON and DBO is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (−4.9988V for the ±5V range, −9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

CONTROLLING THE ADC574A

The Burr-Brown ADC574A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the ouptut data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/8, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The

TABLE II. ADC574A Control Line Functions.

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line.

TABLE III. Control Input Truth Table.

CE	$\overline{CS}$	R/$\overline{C}$	12/8	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50nsec.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the ouptut data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Table IV lists timing specifications for stand-alone operation.

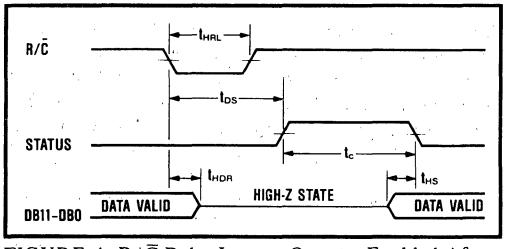


FIGURE 4. R/$\overline{C}$ Pulse Low — Outputs Enabled After Conversion.

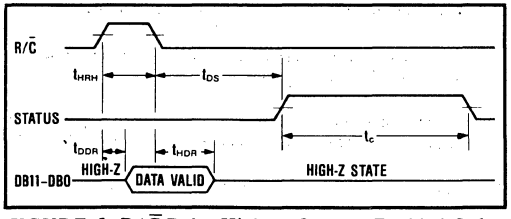


FIGURE 5. R/$\overline{C}$ Pulse High — Outputs Enabled Only While R/$\overline{C}$ Is High.

TABLE IV. Stand-Alone Mode Timing.

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	500	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0-DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate conversion by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50nsec prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

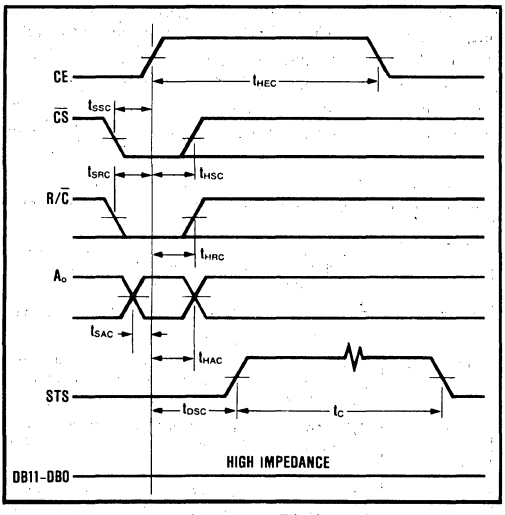


FIGURE 6. Conversion Cycle Timing.

TABLE V. Timing Specifications.

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS delay from CE		100	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE setup	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0	0		ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time, 12 bit cycle	15	20	25	μs
	8 bit cycle	10	13	17	μs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE setup	0	0		ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0	0		ns
t_{HRR}	R/$\overline{C}$ high after CE low	0	0		ns
t_{HAR}	A_0 valid after CE low	50	25		ns
t_{HS}	STS delay after data valid	300	500	1000	ns

NOTE: Specifications are at +25°C and measured at 50% level of transitions.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 7 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0–DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When 12/$\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest

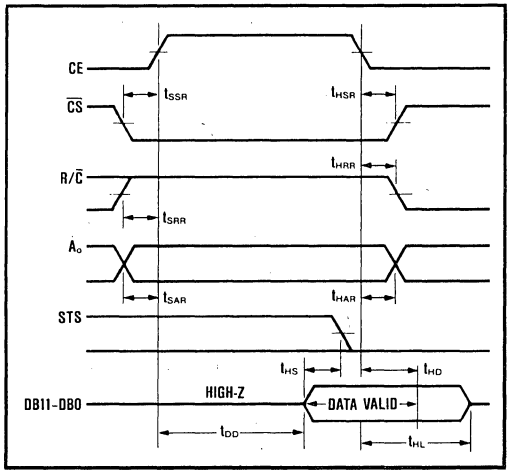


FIGURE 7. Read Cycle Timing.

accomplished by the state of A_0 during the read cycle. Connection of the ADC574A to an 8-bit bus for transfer of left-justified data is illustrated in Figure 8. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is low, the byte addressed contains the 8MSBs. When A_0 is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC574A guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as 1.15μsec (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Figure 7 for these timing relationships.

ORDERING INFORMATION

Model	Temperature Range	Linearity Error, max (T_{MIN} to T_{MAX})	Resolution, No Missing Codes (T_{MIN} to T_{MAX})	Full-Scale TC, max (ppm/°C)
ADC574AJH	0°C to +75°C	±1LSB	11 Bits	±45
ADC574AKH	0°C to +75°C	±1/2LSB	12 Bits	±25
ADC574ASH	−55°C to +125°C	±1LSB	11 Bits	±50
ADC574ATH	−55°C to +125°C	±1LSB	12 Bits	±25

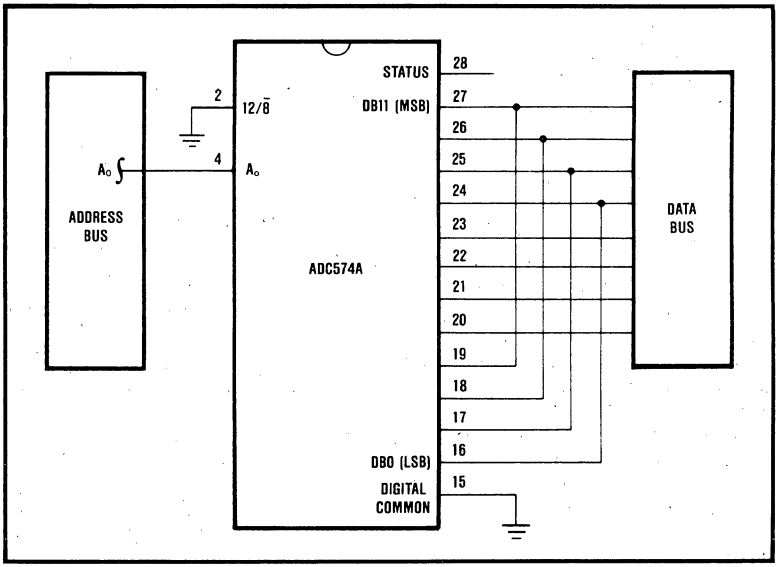


FIGURE 9. Connection to an 8-bit Bus.

BURR-BROWN®

ADC600

ADVANCE INFORMATION
Subject to Change

12-BIT
ULTRA-HIGH SPEED A/D CONVERTER

FEATURES

- 12 BITS AT 10MHz WORD RATE
- SELF-CONTAINED SAMPLE/HOLD: ±25ps Aperture Uncertainty
- SIGNAL-TO-NOISE RATIO: 70dB
- INPUT BANDWIDTH: 50MHz
- POWER DISSIPATION: <10W
- CONVENIENT PC-BOARD-MOUNTED MODULE: 3.75" × 4.5"

DESCRIPTION

The Burr-Brown model ADC600 is an ultra-high speed 12-bit resolution A/D converter capable of digitizing signals at rates up through 10 million samples-per-second. Burr-Brown's unique mix of monolithic and hybrid technologies permits this breakthrough in speed, size, power dissipation, and ease of use.

The conversion technique is two-step subranging with digital error correction. Within the A/D are all the required circuits: sample/hold amplifier, encoders, reference D/A converter, and timing circuits. The ADC600 requires only an external CONVERT command pulse and external power supplies for operation. No external parts are required.

The ADC600 is constructed on a four-layer printed circuit card which is intended for mounting on a system PC board. It occupies only 17 square inches.

The ADC600 is the best performing converter available for digital oscilloscope, radar, spectrum analyzer, high resolution video, and telecommunications applications.

Figure 1 is the timing diagram. The ADC600 uses a two-step subranging with digital error correction conversion technique. Therefore valid digital data output is delayed more than a full CONVERT command cycle from the sampling time for that data. On the first conversion after power-up, there is no valid data for 136ns.

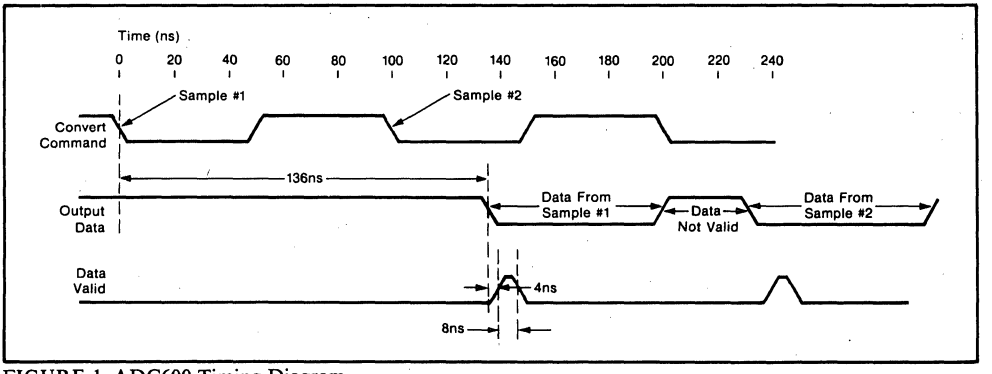


FIGURE 1. ADC600 Timing Diagram.

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SPECIFICATIONS (Preliminary)

ELECTRICAL

At +25°C and rated power supplies, 10MHz sampling rate and after 15 minutes warmup, unless otherwise noted.

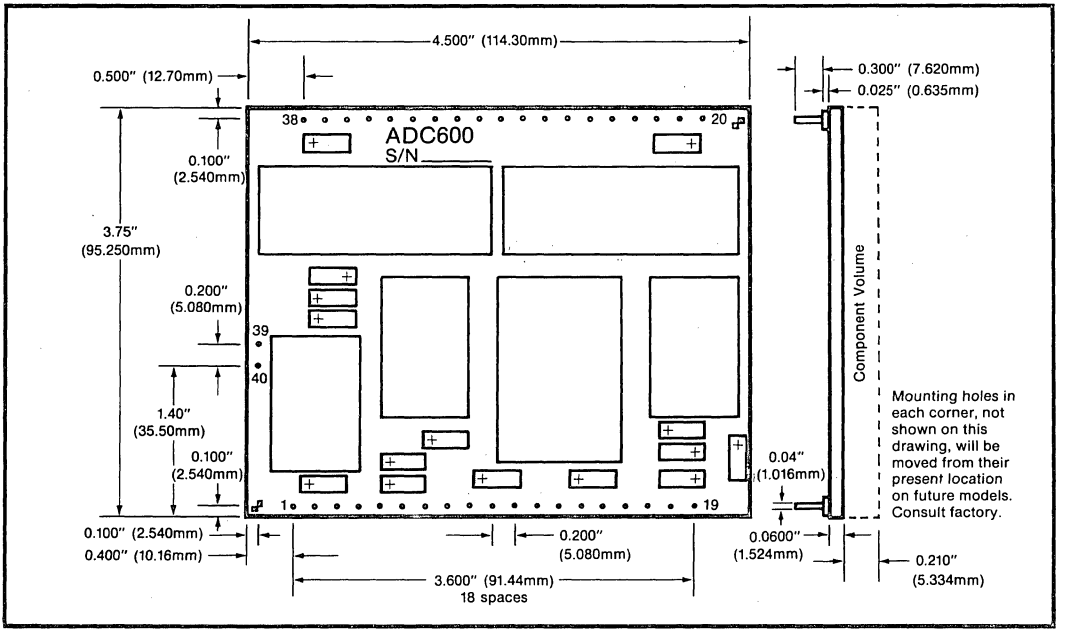
PARAMETER	ADC600K MIN	ADC600K TYP	ADC600K MAX	UNITS
RESOLUTION			12	Bits
INPUTS				
ANALOG				
Voltage Range		±1.25		V
Impedance		1.5		MΩ
Capacitance		5		pF
DIGITAL				
Convert Command		Negative Pulse 10ns (min) Wide (1 to 0) Initiates Conversion		
Logic Loading		ECL 10K-Compatible		
LOW FREQUENCY TRANSFER CHARACTERISTICS (f_{IN} = 200Hz)				
ACCURACY				
Gain Error		±0.1	±0.5	%
Offset Error		±0.1	±0.5	% of FSR[1]
Linearity Error			1.25	LSB
Differential Linearity Error[2]				
68.3% of all codes will not exceed			0.25	±LSB
99.7% of all codes will not exceed			1.00	±LSB
No codes will exceed			+1.25, −1	±LSB
No Missing Codes		Guaranteed		
SAMPLING RATE	10.0			MHz
CONVERSION TIME[3] (time from start convert to status)		130	150	ns
DYNAMIC TRANSFER CHARACTERISTICS				
Differential Linearity Error (f_{IN} = 4.9MHz):				
68.3% of all codes will not exceed			0.50	±LSB
99.7% of all codes will not exceed			1.50	±LSB
No codes will exceed			2.00	±LSB
Harmonic Distortion:				
f_{IN} = DC to 1MHz		70		dB below FSR
f_{IN} = 1MHz to 5MHz		65		dB below FSR
Two-tone Linearity at f_{IN} = 60kHz, 62kHz		70		dB below FSR
= 2.498MHz, 2.500MHz		65		dB below FSR
= 4.996MHz, 4.998MHz		60		dB below FSR
Signal-to-Noise Ratio[4]		70		dB
Aperture Time		6		ns
Aperture Uncertainty			±25	ps
Input Bandwidth (at 40dB below FS)		50		MHz
DRIFT (f_{IN} = 200Hz)				
Gain		±30		ppm/°C
Offset		±50		µV/°C
Linearity Error 0°C to +70°C			1.5	±LSB
Differential Linearity Error 0°C to +70°C:				
63% of all codes will not exceed			0.50	±LSB
98% of all codes will not exceed			1.25	±LSB
No codes will exceed			1.5	±LSB
Sampling Rate, 0°C to +70°C	10			MHz
DIGITAL OUTPUT				
Parallel, Output Coding		Offset Binary; Binary Two's Complement		
Output Drive (data, data valid)	6			ECL Loads
End of Conversion Delay (time from output data to data valid)	5	35		ns
Rise and Fall Time (20% to 80%)		5		ns
Data Valid Pulse Width	5	8		ns
POWER SUPPLY REQUIREMENTS				
Rated Voltage: $+V_{CC}$ (+15V)	+14.25	+15	+15.75	V
$-V_{CC}$ (−15V)	−14.25	−15	−15.75	V
V_{DD1} (+5V)	+4.75	+5	+5.25	V
V_{DD2} (−5.2V)	−4.95	−5.2	−5.46	V
Supply Drain: $+V_{CC}$ (+15V)		75		mA
$-V_{CC}$ (−15V)		45		mA
V_{DD1} (+5V)		400		mA
V_{DD2} (−5.2V)		900		mA
Power Consumption		8.5		W

ELECTRICAL (cont.)

PARAMETER	ADC600K MIN	ADC600K TYP	ADC600K MAX	UNITS
TEMPERATURE RANGE (Ambient)				
Specification	0		+70	°C
Storage	−25		+85	°C

NOTES: (1) FSR means Full-Scale Range, 2.5V for ADC600. (2) Differential Linearity Error is a statistical measurement taken over thousands of samples and evaluated by histogram techniques. (3) Converter uses two-step techniques. S/H acquisition time overlaps the conversion time except on the first conversion. (4) rms signal-to-noise ratio with 500kHz analog input.

MECHANICAL



PIN ASSIGNMENTS

1	Common	21	Common
2	$-V_{CC}$ (−15V)	22	Data Valid
3	V_{DD2} (−5.2V)	23	Bit 12 (LSB)
4	V_{DD1} (+5V)	24	Bit 11
5	$+V_{CC}$ (+15V)	25	Bit 10
6	Common	26	Bit 9
7	V_{DD2} (−5.2V)	27	Bit 8
8	V_{DD1} (+5V)	28	Bit 7
9	Common	29	Bit 6
10	V_{DD2} (−5.2V)	30	Bit 5
11	Common	31	Bit 4
12	Common	32	Bit 3
13	$+V_{CC}$ (+15V)	33	Bit 2
14	$-V_{CC}$ (−15V)	34	Bit 1 (MSB)
15	V_{DD2} (−5.2V)	35	$\overline{\text{Bit 1 (MSB)}}$
16	V_{DD1} (+5V)	36	V_{DD2} (−5.2V)
17	Common	37	Common
18	V_{DD2} (−5.2V)	38	Convert Command
19	V_{DD1} (+5V)	39	Analog Input
20	V_{DD2} (−5.2V)	40	Analog Input Return

ORDERING INFORMATION

ADC600K

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BURR-BROWN®

ADC674A

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE
- IMPROVED PERFORMANCE SECOND SOURCE FOR 574A-TYPE A/D CONVERTERS
  - 15μs Maximum Conversion Time
  - 150ns Bus Access Time
  - A_0 Input: Bus Contention During Read Operation Eliminated
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- NO MISSING CODES OVER TEMPERATURE
  - 0°C to +75°C: ADC674AJH, KH Grades
  - −55°C to +125°C: ADC674ASH, TH Grades

DESCRIPTION

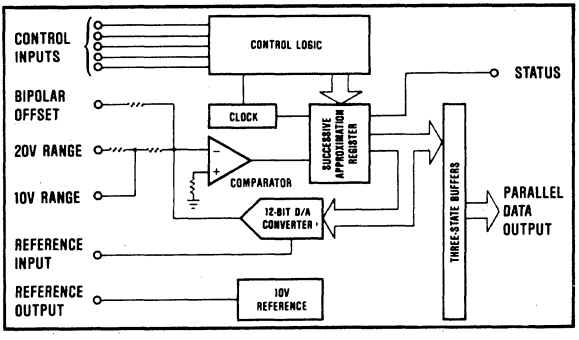
The ADC674A is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally-trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 15μsec maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC674A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a hermetic 28-pin side-brazed ceramic DIP.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC674AJH, ADC674ASH			ADC674AKH, ADC674ATH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			•	Bits
INPUT							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			•		V
Bipolar		±5, ±10			•		V
Impedance: 0 to +10V, ±5V	3.7	5	6.3	•	•	•	kΩ
±10V, 0V to +20V	7.5	10	12.5	•	•	•	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2.4[1]		+5.5	•		•	V
Logic 0	−0.5		+0.8	•		•	V
Current, 0.0V ≤ V_{IN} ≤ 5.0V	−5	0.1	+5	•	•	•	μA
Capacitance		5			•		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			•	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error[2]							
(adjustable to zero)			±0.3			•	% of FS[3]
No Missing Codes Resolution	11			12			Bits
Inherent Quantization Error		±1/2			•		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			•	LSB
Full-Scale Calibration Error							
Without Initial adjustment[2]: J, K Grades			±0.5			±0.4	% of FS
S, T Grades			±0.8			±0.6	% of FS
Adjusted to zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution	11			12			Bits
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
−16.5V < V_{EE} < −13.5V or −12.6V < V_{EE} < −11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5.5V			±1/2			•	LSB
CONVERSION TIME[4]							
8-Bit Cycle	6	8	10	•	•	•	μs
12-Bit Cycle	9	12	15	•	•	•	μs
DRIFT							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Change over Temperature Range, All Grades			±2			±1	LSB
Bipolar Offset, All Grades			±10			±5	ppm/°C
Change over Temperature Range: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Change over Temperature Range: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
OUTPUT							
DIGITAL (DB_{11} − DB_0 STATUS)							
Over Temperature Range							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{sink} = 1.6mA)			+0.4			•	V
Logic 1 (I_{source} = 500μA)	+2.4			•			V
Leakage, Data Bits Only, High-Z State	−5	0.1	+5	•	•	•	μA
Capacitance		5			•		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10.1	•	•	•	V
Source Current Available for External Loads[5]	2.0			•			mA

ELECTRICAL (CONT)

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC674AJH, ADC674ASH			ADC674AKH, ADC674ATH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	•		•	V
V_{EE}	−11.4		−16.5	•		•	V
V_{LOGIC}	+4.5		+5.5	•		•	V
Current: I_{CC}		11	15		•	•	mA
I_{EE}		21	28		•	•	mA
I_{LOGIC}		7	15		•	•	mA
Power Dissipation (±15V Supplies)		515	720		•	•	mW
TEMPERATURE RANGE (Ambient)							
Specification: J, K Grades	0		+75	•		•	°C
S, T Grades	−55		+125	•		•	°C
Storage	−65		+150	•		•	°C

*Same specification as grade to the immediate left.

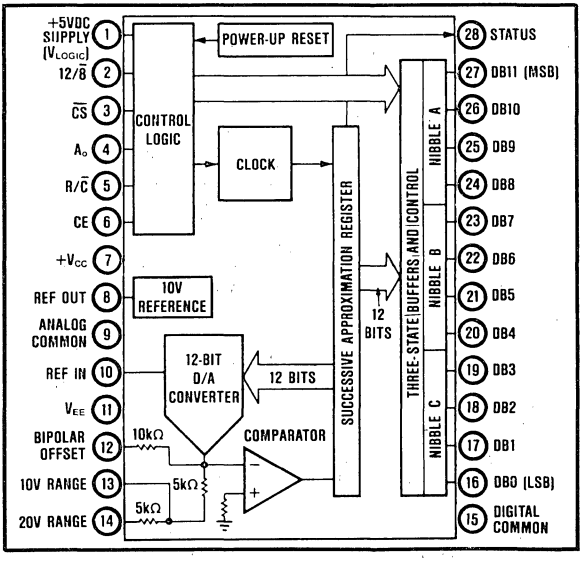
NOTES: (1) Although this guaranteed threshold is higher than the standard TTL guaranteed level (+2.0V), bus loading is much less. Typical input current is only 0.25% of a standard TTL load. (2) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C (see "Optional External Full Scale and Offset Adjustments" section). (3) FS in this specification table means Full-Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. Use of the term Full Scale for these specifications instead of Full-Scale Range is consistent with other vendors' 574 and 574A type specification tables. (4) See "Controlling the ADC674A" section for detailed information concerning digital timing. (5) External loading must be constant during conversion. When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the reference output.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$)
to Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$)
to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
REF OUT ..... Indefinite Short to Common, Momentary Short to V_{CC}
Chip Temperature: J, K Grades ..... +100°C
S, T Grades ..... +150°C
Power Dissipation 1000mW
Lead Temperature, Soldering ..... +300°C, 10s
Thermal Resistance, θ_{JA} ..... 48°C/W

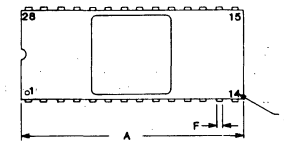
CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

CONNECTION DIAGRAM



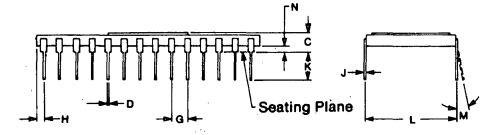
MECHANICAL

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.386	1.414	35.20	35.92
C	.108	.166	2.74	4.22
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	- -	10°	- -	10°
N	.025	.060	0.64	1.52



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



CASE: Ceramic, hermetic
MATING CONNECTOR: 2803MC
WEIGHT: 4.8 grams (0.17oz.)

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 1).

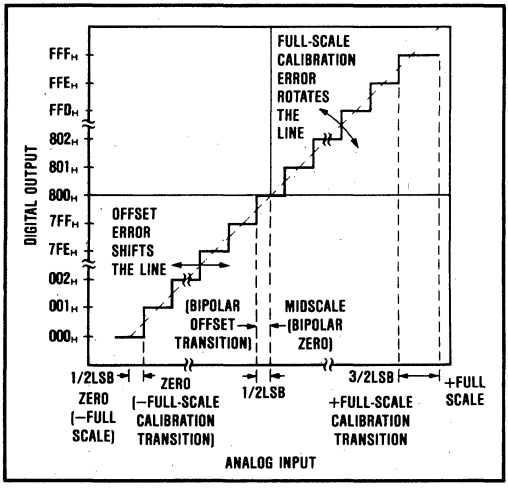


FIGURE 1. ADC674A Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of −10V is 2.44mV below the first code transition (000_H to 001_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Table I).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur.

ADC674A KH and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An ADC674A connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC674A specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC674A is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC674A assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply

TABLE I. Input Voltages, Transition Values, and LSB Values.

Binary (BIN) Output	Input Voltage Range and LSB Values				
Analog Input Voltage Range	Defined As:	±10V	±5V	0 to +10V	0 to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n = 12	4.88mV	2.44mV	2.44mV	4.88mV
Output Transition Values					
FFE_H to FFF_H	+ Full-Scale Calibration	+10V − 3/2LSB	+5V − 3/2LSB	+10V − 3/2LSB	+20V − 3/2LSB
$7FFF_H$ to 800_H	Midscale Calibration (Bipolar Offset)	0 − 1/2LSB	0 − 1/2LSB	+5V − 1/2LSB	±10V − 1/2LSB
000_H to 001_H	Zero Calibration (− Full-Scale Calibration)	−10V + 1/2LSB	−5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

voltage deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC674A, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. This single common path will typically carry about 3mA of current out of the converter. Code-dependent currents do not flow in analog (pin 9) or digital (pin 15) commons. DC currents that flow are typically 6mA in pin 9 and −3mA in pin 15.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC674A as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC674A will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC674A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustments are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48V (5mV LSB) input range, insert a 200Ω potentiometer in series with pin 13 for the 10.24V range, or a 500Ω potentiometer in series with pin 14 for the 20.48V range. Use a fixed 50Ω, 1% resistor for R_2 (Figures 2 and 3). Offset adjustment is still performed as described below. Full-scale adjustment is performed as described below but with adjustment performed using the input potentiometer instead of R_2.

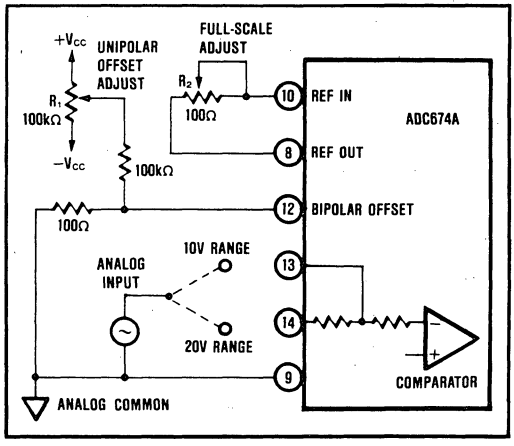


FIGURE 2. Unipolar Configuration.

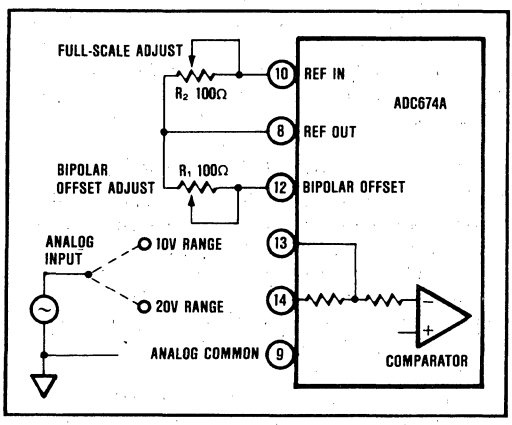


FIGURE 3. Bipolar Configuration.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC674A as shown in Figures 2 and 3 for unipolar and bipolar operation.

CALIBRATION PROCEDURE—UNIPOLAR RANGES

If adjustment of unipolar offset and full scale is not required, replace R_2 with a 50Ω, 1% metal film resistor and connect pin 12 to pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 2. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (high). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1–DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (−4.9988V for the ±5V range, −9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

CONTROLLING THE ADC674A

The Burr-Brown ADC674A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the ouptut data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The

TABLE II. ADC674A Control Line Functions.

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line.

TABLE III. Control Input Truth Table.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50nsec.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/C. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

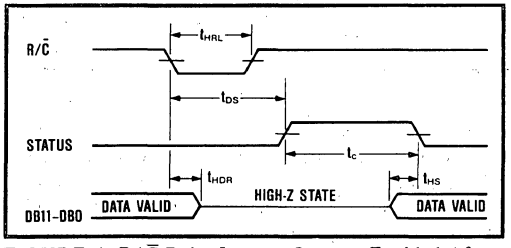


FIGURE 4. R/$\overline{C}$ Pulse Low — Outputs Enabled After Conversion.

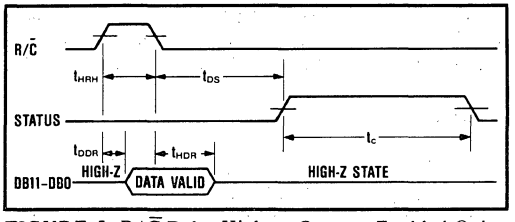


FIGURE 5. R/$\overline{C}$ Pulse High — Outputs Enabled Only While R/$\overline{C}$ Is High.

TABLE IV. Stand-Alone Mode Timing.

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			nsec
t_{DS}	STS Delay from R/$\overline{C}$			200	nsec
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			nsec
t_{HS}	STS Delay After Data Valid	100	300	600	nsec
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			nsec
t_{DDR}	Data Access Time			150	nsec

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0-DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate conversion by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50nsec prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

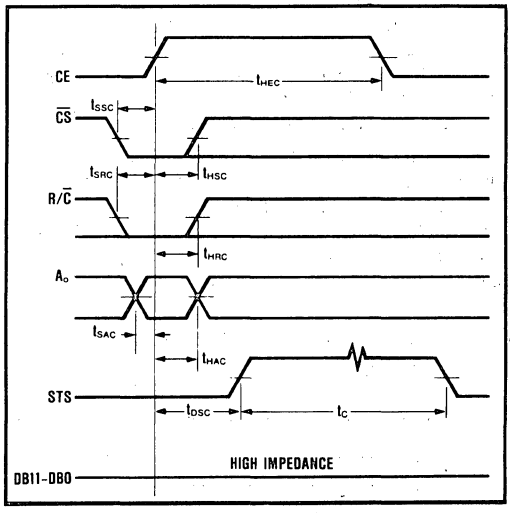


FIGURE 6. Conversion Cycle Timing.

TABLE V. Timing Specifications.

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS delay from CE		100	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE setup	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0	0		ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time, 12 bit cycle	9	12	15	μs
	8 bit cycle	6	8	10	μs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE setup	0	0		ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0	0		ns
t_{HRR}	R/$\overline{C}$ high after CE low	0	0		ns
t_{HAR}	A_0 valid after CE low	50	25		ns
t_{HS}	STS delay after data valid	100	300	600	ns

NOTE: Specifications are at +25°C and measured at 50% level of transitions.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 7 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When 12/$\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest

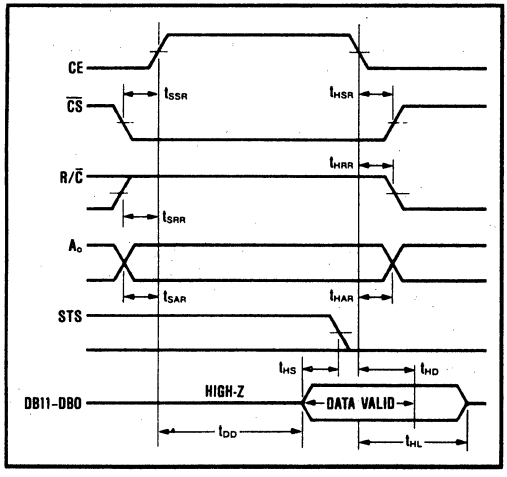


FIGURE 7. Read Cycle Timing.

accomplished by the state of A_0 during the read cycle. Connection of the ADC674A to an 8-bit bus for transfer of left-justified data is illustrated in Figure 9. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is low, the byte addressed contains the 8MSBs. When A_0 is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC674A guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as 950nsec (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Figure 7 for these timing relationships.

ORDERING INFORMATION

Model	Temperature Range	Linearity Error, max (T_{MIN} to T_{MAX})	Resolution, No Missing Codes (T_{MIN} to T_{MAX})	Full-Scale TC, max (ppm/°C)
ADC674AJH	0°C to +75°C	±1LSB	11 Bits	±45
ADC674AKH	0°C to +75°C	±1/2LSB	12 Bits	±25
ADC674ASH	−55°C to +125°C	±1LSB	11 Bits	±50
ADC674ATH	−55°C to +125°C	±1LSB	12 Bits	±25

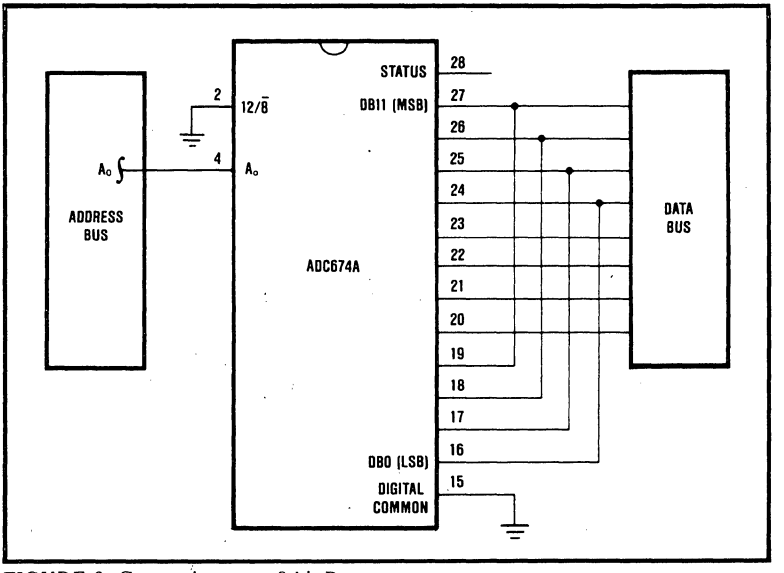


FIGURE 9. Connection to an 8-bit Bus.

BURR-BROWN®

ADC803

High-Speed ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 12-BIT RESOLUTION
- ±0.015% LINEARITY ERROR MAXIMUM (C GRADE)
- NO MISSING CODES –25°C TO +85°C
- 32-PIN METAL PACKAGE
- CONVERSION TIME: 500nsec, 8 bits
  670nsec, 10 bits
  1.5μsec, 12 bits

DESCRIPTION

The ADC803 is a high speed successive approximation analog-to-digital converter utilizing state-of-the-art IC and laser-trimmed thin film components.

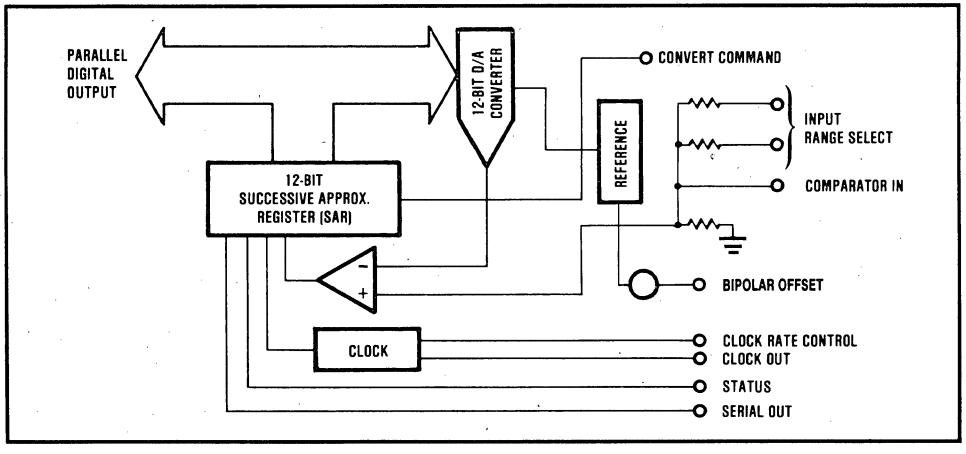
It is complete with internal reference, clock, and comparator and is packaged in a 32-pin metal package. Conversion time is set at the factory to 1.5μsec.

With user-adjusted conversion time set at 1μsec, ±1LSB accuracy can be achieved. The gain and offset errors may be externally-trimmed to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of 0V to -10V, ±5V, and ±10V.

Output data is available in a serial or parallel format. Output codes available are complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are ±15V and +5V.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies, 1.5μsec conversion time, and after 6-minute warm-up unless otherwise noted.

MODEL	ADC803CM			ADC803BM			ADC803SM			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			12			12	Bits
INPUTS										
ANALOG										
Voltage Ranges: Bipolar		±5, ±10			•			•		V
Unipolar		0 to −10			•			•		V
Impedance: −10V to 0V, ±5V		1.4			•			•		kΩ
±10V		2.4			•			•		kΩ
DIGITAL										
Convert Command		Negative pulse 50nsec wide (min) trailing edge (0 to 1) initiates conversion.								
Logic Loading			4			•			•	TTL Loads
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error[1]		±0.04	±0.1		±0.08	±0.2		+0.04	+0.1	%
Offset Error[1]: Unipolar		±0.05	±0.2		±0.07	±0.3		•	•	% of FSR[2]
Bipolar		±0.02	±0.1		•	±0.2		•	•	% of FSR
Linearity Error:										
1.5μsec Conversion Time		±0.009	±0.015			±0.020		±0.012	±0.015	% of FSR
1.0μsec Conversion Time		±0.015	±0.020		±0.020					% of FSR
Differential Linearity Error:										
1.5μsec Conversion Time		±0.012	±0.015			±0.020		•	•	% of FSR
1.0μsec Conversion Time			±0.024		±0.024			•		% of FSR
Inherent Quantization Error		1/2			•			•		LSB
POWER SUPPLY SENSITIVITY										
Gain and Offset: +15VDC		±0.0036			•			•		% of FSR/%V_{CC}
−15VDC		±0.0005			•			•		% of FSR/%V_{CC}
+5VDC		±0.001			•			•		% of FSR/%V_{DD}
Conversion Time: +15VDC		±0.7			•			•		%/%V_{CC}
−15VDC		None			•			•		%/%V_{CC}
+5VDC		±0.8			•			•		%/%V_{DD}
CONVERSION TIME										
Factory Set	1.3		1.5	•		•	•		•	μsec
Range of Adjustments	0.8		2.2	•		•	•		•	μsec
DRIFT										
Gain		±10	±30		±15	•		•	•	ppm of FSR/°C
Offset: Unipolar		±2	±7		±3	•		•	•	ppm of FSR/°C
Bipolar		±3	±10		±5	•		•	•	ppm of FSR/°C
Linearity Error										
−25°C to +85°C:										
1.5μsec Conversion Time		±0.012	±0.018			±0.024			•	% of FSR
1.0μsec Conversion Time		±0.015			±0.020				•	% of FSR
−55°C to +125°C:										
1.7μsec Conversion Time, max.[4]								±.015	±.024	% of FSR
Differential Linearity Error										
−25°C to +85°C:										
1.5μsec Conversion Time		±0.012	±0.018			±0.024				% of FSR
1.0μsec Conversion Time		±0.015			±0.024					% of FSR
−55°C to +125°C:										
1.7μsec Conversion Time, max[4]								±.015	±.024	% of FSR
Conversion Time		±0.1			•			•		% of FSR
No Missing Code Temp. Range:										
1.5μsec Conversion Time	−25		+85	•		•				°C
1.7μsec Conversion Time, max[4]							−55		+125	°C

ELECTRICAL (CONT)

MODEL	ADC803CM			ADC803BM			ADC803SM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT										
DIGITAL DATA										
Parallel										
Output Codes: Unipolar		Complementary Straight Binary			•			•		
Bipolar		Bipolar Offset Binary			•			•		
Output Drive		6		•			•			TTL Loads
Serial Data Codes (NRZ)		Same as Parallel (MSB first)			•			•		
Output Drive		6		•			•			TTL Loads
Status		Logic "1" during Conversion			•			•		
Status Output Drive		6		•			•			TTL Loads
Internal Clock:										
Clock Output Drive		3		•			•			TTL Loads
Frequency (without external clock adjustment)		8			•			•		MHz
POWER SUPPLY REQUIREMENTS										
Power Consumption										
Rated Voltage: Analog ($\pm V_{CC}$)	±14.25	±15.0	±15.75	•	•	•	•	•	•	VDC
Digital (V_{DD})	+4.75	+5.0	+5.25	•	•	•	•	•	•	VDC
Supply Drain: +15V		+27	+32		•	•		•	•	mA
−15V		−38	−55		•	•		•	•	mA
+5V		+180	+210		•	•		•	•	mA
TEMPERATURE RANGE (AMBIENT)										
Specification	−25		+85	•		•	•		•	°C
Storage	−55		+125	•		•	•		•	°C

*Same specification as for ADC803CM.

NOTES: (1) Adjustable to zero. See Optional Gain and Offset Adjustment section. (2) FSR means Full Scale Range. For example, unit connected for ±10V has 20V FSR. (3) See Optional Clock Rate Control section. For faster conversion time at less resolution, see section on External Short Cycle. (4) Conversion time is factory-set at approximately 1.4μsec at +25°C. As temperature increases, the conversion time increases. At +125°C the conversion time will be no more than 1.7μsec. No Missing Codes is guaranteed over −55°C to +125°C provided the conversion time is allowed to increase with temperature.

ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage To Analog Common...±18V

Digital Supply Voltage To Digital Common....+7V

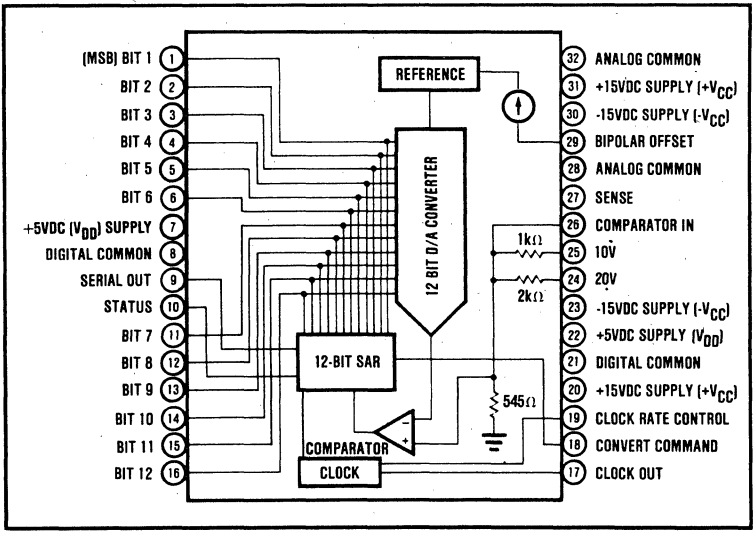
Digital Controls Inputs .....+5.5V

Analog Inputs .....±15V

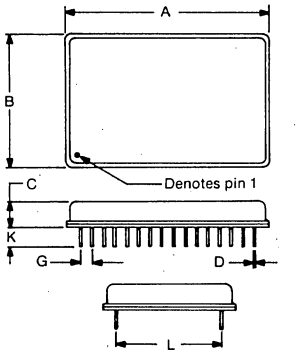
Operating Temperature
- Ambient.....+85°C
- Case.....+125°C

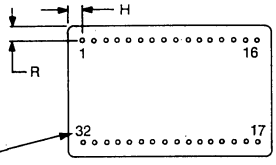
Storage Temperature....+125°C

CONNECTION DIAGRAM



MECHANICAL





Pin numbers shown for reference only. Numbers may not be marked on package.

Pin 1 can be identified from bottom of unit by either a contrasting color of glass seal or a square corner. Case is tied to Digital Common.
NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane. Pin 8 connected to case.

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
CASE: Kovar, Nickel plated
HERMETICITY: Gross Leak Test
MATING CONNECTOR: 2302MC Set of two 16-pin strips
WEIGHT: 13 grams (0.46 oz.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

THEORY OF OPERATION

The accuracy of a successive approximation analog-to-digital converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry matching and tracking properties of the ladder and scaling networks, power supply rejection, reference errors and the dynamic errors of the DAC and comparator. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the transfer function (Figure 1) about the zero point and Offset drift shifts the transfer function left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB. The ADC803 is guaranteed to have no missing codes over the specified temperature range.

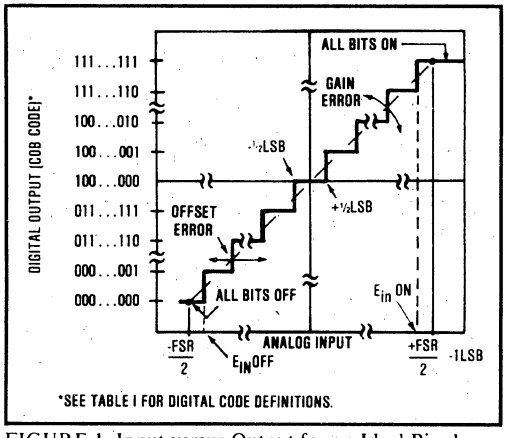


FIGURE 1. Input versus Output for an Ideal Bipolar A/D Converter.

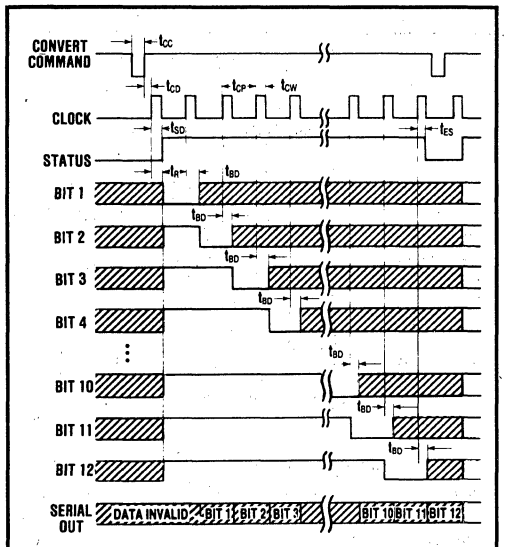
TIMING CONSIDERATIONS

The timing diagram (Figure 2) shows the relationship between the convert command, clock and outputs. The digital output word is positive true logic for bipolar operation and complementary logic for unipolar operation.

The following are some important notes on the ADC803 timing. The times given are typical unless otherwise noted. Nominal maximum and minimum times are also given in Figure 2.

1. When power is first applied, the status of the ADC803 will be undetermined. A CONVERT COMMAND must be applied to initialize the ADC803.
2. The CONVERT COMMAND must be low at least 50nsec prior to the "0" to "1" edge that starts a conversion.
3. The clock runs continuously when the initial CONVERT COMMAND goes high and whenever the CONVERT COMMAND is high thereafter. It does not run when CONVERT COMMAND is low. It may be beneficial to keep CONVERT COMMAND low except during conversions to limit the digital noise induced in the ground and power supply lines.
4. The clock starts 25nsec after the "0" to "1" transition of the CONVERT COMMAND.
5. **Parallel Output Data:** The Successive Approximation Register (SAR) is reset 26nsec after the leading edge of the first clock period in the conversion cycle. The MSB is set to logic "0" and all other bits are set to logic "1". The bits are determined in succession starting with the MSB, Bit 1, as shown in Figure 2. Each bit will be valid 26nsec after its corresponding clock pulse.

   The falling edge of the STATUS signal should not be used to strobe parallel data out of the ADC803



Time Period	Min* (nsec)	Max* (nsec)
t_{CC}	50	—
t_{CD}	15	40
t_{CP}**	100	125
t_{CW}	17	25
t_{SD}	10	38
t_R	10	38
t_{BD}	10	38
t_{ES}	10	38

*Nominal
**Without external adjustment

FIGURE 2. ADC803 Timing Diagram.

directly. The table in Figure 2 indicates that the falling edge of STATUS may occur prior to bit 12 data becoming valid.

6. **Serial Output Data:** The serial output is indeterminate until Bit 1 is valid, which occurs 26nsec after the leading edge of the second clock pulse. The remaining bits (Bits 2 through 12) are valid in succession for one clock period each beginning 26nsec after the leading edge of each clock pulse.
7. STATUS goes high 26nsec after the leading edge of the first clock pulse and goes low 18nsec after the leading edge of the last clock pulse.
8. Bit 12 will become valid at about the same time STATUS goes low and a new conversion can be initiated at anytime after the output data has been read.
9. The converter may be restarted during a conversion. When CONVERT COMMAND makes a "0" to "1" transition after the minimum set-up time, the SAR will be reset and a new conversion will start regardless of the state of the converter prior to the CONVERT COMMAND being received.

Figures 3, 4, and 5 are photographs of the actual pulse shapes and relationships.

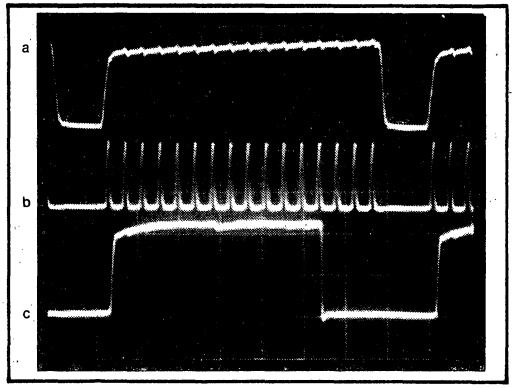


FIGURE 3. Photo of (a) Convert Command, (b) Clock, and (c) Status (200nsec/div).

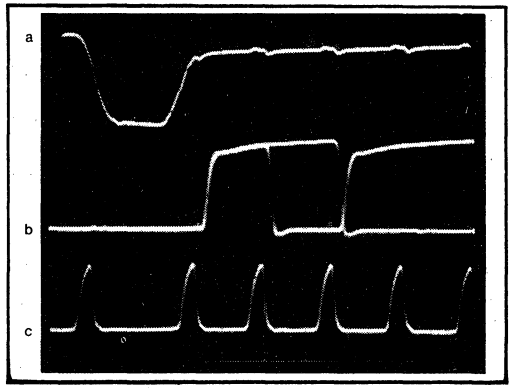


FIGURE 4. Photo of (a) Convert Command, (b) Serial Out, and (c) Clock (50nsec/div).

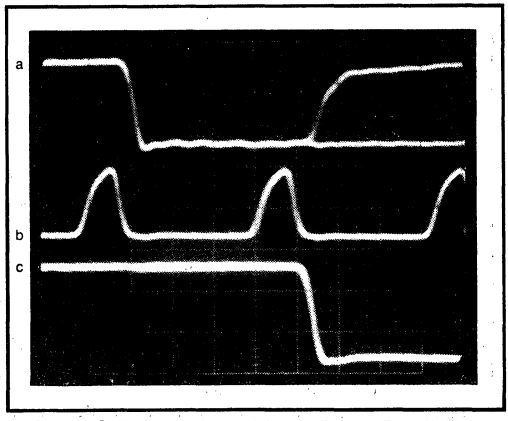


FIGURE 5. Photo of (a) Bit-12 Data (Parallel), (b) Clock, and (c) Status (20nsec/div).

DIGITAL CODES
Parallel Data

Two binary codes are available on the ADC803 parallel output; they are complementary straight binary (Logic "0" true) for unipolar input signal ranges and bipolar offset binary (Logic "1" true) for bipolar input signal ranges. Binary two's complement may be obtained for bipolar input ranges by inverting the MSB. It should be noted that for unipolar input ranges -10 volts is full scale.

Table I shows the LSB, transition values, and code definitions for each possible analog signal range.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Analog Input Voltage Range	±10V	±5V	0 to -10V
Code Designation	BOB(1) or BTC(2)	BOB or BTC	CSB(3)
One Least Significant Bit (LSB)	4.88mV	2.44mV	2.44mV
Transition Values MSB LSB(4)			
000...000 ↔ 000...001	-10V + 1/2LSB	-5V + 1/2LSB	-10V + 3/2LSB
011...111 ↔ 100...000	-1/2LSB	-1/2LSB	-5V + 1/2LSB
111...110 ↔ 111...111	+10V - 3/2LSB	+5V - 3/2LSB	−1/2LSB

NOTES: 1. BOB = Bipolar Offset Binary.
2. BTC = Binary Two's Complement (obtained by inverting the most significant bit (pin 1)).
3. CSB = Complementary Straight Binary.
4. Voltages given are the nominal value for the transition from the next lower code.

Serial Data (NRZ)

Two binary codes are available on the serial output line; they are complementary straight binary (CSB) for unipolar input ranges and bipolar offset binary (BOB) for bipolar input signal ranges. The serial data is available only during conversion and appears with the MSB first. See the timing diagram and discussion under "timing considerations" for more detailed information.

The LSB and transition values shown in Table I. also apply to the serial data output, except serial output does not have a BTC code.

DISCUSSION OF SPECIFICATIONS

The ADC803 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are Linearity, Drift, Gain and Offset errors, and Conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.05% of FSR at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10, 11, and 12.

ACCURACY VERSUS CONVERSION TIME

In successive approximation A/D converters, the conversion time affects Linearity and Differential Linearity errors. Conversion time and its effect on Linearity and Differential Linearity errors for the ADC803 are shown in Figure 6.

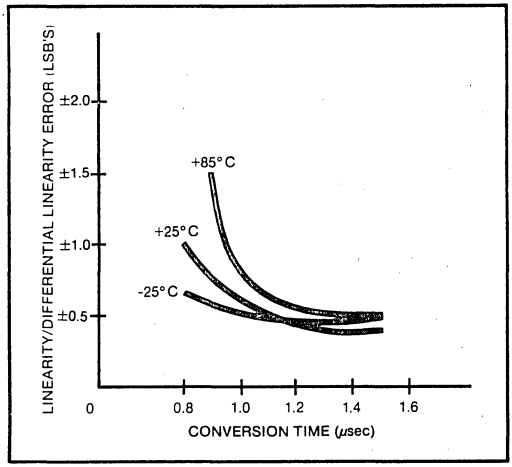


FIGURE 6. Linearity and Differential Linearity Error versus Conversion Time.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 7.

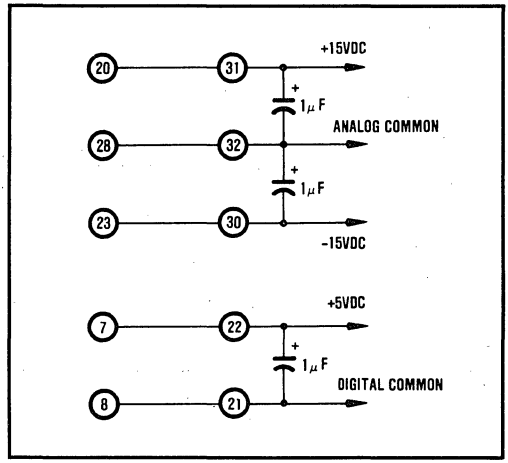


FIGURE 7. Recommended Power Supply Decoupling.

LINEARITY ERROR

Linearity error is not adjustable by the user and is the most meaningful indicator of A/D converter accuracy. Linearity is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity describes the step size between transition values. A Differential Linearity error of ±1/2LSB indicates that the size of any step may not vary from 1LSB by more than ±1/2LSB.

ENVIRONMENTAL SCREENING

Q screening is now available for all models of the ADC803 family. The Q-screened versions have the same specifications as the unscreened versions listed in the Specifications table.

Q Screening

Burr-Brown Q-screened models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those listed below. Burr-Brown's detailed procedures may vary slightly from those of MIL-STD-883.

SCREENING FOR ADC803BMQ, ADC803CMQ AND ADC803SMQ

Screen	Method Burr-Brown or MIL-STD-883	Condition
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008	B (150°C, 24hr)
Temperature Cycling	1010	B (10cy, −55°C to +125°C)
Constant Acceleration	2001	(2000G, Y1 axis)
Burn-in ADC803BMQ, CMQ ADC803SMQ	1015	D (160 hrs, +85°C) (160 hrs, +125°C)
Electrical Test	Burr-Brown Test Specification	
Hermeticity Fine Leak	1014	A1 or A2 (Helium, 5×10^{-7}cc/sec)
Gross Leak	1014	C
Final Electrical	Burr-Brown Test Specification	
External Visual	Burr-Brown QC5150	

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

The ADC803 is a high speed analog-to-digital converter which requires more layout precautions than general purpose products.

The ADC803 has two pins for analog common, two pins for digital common, and two pins for each power supply input. Each pair of these pins must be connected together externally. The connection between the digital supply pins and the connection between the digital common pins must be as short as possible. The analog and digital commons are not connected together internally in the ADC803, but should be connected together externally to a ground plane.

Connecting all commons to a ground plane at the ADC803 is the best method to minimize noise and dissipate heat. Pin 8 (Digital Common) is internally connected to the case.

The ADC803 also has an analog common Sense input (pin 27) for the analog input. This sense pin must be connected to analog common as close to the input signal source as possible or connected to the ground plane. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. Special attention should be taken to ensure that the clock noise on the +5V supply line does not couple into the analog inputs.

The Comparator input (pin 26) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by analog common or ±15VDC supply patterns. The Clock Output (pin 17) is sensitive to stray capacitance; capacitance on this pin could alter the clock wave shape.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF tantalum capacitors as shown in Figure 8 to obtain noise-free operation. These capacitors should be located close to the ADC.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signals as shown in Table II. See Figure 8 for circuit details.

OUTPUT DRIVE

All ADC803 outputs except the clock will drive six TTL loads; the clock will drive three TTL loads. If long digital lines must be driven, external logic buffers are required particularly for the clock which is sensitive to capacitive loading.

TABLE II. ADC803 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 29 To	With Gain Adjust	Connect Pin 24 To	Connect Pin 25 To
±10V	BOB or BTC*	26	Yes	40Ω resistor in series with input signal	Gain Adjust Potentiometer
			No	Input Signal	Analog Common
±5V	BOB or BTC*	26	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal
			No	Analog Common	Input Signal
0 to−10V	CSB	Analog Common	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal
			No	Analog Common	Input Signal

*Obtained by inverting MSB (pin 1) externally.

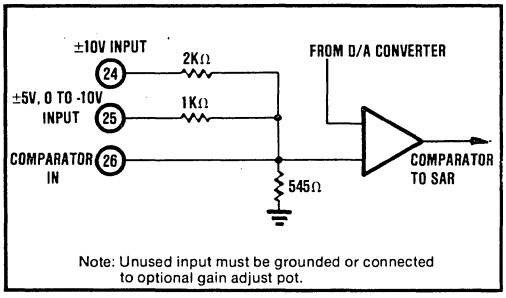


FIGURE 8. Input Scaling Circuit.

INPUT IMPEDANCE

The source impedance to the ADC803 should be low, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the ADC803.

If this impedance is not low, a buffer amplifier should be added between the input signal and the ADC803 input as shown in Figure 9.

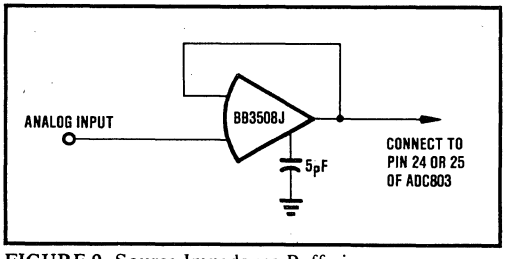


FIGURE 9. Source Impedance Buffering.

A common problem with successive approximation A/D converters is the transients in input current caused by the comparator input being switched back and forth. This requires a fast settling amplifier to drive the input.

The ADC803 comparator is connected in a differential mode (see Figure 8), greatly reducing the size of the input transients. The user, therefore, may use a low cost wideband monolithic amplifier to drive the ADC803. The small signal settling time of the amplifier should be less than 100nsec.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external trim potentiometers connected to the ADC as shown in Figures 10, 11, and 12. For proper gain adjust range a series resistor must be connected to the analog input pin as specified in Table II and shown in Figures 11 and 12. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. All resistors should be ±1% metal film or better. If the Offset adjust is not used, pin 26 should be left open except for bipolar operation when it is connected to pin 29. If the Gain adjust is not used, the unused input (pin 24 or 25) must be grounded to meet specified gain accuracy.

Adjustment Procedure

Refer to Table I for LSB voltages and transition values.

Unipolar offset - connect the offset potentiometer and resistors as shown in Figure 11, sweep the input through the end point transition voltage, from 111...110 to 111...111. Adjust the Offset potentiometer until the actual end point transition voltage occurs at -1/2LSB.

Bipolar offset - connect the offset potentiometer and resistors as shown in Figure 10. Sweep the input through zero and adjust the offset potentiometer until the transition from 0111 1111 1111 to 1000 0000 0000 occurs at −1/2LSB.

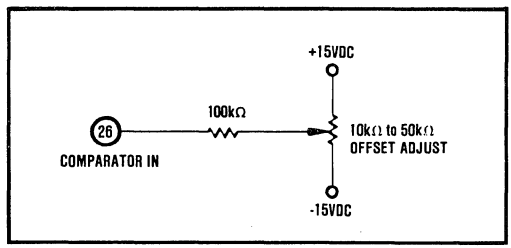


FIGURE 10. Optional Offset Adjust

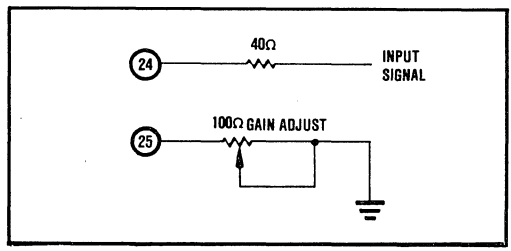


FIGURE 11. Optional Gain Adjust for ±10V Bipolar Operation.

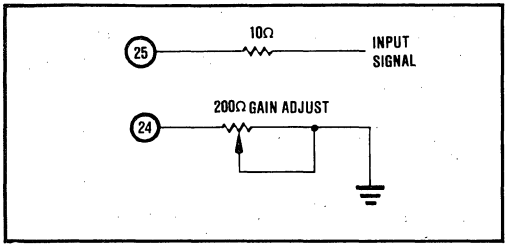


FIGURE 12. Optional Gain Adjust for ±5V Bipolar or 0 to -10V Unipolar Operation.

Gain - connect the Gain potentiometer as shown in Figure 11 or 12. Sweep the input through the end point transition voltage that should cause an output transition from 000...000 to 000...001. Adjust the Gain potentiometer until this transition occurs at the correct end point transition voltage as given in Table I.

OPTIONAL CLOCK RATE CONTROL

The clock is factory-set for a conversion time between 1.3μsec and 1.5μsec. By use of the optional Clock Rate Control as shown in Figure 13, the Conversion time can be adjusted down to 0.8μsec for 12-bit resolution. If the optional Clock Rate Control is not used, pin 19 should be left open. Figure 14 shows Conversion Time versus Clock Rate Control voltage and Figure 6 shows Differential Linearity error versus Conversion time.

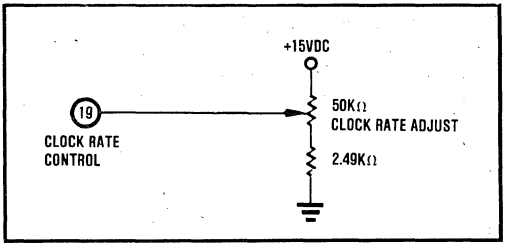


FIGURE 13. Optional Clock Rate Control.

POWER DISSIPATION

The ADC803 dissipates approximately 1.9 watts (typical) and the package has a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above +85°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 15 for θ_{CA} requirements above +85°C. Improved thermal contact with the PC card copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16-square inch (minimum) area, this technique will allow operation to +100°C.

EXTERNAL SHORT CYCLE

If less than 12 bits of resolution is required, the cycle time of the ADC803 can be shortened with the addition of two external components as shown in Figure 16. This circuit will create a shortened status signal directly proportional

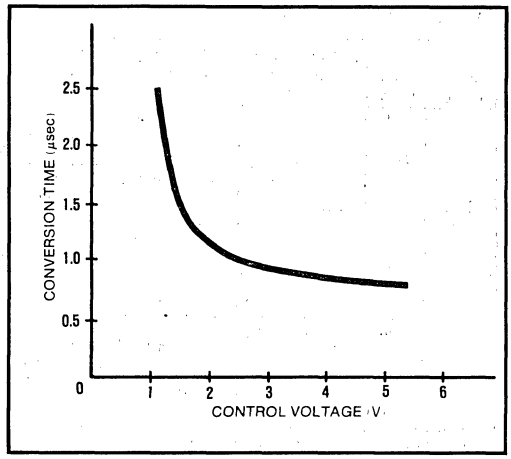


FIGURE 14. Conversion Time versus Clock Rate Control Voltage.

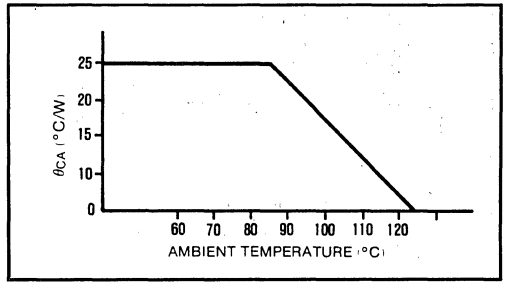


FIGURE 15. θ_{CA} Requirement Above +85°C.

to the reduction of resolution. For n bits of resolution, the n+1 bit is used to create the falling edge of the shortened status signal. It is possible to obtain the equivalent of a 10-bit converter with 670nsec conversion time and an 8-bit converter with 500nsec conversion time using this short cycle technique and the external clock rate control shown in Figure 13. To begin a new conversion, simply give the converter a new convert command pulse. The SAR will reset and a new conversion will begin.

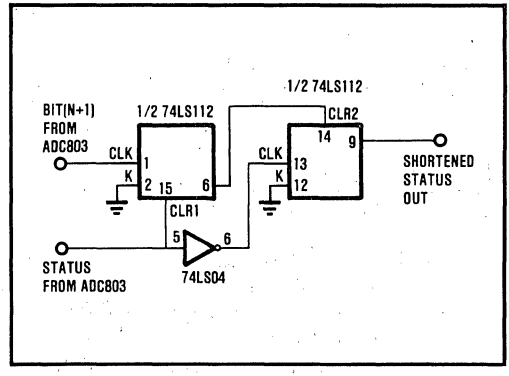


FIGURE 16. External Short Cycle Circuit.

TESTING OF THE ADC803

In order to validate the test results of the ADC803 obtained during final test, the customer must take extreme care in the design and layout of his test fixtures. Proper grounding, correct routing of analog and digital signals and power supply bypassing are crucial in achieving successful results.

ANALOG GROUND, DIGITAL GROUND, SENSE

Figure 17 shows a simplified model of the ADC depicting proper analog and digital grounding. Several analog and digital ground pins have been provided to allow for optimizing the internal layout of the ADC. As will be explained in more detail later, analog and digital grounds should be connected together only at one point by an extremely low resistive and inductive connection (a ground plane is ideal). A special analog ground called "sense" has been provided to eliminate the voltage drop that would otherwise be in the ground return of the R-2R ladder. Measuring the input signal with respect to the sense terminal makes the measurement independent of the impedance that is developed in the connection between the sense terminal and the analog ground, pin 28.

ANALOG-TO-DIGITAL CONVERTER TEST TECHNIQUE

A very effective way of determining the DC performance of an ADC is by using the "servo loop method." The block diagram of this technique is shown in Figure 18. This measurement system automatically locates the analog voltage that causes the digital output to alternate between the desired code and the adjacent code. The

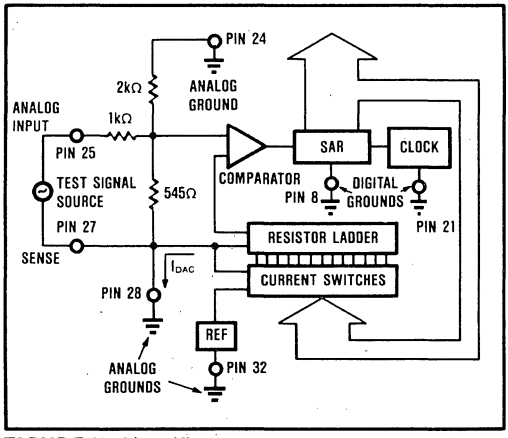


FIGURE 17. Simplified Model of ADC803 Depicting Proper Analog and Digital Ground.

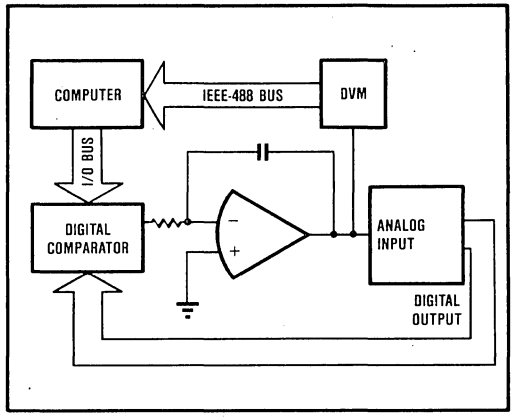


FIGURE 18. Servo Loop Analog-to-Digital Tester.

computer is programmed to place the desired code on the I/O bus which is one set of inputs to the digital comparator. The other set of inputs to this comparator is the digital output of the ADC. Depending upon the result of this comparison, the integrator is directed to change its output until an equilibrium state is achieved. Once in equilibrium, the DVM measures the analog input to the ADC and transmits the information to the computer via the IEEE-488 bus. The test program checks all the desired code combinations, verifying the performance of the ADC. Test time will range from 10 seconds to several minutes depending on the speed of the test program, settling time of the DVM, and number of codes to be checked.

GROUND LOOPS

Figure 19 illustrates the interaction that occurs between the analog and digital grounds when an ADC is connected into a test circuit. This interaction is created by ground loops. The circuit in Figure 19 shows how ground loops are created when the ADC tester combines digital and analog portions of the circuit together—in this case, the test signal generator (analog) and the digital circuitry that detects the ADC code which corresponds to the analog signal (digital). The ground loop exists when the digital ground connection between the ADC and the tester is in parallel with the analog grounds that connect the tester with the ADC. When the connection is made in this manner some of the digital current is diverted into the analog signal return, which creates a code-dependent error signal due to the resistance in the analog signal return. This error distorts the linearity measurement and induces hysterisis. The error can be substantially reduced if the analog and digital grounds are isolated from each other in the ADC tester.

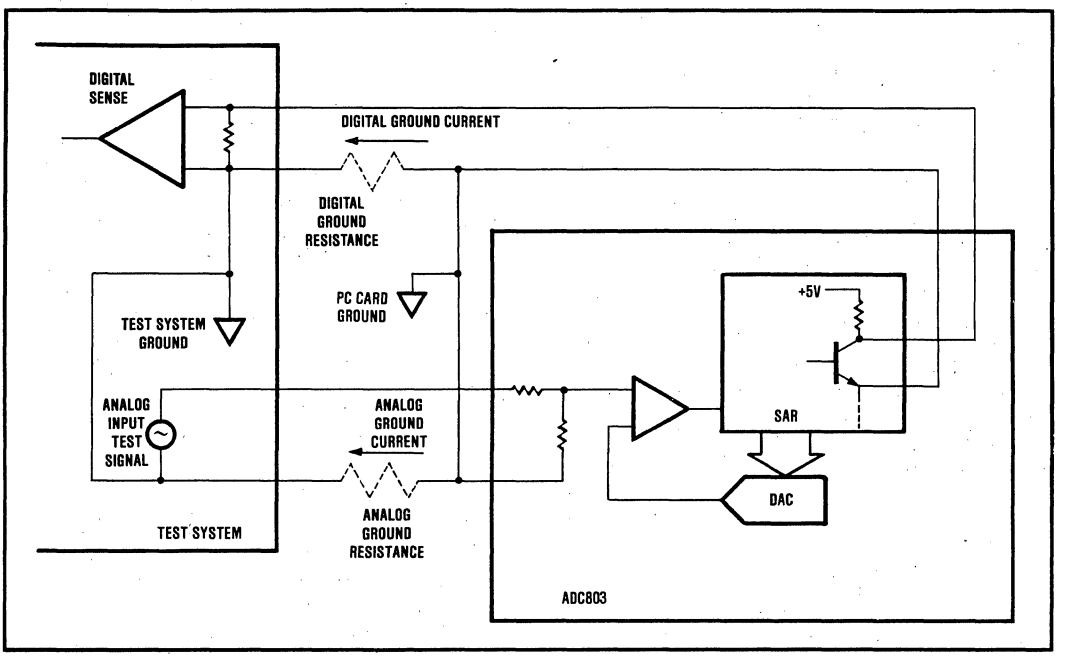


FIGURE 19. Ground Loop Interaction Between Analog and Digital Grounds When ADC Is Connected Into Test Circuit.

BEAT FREQUENCY TEST

A "beat frequency test" applied to an ADC803 with a companion sample/hold illustrates both an effective means of testing the high frequency performance of such a system and demonstrating that the ADC803 with its associated sample/hold is capable of digitizing high frequency signals cleanly. A sample/hold must be used when performing this test to hold the input of the ADC803 constant during the conversion time. Figure 20 is a block diagram of the beat frequency test setup.

The beat frequency test is useful for being able to rapidly determine whether there are any serious problems with the ADC. In this test the input frequency is set at slightly less than one-half the sampling rate. The slight difference is selected to allow the sample point to vary by 1LSB, or less, on successive samples. The data is clocked into a low frequency reconstruction DAC at one-half the sampling rate to enable viewing on an oscilloscope. Figure 21 is a photograph of the response to a full-scale input sine wave centered around the MSB and Figure 22 is a photograph of the response of a small signal sine wave centered around the MSB. For comparison, a photograph (Figure 23) is included which shows the response of the ADC803 to a 125Hz input signal which is the same as the beat frequency.

Figure 24 is the PC card layout that was used for the beat frequency test. This layout demonstrates some of the layout practices that must be followed when using a high speed ADC like the ADC803.

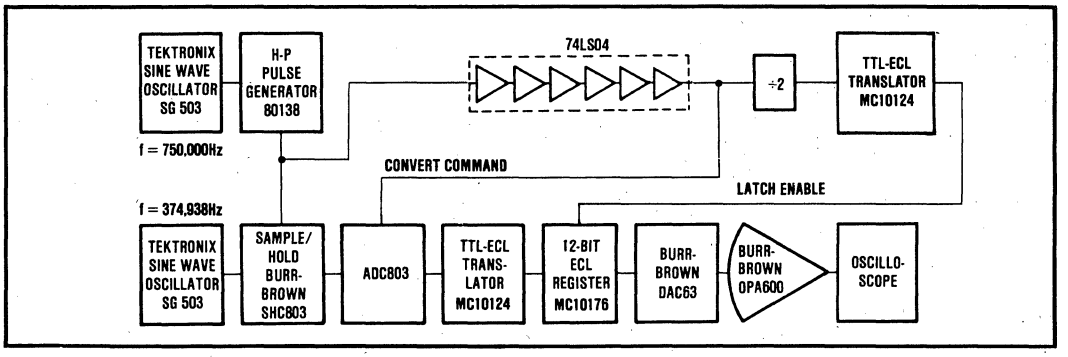


FIGURE 20. Block Diagram of Beat Frequency Test Circuit.

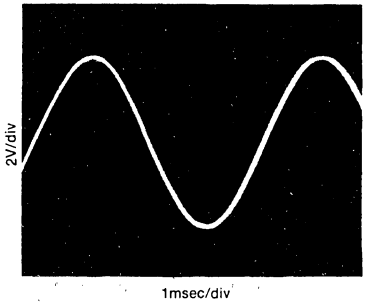


FIGURE 21. Beat Frequency Test Response of Full Scale Sine Wave Input.

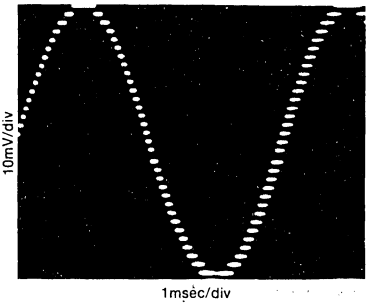


FIGURE 22. Beat Frequency Test Response of Small Signal Sine Wave Input.

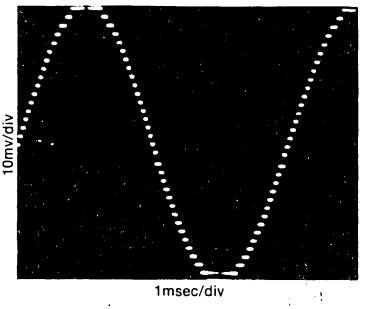
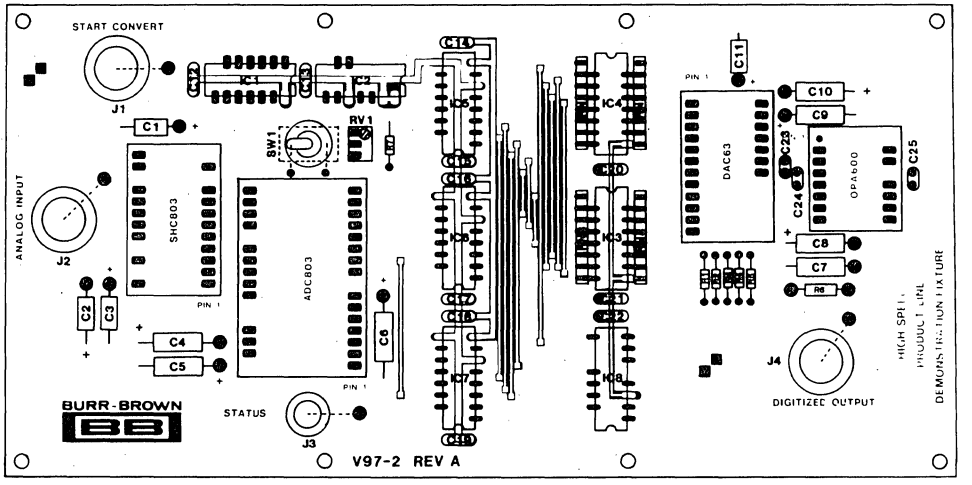
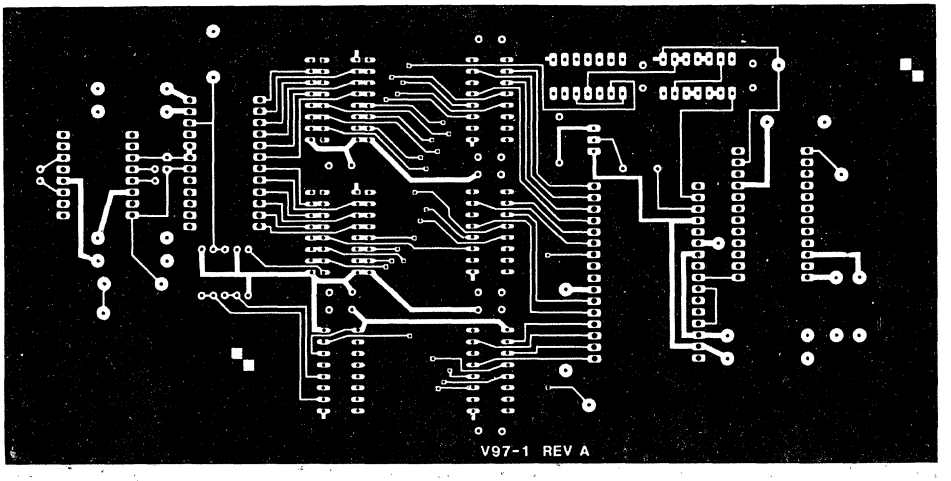


FIGURE 23. Response of Small Signal 125Hz Sine Wave Input.



(a) Top View



(b) Bottom View

FIGURE 24. PC Board Layout for Beat Frequency Test Fixture.

BURR-BROWN®

ADC804

Serial Output
ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 17μsec CONVERSION TIME
- SERIAL OUTPUT—Ideal for applications requiring isolation or long-distance data transmission
- <500mW POWER DISSIPATION
- 24-PIN DUAL-WIDE HERMETIC PACKAGE
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- ±0.012% INTEGRAL LINEARITY
- 12-BIT RESOLUTION
- TWO TEMPERATURE RANGES AVAILABLE:
  ADC804BH for −25°C to +85°C Operation
  ADC804SH for −55°C to +125°C Operation
- NO MISSING CODES −25°C TO +85°C

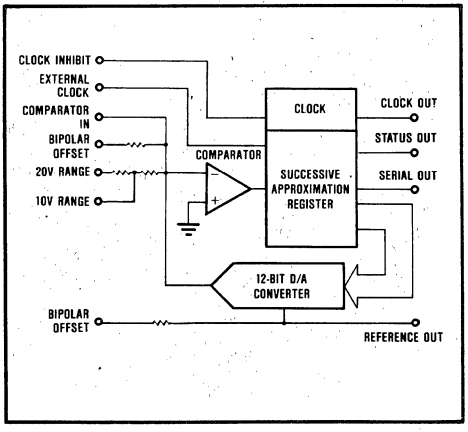
DESCRIPTION

The ADC804 is a 12-bit successive approximation analog-to-digital converter, custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic funtions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than ±0.012% (±1/2LSB). The ADC804 has two grades, one completely specified for −25°C to +85°C operation (ADC804BH), and the other for −55°C to +125°C operation (ADC804SH).

The maximum conversion time of 17μsec makes the ADC804 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 59kHz. In addition, an external clock may be used to synchronize the converter to the system clock or to obtain faster operation. As an added benefit for ADC80 users employing the serial output capability, the ADC804 is designed to replace or provide an alternate source to ADC80 with a minimum of circuit board changes and it provides a 40% reduction in conversion time.

Data is available in serial form with corresponding clock and status signals. Elimination of the parallel output capability enables the ADC804 to be the smallest fully self-contained 12-bit ADC available today. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC804 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic supply. It is packaged in a hermetic 24-pin side-brazed ceramic dual-in-line package.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise specified.

MODEL	ADC804BH			ADC804SH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			*	Bits
INPUT							
ANALOG							
Voltage Ranges: Unipolar		0 to +5, 0 to +10			*		V
Bipolar		±2.5, ±5, ±10			*		V
Impedance: 0 to +5V, ±2.5V		2.3			*		kΩ
0 to +10V, +5V		4.6			*		kΩ
±10V		9.2			*		kΩ
DIGITAL							
Logic Characteristics (over specification temperature range)							
V_{IH} (logic "1")	2.0		5.5	*		*	V
V_{IL} (logic "0")	−0.3		+0.8	*		*	V
I_{IH} (V_{IN} = +2.7V)			−150			*	μA
I_{IL} (V_{IN} = +0.4V)			500			*	μA
Convert Command Pulse Width	100		1200	*		*	nsec
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error[1]		±0.1	±0.3		*	*	% of FSR[2]
Offset Error[1]: Unipolar		±0.05	±0.2		*	*	% of FSR
Bipolar		±0.1	±0.3		*	*	% of FSR
Linearity Error			±0.012			*	% of FSR
Differential Linearity Error			±1			*	LSB
Inherent Quantization Error		1/2			*		LSB
POWER SUPPLY SENSITIVITY							
$+13.5V \leq +V_{CC} \leq +16.5V$ or $+11.4V \leq +V_{CC} \leq +12.6V$		±0.003	±0.009		*	*	% of FSR/%V_{CC}
$-16.5V \leq -V_{CC} \leq -13.5V$ or $-12.6V \leq -V_{CC} \leq -11.4V$		±0.003	±0.009		*	*	% of FSR/%V_{CC}
$+4.5V \leq V_{DD} \leq +5.5V$		±0.002	±0.005		*	*	% of FSR/%V_{DD}
DRIFT							
Total Accuracy, Bipolar[3]		±10	±23		*	*	ppm/°C
Gain		±15	±30		*	*	ppm/°C
Offset: Unipolar		±3			*		ppm of FSR/°C
Bipolar		±7	±15		*	*	ppm of FSR/°C
Linearity Error Drift		±1	±3		*	*	ppm of FSR/°C
Differential Linearity over Temperature Range			+1, −3/4			*	LSB
No Missing Code Temperature Range	−25		+85	−55		+125	°C
Monotonicity Over Temperature Range		Guaranteed			Guaranteed		
CONVERSION TIME[4]		15	17		*	*	μsec
OUTPUTS							
DIGITAL(Clock Out, Status, Serial Out)							
Output Codes, Serial (NRZ)[5]		CSB,COB			*		
Logic Levels: Logic 0 ($I_{sink} \leq 3.2mA$)			+0.4			*	V
Logic 1 ($I_{source} \leq 80\mu A$)	+2.4			*			V
Internal Clock Frequency		92.3			*		kHz
INTERNAL REFERENCE VOLTAGE							
Voltage	+6.2	+6.3	+6.4	*	*	*	V
Source Current Available for External Loads[6]	200			*			μA
Temperature Coefficient		±10	±30		*	*	ppm/°C
POWER SUPPLY REQUIREMENTS							
Voltage, $\pm V_{CC}$	±11.4	±15	±16.5	*	*	*	V
V_{DD}	+4.5	+5.0	+5.5	*	*	*	V
Current, $+I_{CC}$		5	8.5		*	*	mA
$-I_{CC}$		21	26		*	*	mA
I_{DD}		11	15		*	*	mA
Power Dissipation ($\pm V_{CC}$ = 15V)		450	595		*	*	mW
TEMPERATURE RANGE (Ambient)							
Specification	−25		+85	−55		+125	°C
Storage	−65		+150	*		*	°C

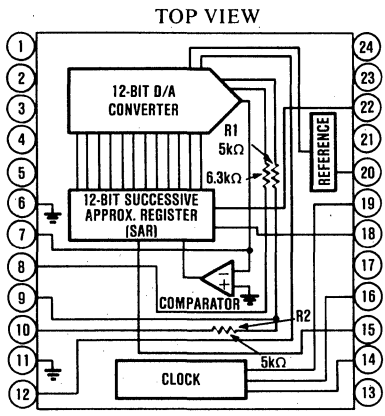
*Same as specification for ADC804BH.

NOTES: (1) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustments" section. (2) FSR means full-scale range and is 20V for ±10V Range, 10V for ±5V and 0 to +10V ranges, etc. (3) Includes drift due to linearity, gain, and offset drifts. (4) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. (5) CSB means Complementary Straight Binary, and COB means Complementary Offset Binary, NRZ means non-return-to-zero coding. See Table I for additional information. (6) External loading must be constant during conversion, and must not exceed 200μA for guaranteed specifications.

CONNECTION DIAGRAM

Pin 1 - N/C
Pin 2 - N/C
Pin 3 - N/C
Pin 4 - N/C
Pin 5 - V_{DD}
Pin 6 - Digital Common
Pin 7 - Comparator In
Pin 8 - Bipolar Offset
Pin 9 - R1 10V Range
Pin 10 - R2 20V Range
Pin 11 - Analog Common
Pin 12 - Gain Adjust

Pin 24 - N/C
Pin 23 - N/C
Pin 22 - Serial Out
Pin 21 - $-V_{CC}$
Pin 20 - Reference Out (+6.3V)
Pin 19 - Clock Out
Pin 18 - Status
Pin 17 - N/C
Pin 16 - Clock Inhibit
Pin 15 - External Clock
Pin 14 - Convert Command
Pin 13 - $+V_{CC}$



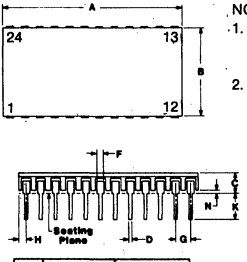
ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common ..... 0 to +16.5V
$-V_{CC}$ to Analog Common ..... 0 to −16.5V
V_{DD} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±0.5V
Logic Inputs (Convert Command, Clock In)
to Digital Common ..... −0.3V to V_{DD} +0.5V
Analog Inputs (Analog In, Bipolar Offset)
to Analog Common ..... ±16.5V
Reference Output ..... Indefinite Short to Common, Momentary Short to V_{CC}
Power Dissipation 1000mW
Lead Temperature, Soldering ..... +300°C, 10sec
Thermal Resistance, θ_{JA} ..... 60°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

MECHANICAL



NOTES:
1. Leads in true position within .010" (.25MM) R at MMC at Seating Plane.
2. Pin numbers shown for reference only. may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.190	1.210	30.23	30.73
B	.550	.600	14.73	15.24
C	.112	.197	2.84	5.08
D	.015	.019	0.38	0.48
F	.040	.060	1.02	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.23	0.30
K	.135	.175	3.43	4.45
L	.590	.610	14.99	15.49
N	.010	.030	0.25	0.76

CASE: Ceramic, hermetic
MATING CONNECTOR: 0245MC
WEIGHT: 4.4gm (0.16oz)

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a significantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers. The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1, which illustrates these relationships. A linearity specification which guarantees

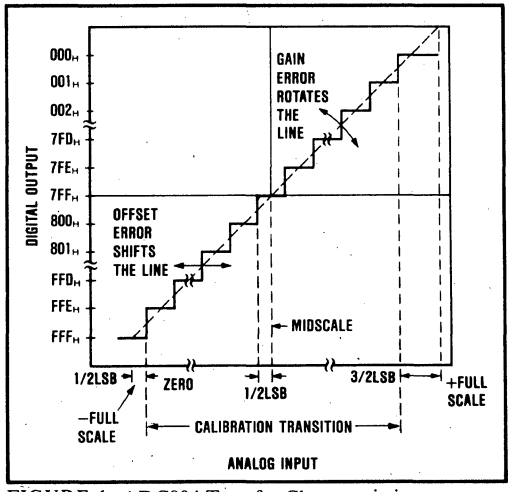


FIGURE 1. ADC804 Transfer Characteristic Terminology.

±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and code definitions for each possible ADC804 analog input signal range are described in Table I.

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC804 input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is a definition of the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. The ADC804BH is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range of −25°C to +85°C, and the ADC804SH displays no missing codes over the temperature range of −55°C to +125°C.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC804 connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC804 follows this convention. Thus, bipolar offset error for the ADC804 is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the specification range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC804 assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of course, results in a proportional change in all code transition values (i.e., a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

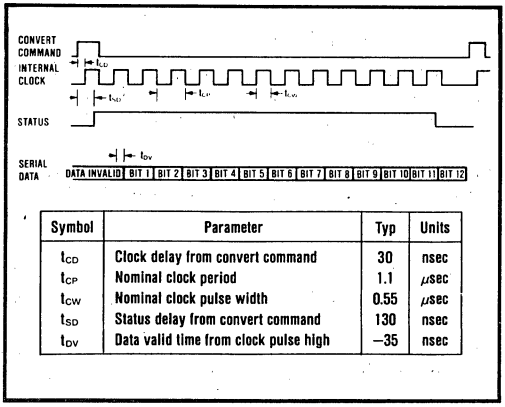
TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	**Input Voltage Range and LSB Values**					
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB*	COB*	COB*	CSB**	CSB**
One Least Significant Bit (LSB)	$FSR/2^n$ n = 12	$20V/2^n$ 4.88mV	$10V/2^n$ 2.44mV	$5V/2^n$ 1.22mV	$10V/2^n$ 2.44mV	$5V/2^n$ 1.22mV
Transition Values MSB LSB 001_H to 000_H 800_H to $7FF_H$ FFF_H to FFE_H	 +Full Scale Mid Scale −Full Scale	 +10V − 3/2LSB 0 −10V + 1/2LSB	 +5V − 3/2LSB 0 −5V + 1/2LSB	 +2.5V − 3/2LSB 0 −2.5V + 1/2LSB	 + 10V − 3/2LSB +5V 0 + 1/2LSB	 +5V − 3/2LSB + 2.5V 0 + 1/2LSB

*COB = Complementary Offset Binary **CSB = Complementary Straight Binary

TIMING CONSIDERATIONS

Timing relationships of the ADC804 are shown in Figure 2. It should be noted that although the convert command pulse width must be between 100nsec and 1.2μsec to obtain the specified conversion time with internal clock, the ADC804 will accept longer convert commands with no loss of accuracy, assuming that the



Symbol	Parameter	Typ	Units
t_{CD}	Clock delay from convert command	30	nsec
t_{CP}	Nominal clock period	1.1	μsec
t_{CW}	Nominal clock pulse width	0.55	μsec
t_{SD}	Status delay from convert command	130	nsec
t_{DV}	Data valid time from clock pulse high	−35	nsec

FIGURE 2. ADC804 Timing Diagram (normal values at +25°C with internal clock).

analog input signal is stable. In this situation, the actual indicated conversion time (during which status is high) for 12-bit operation will be equal to approximately 600nsec less than the sum of the factory-set conversion time and the length of the convert command. The code returned by the converter at the end of the conversion will accurately represent the analog input to the converter at the time the convert command returns to the low state. In addition, although the initial state of the converter will be indeterminate when power is first applied, it is designed to time-out and be ready to accept a convert command within approximately 15μsec after power-up, provided that either an external clock source is present or the internal clock is not inhibited.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse "n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the rising edge of the thirteenth clock pulse. A new conversion may not be initiated until 50nsec after the fall of the thirteenth clock pulse. Additional convert commands applied during conversion will be ignored.

DEFINITION OF DIGITAL CODES

Two binary codes are available on the serial output of the ADC804, complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) for bipolar input ranges. Both are complementary codes, meaning that logic "0" is true. Serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. All clock pulses available from the ADC804 have a nominal pulse width of 550nsec to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC804 but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use a wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC804 as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC804 will be driving into a nominal DC input impedance of 2.5kΩ to 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC804 offers five standard input ranges: 0V to+5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate

input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. Use of external padding resistors to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range) will require matching of the external fixed resistor values to individual devices, due to the large tolerance of the internal input resistors. Alternatively, the gain range of the converter may be easily increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by decreasing the value of the gain adjust series resistor in Figure 6.

TABLE II. ADC804 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 8 To Pin	Connect Pin 10 To	Connect Input Signal To
±10V	COB	7	Input Signal	10
±5V	COB	7	Open	9
±2.5V	COB	7	Pin 7	9
0 to +5V	CSB	11	Pin 7	9
0 to +10V	CSB	11	Open	9

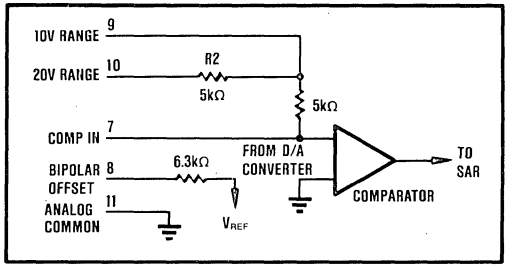


FIGURE 3. ACD804 Input Scaling Circuit.

REPLACEMENT OF ADC80

As illustrated in Figure 4, a circuit board configured for use of the ADC80 serial output capability may be very easily adapted to also use the ADC804, or to achieve space savings due to the smaller package of the ADC804. The pin assignments of the ADC804 have been chosen to allow it to fit neatly into one corner of the ADC80 layout. When replacing ADC80 with ADC804, a board space improvement of approximately 1.25 square inches (8.06cm^2) is obtained.

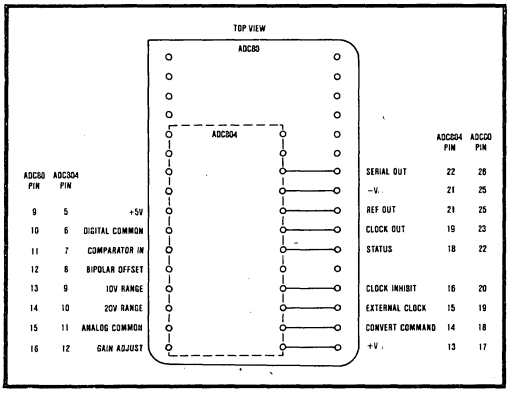


FIGURE 4. Adapting an ADC80 Layout for ADC804.

CALIBRATION

Optional External Gain and Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC804 as shown in Figures 5 and 6 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These potentiometers may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 12 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

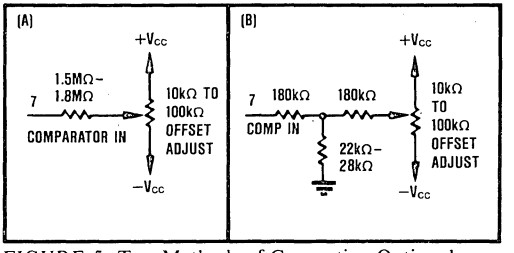


FIGURE 5. Two Methods of Connecting Optional Offset Adjust.

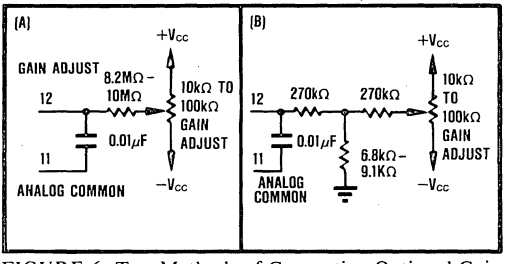


FIGURE 6. Two Methods of Connecting Optional Gain Adjust.

Adjustment Procedure

OFFSET—Connect the offset potentiometer as shown in Figure 5. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V + 2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiomter until an output code is obtained which is alternating between FFE_H and FFF_H with approximately 50% occurrence of each of the two codes. In other words, the potentiomter is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 6. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V − 7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiometer until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transition to a precisely known value.

CLOCK OPTIONS

The ADC804 is extremely versatile in that it can be operated with either internal or external clock. Thus, use of an available system clock enables synchronization of the converter to the rest of the system to optimize performance in a noisy environment.

When operating with the internal clock, pin 15 (external clock input) and pin 16 (clock inhibit) may be left unconnected. No external pull-ups are required due to the inclusion of pull-up resistors in the ADC804. Pin 16 (clock inhibit) must be grounded for use with an external clock, which is applied to pin 15.

See Figures 7 through 10 for diagrams to implement the various clock options.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models

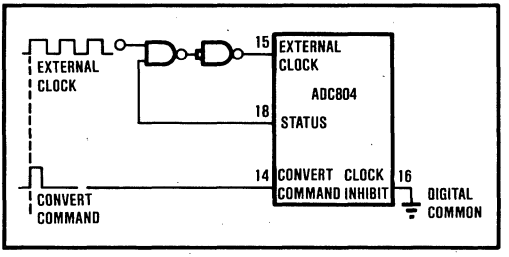


FIGURE 8. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

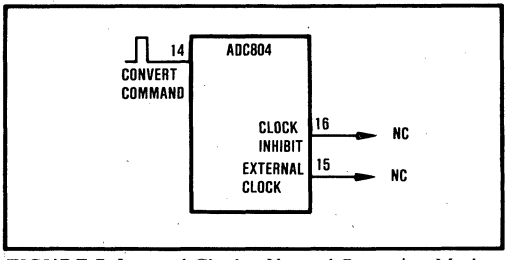


FIGURE 7. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

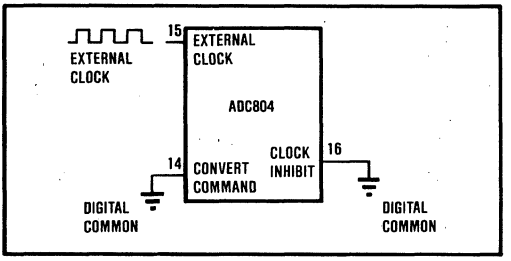


FIGURE 9. Continuous Conversion with external Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

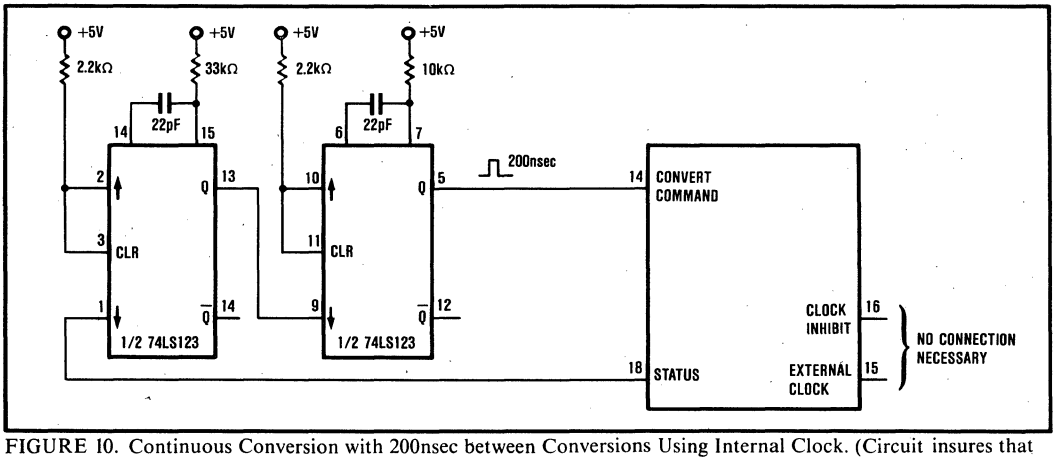


FIGURE 10. Continuous Conversion with 200nsec between Conversions Using Internal Clock. (Circuit insures that the conversion process will start when power is applied.)

are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table III is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

TABLE III. Screening Flow for ADC804xHQ

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Electrical Test	Burr-Brown test procedure	
Burn-in	1015, B	160 hour, +125°C, steady-state
Hermeticity: Fine Leak Gross Leak	1014, A1 or A2 1014, C	5×10^{-7} atm cc/sec bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	Burr-Brown QC4118	

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BURR-BROWN®

PCM75
DESIGNED FOR AUDIO

16-Bit Hybrid
ANALOG-TO-DIGITAL CONVERTER

FEATURES

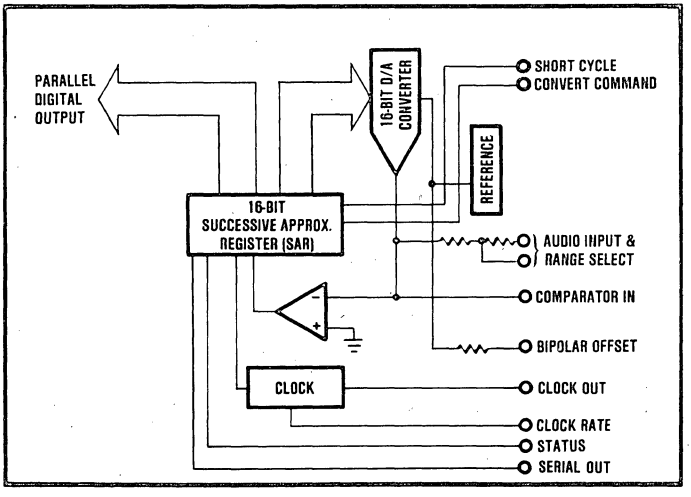
- 16-BIT RESOLUTION
- 90dB DYNAMIC RANGE
- 0.004% THD (FS Input, 16 Bits)
- 0.02% MAX THD (-15dB, 16 Bits)
- 17μs MAX CONVERSION TIME (16 Bits)
- 15μs MAX CONVERSION TIME (14 Bits)
- 10μs CONVERSION TIME (Reduced Specs)
- EIAJ STC-007-COMPATIBLE

DESCRIPTION

The PCM75 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The PCM75 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a bottom-brazed ceramic 32-pin dual-in-line package. The converter is complete with internal reference and clock.

The PCM75 is designed for PCM audio applications and is compatible with EIAJ STC-007 specifications.

The conversion time can be reduced from 15μs to 10μs with some increase in distortion. Distortion is specified on the data sheet to assure performance in critical audio applications.



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SPECIFICATIONS

ELECTRICAL

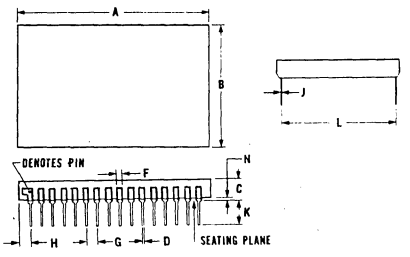
At 25°C and rated power supplies unless otherwise noted.

MODEL	PCM75KG			PCM76JG			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			*	Bits
DYNAMIC RANGE[1]		90			*		dB
INPUT							
ANALOG							
Voltage Ranges, Bipolar		±2.5, ±5, ±10			*		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			*		kΩ
0 to +10V, ±5V		5			*		kΩ
0 to +20V, ±10V		10			*		KΩ
DIGITAL[2]							
Convert Command		Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)					
Logic Loading			1			*	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error		±0.1[3]			*		%
Offset Error, Bipolar		±0.1[3]			*		% of FSR[4]
Differential Linearity Error (major carry)		±0.0015			±0.003		% of FSR
Inherent Quantization Error		±1/2			*		LSB
TOTAL HARMONIC DISTORTION[1]							
V_{IN} = ±FS at f = 400Hz							
14-Bit Resolution		0.006			0.008		%
16-Bit Resolution		0.004			0.006		%
V_{IN} = −15dB at f = 400Hz							
14-Bit Resolution		0.025			0.03	0.05	%
16-Bit Resolution		0.015	0.02		0.021		%
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			*		% of FSR/%V_S
+5VDC		0.001			*		% of FSR/%V_S
CONVERSION TIME[5]							
14 Bits			15			*	μs
16 Bits			17				μs
WARM-UP TIME	5			*			min
DRIFT							
Gain			±20			*	ppm/°C
Offset, Bipolar			±15			*	ppm of FSR/°C
OUTPUT							
DIGITAL (all codes complementary)							
Parallel							
Bipolar Output Codes[6]		COB, CTC[7]			*		
Output Drive	2			*			TTL Loads
Serial Data Code (NRZ)		CSB, COB			*		
Output Drive			2			*	TTL Loads
Status		Logic "1" during conversion			*		
Status Output Drive	2			*			TTL Loads
Internal Clock: Output Drive	2			*			TTL Loads
Frequency[8]		933			*		kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		0.525			*		W
Rated Voltage: Analog	±14.5	±15	±15.5	*	*	*	VDC
Digital	+4.75	+5	+5.25	*	*	*	VDC
Supply Drain: +15VDC		+14			*		mA
−15VDC		−17			*		mA
+5VDC		+10			*		mA
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Operating (derated specs)	−25		+85	*		*	°C
Storage	−55		+100	*		*	°C

*Specification same as PCM75KG.

NOTES: (1) The measurement of total harmonic distortion (THD) and Dynamic Range is highly dependent on the characteristics of the sample/hold amplifier, the digital-to-analog converter, the deglitcher, and the low-pass filter. To accurately measure THD and Dynamic Range, the accuracy of each device should be better than 16-bit accuracy. A block diagram showing the measurement technique Burr-Brown uses is shown in Figure 6. (2) DTL/TTL compatible, i.e., Logic "0" = 0.8V max. Logic "1" = 2.0V min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min. (3) Adjustable to zero. (see "Optional External Gain and Offset Adjustment.") (4) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (5) Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Additional Optional Connections" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified max conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to bit 15 (pin 15) for 14-bit resolution. (6) See Table I. CSB—Complementary Straight Binary, COB—Complementary Offset Binary, CTC—Complementary Two's Complement. (7) CTC coding obtained by inverting MSB (pin 1). (8) Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz. See Figures 14 and 15 and Table III.

MECHANICAL



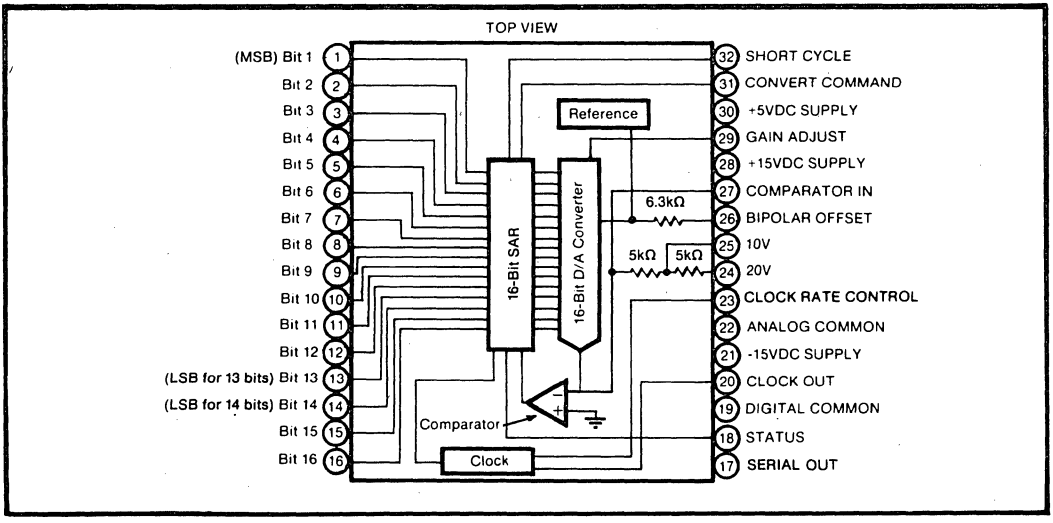
Pin numbers shown for reference only. Numbers may not be marked on package.

CASE: Ceramic
MATING CONNECTOR:
2302MC
WEIGHT: 13 grams (0.46oz.)
HERMETICITY:
Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	.180	.210	4.57	5.33
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	100 BASIC		2.54 BASIC	
H	.089	.106	2.26	2.69
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.900 BASIC		22.86 BASIC	
N	.015	.035	.38	.89

LEADS IN TRUE POSITION WITHIN .010" (.25 MM) R @ MMC AT SEATING PLANE

CONNECTION DIAGRAM



THEORY OF OPERATION

The accuracy of a successive-approximation A/D converter is described by the transfer function shown in Figure 1. All successive-approximation A/D converters have an inherent Quantization Error ±1/2LSB. The remaining errors in the A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off), and Offset drift shifts the line left or right over the operating temperature range. Total Harmonic Distortion (THD) is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error, that is useful in Audio Applications. To be useful, THD should be specified for both high level and low level input

signals. This error is unadjustable and is the most meaningful indicator of A/D converter accuracy for Audio Applications. The resolution of an A/D converter can be expressed in terms of Dynamic Range. The Dynamic Range is a measure of the ratio of the smallest signals the converter can resolve to the full scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 x n, where n is the number of bits of resolution, or 96dB for a 16-bit converter. The actual or useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.

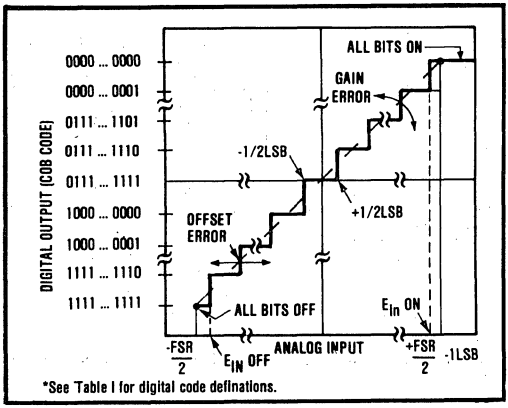


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram in Figure 2 assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 3 and 4 are timing diagrams showing the relationship of serial data to clock and valid data to status.

DEFINITION OF DIGITAL CODES

Parallel Data

Two binary codes are available on the PCM75 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (pin1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 14-, 15- and 16-bit resolutions. Figure 5 shows the connections for 14-bit resolution, parallel data output, with ±5V input.

Serial Data

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

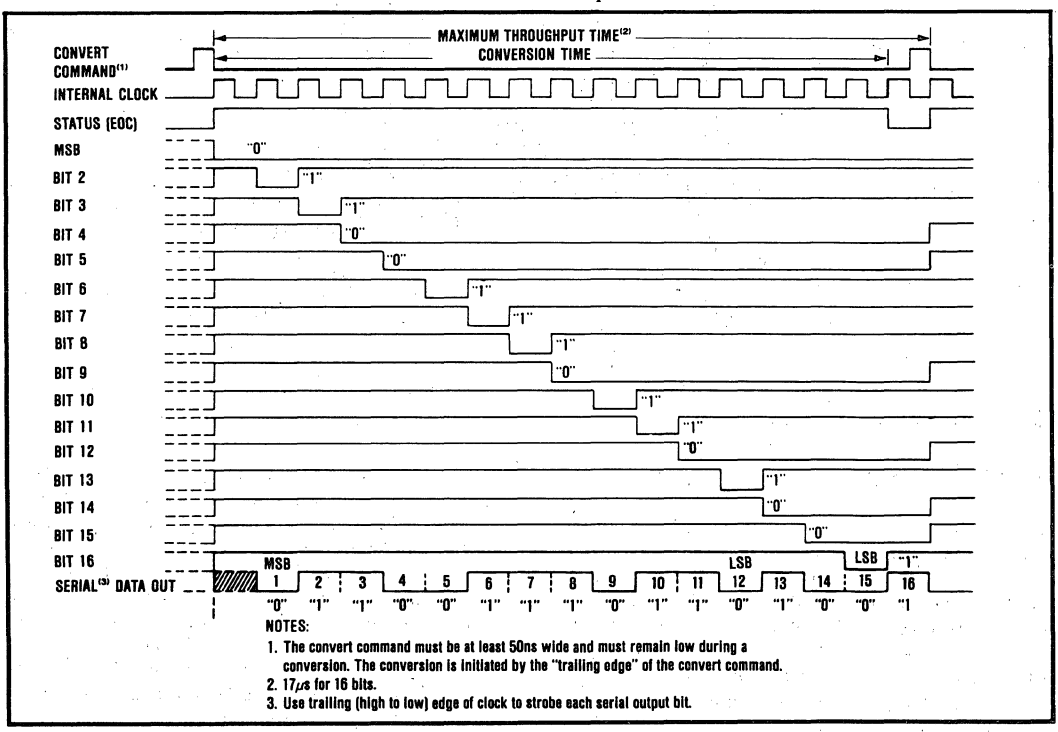


FIGURE 2. Timing Diagram.

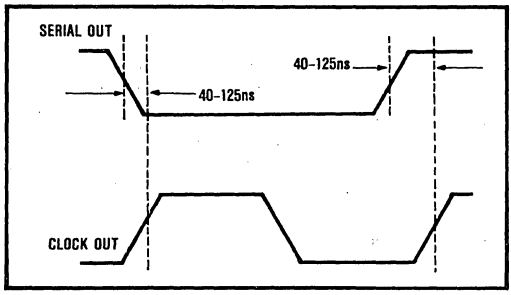


FIGURE 3. Timing Relationship of Serial Data to Clock.

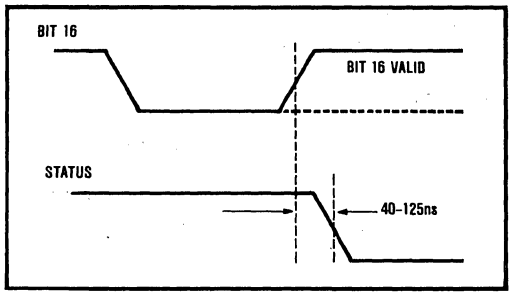


FIGURE 4. Timing Relationship of Valid Data to Status.

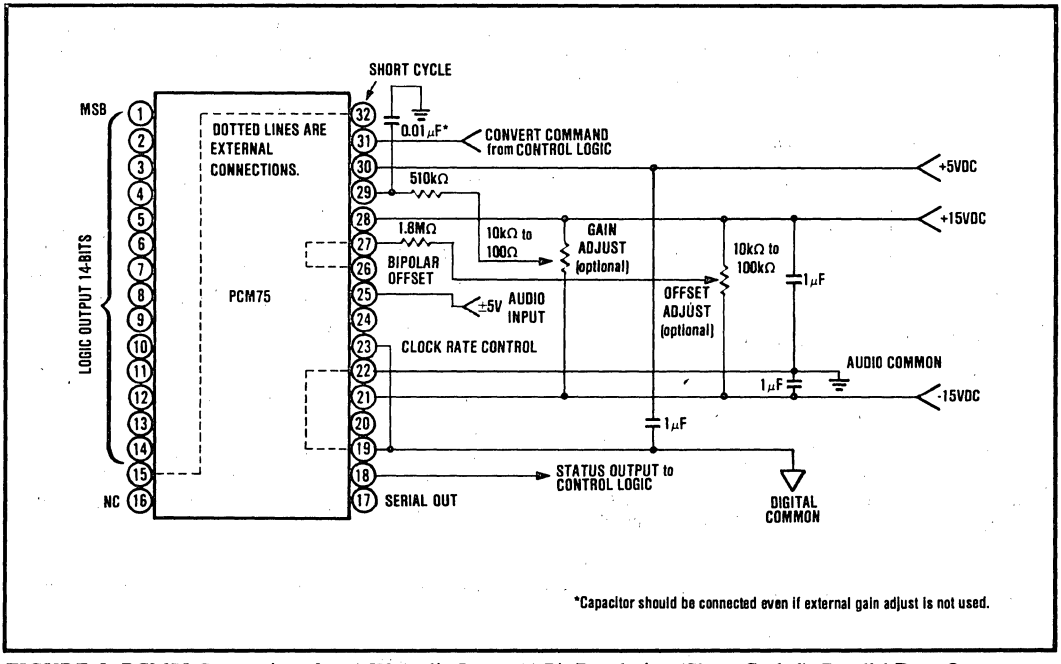


FIGURE 5. PCM75 Connections for: ±5V Audio Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Audio Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 16	305µV	153µV	77µV	153µV	77µV	305µV
	n = 15	610µV	305µV	153µV	305µV	153µV	610µV
	n = 14	1.22mV	610µV	305µV	6.0µV	305µV	1.22mV
Transition Values MSB LSB							
000...000(4)	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

(1) COB = Complementary Offset Binary
(2) CTC = Complementary Two's Complement - obtained by inverting the most significant bit. MSB (pin 1).
(3) CSB = Complementary Straight Binary
(4) Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The PCM75 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter in audio applications are total harmonic distortion, drift, gain and offset errors, and conversion time effects on accuracy. The ADC is factory-trimmed and tested for all critical key specifications.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 12 and 13.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM75 power supply sensitivity is specified for ±0.003% of FSR/%V, for ±15VDC supplies and ±0.0015% of FSR/%V, for +5VDC supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 9.

TOTAL HARMONIC DISTORTION

The Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics to the value of the rms fundamental and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM75 is shown in Figure 6 along with a timing diagram for the control logic. If we assume that the error due to the test circuit is negligible, then the rms value of the PCM75 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} [E_L(i) + E_Q(i)]^2}$$

where N is the number of samples, $E_L(i)$ is the linearity error of the PCM75 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N} [E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\%$$

This expression indicates that there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the A/D is directly correlated to the THD because the digital output words from the A/D vary according to the amplitude and frequency of the sine wave input as well as the sampling frequency.

For the PCM75 the test sampling period was chosen to be 22.7μs, which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 400Hz and the amplitude of the input signal is 0dB (full scale) and −15dB.

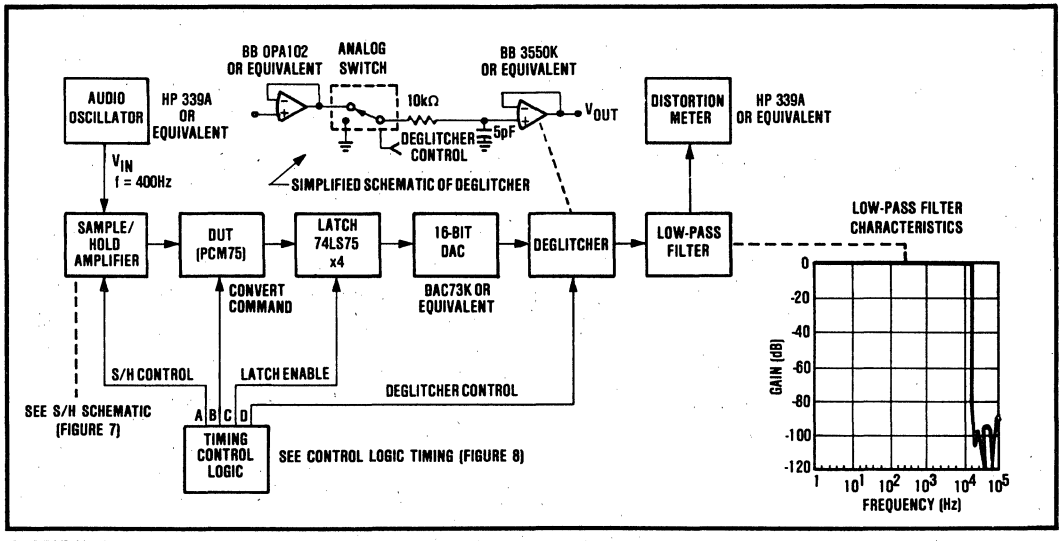


FIGURE 6. Block Diagram of Distortion Test Circuit.

ACCURACY VS CONVERSION TIME

Figures 16 and 17 show the relationship of THD vs input voltage level for the PCM75 with both 14-bit and 16-bit resolution. Notice that the distortion level is reduced by increasing the resolution from 14 to 16 bits due to the reduced quantization error.

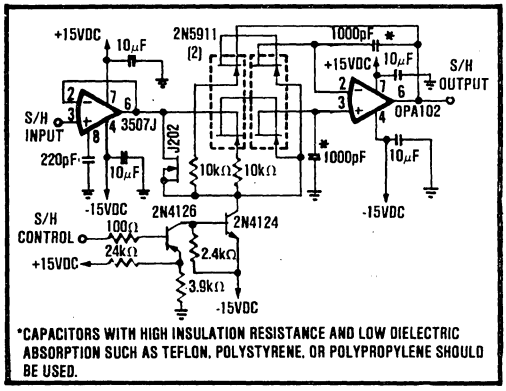


FIGURE 7. Schematic of Sample/Hold Amplifier.

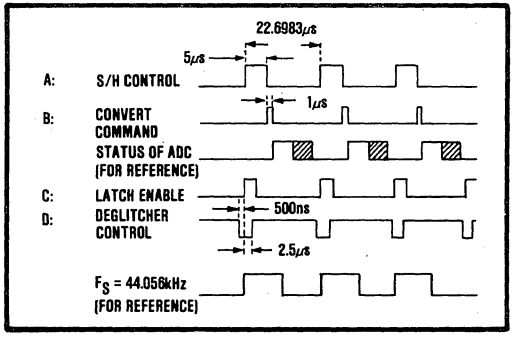


FIGURE 8. Control Logic Timing for PCM75 Distortion Test Circuit.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and Digital Common are not connected internally in the PCM75 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 9 to obtain noise free operation. These capacitors should be located close to the ADC. Bypass the 1μF electrolytic type capacitors with 0.01μF ceramic capacitors for improved high frequency performance.

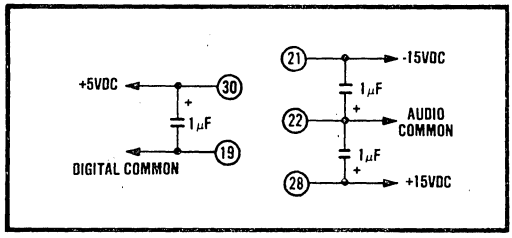


FIGURE 9. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 10 for circuit details.

TABLE II. PCM75 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB (pin 1).

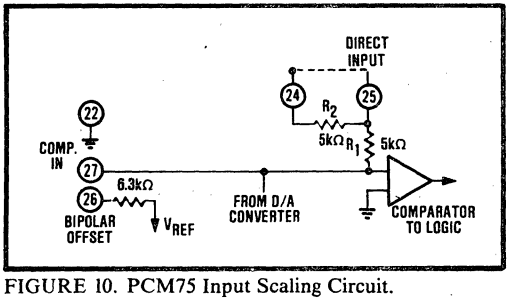


FIGURE 10. PCM75 Input Scaling Circuit.

INPUT IMPEDANCE

The input signal to the PCM75 should come from a low impedance source, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the PCM75.

If this impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the PCM75 as shown in Figure 11.

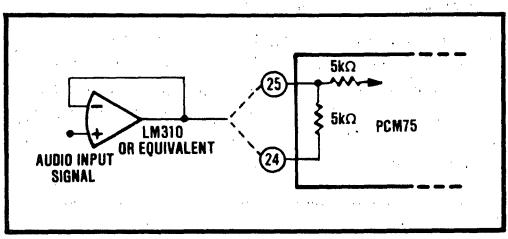


FIGURE 11. Buffer Amplifier for PCM75 Input.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 12 and 13. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and pin 27 (Offset Adjust) may be left open if no external adjustment is required; however, pin 29 should always be bypassed with 0.01μF to Audio Common.

ADJUSTMENT PROCEDURE

OFFSET—Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 12. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

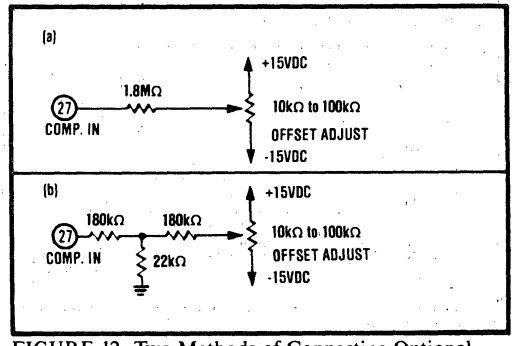


FIGURE 12. Two Methods of Connecting Optional Offset Adjust.

GAIN—Connect the Gain adjust potentiometer as shown in Figure 13. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

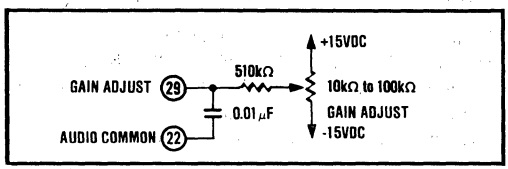


FIGURE 13. Connecting Optional Gain Adjust.

OUTPUT DRIVE

Normally all PCM75 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

ADDITIONAL OPTIONAL CONNECTIONS

The PCM75 may be operated with faster conversion times for resolutions less than 14 bits, if a higher THD is acceptable, by connecting Short Cycle (pin 32) as shown in Table III. Typical conversion times for the resolution and connections are indicated.

TABLE III. Short Cycle Connections for 14- to 16-Bit Resolutions.

Resolution (Bits)	16	15	14
Connect Pin 32 to	Open	Pin 16	Pin 15
Conversion Time (Typical) μsec	17	16	15

The Clock Rate pin may be connected to an external multiturn trim potentiometer with a TCR of ±100ppm/°C or less as shown in Figure 14. The typical conversion time vs the Clock Rate Control voltage is shown in Figure 15. The effect of varying the conversion time and the resolution on the total harmonic distortion is shown in Figures 16 and 17.

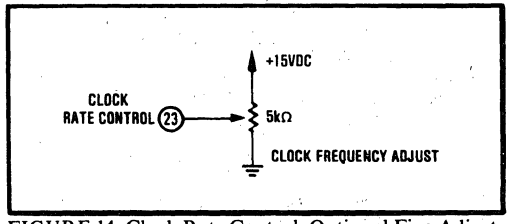


FIGURE 14. Clock Rate Control, Optional Fine Adjust.

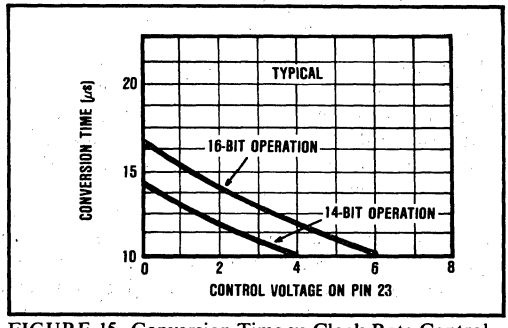


FIGURE 15. Conversion Time vs Clock Rate Control Voltage.

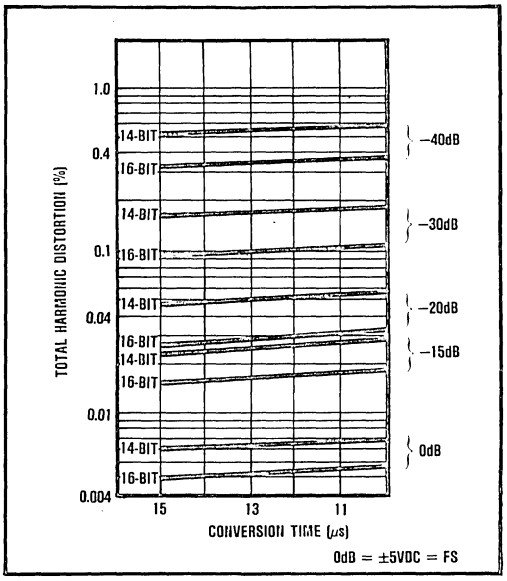


FIGURE 16. Total Harmonic Distortion vs Conversion Time.

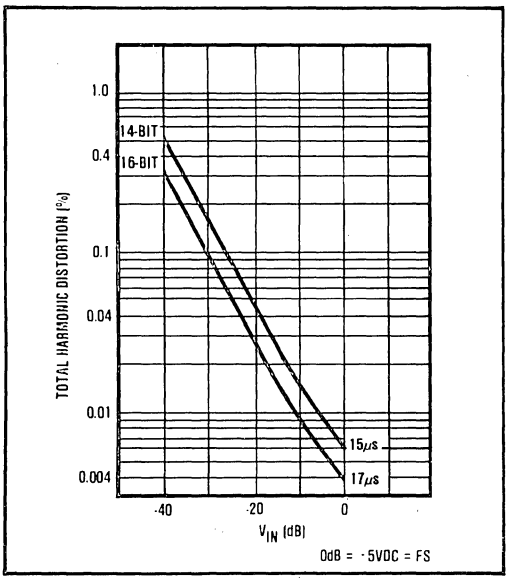
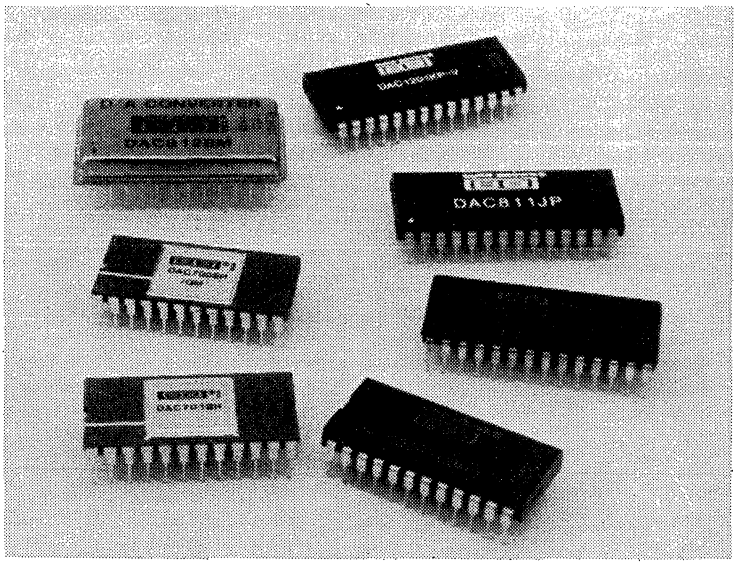


FIGURE 17. Total Harmonic Distortion vs Input Voltage Level.

DIGITAL-TO-ANALOG CONVERTERS



The Burr-Brown digital-to-analog converter product line contains a broad variety of products designed to simplify your task of converting digital information to analog form. The available products provide resolutions ranging from 8 bits to 16 bits, and encompass a variety of performance features and package types engineered to meet your needs for accuracy and reliability at low cost.

These products are designed to ease the task of application. Most units are complete, requiring no external components to achieve the desired function. All the D/A converters listed in this section include an internal reference and most have an output voltage amplifier, although the line also includes current output versions carefully designed for applications requiring current outputs, such as driving displays.

For low-cost general-purpose applications, consider the pin-compatible DAC800 and DAC80. If you require high resolution and accuracy, such as in test equipment and high performance instrumentation, the DAC700 and DAC70 families provide a variety of alternatives. Need high speed? Try the ECL-compatible DAC63 or TTL-compatible DAC812. The PCM52 and PCM53 have been optimized to provide 16-bit resolution with very low total harmonic distortion, required in audio and acoustic applications. Recent additions to the line include DAC708/709 and DAC811, designed for complete microprocessor compatibility. Refer to the Selection Guide in this section for a complete listing of available products.

Whether your system requires low cost, high resolution, high speed, wide temperature range, or low drift, consider Burr-Brown—a world leader in D/A converters.

SELECTION GUIDE

DIGITAL-TO-ANALOG CONVERTERS FOR INDUSTRIAL APPLICATIONS

The Burr-Brown DAC80 set the world-wide standard for complete hybrid and monolithic 12-bit D/A converters used in the past 10 years. Two years ago we added the DAC811, a complete 12-bit D/A converter with reference, output op amp and microprocessor interface logic—all on a single chip.

Burr-Brown is a world leader in the design and manufacture of 16-bit resolution D/A converters. Our product line includes a wide range of circuit options and packages. DAC700 through DAC703 are complete monolithic D/A converters. DAC705 through DAC709 provide microprocessor interface logic, allowing 8- and 16-bit ports, as well as serial data input (DAC708/709).

Technical advances in design and manufacturing, plus high volume production, have pushed our 16-bit D/A family far down the learning curve. A user today needs to carefully consider the low-cost 16-bit options before designing in an 8- or 12-bit converter.

16-BIT DIGITAL-TO-ANALOG CONVERTERS

Description	Model[1]	Resolution (Bits)	Linearity Error, max (% of FSR)	Gain Drift, max[2] (ppm/°C)	Zero Drift, max (ppm FSR/°C)	Output Ranges	Settling Time, max[3]	Temp Range[4]	Package	Page
High Resolution, Monolithic, Industry Standard; DAC 70, 71, 72 Compatible	DAC700KH	16	±0.003	±25	±5	0 to −1mA	1µsec	Com	24-pin DIP, Hermetic, Ceramic	6-98
	DAC700LH	16	±0.0015	±10	±3	0 to −1mA	1µsec	Com		6-98
	DAC700BH, (/QM)	16	±0.003	±15	±3	0 to −1mA	1µsec	Ind		6-98
	DAC700CH	16	±0.0015	±10	±3	0 to −1mA	1µsec	Ind		6-98
	DAC700SH, (/QM)	16	±0.003	±15	±3	0 to −1mA	1µsec	MIL		6-98
	DAC700BL, (/QM)	16	±0.003	±15	±3	0 to −1mA	1µsec	Ind	28-term. LCC, Hermetic, Ceramic	6-98
	DAC700SL, (/QM)	16	±0.003	±15	±3	0 to −1mA	1µsec	MIL		6-98
	DAC701KH	16	±0.003	±25	±5	0 to +10V	8µsec	Com	24-pin DIP, Hermetic, Ceramic	6-98
	DAC701LH	16	±0.0015	±10	±3	0 to +10V	8µsec	Com		6-98
	DAC701BH, (/QM)	16	±0.003	±15	±3	0 to +10V	8µsec	Ind		6-98
	DAC701CH	16	±0.0015	±10	±3	0 to +10V	8µsec	Ind		6-98
	DAC701SH, (/QM)	16	±0.003	±15	±3	0 to +10V	8µsec	MIL		6-98
	DAC701BL, (/QM)	16	±0.003	±15	±3	0 to +10V	8µsec	Ind	28-term. LCC, Hermetic, Ceramic	6-98
	DAC701SL, (/QM)	16	±0.003	±15	±3	0 to +10V	8µsec	MIL		6-98
	DAC702JP	16	±0.006	±30	±15	±1mA	350nsec, typ	Com	24-pin DIP, Plastic	6-98
	DAC702KP	16	±0.003	±25	±12	±1mA	1µsec	Com		6-98
	DAC702KH	16	±0.003	±25	±12	±1mA	1µsec	Com	24-pin DIP, Hermetic, Ceramic	6-98
	DAC702LH	16	±0.0015	±10	±5	±1mA	1µsec	Com		6-98
	DAC702BH, (/QM)	16	±0.003	±15	±10	±1mA	1µsec	Ind		6-98
	DAC702CH	16	±0.0015	±10	±5	±1mA	1µsec	Ind		6-98
	DAC702SH, (/QM)	16	±0.003	±15	±10	±1mA	1µsec	MIL		6-98
	DAC702BL, (/QM)	16	±0.003	±15	±10	±1mA	1µsec	Ind	28-term. LCC, Hermetic, Ceramic	6-98
	DAC702SL, (/QM)	16	±0.003	±15	±10	±1mA	1µsec	MIL		6-98
	DAC703JP	16	±0.006	±30	±15	±10V	4µsec, typ	Com	24-pin DIP, Plastic	6-98
	DAC703KP	16	±0.003	±25	±12	±10V	8µsec	Com		6-98
	DAC703KH	16	±0.003	±25	±12	±10V	8µsec	Com	24-pin DIP, Hermetic, Ceramic	6-98
	DAC703LH	16	±0.0015	±10	±5	±10V	8µsec	Com		6-98
	DAC703BH, (/QM)	16	±0.003	±15	±10	±10V	8µsec	Ind		6-98
	DAC703CH	16	±0.0015	±10	±5	±10V	8µsec	Ind		6-98
	DAC703SH, (/QM)	16	±0.003	±15	±10	±10V	8µsec	MIL		6-98
	DAC703BL, (/QM)	16	±0.003	±15	±10	±10V	8µsec	Ind	28-term. LCC, Hermetic, Ceramic	6-98
	DAC703SL, (/QM)	16	±0.003	±15	±10	±10V	8µsec	MIL		6-98
High Resolution, Micro-Processor Interface, 16-bit port	DAC705KH	16	±0.003	±25	±12	±5V	8µsec	Com	28-pin DIP, Hermetic, Ceramic	6-106
	DAC705BH, (/QM)	16	±0.003	±15	±10	±5V	8µsec	Ind		6-106
	DAC705SH, (/QM)	16	±0.003	±15	±10	±5V	8µsec	MIL		6-106
	DAC706KH	16	±0.003	±25	±12	±1mA	350nsec, typ	Com	28-pin DIP, Hermetic, Ceramic	6-106
	DAC706BH, (/QM)	16	±0.003	±15	±10	±1mA	350nsec, typ	Ind		6-106
	DAC706SH, (/QM)	16	±0.003	±15	±10	±1mA	350nsec, typ	MIL		6-106
	DAC707KH	16	±0.003	±25	±12	±10V	8µsec	Com	28-pin DIP, Hermetic, Ceramic	6-106
	DAC707BH, (/QM)	16	±0.003	±15	±10	±10V	8µsec	Ind		6-106
	DAC707SH, (/QM)	16	±0.003	±15	±10	±10V	8µsec	MIL		6-106
High Resolution, Micro-Processor Interface, 8-bit Port, Serial Input	DAC708KH	16	±0.003	±25	±5U, ±12B[5]	±1, −2mA	350nsec, typ	Com	24-pin DIP, Hermetic, Ceramic	6-106
	DAC708BH, (/QM)	16	±0.003	±15	±3U, ±10B[5]	±1, −2mA	350nsec, typ	Ind		6-106
	DAC708SH, (/QM)	16	±0.003	±15	±3U, ±10B[5]	±1, −2mA	350nsec, typ	MIL		6-106
	DAC709KH	16	±0.003	±25	±5U, ±12B[5]	±5, ±10, +10V	8µsec	Com	24-pin DIP, Hermetic, Ceramic	6-106
	DAC709BH, (/QM)	16	±0.003	±15	±3U, ±10B[5]		8µsec	Ind		6-106
	DAC709SH, (/QM)	16	±0.003	±15	±3U, ±10B[5]		8µsec	MIL		6-106
Motor Control, Monolithic	DAC710KH	16	±0.003	±50		±1mA	350nsec, typ	Com	24-pin DIP, Hermetic, Ceramic	6-116
	DAC711KH	16	DLE around BP Zero	±50		±10V	8µsec	Com		6-116
Monolithic Replacements for Industry Standard Hybrids	DAC71-CSB-I	16	±.003	±45	±1	0 to −2mA	1µsec	Com	24-pin DIP, Hermetic, Ceramic	6-28
	DAC71-COB-I	16	±.003	±45	±40	±1mA	1µsec	Com		6-28
	DAC71-COB-V	16	±.003	±15	±10	±10V	10µsec	Com		6-28
	DAC71-CSB-V	16	±.003	±15	±2	0 to +10V	10µsec	Com		6-28
CCD Code Hybrids	DAC71-CCD-I	4 Digit	±0.005	±45	±1	0 to −1.25mA	1µsec	Com	24-pin DIP	6-35
	DAC71-CCD-V	4 Digit	±0.005	±15	±1	0 to +10V	10µsec	Com	24-pin DIP	6-35
High Resolution, High Accuracy	DAC73J	16	±0.0015	±10[6]	±2U, ±5B[6]	±1, −2mA, ±2.5, ±5, ±10, +5, +10V	50µsec, typ	Com	Modular	6-41
	DAC73K	16	±0.00075	±10[6]	±2U, ±5B[6]		50µsec, typ	Com	Modular	6-41
	DAC736J	16	±0.0015	±10[6]	±2U, ±5B[6]		50µsec, typ	Com	Modular	6-41
	DAC736K	16	±0.00075	±10[6]	±2U, ±5B[6]		50µsec, typ	Com	Modular	6-41

12-BIT DIGITAL-TO-ANALOG CONVERTERS

Description	Model[1]	Resolution (Bits)	Linearity Error, max (% of FSR)	Gain Drift, max[2] (ppm/°C)	Zero Drift, max (ppm FSR/°C)	Output Ranges	Settling Time, max[3]	Temp Range [4]	Package	Page
Monolithic, Low Cost, Industry Standard Pinout	DAC800P-CBI-I	12	±0.012	±30	±3U, ±15B[7]	±1, −2mA	300nsec, typ	Com	24-pin DIP, Plastic	6-123
	DAC800P-CBI-V	12	±0.012	±30	±3U, ±15B[7]	±2.5, ±5, ±10, +5, +10V	5μsec	Com		6-123
	DAC800-CBI-I	12	±0.012	±30	±3U, ±15B[7]	±1, −2mA	300nsec, typ	Com	24-pin DIP, Hermetic, Ceramic	6-123
	DAC800-CBI-V	12	±0.012	±30	±3U, ±15B[7]	±2.5, ±5, ±10, +5, +10V	5μsec	Com		6-123
	DAC850-CBI-I, (/QM)	12	±0.012	±20	±3U, ±10B[7]	±1, −2mA	300nsec, typ	Ind	24-pin DIP, Hermetic, Ceramic	6-144
	DAC850-CBI-V, (/QM)	12	±0.012	±20	±3U, ±10B[7]	±2.5, ±5, ±10, +5, +10V	5μsec	Ind		6-144
	DAC850BL-I, (/QM)	12	±0.012	±20	±3U, ±10B[7]	±1, −2mA	300nsec, typ	Ind	28-term. LCC, Hermetic, Ceramic	6-144
	DAC850BL-V, (/QM)	12	±0.012	±20	±3U, ±10B[7]	±2.5, ±5, ±10, +5, +10V	5μsec	Ind		6-144
	DAC851-CBI-I, (/QM)	12	±0.012	±25	±3U, ±15B[7]	±1, −2mA	300nsec, typ	MIL	24-pin DIP, Hermetic, Ceramic	6-144
	DAC851-CBI-V, (/QM)	12	±0.012	±25	±3U, ±15B[7]	±2.5, ±5, ±10, +5, +10V	5μsec	MIL		6-144
	DAC851SL-I, (/QM)	12	±0.012	±25	±3U, ±15B[7]	±1, −2mA	300nsec, typ	MIL	28-term. LCC, Hermetic, Ceramic	6-144
	DAC851SL-V, (/QM)	12	±0.012	±25	±3U, ±15B[7]	±2.5, ±5, ±10, +5, +10V	5μsec	MIL		6-144
Monolithic, Micro-Processor Interface, Low Cost	DAC811JP	12	±0.012	±30	±10U, ±10B[5]	±5, ±10, +10	4μsec	Com	28-pin DIP, Plastic	6-130
	DAC811KP	12	±0.006	±20	±7U, ±7B[5]	±5, ±10, +10	4μsec	Com		6-130
	DAC811AH, (/QM)	12	±0.012	±30	±10U, ±10B[5]	±5, ±10, +10	4μsec	Ind	28-pin DIP, Hermetic, Ceramic	6-130
	DAC811BH, (/QM)	12	±0.006	±20	±7U, ±7B[5]	±5, ±10, +10	4μsec	Ind		6-130
	DAC811RH, (/QM)	12	±0.012	±30	±10U, ±10B[5]	±5, ±10, +10	4μsec	MIL		6-130
	DAC811SH, (/QM)	12	±0.006	±20	±7U, ±7B[5]	±5, ±10, +10	4μsec	MIL		6-130
	DAC811AL, (/QM)	12	±0.012	±30	±10U, ±10B[5]	±5, ±10, +10	4μsec	Ind	28-term. LCC, Hermetic, Ceramic	6-130
	DAC811BL, (/QM)	12	±0.006	±20	±7U, ±7B[5]	±5, ±10, +10	4μsec	Ind		6-130
	DAC811RL, (/QM)	12	±0.012	±30	±10U, ±10B[5]	±5, ±10, +10	4μsec	MIL		6-130
	DAC811SL, (/QM)	12	±0.006	±20	±7U, ±7B[5]	±5, ±10, +10	4μsec	MIL		6-130
Industry Standard DAC80 Monolithic	DAC80-CBI-I	12	±0.012	±30	±3U, ±15B[7]	±1, −2mA	300nsec, typ	Com	24-pin DIP, Hermetic, Ceramic	6-64
	DAC80-CBI-V	12	±0.012	±30	±3U, ±15B[7]	±2.5, ±5, ±10, +5, +10V	3μsec, typ	Com		6-64
	DAC80P-CBI-I	12	±0.012	±30	±3U, ±15B[7]	±1, −2mA	300nsec, typ	Com	24-pin DIP, Plastic	6-64
	DAC80P-CBI-V	12	±0.012	±30	±3U, ±15B[7]	±2.5, ±5, ±10, +5, +10	3μsec, typ	Com		6-64
DAC80 with Decimal Coding	DAC80-CCD-I	3 Digit	±0.025	±30	±3U, ±15B[7]	0 to −2mA	300nsec, typ	Com	24-pin DIP, Ceramic	6-72
	DAC80-CCD-V	3 Digit	±0.025	±30	±3U, ±15B[7]	0 to +10V	5μsec, typ,	Com		6-72
Industry Standard DAC85 Monolithic	DAC85H-CBI-I, (QM)	12	±0.012	±20	±3U, ±10B[7]	±1, −2mA	300nsec, typ	Ind	24-pin DIP, Hermetic, Ceramic	6-85
	DAC85H-CBI-V, (QM)	12	±0.012	±20	±3U, ±10B[7]	±2.5, ±5, ±10, +5, +10V	3μsec, typ	Ind		6-85
	DAC85L-V, (QM)	12	±0.012	±20	±3U, ±10B[7]	±2.5, ±5, ±10, +5, +10V	3μsec, typ	Ind	28-term LCC, Hermetic, Ceramic	6-85
MIL Temp. −55°C to +125°C, Monolithic	DAC87H-CBI-V, (QM)	12	±0.012	±20	±3U, ±10B[7]	±2.5, ±5, ±10, +5, +10	3μsec, typ	MIL	24-pin DIP Hermetic, Ceramic	6-85
	DAC87L-V, (QM)	12	±0.012	±20	±3U, ±10B[7]	±2.5, ±5. ±10 +5, +10	3μsec, typ	MIL	28-term. LCC, Hermetic, Ceramic	6-85
Ultra-High Speed, ECL Input	DAC63BG	12	±0.012	±40	±1U, ±15B[7]	±5, −10mA	55nsec[9]	Ind	24-pin DIP, Ceramic	6-12
	DAC63CG	12	±0.012	±30	±0.6U, ±10B[7]	±5, −10mA	50nsec[9]	Ind		6-12
	DAC63BM	12	±0.012	±40	±1U, ±15B[7]	±5, −10mA	55nsec[9]	Ind	24-pin DIP, Hermetic, Metal	6-12
	DAC63CM	12	±0.012	±30	±0.6U, ±10B[7]	±5, −10mA	50nsec[9]	Ind		6-12
	DAC63SM	12	±0.012	±40	±1U, ±15B[7]	±5, −10mA	55nsec[9]	MIL		6-12
	DAC63TM	12	±0.012	±30	±0.6U, ±10B[7]	±5, −10mA	50nsec[9]	MIL		6-12
Ultra-High Speed, TTL Input	DAC812BM	12	±0.012	±40	±1U, ±15B[7]	±5, −10mA	65nsec	Ind	24-pin DIP, Hermetic	6-138
	DAC812CM	12	±0.012	±20	±0.5U, ±10B[7]	±5, −10mA	80nsec	Ind		6-138
Monolithic 8-Bit	DAC90BG, (Q)	8	±0.2	±75	±2U, ±75B[7]	±1, −2mA	200nsec, typ	Ind	16-pin DIP Hermetic, Ceramic	6-93
	DAC90SG, (Q)	12	±0.2	±75	±2U, ±75B[7]	±1, −2mA	200nsec, typ	MIL		6-93
Wide Temp −55°C to +200°C	DAC10HT	12	±0.012	±10[8]	±2U, ±10B[7]	±2.5, ±5, ±10,	300nsec, typ	−55°C to +200°C	24-pin DIP Hermetic, Ceramic	6-5
Military				See Military Products, section 12.						

NOTES: (1) "Q" or "/QM" indicates product is also available with screening for increased reliability. See High Reliability Screening, section 12. (2) This spec applies to current output D/A converters when used with an external output amplifier and also using the internal feedback resistor of the D/A converter. (3) For 12-bit converters: settling to within ±0.012% of FSR (±1/2LSB). For 16-bit converters: settling to within ±0.003% of FSR. (4) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (5) U = Unipolar Zero; B = Bipolar Zero. (6) Exclusive of Reference Drift. (7) U = Unipolar Zero; B = Bipolar Offset. (8) DAC80Z models are available that operate from ±12V power supplies. (9) Settling time to within ±1LSB.

DIGITAL-TO-ANALOG CONVERTERS FOR COMMERCIAL APPLICATIONS

Achieving new levels of price/performance in low cost D/As, these 12- and 16-bit converters are truly the lowest priced complete D/As on the market. The prices of these parts make it possible to apply high resolution solutions to your cost sensitive applications. These D/A converters are ideal for applications where high resolution and monotonicity are the key application parameters and where tightly-specified performance over temperature is not required. Use of reliable, cost-effective plastic packages makes these parts the solution of choice in many commercial applications.

DIGITAL-TO-ANALOG CONVERTERS

Description	Model[1]	Resolution (Bits)	Linearity Error, max (% of FSR)	Gain Drift, typ (ppm/°C)	Zero Drift, typ (ppm FSR/°C)	Output Ranges (V)	Settling Time, max[1]	Temp Range [2]	Package	Page
12-Bit Microprocessor Interface	DAC1200KP-V	12	±0.018	±10	±8, Bipolar Offset	±2.5, ±5, ±10, +5, +10	7μsec	Com	24-pin DIP, Plastic	6-151
	DAC1201KP-V	12	±0.018	±10	±6, Bipolar Zero	±5, ±10, +10	7μsec	Com	28-pin DIP, Plastic	6-155
16-Bit	DAC1600JP-V	16	±0.006	±10	±5, Bipolar Zero	±10	10μsec	Com	24-pin DIP, Plastic	6-160
	DAC1600KP-V	16	±0.003	±10		±10	10μsec	Com		6-160

NOTES: (1) For 12-bit converters: to within ±0.012% of FSR (±1/2LSB). For 16-bit converters: to within ±0.003% of FSR (±1/2LSB at 14 bits). (2) Com = 0°C to +70°C.

ULTRA-HIGH SPEED CONVERTERS

Burr-Brown is committed to applying higher levels of integration to high performance converter components. Our ultra-high speed D/A converters are listed here.

ULTRA-HIGH SPEED CONVERTERS										
Digital-to-Analog	Model	Resolution (Bits)	Linearity Error, max (% of FSR)	Gain Drift, max[2] (ppm/°C)	Zero Drift, max[3] (ppm FSR/°C)	Output Ranges (mA)	Settling Time, max (nsec)[4]	Temp Range	Package	Page
Ultra-High Speed, ECL Input	DAC63BG	12	±0.012	±40	±1U, ±15B	±5, −10mA	50	Ind	24-pin DIP, Ceramic	6-12
	DAC63CG	12	±0.012	±30	±0.6U, ±10B	±5, −10mA	50	Ind		6-12
	DAC63BM	12	±0.012	±40	±1U, ±15B	±5, −10mA	65	Ind		6-12
	DAC63CM	12	±0.012	±30	±0.6U, ±10B	±5, −10mA	65	Ind	24-pin DIP, Metal	6-12
	DAC63SM	12	±0.012	±40	±1U, ±15B	±5, −10mA	65	MIL		6-12
	DAC63TM	12	±0.012	±30	±0.6U, ±10B	±5, −10mA	65	MIL		6-12
Ultra-High Speed, TTL Input	DAC812BM	12	±0.012	±40	±1U, ±15B	±5, −10mA	65	Ind	24-pin DIP, Metal	6-138
	DAC812CM	12	±0.012	±20	±0.5U, ±10B	±5, −10mA	80	Ind		6-138

NOTES: (1) This spec applies to current output D/A converters when used with an external output amplifier and also using the internal feedback resistor of the D/A converter. (2) COM = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) U = Unipolar Zero, B = Bipolar Offset. (4) Settling to within ±1LSB.

CONVERTERS FOR DIGITAL AUDIO APPLICATIONS

Burr-Brown PCM D/A converters have set the standards for price/performance in digital audio applications world-wide. Applications include compact disk players and electronic musical instruments and systems. Our broad product line provides a wide range of choices of specifications, features and power supply voltages making Burr-Brown PCM D/A converters ideal for any digital audio application.

PCM DIGITAL-TO-ANALOG CONVERTERS									
Description	Model	Resolution (Bits)	Total Harmonic Distortion, max	Settling Time, typ (FSR to ±1/2LSB)	Output Range	Temp Range [1]	Dynamic Range (dB)	Package	Page
±15V Supplies	PCM53JG-V	16	0.004% at FS	3µsec	±10V	Com	96dB	24-pin DIP, Ceramic	6-164
	PCM53JG-I	16	0.004% at FS	350nsec	±1mA	Com	96dB		6-164
	PCM53JP-V	16	0.004% at FS	3µsec	±10V	Com	96dB		6-164
	PCM53JP-I	16	0.004% at FS	350nsec	±1mA	Com	96	24-pin DIP, Plastic	6-168
	PCM53KP-I	16	0.0025% at FS	350nsec	±1mA	Com	96		6-168
	PCM53JP-V	16	0.004% at FS	3µsec	±10V	Com	96		6-168
	PCM53KP-V	16	0.0025% at FS	3µsec	±10V	Com	96		6-168
+5V to ±12V Supplies	PCM54HP[2]	16	0.008% at FS	3µsec	±3V	Com	96	28-pin DIP, Plastic	6-180
	PCM54JP	16	0.004% at FS	3µsec	±3V	Com	96		6-180
	PCM54KP	16	0.0025% at FS	3µsec	±3V	Com	96		6-180
SOIC Package, ±5V Supplies	PCM55HP[3]	16	0.008% at FS	3µsec	±3V	Com	96	24-lead Plastic SOIC	6-180
	PCM55JP	16	0.004% at FS	3µsec	±3V	Com	96		6-180

NOTES: (1) Com = 0 to +70°C. (2) Operates on ±5V to ±12V supplies. (3) Operates on ±5V supplies.

BURR-BROWN®

DAC10HT

A Wide Temperature Range General Purpose 12-Bit DIGITAL-TO-ANALOG CONVERTER

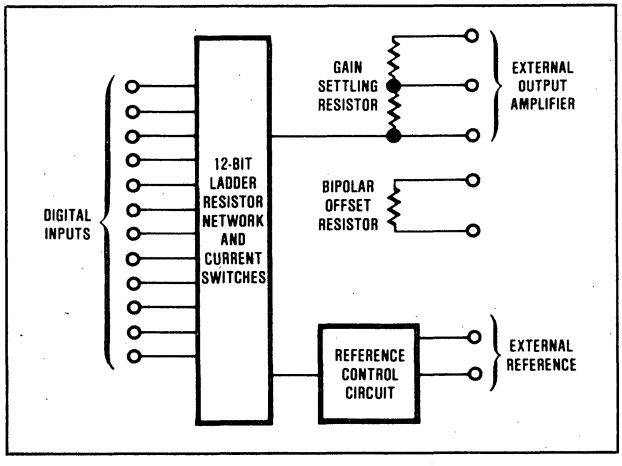
FEATURES

- −55°C TO +200°C SPECIFICATION
- FULL 12-BIT RESOLUTION
- 300nsec SETTLING TIME, TYPICAL
- MONOTONIC OVER FULL TEMPERATURE RANGE
- TTL- AND CMOS-COMPATIBLE
- HERMETIC DUAL-WIDTH CERAMIC PACKAGE

DESCRIPTION

Desiged for use in circuits that operate over a wide temperature range, DAC10HT is a general purpose, 12-bit D/A converter. The design uses state-of-the-art integrated circuit and laser-trimmed thin-film techniques for maximum accuracy. Compatible with TTL and CMOS logic, DAC10HT is monotonic over the full −55°C to +200°C temperature range. Special design techniques minimize output glitches. The package is a compact, dual-width, 24-pin ceramic DIL.

100% screening operations are conducted at key manufacturing steps. Burn-in and temperature cycling are examples.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at V_{CC} = +15VDC, V_{EE} = -15VDC, Reference = +10VDC, and T_A = +25°C unless otherwise noted.

MODEL	DAC10HT			
	MIN	TYP	MAX	UNITS
INPUT				
DIGITAL INPUTS				
Resolution	12			Bits
TTL-Logic "1" at 100nA, max	2.0			V
Logic "0" at -100μA, max			0.8	V
Logic "0" at −100μA, max, at +200°C			0.6	V
CMOS(1)-Logic "1" at 100nA, max	70% V_{CC}			V
Logic "0" at -100μA, max			30% V_{CC}	V
TRANSFER CHARACTERISTICS				
ACCURACY				
Linearity Error at +25°C				
12-Bit		±1/4	±1/2	LSB
at -55°C to +200°C				
12-Bit			±2	LSB
Gain Error(2)		0.05	0.2	%
Bipolar Offset Error (input all 0's)(2)		0.05	0.2	% of FSR
Unipolar Offset Error (input all 0's)(2)			0.2	% of FSR
Monotonic Temperature Range				
12-Bit	-55		+200	°C
Differential Linearity Error				
12-Bit		±1/2	±1	LSB
Total Unadjusted Error(3)				
+25°C		±0.1	±0.4	% of FSR
-55°C to +200°C		±0.3	±0.8	% of FSR
Total Adjusted Error(4)				
+25°C		±0.006	±0.012	% of FSR
-55°C to +200°C		±0.015	±0.40	% of FSR
CONVERSION SPEED				
Setting Time to ±1/2LSB (+FS change)(5)		300		nsec
Major Carry Glitch Duration				
(to 90% complete)		35		nsec
DRIFT (-55°C to +200°C)				
Gain (exclusive of reference drift)		±2	±10	ppm/°C
Bipolar Offset		±2	±10	ppm of FSR/°C
Unipolar Offset		±1	±2	ppm of FSR/°C
Differential Linearity		±2	±3	ppm of FSR/°C
OUTPUT				
Current - Unipolar (±10%)		0 to -2		mA
Current - Bipolar (±10%)		-1 to +1		mA
Selectable Ranges(6)	0 to +5, 0 to +10, -2.5 to +2.5, -5 to +5, -10 to +10			V
Resistance		2		kΩ
Capacitance		20		pF
Compliance Voltage		±1		V
EXTERNAL ADJUSTMENTS				
Gain Adjust Range		±0.25		% of FSR
Bipolar Offset Adjust Range		±0.25		% of FSR
Unipolar Offset Adjust Range		±0.25		% of FSR
NOISE (0.1Hz to 10Hz, all "1"s)		30		μV, p-p
MULTIPLYING MODE PERFORMANCE				
Number of Quadrants(7)			2	
Reference Voltage Range	0		+10.24	V
Accuracy(8)	±0.05			% of FSR
Feedthrough(9)		±0.02		% of FSR
Output Slew Rate(10)		6		mA/μsec
Output Settling Time (to 0.01% of FS)(10)		3		μsec
Control Amplifier BW (small-signal, closed-loop)		10		MHz
POWER SUPPLIES AND REFERENCE				
Reference Input Impedance		20±10%		kΩ
Reference Voltage Range	0		+10.0	V
Power Supply, Voltage - V_{CC}	+4.75		+15.0	VDC
Voltage - V_{EE}	-13.5	-15	-16.5	VDC
Current - V_{CC}		+9	+15.0	mA
Current - V_{EE}		-28	-40.0	mA
Power Supply Sensitivity				
V_{CC} at +5VDC		1	5	ppm/%ΔV
V_{EE} at -15VDC		3	10	ppm/%ΔV

ELECTRICAL (CONT)

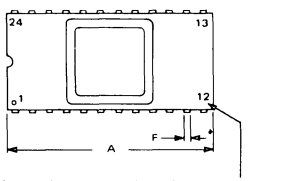
MODEL	DAC10HT			UNITS
	MIN	TYP	MAX	
TEMPERATURE RANGE				
Specification	-55		+200	°C
Operating	-55		+200	°C
Storage	-65		+210	°C

NOTES:
1. +4.75V < V_{CC} < +15.0V and pin 2 tied to pin 1.
2. Adjustable to zero (see Figures 4 and 5).
3. Includes Gain, Offset, and Linearity Errors with external +10.0V ±1mV reference. Does not include Reference Drift.
4. Gain and Offset Errors removed at +25°C with external +10.0V ±1mV reference. Does not include Reference Drift.
5. Current settling into short circuit.
6. Using internal scaling resistors and OPA11HT output op amp.
7. Bipolar operation at digital inputs only.
8. For 1VDC reference voltage (see Figure 2). Full Scale Range = 1V.
9. Voltage at reference input: 0 to +10V, 2kHz sine wave (see Figure 3).
10. All "1"s, 10V step on reference input.

PIN DESIGNATIONS

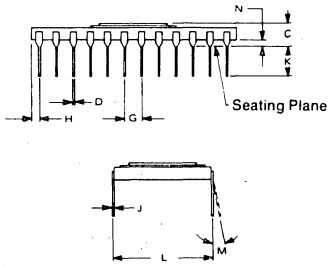
+V_{CC}	1	24	BIT 1 (MSB)
LOGIC THRESHOLD	2	23	BIT 2
V_{REF} INPUT (LO)	3	22	BIT 3
N/C	4	21	BIT 4
V_{REF} INPUT (HI)	5	20	BIT 5
-V_{EE}	6	19	BIT 6
BIPOLAR OFFSET	7	18	BIT 7
BIPOLAR OFFSET	8	17	BIT 8
CURRENT OUTPUT	9	16	BIT 9
10V RANGE	10	15	BIT 10
20V RANGE	11	14	BIT 11
COMMON	12	13	BIT 12 (LSB)

MECHANICAL



Pin numbers shown for reference only.
Numbers may not be marked on package.

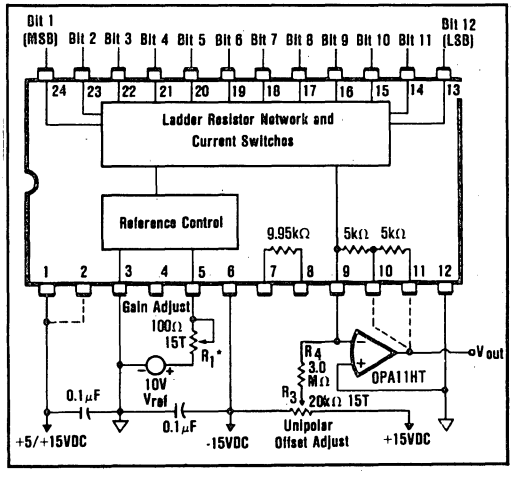
NOTE:
Leads in true position within 0.010"
(0.25mm)R at MMC at seating plane.



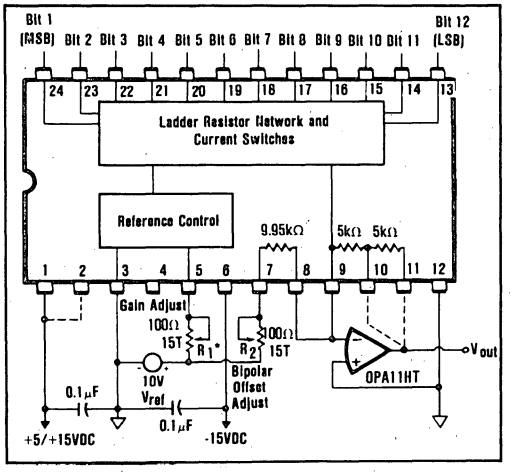
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	— —	10°	— —	10°
N	.025	.060	0.64	1.52

CASE: Ceramic with hermetic seal

CONNECTION DIAGRAM - UNIPOLAR



CONNECTION DIAGRAM - BIPOLAR



*In high temperature environments with high levels of shock and vibration it is recommended that discrete wirewound or metal film resistors be used instead of potentiometers.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

DAC10HT accepts a positive-true straight binary (BIN) input code. Offset-binary code is created by offsetting the output amplifier with the DAC reference. Two's complement code is obtained from offset binary by inverting bit 1 (the most significant bit) externally. See Table I.

ACCURACY

Linearity of the DAC10HT is guaranteed to be within the specification over its temperature range. This is the measure of the deviation of the actual transfer curve from the ideal transfer curve expressed graphically as a straight line drawn between the end-point values. For the DAC10HT the maximum deviation is ±1 2LSB at 25°C and ±LSB over the full specification temperature range from −55°CC to +200°C.

Differential Linearity error is the deviation from an ideal 1LSB output voltage change from one adjacent state to the next. An error specification of ±1/2LSB indicates that output voltage step size can range from 1/2LSB to 3/2LSB between adjacent states.

Monotonicity is an important property for a D/A converter, especially one used in a closed control loop. A converter is monotonic if the output signal increases or remains the same for an increase in digital input. A converter's differential linearity determines whether or not it is monotonic. If differential linearity is <±1LSB, the converter will be monotonic. Monotonicity is guaranteed over the entire specified temperature range for the DAC10HT.

Leakage Current is measured at the converter output with logic 0 on all digital inputs. It appears as part of offset error, both at room temperature and over the specified temperature range. In the unipolar configuration, virtually all offset error is due to leakage current.

DRIFT

Gain Drift is a measure of the change in the full scale range output due to a change in temperature and is expressed in parts per million per °C (ppm/°C). It is calculated by determining the full scale range value at high temperature, then at low temperature. The difference in the two values is divided by the difference in the two temperatures.

Offset Drift is a measure of the actual change in output over the specified temperature range with logic 0 on all digital inputs. It is calculated by measuring offset voltage at the temperature extremes. The maximum change referred to the offset voltage at +25°C is divided by the temperature excursion from +25°C. Offset drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

Differential Linearity Drift (the change in differential linearity over the specified temperature range) is calculated in a manner similar to offset drift and is expressed in ppm of FSR/°C.

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES				
	ANALOG OUTPUT			
LOGIC INPUTS	VOLTAGE*		CURRENT	
Binary	0 to +10V	-10V to +10V	0 to -2mA	-1mA to +1mA
111111111111	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
100000000000	+5.0000V	0.0000V	-1.0000mA	0.0000mA
011111111111	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
000000000000	0.0000V	-10.0000V	0.0000mA	+1.0000mA
Binary Two's Complement**				
011111111111		+9.9951V		-0.9995mA
000000000000		0.0000V		0.0000mA
111111111111		-0.0049V		+0.0005mA
100000000000		-10.000V		+1.0000mA
1LSB (BIN)	2.44mV	4.88mV	0.488μA	0.488μA

* To obtain values for other binary ranges: 0 to +5V range—divide 0 to +10V range values by 2; ±5V range—divide ±10V range values by 2; ±2.5V range—divide ±10V range values by 4.
** MSB must be inverted externally for this code.

CONVERSION SPEED

Settling Time is the time required for the output to enter and remain within an error band of the final value measured from the time the digital input is changed.

The settling time for a 1LSB change at the input is naturally less than for a full scale change. It is greatest at the major carry point (the point at which all of the bits change states) due to nonuniform switching times of the internal current switches. For a 1LSB change at the major carry point, settling time to within ±0.01% will typically be 300nsec.

COMPLIANCE VOLTAGE

This is the maximum voltage which can be impressed on the current output node and still remain within the specified accuracy. These voltages are −1.0V and +1.0V.

POWER SUPPLY SENSITIVITY

This measure of the effect of a power supply voltage change on the D/A converter output is defined as a percent of FSR/percent of change in either the +5V, +15V or -15V power supplies about the nominal supply voltages. Figure 1 shows power supply rejection vs frequency.

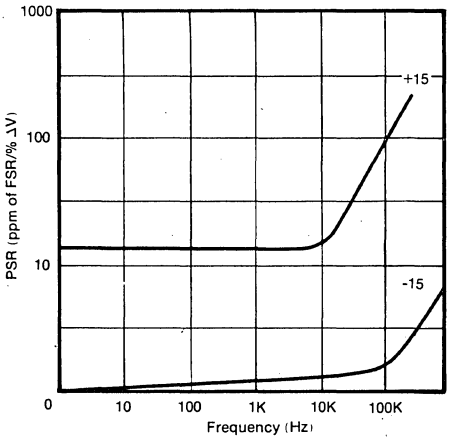


FIGURE 1. Power-Supply Rejection vs Power-Supply Ripple Frequency.

MULTIPLYING MODE PERFORMANCE

The output of the DAC10HT is the product of the reference input and digital input values. The reference may be an AC signal and can vary from 0 to +10 volts. This is useful in applications where digitally programmed attenuation of a signal is desired. Bcause the reference voltage input must be positive, the DAC10HT multiplies in two quadrants only. For highest accuracy the input reference voltage should be as high as possible (see Figure 2).

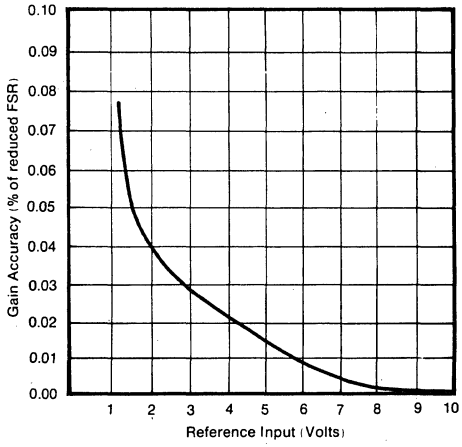


FIGURE 2. Gain Accuracy vs Reference Voltage.

Feedthrough of the DAC10HT is the amount of reference signal that appears at the output when all digital inputs are logic 0. Expressed in % of FSR, it increases with increasing reference frequency (see Figure 3).

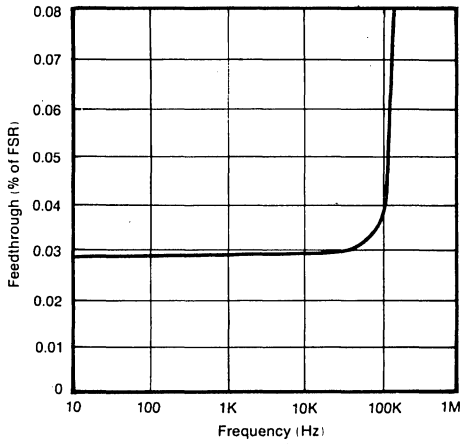


FIGURE 3. Feedthrough Voltage vs Power-Supply Ripple Frequency (Unipolar Mode).

OPERATING INSTRUCTIONS

INPUT LOGIC LEVELS

Inputs of the DAC10HT are either TTL or CMOS logic compatible. For TTL, connect +5V to pin 1 (pin 2 open). For +5V CMOS, connect +5V to pins 1 and 2. For +15V CMOS compatibility, connect +15V to pins 1 and 2.

In circuits where pin 2 is used to determine the digital threshold level, the following application tip may be helpful. If the analog system ground (to which the DAC10HT is referred) is separate from the digital driving logic ground, the threshold voltage input (at pin 2) may be driven from an external voltage source to keep the threshold at proper value. Threshold voltage will always be at one-half the voltage applied to pin 2 ($+1.4V < \text{pin } 2 < +15V$).

POWER SUPPLIES

Each power supply should be bypassed to ground with a 0.1μF capacitor as shown in the Connection Diagrams. Locate the capacitors as close as possible to the DAC10HT.

GAIN AND OFFSET ADJUSTMENTS

(Voltage Output Configuration)

Initial gain and offset errors of the DAC10HT circuit may be trimmed out using the following procedures:

Unipolar configuration - input all 0's and null offset error by adjusting R_3 until output voltage equals zero. Input all 1's and adjust R_1 until the output voltage is +FS -1LSB (see Table I and Connection Diagram).

Bipolar configuration - input all 0's and null offset error by adjusting R_2 until output voltage equals -FS. Input all 1's and adjust R_1 until the output voltage is +FS - 1LSB (see Table I and Connection Diagram).

To obtain specified gain and offset errors, replace the 100Ω potentiometers (R_1 and R_2) shown in the Connection Diagrams with 50Ω 0.1% fixed resistors.

SELECTING AN EXTERNAL REFERENCE

DAC10HT is configured to use a +10V reference. An internal 19.9Ω resistor in series with an external 100Ω adjust potentiometer sets the current into the reference input at 0.5mA (see Figure 4).

Temperature drift of the reference increases drift of the entire circuit. In unipolar configurations the drift specification adds directly to the total circuit drift. In the bipolar configuration some drift cancelling effects take place. One-half of the reference drift added to the total DAC drift will give total circuit drift.

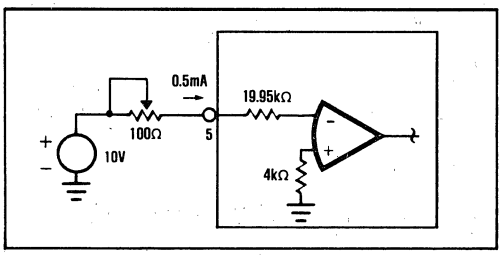


FIGURE 4. Using a +10V Reference.

SELECTING AN EXTERNAL REFERENCE

Building An External +10V 200°C Reference

The DAC10HT requires an external +10V reference for normal operation. A circuit for obtaining this reference voltage that will operate a +200°C is shown in Figure 5. The value of R_1 or R_2 should be adjusted to provide a reference voltage of 10V ±1mV due to the tolerance of the zener voltage. With no adjustment to the zener current for optimum zero T.C. point this reference will have an average temperature coefficient of about ±20ppm/°C over −55°C to +200°C.

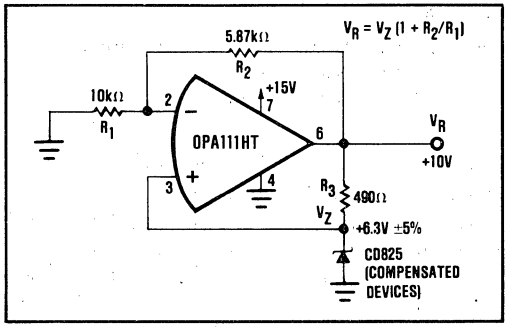


FIGURE 5. +10V Reference That Will Operate at +200°C.

LOW POWER OPERATION

The typical supply currents required by the DAC10HT under normal operating conditions are 9mA (V_{CC}) and 28mA (V_{EE}). The average power required (P_D) is therefore

$$P_D = |V_{CC} \times 9mA| + |V_{EE} \times 28mA|$$
$$= 555mW\ (+V_S = 15V, -V_S = 15V), \text{ or}$$
$$= 465mW\ (+V_S = 5V, -V_S = 15V).$$

Under certain operating conditions this power consumption can be reduced to as little as 245mW.

The major contributor to the power consumption is the -15V supply. As long as a +10V reference is used, V_{EE} must be between -13.5V and -16.5V. If, however, a lower reference voltage is used, V_{EE} can be reduced considerably and this greatly reduces the power consumption. Lowering the reference voltage will, of course, lower the full scale output voltage by a proportional amount. For example, if the reference voltage is +5V, the full scale output voltage when using the 10V range pin (pin 10) will be +5V instead of +10V with a +10V reference in the unipolar mode of operation. Table II indicates the minimum supply voltages and the power consumption obtained when using these supply voltages for various values of V_{REF}.

TABLE II. Minimum Power Supply Voltages and Typical Power Consumption for Operation with Various Values of V_{REF}.

External V_{REF}	$+V_{CC}$ (Pin 1)	$-V_{EE}$ (Pin 6)	Total Power Consumption (Typical)
+10V	+5V	-13V	409mW
+6.3V	+5V	-10V	275mW
+5V	+5V	-8V	235mW

SELECTING AN OUTPUT AMPLIFIER

The most important characteristics of the output amplifier are input offset voltage drift, input bias (or difference) current drift, and settling time. Specifications over the full operating temperature range are very important. Initial input offset voltage and bias current effects will be trimmed out, but bias errors will be introduced as these parameters drift with temperature changes. Errors introduced will appear as offset in the D/A circuit output.

Table III provides the equations used to convert these amplifier errors to D/A output errors.

TABLE III. Computing DAC Error Contributed by External Amplifier.

PARAMETER	UNIPOLAR CONFIGURATION	BIPOLAR CONFIGURATION
I_{Bias}	$\frac{I_B \times R_F}{FSR} \times 100$	$\frac{I_B \times R_F}{FSR} \times 100$
V_{os}	$\frac{V_{os}\left(1 + \frac{R_F}{2k\Omega}\right)}{FSR} \times 100$	$\frac{V_{os}\left(1 + \frac{R_F}{1.67k\Omega}\right)}{FSR} \times 100$

FSR = Full scale range (-2.5V to +2.5V is a 5V FSR, etc.). Results are in % of FSR; to get ppm of FSR, multiply by 10^4.
R_F is the value of the feedback resistor.
R_{F1} and R_{F2} are options shown in Figure 6.

Example:
If V_{os} drift and I_{bias} drift of the output amplifier are $10\mu V/°C$ and 0.5nA/°C, respectively, in a D/A converter with -10V to +10V output, the output drift due to these effects would be computed in this manner.

$$V_{OS}: \frac{(10 \times 10^{-6}) \left(1 + \frac{10k\Omega}{1.67k\Omega}\right)}{20} \times 100 = 0.00035\% \text{ of FSR/°C}$$

or 3.5ppm of FSR/°C

$$I_{BIAS}: \frac{0.5 \times 10^{-9} \times (10k\Omega)}{20} \times 100 = 0.00003\% \text{ of FSR/°C}$$

or 0.3ppm of FSR/°C

Total error contribution of amplifier =
3.5 + 0.3 = 3.8ppm of FSR/°C

Effects of input bias current drift may be reduced approximately by a factor of 5 by placing a resistor in series with the positive input lead of the amplifier as shown in Figure 6.

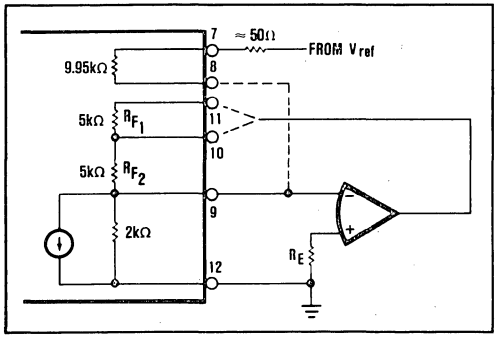


FIGURE 6. Equivalent Output Circuit.

This balances the offset created by bias currents and the error is reduced to the difference in bias currents in the positive and negative inputs. (Substitute I_{offset} in equations in Table III).

The value of this resistor is shown in Table IV for different output ranges.

TABLE IV. R_E Values.

Output Range	±2.5V	±5V	±10V	0 to +5V	0 to +10V
R_E Value	1kΩ	1.25kΩ	1.43kΩ	1.11kΩ	1.43kΩ

Settling time of the DAC10HT is less than 400nsec for an FSR change to within 0.01% of final value. The output amplifier's dynamic characteristics should be compatible with this performance. Burr-Brown's OPA111HT, OPA27HT and OPA37HT are fully specified to operate up to +200°C.

CURRENT OUTPUT OPERATION

DAC10HT can be connected to produce a bipolar voltage output without the use of external components by connecting the internal resistors as shown in Figure 7. Output voltage range of this circuit is limited to approximately the compliance voltage range of ±1V by the 909Ω resistor between pins 9 and 12.

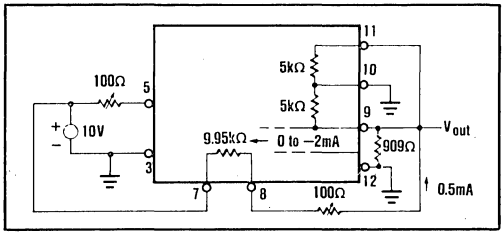


FIGURE 7. Bipolar Current Output Operation Utilizing Internal Resistors.

Gain and offset adjustments are made as described previously except the "+FS" and "-FS" are interchanged and "-FS + 1LSB substituted for +FS -1LSB.

Unipolar and other bipolar ranges may be selected by using an external load resistor as long as the compliance voltage limits, −1V to +1V, are observed.

MULTIPLYING MODE OPERATION

DAC10HT can be used as a two-quadrant multiplying D/A converter by applying the analog signal to be processed through a 100Ω potentiometer to the reference voltage input, pin 5. The analog signal must be between 0 and +10V. The output will be an analog signal equal to the product of the input analog signal and the input digital code. DC error of the output signal is less than 0.05% for a reference voltage range of +1V to +10V. For voltages near zero, the error can be quite large (see Figure 2).

HEAT DISSIPATION

The DAC10HT dissipates approximately 430mW (with +5V and -15V power supplies) and the package has a case-to-ambient thermal resistance (θ_{CA}) of 34°C/W. For optimum performance at +200°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the package can be achieved by using a silicone heat-sink compound.

BURR-BROWN®

DAC63

Ultra-High Speed DIGITAL-TO-ANALOG CONVERTER

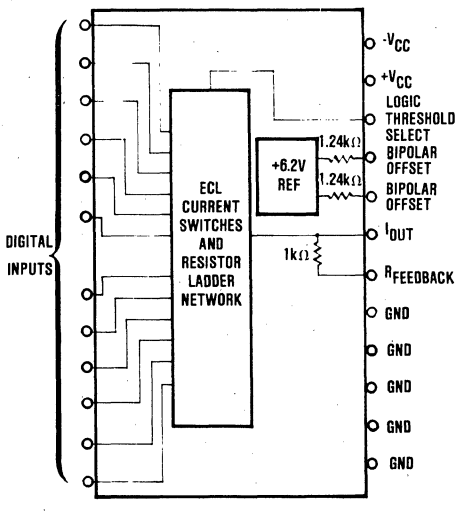
FEATURES

- 12-BIT RESOLUTION AND ACCURACY
- 30nsec SETTLING TIME (MAJOR CARRY)
- ECL-COMPATIBLE INPUTS
- LOW GLITCH ENERGY
- ±30ppm/°C MAX GAIN DRIFT
- LINEARITY ERROR LESS THAN ±1/2LSB OVER SPECIFIED TEMP RANGE
- ADJUSTABLE LOGIC THRESHOLD FOR IDEAL SWITCHING
- INTERNALLY-BYPASSED SUPPLY LINES TO MINIMIZE SETTLING TIME
- INTERNAL FEEDBACK RESISTOR FOR EXCELLENT THERMAL TRACKING
- INDUSTRIAL AND MILITARY GRADES
- HIGH RELIABILITY SCREENING AVAILABLE

DESCRIPTION

The DAC63 is an ultra-fast-settling 12-bit current output D/A converter in a 24-pin dual-in-line package. The inputs are ECL-compatible and the output settles in 30nsec, typ (40nsec, max for C and T grades) to within ±0.012% of Full Scale Range for an MSB change. The DAC63 utilizes a monolithic 12-bit switch chip and a stable thin-film-on-sapphire resistor network to achieve fast settling time and excellent stability over temperature and time. Because of the close thermal tracking of the current-switching transistors (all on one monolithic chip), the possibility of thermal-tail settling time problems are eliminated. An internal applications resistor for use with an external output op amp is included to convert the output current to insure excellent tracking and therefore lower drift. The linearity is guaranteed to be within ±1/2LSB over the specified temperature range of −25°C to +85°C for the CG, CM, BG, and BM grades and −55°C to +125°C for SM and TM grades. Gain drift is ±30ppm/°C max and bipolar offset drift is ±10ppm of FSR/°C max (high grades). Also included internally is a +6.2V reference. An output voltage compliance range of +2.0V to −0.5V allows the generation of an output voltage without using an external output amplifier. The device is available in both metal and ceramic bottom-brazed packages.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

ELECTRICAL

At +25°C and rated supplies unless otherwise specified.

MODEL	DAC63CG/CM/TM			DAC63BG/BM/SM			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT							
DIGITAL INPUT							
Resolution			12			•	Bits
Logic Inputs[1]		ECL-compatible			•		
Logic "1": Voltage	−0.78	−0.90	−0.96	•	•	•	V
Current	6.0		33.0	•		•	μA
Logic "0": Voltage	−1.62	−1.75	−1.85	•	•	•	V
Current		10.0			•		nA
Logic Threshold: Voltage	−1.20	−1.33	−1.40	•	•	•	V
Current			0.25			•	mA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±0.012			•	% of FSR[3]
Differential Linearity Error			±0.012			•	% of FSR
Gain Error[2]		±0.02	±0.1		•	•	%
Offset Error[2]: Unipolar		±0.01	±0.04		•	•	% of FSR
Bipolar		±0.02	±0.1		•	•	% of FSR
Monotonicity Temp. Range (min)							
CG, CM, BG, BM	−25		+85	•		•	°C
TM, SM	−55		+125	•		•	°C
SETTLING TIME (into 150Ω)							
1LSB Change							
Settling to ±0.012% of FSR							
CM/TM, BM/SM		30	40		40	50	nsec
CG, BG		30	40		35	45	nsec
Full Scale Change							
Settling to ±1% of FSR		17			20		nsec
±0.1% of FSR		30			•		nsec
±0.024% of FSR							
CM/TM, BM/SM		55	65		65	75	nsec
CG, BG		35	50		40	55	nsec
±0.012% of FSR							
CM/TM, BM, SM		70			80		nsec
CG, BG		40			•		nsec
Glitch Energy[4]		250			•		LSB/nsec
DRIFT (over specified temp. range)							
Gain		±15	±30		±20	±40	ppm/°C
Offset: Unipolar		±0.3	±0.6		±0.5	±1	ppm/°C
Bipolar			±10			±15	ppm/°C
Linearity Error							
(over specified temp. range)			±0.012			±0.025	% of FSR
Differential Linearity Error							
(over specified temp. range)			±0.025			±0.05	% of FSR
OUTPUT							
ANALOG OUTPUT							
Output Current		0 to −10, ±5			•		mA
Output Voltage Ranges							
with External Op Amp		0 to +10, ±5			•		V
without External Op Amp[5]		0 to +1.5, ±0.5			•		V
Output Impedance without							
External Op Amp							
Unipolar: Positive		150			•		Ω
Negative		200			•		Ω
Bipolar		170			•		Ω
Compliance Voltage	−0.5		+2.0	•		•	V
POWER SUPPLIES AND REFERENCE							
Internal Reference Voltage		+6.2			•		V
Internal Reference Drift		±15			•		ppm/°C
Power Supply Voltages	±13	±15	±18	•	•	•	V
Power Supply Current: +15V		26	31		•	•	mA
−15V		38	46		•	•	mA
Power Supply Sensitivity: +15V		±0.0035			•		%/%ΔV
−15V		±0.0004			•		%/%ΔV
Power Dissipation		960	1160		•	•	mW

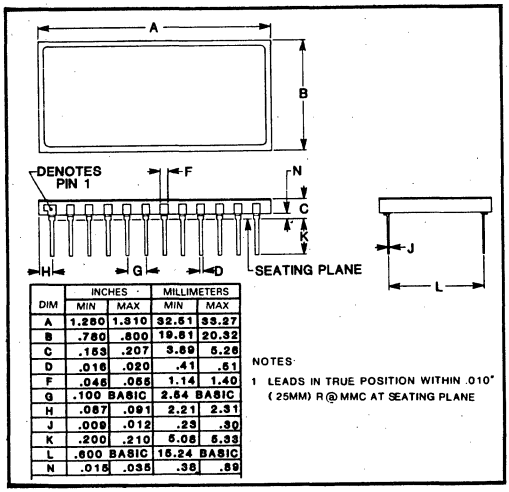
ELECTRICAL (CONT)

MODEL	DAC63CG/CM/TM			DAC63BG/BM/SM			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification: CG, CM, BG, BM	−25		+85	*		*	°C
TM, SM	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C
PACKAGE							
CG, BG	24-pin DIP bottom-brazed ceramic						
CM, TM, BM, SM	24-pin DIP metal						

*Specification same as for DAC63CG/CM/TM.

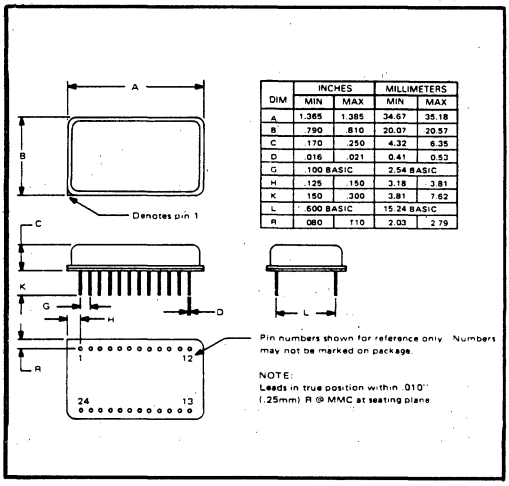
NOTES: (1) Logic Input voltages and currents are dependent on the logic threshold voltage. The logic input values given in each column are correct for the logic threshold voltage given in that column. (2) When used with an external output op amp or when the internal impedances/resistors are used as the load. (3) FSR is Full Scale Range, which is 10mA for both the DAC63BG and DAC63CG. (4) Refer to Output Glitch section. (5) Refer to Figures 8 and 9.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.280	1.310	32.51	33.27
B	.780	.800	19.81	20.32
C	.165	.207	3.89	5.26
D	.016	.020	.41	.51
F	.046	.056	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.067	.091	2.21	2.31
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.600 BASIC		15.24 BASIC	
N	.015	.035	.38	.89

NOTES:
1 LEADS IN TRUE POSITION WITHIN .010" (.25MM) R@MMC AT SEATING PLANE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

PIN ASSIGNMENTS

Pin No.	Function
1	Bit 1 (MSB)
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7
8	Bit 8
9	Bit 9
10	Bit 10
11	Bit 11
12	Bit 12 (LSB)
13	GND
14	GND
15	GND
16	GND
17	GND
18	Feedback Resistor Connection
19	Current Output
20	Bipolar Offset
21	Bipolar Offset
22	Logic Threshold
23	+15VDC
24	-15VDC

DISCUSSION OF SPECIFICATIONS

ACCURACY

Linearity of a D/A converter is one of the true measures of its performance. The linearity error of the DAC63 is specified over its entire temperature range. The analog output will not vary by more than ±1/2LSB from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specified temperature range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for the DAC63 at t_{min}, +25°C, and t_{max}; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications (includes internal reference).

Offset Drift is a measure of the actual change in output around zero over the specified temperature range. The offset is measured at t_{min}, +25°C, and t_{max}. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of the DAC63 is +2.0V and −0.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltage. To insure precision operation, each supply lead should be bypassed to ground as close to the unit as possible with a 1μF CS-type tantalum capacitor.

GROUNDING

Care must be exercised when grounding the DAC63 (pins 13, 14, 15, 16, and 17). In order to preserve the stated linearity and accuracy specifications it is necessary to use the ground pins as the analog ground reference point. Any voltage drop that develops between any of these five pins and the actual ground reference point will degrade the performance of the DAC63. To achieve fast settling performance it is recommended that pins 13 through 17 be returned directly to a ground plane (see Figure 1). The analog ground should be located as close to the DAC63 as possible. Otherwise, the accuracy will be degraded by the voltage drop in the ground lines.

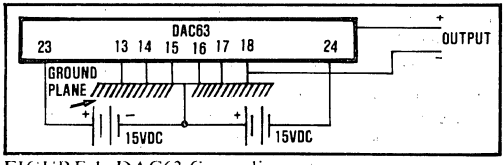


FIGURE 1. DAC63 Grounding.

DIGITAL INTERFACE, LOGIC THRESHOLD, AND NOISE IMMUNITY

The DAC63 is compatible with conventional ECL logic families such as ECL 10,000. The circuit diagram shows that the equivalent circuit of each DAC63 digital input is the base of one side of a differential amplifier. The logic 1 input voltage is −0.85V with a typical input current of 8μA. The logic 0 input voltage is −1.75V with an input current of less than 8nA.

The Logic Threshold function of the DAC63 is very important in dealing with noise in the ECL input-driving circuitry. The ECL 10,000 logic family has a noise immunity of 125mV maximum. It has a temperature coefficient of −1.4mV/°C and a power supply sensitivity of 16mV/%ΔV. With a realistic condition of a 5% power supply variation and a 25°C temperature change, the noise immunity would be degraded to 10mV. In addition, a precision D/A converter is more susceptible to noise than is the ECL logic. Noise at levels acceptable to the logic can couple through the D/A, resulting in an unacceptably noisy output.

Through the logic threshold input, the threshold voltage of the DAC63 is dynamically adjusted as the temperature and power supplies vary to give maximum noise immunity at the analog output over a wide range of conditions.

If an MC10115 line receiver (or similar logic function) is used to drive the DAC63 input, the logic threshold pin can be driven by the V_{BB} output of the ECL gate. Refer to an ECL 10,000 data book for more detail. Figure 2 shows alternate methods for generating the drive signal for logic threshold, pin 22.

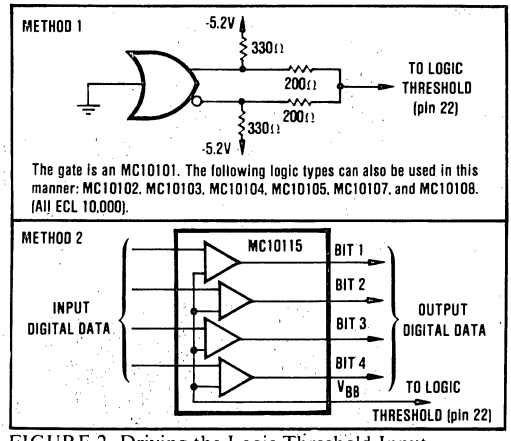


FIGURE 2. Driving the Logic Threshold Input.

SETTLING TIME

Settling time for the DAC63 is the total time required for the output to settle within an error band around its final value after a digital input change. This time includes the digital delay of the internal switches.

The settling time of the DAC63 is determined by digitizing the output waveform produced by toggling the inputs between 011111111111 and 100000000000 continuously and verifying the output settles to within ±1/2LSB in the specified time. The testing technique used is described in detail in Application Note AN-115 which can be obtained from the factory.

Figure 3 shows a typical settling time curve of the DAC63 versus output error. This curve is for full-scale digital code changes. Figure 4 is a photograph showing typical output response characteristics of the DAC63.

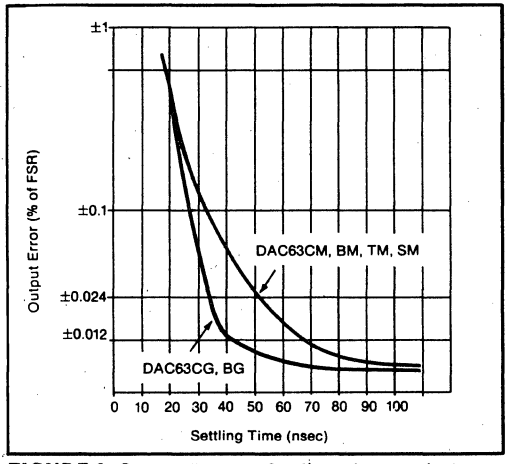


FIGURE 3. Output Error vs Settling Time (typical).

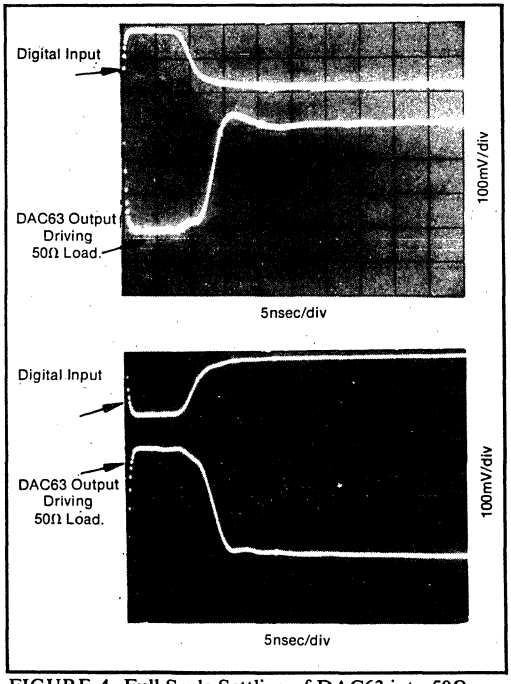


FIGURE 4. Full Scale Settling of DAC63 into 50Ω Load.

In order to achieve minimum settling time it is necessary to observe the following good high frequency construction techniques:

1. The power supplies, including the logic threshold input (pin 22), should be bypassed by 1μF CS-type tantalum capacitors.
2. Use a ground plane to connect common ground points.
3. Remove the ground plane from underneath signal lines where it would add capacitance.
4. Separate analog and digital signal leads to avoid coupling of the digital signal into the analog paths.
5. Bring the source of the digital driving signal as close to the inputs of the DAC63 as possible. If the digital inputs are not clean it will be necessary to reshape them using registers or line drivers. Figure 6 shows how to interface the DAC63 to an input register. It is recommended that the logic power line be bypassed near the digital logic circuitry as a further measure to achieve clean signals.
6. If possible, the DAC63 should be soldered directly into the printed circuit board since connector lead length will cause ringing in the output.

OUTPUT GLITCH

"Glitch" is defined as the difference in the waveforms at the output of the DAC if there is data skew and if there is not. The measurement of glitch is accomplished by measuring the area between these two waveforms.

An output glitch of less than 250LSB-nsec is achievable with the DAC63 because it employs ECL circuitry with current switches that have virtually identical delay times for logic signals making either positive or negative transitions. A glitch results when the digital data changes from one code to the next and the bits do not all switch at the same time. The delay time between the earliest and latest switching bits is called skew time. Typically during the skew time of the digital data, which includes the DAC switching, the digital code is undefined and the DAC output can go to any voltage between the full scale extremes. The glitch creates a noisy output which can be troublesome in some applications such as precision displays and complex waveform generation. Figure 5 is a photograph of a scope trace of the DAC output with a glitch occurring at the major carry transition.

The DAC63 design has been optimized for low glitch energy. However, a further reduction in the output glitch can be achieved by adjusting the skew of the higher order bits of the driving circuitry and by adjusting the logic threshold. This can be done by connecting a variable capacitor from the data lines to ground on each of the first three significant bits (more than three lines may be adjusted if desired). Refer to Figure 6. It will be necessary to create a driving digital code pattern that causes a major carry transition around these bits. It is convenient to use a digital ramp from a counter for this purpose. Initially set the logic threshold exactly half-way between logic 1 and a logic 0. This will be about −1.3V. Then

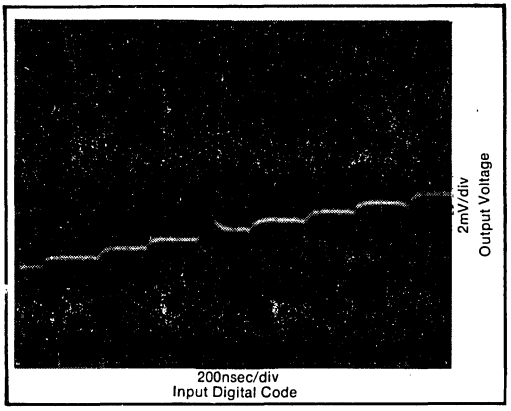


FIGURE 5. Typical Glitch Repsonse of DAC63 at Major Carry Transition with a 1.6V Full Scale Range.

examine the major carry transition associated with bit 3 and adjust the capacitor for minimum glitch. Make the same adjustment to bit 2 and then to bit 1. If done in this order, interactions will be minimized. Finally, fine tune the response by adjusting the logic threshold voltage (pin 22) for minimum glitch. It may be necessary to repeat this procedure once or twice for complete optimization.

OUTPUT CONFIGURATIONS AND APPLICATIONS INFORMATION

The DAC63 contains two 1.24kΩ resistors for generating the bipolar offset current and a 1kΩ resistor which is primarily used as the feedback resistor when used with an external op amp. This thin-film network is constructed on sapphire to provide excellent temperature tracking capability inherent in thin-film networks. These internal resistors along with other internal resistors cause the DAC63 output, in any mode, to be a ratiometric product of the reference. The feedback resistor has very low power sensitivity so that linearity is maintained independent of digital code changes. Because this resistor is constructed on a sapphire network, it is possible to have both superior tracking and low capacitance. Figure 7 shows the DAC63 connected to an external op amp in unipolar and bipolar modes. With the Burr-Brown model OPA600 it is possible to achieve settling times to ±0.01% accuracy in 150nsec. Many of the output accuracy and linearity specifications are given when connected to an external op amp.

For highest speed operation, the DAC63 should be used without an external op amp. Figures 8 and 9 show how to connect the DAC63 for bipolar and positive unipolar

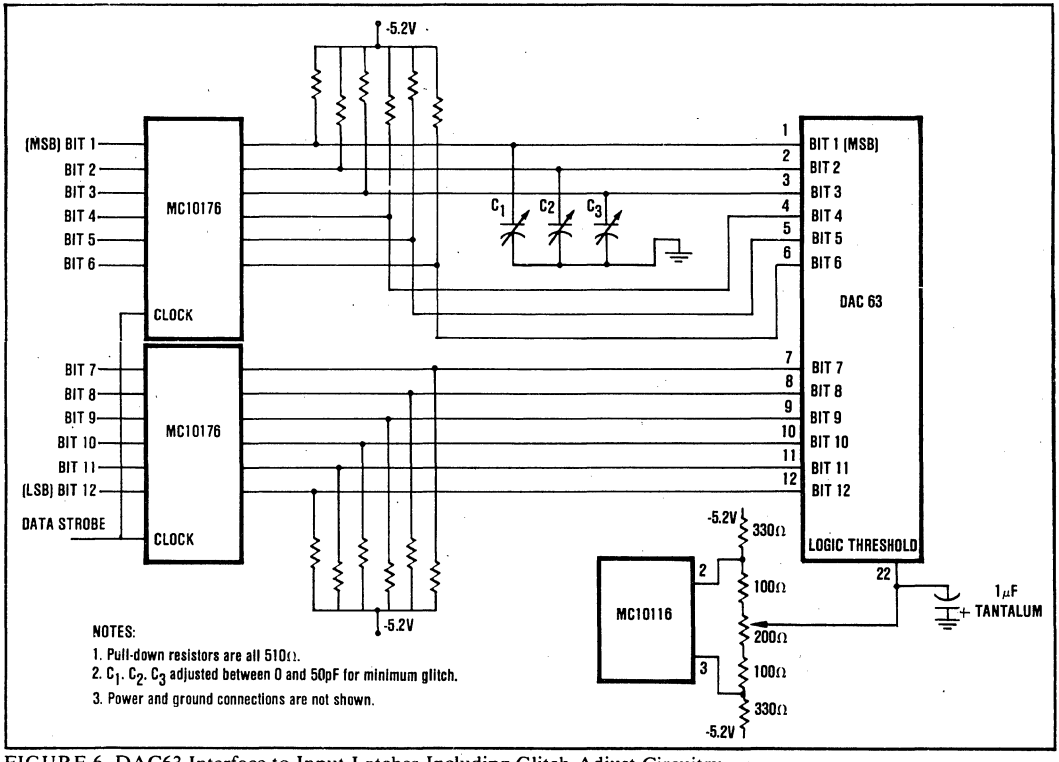
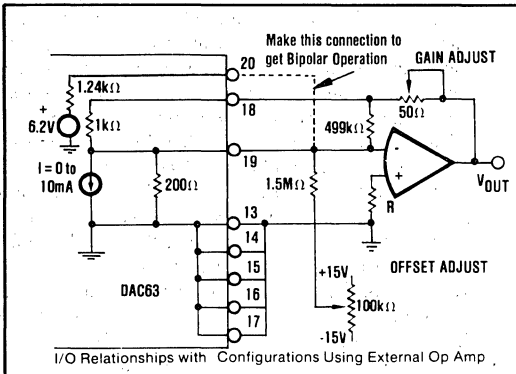


FIGURE 6. DAC63 Interface to Input Latches Including Glitch-Adjust Circuitry.

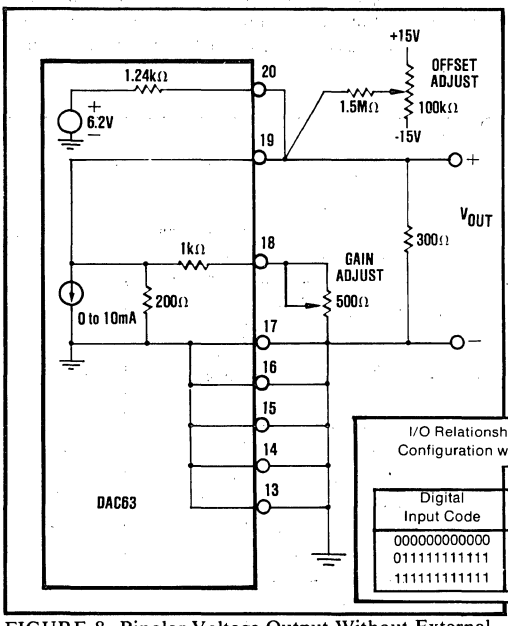
operation. Figure 10 illustrates how to connect the DAC63 to construct a fast A/D converter. The ADC attempts to create a null at the DAC output, so it is possible to clamp the output voltage with a pair of diodes, thereby avoiding the negative compliance limit.



		Unipolar	Bipolar
Digital Codes vs Output Voltage	111111111111	0.0000V	-5.0000V
	011111111111	5.0000V	0.0000V
	000000000000	9.9976V	4.9976V
R Value	R	169Ω	147Ω
Pin 20 Connection		Open	Connect to Pin 19

I/O Relationships with Configurations Using External Op Amp

FIGURE 7. Bipolar and Unipolar Output Connections when Used with External Op Amp.



I/O Relationships for Voltage Output Configuration without External Op Amp

Digital Input Code	Output Voltage Positive Unipolar	Bipolar
000000000000	0.0000V	-0.500V
011111111111	0.7500V	0.000V
111111111111	1.4996V	0.500V

FIGURE 8. Bipolar Voltage Output Without External Op Amp.

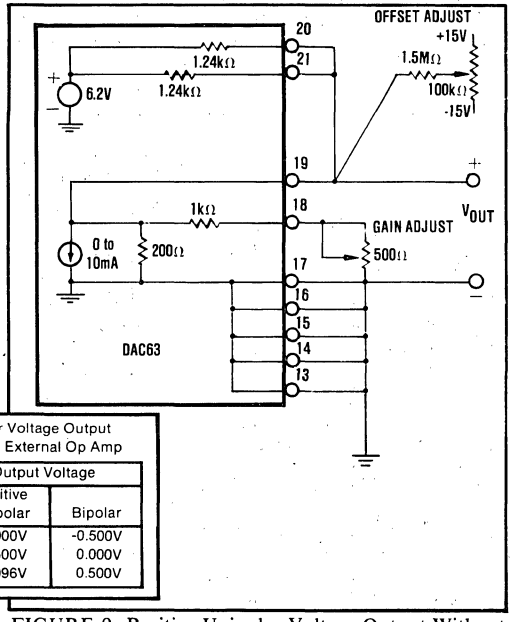


FIGURE 9. Positive Unipolar Voltage Output Without External Op Amp.

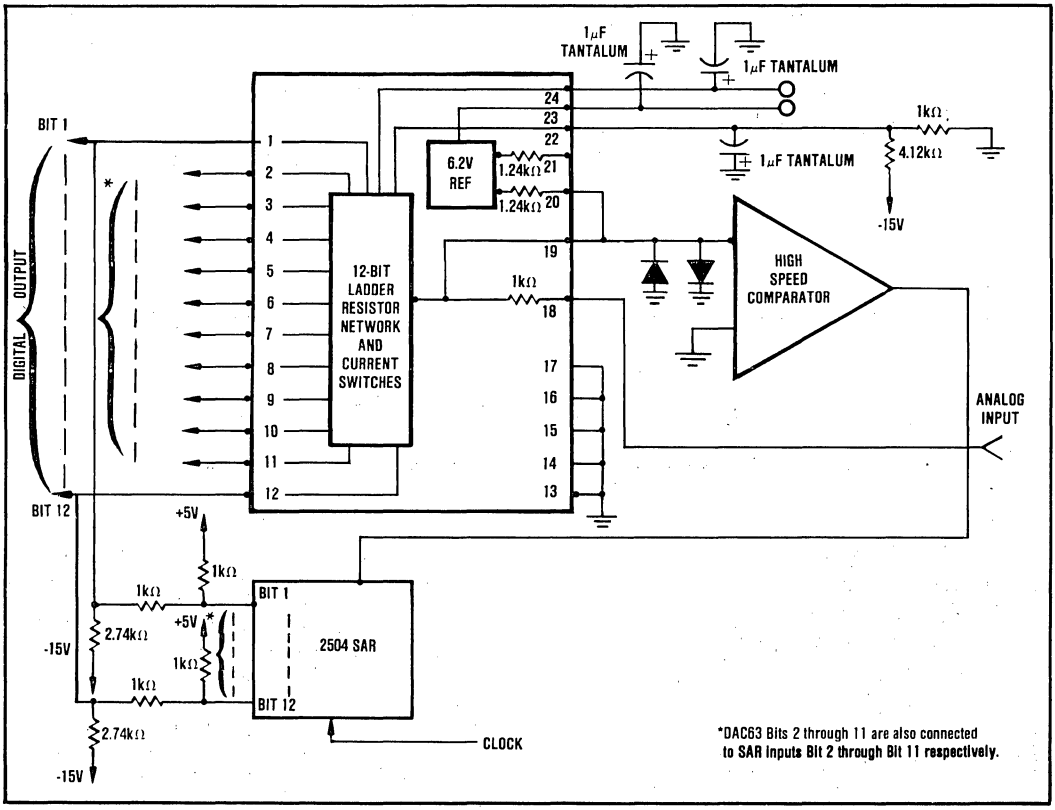


FIGURE 10. DAC63 Used in a Fast A/D Converter.

BURR-BROWN®

DAC70BH
DAC72BH

Monolithic 16-Bit
DIGITAL-TO-ANALOG CONVERTERS

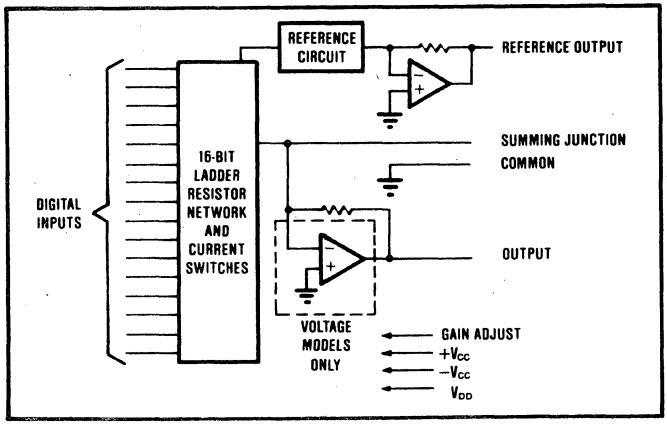
FEATURES

- 16-BIT, 4-DIGIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- LOW DRIFT ±7ppm/°C, (TYPICAL)
- MONOLITHIC CONSTRUCTION
- EXACT DAC70/72 HYBRID REPLACEMENT
- MONOTONIC (AT 14 BITS) OVER FULL SPECIFICATION TEMPERATURE RANGE
- CURRENT AND VOLTAGE MODELS

DESCRIPTION

The DAC70BH/72BH are complete 16-bit digital-to- analog converters that include a precision buried-zener voltage reference and a low-noise, fast-setting output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 14-bit monotonicity over the entire specified temperature range but also a maximum end-point linearity error of ±0.003% of full-scale range. Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C-, 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V, ±10V, 0 to −2mA, and ±1mA are available.

These D/A converters are packaged in hermetic 24-pin ceramic side-brazed packages.



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SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	DAC70BH			DAC72BH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution, CSB, COB			16			•	Bits
Digital Inputs[1]: V_{IH}	+2.4		+5.5	•		•	V
V_{IL}	0		+0.4	•		•	V
I_{IH} V_I = +2.7V			+40			•	µA
I_{IL} V_I = +0.4V			−1.6			•	mA
TRANSFER CHARACTERISTICS							
ACCURACY[2]							
Linearity Error At +25°C			±0.003			•	% of FSR[3]
Gain Error[4]: Voltage					±0.05	±0.15	%
Current			±0.05		±0.05	±0.25	%
Offset Error[4]: Voltage, Unipolar					±0.10	±2	mV
Bipolar						±10	mV
Current, Unipolar			±1			•	µA
Bipolar			±1			±5	µA
Monotonicity Temperature Range (14 bits)	−25		+85	•		•	°C
DRIFT (OVER SPECIFIED TEMPERATURE RANGE)							
Total Bipolar Drift (Includes							
Gain, Offset, and Linearity Drift):[5] Voltage					±5	±11	ppm of FSR/°C
Current		±10			•	±40	ppm of FSR/°C
Total Error Over Temperature Range:							
Voltage, Unipolar						±0.072	% of FSR
Bipolar						±0.072	% of FSR
Current, Unipolar		±0.12				±0.24	% of FSR
Bipolar		±0.12				±0.24	% of FSR
Gain: Voltage					±5	±20	ppm/°C
Current			±7			±47	ppm/°C
Offset: Voltage, Unipolar					±1	±2	ppm of FSR/°C
Bipolar						±8	ppm of FSR/°C
Current, Unipolar		±1				±1	ppm of FSR/°C
Bipolar			±5			±35	ppm of FSR/°C
Differential Linearity over Temperature		±1				±1	ppm of FSR/°C
Linearity over Temperature			±2			±1	ppm of FSR/°C
SETTLING TIME[6]							
Voltage Models (to ±0.003% of FSR)							
Output: 20V Step					5	10	µs
1LSB Step[7]					3	5	µs
Slew Rate					10		V/µs
Switching Transient[8]					500		mV
Current Models (to ±0.003% of FSR)							
Output, 2mA step: 10Ω to 100Ω load		15				1	µs
1kΩ load		50				3	µs
OUTPUT							
ANALOG OUTPUT							
Voltage Models							
Ranges: CSB					0 to +10		V
COB					±10		V
Output Current				±5			mA
Output Impedance (DC)					0.05		Ω
Short Circuit Duration					Indefinite to Common		
Current Models							
Ranges: CSB		0 to −2			•		mA
COB		±1			•		mA
Output Impedance: Unipolar		4.0			•		kΩ
Bipolar		2.45			•		kΩ
Compliance		±2.5			•		V
INTERNAL VOLTAGE REFERENCE	6.0	6.3	6.6	•	•	•	V
Maximum External Current		±200				±200	µA
Temperature Coefficient of Drift		±7			±10		ppm/°C

ELECTRICAL (CONT)

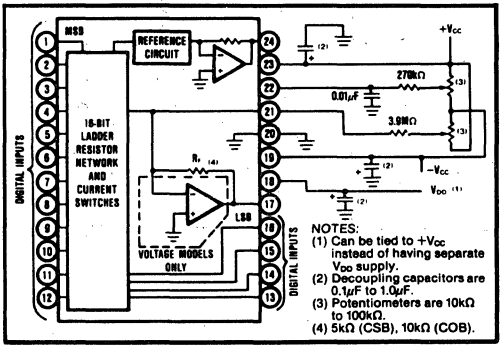
Typical at T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	DAC70BH			DAC72BH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY SENSITIVITY							
Unipolar Offset: ±15VDC		±.0001			*		% of FSR/% V_{CC}
+5VDC		±.0001			*		% of FSR/% V_{DD}
Bipolar Offset: ±15VDC		±.0004			*		% of FSR/% V_{CC}
+5VDC		±.0001			*		% of FSR/% V_{DD}
Gain: ±15VDC		±0.001			*		% of FSR/% V_{CC}
+5VDC		±.0005			*		% of FSR/% V_{DD}
POWER SUPPLY REQUIREMENTS							
Voltage	±14.5, +4.75	±15.0, +5.0	±15.5, +5.25	*	*	*	VDC
Supply Drain: ±15VDC (no load)		±20			*	±30	mA
+5VDC (logic supply)		+5			*	±10	mA
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Storage	−60		+150	*		*	°C

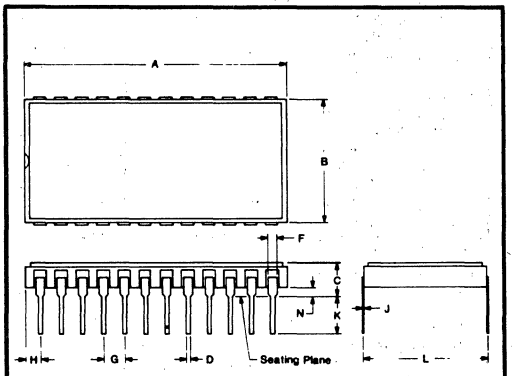
*Specification same as DAC70.

NOTES: (1) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC, and 54/74HTC compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD} = +5V to +15V. (2) Current-output models are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time. (3) FSR means full-scale range and is 20V for the ±10V range (COB-V), 10V for the 0 to +10V range (CSB-V). FSR is 2mA for the ±1mA range (COB-I) and the 0 to −2mA range (CSB-I). (4) Adjustable to zero with external trim potentiometer. (5) With gain and zero errors adjusted to zero at +25°C. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) LSB is for 14-bit resolution. (8) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$.

CONNECTION DIAGRAM



MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.238	1.262	31.45	32.05
B	.585	.602	14.86	15.29
C	.160	.166	4.06	4.98
D	.016	.020	0.41	0.51
F	.038	.042	0.97	1.07
G	.100 BASIC		2.54 BASIC	
H	.067	.085	1.70	2.16
J	.008	.012	0.20	0.30
K	.170 BASIC		4.32 BASIC	
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

PIN ASSIGNMENTS

I Models	Pin No.	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
Bit 12	12	Bit 12
Bit 13	13	Bit 13
Bit 14	14	Bit 14
Bit 15	15	Bit 15
(LSB) Bit 16	16	Bit 16 (LSB)
R_F	17	V_{OUT}
+5VDC	18	+5VDC
-15VDC	19	-15VDC
COMMON	20	COMMON
I_{OUT}	21	SUMMING JUNCTION
GAIN ADJUST	22	GAIN ADJUST
+15VDC	23	+15VDC
6.3V REF. OUT	24	6.3V REF. OUT

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC70BH/72BH accept complementary digital input codes in either binary format (CSB, Unipolar or COB, Bipolar). The COB models may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output		
	Complementary Straight Binary (CSB)	Complementary Offset Binary (COB)	Complementary Two's Complement (CTC)*
0000_H	+ Full Scale	+ Full Scale	−1LSB
$7FFF_H$	+1/2 Full Scale	Bipolar Zero	− Full Scale
8000_H	+1/2 Full Scale −1LSB	−1LSB	+ Full Scale
$FFFF_H$	Zero	− Full Scale	Bipolar Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than −1LSB (−0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC70BH/72BH are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by : (1) testing the end point differences for each D/A at t_{min}, +25°C and t_{max}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Offset Drift

Offset drift is a measure of the change in the output with $FFFF_H$ applied to the digital inputs over the specified temperature range. The maximum change in offset at t_{min} or t_{max} is referenced to the offset error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

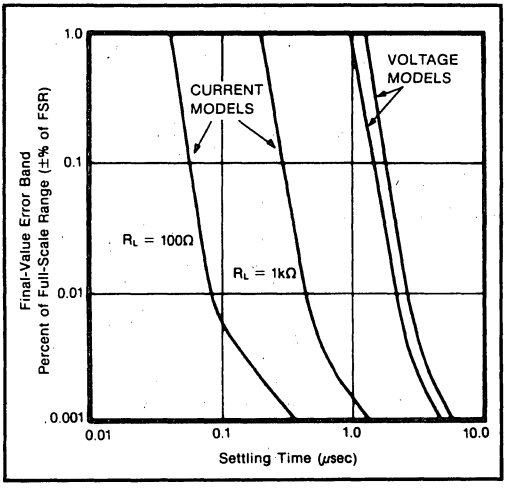


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (COB) or 10V (CSB) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next).

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

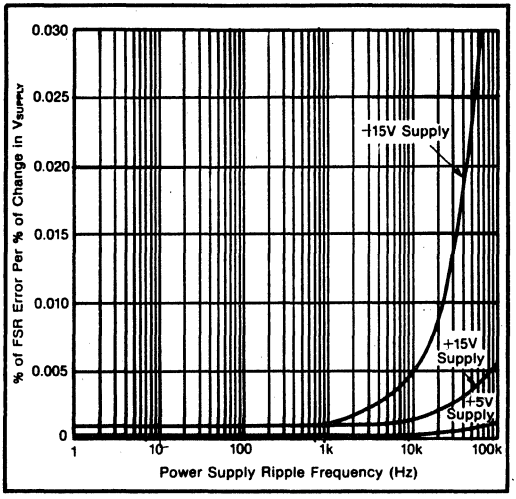


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

REFERENCE SUPPLY

All models have an internal low-noise +6.3V reference voltage derived from an on-chip buried zener diode. This reference voltage is available to the user. A minimum of 200μA is available for external loads. Since the output impedance of the reference output is typically 1Ω, the external load should remain constant.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the Bipolar Offset (connected internally to the reference) from load variations.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF to 10μF tantalum recommended) should be located close to the DAC70BH/72BH. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 510kΩ resistors (20% carbon or better) should be located close to the DAC70BH/72BH to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust (pin 22) to common to prevent noise pickup. Refer to Figures 4 and 5 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

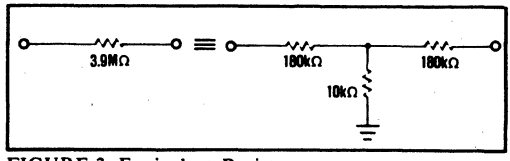


FIGURE 3. Equivalent Resistances.

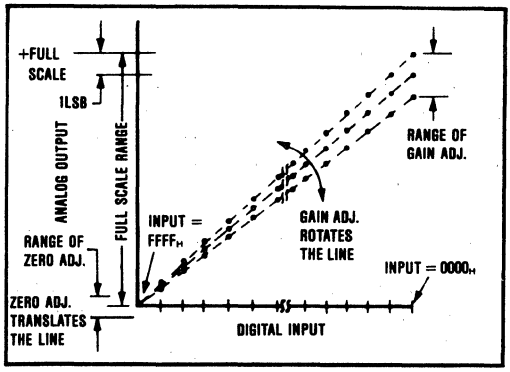


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

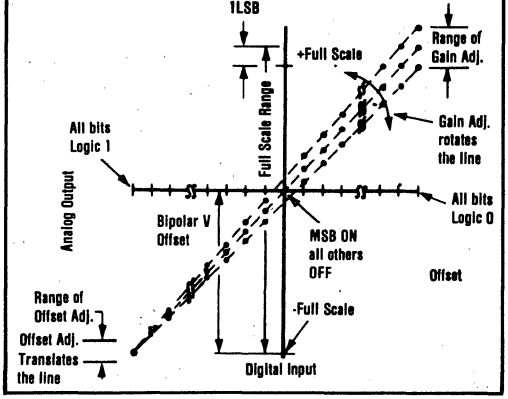


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

TABLE II. Digital Input and Analog Output Relationships.

VOLTAGE OUTPUT MODELS						
	Analog Output					
	Unipolar			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μV)	153	305	610	305	610	1224
0000_H (V)	+9.99985	+9.99969	+9.99939	+9.99969	+9.99939	+9.99878
$FFFF_H$ (V)	0	0	0	−10.0000	−10.0000	−10.0000
CURRENT OUTPUT MODELS						
	Analog Output					
	Unipolar			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μA)	0.031	0.061	0.122	0.031	0.061	0.122
0000_H (mA)	−1.99997	−1.99994	−1.99988	−0.99997	−0.99994	−0.99988
$FFFF_H$ (mA)	0	0	0	+1.00000	+1.00000	+1.00000

OFFSET ADJUSTMENT

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that should produce the maximum negative output voltage. The COB model is internally connected for a 20V FSR range where the maximum negative output voltage is −10V. See Table II for corresponding codes and the Connection Diagram for offset adjustment connections. Offset adjust should be made prior to gain adjust.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiomenter for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 6, 7, and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2, simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DAC70 family because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under

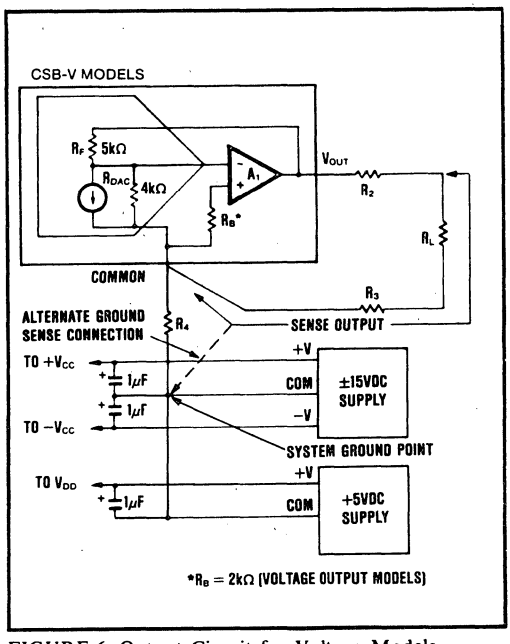
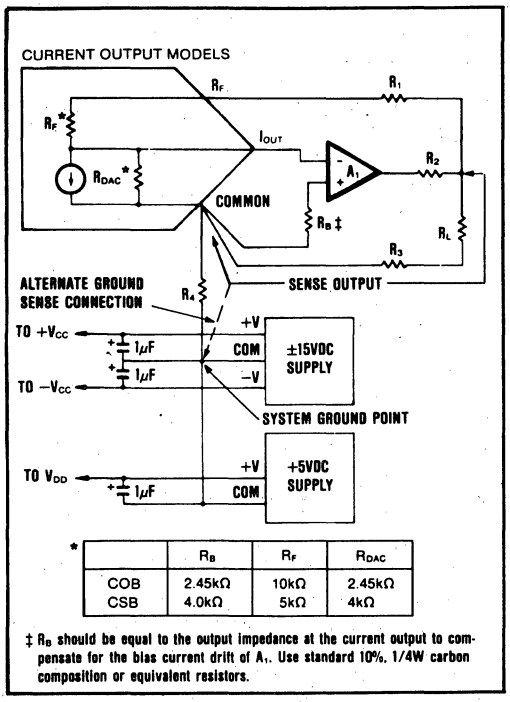


FIGURE 6. Output Circuit for Voltage Models.

$20\mu A$ (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times$ 2mA) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 6, 7, and 8.

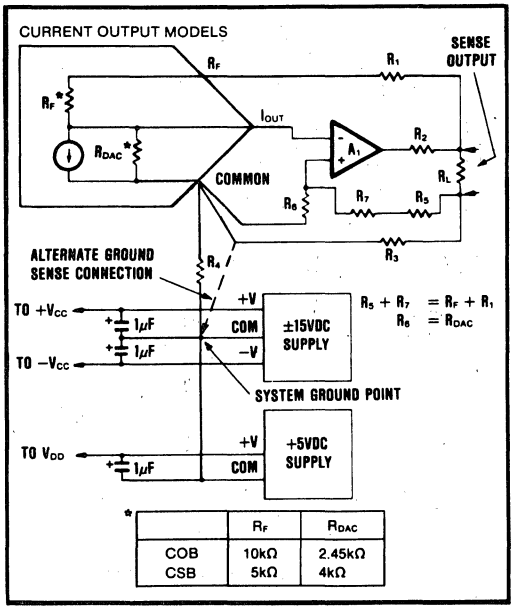


*

	R_B	R_F	R_{DAC}
COB	2.45kΩ	10kΩ	2.45kΩ
CSB	4.0kΩ	5kΩ	4kΩ

‡ R_B should be equal to the output impedance at the current output to compensate for the bias current drift of A_1. Use standard 10%, 1/4W carbon composition or equivalent resistors.

FIGURE 7. Preferred External Op Amp Configuration.



*

	R_F	R_{DAC}
COB	10kΩ	2.45kΩ
CSB	5kΩ	4kΩ

FIGURE 8. Differential Sensing Output Op Amp Configuration.

Figures 7 and 8 show two methods of connecting the current output models with external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

If the output cannot be sensed at Common or the system ground point as mentioned above, the differential output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 7. Again the effect of R_4 is negligible. The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT DACs

The DAC70BH/72BH current output models will drive the summing junction of an op amp to produce an output voltage as shown in Figure 9. Use of the internal feedback resistor is required to obtain specified gain accuracy and low gain drift.

Current output models can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±50ppm/°C. The resistors in the D/A converter ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 10.

OUTPUTS LARGER THAN 20-VOLT RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges (see Figure 11). Use protection diodes as shown when a high voltage op amp is used.

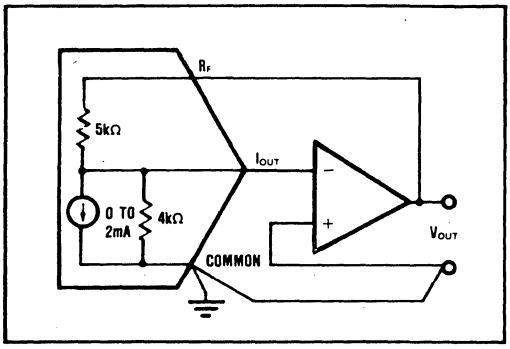


FIGURE 9. External Op Amp Using Internal Feedback Resistors.

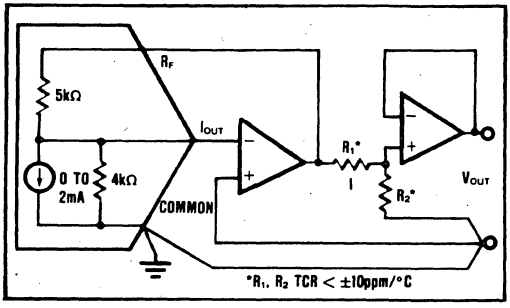


FIGURE 10. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

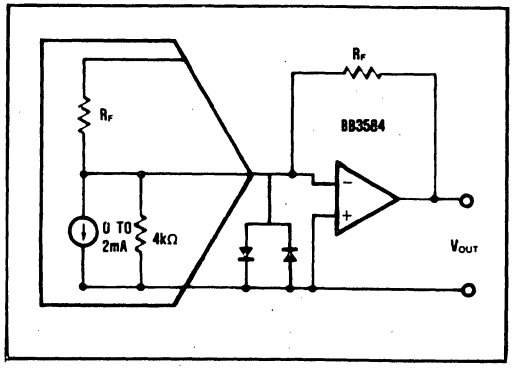


FIGURE 11. External Op Amp Using External Feedback Resistors.

ORDERING INFORMATION

Model		Input Code
Current Output:	DAC70BH-COB-I	Complementary Offset Binary
	BH-CSB-I	Complementary Straight Binary
	DAC72BH-COB-I	Complementary Offset Binary
	BH-CSB-I	Complementary Straight Binary
Voltage Output:	DAC72BH-COB-V	Complementary Offset Binary
	BH-CSB-V	Complementary Straight Binary

BURR-BROWN®

DAC71

Monolithic 16-Bit DIGITAL-TO-ANALOG CONVERTER

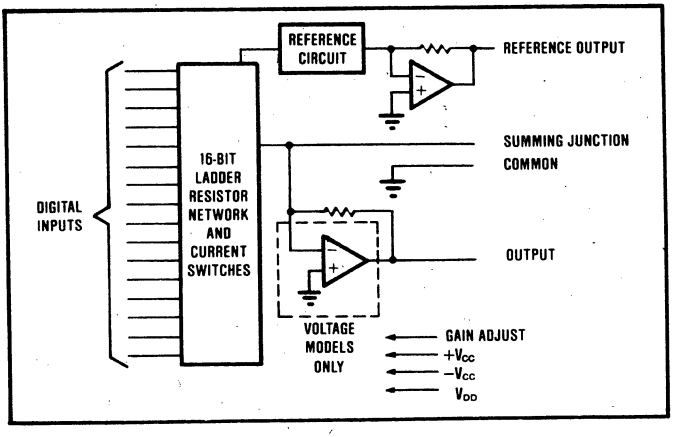
FEATURES

- 16-BIT, 4-DIGIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- LOW DRIFT ±7ppm/°C, (TYPICAL)
- MONOLITHIC CONSTRUCTION
- EXACT DAC71 HYBRID REPLACEMENT
- MONOTONIC (AT 14 BITS) OVER FULL SPECIFICATION TEMPERATURE RANGE
- CURRENT AND VOLTAGE MODELS

DESCRIPTION

The DAC71 is a complete 16-bit digital-to- analog converter that includes a precision buried-zener voltage reference and a low-noise, fast-setting output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 14-bit monotonicity over the entire specified temperature range but also a maximum end-point linearity error of ±0.003% of full-scale range. Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C-, 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V, ±10V, 0 to −2mA, and ±1mA are available.

This D/A converter is packaged in a hermetic 24-pin ceramic side-brazed package.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	DAC71			
	MIN	TYP	MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution, CSB, COB			16	Bits
Digital Inputs[1]:				
V_{IH}	+2.4		+5.5	V
V_{IL}	0		+0.4	V
I_{IH} V_I = +2.7V			+40	µA
I_{IL} V_I = +0.4V			−1.6	mA
TRANSFER CHARACTERISTICS				
ACCURACY[2]				
Linearity Error At +25°C			±0.003	% of FSR[3]
Gain Error[4]: Voltage		±0.01	±0.10	%
Current		±0.05	±0.25	%
Offset Error[4]:				
Voltage Unipolar		±0.10	±2	mV
Voltage Bipolar			±5	mV
Current Unipolar			±1	µA
Current Bipolar			±5	µA
Monotonicity Temperature				
Range (14 bits)	0		+70	°C
DRIFT (OVER SPECIFIED TEMPERATURE RANGE)				
Total Bipolar Drift:				
(Includes Gain, Offset, and Linearity Drift)[5]				
Voltage		±7	±15	ppm of FSR/°C
Current		±15	±50	ppm of FSR/°C
Total Error Over Temperature Range:				
Voltage, Unipolar			±0.083	% of FSR
Voltage, Bipolar			±0.071	% of FSR
Current, Unipolar			±0.23	% of FSR
Current, Bipolar			±0.23	% of FSR
Gain: Voltage			±20	ppm/°C
Current			±60	ppm/°C
Offset: Voltage, Unipolar		±1	±2	ppm of FSR/°C
Voltage, Bipolar			±10	ppm of FSR/°C
Current, Unipolar			±1	ppm of FSR/°C
Current, Bipolar			±40	ppm of FSR/°C
Differential Linearity over Temperature			±2	ppm of FSR/°C
Linearity over Temperature			±2	ppm of FSR/°C
SETTLING TIME[6]				
Voltage Models (to ±0.003% of FSR)				
Output: 20V Step		5	10	µs
1LSB Step[7]		3	5	µs
Slew Rate		10		V/µs
Switching Transient[8]		500		mV
Current Models (to ±0.003% of FSR)				
Output, 2mA step:				
10Ω to 100Ω load			1	µs
1kΩ load			3	µs

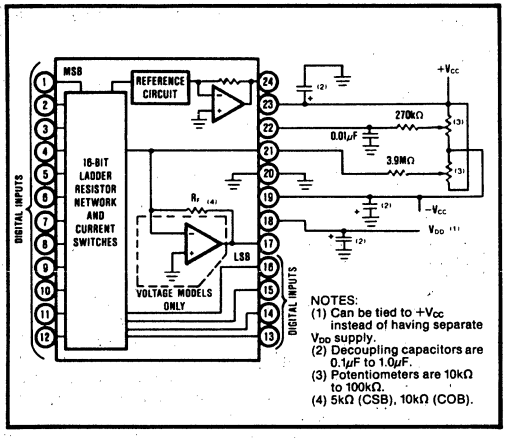
MODEL	DAC71			
	MIN	TYP	MAX	UNITS
OUTPUT				
ANALOG OUTPUT				
Voltage Models				
Ranges: CSB		0 to +10		V
COB		±10		V
Output Current	±5			mA
Output Impedance (DC)		0.05		Ω
Short Circuit Duration		Indefinite to Common		
Current Models				
Ranges: CSB		0 to −2		mA
COB		±1		mA
Output Impedance:				
Unipolar		4.0		kΩ
Bipolar		2.45		kΩ
Compliance		±2.5		V
INTERNAL VOLTAGE REFERENCE	6.0	6.3	6.6	V
Maximum External Current		±200		µA
Temperature Coefficient of Drift		±10		ppm/°C
POWER SUPPLY SENSITIVITY				
Unipolar Offset: ±15VDC		±.0001		% of FSR/% V_{CC}
+5VDC		±.0001		% of FSR/% V_{DD}
Bipolar Offset: ±15VDC		±.0004		% of FSR/% V_{CC}
+5VDC		±.0001		% of FSR/% V_{DD}
Gain: ±15VDC		±0.001		% of FSR/% V_{CC}
+5VDC		±.0005		% of FSR/% V_{DD}
POWER SUPPLY REQUIREMENTS				
Voltage	±14.5, +4.75	±15.0, +5.0	±15.5, +5.25	VDC
Supply Drain:				
±15VDC (no load)		±20	±30	mA
+5VDC (logic supply)		+5	+10	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Storage	−60		+150	°C

NOTES: (1) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC, and 54/74HTC compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD} = +5V to +15V. (2) Current-output models are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time. (3) FSR means full-scale range and is 20V for the ±10V range (COB-V), 10V for the 0 to +10V range (CSB-V). FSR is 2mA for the ±1mA range (COB-I) and the 0 to −2mA range (CSB-I). (4) Adjustable to zero with external trim potentiometer. (5) With gain and zero errors adjusted to zero at +25°C. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) LSB is for 14-bit resolution. (8) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$.

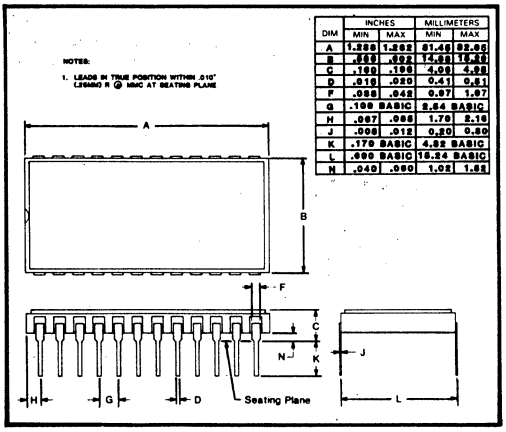
PIN ASSIGNMENTS

I Models	Pin No.	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
Bit 12	12	Bit 12
Bit 13	13	Bit 13
Bit 14	14	Bit 14
Bit 15	15	Bit 15
(LSB) Bit 16	16	Bit 16 (LSB)
R_F	17	V_{OUT}
+5VDC	18	+5VDC
-15VDC	19	-15VDC
COMMON	20	COMMON
I_{OUT}	21	SUMMING JUNCTION
GAIN ADJUST	22	GAIN ADJUST
+15VDC	23	+15VDC
6.3V REF. OUT	24	6.3V REF. OUT

CONNECTION DIAGRAM



MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.580	1.602	81.48	82.06
B	.580	.602	14.68	15.28
C	.160	.180	4.06	4.82
D	.010	.020	0.41	0.51
F	.058	.042	0.97	1.07
G	.100 BASIC		2.54 BASIC	
H	.067	.086	1.70	2.18
J	.008	.012	0.20	0.30
K	.170 BASIC		4.32 BASIC	
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC71 accepts complementary digital input codes in either binary format (CSB, Unipolar or COB, Bipolar). The COB models may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output: Complementary Straight Binary (CSB)	Analog Output: Complementary Offset Binary (COB)	Analog Output: Complementary Two's Complement (CTC)*
0000_H	+ Full Scale	+ Full Scale	−1LSB
$7FFF_H$	±1/2Full Scale	Bipolar Zero	− Full Scale
8000_H	+1/2 Full Scale −1LSB	−1LSB	+ Full Scale
$FFFF_H$	Zero	− Full Scale	Bipolar Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than −1LSB (−0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC71 is specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences for each D/A at t_{MIN}, +25°C and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Offset Drift

Offset drift is a measure of the change in the output with $FFFF_H$ applied to the digital inputs over the specified temperature range. The maximum change in offset at

t_{MIN} or t_{MAX} is referenced to the offset error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

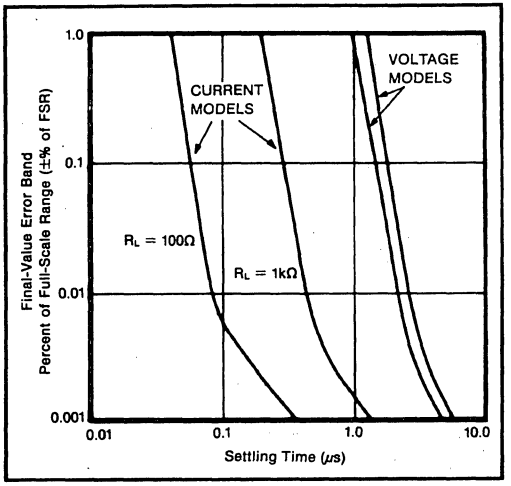


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (COB) or 10V (CSB) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next).

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). I is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

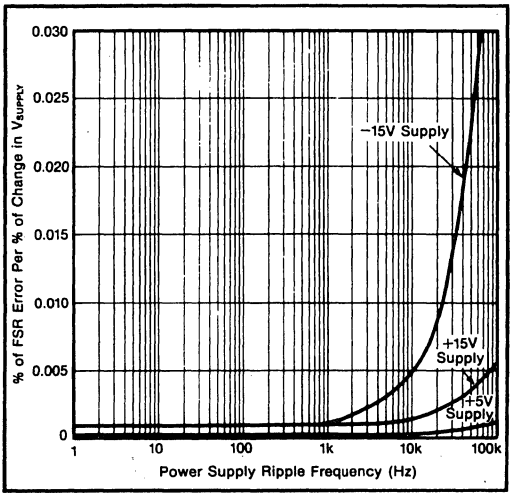


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

REFERENCE SUPPLY

All models have an internal low-noise +6.3V reference voltage derived from an on-chip buried zener diode. This reference voltage is available to the user. A minimum of 200μA is available for external loads. Since the output impedance of the reference output is typically 1Ω, the external load should remain constant.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the Bipolar Offset (connected internally to the reference) from load variations.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF to 10μF tantalum recommended) should be located close to the DAC71. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 510kΩ resistors (20% carbon or better) should be located close to the DAC71 to prevent noise pickup. If it is not convenient to

use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust (pin 22) to common to prevent noise pickup. Refer to Figures 4 and 5 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

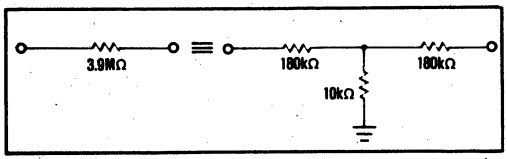


FIGURE 3. Equivalent Resistances.

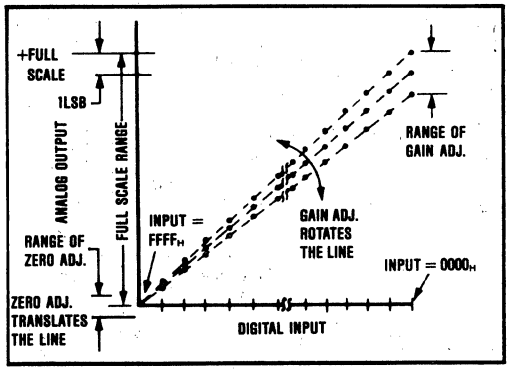


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

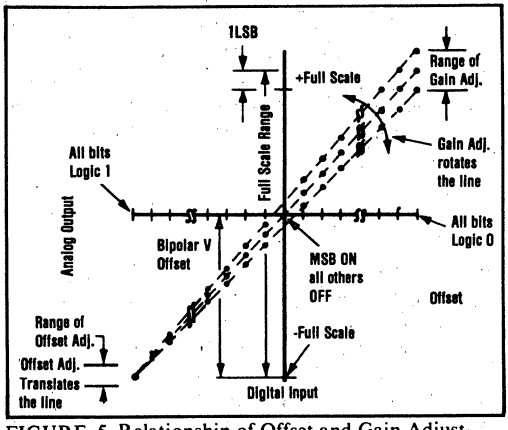


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

OFFSET ADJUSTMENT

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that should produce the maximum negative output voltage. The COB model is internally connected for a 20V FSR range where the maximum negative output voltage is −10V. See Table II for corresponding codes and the Connection Diagram for offset adjustment connections. Offset adjust should be made prior to gain adjust.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiomenter for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment connections.

INSTALLATION CONSIDERATIONS

This D/A converter is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bits 15 and 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a ±10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 6, 7, and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{L\ MIN}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if $R_{L\ MIN}$ is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DAC71 because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times 2mA$) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 6, 7, and 8.

Figures 7 and 8 show two methods of connecting the current output models with external precision output op

TABLE II. Digital Input and Analog Output Relationships.

VOLTAGE OUTPUT MODELS						
	Analog Output					
	Unipolar			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μV)	153	305	610	305	610	1224
0000_H (V)	+9.99985	+9.99969	+9.99939	+9.99969	+9.99939	+9.99878
$FFFF_H$ (V)	0	0	0	−10.0000	−10.0000	−10.0000
CURRENT OUTPUT MODELS						
	Analog Output					
	Unipolar			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μA)	0.031	0.061	0.122	0.031	0.061	0.122
0000_H (mA)	−1.99997	−1.99994	−1.99988	−0.99997	−0.99994	−0.99988
$FFFF_H$ (mA)	0	0	0	+1.00000	+1.00000	+1.00000

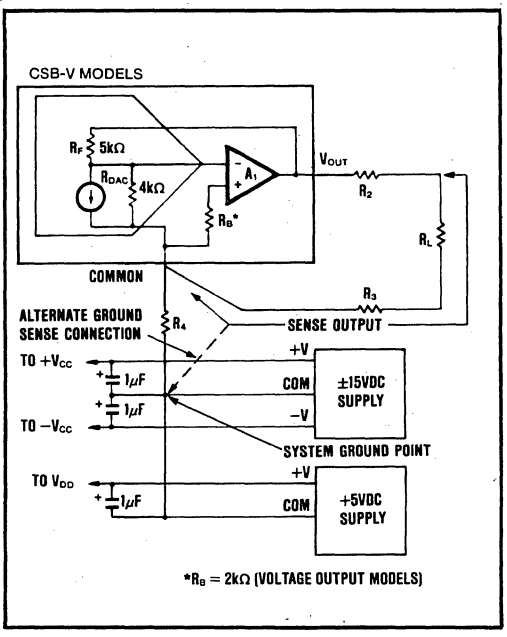


FIGURE 6. Output Circuit for Voltage Models.

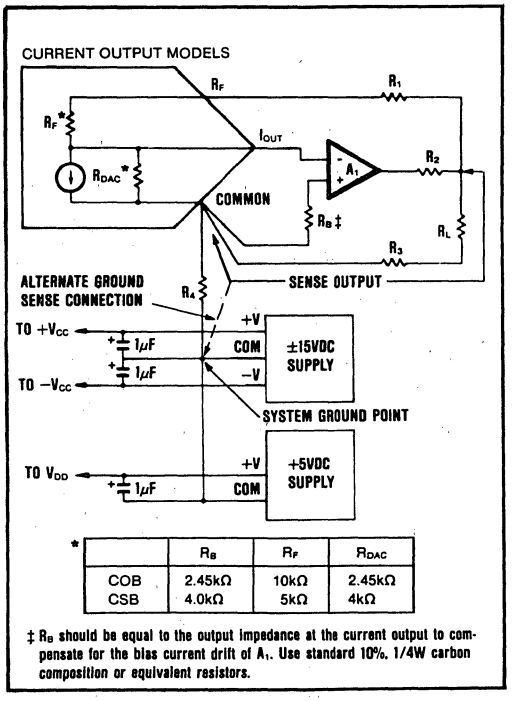


FIGURE 7. Preferred External Op Amp Configuration.

amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

If the output cannot be sensed at Common or the system ground point as mentioned above, the differential output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 7. Again the effect of R_4 is negligible. The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

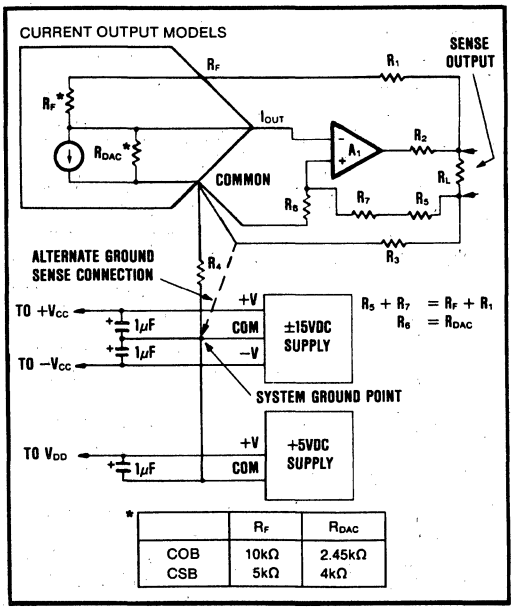


FIGURE 8. Differential Sensing Output Op Amp Configuration.

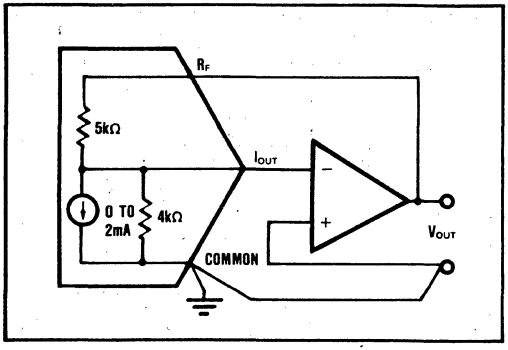


FIGURE 9. External Op Amp Using Internal Feedback Resistors.

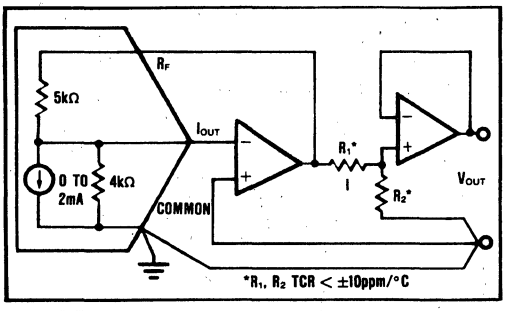


FIGURE 10. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

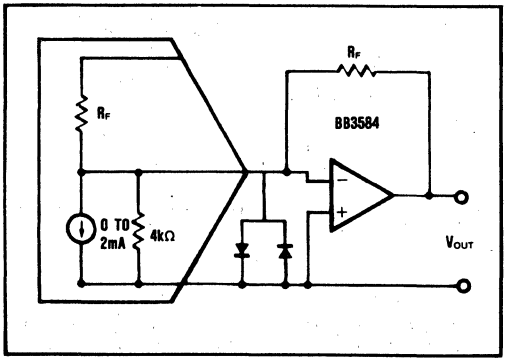


FIGURE 11. External Op Amp Using External Feedback Resistors.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT DACs

The DAC71 current output models will drive the summing junction of an op amp to produce an output voltage as shown in Figure 9. Use of the internal feedback resistor is required to obtain specified gain accuracy and low gain drift.

Current output models can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±50ppm/°C. The resistors in the D/A converter ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 10.

OUTPUTS LARGER THAN 20V RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges (see Figure 11). Use protection diodes as shown when a high voltage op amp is used.

ORDERING INFORMATION

Model	Input Code
Current Output: DAC71-COB-I	Complementary Offset Binary
-CSB-I	Complementary Straight Binary
Voltage Output: DAC71-COB-V	Complementary Offset Binary
-CSB-V	Complementary Straight Binary

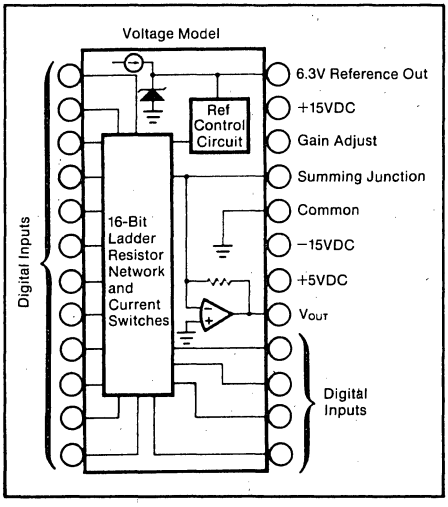
BURR-BROWN®

DAC71-CCD

High Resolution
16-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT, 4-DIGIT RESOLUTION
- ±0.005% MAXIMUM NONLINEARITY
- LOW DRIFT, ±7ppm/°C TYPICAL
- CURRENT AND VOLTAGE MODELS
- LOW COST



DESCRIPTION

The DAC71 is a high quality 16-bit hybrid IC D/A converter available in a 24-pin dual-in-line ceramic package.

The DAC71 with internal reference and optional output amplifier offers a maximum linearity error of ±0.005% of FSR at room temperature and a maximum gain drift of ±20ppm/°C over a temperature range of 0°C to +70°C.

The DAC71-CCD accepts complementary 4-digit BCD TTL-compatible input codes.

Packaged within the DAC71 are fast-settling switches and stable laser-trimmed thin-film resistors that let you select two output ranges: 0 to +10VDC (DAC71-CCD-V) and 0 to −1.25mA (DAC71-CCD-I).

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

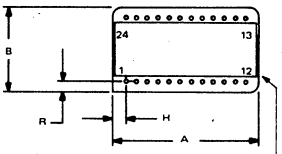
Typical at T_A = 25°C and rated power supplies unless otherwise noted.

MODEL	DAC71-CCD			
	MIN	TYP	MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution		4		Digits
Logic Levels (TTL-Compatible)[1]:				
Logical "1" (at +40μA)	+2.4		+5.5	VDC
Logical "0" (at −1.6mA)	0		+0.4	VDC
TRANSFER CHARACTERISTICS				
ACCURACY				
Linearity Error at 25°C			±0.005	% of FSR[2]
Gain Error[3]: Voltage		±0.01	±0.1	%
Current		±0.05	±0.25	%
Offset Error[3]: Voltage, Unipolar		±0.1	±2	mV
Current, Unipolar			±1	μA
Monotonicity, Temperature Range (14 bits)	0		+50	°C
DRIFT (Over specified temp. range)				
Total Error over Temperature Range[4]:				
Voltage, Unipolar			±0.063	% of FSR
Current, Unipolar			±0.23	% of FSR
Gain: Voltage			±20	ppm/°C
Current			±60	ppm/°C
Offset: Voltage, Unipolar		±1	±2	ppm of FSR/°C
Current, Unipolar			±1	ppm of FSR/°C
Differential Linearity over Temperature			±2	ppm of FSR/°C
Linearity Error over Temperature			±2	ppm of FSR/°C
SETTLING TIME				
Voltage Model (to ±0.005% of FSR)				
Output: 20V Step		5	10	μs
1LSB Step[5]		3	5	μs
Slew Rate		20		V/μs
Current Model (to ±0.005% of FSR)				
Output: 2mA step, 10Ω to 100Ω Load			1	μs
1kΩ Load			3	μs
Switching Transient		500		mV
OUTPUT				
ANALOG OUTPUT				
Voltage Model				
Range		0 to +10		V
Output Current	±5			mA
Output Impedance (DC)		0.05		Ω
Short-Circuit Duration		Indefinite to Common		
Current Model				
Range		0 to −1.25		mA
Output Impedance, Unipolar		15		kΩ
Compliance		±2.5		V
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	V
Maximum External Current[6]			±200	μA
Temperature Coefficient of Drift			±10	ppm/°C
POWER SUPPLY SENSITIVITY				
Unipolar Offset: ±15VDC		±0.001		% of FSR/%V_S
+15VDC		±0.001		% of FSR/%V_S
Gain: ±15VDC		±0.001		% of FSR/%V_S
+5VDC		±0.0005		% of FSR/%V_S
POWER SUPPLY REQUIREMENTS				
Voltage	±14.5, +4.75	±15, +5	±15.5, +5.25	VDC
Supply Drain: ±15VDC (no load)		±25	±35	mA
+5VDC (logic supply)		±20	±35	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating (double above Drift Specs)	−25		+85	°C
Storage	−55		+100	°C

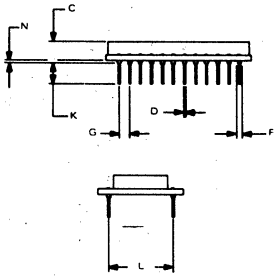
*NOTES: (1) Adding external CMOS hex buffers CD4009A will provide 15VDC CMOS input compatibility. The percent change in output ΔV_o as logic 0 varies from 0.0V to +0.4V and logic 1 changes from +2.4V to +5.0V on all inputs is less than 0.006% of FSR. (2) FSR means Full Scale Range and is 20V for ±10V range, 10V for ±5V range, etc. (3) Adjustable to zero with external trim potentiometer. (4) With gain and offset errors adjusted to zero at 25°C. (5) LSB is for 14-bit resolution. (6) Maximum with no degradation of specifications.

MECHANICAL

NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.



Pin numbers shown for reference only. Numbers may not be marked on package.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	0.85	.105	2.16	2.67

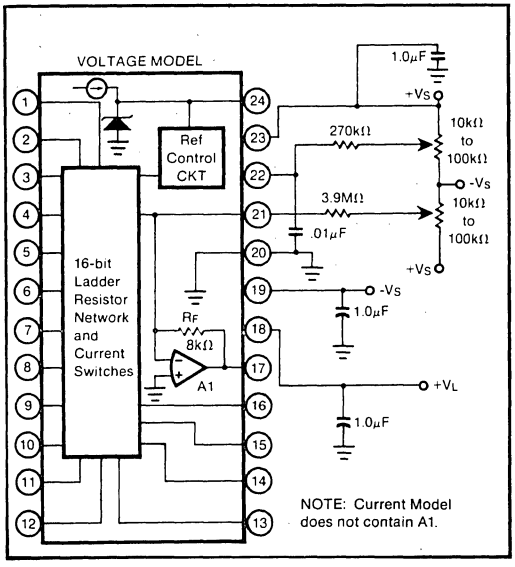
CASE: Ceramic

MATING CONNECTOR: 245MC

WEIGHT: 8.4 grams (0.3 oz.)

HERMETICITY: Conforms to method 1014, condition C, step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

CONNECTION DIAGRAM



PIN ASSIGNMENTS

I Model	Pin	V Model
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
Bit 12	12	Bit 12
Bit 13	13	Bit 13
Bit 14	14	Bit 14
Bit 15	15	Bit 15
(LSB) Bit 16	16	Bit 16 (LSB)
RF	17	VOUT
+5VDC	18	+5VDC
-15VDC	19	-15VDC
COMMON	20	COMMON
IOUT	21	SUMMING JUNCTION
GAIN ADJUST	22	GAIN ADJUST
+15VDC	23	+15VDC
6.3V REF. OUT	24	6.3V REF OUT

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC71 accepts comlementary digital input codes in decimal (CCD) format (see Table I).

TABLE I. Digital Input Codes.

CCD MODELS	DIGITAL INPUT CODES		
	CCD Complementary Coded Decimal 4 Digits		*Invert the MSB of the COB code with an external inverter to obtain CTC code.
F S bits ON 0110 0110 All Bits OFF 1111 1111	*Full Scale Zero		

ACCURACY

Linearity

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.005% max (CCD) from a straight line drawn through the end points (all bits ON and all bits OFF) at +25°C.

Differential Linearity

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can be anywhere from 1/2LSB to 3/2LSB when the input changes from one adjacent input stage to the next.

Monotonicity

Monotonicity over 0°C to +50°C is guaranteed. This insures that the analog output will increase or remain the same for increasing 14-bit input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (see Figure 1). Gain Drift is established by:

1. testing the end point differences for each DAC71 model at +25°C and the appropriate specification temperature extremes;

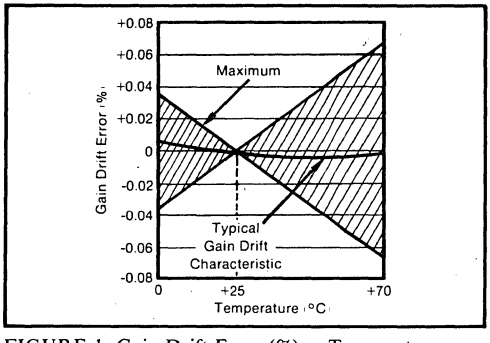


FIGURE 1. Gain Drift Error (%) vs Temperature.

2. calculating the gain error with respect to the +25°C value; and
3. dividing by the temperature change. This is expressed in ppm/°C.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range.

The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 2).

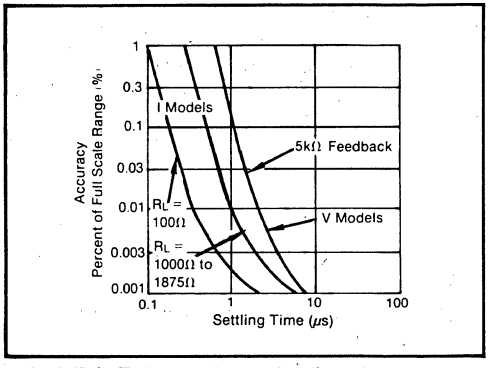


FIGURE 2. Full Scale Range Settling Time vs Accuracy.

Voltage Output Models

Settling times are specified to ±0.005% of FSR; one for maximum full scale range changes of 20V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111 . . . 11 to 1000 . . . 00), the point at which the worst-case settling time occurs.

Current Output Models

Two settling times are specified to ±0.005% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the output of the current models while maintaining specified accuracy. The typical compliance voltage of all current output models is +2.5V and maximum safe voltage swing permitted without damage is +5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 3).

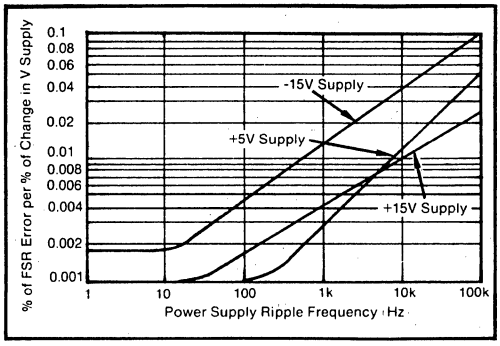


FIGURE 3. Power Supply Rejection vs Power Supply Ripple Frequency.

REFERENCE SUPPLY

All DAC71 models are supplied with an internal +6.3V reference voltage supply. This reference voltage (pin 24) has a tolerance of ±5% and is connected internally for specified operation. The zener is selected for a Gain Drift of typically ±3ppm/°C and is burned-in for a total of 168 hours for guaranteed reliability. This reference may also be used externally but the current drain is limited to 200μA. An external buffer amplifier is recommended if the DAC71 internal reference is used externally in order to provide a constant load to the reference supply output.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC71. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (20% carbon or better) should be located close to the DAC71 to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic

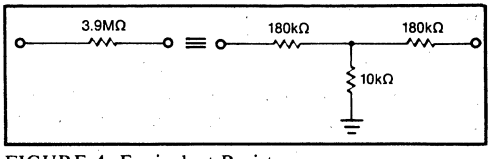


FIGURE 4. Equivalent Resistances.

capacitor should be connected from Gain Adjust (pin 22) to common to prevent noise pickup. Refer to Figure 5 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

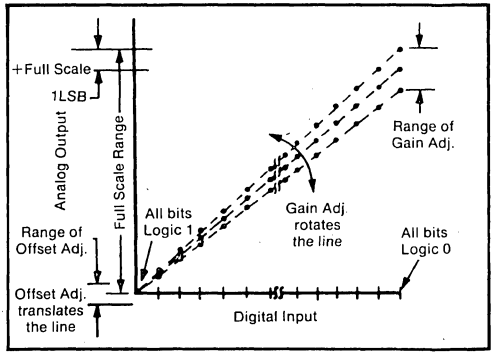


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

Offset Adjustment

For unipolar configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

See Table II for corresponding codes and the Connection Diagram for offset adjustment connections. Offset adjust should be made prior to gain adjust.

TABLE II. Digital Input and Analog Output Relationships.

DIGITAL INPUT CODE	OUTPUT CODE			
	VOLTAGE		CURRENT	
	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Binary Coded Decimal CCD 0 to +10V or 0 to -1 25mA	4-Digit Resolution	N A	4-Digit Resolution	N A
One LSB	+1 0mV		0 125μA	
Full Scale 0110 0110	+9 999V		-1 24987mA	
All Bits OFF 1111 1111	Zero		Zero	

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment connections.

INSTALLATION CONSIDERATIONS

Figure 6 shows the connection diagram for a voltage output DAC71. Lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L) is constant. R_2 simply introduces a gain error that can be removed during initial calibration. R_3 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is $5k\Omega$, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the DAC71 for optimum performance.

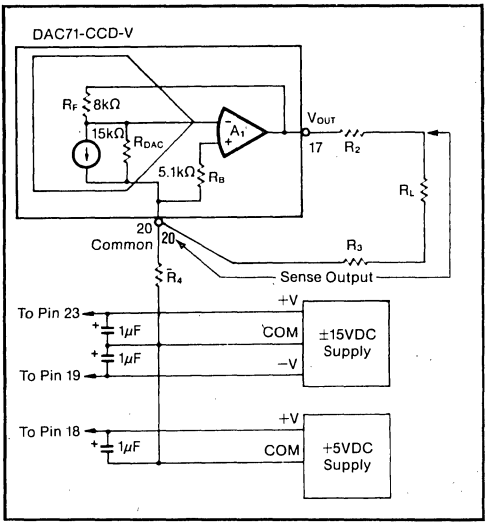


FIGURE 6. Output Circuit for Voltage Models.

Figures 7 and 8 show two methods of connecting current model DAC71s with the external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_1) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated during initial calibration. The effect of R_2 is negligible because it is inside the feedback loop of the

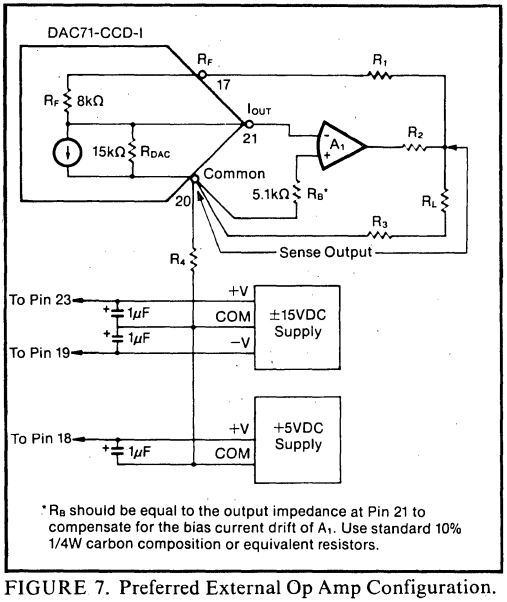


FIGURE 7. Preferred External Op Amp Configuration.

output op amp and is therefore greatly reduced by the loop gain. If the output cannot be sensed at Common (pin 20), then the differental output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the DAC common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_1. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 8 because $R_8 = (R_7 + R_5) \parallel R_6$. In all three circuits the effect of R_4 is negligible.

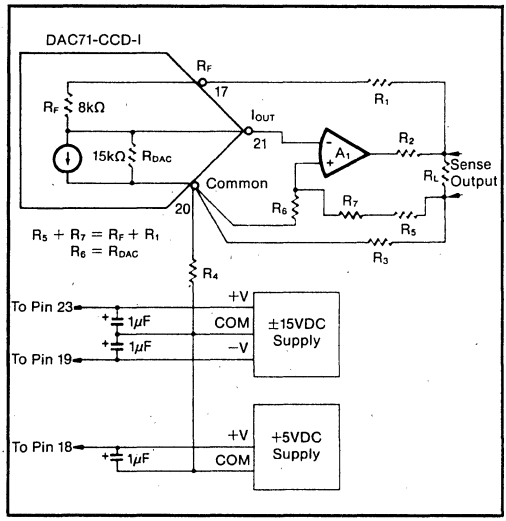


FIGURE 8. Differential Sensing Output Op Amp Configuration.

The DAC71 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

NOTE: It is recommended that the digital input lines of the DAC71 be driven from inverters or buffers of TTL input registers to obtain specified accuracy.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT DAC

The DAC71-CCD-I is a current output device and will drive the summing junction of an op amp to produce an output voltage (see Figure 9). The op amp output voltage is:

$$V_{OUT} = -I_{OUT} R_F$$

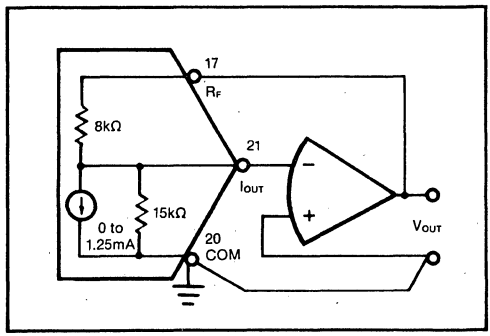


FIGURE 9. External Op Amp Using Internal Feedback Resistors.

where I_{OUT} is the DAC71 output current and R_F is the feedback resistor. Use of the internal feedback resistor (pin 17) is required to obtain specified gain accuracy and low gain drift.

The DAC71 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±25ppm/°C. The resistors in the DAC71 are chosen for ratio tracking of ±1ppm/°C and not absolute TCR (which may be as high at ±25ppm/°C).

An alternative method of scaling the output voltage of the DAC71 and preserving the low gain drift is shown in Figure 10.

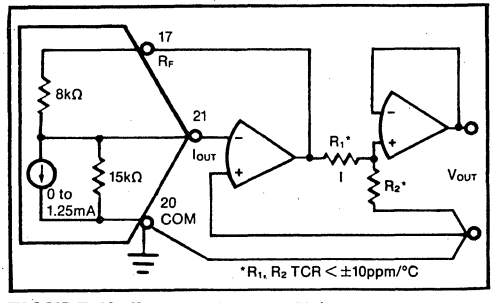


FIGURE 10. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

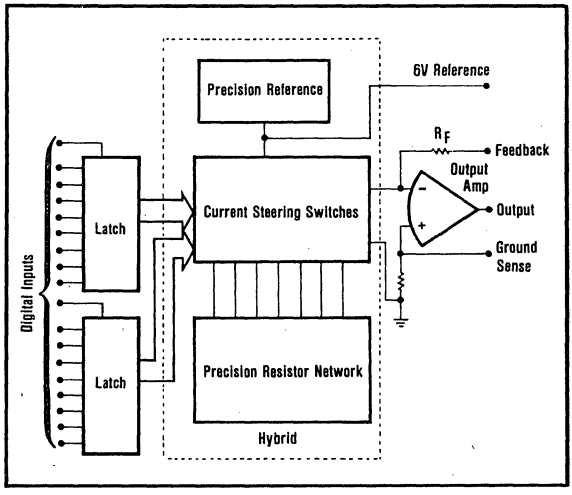
BURR-BROWN®

DAC73
DAC736

High Resolution 16-Bit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT RESOLUTION
- ±1/2LSB MAXIMUM NONLINEARITY
- LOW DRIFT
- CURRENT OR VOLTAGE OUTPUT
- INTERNAL GAIN, OFFSET, AND LINEARITY ADJUSTMENT
- LATCHED INPUTS (DAC73)
- LOW COST



DESCRIPTION

The DAC73 is a 16-bit modular high performance digital-to-analog converter in a 2" x 4" x 0.4" (50.8mm x 101.6mm x 10.2mm) package. The low drift and ultra-high linearity of the DAC73 provide voltage or current output signals that are accurate to ±0.00075% of full scale input range at 25°C ambient.

The critical components including the current steering switches, the temperature-compensated zener reference, and the precision laser-trimmed bit resistor network are contained in a single ceramic hybrid package.

The feedback and reference resistors are laid out for maximum stability with low current density and ±10ppm/°C maximum temperature coefficient with ±1ppm °C tracking. This insures very-low superposition errors and low temperature coefficient of gain.

The inputs are TTL-compatible CMOS and contain level triggered latches in an 8-bit format for microprocessor data bus compatibility. No external components are required to achieve full 16-bit accuracy. Gain and offset potentiometers are also included in the DAC73.

The DAC736 has electrical specifications identical to the DAC73, but it is pin-compatible with the AD1136. The input latches, bit adjust pins, ground sense pin, and internal offset adjust pot are not included.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	DAC73J/DAC736J MIN	DAC73J/DAC736J TYP	DAC73J/DAC736J MAX	DAC73K/DAC736K MIN	DAC73K/DAC736K TYP	DAC73K/DAC736K MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution - CSB, COB			16			16	Bits
Logic Levels (TTL-Compatible CMOS)							
Logical "1" (at +1.0μA)	+3.5		+5.5	+3.5		+5.5	VDC
Logical "0" (at -0.5mA)	-0.5		+1.5	-0.5		+1.5	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error at 25°C			±0.0015			±0.00075	% of FSR(1)
Gain Error,(2) Voltage CSB		±0.005	±0.02		±0.005	±0.02	%
COB		±0.01	±0.05		±0.01	±0.05	%
Current		±0.05	±0.25		±0.05	±0.25	%
Offset Error,(2) Voltage, Unipolar			±0.8			±0.8	mV
Bipolar			±10			±10	mV
Current, Unipolar			±1			±1	μA
Bipolar			±5			±5	μA
Monotonicity Temp. Range 16 Bits for K, 15 Bits for J		±15		+5		+35	°C
DRIFT (Over specified temp. range)							
Total Drift (includes gain, offset, and linearity drift)							
CSB		±9.5	±24		±9.5	±24	ppm of FSR/°C
COB		±9	±22		±9	±22	ppm of FSR/°C
Total Error over Temp. Range(3)							
Voltage, Unipolar 0°C to 70°C		±0.043	±0.108		±0.043	±0.108	% of FSR
Bipolar		±0.040	±0.099		±0.040	±0.099	% of FSR
Voltage, Unipolar 15°C to 35°C		±0.010	±0.024		±0.010	±0.024	% of FSR
Bipolar		±0.009	±0.022		±0.009	±0.022	% of FSR
Gain (Exclusive of reference drift		±4	±10		±4	±10	ppm/°C
Offset (Exclusive of reference drift)							
Unipolar		±0.5	±2		±0.5	±2	ppm of FSR/°C
Bipolar		±2	±5		±2	±5	ppm of FSR/°C
Differential Linearity over Temperature		±1	±2		±1	±2	ppm of FSR/°C
Linearity Error over Temperature		±1	±2		±1	±2	ppm of FSR/°C
SETTLING TIME							
Voltage (to ±0.00075% of FSR)							
Output: 20V Step			50			50	μsec
1LSB Step(4)		6	10		6	10	μsec
Slew Rate		18			18		V/μsec
Current (to ±0.00075% of FSR)							
Output: 2mA Step		6			6		μsec
COB Switching Transient Magnitude		600			600		mV
COB Switching Transient Energy		0.45			0.45		V-μsec
OUTPUT							
ANALOG OUTPUT							
Voltage Output							
Ranges - CSB		0 to +5			0 to +5		V
		0 to +10			0 to +10		V
COB		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Output Current - Unipolar			+4			+4	mA
Bipolar			±2			±2	mA
Output Impedance (DC)		0.03	0.05		0.03	0.05	Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
Current Output							
Ranges - CSB		0 to -2			0 to -2		mA
COB		±1			±1		mA
Output Impedance - Unipolar		15			15		kΩ
Bipolar		4.4			4.4		kΩ
Compliance		-1.5 to +10			-1.5 to +10		V
INTERNAL REFERENCE VOLTAGE	5.990	6.000	6.010	5.990	6.000	6.010	V
Maximum External Current(5)			+4			+4	mA
Temp. Coeff.		±4	±10		±4	±10	ppm/°C
OUTPUT NOISE							
Current, COB							
0.1Hz to 10Hz		1			1		nA, p-p
10Hz to 100kHz		4			4		nA, rms
Voltage, COB, ±10V Range							
0.1Hz to 10Hz		10			10		μV, p-p
10Hz to 100kHz		70			70		μV, rms

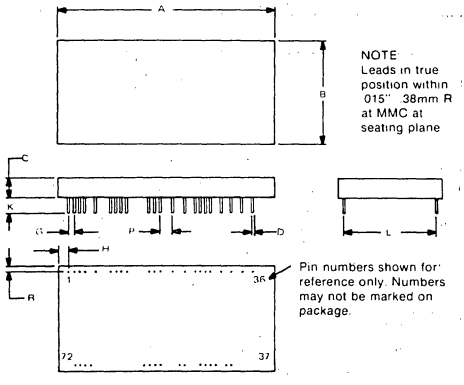
ELECTRICAL (CONT)

MODEL	DAC73J/DAC736J MIN	DAC73J/DAC736J TYP	DAC73J/DAC736J MAX	DAC73K/DAC736K MIN	DAC73K/DAC736K TYP	DAC73K/DAC736K MAX	UNITS
STABILITY, LONG TERM							
Gain (Exclusive of reference)		±30			±30		ppm/10³hr
Offset COB (Exclusive of reference)		±30			±30		ppm of FSR/ 10³hr
CSB		±5			±5		ppm of FSR/ 10³hr
Linearity		±0.25			±0.25		LSB/10³hr
Reference		±10			±10	±20	ppm/10³hr
POWER SUPPLY SENSITIVITY							
Unipolar Offset							
±15VDC		±0.0001			±0.0001		% of FSR/% V_S
+5VDC		±0.0001			±0.0001		% of FSR/% V_S
Bipolar Offset							
±15VDC		±0.0004			±0.0004		% of FSR/% V_S
+5VDC		±0.0001			±0.0001		% of FSR/% V_S
Gain							
±15VDC		±0.001			±0.001		% of FSR/% V_S
+5VDC		±0.0005			±0.0005		% of FSR/% V_S
POWER SUPPLY REQUIREMENTS							
Rated Voltage		±15, +5			±15, +5		VDC
Range	±14.5, +4.75	±15, +5	±15.5, +5.25	±14.5, +4.75	±15, +5	±15.5, +5.25	VDC
Supply Drain, ±15VDC no load		+35, -45	+50, -60		+35, -45	+50, -60	mA
+5VDC logic supply		9			9		mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Storage	-55		+100	-55		+100	C

NOTES:
1. FSR means Full Scale Range and is 20V for ±10V range, 10V for ±5V range, etc.
2. Adjustable to zero with internal trim potentiometer (offset adjustment external on DAC736).
3. With gain and offset errors adjusted to zero at +25°C.
4. LSB is for 16-bit resolution.
5. Maximum with no degradation of specifications.

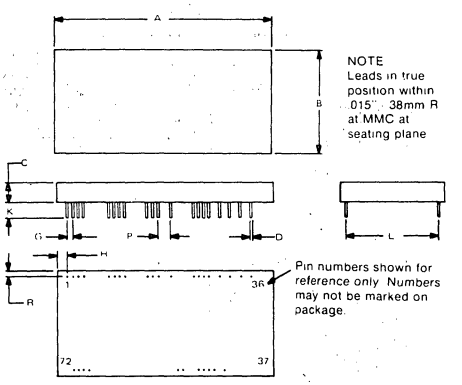
MECHANICAL

DAC73



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	3.950	4.010	100.33	101.85
B	1.950	2.010	49.53	51.05
C	.350	.410	8.89	10.41
D	.019	.021	0.48	0.53
G	.100 BASIC		2.54 BASIC	
H	.150	.250	3.81	6.35
K	.250	.350	6.35	8.89
L	1.800 BASIC		45.72 BASIC	
P	.200 BASIC		5.08 BASIC	
R	0.50	.150	1.27	3.81

DAC736



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	3.950	4.010	100.33	101.85
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C	.350	.410	8.89	10.41
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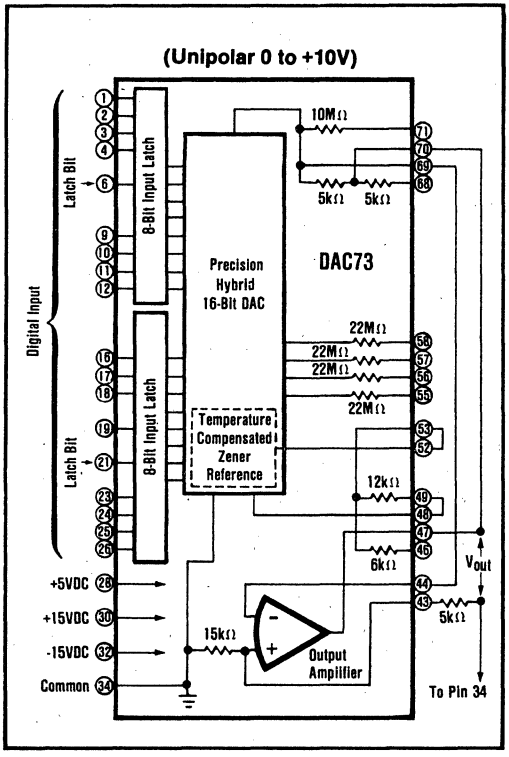
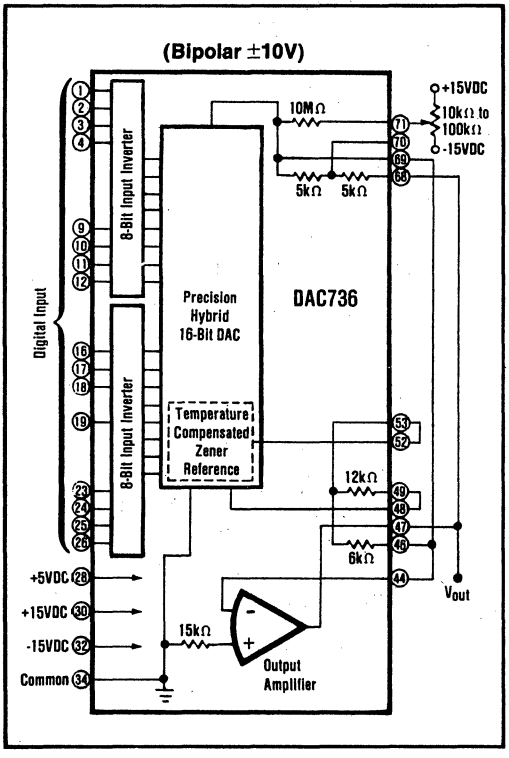
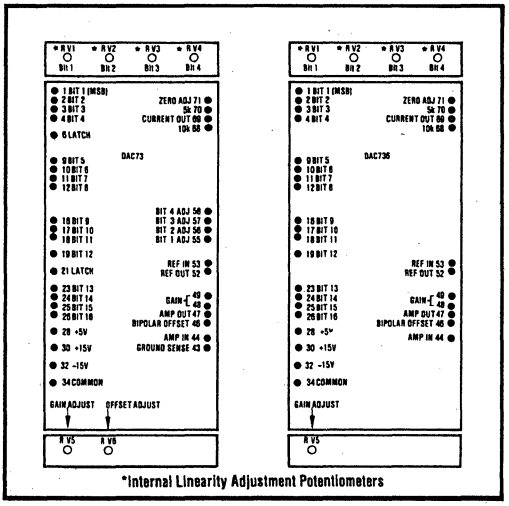
G	.100 BASIC		2.54 BASIC	
H	.150	.250	3.81	6.35
K	.250	.350	6.35	8.89
L	1.800 BASIC		45.72 BASIC	
P	.200 BASIC		5.08 BASIC	
R	0.50	.150	1.27	3.81

CONNECTION DIAGRAMS





PIN ASSIGNMENTS



DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC73/736 accepts complementary digital input codes in CSB or COB format. The COB model may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

	DIGITAL INPUT CODES			
CSB, COB MODELS	MSB LSB ↓ . . ↓	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Complement
All bits ON	0000...000	+Full Scale	+Full Scale	-1LSB
Mid Scale	0111...111	+1/2 Full Scale	Zero	-Full Scale
All Bits OFF	1111...111	Zero	-Full Scale	Zero
	1000...000	Mid Scale-1LSB	-1LSB	+Full Scale

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

INPUTS

Each bit input of the DAC73 consists of a buffered CMOS D type latch (see Figure 1). Bits 1 (MSB) through 8 are latched by a low level on pin 6. Bits 9 through 16 (LSB) are latched by a low level on pin 21. The latch inputs may be left open for transparent transfer of data.

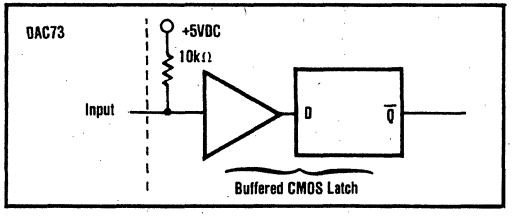


FIGURE 1. DAC73 Input.

The DAC736 inputs are CMOS inverters with 10kΩ pull-up resistors (see Figure 2).

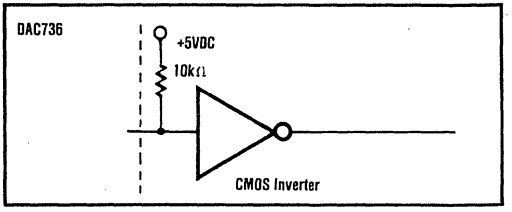


FIGURE 2. DAC736 Input.

The DAC73 and DAC736 can be driven directly by open collector or totem pole TTL logic.

ACCURACY

Linearity

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.00075% max (CSB, COB) from a straight line drawn through the end points (all bits ON and all bits OFF) at +25°C (see Figure 3).

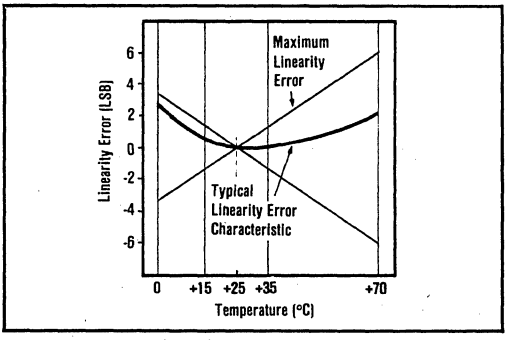


FIGURE 3. Nonlinearity vs Temperature.

Differential Linearity

Differential linearity error of a D A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1 2LSB means than the output voltage step sizes can be anywhere from 1 2LSB to 3/2LSB when the input changes from one adjacent input stage to the next.

Monotonicity

Monotonicity over a ±5°C range for the DAC73 and DAC736 is guaranteed when ambient linearity is calibrated. This insures that the analog output will increase or remain the same for increasing 16-bit input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in LSB's per °C (see Figure 4). Gain Drift is established by: 1) testing the end point differences for each DAC73 model at +25°C and the appropriate specification temperature extremes; 2) calculating the gain error with respect to the +25°C value; and 3) dividing by the temperature change. This is expressed in ppm/°C.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range.

The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

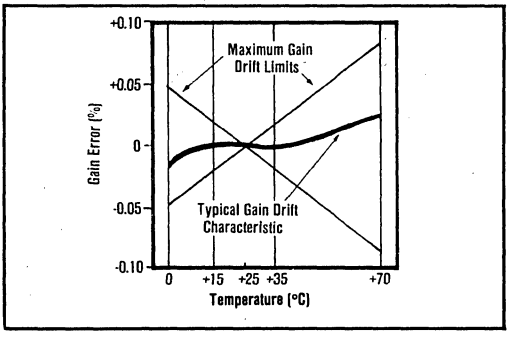


FIGURE 4. Gain Drift Error (%) vs Temperature.

SETTLING TIME

Settling time for each DAC73/736 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 5).

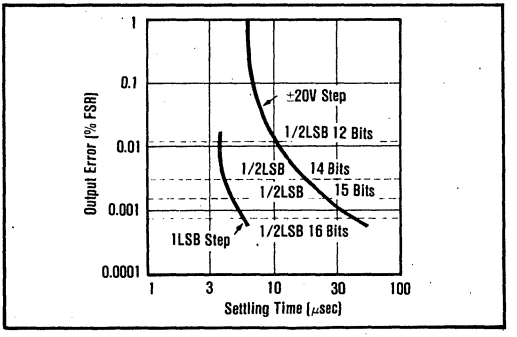


FIGURE 5. Full Scale Range Settling Time vs Accuracy.

Settling times are specified to ±0.00075% of FSR; one for maximum full scale range changes of 20V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output while maintaining

specified accuracy. The maximum compliance voltage is -1.5V to +10V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 6).

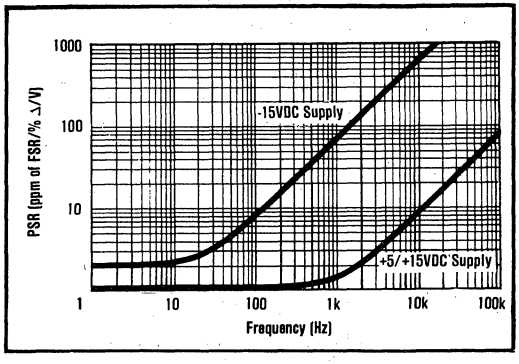


FIGURE 6. Power Supply Rejection vs Power Supply Ripple Frequency.

REFERENCE SUPPLY

All models are supplied with an internal +6V reference voltage supply. This reference voltage (pin 52) has a tolerance of ±0.05% and is connected internally for specified operation. The zener is selected for a Gain Drift of typically ±4ppm/°C and is burned-in for a total of 48 hours for guaranteed reliability. This reference may also be used externally but the current drain is limited to 4mA and constant load conditions.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection the DAC73 736 decoupling capacitors are included internally. Refer to Figure 13 for correct grounding connections.

OFFSET AND GAIN ADJUSTMENT

Before taking measurements or making adjustments, the DAC73 736 should be warmed up for at least 25 minutes. The DAC73 has internal gain and offset potentiometers that are connected to an internal regulated supply. In most applications no external adjustment will be required.

External offset and gain adjustment of the DAC736, or DAC73 if the application requires, maybe accomplished as shown in Figures 7 and 8. These external circuits could be used in an application using both unipolar and bipolar modes. Refer to Figures 9 and 10 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters. The internal potentiometers could be used to null the unipolar gain and offset, and the external null could be switched in by relays to null bipolar gain and offset. An alternate offset adjustment is shown on the DAC736 connection diagram.

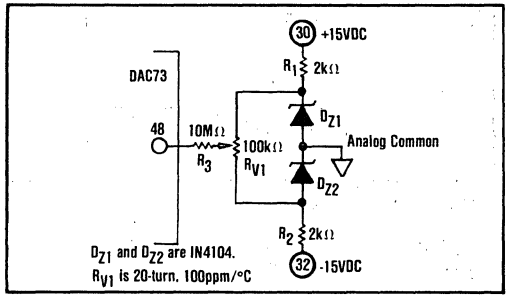


FIGURE 7. External Gain Adjustment.

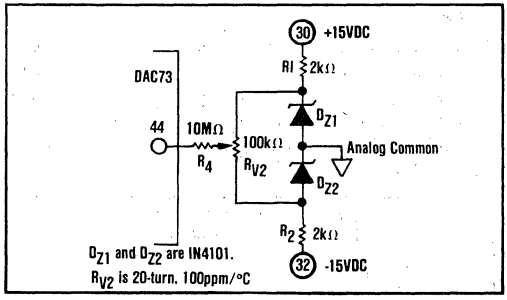


FIGURE 8. External Offset Adjustment.

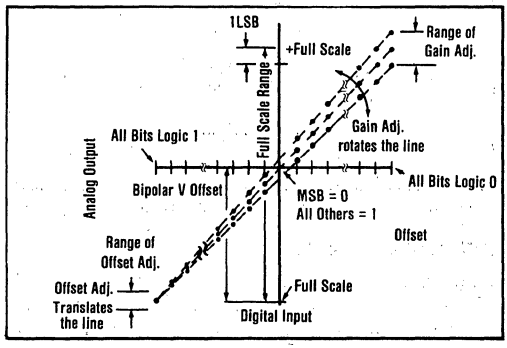


FIGURE 9. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

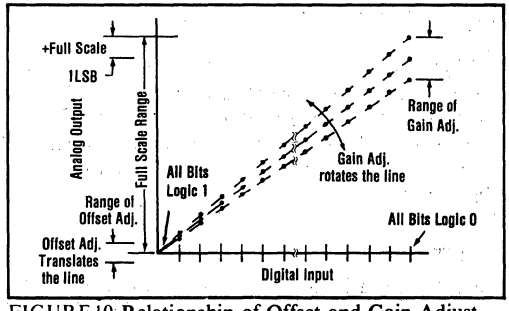


FIGURE 10. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors in the DAC73/736 provide a wide range of output voltage range connections. These internal resistors may be connected to provide three bipolar output voltage ranges of ±10V, ±5V, or ±2.5V or two unipolar voltage ranges of 0 to +5V or 0 to +10V. Since the internal scaling resistors are an integral part of the DAC73/736, gain and offset drift are minimized by their use. Connections for DAC73/736 are shown in Table II. Figure 11 is a connection diagram.

TABLE II. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 47 to	Connect Pin 46 to	Connect Pin 44 to	Connect Pin 68 to
±10V	COB	68	44	69	47
±5V	COB	70	44	69	NC
±2.5V	COB	70	44	69	69
0 to +10V	CSB	70	NC	69	NC
0 to +5V	CSB	70	NC	69	69

In all cases pins 52 and 53 and pins 48 and 49 should be shorted together with low resistance capacitance connections.

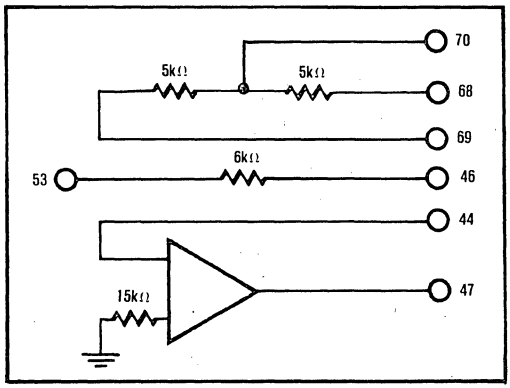


FIGURE 11. Output Amplifier Voltage Range Scaling Circuit.

LINEARITY ADJUSTMENT

Internal

If it becomes necessary to adjust the linearity of the DAC73 or DAC736 after an extended time period or for operation under temperature extremes, the 4MSB's may be user-adjusted. For optimum operation the unit should be calibrated in its operating environment. Calibration is performed by a differential linearity adjustment at the first four major carries. This method of calibration is possible since the DAC73 and DAC736 have almost no superposition error. The calibration procedure including gain, offset, and linearity adjustment is outlined in Table III. Steps 1 and 10 may be omitted for linearity adjustment only.

External (DAC73 only)

The linearity adjustment of the first 4MSB's of the DAC73 may be accomplished externally either with potentiometers or with D/A converters. Using a DAC to adjust linearity will allow computer controlled accuracy adjustments of the DAC thus giving the capability of maintaining 16-bit accuracy over all environmental variations. Gain and offset may also be adjusted in this manner.

Eight-bit bipolar voltage output DAC's can be used for all of the adjustments. Each circuit is shown in Figure 12.

INSTALLATION CONSIDERATIONS

To maintain the extremely-high accuracy of the DAC73 and DAC736 when installed in a system environment, careful attention must be paid to grounding and to connection resistances. Figures 13 and 14 are examples of correct connection configurations to yield maximum accuracy. The effects of various wiring and contact resistances R_1, R_2, R_3, and R_4 are reduced or eliminated as follows.

R_1 appears in series with the feedback resistance and therefore introduces only a gain error that can be nulled during calibration.

R_2 is inside the output amplifier feedback loop and its effect will be reduced by the loop gain.

In Figure 13 for the DAC736, R_3 is in series with the load

TABLE III. Calibration Procedure.

STEP	HEX INPUT CODE	ADJUST POTENTIOMETER(1)	DVM READING		DESCRIPTION
			UNIPOLAR MODE	±10 VOLT BIPOLAR MODE	
1	FFFF	R_{V6}(2)	0.0V	-10.0000V	Null Offset
2	F000	N/A	V_4	V_4	Read Output Voltage
3	EFFF	R_{V4}	V_4 + 153µV	V_4 + 305µV	Adjust R_{V4} until DVM reads V_4 + 1LSB
4	E000	N/A	V_3	V_3	Read Output Voltage
5	DFFF	R_{V3}	V_3 + 153µV	V_3 + 305µV	Adjust R_{V3} until DVM reads V_3 + 1LSB
6	C000	N/A	V_2	V_2	Read Output Voltage
7	BFFF	R_{V2}	V_2 + 153µV	V_2 + 305µV	Adjust R_{V2} until DVM reads V_2 + 1LSB
8	8000	N/A	V_1	V_1	Read Output Voltage
9	7FFF	R_{V1}	V_1 + 153µV	V_1 + 305µV	Adjust R_{V1} until DVM reads V_1 + 1LSB
10	0000	R_{V5}	+9.999847V	+9.999695V	Adjust Gain

NOTES: 1. For potentiometer location see Pin Assignments. 2. External offset adjustment on DAC736.

resistor and will cause an error in the voltage across R_L. One-half LSB error would result at full load for $R_3 = 0.02\Omega$. Therefore, if possible, sense the output voltage to include R_3.

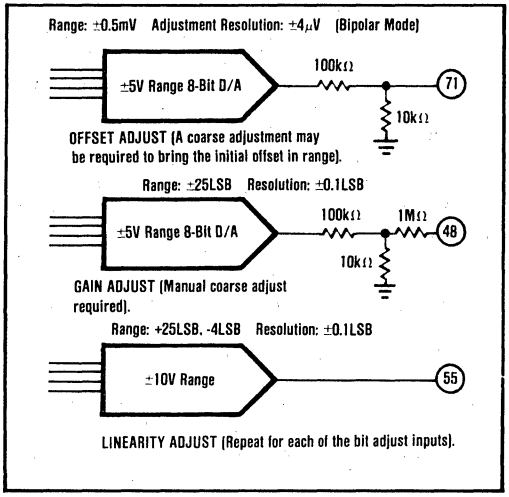


FIGURE 12. External Accuracy Adjustment.

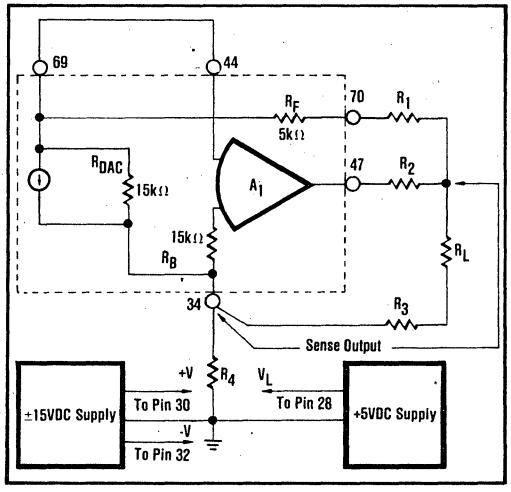


FIGURE 13. DAC736 - Unipolar Mode.

Figure 14 illustrates the optimum connection made possible by the ground sense pin on the DAC73. In the configuration shown $R'_F = R_F$ and $R'_B \parallel R_B = R_{DAC} \parallel R_{BPO}$. This causes any signal developed across R_3 to be rejected as a common-mode input, and R_3 will not affect the voltage across R_L. This configuration will also reject noise present on the system common.

R_4 is negligible in both circuits when ground connections are made as shown.

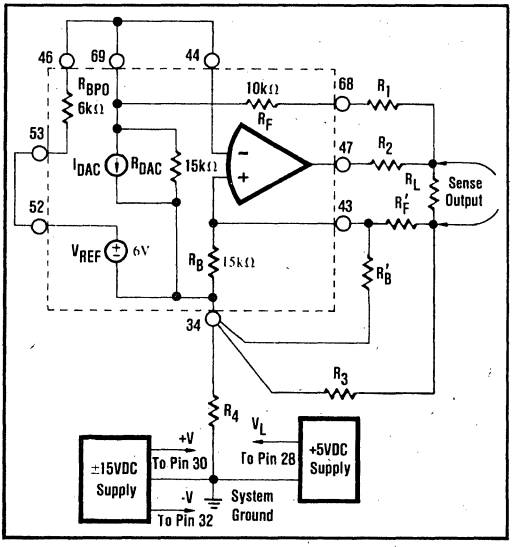


FIGURE 14. DAC73 - ±10V Bipolar Mode.

The DAC73/736 and the wiring to their connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field.

BURR-BROWN®

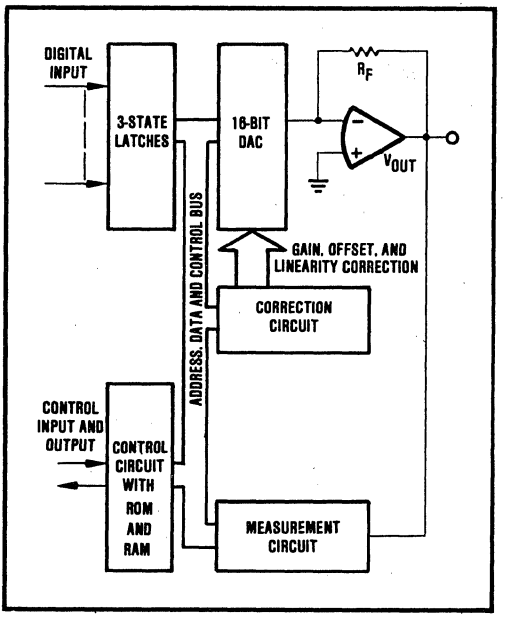
DAC74

Self-Calibrating High Resolution True 16-Bit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT RESOLUTION
- SELF-CALIBRATION MAINTAINS ACCURACY OF
  - ±1/2LSB NONLINEARITY
  - ±0.00035% GAIN ERROR
  - ±40μV OFFSET

  } +15°C TO +45°C
- UNIPOLAR OR BIPOLAR VOLTAGE OUTPUT
- DOUBLE BUFFERED FOR AN 8- OR 16-BIT BUS



DESCRIPTION

The DAC74 is a self-contained true 16-bit Digital-to-Analog converter designed for applications requiring high resolution and accuracy such as displays, frequency synthesizers, automated test equipment, analytical instruments, and high resolution controllers. Furthermore, in applications where equipment is inaccessible or frequent calibration is impractical the DAC74 is ideal because the self-calibration accuracy depends only on the long term stability of a heated zener reference diode.

Using self-calibration circuits, the DAC74 maintains typically ±1LSB total error over +15°C to +45°C! Compare this with other high resolution converters which can only maintain this accuracy over a ±2°C or ±3°C range. A patented microprocessor-controlled differential measurement technique is the key contributor to the DAC74's drift performance. This technique allows use of low cost hybrid and monolithic circuits to remove linearity, gain, and offset errors resulting from ambient temperature variations, component aging, and varying load conditions.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SYSTEM DESCRIPTION

The DAC74 is a self-calibrating, 16-bit digital-to-analog converter in a 5" x 7" x 0.6" (127mm x 178mm x 15.2mm) package. This D/A converter provides either a unipolar or a bipolar voltage output that is linear to within ±1/2LSB of the Full Scale Range (FSR). The FSR in the unipolar mode is set by the internal +10V reference. The FSR in the bipolar mode is set by the difference between the +10V and the -10V references. With respect to the internal references, the offset and gain errors are also less than ±1/2LSB. The settling time to ±1/2LSB is typically 6μsec for a 1LSB step.

A microprocessor-controlled calibration circuit retrims the D/A converter to this accuracy in the face of drift over temperature and time. The absolute accuracy of the calibration is dependent upon the accuracy of the internal voltage references. The drift of the reference is typically ±0.5ppm/°C.

The linearity and accuracy of the DAC74 versus temperature is illustrated in Figures 1 and 2. The calibration was performed at 5°C intervals. It can be seen that the calibration greatly increases the useful temperature range of the D/A converter.

The DAC74 (see Figure 3) consists of (1) a 16-bit, latched input main D/A converter, which performs the digital-to-analog conversion, (2) a stable, temperature-compensated voltage reference, (3) an error-measuring circuit which compares the D/A converter output to known references, and (4) a microcomputer-based controller that stores the output of the error measuring circuit and calculates correction factors for offset, gain, and linearity. The controller stores these correction factors in RAM and these are used to adjust errors when an input data word selected by the user is presented at the input to the main D/A converter.

The critical components, including the current steering switches and the laser-trimmed resistor network, are contained in a single ceramic hybrid package for improved thermal tracking. The zener reference is maintained at a constant temperature to reduce drift due to ambient temperature fluctuations.

The DAC74 is housed in a steel package which provides excellent electromagnetic shielding. The package can be mounted from either side for socket mounting or for use of ribbon cable connectors.

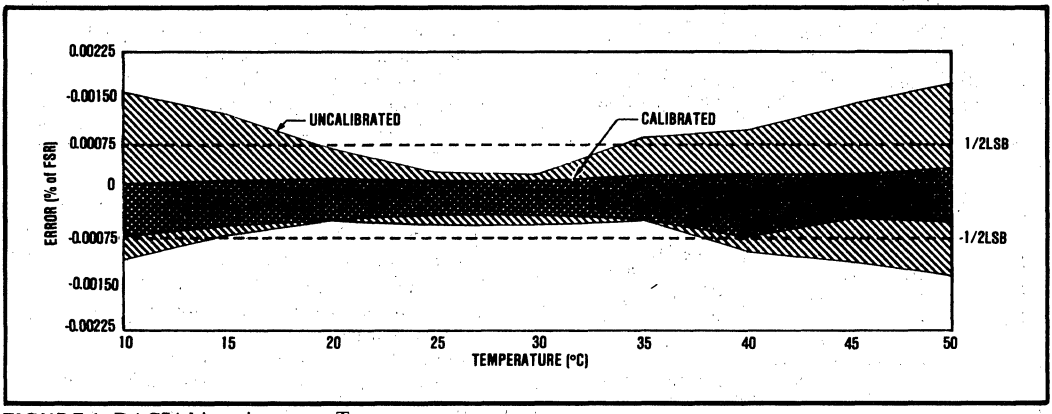


FIGURE 1. DAC74 Linearity versus Temperature.

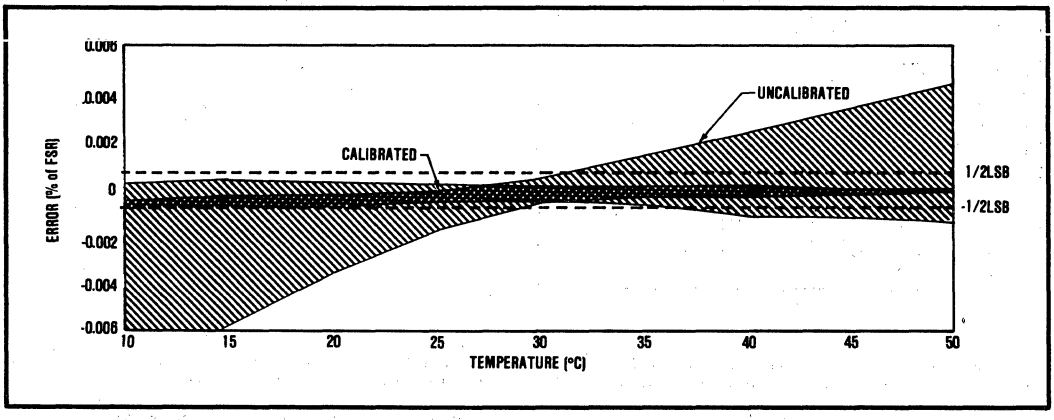


FIGURE 2. DAC74 Accuracy versus Temperature.

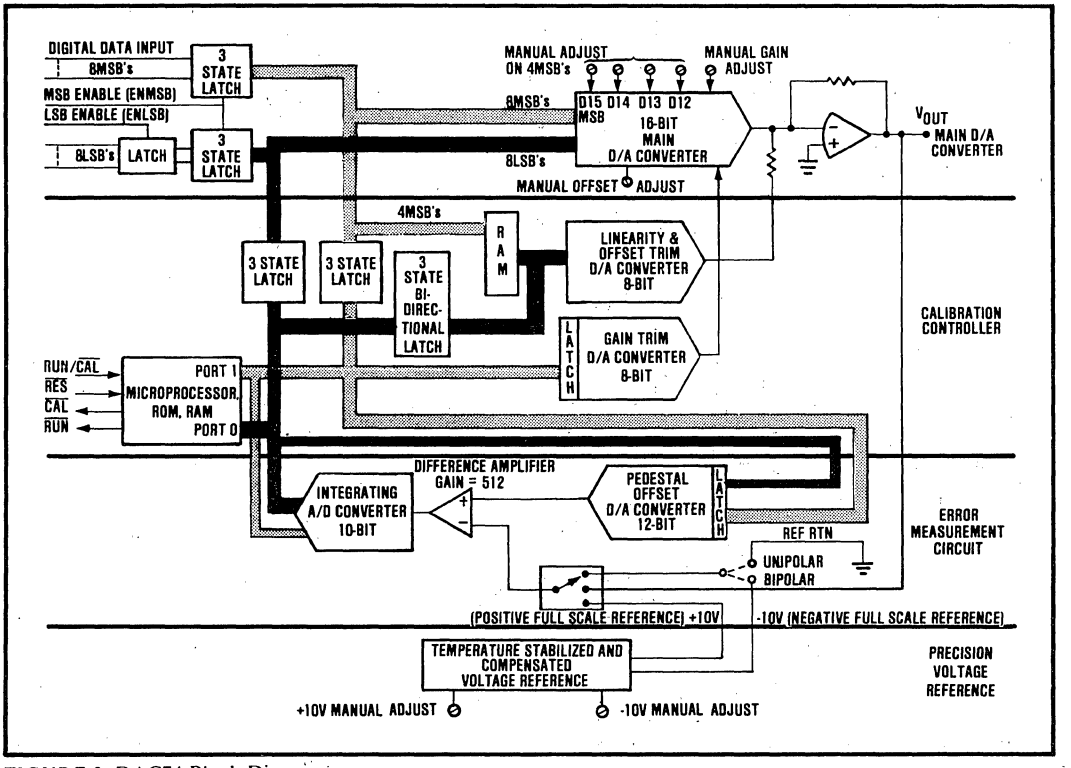


FIGURE 3. DAC74 Block Diagram.

A user initiates a calibration by applying a negative pulse to the reset input $\overline{\text{RES}}$ with the RUN $\overline{\text{CAL}}$ input held low. After an initial system check, the $\overline{\text{CAL}}$ status goes low and a 2.5 second calibration cycle is started. During calibration, the external inputs are disabled and the $\overline{\text{RUN}}$ status is high. The D/A converter returns to the RUN mode at the end of the calibration cycle. $\overline{\text{CAL}}$ remains low in the RUN mode if the calibration was successful. The $\overline{\text{RUN}}$ status output is low during normal D/A converter operation; in this state, the external digital data inputs are routed to the main D/A converter.

THE MAIN D/A CONVERTER

The 16 data inputs to the main D/A converter are buffered by two octal latches that are enabled by a high input to ENMSB. In addition, the 8LSB's are double buffered by a latch with an enable input labeled ENLSB. This arrangement allows transparent operation, a 16-bit interface, or an 8-bit interface. The data inputs are positive true. The MSB is labeled D15 and the LSB is labeled D0. Both latches transfer their inputs to the output when the enable is high. The input data is held in the latch when the enable is low.

Four potentiometers adjust the bit currents for the 4MSB's. Two more potentiometers allow the Offset and Gain to be adjusted manually. After a calibration period of 1 year, these potentiommeter adjustments may be required to trim the D/A converter to within the error range which can be trimmed by the self-calibration circuits. The procedure is given in the Manual Calibration section.

The output operational amplifier converts the 0 to 2mA current from the bit switches into a voltage output. A 5-wire output connection to the main D/A converter is described in the Installation section. All five wires MUST be installed to the load as indicated to obtain the full specified accuracy.

The output connection diagrams for 0 to +10V unipolar operation or ±10V bipolar operation are shown in the Installation section. Jumpers must be installed to configure the main D/A converter and the calibration circuits for each of these output configurations.

PRECISION VOLTAGE REFERENCES

The +10V and -10V references, shown in Figure 3, supply the voltage standards for calibrating the main D/A converter. The -10V reference is required only for bipolar operation. The ±10V references derive their outputs from a heated zener reference diode. In addition, both reference circuits are temperature compensated to cancel variations caused by drift in the other components of the reference. The accuracy of these references over temperature and time determine the accuracy of the D/A converter after calibration. These reference voltages are available for external use but the load must remain constant. Alternatively, external +10V and -10V references may be used with the DAC74.

ERROR MEASUREMENT CIRCUIT

The error measurement circuit of the DAC74 includes an analog switch, differential instrumentation amplifier, pedestal offset D/A converter, and an analog-to-digital converter. The circuit measures a sequence of voltage pairs. The error of the main D/A converter trim is derived from the differences in each pair of voltages. For instance, the Offset error is the difference between the minus full scale D/A converter output and the minus full scale reference (RTN for unipolar and -10V for bipolar). The Gain error is the difference between the plus full scale D/A converter output and the +10V reference less 1LSB.

The analog switch selects one of three sources as the input to the instrumentation amplifier. These sources are the main D/A converter output, minus full scale reference, and the plus full scale reference. The analog switch is controlled by the calibration controller.

The difference amplifier derives one of its inputs from a pedestal offset D/A converter which provides a voltage roughly comparable to the other input. The other input comes from the analog switch. During any pair of measurements, the pedestal offset D/A converter output remains the same. Since the gain of the instrumentation amplifier is 512, small differences (20μV) in the voltage pair are detected by the analog-to-digital converter connected to the output of the difference amplifier. The input to the pedestal offset D/A converter is set to the same value as that sent to the main D/A converter so that the high gain difference amplifier will stay within its linear range. The accuracy of the pedestal offset D/A converter does not affect the calibration accuracy.

The 10-bit analog-to-digital converter translates the output of the difference amplifier into a digital code for the microcomputer-based controller. Only the difference in the readings between a pair of measurements is used by the controller. The Gain and Offset of this 10-bit analog-to-digital converter are preset at the factory. The control signals to the A/D converter are generated by the controller during a calibration cycle.

CALIBRATION CONTROLLER

The Calibration Controller consists of a microcomputer which has three functions; (1) interpret commands from the control inputs and terminal interface, (2) conduct measurements by sending control signals to the error measurement subsystem, and (3) calculate the trims to be sent to the trim D/A converters. In the RUN mode, the microcomputer is idle; in fact, it can be turned off to reduce noise by asserting the MPUOFF control input high or leaving it open. The user may initiate a calibration cycle with a negative pulse to the $\overline{\text{RES}}$ control input with the MPUOFF and the RUN/$\overline{\text{CAL}}$ control inputs both low. At the end of the pulse to $\overline{\text{RES}}$, the $\overline{\text{RUN}}$ status output goes high indicating the main D/A converter is no longer under user control. As discussed in the Manual Calibration section, the $\overline{\text{CAL}}$ output goes low indicating that the calibration process is underway. At the end of the calibation, the $\overline{\text{RUN}}$ status will return low. If and only if the calibration succeeds, the $\overline{\text{CAL}}$ status will remain low.

The two status outputs $\overline{\text{RUN}}$ and $\overline{\text{CAL}}$ are open-collector TTL outputs (7406) which can drive an LED indicator directly. At the end of the calibration, the controller automatically returns to the RUN mode and control of the main D/A converter inputs is returned to the user.

The Offset is first adjusted with respect to the minus full scale reference. Then a sequence of four differential linearity measurements are conducted on the four MSB's of the D/A converter. Starting with the LSB of these four bits, each bit is trimmed to be linear with respect to all the lesser significant bits. After the linearity is established, a final gain correction is made with respect to the full scale reference. If the calibration fails, either a component has failed, or the internal drift of the system has exceeded the range of the trim circuit. If calibration under normal operating conditions fails, adjustments of eight potentiometers must be made to restore the D/A converter to its original accuracy. A detailed description of the calibration procedure is contained in the Manual Calibration section.

The trim circuits of the DAC74 consist of 16 RAM locations, Linearity/Offset trim D/A converter, and a Gain trim D/A converter. As shown in the block diagram, the RAM address inputs are taken from either a latch connected to the controller bus or from the four MSB's of the data input to the main D/A converter. In the RUN mode, the four inputs from the main D/A converter select one of 16 digital codes. The 8-bit code selected by the address inputs constitutes the sum of the corrections for the Offset error and the sum of the bit errors for those bits of the upper four which are logic ones. For instance, the RAM location 0 contains the digital code for just the Offset correction since none of the upper four bits are turned on. The RAM location 8 contains the digital code for the sum of the Offset correction and the correction for the MSB error. During calibration, the controller addresses the RAM. It first zeros the RAM and then adds the correction for the Offset error to all the RAM locations. Then the corrections for the bit errors are added to those locations which have that bit turned on. For instance, the correction for the MSB is added to all locations whose address starts with one (1XXX). The 8-bit digital code from the RAM is the input to the Offset/Linearity trim D/A converter. The output of the trim D/A converter makes a slight adjustment in the total current of the main D/A converter (one part in 2048). The maximum trim in the unipolar mode is ±2.44lmV. With an 8-bit resolution trim D/A converter, the minimum possible trim is 1/8LSB or 0.019mV at the main D/A converter output.

A final Gain trim is made by sending a separate 8-bit trim word to the Gain D/A converter. The Gain error is the deviation of the full scale output from the full scale reference (+10V -1LSB). The maximum and minimum correction range in the full scale output are the same as the linearity/offset maximum and minimum, 2.441mV.

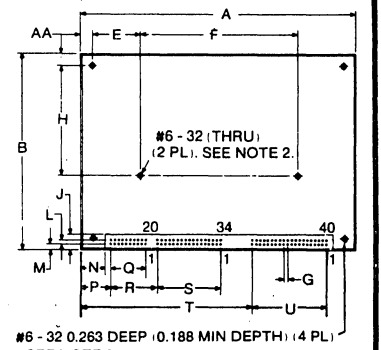
SPECIFICATIONS

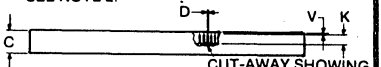
ELECTRICAL

T_A = 25°C, rated power supplies and after 30 minute warm-up unless otherwise noted.

MODEL	DAC74			
	MIN	TYP	MAX	UNITS
DIGITAL INPUT				
Resolution			16	Bits
Voltage Levels				
Logic 1, V_{IH}	+2		+5.5	VDC
Logic 0, V_{IL}	0		+0.8	VDC
Current				
D0-D15, ENLSB, ENMSB (SN74LS373)				
I_{IH}, V_I = 2.7V			20	µA
I_{IL}, V_I = 0.4V			-0.4	mA
$\overline{RES}$, RUN/$\overline{CAL}$, $\overline{UNIPOLAR\ CAL}$				
I_{IH}, V_I = 2.4V			40	µA
I_{IL}, V_I = 0.4V			-1.6	mA
MPUOFF (inc. 10kΩ pullup)				
I_{IH}, V_I = 2.4V			-0.3	mA
I_{IL}, V_I = 0.4V			-2.1	mA
ANALOG OUTPUT				
Ranges, Unipolar		0 to +10		V
Bipolar		±10		V
Output Impedance (DC)		0.03	0.05	Ω
Short Circuit to Common (Duration)		Indefinite		
Load Current	±5			mA
Settling Time (to ±1/2LSB				
20V Step		20	50	µsec
1LSB Step(1)			10	µsec
Slew Rate		18		V/µsec
Noise				
Voltage, Bipolar				
0.1Hz to 10Hz		10		µV, p-p
10Hz to 100Hz		70		µV, rms
DIGITAL OUTPUT				
Open Collector (SN7406) (with 10kΩ Pullup)				
Voltage Levels				
Logic 1	+2.4			V
Logic 0			+0.4	V
Current (with 10kΩ Pullup)				
$\overline{CAL}$, $\overline{RUN}$				
I_{OH}			1	mA
I_{OL}			-15	mA
TRANSFER CHARACTERISTICS AFTER SELF-CALIBRATION CYCLE				
Accuracy(2)				
Total Error				
Unipolar			±0.0015	% of FSR(3)
Bipolar			±0.0015	% of FSR
Linearity Error			±1/2	LSB
Gain, Error, Unipolar			±0.00035	% of output
Bipolar			±0.00035	% of output
Offset Error, Unipolar			±40	µV
Bipolar			±80	µV
Monotonicity after Calibration, 16 bits		Guaranteed		
DRIFT				
Total Error Drift (includes gain, offset and linearity drift(4))				
Unipolar		±4	±9	ppm of FSR/°C
Bipolar		±5	±11	ppm of FSR/°C
Total Error over Temp Range				
Voltage, Unipolar (0°C to 70°C)			±0.06	% of FSR
Bipolar			±0.06	% of FSR
Voltage, Unipolar (+15°C to +45°C)			±0.013	% of FSR
Bipolar			±0.013	% of FSR
Gain (exclusive of reference drift)		±2	±5	ppm/°C
Offset (exclusive of reference drift)				
Unipolar		±0.5	±1	ppm of FSR/°C
Bipolar		±2	±3	ppm of FSR/°C
Differential Linearity over Temperature		±1	±2	ppm of FSR/°C
Linearity Error over Temperature		±1	±2	ppm of FSR/°C
PRECISION 10V REFERENCES				
Voltage(5)	±9.9995	±10.00	±10.0005	V
Drift vs Temperature		±0.5	±1	ppm/°C
External Current(6)			±4	mA

MECHANICAL

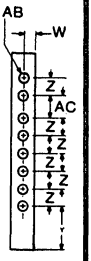




NOTES:
1. Leads in true position within 0.015" (0.38mm) R at MMC at seating plane.
2. Holes in true position within 0.015" (0.38mm) R at MMC.

CASE MATERIAL: Epoxy coated steel
LABEL: Metal foil
WEIGHT: 20oz. (257gm.) max.
PIN: Gold Flashed
Mating Connectors shipped with DAC74:

AMP86418-1	20 pin, P1 Test Interface
AMP1-86418-8	34 pin, P2 Digital
AMP86418-2	40 pin, P3 Analog

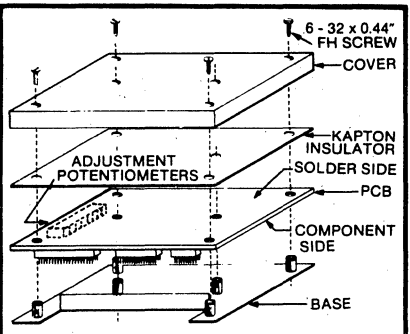


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	6.980	7.020	177.29	178.31
B	4.980	5.020	126.49	127.51
C	.550	.600	13.97	15.24
D	.022	.028	.56	.71
E	1.112 BASIC		28.24 BASIC	
F	4.150 BASIC		105.41 BASIC	
G	.100 BASIC		2.54 BASIC	
H	2.837 BASIC		71.98 BASIC	
J	.353	.373	8.97	9.47
K	.308	.328	7.82	8.33
L	.100 BASIC		2.54 BASIC	
M	.143	.183	3.63	4.65
N	.573	.613	14.55	15.57
P	.730	.770	18.54	19.56
Q	.900 BASIC		22.86 BASIC	
R	1.200 BASIC		30.48 BASIC	
S	1.600 BASIC		40.64 BASIC	
T	3.600 BASIC		91.44 BASIC	
U	1.900 BASIC		48.26 BASIC	
V	.020	.040	.51	1.02
W	.267	.287	6.78	7.29
Y	.831	.851	21.11	21.62
Z	.430	.470	10.92	11.94
AA	.293	.333	7.44	8.46
AB	.240	.260	6.10	6.60
AC	.565	.585	14.35	14.86

ELECTRICAL (CONT)

MODEL	DAC74			
	MIN	TYP	MAX	UNITS
STABILITY, LONG TERM				
Gain (exclusive of reference)		±30		ppm/10³ hr
Offset (exlusive of reference)				
Unipolar		±5		ppm of FSR/10³ hr
Bipolar		±30		ppm of FSR/10³ hr
Linearity		±0.25	±0.5	LSB/10³ hr
Precision 10V References		±20		ppm/10³ hr
POWER SUPPLY SENSITIVITY				
Unipolar Offset				
+15V and -15V Supplies		±0.0001		% of FSR/%Vs
+5V Supply		±0.0001		% of FSR/%Vs
Bipolar Offset				
+15V and -15V Supplies		±0.0004		% of FSR/%Vs
+5V Supply		±0.0001		% of FSR/%Vs
Gain				
+15V and -15V Supplies		±0.001		% of FSR/%Vs
+5V Supply		±0.0005		% of FSR/%Vs
POWER SUPPLY REQUIREMENTS				
Range	±14.5, +4.75	±15, +5	±15.5, +5.25	V V
Supply Drain, ±15VDC (not including output load)			200	mA
Current Surge, +15V Supply[7]			400	mA
+5VDC Supply			800	mA
TEMPERATURE RANGE				
Self-calibration Operation	+15		±45	°C
Drift Specification	0		+70	°C
Storage	-55		+100	°C
TIMING SPECIFICATIONS				
Control and Status Timing[8]				
t_{on}	50			msec
t_{RES}	14			µsec
t_{IN}			500	µsec
td_0		100		µsec
td_1		100		µsec
t_{RUN} (self-cal mode)		2.5	3	sec
t_{RUN} (service mode)		300	350	msec
Data Input Timing				
$t_{ENLSB, ENMSB}$ (pulse width t_w)	15			nsec
t_{su} (data input setup time)	20			nsec
t_h (data input hold time)	10			nsec

MECHANICAL (CONT)



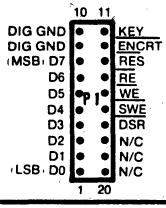
Screws holding the package together are covered by the top label (not shown). If the package must be opened, the top label must be peeled back at the corners. The package is mounted through inserts in the corners when the connectors are mounted pins-down or through the two holes in the center of the package when the connectors are mounted pins-up.

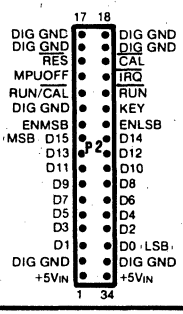
Manual calibration potentiometers are located on one end of the package. The potentiometers are accessed by peeling off the label on the edge of the package.

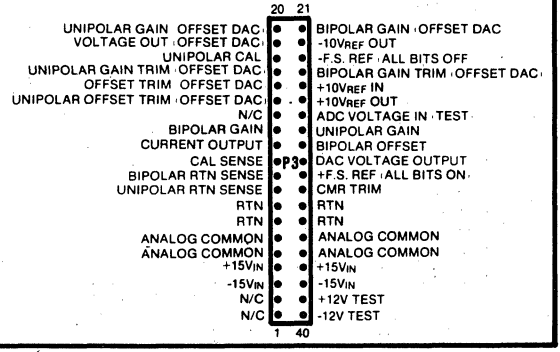
NOTES:
1. 1LSB at 16 bits = 0.00152% of FSR, = 15.2ppm of FSR, 152µV unipolar, 304µV bipolar.
2. Self-calibration can operate over +15°C to +45°C. DAC74 meets these specifications after the calibration cycle. These assume that the ±10V references have been adjusted to ±10.0000V ±10µV after 30-minute warm-up.
3. FSR means Full Scale Range and is 20V for bipolar and 10V for unipolar.
4. DAC74 will operate as a D/A converter over 0°C to +70°C. Self-calibration feature may be out of correctable range over a temperature range wider than +15°C to +45°C.
5. Manually adjustable to +10.00000 and -10.00000 after 30-minute warm-up.
6. Maximum with constant load for no degradation of specifications.
7. The heater current of the heated zener reference momentarily causes the initial power-up current of the +15V supply to approach 400mA. The +15V supply current then tapers to less than 200mA within 3 seconds.
8. See Operation section for timing diagrams.

PIN CONFIGURATION

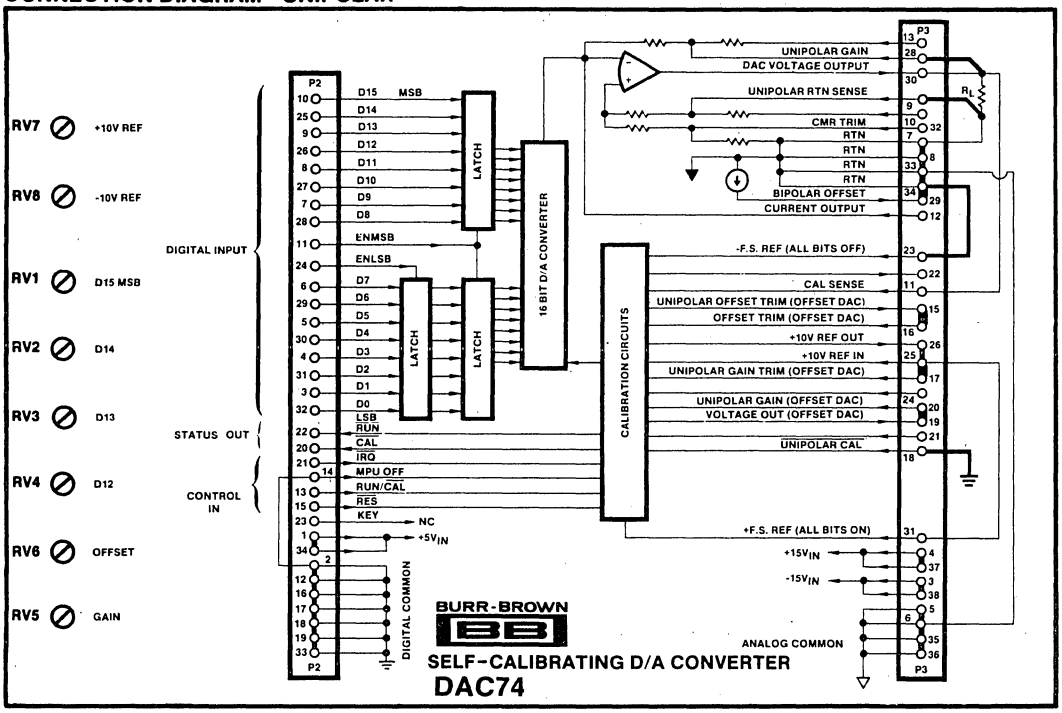
Connector P1 is a special service and test connector used by the factory. P2 is the Digital I/O connector containing the 16 input lines to the D/A converter, the control and status signals, and the +5V supply pins. Connector P3 contains all analog function pins for output, output sense, references, options, analog test points, and ±15V power supply input.
The DAC74 is delivered complete with mating connectors for printed circuit mounting.



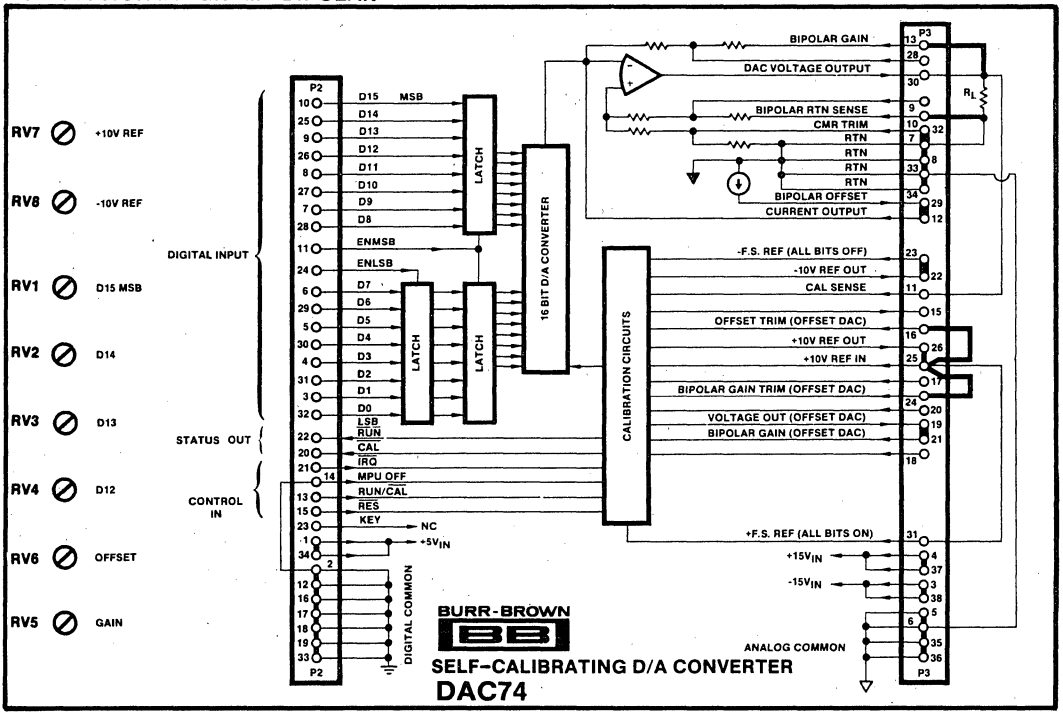




CONNECTION DIAGRAM - UNIPOLAR



CONNECTION DIAGRAM - BIPOLAR



DESCRIPTION OF PIN FUNCTIONS

CONNECTOR P1

Connector P1 is a test connector used by the factory. It is not described in this data sheet.

CONNECTOR P2 (Digital Signal Connector)

Pin No.	Designation	Function
1	$+5V_{IN}$	+5V supply input. Connected internally to pin 34.
2	DIGITAL COMMON	+5V supply return. Connected internally to pins 12, 16, 17, 18, 19, 33.
3 through 10	D1, D3, D5, D7, D9, D11, D13, D15	Data input to the Main D/A. D15 is the MSB. Logic 1 is a high input logic level.
11	ENMSB	Enable for the data input latches. Controls the MSB byte latch and the 2nd latch in the double-buffered LSB byte. Level triggered on high level.
12	DIGITAL COMMON	+5V supply return.
13	RUN $\overline{\text{CAL}}$	Control input. Low input for SELF-CALIBRATION mode. High input for SERVICE, the manual calibration mode.
14	MPU OFF	Controls microprocessor oscillator. Low - ON, High - OFF. Must be low for 50msec before $\overline{\text{RES}}$ is asserted.
15	$\overline{\text{RES}}$	Control input. Resets the DAC74 controller and subsequently causes the RAM to be cleared and "calibration" or "service" to begin. Input is a logic 0 (low) pulse with 14μsec minimum width.
16, 17, 18, 19	DIGITAL COMMON	+5V supply return.
20	$\overline{\text{CAL}}$	Status Output. Informs the user if calibration failed. Logic low means calibration successful.
21	$\overline{\text{IRQ}}$	An internal microprocessor control input. Not used by user.
22	$\overline{\text{RUN}}$	Status Output. This is high during the time the calibration controller has control of the main D/A converter.
23	KEY	This pin may be used to key the module to protect against incorrect plug-in alignment.
24	ENLSB	Enable input for LSB byte latch. Level triggered on high level.
25 through 32	D14, D12, D10, D8, D6, D4, D2, D0	Data input to the main D/A. D0 is the LSB. Logic 1 is high logic level.
33	DIGITAL COMMON	+5V supply return.
34	$+5V_{IN}$	+5V supply input.

CONNECTOR P3 (Analog Connector)

Pin No.	Designation	Function
1, 2	NC	No connection.
3	$-15V_{IN}$	-15V supply input. Connected internally to pin 38.
4	$+15V_{IN}$	+15V supply input. Connected internally to pin 37.
5, 6	ANALOG COMMON	Return for ±15V supply. Connected internally to pins 35 and 36.
7, 8	RTN	Analog return for the analog output. Connected internally to pins 33 and 34.
9	UNIPOLAR RTN SENSE	Unipolar Return Sense. Analog load sense for unipolar output configuration.
10	BIPOLAR RTN SENSE	Bipolar Return Sense. Analog load sense for bipolar output configuration.
11	CAL SENSE	Calibration Sense. A connection to sense the D/A output at the load and provide an input to the error measurement circuit.
12	CURRENT OUTPUT	A connection to the current output of the bit switches. Used to connect Bipolar Offset, pin 29.
13	BIPOLAR GAIN	Connection to scale the output amplifier for bipolar output range (-10 to +10V) and to provide a sense input from the load.
14	NC	No connection.
15	UNIPOLAR OFFSET TRIM (OFFSET DAC)	Connects an internal trim network to pin 16 for unipolar operation. This network is factory set.
16	OFFSET TRIM (OFFSET DAC)	Offset trim input connection to the pedestal offset D/A converter.
17	UNIPOLAR GAIN TRIM (OFFSET DAC)	Gain trim input connection to the pedestal offset D/A converter for unipolar operation.
18	UNIPOLAR CAL	A digital option line selecting the software routine calibrating the main D/A converter for the bipolar or unipolar configuration.
19	VOLTAGE OUT (OFFSET DAC)	Analog output of the pedestal offset D/A converter.
20	UNIPOLAR GAIN (OFFSET DAC)	Connects the pedestal offset D/A converter for 0 to +10V output range. Connect to pin 19.
21	BIPOLAR GAIN (OFFSET DAC)	Connects the pedestal offset D/A converter for -10V to +10V output range. Connect to pin 19.
22	$-10V_{REF}$ OUT	-10V precision reference output.
23	-F.S. REF (ALL BITS OFF)	Minus Full Scale input to analog switch of error measurement circuit. Connect to pins 7, 8, 33, 34 for unipolar. Connect to pin 22 for bipolar.
24	BIPOLAR GAIN	Gain trim input connection to the pedestal offset D/A converter for bipolar operation. Connect to pin 25.

25	$+10V_{REF}$ IN	Connection to provide precision +10V reference to the D A converter circuits. Connect to pin 26.
26	$+10V_{REF}$ OUT	+10V precision reference output.
27	ADC VOLTAGE IN (TEST)	The analog output of the difference amplifier in the error measurement circuit.
28	UNIPOLAR GAIN	Connection to scale the output amplifier for unipolar output range (0 to +10V) and to provide a sense input from the load.
29	BIPOLAR OFFSET	Connects the bipolar offset current source to the current output of the main D A converter to provide bipolar offset. Connect to pins 7, 8, 33, 34 for unipolar. Connect to pin 12 for bipolar.
30	DAC VOLTAGE OUTPUT	Analog voltage output of the main D A converter.
31	+F.S. REF (ALL BITS ON)	Plus Full Scale input to analog switches of the error measurement circuit. Connect to pin 25.
32	CRM TRIM	Common-mode rejection trim for the output amplifier for bipolar operation only. Connect to pins 7, 8, 33, 34 for unipolar. Connect to pin 12 for bipolar.
33, 34	RTN	Analog return for the analog output. Also connected internally to pins 7 and 8.
35, 36	ANALOG COMMON	Return for ±15V supplies. Connected internally to pins 5 and 6.
37	$+15V_{IN}$	+15V supply input. Connected internally to pin 4.
38	$-15V_{IN}$	-15V supply input. Connected internally to pin 3.
39	+12V TEST	Test pin for internal +12VDC.
40	-12V TEST	Test pin for internal -12VDC.

INSTALLATION

The three connectors described in the previous section have three separate functions; analog interface, digital interface, and the terminal interface. The terminal interface is used only for factory test. Connection to a printed circuit board can be made using female printed-circuit-mounted connectors supplied with the DAC74. They should be positioned relative to the four internally-threaded mounting holes at the corners of the DAC74 as shown in Figure 4. Mount the DAC74 with four #6 external tooth lockwashers and four #6-32 screws using 0.156" diameter holes. Be sure to leave clearance for screwdriver adjustment of the trim potentiometers.

Alternatively, the DAC74 can be mounted on a chassis with the connectors facing upward using two #6 lockwashers and two #6-32 screws by means of the two internally-threaded holes near the center of the DAC74 as shown in Figure 4. In this orientation, connection to ribbon cable can be made with mass terminated, female, flat cable connectors (3M, 3421-0000, 3414-0000, 3417-0000). Individual wires may also be connected to the DAC74 in this orientation using female wire-applied connectors (AMP 1-87456-6, 3-87456-0, 3-87456-6 housings plus appropriate crimp snap-in pins). In either case, the jumpers for the unipolar or the bipolar configuration should be made right at the analog connector P2 as described in the following paragraph. The potential drops due to long jumpers cause a degradation in the accuracy of the calibration circuit.

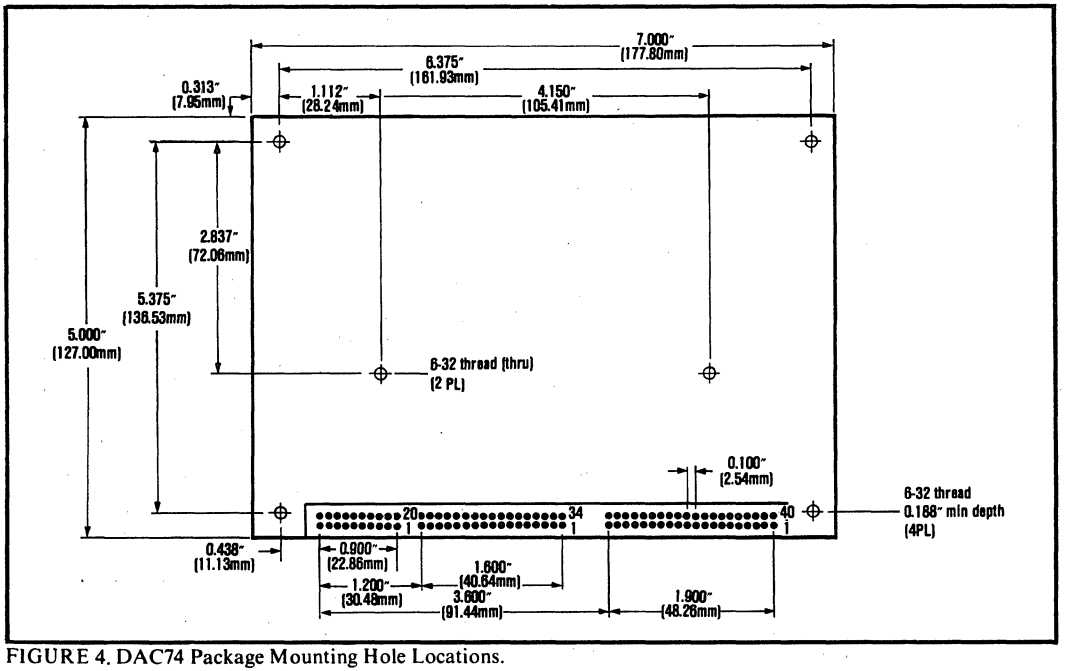


FIGURE 4. DAC74 Package Mounting Hole Locations.

POWER SUPPLY CONNECTIONS

A typical configuration is shown in Figure 5. Regardless of the local grounding, bring two separate return lines from the common near the power supplies to the DAC74. Connect one to Digital Common and the other to Analog Common. The load return line should be connected only to RTN (pins 7, 8, 33, 34) on P3 as shown in the unipolar and bipolar Connection Diagrams. Other connections to local grounds should be made with caution as they may cause ground loops which induce undesirable voltages at the common return points. The case is tied internally to Analog Common. Normally it should not be connected to any local grounds. Besides the power supply connections, other connections to the DAC74 should be limited to the digital inputs with a single digital current return and the 5-wire connection to the load. The external connections should be made so as to minimize the conduction paths to external noise sources. Internal bypass capacitors are included in the DAC74; no other bypass is needed nor recommended.

The power supply voltages may be sequenced on or off in any order provided that the power supply inputs have no transient voltages of polarity opposite to the normal DC input with respect to Analog or Digital Common.

The power supply requirements are listed below. During power-up, an initial surge of 400mA is required by the +15V supply input.

Input Voltage	+5V	+15V	-15V
Current, max	800mA	200mA	200mA
typ	500mA	150mA	150mA

Precautions

1. Provide all three grounds before applying voltage to either the power supply inputs or the signal inputs.
2. Avoid static discharge during handling and installation. Store the DAC74 in a conductive package.
3. Use short pairs of wire close together to minimize electromagnetic pickup.

In very noisy environments, separate floating supplies may be needed to power the DAC74. These supplies and their common returns should be connected only to the DAC74. Some experimentation with extra shielding and alternative return configurations may be necessary in extreme circumstances.

OUTPUT CONNECTION

The output connection for unipolar and bipolar operation are shown in the Connection Diagrams. For either unipolar or bipolar, it is very important to provide both a current-carrying wire and a sense wire to both sides of the load in order to minimize the errors caused by induced potentials and losses in the wiring to the load. The fifth wire, CAL SENSE, returns the output voltage at the load to the error measurement circuit. In a noisy environment these wires should be enclosed in a shield that is connected only to the RTN pins of the DAC74. The return line from the load to the RTN pin of the DAC74 must be separate from other grounds in order to avoid potential drops due to shared current paths. The resistance of this path must be low so that the voltage drop is less than 20μV. For example, at 5mA one foot of 16-guage copper wire (4Ω/1000ft.) produces a 20μV drop.

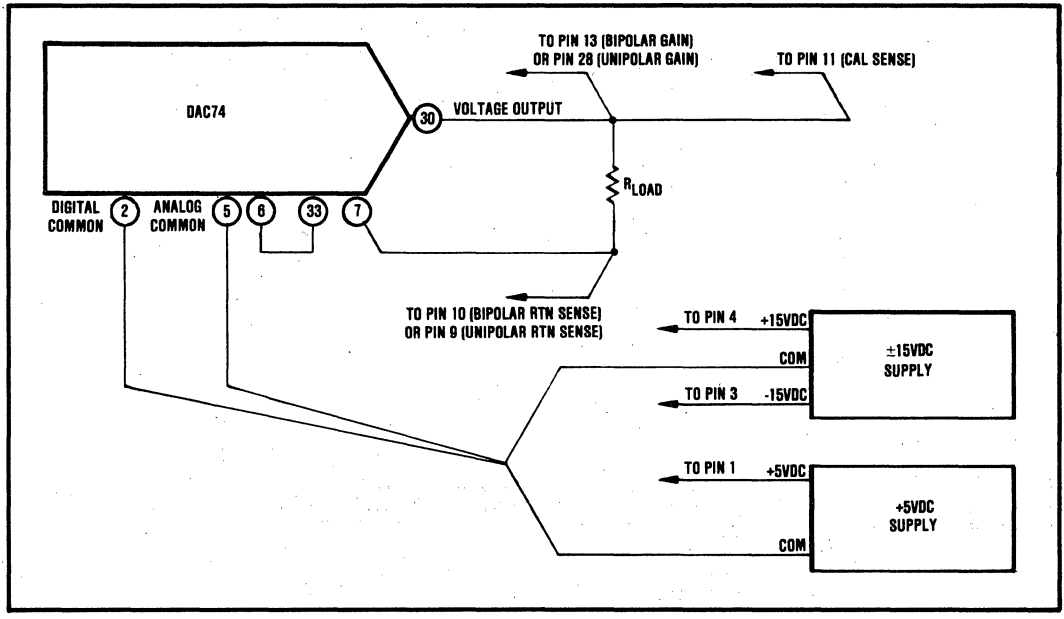


FIGURE 5. Power Supply and Common Connections.

Unipolar Connection. The output connections and jumpers are listed below. The pin numbers refer to the analog connector P3. The first five connections constitute the 5-wire connection to the load.

Connection	Purpose
30 to load (top)	DAC VOLTAGE OUTPUT Output connection to the load.
28 to load (top)	UNIPOLAR GAIN Output sense to the inverting input of the output amplifier. Sets unipolar range.
7 to load (bottom)	RTN Current return from the load. This return impedance must be low - equivalent of 16-gauge wire.
9 to load (bottom)	UNIPOLAR RETURN SENSE Return sense to the noninverting input of the output amplifier.
11 to load (top)	CAL SENSE Input to the error measurement circuit from the load.
33 to 6	RTN TO ANALOG COMMON Connect common returns. This jumper is essential to prevent damage to the internal reference.
23 to 34	-F.S. REF (ALL BITS OFF) Set minus full scale to 0 volts. Keep as short as possible.
29 to 34	BIPOLAR OFFSET TO RTN Maintain the same current drain on the +10 volt reference as bipolar connection.
26 to 25	+10V REF OUT TO +10V REF IN Keep as short as possible.
15 to 16	UNIPOLAR OFFSET TRIM TO OFFSET TRIM Connect offset trim to offset adjust input of the pedestal offset D/A converter.
17 to 25	UNIPOLAR GAIN TRIM (OFFSET DAC) to +10 VOLT REF Connect the full scale gain reference of pedestal offset D/A converter.
19 to 20	VOLTAGE OUT (OFFSET DAC) output to UNIPOLAR GAIN (OFFSET DAC) Return sense to inverting input of the pedestal offset D/A converter.
18 to digital common	UNIPOLAR CAL to DIGITAL COMMON Set software to unipolar mode.
31 to 25	+F.S. REF to +10V REF IN.

Bipolar Connection. The output connections and jumpers for bipolar operation are listed below. The pin numbers refer to the analog connector P3. The first five connections constitute the 5-wire connection to the load.

Connection	Purpose
30 to load (top)	DAC VOLTAGE OUTPUT Output connection to the load.
13 to load (top)	BIPOLAR GAIN Sense to the inverting input of the output amplifier. Sets bipolar range.
7 to load (bottom)	RTN Current return from the load. This return impedance must be low - equivalent of 1 foot 16-guage wire for 5mA output.
10 to load (bottom)	BIPOLAR RETURN SENSE Return sense to the noninverting input of the output amplifier.
11 to load (top)	CAL SENSE Input to the error measuring circuit from the load.
32 to 7	CMR to RTN Match the equivalent impedance to RTN for both inputs of output amplifier for the bipolar configuration.
7, 8, 33, 34	RTN Tied together internally.
33 to 6	RTN to ANALOG COMMON Connect common returns. This jumper is essential to prevent damage to the internal references

Connection	Purpose
23 to 22	-F.S. REF (ALL BITS OFF) to -10V REF OUT Set minus Full Scale to -10 volts. Keep as short as possible.
29 to 12	BIPOLAR OFFSET to CURRENT OUTPUT Bipolar offset for output amplifier.
26 to 25	+10V REF OUT to +10V REF IN Keep as short as possible.
16 to 25	OFFSET TRIM (OFFSET DAC) to +10V REFERENCE IN Connect bipolar offset of the pedestal offset D/A converter to +10V REF.
24 to 25	BIPOLAR GAIN TRIM (OFFSET DAC) to +10V REF Connect the Full Scale gain reference of the pedestal offset D/A converter.
19 to 21	VOLTAGE OUTPUT (OFFSET DAC) to BIPOLAR GAIN (OFFSET DAC) Return sense to inverting input of the pedestal offset D/A converter.
31 to 25	+F.S. REF to +10V REF IN.

Internally Connected Pins. The following pins are connected internally:

Function	Pin No.
DIGITAL COMMON	2, 12, 16, 17, 18, 19, 33
$+5V_{IN}$	1, 34
ANALOG COMMON	5, 6, 35, 36
$+15V_{IN}$	4, 37
$-15V_{IN}$	3, 38
RTN	7, 8, 33, 34

DIGITAL INPUTS

Data inputs D0 - D15 and enable inputs, ENMSB and ENLSB, are low power Schottky (74LS373). Control inputs $\overline{RES}$, RUN/$\overline{CAL}$ and $\overline{UNIPOLAR\ CAL}$ are standard TTL inputs. MPUOFF is a standard TTL input with a 10kΩ pullup resistor connected to +5V volts.

Timing specifications on the digital inputs are listed in the Specifications table and discussed in the Operation section.

OPERATION

DAC74 data inputs, control signals, and status lines are shown in Figure 6. MPUOFF will usually be tied to DIGITAL COMMON permitting the internal crystal ocsillator to run continuously. However, one may wish to control the oscillator to remove all possible sources of noise during D/A converter operation. MPUOFF must be asserted low 50msec before the $\overline{RES}$ pulse is asserted.

The $\overline{RES}$ line resets the calibration controller and starts controller operation when it returns high after being asserted low for at least 14μsec.

RUN/$\overline{CAL}$ is a mode control line. When high, RUN/$\overline{CAL}$ enables the controller to set up the SERVICE mode. In this mode, the user performs a coarse manual adjustment of the D/A converter. When RUN/$\overline{CAL}$ is low, the controller is informed to set up the SELF-CALIBRATION mode, the normal mode of operation.

Data input latches are level-triggered by ENSMB and ENLSB. These are used to strobe-in data from an 8-bit bus with D0 through D7 connected to D8 through D15 respectively. For 16-bit bus operation ENLSB can be permanently connected to +5V. Since all three latches are octal transparent latches (74LS373), their inputs may be transferred directly to their outputs by setting their respective enable inputs high. The table below indicates four common interfaces. A high input refers to a logic 1 input (2V to 3.5V) and a low input refers to a logic 0 input (0V to 0.8V).

Mode	ENMSB	ENLSB	Description
Transparent	High	High	Inputs are transferred directly to the MAIN D/A converter.
16-bit interface	Positive Pulse	High	All 16 bits are latched at the end of the ENMSB pulse.
8-bit interface	Low	Positive Pulse	Capture 8LSB's from the data bus in low byte buffer.
8-bit interface	Positive Pulse		Transfer 8MSB's from the data bus and transfer latched 8LSB's to the MAIN D/A converer at the end of the pulse.

The three-state output in the second rank of latches is disabled by $\overline{RUN}$, a status output signal, during the time the calibration controller has control of the main D/A converter.

INITIAL SETUP

It is necessary to trim the +10V and -10V reference as close to 10V as possible using the potentiometers located at the edge of the module. The procedure is described in Manual Calibration section.

It should not be necessary to manually adjust OFFSET, GAIN, and LINEARITY on units received from the factory. However, after a year or more of operation it may be necessary to adjust these parameters to within the range which can be trimmed by the self-calibration circuits. The manual adjustment procedure is described in the Manual Calibration section. It is important that either the load be connected or that a dummy load be switched in during calibration or adjustment.

Self-Calibration Mode

After power-up, a 1/2-hour warm-up period must be allowed. This permits the heated zener reference and other critical circuits to stabilize.

The next step is to initiate the SELF-CALIBRATION routine. Self-calibration is initiated by providing a pulse (low, 14μsec min) from the host equipment to the $\overline{\text{RES}}$ line. Self-calibration typically takes 2-1/2 seconds. $\overline{\text{CAL}}$ and $\overline{\text{RUN}}$ inform the user on the internal status of the calibration controller. The operation of these is best explained by a timing diagram, Figure 7.

Upon application of the reset pulse, $\overline{\text{CAL}}$ goes (or remains) low and goes high about 100μsec after $\overline{\text{RES}}$ is returned high. $\overline{\text{CAL}}$ remains high for 500μsec maximum. If it remains high, self-calibration has failed. If it goes low, self-calibration will be successful. The fact that calibration has failed means that either a noise transient has interferred with system operation or that the maximum correction factors have been used and that the main D/A converter connot be corrected to within specification. However, the converter will still operate. It will be necessary to perform manual adjustments described in the Manual Calibration section.

$\overline{\text{RUN}}$ goes high about 100μsec after the $\overline{\text{RES}}$ pulse returns high and remains high until all calibration controller operations are complete and control of the main D/A converter is returned to the digital data inputs. It is important to be aware of two facts during self-calibration: (1) the main D/A converter is being exercised, its output is moving and changing the voltage on the load; and (2) the three-state output enable of the main D/A converter input latches is held high by $\overline{\text{RUN}}$ thereby disconnecting the data inputs from the main D A converter.

Service Mode

Before one can manually adjust the GAIN, OFFSET and LINEARITY of the DAC74, it must be put in a mode called the SERVICE mode. This is accomplished by switching RUN/$\overline{\text{CAL}}$ high and asserting a pulse on the $\overline{\text{RES}}$ line. The result of going into this mode is that all corrections in the RAM are set to zero before control is returned to the user data input lines.

The timing is illustrated in Figure 7. $\overline{\text{CAL}}$ does not return low as it did in the SELF-CALIBRATION mode but remains high. $\overline{\text{RUN}}$ returns low indicating that control has been returned to the data inputs. $\overline{\text{RUN}}$ time is about 300msec. Manual calibration may proceed as described in the Manual Calibration section.

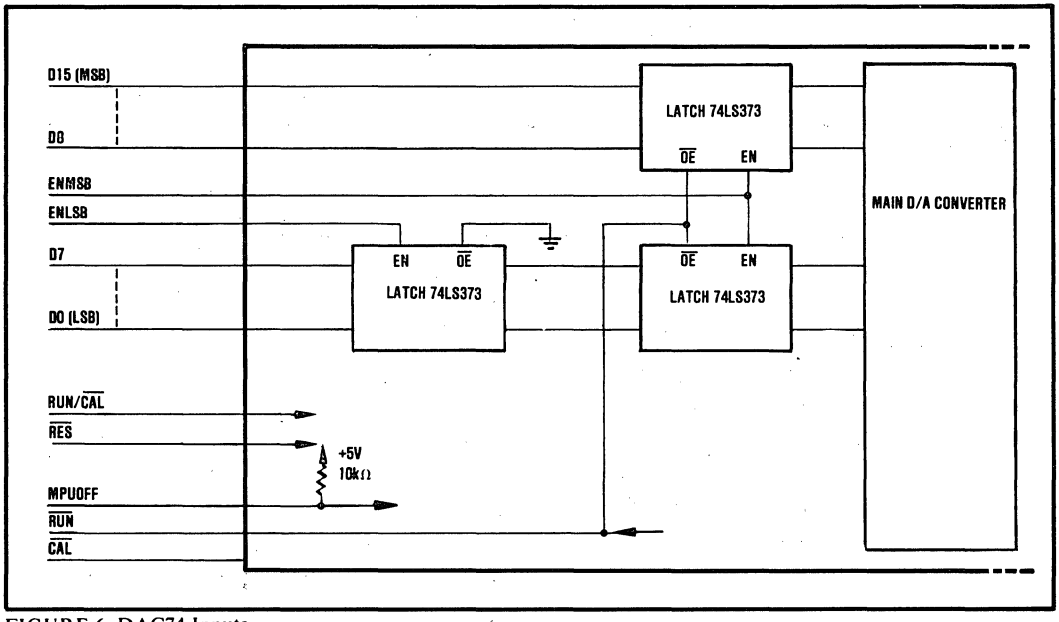


FIGURE 6. DAC74 Inputs.

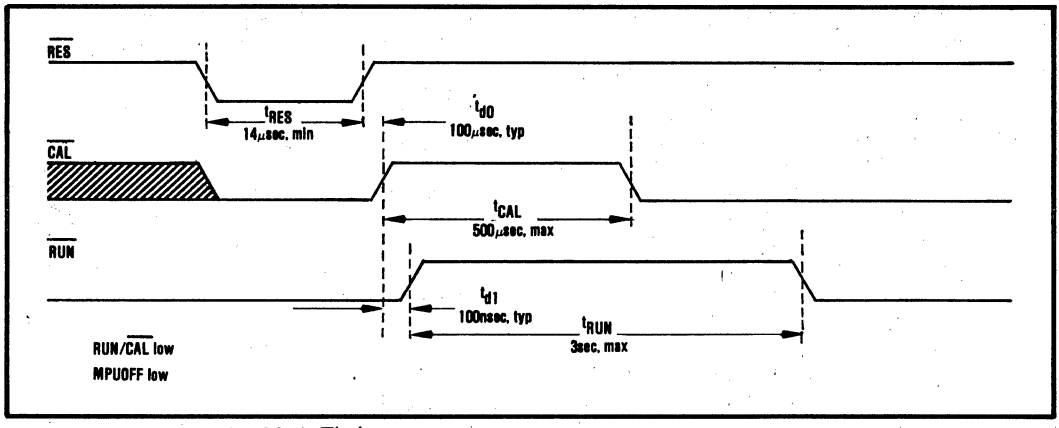


FIGURE 7. Self-Calibration Mode Timing.

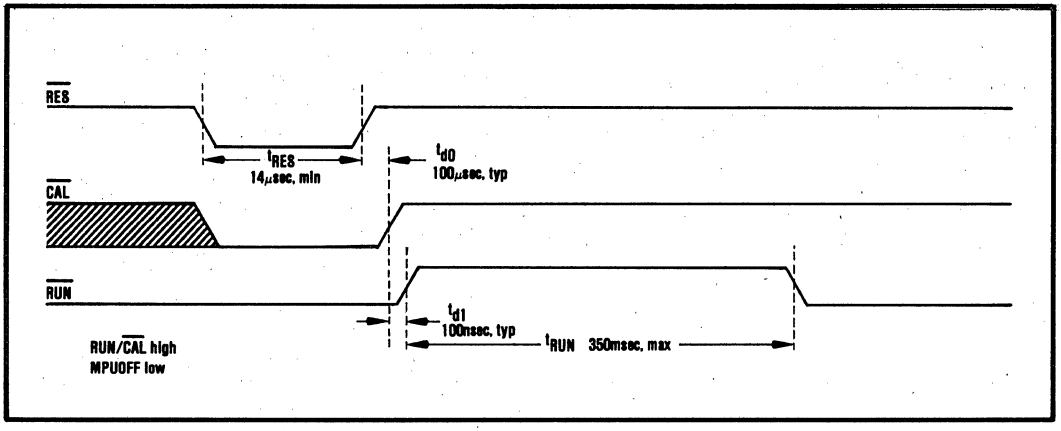


FIGURE 8. Service Mode Timing.

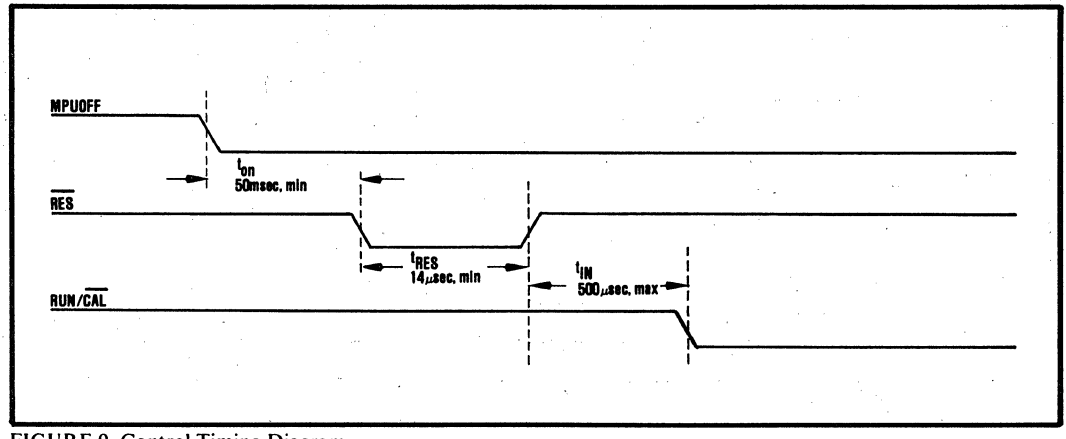


FIGURE 9. Control Timing Diagram.

Full Automatic Control

If the user wishes to automatically control the total operation of the DAC74 including the SERVICE mode as well as the SELF-CALIBRATION mode, additional timing considerations apply. An additional timing diagram is shown in Figure 8. Note that the MPUOFF must be asserted low 50msec before $\overline{RES}$ is asserted and the RUN/$\overline{CAL}$ must be asserted within 500μsec of the time that the $\overline{RES}$ pulse returns high.

MANUAL CALIBRATION

Manual adjustment of the DAC74 is accomplished by eight potentiometers located at one end of the package. Space for screwdriver access must be provided on the mounting surface. A label marked "REFER TO MANUAL BEFORE REMOVING LABEL" must be removed from the end of the package to access the potentiometers.

10V Reference Adjustment

After the DAC74 has been installed, the load connected, and a 1/2-hour warm-up period has elapsed, the references may be adjusted. The reference voltages should be set to 10V, ±10μV.

A 6-1/2 digit voltmeter, which has been calibrated as accurately as possible may be used to adjust the reference and coarse calibrate the D/A converter.

ADJUSTMENT PROCEDURE

1. Connect the voltmeter between the +10V REF OUT pin (26) and an ANALOG COMMON pin (5, 6, 35, 36). Adjust the +10V REF potentiometer to obtain a reading of 10.00000V, ±10μV.
2. Connect the voltmeter to the -10V REF OUT pin (22) and adjust the -10V REF potentiometer to read -10.00000V, ±10μV. Needed for bipolar only.

Note: If these reference voltages are to be used to provide references to other circuits, those loads must be connected before the above adjustments are made. External reference loads must remain constant for accurate operation of the DAC74.

Coarse Calibration of the Main D/A Converter.

The self-calibration controller can correct main D/A errors within a limited range. If the gain, offset or linearity shift due to initial installation environment, such as load return wire voltage drops, power supply voltage line regulation, or component aging, a manual coarse adjustment will be necessary. These six adjustments are made using potentiometers at the edge of the DAC74 package.

Coarse adjustments bring the errors of the DAC74 to within the operating range of the self-calibration circuit. It is sufficient to adjust the DAC74 output to within norminal values.

ADJUSTMENT PROCEDURE

After the DAC74 had been installed, the load connected, a 1/2-hour warm-up period has elapsed, and the reference voltages have been set, manual calibration may proceed.

Put the DAC74 into the SERVICE mode as described in the Service Mode section.

Adjustments will be made in the following order: OFFSET, preliminary GAIN, 4MSB's (LINEARITY), and final GAIN. Output voltage readings will be different for bipolar and unipolar configurations. Table I shows the data word to be strobed into DAC74, the potentiometer to be adjusted, and the output reading to be attained for unipolar and bipolar configurations.

After these adjustments are made, put the DAC74 in the SELF-CALIBRATION mode as described in the Self-Calibration Mode section. The DAC74 is now ready for normal operation.

TABLE I. Calibration Voltages.

Step	Data Input Word (hex)	Adjust Poteniometer	D/A Output Reading	
			Unipolar	Bipolar
1	0000	OFFSET	0.0000V,±50μV	-10.0000V,±100μV
2	0800	GAIN	0.3125V,±50μV	-9.3750V,±100μV
3	1000	D12	0.6250V,±50μV	-8.7500V,±100μV
4	2000	D13	1.2500V,±50μV	-7.5000V,±100μV
5	4000	D14	2.5000V,±50μV	-5.0000V,±100μV
6	8000	D15	5.0000V,±50μV	0.0000V,±100μV
7	FFFF	GAIN	9.99985V,±50μV	-9.9997V,±100μV

OPERATIONAL CHECKLIST

1. Be sure that all pins and jumpers are connected properly as discussed and illustrated in the Installation section. Careful layout and shielding is necessary to keep digital noise out of the analog circuits.
2. The load return line from the load to RTN (pin 7, P3) must have less than 20μV voltage drop across its length for proper operation. See Installation section.
3. Be sure and wait about 1 2-hour for warm-up.
4. Check power supply voltages at the module pins.
   +15V and -15V, ±0.5V
   +5V, ±0.25V
5. Check +12V and -12V voltages generated internally.
   +12V, ±0.6V pin 39, P3
   -12V, ±0.6V pin 40, P3
6. Check +10V and -10V references. The D/A converter accuracy is directly dependent on these voltages. See Adjustment Procedure in the Manual Calibration section.
   +10.00000V, ±10μV pin 26, P3
   -10.00000V, ±10μV pin 22, P3
7. Check MPUOFF (pin 14, P3) to be sure it is low. It must be low for at least 50msec before attempting self-calibration.
8. Be sure $\overline{UNIPOLAR\ CAL}$ (pin 18, P3) is high for bipolar operation or low for unipolar operation.
9. $\overline{RES}$ pulse must be at least 14μsec wide.
10. If $\overline{CAL}$ status does not return low during an automatic self-calibration, the D/A converter may be out of tolerance. Adjust it using the procedure in the Manual Calibration section. An unsuccessful self-calibration can result from a voltage or current transient in the D/A converter system. Attempt a second self-calibration.

BURR-BROWN®

DAC80
DAC80P

Monolithic 12-Bit DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- INDUSTRY STANDARD PINOUT
- LOW POWER DISSIPATION: 345mW
- FULL ±10V SWING WITH V_{CC} = ±12VDC
- DIGITAL INPUTS ARE TTL- AND CMOS-COMPATIBLE
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES
- SINGLE-CHIP DESIGN
- ±1/2LSB MAXIMUM NONLINEARITY, 0°C to +70°C
- GUARANTEED MONOTONICITY, 0°C to +70°C
- TWO PACKAGE OPTIONS: Hermetic side-brazed ceramic and low-cost molded plastic
- SETTLING TIME: 4μs max to ±0.01% of Full Scale

DESCRIPTION

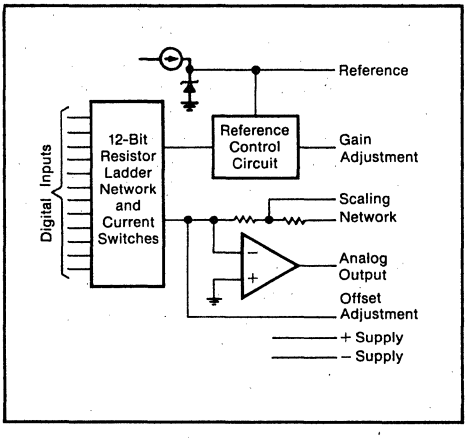
This monolithic digital-to-analog converter is pin-for-pin equivalent to the industry standard DAC80, first introduced by Burr-Brown. Its single-chip design includes the output amplifier and provides a highly stable reference capable of supplying up to 2.5mA to an external load without degradation of D/A performance.

This converter uses proven circuit techniques to provide accurate and reliable performance over temperature and power supply variations. The use of a buried zener diode as the basis for the internal reference contributes to the high stability and low noise of the device. Advanced methods of laser trimming result in precision output current and output amplifier feedback resistors, as well as low integral and differential linearity errors. Innovative circuit design enables the DAC80 to operate at supply voltages as low as ±11.4V with no loss in performance or accuracy over any range of output voltage. The lower power dissipation of this 118-mil by 121-mil chip results in higher reliability and greater long term stability.

Burr-Brown has further enhanced the reliability of the monolithic DAC80 by offering a hermetic, side-brazed, ceramic package. In addition, ease of use has been enhanced by eliminating the need for a +5V logic power supply.

For applications requiring both reliability and low cost, the DAC80P in a molded plastic package offers the same electrical performance over temperature as the ceramic model. The DAC80P is available with either voltage or current output.

For designs that require a wider temperature range, see Burr-Brown models DAC85H and DAC87H. For designs that require complementary coded decimal inputs, see Burr-Brown model DAC80-CCD-V (-I).



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

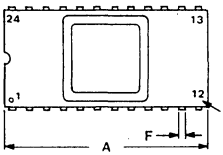
Typical at +25°C and ±V_{CC} = 12V or 15V unless otherwise noted.

MODEL	DAC80			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT				
Resolution			12	Bits
Logic Levels (0°C to +70°C)[1]:				
V_{IH} (Logic "1")	+2		+16.5	VDC
V_{IL} (Logic "0")	0		+0.8	VDC
I_{IH} (V_{IN} = +2.4V)			+20	µA
I_{IL} (V_{IN} = +0.4V)			−180	µA
ACCURACY (at +25°C)				
Linearity Error		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	±3/4	LSB
Gain Error[2]		±0.1	±0.3	%
Offset Error[2]		±0.05	±0.15	% of FSR[3]
DRIFT (0°C to +70°C)[4]				
Total bipolar drift (includes gain, offset, and linearity drifts)		±10	±25	ppm of FSR/°C
Total Error Over 0°C to +70°C[5]				
Unipolar		±0.06	±0.15	% of FSR
Bipolar		±0.06	±0.12	% of FSR
Gain: Including Internal Reference		±10	±30	ppm/°C
Excluding Internal Reference		±5	±10	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	±3/4	LSB
Linearity Error 0°C to +70°C		±1/4	±1/2	LSB
Monotonicity Guaranteed	0		+70	°C
CONVERSION SPEED, V_{OUT} models				
Settling Time to ±0.01% of FSR				
For FSR change (2kΩ || 500pF load)				
with 10kΩ Feedback		3	4	µs
with 5kΩ Feedback		2	3	µs
For 1LSB Change		1		µs
Slew Rate	10			V/µs
CONVERSION SPEED, I_{OUT} models				
Settling Time to ±0.01% of FSR				
For FSR change: 10Ω to 100Ω load		300		ns
1kΩ load		1		µs
ANALOG OUTPUT, V_{OUT} models				
Ranges	±2.5, ±5, ±10, +5, +10			V
Output Current[6]	±5			mA
Output Impedance (DC)		0.05		Ω
Short Circuit to Common, Duration[7]		Indefinite		
ANALOG OUTPUT, I_{OUT} models				
Ranges: Bipolar	±0.96	±1.0	±1.04	mA
Unipolar	−1.96	−2.0	−2.04	mA
Output Impedance: Bipolar	2.6	3.2	3.7	kΩ
Unipolar	4.6	6.6	8.6	kΩ
Compliance	−2.5		+2.5	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6.30	+6.37	V
External Current (constant load)			2.5	mA
Drift vs Temperature		±10	±20	ppm/°C
Output Impedance		1		Ω
POWER SUPPLY SENSITIVITY				
V_{CC} = ±12VDC or ±15VDC		±0.002	±0.006	% FSR/ % V_{CC}
POWER SUPPLY REQUIREMENTS				
±V_{CC}	±11.4		±16.5	VDC
Supply Drain (no load): +V_{CC}		8	12	mA
−V_{CC}		15	20	mA
Power Dissipation (V_{CC} = ±15VDC)		345	480	mW
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating	−25		+85	°C
Storage: Plastic DIP	−60		+100	°C
Ceramic DIP	−65		+150	°C

NOTES: (1) Refer to "Logic Input Compatibility" section. (2) Adjustable to zero with external trim potentiometer. (3) FSR means full scale range and is 20V for ±10V range, 10V for ±5V range for V_{OUT} models; 2mA for I_{OUT} models. (4) To maintain drift spec, internal feedback resistors must be used. (5) Includes the effects of gain, offset and linearity drift. Gain and offset errors externally adjusted to zero at +25°C. (6) For ±V_{CC} less than ±12VDC, limit output current load to ±2.5mA to maintain ±10V full scale output voltage swing. For output range of ±5V or less, the output current is ±5mA over entire ±V_{CC} range. (7) Short circuit current is 40mA, max.

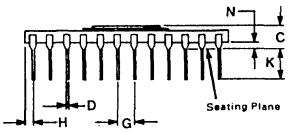
MECHANICAL

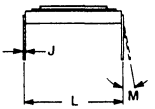
Hermetic Ceramic 24-Lead DIP



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	–	10°	–	10°
N	.025	.060	0.64	1.52

PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

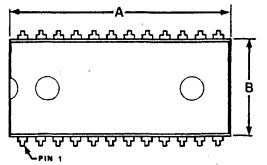
HERMETICITY: Conforms to Method 1014, Condition A1 or A2 (fine leak) and Condition C (gross leak). Metal lid of package is connected to −V_{CC} internally.

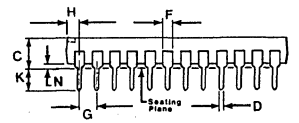
CASE: Ceramic

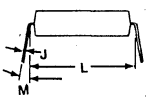
MATING CONNECTOR: 0245MC

WEIGHT: 4.1 grams (0.15 oz.)

Molded Plastic 24-Lead DIP







NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.233	1.283	31.32	32.59
B	.538	.575	13.67	14.61
C	.160	.224	4.29	5.70
D	.016	.023	0.38	0.58
F	.043	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

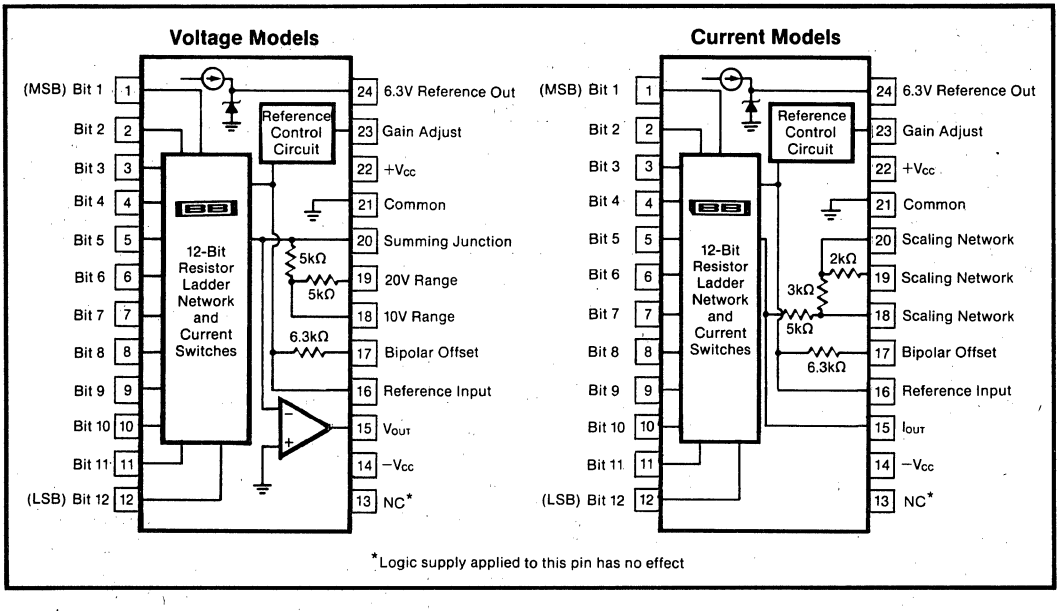
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CASE: Plastic

MATING CONNECTOR: 0245MC

WEIGHT: 3.7 grams (0.13 oz.)

FUNCTIONAL DIAGRAM AND PIN ASSIGNMENTS



*Logic supply applied to this pin has no effect

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC80 accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB, or CTC (see Table I).

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB ↓ LSB ↓	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
000000000000	+Full Scale	+Full Scale	-1LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	1/2 Full Scale -1LSB	-1LSB	-Full Scale
111111111111	Zero	-Full Scale	Zero

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

ORDERING INFORMATION

Model	Output	Package
DAC80-CBI-I	Current	Ceramic
DAC80-CBI-V	Voltage	Ceramic
DAC80P-CBI-I	Current	Plastic
DAC80P-CBI-V	Voltage	Plastic
DAC80Z-CBI-I*	Current	Ceramic
DAC80Z-CBI-V*	Voltage	Ceramic

*DAC80Z is not recommended for new designs; both standard DAC80 and DAC80P now operate over extended power supply range.

ABSOLUTE MAXIMUM RATINGS

+Vcc to Common	0V to +18V
−Vcc to Common	0V to −18V
Digital Data Inputs to Common	−1V to +18V
Reference Output to Common	±Vcc
Reference Input to Common	±Vcc
Bipolar Offset to Common	±Vcc
10V Range R to Common	±Vcc
20V Range R to Common	±Vcc
External Voltage to DAC Output	−5V to +5V
Lead Temperature, Soldering	+300°C, 10s
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}: Plastic DIP	100°C/W
Ceramic DIP	65°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC80 model at 0°C, +25°C and +70°C; 2) calculating the gain error with respect to the 25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

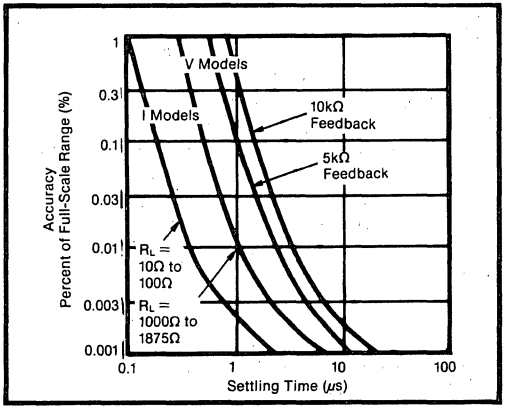


FIGURE 1. Full Scale Range Settling Time vs Accuracy.

Voltage Output Models

Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111 . . . 11 to 1000 . . . 00), the point at which the worst case settling time occurs.

Current Output Models

Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω to 1875Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000Ω to 1800Ω for output voltage range of ±1V and 0 to −2V (see Figures 11 and 12).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage range of ±1V and 0 to −2V. (See Figures 11 and 12).

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages (see Figure 2).

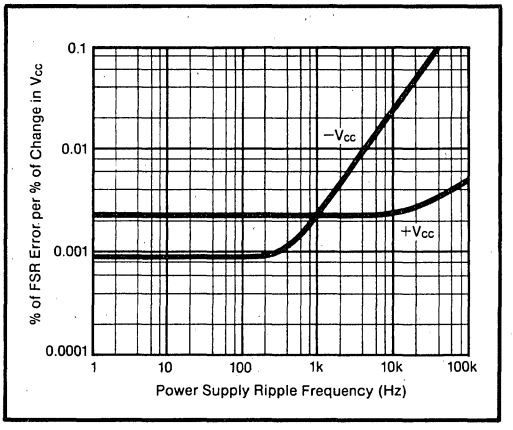


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 2.5mA.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

LOGIC INPUT COMPATIBILITY

DAC80 digital inputs are TTL, LSTTL and 4000B, 54/74HC CMOS compatible. The input switching threshold remains at the TTL threshold over the entire supply range.

Logic "0" input current over temperature is low enough to permit driving DAC80 directly from outputs of 4000B and 54/74C CMOS devices.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Connect power supply voltages as shown in Figure 3. For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown. These capacitors (1μF tantalum) should be located close to the DAC80.

±12V OPERATION

All DAC80 models can operate over the entire power supply range of ±11.4V to ±16.5V. Even with supply levels dropping to ±11.4V, the DAC80 can swing a full ±10V range, provided the load current is limited to ±2.5mA. With power supplies greater than ±12V, the DAC80 output can be loaded up to ±5mA. For output swing of ±5V or less, the output current is ±5mA, min. over the entire V_{CC} range.

No bleed resistor is needed from +V_{CC} to pin 24, as was needed with prior hybrid Z versions of DAC80. Existing ±12V applications that are being converted to the monolithic DAC80 must omit the resistor to pin 24 to insure proper operation.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted.

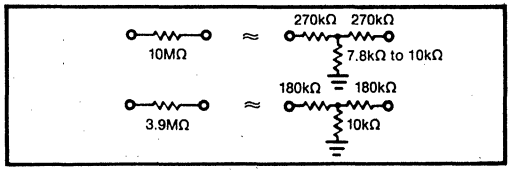


FIGURE 4. Equivalent Resistances.

Existing applications that are converting to the monolithic DAC80 must change the gain trim resistor on pin 23 from 33MΩ to 10MΩ to insure sufficient adjustment range. Pin 23 is a high impedance point and a 0.001μ1F to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figure 5 for relationship of Offset and Gain adjustments to unipolar and bipolar D/A operation.

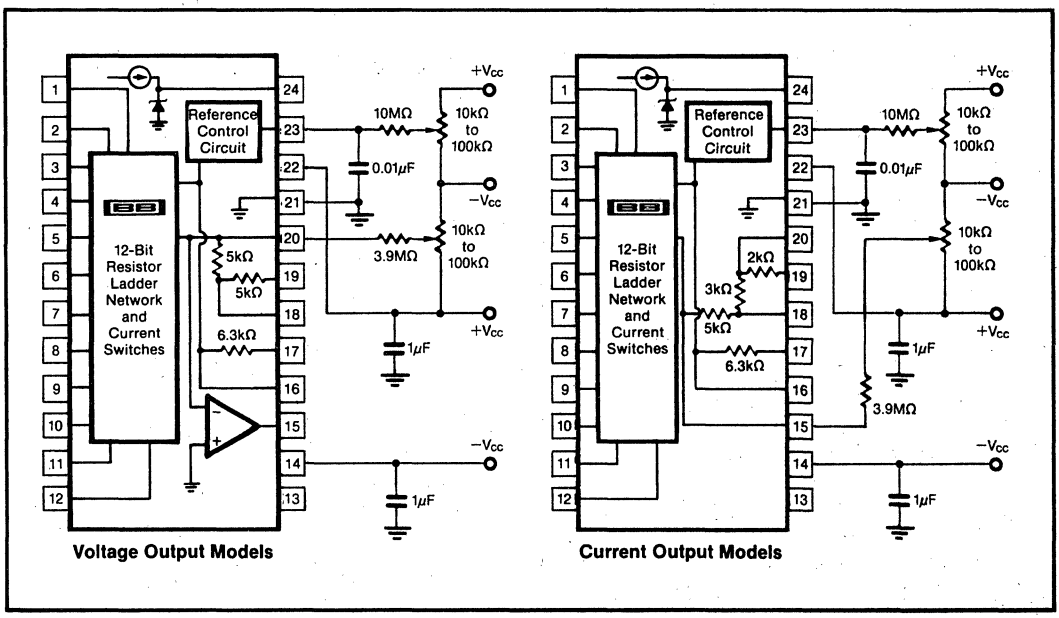


FIGURE 3. Power Supply and External Adjustment Connection Diagrams

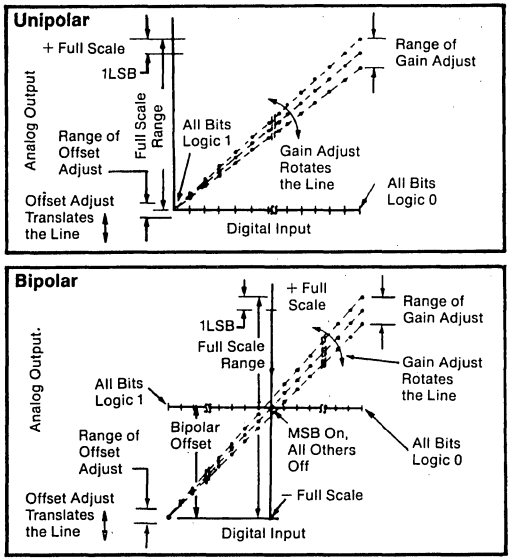


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar and Bipolar D/A Converter.

Offset Adjustment

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table II for corresponding codes.

TABLE II. Digital Input/Analog Output.

DIGITAL INPUT	ANALOG OUTPUT			
	VOLTAGE *		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output. Adjust the Gain potentiometer for this positive full scale output. See Table II for positive full scale voltages and currents.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

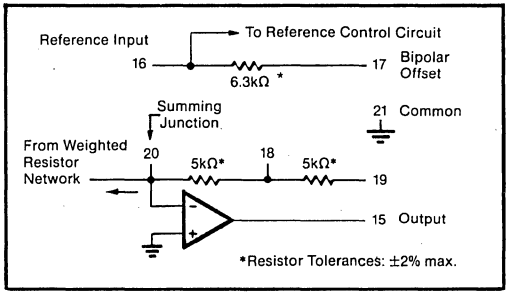


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other internal device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full-scale range change is specified as 4μs for the 20V range and 3μs for the 10V range.

TABLE III. Output Voltage Range Connections for Voltage Models.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

CURRENT OUTPUT MODELS

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.

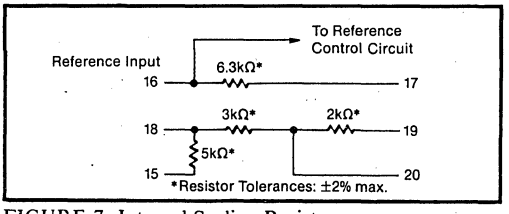


FIGURE 7. Internal Scaling Resistors.

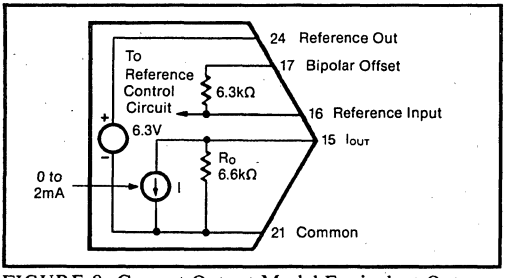


FIGURE 8. Current Output Model Equivalent Output Circuit.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving An External Op Amp

The current output model DAC80 will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage. See Figure 9.

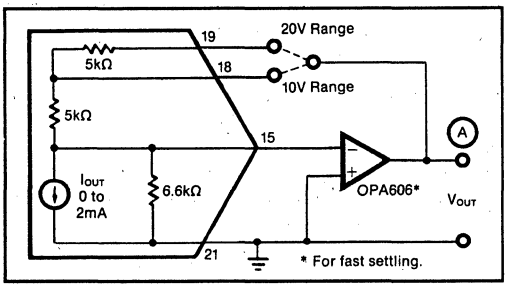


FIGURE 9. External Op-Amp—Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges. See Figure 10. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C plus R_F drift to total drift.

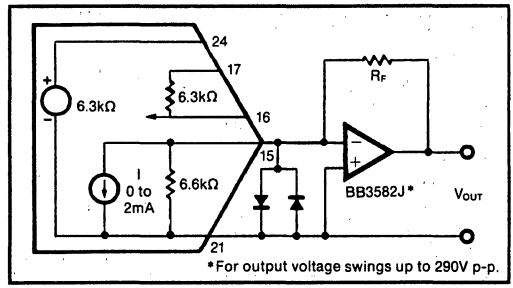


FIGURE 10. External Op-Amp—Using External Feedback Resistors.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 11 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA\ [(R_L \times R_O) \div (R_L + R_O)]$$

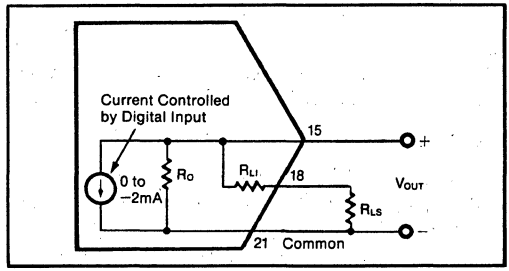


FIGURE 11. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

The unipolar output impedance R_O equals 6.6kΩ (typ) and R_{LI} is the internal load resistance of 968Ω (derived by connecting pin 15 to pin 20 and pin 18 to 19). By choosing $R_{LS} = 210\Omega$, $R_L = 1178\Omega$. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of 0 to −2V. Since R_O is not exact, initial trimming per Figure 3 may be necessary; also R_{LS} may be trimmed.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 12, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA\ [(R_O \times R_L) \div (R_O + R_L)]$$

By connecting pin 17 to 15, the output current becomes bipolar (±1mA) and the output impedance R_O becomes 3.2kΩ (6.6kΩ in parallel with 6.3kΩ). R_{LI} is 1200Ω (derived by connecting pin 15 to 18 and pin 18 to 19). By choosing $R_{LS} = 255\Omega$, $R_L = 1455\Omega$. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of ±1V. As indicated above, trimming may be necessary.

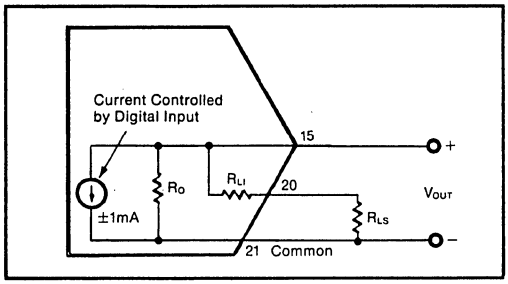


FIGURE 12. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

BURR-BROWN®

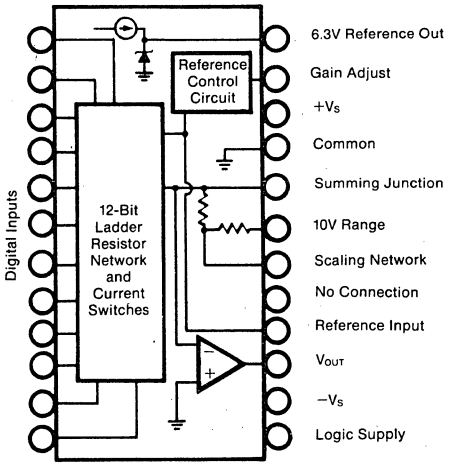
DAC80-CCD

Integrated Circuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 3-DIGIT RESOLUTION
- COMPLETE WITH INTERNAL REFERENCE AND OUTPUT AMPLIFIER (V MODELS)
- FAST SETTLING: 300ns to ±0.01% (I MODELS)
- WIDE POWER SUPPLY RANGE MODELS AVAILABLE (Z MODELS)
- CERAMIC DUAL-IN-LINE PACKAGE

Voltage Model



DESCRIPTION

Use this popular 3-digit digital-to-analog converter for low cost precision performance applications.

DAC80, with internal reference and optional output amplifier, offers a maximum nonlinearity error of ±0.012%, ±30ppm/°C maximum gain drift, and monotonicity—all over a 0°C to +70°C operating range. Total accuracy drift is guaranteed to be less than ±25ppm/°C.

Packaged within DAC80's 24-pin dual-in-line ceramic case are fast-settling switches and stable, laser-trimmed thin-film resistors. Voltage output models settle to ±0.05% of FSR in 3μs for a 10V step change.

By specifying the DAC80Z model with a supply range of ±11.4V to ±16.0V, you can use this proven D/A converter in microprocessor and semiconductor memory systems.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

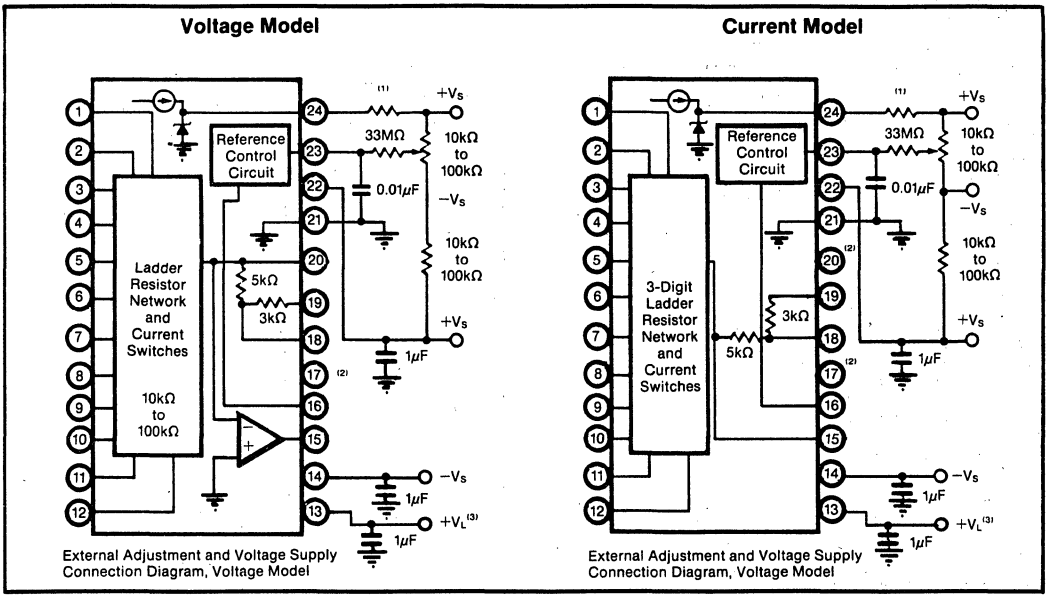
ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	DAC80-CCD			
	MIN	TYP	MAX	UNITS
DIGITAL INPUT				
Resolution			3	Digits
Logic Levels (TTL compatible)[1]: Logic "1" (+40μA max at +5.0V)	+2.4		+5.0	VDC
Logic "0" (1.6mA max at +0.4V)	0		+0.4	VDC
ACCURACY				
Linearity Error at 25°C		±1/8	±1/4	LSB[2]
Differential Linearity Error		±1/4	±1/2	LSB
Gain Error[3]		±0.1	±0.3	%
Offset Error[3]		±0.05	±0.15	% of FSR[4]
Monotonicity Temp. Range, min	0		+70	°C
DRIFT[5] (0°C to +70°C)				
Total drift, max (includes gain, offset, and linearity drifts)			±25	ppm of FSR/°C
Total error over 0°C to +70°C[6]		±0.08	±0.15	% of FSR
Gain		±15	±30	ppm/°C
Exclusive of internal reference			±10	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	+1, −7/8	LSB
Linearity Error 0°C to +70°C			±1/2	LSB
CONVERSION SPEED (V MODELS)				
Settling Time to ±0.01% of FSR: For FSR Change with 8kΩ Feedback		5		μs
For 1LSB Change		1.5		μs
Slew Rate	10	20		V/μs
CONVERSION SPEED (I MODELS)				
Settling Time to ±0.01% of FSR				
For FSR Change: 10Ω to 100Ω Load		300		ns
1kΩ Load		1		μs
ANALOG OUTPUT (V MODELS)				
Range[7]		0 to +10		V
Output Current	5			mA
Output Impedance (DC)		0.05		Ω
Short Circuit Duration		Indefinite to Common		
ANALOG OUTPUT (I MODELS)				
Range		0 to −1.25		mA
Output Impedance, Unipolar		15.6		kΩ
Compliance			±2.5	V
INTERNAL REFERENCE VOLTAGE		+6.3		V
Maximum External Current[8]			±200	μA
Tempco of Drift, max		±10	±20	ppm/°C
POWER SUPPLY SENSITIVITY				
+15V Supply		±0.02		% of FSR/% V_S
−15V and +5V Supplies		+0.002		% of FSR/% V_S
POWER SUPPLY REQUIREMENTS				
DAC80	±14, +4.75	±15, +5	±16, +16	VDC
DAC80Z[7]	±11.4, +4.75	±12, +5	±16, +16	VDC
Supply Drain: ±15V/±12V (including 5mA load)		±25	±35	mA
+5V (logic supply)		+20	+30	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating (double above specs)	−25		+85	°C
Storage	−55		+100	°C

NOTES: (1) Adding external CMOS hex buffers CD 4009A will provide CMOS input compatibility. (2) LSB is based on 3-digit or 10-bit resolution. (3) Adjustable to zero with external trim potentiometer. (4) FSR means "Full Scale Range" and is 10V. (5) To maintain drift spec, internal feedback resistor must be used for current output models. (6) With gain and offset errors adjusted to zero at +25°C. (7) DAC80Z supply range is ±12.0V min to ±16.0V max for 0 to +10V output. (8) Maximum with no degradation of specifications.

CONNECTION DIAGRAMS

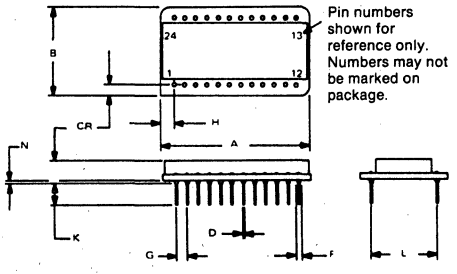


External Adjustment and Voltage Supply Connection Diagram, Voltage Model

External Adjustment and Voltage Supply Connection Diagram, Voltage Model

NOTES: (1) This resistor is required only for Z models (see "Operating Instructions"). Make no connection to power supply on non-Z models. (2) No internal connection. (3) Pin 13 can be connected to +Vs; power dissipation will increase 200mW.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

CASE: Ceramic

MATING CONNECTOR: 245MC

PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

WEIGHT: 8.4 grams (0.3 oz.)

HERMETICITY: Conforms to method 1014, condition C, step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

PIN ASSIGNMENTS

I Models	Pin	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)
Logic Supply	13	Logic Supply
−Vs	14	−Vs
IOUT	15	VOUT
Reference Input	16	Reference Input
No Connection	17	No Connection
Scaling Network	18	Scaling Network
Scaling Network	19	10V Range
No Connection	20	Summing Junction
Common	21	Common
+Vs	22	+Vs
Gain Adjust	23	Gain Adjust
6.3V Reference Out	24	6.3V Reference Out

ORDERING INFORMATION

Model	Supply Range (V)	Output
DAC80-CCD-V	±14 to ±16	Voltage
DAC80Z-CCD-V	±11.4 to ±16	Voltage
DAC80-CCD-I	±14 to ±16	Current

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC80-CCD-V (or -I) produce the analog outputs given in Table I for the indicated digital inputs.

TABLE I. Digital Input Codes.

Digital Input	Analog Output
MSB LSB	CCD Complementary Coded Decimal—3 Digits
0110 0110 0110	Full Scale
1111 1111 1111	Zero

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points of Table I over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by:

1. testing the end point differences for each DAC80 model at 0°C, +25°C and +70°C;
2. calculating the gain error with respect to the 25°C value and;
3. dividing by the temperature change.

This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

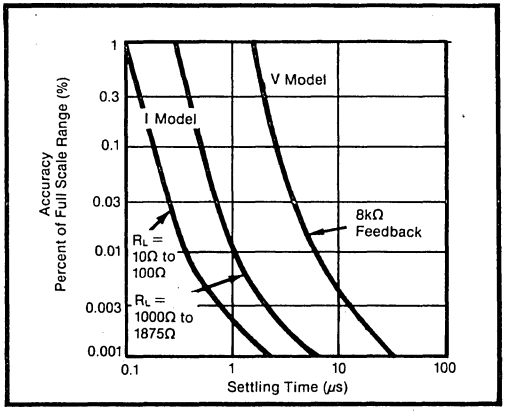


FIGURE 1. Full Scale Range Settling Time vs Accuracy.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage swing permitted without damage to the DAC80 is ±5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

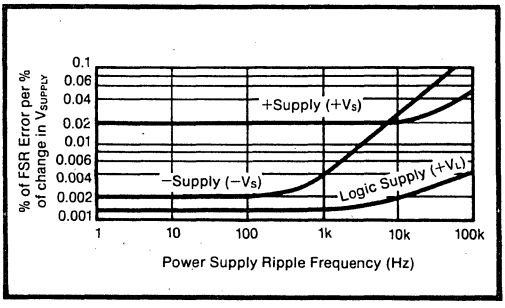


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±5% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 200μA. An external buffer amplifier is recommended if this reference will be used to drive other system components.

OPERATING INSTRUCTIONS

±12V SUPPLY OPERATION

The Z models will operate with supply voltages as low as ±11.4V. For operation with supplies less than ±14V, an external resistor must be connected between the positive supply and pin 24. This provides additional current required by the internal reference. The required resistor value for supply voltages of ±11.4V to ±12.6V is 2.0kΩ and for supplies of ±12.6V to ±14V is 3.9kΩ. For supplies in the range ±14V to ±16V, no resistor is required.

It is recommended that an output voltage range of 0 to +10V not be used with the Z model if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{SUPPLY}| - |V_{OUT}\ max| < 2.0V$ Except for operation at lower supply voltages, the DAC80Z and DAC80 operation is identical.

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC80. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiomters. Conect these potentiometers as shown in the connection diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 33MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in each case. The Gain Adjust (pin 23) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figure 4 for relationship of Offset and Gain adjustments to D/A converter output.

Offset Adjustment: For the unipolar CCD configuration, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

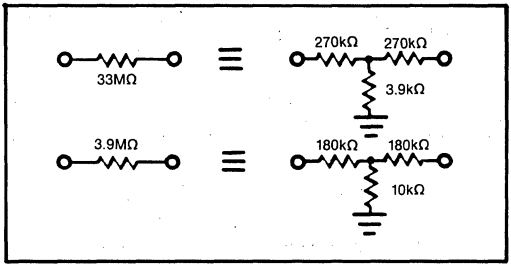


FIGURE 3. Equivalent Resistance.

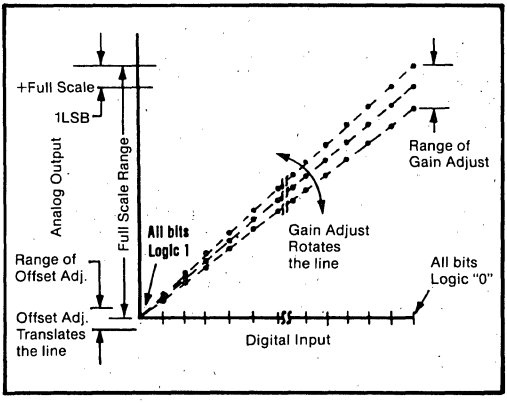


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

Gain Adjustment: Apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagrams for gain adjustment connections.

TABLE II. Digital Input/Analog Output.

Digital Input	Analog Output	
	0 to +10V	0 to −2mA
3-Digit Resolution MSB LSB		
0110 0110 0110	+9.990V*	−1.249mA
0110 0110 1111	+9.9900V	−1.238mA
0110 1111 1111	+9.000V	−1.125mA
1111 1111 1111	0.000V	0.000mA
One LSB	10.00mV	1.25μA

*To obtain values for other binary (CBI) ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.
*Normal Full Scale Range with correct codes; output can go higher if illegal codes are applied.

VOLTAGE OUTPUT MODELS

OUTPUT RANGE CONNECTIONS

An output of 0 to +10V is derived from voltage output models by connecting pin 15 to pin 18. Also connect pin 16 to pin 24 to connect the internal reference.

Thermal tracking of the internal scaling resistors with other devices in the DAC80 minimizes output drift versus temperature.

CURRENT OUTPUT MODELS

The equivalent output circuit and resistive scaling network of the current model differ from the voltage model and are shown in Figures 5 and 6. Instructions for using the DAC80-I with a resistor or an external op amp follow. External R_{LS} or R_{LP} resistors are required to produce exactly 0 to −2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

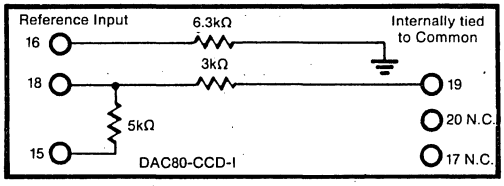


FIGURE 5. Internal Scaling Resistors.

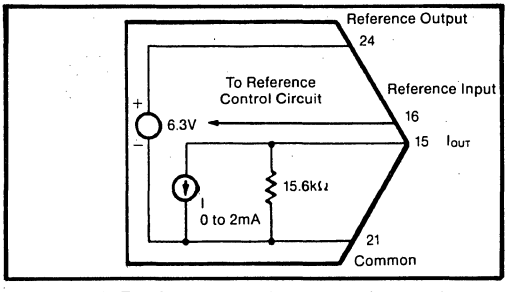


FIGURE 6. DAC80 Current Model Equivalent Output Circuit.

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to −2V. These resistors (R_{LI}) are an integral part of the DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

TABLE III. DAC80-CCD-I Resistive Load Connections.

Digital Input Code	Output Range	Internal Resistance, R_{LI}	1% Metal Film External Resistance, R_{LP}	R_{LI} Connections		Reference	External Load, R_{LP}
				Connect Pin 15 to	Connect Pin 18 to	Connect Pin 16 to	
CCD	0 to −2V	1.875kΩ	36.5kΩ	19	Common (21)	24	Between pins 15 and 21

DRIVING A RESISTIVE LOAD UNIPOLAR

Connect the internal scaling resistors as shown in Table III and add an external metal film resistor (R_{LP}) in parallel as shown in Figure 7 to obtain a 0 to −2V full scale output voltage range for CCD input codes:

With $R_L = (R_{LI} \times R_{LP}) \div (R_{LI} + R_{LP}) = 1.78k\Omega$

$$V_{OUT} = -1.25mA \times \frac{15.6k\Omega \times R_L}{15.6k\Omega + R_L} = -2.0V$$

If $R_{LP} = \infty$, $V_{OUT} = -2.0V$.

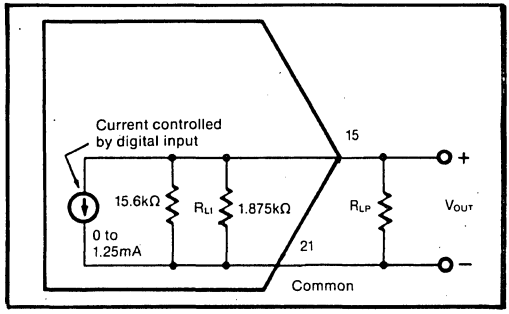


FIGURE 7. DAC80-CCD-I Connected for Voltage Output with Resistive Load.

DRIVING AN EXTERNAL OP AMP

The current model DAC80 will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage. See Figure 8.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model, DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Figure 8.

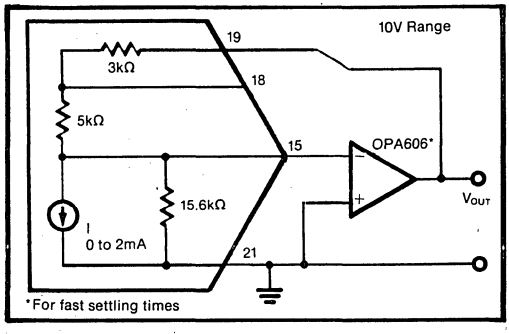


FIGURE 8. External Op Amp Using Internal Feedback Resistors.

BURR-BROWN®

DAC82

8-BIT DIGITAL-TO-ANALOG CONVERTER

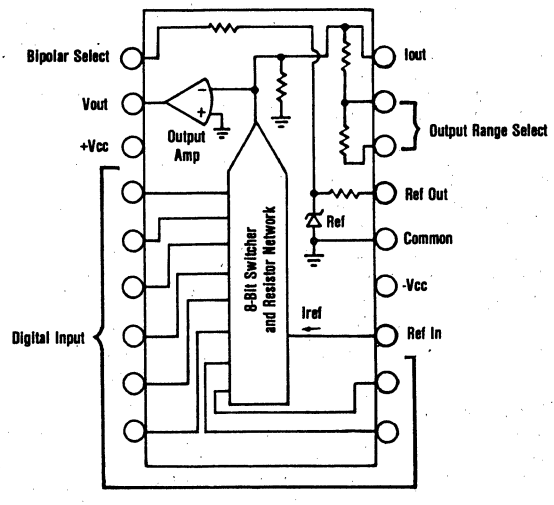
FEATURES

- 8-BIT RESOLUTION/LINEARITY
- NO EXTERNAL ADJUSTMENTS REQUIRED FOR ±1LSB ACCURACY
- INTERNAL REFERENCE AND SCALING RESISTORS
- 2-QUADRANT MULTIPLYING WITH EXTERNAL REFERENCE
- HERMETIC, DUAL-IN-LINE PACKAGE
- OPERATION OVER −55°C TO +125°C

DESCRIPTION

The DAC82 is an 8-bit digital-to-analog converter with voltage and current outputs. Packaged in an 18-pin metal DIP, it is complete with its own internal reference and scaling resistors. When used with a variable, external reference, the DAC82 will multiply in two quadrants. Two versions are available: the DAC82BM (-25°C to +85°C) and the DAC82SM (-55°C to +125°C). Both offer ±1LSB absolute accuracy at room temperature with no external adjustments required and nonlineaity is guaranteed to be within ±1/2LSB over the specified temperature ranges. The small size of the DAC82 makes it an ideal choice for applications where space or weight is at a premium such as aircraft instrumentation, portable instruments, or CRT displays.

FUNCTIONAL DIAGRAM



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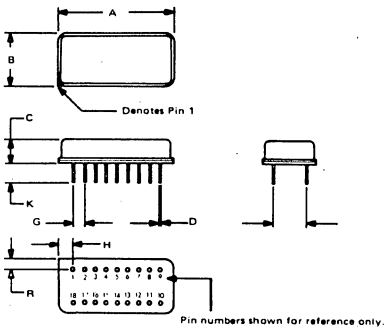
ELECTRICAL SPECIFICATIONS

MODEL	DAC82KG DAC82BM	DAC82SM	UNITS
DIGITAL INPUT			
Resolution	8	8	Bits
Logic Levels (TTL compatible)			
Logic "1"	$+2 < e_d < +5.5$ at $+40\mu A$		V
Logic "0"	$0 < e_d < +0.8$ at -1.0mA		V
TRANSFER CHARACTERISTICS			
ACCURACY			
Linearity Error at 25°C (max)	±0.16	±0.16	% of FSR
-25°C to +85°C (max)	±0.2		% of FSR
-55°C to +125°C (max)		±0.2	% of FSR
Differential Linearity Error	±0.5	±0.5	LSB
Gain Error	±0.1	±0.1	%
Offset Error	±0.05	±0.05	% of FSR
Total Accuracy Error (max)	±1	±1	LSB
Monotonicity Temp Range	-25 to +85	-55 to +125	°C
DRIFT			
Gain (max)			
-25°C to +85°C	±50		ppm/°C
-55°C to +125°C		±35	ppm/°C
Offset			
Unipolar			
-25°C to +85°C	±1		ppm of FSR/°C
-55°C to +125°C		±1	ppm of FSR/°C
Bipolar (max)			
-25°C to +85°C	±20		ppm of FSR/°C
-55°C to +125°C		±15	ppm of FSR/°C
CONVERSION SPEED			
Voltage Output			
Settling time to ±0.2% of FSR			
For FSR change			
20V Range	2.5		µsec
10V Range	2.0		µsec
For 1 LSB change	0.5		µsec
Slew Rate	20		V/µsec
Current Output			
Settling time to ±0.2%			
For FSR change			
10 to 100Ω load	250		nsec
1kΩ load	350		nsec
OUTPUT			
ANALOG OUTPUT			
Voltage Output			
Ranges	±2.5, ±5, ±10, +5, +10		Volts
Output Current, min	±5		mA
Output Impedance (DC)	0.05		Ω
Current Output			
Ranges	±0.8, 0 to -1.6		mA
Output Impedance - Bipolar	1.8		kΩ
Unipolar	2.0		kΩ
Compliance	±4.0V		Volts
INTERNAL REFERENCE VOLTAGE			
Magnitude	+6.3		Volts
Tempco of Drift, max	±20		ppm/°C
POWER SUPPLY SENSITIVITY			
+15VDC Supply	±0.02		% of FSR/%Vs
-15VDC Supply	±0.002		% of FSR/%Vs
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15		Volts
Range	±14.0 to ±16.0		Volts
Supply Drain (No load)			
+15VDC	15		mA
-15VDC	10		mA
TEMPERATURE RANGE			
Specification	-25 to +85	-55 to +125	°C
Operating (double above drift specs)	-55 to +125	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C

MECHANICAL

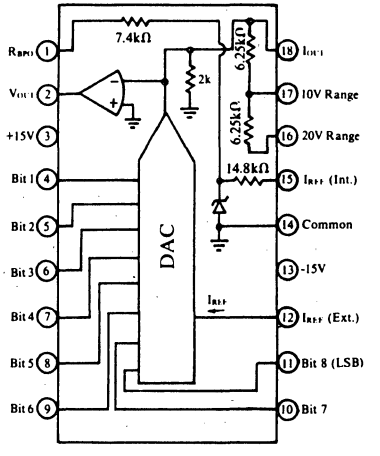
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.



CONNECTOR: None
CASE: Metal (BM, SM) Ceramic (KG)
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
HERMETICITY: Gross Leak (fluorocarbon) Fine Leak (helium, 5 x 10^{-7}cc/sec) (BM, SM only)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.060	1.080	26.92	27.43
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

CONNECTION DIAGRAM



DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC82 accepts digital inputs in complementary binary (CBI) format and may be connected for complementary straight binary (CSB) or complementary offset binary (COB) operation. By using one external inverter, the user can operate the DAC82 in the complementary two's complement (CTC) mode.

DIGITAL INPUT CODES	OUTPUT RANGE			
	VOLTAGE*		CURRENT	
	0 to +10V	±10V	0 to 1.6mA	±0.8mA
MSB LSB				
0 0 0 0 0 0 0 0	+9.961V	+9.922V	-1.594mA	-0.794mA
0 1 1 1 1 1 1 1	+5.000V	0.000V	-0.800mA	0.000mA
1 0 0 0 0 0 0 0	+4.961V	-78.12mV	-0.792mA	+6.248μA
1 1 1 1 1 1 1 1	0.000V	-10.000V	0.000mA	+0.800mA
one LSB	39.06mV	78.12mV	6.248μA	6.248μA

* To obtain values for other binary (CBI) ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE I. Digital Input and Analog Output Relationship.

ACCURACY

LINEARITY

The LINEARITY of a D/A converter is the true measure of its performance. The DAC82 analog output will not vary by more than ±1/2 LSB from an ideal straight line drawn between the end points (all 1's and all 0's) over the specified temperature range.

DIFFERENTIAL LINEARITY

The DIFFERENTIAL LINEARITY error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A DIFFERENTIAL LINEARITY error specification of ±1/2 LSB means that the output voltage can change anywhere from 1/2 LSB to 3/2 LSB when the input changes from one adjacent digital state to the next.

DRIFT

GAIN DRIFT

GAIN DRIFT is a measure of the change in the analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at the high and low temperature extremes and at 25°C for each model, calculating the GAIN ERROR with respect to the 25°C value, and dividing by the temperature change.

OFFSET DRIFT

OFFSET DRIFT is a measure of the actual change in output voltage at zero volts output over the specified temperature range. The offset voltage is measured at the temperature extremes, and the maximum change referenced to 25°C is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time is the time required for the output to enter and remain in an error band equal to ±0.2% of full scale range measured from the time the digital input is changed. Typical settling time values for full scale changes are a function of the load resistor and are shown in the figure below.

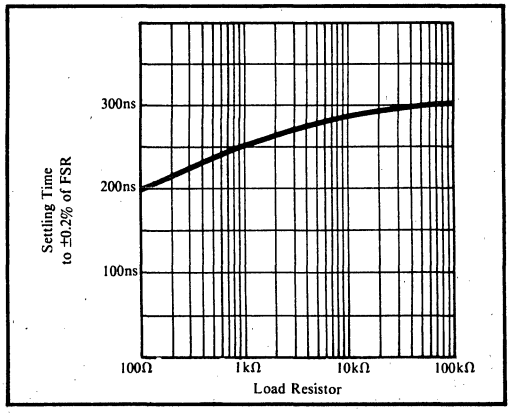


FIGURE 1. Settling Time for FSR Change vs Load.

COMPLIANCE

The COMPLIANCE VOLTAGE of the DAC82 is the maximum voltage swing allowed on the current output in order to maintain the specified accuracy. It is -4.0 to +4.0 volts for the unipolar and bipolar current ranges.

POWER SUPPLY SENSITIVITY

POWER SUPPLY SENSITIVITY is a measure of the effect of a power supply voltage change on the D/A converter output. It is defined as a percent of FSR/percent of change in either the +15 volt or -15 volt power supplies about the nominal power supply voltages. Figure 2 shows Power Supply Rejection vs Frequency.

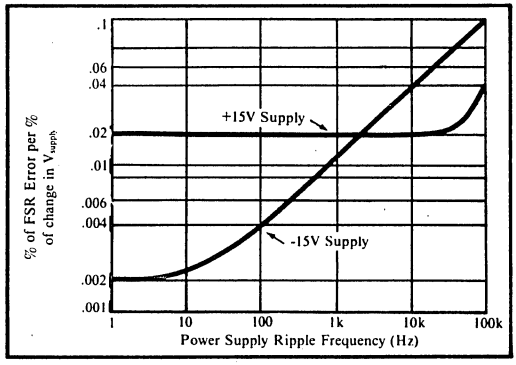


FIGURE 2. Power Supply Rejection vs. Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

DECOUPLING

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 3. These capacitors should be located close to the DAC82 and should be tantalum or electrolytic types bypassed with a 0.01 μF ceramic capacitor for best high frequency performance.

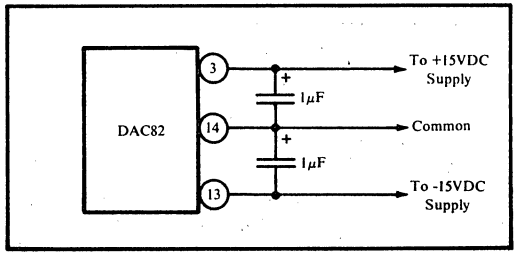


FIGURE 3. Recommended Power Supply Decoupling.

OPERATION IN THE CURRENT OUTPUT MODE

On the current output pin, the DAC82 provides a unipolar output current of 0 to -1.6mA and a bipolar output current of ±0.8mA. Refer to Figure 4 and Table II for proper connections. In applications requiring the use of the DAC82 in the current output mode, such as an A/D converter, the internal scaling resistors should be used to generate currents corresponding to analog input voltages.

OUTPUT RANGE	CONNECT PIN 1 TO:
0 to -1.6mA	N.C.
±0.8mA	Pin 18

TABLE II. Connections for Current Output Mode.

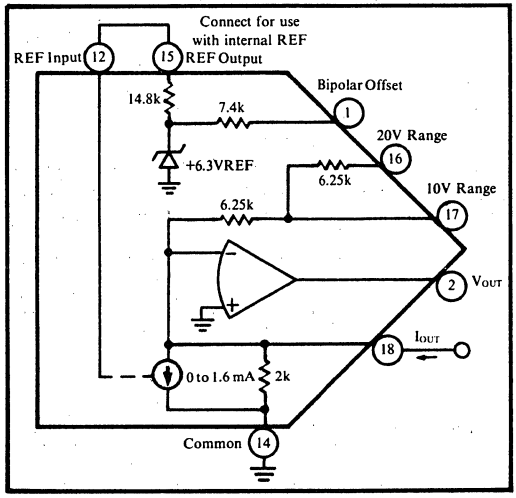


FIGURE 4. Current Output Mode Connection Diagram.

DRIVING AN EXTERNAL OP AMP

UNIPOLAR OR BIPOLAR - UP TO 20V OUTPUT RANGE

The DAC82 will drive the summing junction of an op amp (the op amp being used as a current to voltage converter) to produce an output voltage (see Figure 5).

$$V_{OUT} = -I_{OUT} \times R_F$$

where I_{OUT} is the DAC82 output current and R_F is the feedback resistor. The internal feedback resistors should be used to maintain the temperature drift specification. Refer to Table III and Figure 5 for proper connections.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT Ⓐ TO	CONNECT PIN 1 TO	CONNECT PIN 16 TO
±10V	COB or CTC	16	18	Ⓐ
±5V	COB or CTC	17	18	N.C.
±2.5V	COB or CTC	17	18	18
0 to +10V	CSB	17	Common	N.C.
0 to +5V	CSB	17	Common	18

TABLE III. Voltage Ranges of Current Output DAC82 with External Op Amp.

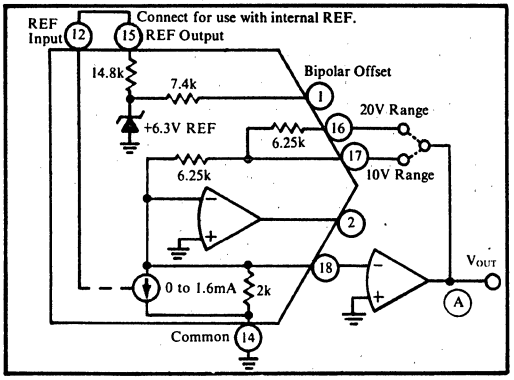


FIGURE 5. External Op Amp - Using Internal Feedback Resistors.

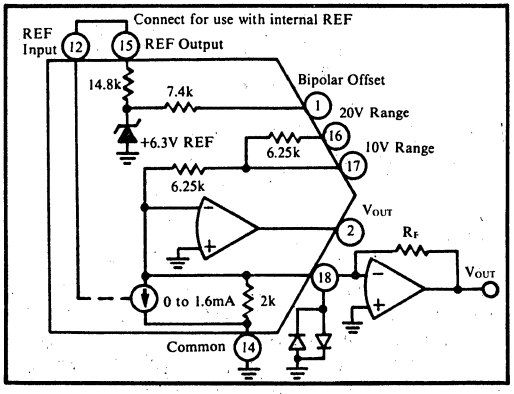


FIGURE 6. External Op Amp - Using External Feedback Resistors.

OUTPUTS LARGER THAN 20 VOLT RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±0.8mA for bipolar voltage ranges, and 0 to -1.6mA for unipolar voltage ranges (see Figure 6). Use protection diodes when a high voltage op amp is used.

VOLTAGE OUTPUT OPERATION USING INTERNAL AMPLIFIER

The DAC82 contains internal scaling resistors to provide a wide range of output voltage ranges. These resistors may be connected to provide 3 bipolar output ranges of ±10, ±5, or ±2.5 volts or two unipolar output voltage ranges of 0 to +5 or 0 to +10 volts. Gain and offset drift errors are minimized since these scaling resistors are an integral part of the DAC. Connections for DAC82 output voltage ranges are shown in Table IV and Figure 7 below.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 2 TO	CONNECT PIN 1 TO	CONNECT PIN 16 TO
±10V	COB or CTC	16	18	2
±5V	COB or CTC	17	18	N.C.
±2.5V	COB or CTC	17	18	18
0 to +10V	CSB	17	Common	N.C.
0 to +5V	CSB	17	Common	18

TABLE IV. Voltage Ranges of Current Output DAC82 with External Op Amp.

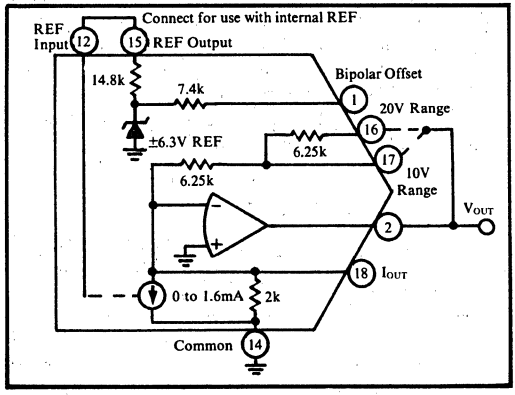


FIGURE 7. Voltage Output Using Internal Amplifier.

OPERATION AS MULTIPLYING DAC

By using an external voltage reference, the DAC82 can be connected as a multiplying DAC, such that the analog output represents the product of the digital input and the analog reference input. To operate the DAC82 as a two quadrant MDAC, connect the unit as shown in Figure 8. If R2, the bipolar offset resistor, is replaced with an open circuit, the DAC will operate in one quadrant. Table V below shows the digital input and analog output relationships for one quadrant and two quadrant multiplication and Figure 8 shows the connection for output voltage or output current. Since the absolute temperature coefficient of the internal feedback resistors (6.25k) is typically 30 ppm/°C, improved temperature stability can be achieved by using an external 13.5k resistor connected between pins 2 and pins 18, making no connection to pins 16 or 17.

DIGITAL INPUT CODES	OUTPUT RANGE			
	VOLTAGE*		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -1.6mA	±0.8mA
00000000	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.9961)$	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.9922)$	$\frac{(4\ V_R)}{(R_1)}(0.9961)$	$\frac{(4\ V_R)}{(R_1)}(0.9922)$
01111111	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.5000)$	0.0000	$\frac{(4\ V_R)}{(R_1)}(0.5000)$	0.0000
10000000	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.4961)$	$\frac{(4\ V_R)(R_F)}{(R_1)}(-0.0078)$	$\frac{(4\ V_R)}{(R_1)}(0.4961)$	$\frac{(4\ V_R)}{(R_1)}(-0.0078)$
11111111	0.0000	$\frac{(4\ V_R)(R_F)}{(R_1)}(-1)$	0.0000	$\frac{(4\ V_R)}{(R_1)}(-1)$
1 LSB	$\frac{(4\ V_R)(R_F)}{(R_1)}0.0039)$	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.0078)$	$\frac{(4\ V_R)}{(R_1)}(0.0039)$	$\frac{(4\ V_R)}{(R_1)}(0.0078)$

TABLE V. Digital Input and Analog Output Relationship for Multiplying Configuration.

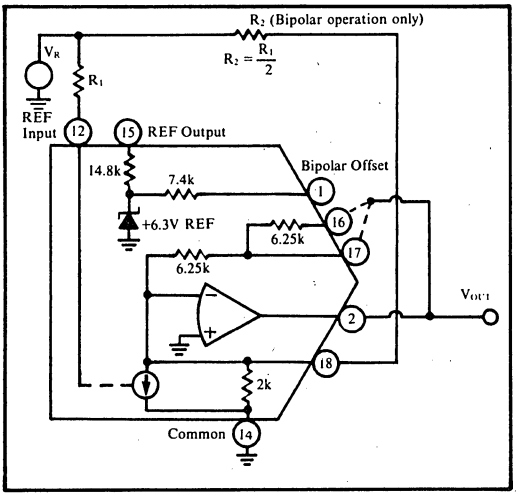


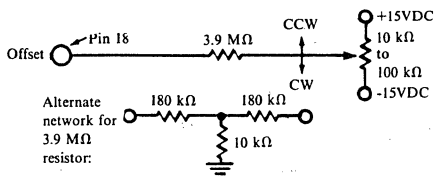
FIGURE 8. Connection for Multiplying Mode.

OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS

The DAC82 has been laser trimmed at the factory to insure absolute accuracy of 1 LSB at +25°C. However, externally connected offset and gain potentiometers may be used to null these error components to zero. If these adjustments are not used, simply leave the pins open. Adjustment networks should be located physically closed to the DAC82 to minimize signal pickup.

OFFSET ADJUSTMENT

For unipolar operation, apply the digital input code that should give zero volts output and adjust the OFFSET potentiometer for zero volts output. For bipolar operation, apply the digital input code that should give the maximum negative voltage output. Example: If the FULL SCALE RANGE is connected for 20 volts, then the maximum negative voltage output is -10 volts. See Table I for corresponding codes.



Range of adjustment: ±0.2% of FSR

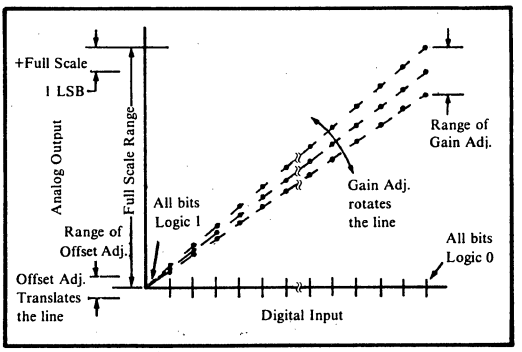
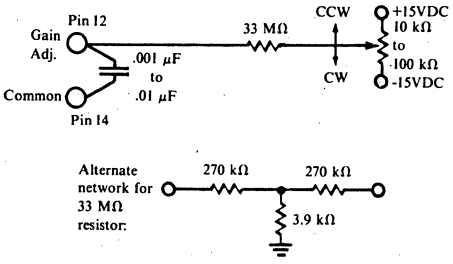


FIGURE 9. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter.

GAIN ADJUSTMENT

For either unipolar or bipolar D/A converters, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. The positive full scale voltages for the DAC82 are given in Table V.



Range of Offset Adjustment: ±0.2% of FSR

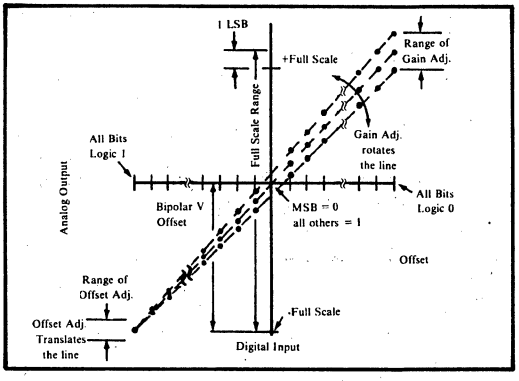


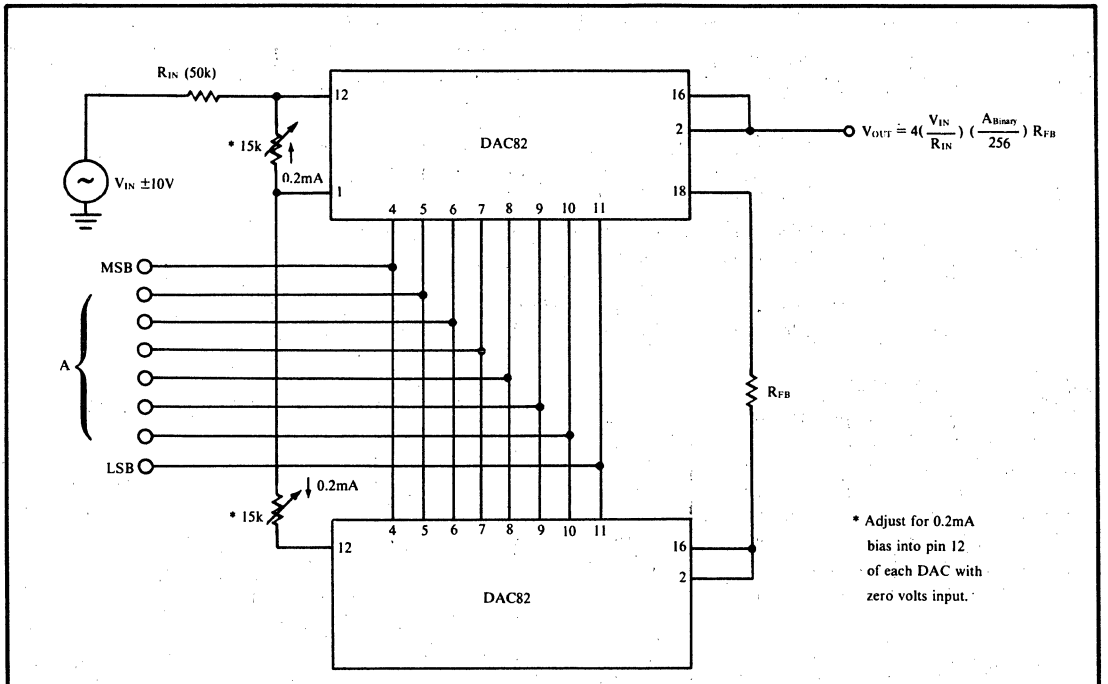
FIGURE 10. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter.

APPLICATIONS

Two DAC82's can be connected as shown to construct a digitally-controlled attenuator which will accept bipolar input voltages. Since the input to the DAC is a summing junction (pin 12), input voltages greater than ±10V can be used if R_{IN} is increased proportionately. The transfer function is:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{4\,R_{FB}}{R_{IN}}\right)\left(\frac{A_{BINARY}}{256}\right)$$

To remove initial gain errors, the two 15k resistors should be adjusted such that 0.2 mA flows into pin 12 of each DAC82 when $V_{IN} = 0$.



DIGITALLY CONTROLLED ATTENUATOR WITH BIPOLAR INPUT

BURR-BROWN®

DAC85H
DAC85L
DAC87H
DAC87L

Monolithic 12-Bit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

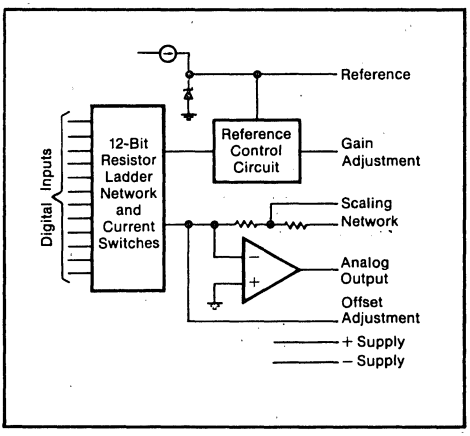
- INDUSTRY STANDARD PINOUT
- LOW POWER DISSIPATION: 345mW
- FULL ±10V SWING WITH V_{CC} = ±12VDC
- DIGITAL INPUTS ARE TTL- AND CMOS-COMPATIBLE
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES
- SINGLE-CHIP DESIGN
- ±1/2LSB MAXIMUM NONLINEARITY, −55°C to +125°C
- GUARANTEED MONOTONICITY, −55°C TO +125°C
- TWO PACKAGE OPTIONS: Hermetic DIP and Leadless Chip Carrier
- SETTLING TIME: 4μs max to ±0.01% of Full Scale

DESCRIPTION

These monolithic digital-to-analog converters are pin-for-pin equivalent to the industry standard DAC85 and DAC87 first introduced by Burr-Brown. Their single-chip design includes the output amplifier and provides a highly stable reference capable of supplying up to 2.5mA to an external load without degradation of D/A performance.

These converters use proven circuit techniques to provide accurate and reliable performance over temperature and power supply variations. The use of a buried zener diode as the basis for the internal reference contributes to the high stability and low noise of the device. Advanced methods of laser trimming result in precision output current and output amplifier feedback resistors, as well as low integral and differential linearity errors. Innovative circuit design enables the DAC85 and DAC87 to operate at supply voltages as low as ±11.4V with no loss in performance or accuracy over any range of output voltage. Ease of use has been enhanced by eliminating the need for a +5V logic power supply. The lower power dissipation of the 118 mil by 121 mil chip results in higher reliability and greater long term stability.

Both models are available in a hermetic, side-brazed, ceramic DIP and in a ceramic leadless chip carrier. The DAC85H and L are specified over the industrial temperature range of −25°C to +85°C. The DAC87H and L are specified over the entire military temperature range of −55°C to +125°C.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

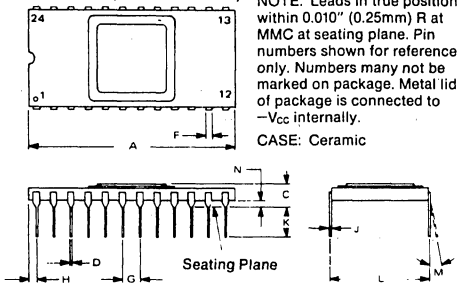
Typical at +25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

MODEL	DAC85H, L			DAC87H, L			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT							
Resolution			12			12	Bits
Logic Levels (0°C to +70°C)[1]:							
V_{IH} (Logic "1")	+2		+16.5	+2		+16.5	VDC
V_{IL} (Logic "0")	0		+0.8	0		+0.8	VDC
I_{IH} (V_{IN} = +2.4V)			+20			+20	µA
I_{IL} (V_{IN} = +0.4V)			−180			−180	µA
ACCURACY (at 25°C)							
Linearity Error		±1/4	±1/2		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	±3/4		±1/2	±3/4	LSB
Gain Error[2]		±0.1	±0.2			±0.1	%
Offset Error[2]		±0.05	±0.1			±0.05	% of FSR[3]
DRIFT (over specification temperature range)[4]							
Total bipolar drift (incldues gain, offset, and linearity drifts)		±10	±25			±30	ppm of FSR/°C
Total Error (over specification temperature range)[5]: Unipolar			±0.2			±0.2	% of FSR
Bipolar			±0.12			±0.2	% of FSR
Gain: Including Internal Reference			±20			±20	ppm/°C
Excluding Internal Reference		±5	±10		±5	±10	ppm/°C
Unipolar Offset			±3			±3	ppm of FSR/°C
Bipolar Offset			±10			±10	ppm of FSR/°C
Differential Linearity			±3/4			±3/4	LSB
Linearity Error		±1/4	±1/2		±1/4	±1/2	LSB
Monotonicity Guaranteed	−25		+85	−55		+125	°C
CONVERSION SPEED, V_{OUT} models							
Settling Time to ±0.01% of FSR							
For FSR change (2kΩ ‖ 500pF load)							
with 10kΩ Feedback		3	4		3	4	µs
with 5kΩ Feedback		2	3		2	3	µs
For 1LSB Change		1			1		µs
Slew Rate	10			10			V/µs
CONVERSION SPEED, I_{OUT} models							
Settling Time to ±0.01% of FSR							
For FSR change: 10Ω to 100Ω load		300			300		ns
1kΩ load		1			1		µs
ANALOG OUTPUT, V_{OUT} models							
Ranges		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current[6]	±5			±5			mA
Output Impedance (DC)		0.05			0.05		Ω
Short Circuit to Common, Duration[7]		Indefinite			Indefinite		
ANALOG OUTPUT, I_{OUT} models							
Ranges: Bipolar	±0.96	±1.0	±1.04	±0.96	±1.0	±1.04	mA
Unipolar	−1.96	−2.0	−2.04	−1.96	−2.0	−2.04	mA
Output Impedance: Bipolar	2.6	3.2	3.7	2.6	3.2	3.7	kΩ
Unipolar	4.6	6.6	8.6	4.6	6.6	8.6	kΩ
Compliance	−2.5		+2.5	−2.5		+2.5	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6.30	+6.37	+6.23	+6.30	+6.37	V
External Current (constant load)			2.5			2.5	mA
Drift vs Temperature			±20			±10	ppm/°C
Output Impedance		1			1		Ω
POWER SUPPLY SENSITIVITY							
V_{CC} = ±12VDC or ±15VDC		±0.002	±0.006		±0.002	±0.004	% FSR/ % V_{CC}
POWER SUPPLY REQUIREMENTS							
$\pm V_{CC}$	±11.4		±16.5	±11.4		±16.5	VDC
Supply Drain (no load): $+V_{CC}$		8	12		8	12	mA
$-V_{CC}$		15	20		15	20	mA
Power Dissipation (V_{CC} = ±15VDC)		345	480		345	480	mW
TEMPERATURE RANGE							
Specification	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES: (1) Refer to "Logic Input Compatibility" section. (2) Adjustable to zero with external trim potentiometer. (3) FSR means full scale range and is 20V for ±10V range, 10V for ±5V range for V_{OUT} models; 2mA for I_{OUT} models. (4) To maintain drift spec, internal feedback resistors must be used. (5) Includes the effects of gain, offset and linearity drift. Gain and offset errors externally adjusted to zero at +25°C. (6) For $\pm V_{CC}$ less than ±12VDC, limit output current load to ±2.5mA to maintain ±10V full scale output voltage swing. For output range of ±5V or less, the output current is ±5mA over entire $\pm V_{CC}$ range. (7) Short circuit current is 40mA, max.

MECHANICAL

H PACKAGE (Hermetic DIP)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°		10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers many not be marked on package. Metal lid of package is connected to $-V_{CC}$ internally.

CASE: Ceramic

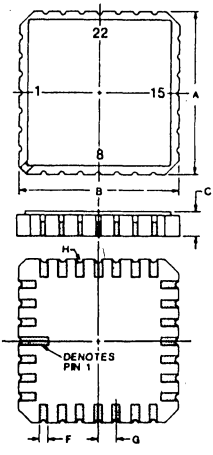
MATING CONNECTOR: 0245MC

WEIGHT: 4.1 grams (0.15 oz.)

PIN: Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

HERMETICITY: Conforms to Method 1014, Condition A1 or A2 (fine leak) and Condition C (gross leak).

L PACKAGE (Hermetic LCC*)



*Leadless Chip Carrier

NOTE: Pin numbers shown for reference only. Numbers many not be marked on package. Metal lid is floating.

CASE: Ceramic

CAP: Kovar, gold plated

MATING CONNECTOR: 2802MC (adapts LCC package to 24-pin DIP DAC85H pinout.)

WEIGHT: 0.76 grams (0.026 oz.)

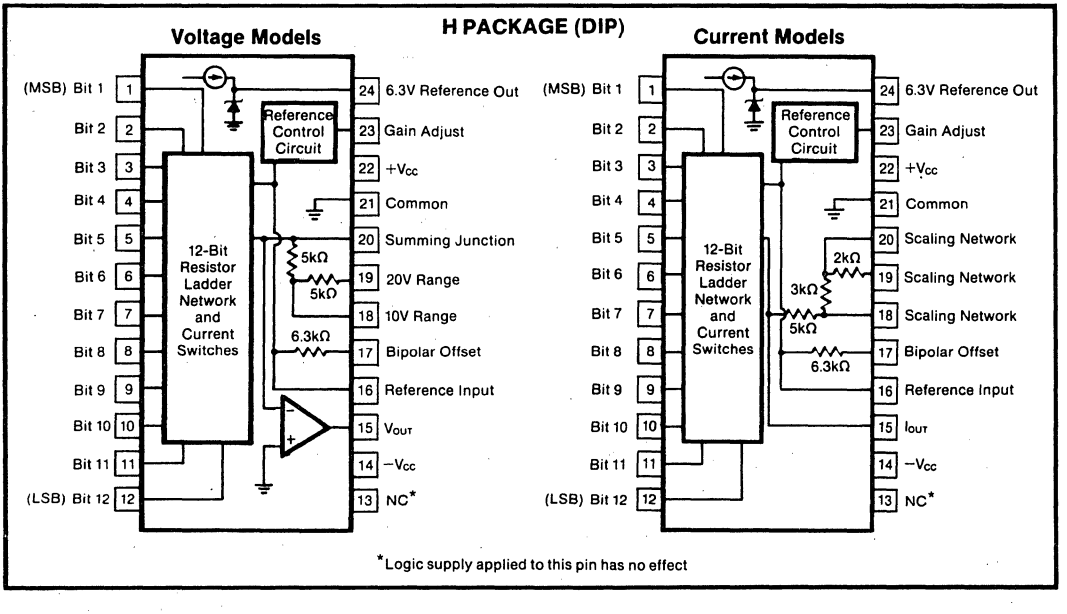
CONTACTS: Material and composition conform to Method Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2, steam aging).

HERMETICITY: Conforms to Method 1014, Condition A1 or A2 and Condition C.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.442	.458	11.23	11.63
B	.442	.458	11.23	11.63
C	.064	.100	1.63	2.54
F	.022	.028	0.56	0.71
G	0.50 BASIC		1.27 BASIC	
H	.008 R TYP.		0.20R TYP	

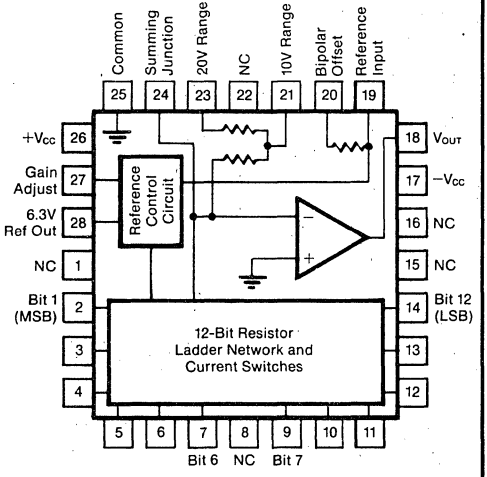
FUNCTIONAL DIAGRAM AND PIN ASSIGNMENTS

H PACKAGE (DIP)



*Logic supply applied to this pin has no effect

L PACKAGE (LCC)



NOTE: All references to pin numbers in this data sheet are relative to the H Package (24-pin DIP). The L Package (28-pin LCC) sequence of functions around the periphery is the same as the sequence for the H Package; however, the numbering is different. Therefore, "Operating Instructions" that follow should be interpreted for the L Package in terms of pin function rather than pin number.

ABSOLUTE MAXIMUM RATINGS

+Vcc to Common	0V to +18V
−Vcc to Common	0V to −18V
Digital Data Inputs to Common	−1V to +18V
Reference Output to Common	±Vcc
Reference Input to Common	±Vcc
Bipolar Offset to Common	±Vcc
10V Range R to Common	±Vcc
20V Range R to Common	±Vcc
External Voltage to DAC Output	−5V to +5V
Max Junction Temperature	165°C
Lead Temperature, Soldering	+300°C, 10s
Thermal Resistance, θ_{JA}: H Package	65°C/W
L Package	65°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ENVIRONMENTAL SCREENING

/QM Screening

Burr-Brown /QM models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

Screening Flow For /QM Models

Screen	MIL-STD-883 Method	Condition	Comments
Internal Visual	2010	B	
High Temperature Storage (Stabilization Bake)	1008	C	+150°C, 24hrs
Temperature Cycling	1010	C	−65 to +150°C, 10 cycles
Burn-in	1015	B	+125°C, 160hrs
Constant Acceleration	2001	E	30,000 Gs
Hermeticity			
Fine Leak	1014	A1 or A2	5×10^{-8} atm cc/sec
Gross Leak	1014	C	60psig, 2hrs
External Visual	2009		

ORDERING INFORMATION

Model	Output	Package
DAC85H-CBI-I	Current	DIP
DAC85H-CBI-I/QM	Current	DIP
DAC85H-CBI-V	Voltage	DIP
DAC85H-CBI-V/QM	Voltage	DIP
DAC85L-V	Voltage	LCC
DAC85L-V/QM	Voltage	LCC
DAC87H-CBI-V	Voltage	DIP
DAC87H-CBI-V/QM	Voltage	DIP
DAC87L-V	Voltage	LCC
DAC87L-V/QM	Voltage	LCC

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC85H Series accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB, or CTC (see Table I).

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC85H Series is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn

TABLE I. Digital Input Codes.

Digital Input	Analog Output		
MSB ↓ LSB ↓	CSB Complementary Straight Binary	COB Complemen. Offset Binary	CTC* Complemen. Two's Complement
000000000000	+Full Scale	+Full Scale	−1LSB
011111111111	+1/2 Full Scale	Zero	−Full Scale
100000000000	1/2 Full Scale −1LSB	−1LSB	+Full Scale
111111111111	Zero	−Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specification temperature range is guaranteed in the DAC85H Series to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC85H Series model at 0°C, +25°C and +70°C; 2) calculating the gain error with respect to the 25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specification temperature range. The offset is measured at 0°C, minimum temperature and maximum temperature. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC85H Series model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

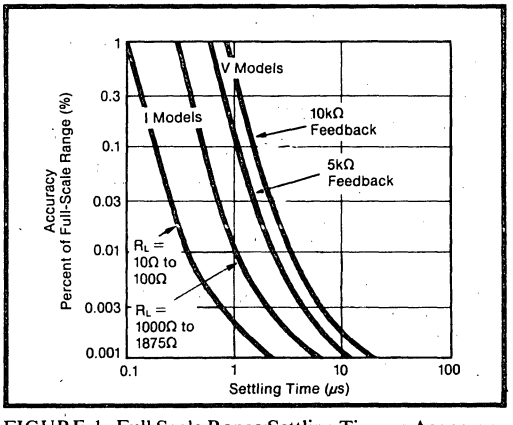


FIGURE 1. Full Scale Range Settling Time vs Accuracy.

Voltage Output Models

Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Models

Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω to 1875Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000Ω to 1800Ω for output voltage range of ±1V and 0 to −2V. See Figure 11.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage swing permitted without damage to the DAC85H Series is ±5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages (see Figure 2).

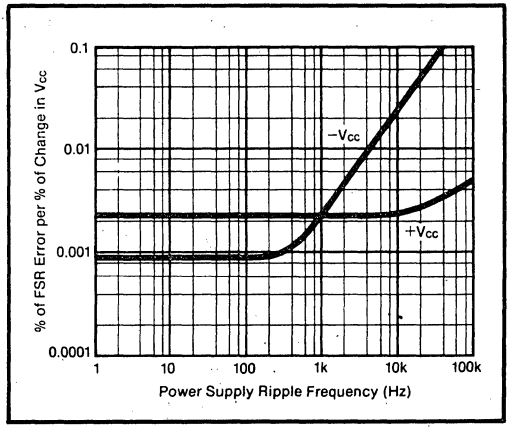


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC85H Series models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 2.5mA.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

LOGIC INPUT COMPATIBILITY

DAC85H Series digital inputs are TTL, LSTTL and 4000B, 54/74HC CMOS compatible. The input switching threshold remains at the TTL threshold over the entire supply range.

Logic "0" input current over temperature is low enough to permit driving DAC85H Series directly from outputs of 4000B and 54/74C CMOS devices.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Connect power supply voltages as shown in Figure 3. For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown. These capacitors (1μF tantalum) should be located close to the DAC85H Series.

±12V OPERATION

All DAC85H Series models can operate over the entire power supply range of ±11.4V to ±16.5V. Even with supply levels dropping to ±11.4V, the DAC can swing a full ±10V range, provided the load current is limited to ±2.5mA. With power supplies greater than ±12V, the DAC output can be loaded up to ±5mA. For output swing of ±5V or less, the output current is ±5mA, min. over the entire V_{CC} range.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted.

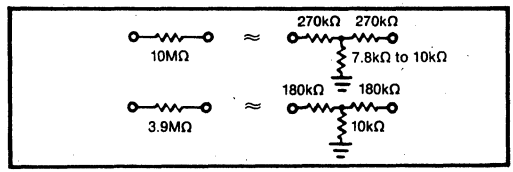


FIGURE 4. Equivalent Resistances.

Existing applications that are converting to the monolithic DAC85H Series must change the gain trim resistor on pin 23 from 18MΩ to 10MΩ to insure sufficient adjustment range. Pin 23 is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figure 5 for relationship of Offset and Gain adjustments to unipolar and bipolar D/A operation.

Offset Adjustment

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

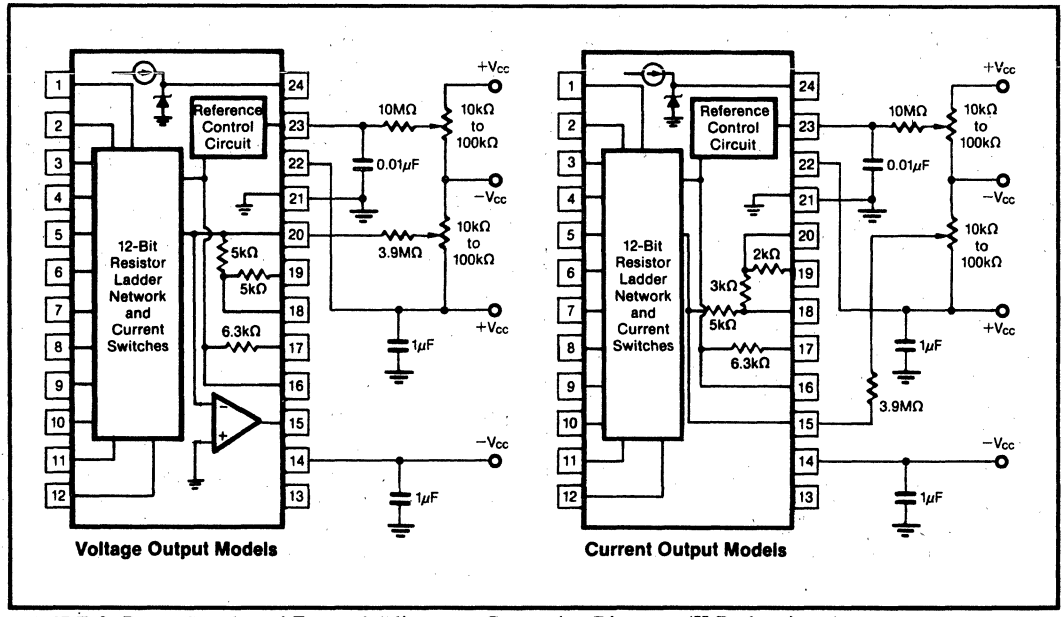
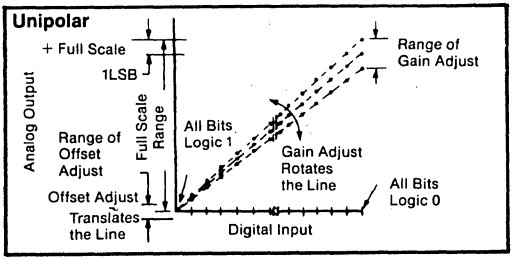


FIGURE 3. Power Supply and External Adjustment Connection Diagrams (H Package).

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table II for corresponding codes.



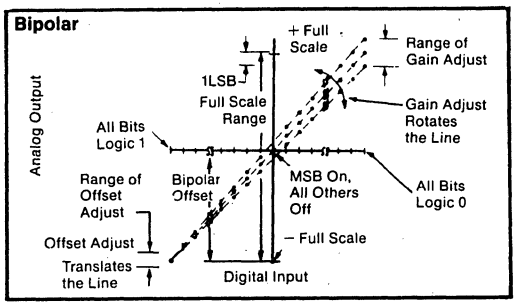


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar and Bipolar D/A Converter.

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output. Adjust the Gain potentiometer for this positive full scale output. See Table II for positive full scale voltages and currents.

TABLE II. Digital Input/Analog Output.

DIGITAL INPUT	ANALOG OUTPUT			
	VOLTAGE*		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC85H Series may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

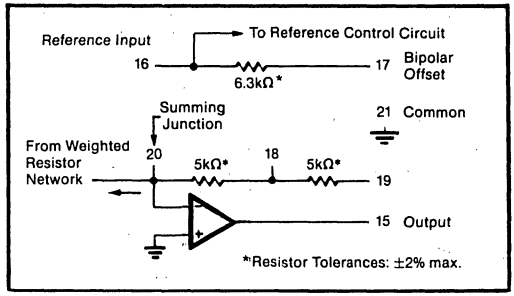


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other internal device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full-scale range change is specified as 4μs for the 20V range and 3μs for the 10V range.

TABLE III. Output Voltage Range Connections for Voltage Models.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24

CURRENT OUTPUT MODELS

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.

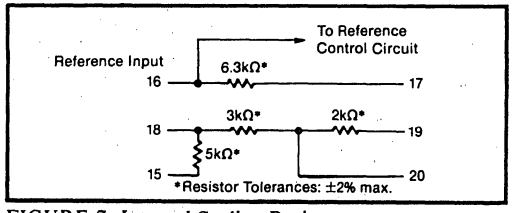


FIGURE 7. Internal Scaling Resistors.

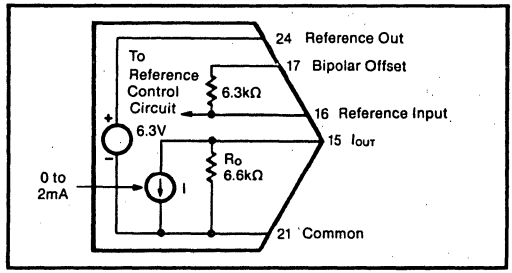


FIGURE 8. Current Output Model Equivalent Output Circuit.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving An External Op Amp

The current output model DAC85H will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage. See Figure 9.

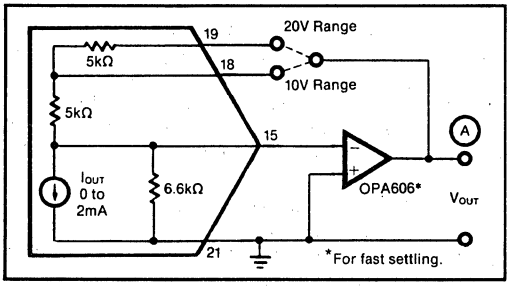


FIGURE 9. External Op-Amp—Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC85H output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model DAC85H provides output voltage ranges the same as the voltage model DAC85H. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges. See Figure 10. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C plus R_F drift to total drift.

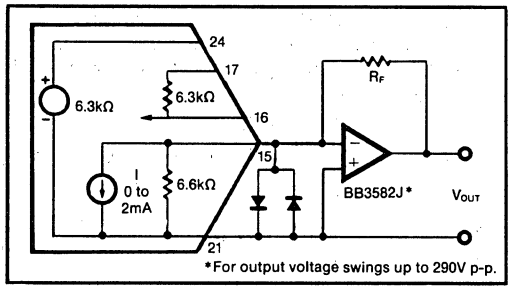


FIGURE 10. External Op-Amp—Using External Feedback Resistors.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 11 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA\ [(R_L \times R_O) \div (R_L + R_O)]$$

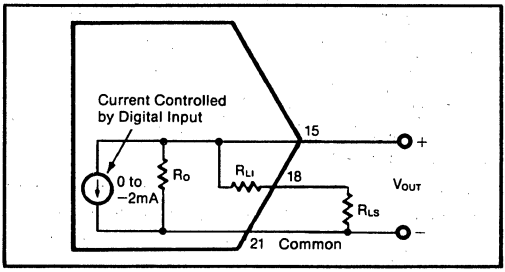


FIGURE 11. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

The unipolar output impedance R_O equals 6.6kΩ (typ) and R_{LI} is the internal load resistance of 968Ω (derived by connecting pin 15 to pin 20 and pin 18 to 19). By choosing $R_{LS} = 210\Omega$, $R_L = 1178\Omega$. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of 0 to −2V. Since R_O is not exact, initial trimming per Figure 3 may be necessary; also R_{LS} may be trimmed.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is similar to Figure 11, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA\ [(R_O \times R_L) \div (R_O + R_L)]$$

By connecting pin 17 to 15, the output current becomes bipolar (±1mA) and the output impedance R_O becomes 3.2kΩ (6.6kΩ || 6.3kΩ). R_{LI} is 1200Ω (derived by connecting pin 15 to 18 and pin 18 to 19). By choosing $R_{LS} =$ 255Ω (for a bipolar output connect R_{LS} between pin 20 and pin 21), $R_L = 1455\Omega$. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of ±1V. As indicated above, trimming may be necessary.

BURR-BROWN®

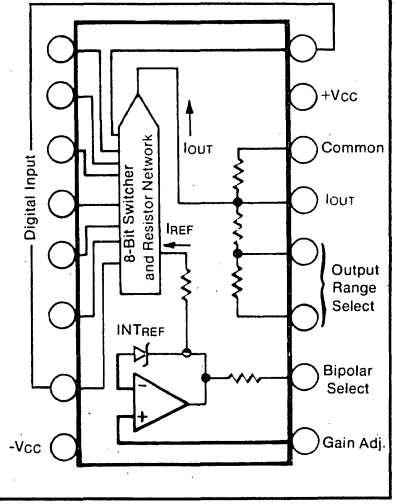
DAC90

Monolithic Microcircuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 8-BIT RESOLUTION
- CURRENT OUTPUT
- FAST SETTLING
  200nsec to ±0.2%
- HERMETIC DUAL-IN-LINE PACKAGE
- LOW COST
- INTERNAL REFERENCE AND SCALING RESISTORS

FUNCTIONAL DIAGRAM



DESCRIPTION

The DAC90 is an 8-bit D/A Converter that offers performance usually found only in larger, modular units. Housed in a 16-pin ceramic dual-in-line package, the DAC90 is complete with its own internal reference and scaling resistors.

Two versions are available: the DAC90BG (-25°C to +85°C) and DAC90SG (-55°C to +125°C) both offer ±0.2% nonlinearity over their respective temperature ranges. Settling time to ±0.2% is typically 200nsec.

The small size of the DAC90 makes it an ideal choice as the heart of your A/C converter design or for applications where space or weight is at premium, such as CRT displays, aircraft instrumentation, and portable instruments.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

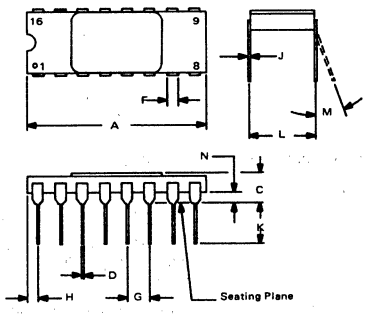
ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	DAC90BG	DAC90SG	UNITS
DIGITAL INPUT			
Resolution	8	8	Bits
Logic Levels (TTL-compatible)			
Logic "1"	+2< e_d < +5.5 at +40μA		V
Logic "0"	0< e_d < +0.8 at -1.0mA		V
TRANSFER CHARACTERISTICS			
ACCURACY			
Linearity Error at 25°C, max	±1/2	±1/2	LSB
-25°C to +85°C, max	±1/2		LSB
-55°C to +125°C, max		±1/2	LSB
Differential Linearity Error	±1/2	±1/2	LSB
Gain Error(1)	5	5	%
Offset Error(1)	1	1	% of FSR(2)
Minimum Temperature Range for Guaranteed Monotonicity	-25 to +85	-55 to +125	°C
DRIFT(3)			
Gain			
-25°C to +85°C	±50		ppm/°C
-55°C to +125°C		±50	ppm/°C
Offset			
Unipolar			
-25°C to +85°C	±1		ppm of FSR/°C
-55°C to +125°C		±1	ppm of FSR/°C
Bipolar			
-25°C to +85°C	±50		ppm of FSR/°C
-55°C to +125°C		±50	ppm of FSR/°C
CONVERSION SPEED			
Settling time to ±0.2% of FSR for FSR change			
10Ω to 100Ω load	200		nsec
1kΩ load	300		nsec
ANALOG OUTPUT			
Ranges	±1, 0 to -2		mA
Output Impedance - Bipolar	1.8		kΩ
Unipolar	2		kΩ
Compliance	-4 to +4		V
Internal Reference Voltage(V_r)	7.6		V
Tempco of Drift	±50	±50	ppm of V_r/°C
POWER SUPPLY SENSITIVITY			
+15VDC	±0.02%		% of FSR/%V_S
-15VDC	±0.002		% of FSR/%V_S
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15		VDC
Range	±14.5 to ±15.5		VDC
Supply Drain ±15VDC	7		mA
TEMPERATURE RANGE			
Specification	-25 to +85	-55 to +125	°C
Operating	-55 to +125	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C

NOTES:
1. Adjustable to zero with external trim potentiometer.
2. FSR means "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.
3. To maintain drift spec internal feedback resistors must be used.

MECHANICAL

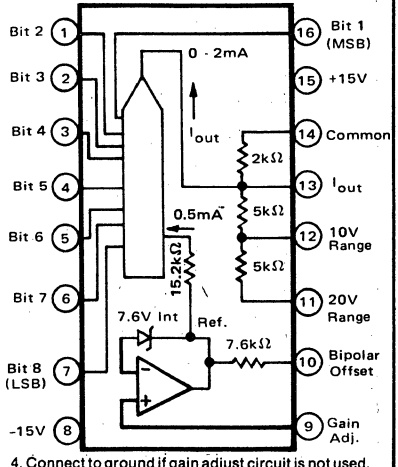


NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

CASE: Ceramic, with hermetic seal
HERMETICITY: Conforms to MIL-STD-883 Method 1014, Condition C, Step 1 Fluorocarbon Gross leak and Condition A Helium), 5 x 10-7 cc/sec (fine leak).

CONNECTION DIAGRAM



4. Connect to ground if gain adjust circuit is not used.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC90 accepts digital inputs in complementary binary (CBI) format and may be connected for complementary straight binary (CSB) or complementary offset binary (COB) operation (see Table I). By using one external inverter, the user can operate the DAC90 in the complementary two's complement (CTC) mode.

TABLE I. Digital Input and Analog Output Relationship.

DIGITAL INPUT CODES	OUTPUT RANGE			
	VOLTAGE*		CURRENT	
	0 to +10V	±10V	0 to -2mA	±1mA
MSB LSB				
00000000	+9.961V	+9.922V	-1.992mA	-0.992mA
01111111	+5.000V	0.000V	-1.000mA	0.0000mA
10000000	+4.961V	-78.12mV	-0.99mA	+7.81μA
11111111	0.000V	-10.000V	0.000mA	+1.000mA
one LSB	39.06mV	78.12mV	7.81μA	7.81μA

* Requires external amplifier. To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

ACCURACY

Linearity

The LINEARITY of a D/A converter is the true measure of its performance. The DAC90 analog output will not vary by more than ±1/2LSB from an ideal straight line drawn between the end points (all 1's and all 0's) over the specified temperature range.

Differential Linearity

DIFFERENTIAL LINEARITY error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A DIFFERENTIAL LINEARITY error specification of ±1/2LSB means that the output voltage can change anywhere from 1/2LSB to 3/2LSB when the input changes from one adjacent digital state to the next.

DRIFT

Gain Drift

GAIN DRIFT is a measure of the change in the analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at the high and low temperature extremes and at 25°C for each model, calculating the GAIN ERROR with respect to the 25°C value, and dividing by the temperature change.

Offset Drift

OFFSET DRIFT is a measure of the actual change in output voltage (using an external amplifier) at zero volts output over the specified temperature range. The offset voltage is measured at the temperature extremes, and the maximum change referenced to 25°C is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

SETTLING TIME is the time required for the output to enter and remain in an error band equal to ±0.2% of full scale range measured from the time the digital input is changed. Typical settling time values for full scale changes are a function of the load resistor and are shown in the figure below.

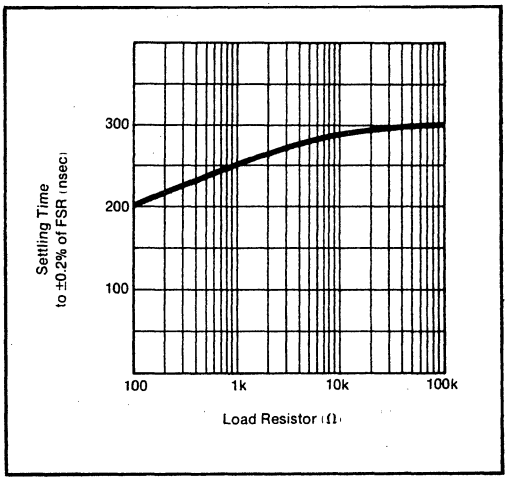


FIGURE 1. Settling Time for FSR Change vs Load.

Compliance

The COMPLIANCE VOLTAGE of the DAC90 is the maximum voltage swing allowed on the current output in order to maintain the specified accuracy; it is -4.0V to +4.0V for the unipolar and bipolar current ranges. The maximum safe voltage swing allowed with no damage to the DAC90 output is -4.0B to +15.0V

POWER SUPPLY SENSITIVITY

POWER SUPPLY SENSITIVITY is a measure of the effect of a power supply voltage change on the D A converter output. It is defined as a percent of FSR/ percent of change in either the +15VDC or -15VDC power supplies about the nominal power supply voltages. Figure 2 shows power supply rejection vs frequency.

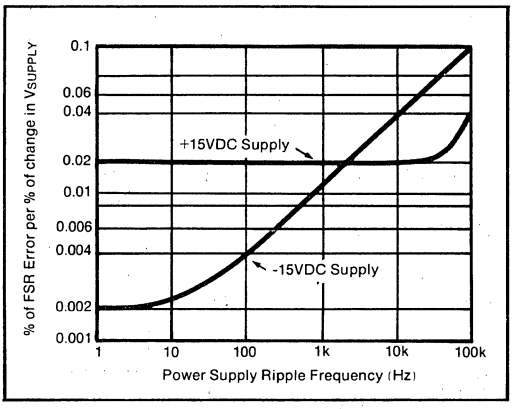


FIGURE 2. Power Supply Rejection vs. Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Decoupling

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 3. These capacitors should be located close to the DAC90 and should be tantalum or electrolytic types bypassed with a 0.01μF ceramic capacitor for best high frequency performance.

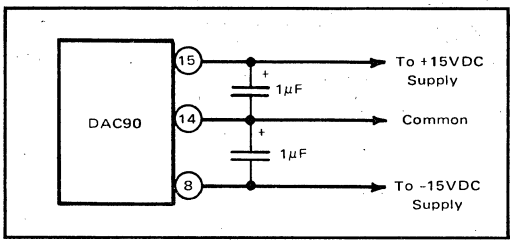


FIGURE 3. Recommended Power Supply Decoupling

OPERATION IN THE CURRENT OUTPUT MODE

In the current output mode, the DAC90 provides a unipolar output current of 0 to -2mA and a bipolar output current of ±1mA. Refer to Figure 4 and Table II for proper connections. In applications requiring the use of the DAC90 in the current output mode, such as an A/ D converter, the internal scaling resistors should be used to generate currents corresponding to analog input voltages.

TABLE II. Connections for Current Output Mode.

Output Range	Connect Pin (13) to:
0 to -2mA	N.C.
±1mA	Pin 10

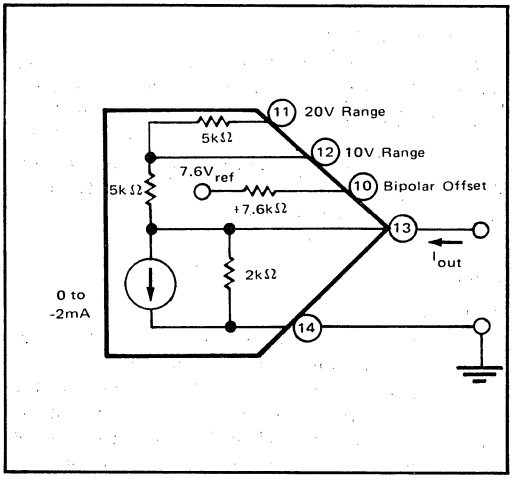


FIGURE 4. Current Output Mode Connection Diagram.

VOLTAGE OUTPUT using an EXTERNAL OP AMP

UNIPOLAR OR BIPOLAR OPERATION

The DAC90 will drive the summing junction of an op amp (the op amp being used as a current-to-voltage converter) to produce and output voltage.

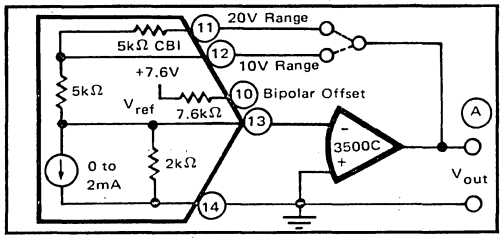


FIGURE 5. External Op Amp Using Internal Feedback Resistors.

$$V_{OUT} = -I \times R_F$$

where I_{OUT} is the DAC90 output current and R_F is the feedback resistor. Refer to Table III and Figure 5.

TABLE III. Voltage Ranges of Current Output DAC90 with External Op Amp.

Output Range	Digital Input Codes	Connect (A) to	Connect Pin (13) to
±10V	COB	11	10
±5V	COB	12	10
±2.5V	COB	12	10,11
0 to +10V	CSB	12	N.C.
0 to +5V	CSB	12	11

EXTERNAL OFFSET and GAIN ADJUSTMENT

Initial offset and gain errors may be trimmed by the user with externally connected OFFSET and GAIN potentiometers and an operational amplifier. Refer to Figures 5 and 6 for proper connections. The adjustment procedures are described below. Potentiometer resistances are shown as a range of values and should have a temperature drift coefficient of 100ppm/°C or less. The trimming networks should be located as close to the DAC90 as possible to minimize noise pickup. The ceramic capacitor shown in Figure 6 will further reduce noise pickup at the gain adjust point.

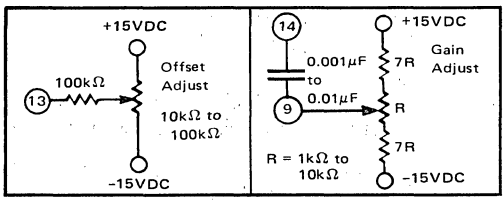


FIGURE 6. Connections for OFFSET and GAIN Adjustment.

OFFSET ADJUSTMENT

Offset adjustment should be made prior to gain adjustment. Connect the unit as shown in Figure 5 for the desired output range and add the offset adjust network shown in Figure 6. Offset adjustment is the same procedure for either bipolar or unipolar operation. Apply the digital input code which should give zero volts output and adjust the offset potentiometer for zero volts output. See Table I for the corresponding codes.

GAIN ADJUSTMENT

The gain adjust procedure is the same for either bipolar or unipolar operation. An external amplifier should be connected as shown in Figure 5. Connect the unit for the desired output range and add the gain adjust network shown in Figure 6. Apply the digital input code which should give the maximum positive output voltage and adjust the gain potentiometer for the correct output. Refer to Table I for the corresponding codes.

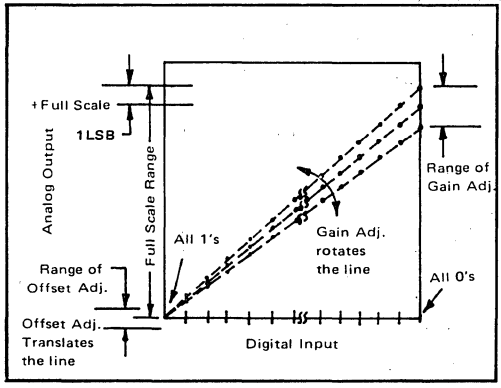


FIGURE 7. Relationship of OFFSET and GAIN Adjustment for a UNIPOLAR D/A Converter.

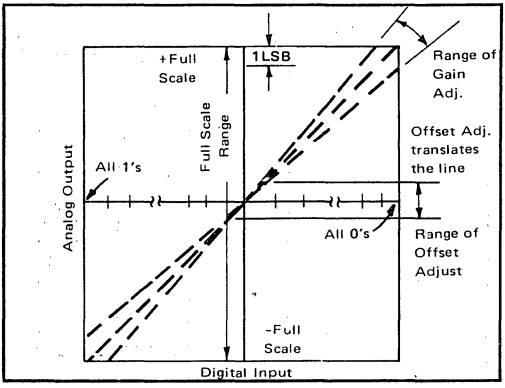


FIGURE 8. Relationship of OFFSET and GAIN Adjustments for BIPOLAR D/A Converter.

BURR-BROWN®

DAC700/702
DAC701/703

Monolithic 16-Bit DIGITAL-TO-ANALOG CONVERTERS

FEATURES

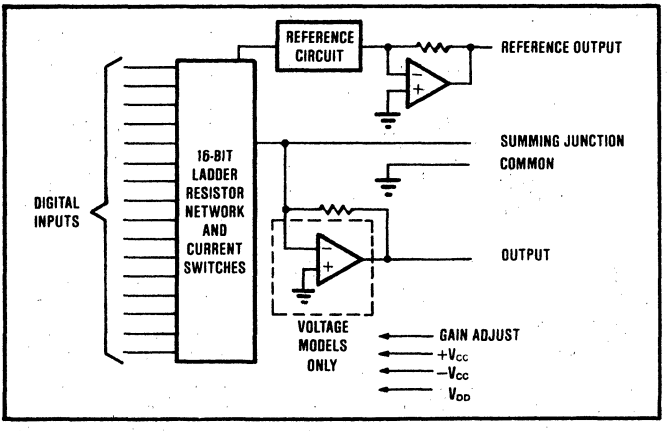
- MONOLITHIC CONSTRUCTION
- V_{OUT} AND I_{OUT} MODELS
- HIGH ACCURACY:
  Linearity Error ±0.0015% of FSR max
  Differential Linearity Error ±0.003% of FSR max
- MONOTONIC (at 15 bits) OVER FULL SPECIFICATION TEMPERATURE RANGE
- PIN-COMPATIBLE WITH DAC70, DAC71, DAC72
- LOW COST
- DUAL-IN-LINE PLASTIC AND HERMETIC CERAMIC, AND LEADLESS CHIP CARRIER PACKAGES
- /QM ENVIRONMENTAL SCREENING AVAILABLE

DESCRIPTION

This is another industry first from Burr-Brown—a complete 16-bit digital-to-analog converter that includes a precison buried-zener voltage reference and a low-noise, fast-settling output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 15-bit monotonicity over the entire specified temperature range but also a maximum end-point linearity error of ±0.0015% of full-scale range. Total full-scale gain drift is limited to ±10ppm/°C maximum (LH and CH grades).

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V, ±10V, 0 to −2mA, and ±1mA are available.

These D/A converters are packaged in hermetic 24-pin ceramic side-brazed or molded plastic and 28-contact leadless chip carrier packages. The DIP-packaged parts are pin-compatible with the voltage and current output DAC71 and DAC72 model families. The DAC700 and DAC702 are also pin-compatible with the DAC70 model family.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	DAC702/703J			DAC700/701/702/703K			DAC700/701/702/703B, S			DAC700/701/702/703L, C			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT													
DIGITAL INPUT													
Resolution			16			*			*			*	Bits
Digital Inputs[1]													
V_{IH}	+2.4		$+V_{CC}$	*		*	*		*	*		*	V
V_{IL}	−1.0		+0.8	*		*	*		*	*		*	V
I_{IH}, V_I = +2.7V			+40			*			*			*	µA
I_{IL}, V_I = +0.4V		−0.35	−0.5		*	*		*	*		*	*	mA
TRANSFER CHARACTERISTICS													
ACCURACY[2]													
Linearity Error[4]		±0.0015	±0.006		*	±0.003		*	*		±0.00075	±0.0015	% of FSR[3]
Differential Linearity Error[4]		±0.003	±0.012		*	±0.006		*	*		±0.0015	±0.003	% of FSR
Differential Linearity Error at Bipolar Zero (DAC702/703)[4]					±0.003	±0.006		±0.0015	±0.003		*	*	% of FSR
Gain Error[5]		±0.07	±0.30		*	±0.15		±0.05	±0.10		*	*	%
Zero Error[5][6]		±0.05	±0.10		*	*		*	*		*	*	% of FSR
Monotonicity Over Spec. Temp. Range	13			14			*			15			Bits
DRIFT (over specification temperature range)													
Total Error Over Temperature Range (all models)[7]		±0.08			*	±0.15		±0.05	±0.10		*	*	% of FSR
Total Full Scale Drift:													
DAC700/701		±10			*	±30		±8.5	±18		±6	±13	ppm of FSR/°C
DAC702/703		±10			*	±25		±7	±15		*	*	ppm of FSR/°C
Gain Drift (all models)		±10	±30		*	±25		±7	±15		±5	±10	ppm/°C
Zero Drift:													
DAC700/701					±2.5	±5		±1.5	±3		*	*	ppm of FSR/°C
DAC702/703		±5	±15		*	±12		±4	±10		±2.5	±5	ppm of FSR/°C
Differential Linearity Over Temp.[4]			±0.012			+0.009, −0.006			*			+0.006, −0.003	% of FSR
Linearity Error Over Temp.[4]			±0.012			±0.006			*			±0.003	% of FSR
SETTLING TIME (to ±0.003% of FSR)[8]													
DAC701/703 (V_{OUT} models)													
Full Scale Step, 2kΩ load		4			*	8		*	*		*	*	µsec
1LSB Step at Worst-Case Code[9]		2.5			*			*			*		µsec
Slew Rate		10			*			*			*		V/µsec
DAC700/702 (I_{OUT} models)													
Full Scale Step (2mA), 10 to 100Ω load		350			*	1000		*	*		*	*	nsec
1kΩ load		1			*	3		*	*		*	*	µsec
OUTPUT													
VOLTAGE OUTPUT MODELS													
DAC701 (CSB Code)					0 to +10			*					V
DAC703 (COB Code)		±10			*			*			*		V
Output Current	±5			*			*			*			mA
Output Impedance		0.15			*			*			*		Ω
Short Circuit to Common Duration		Indefinite			*			*			*		
CURRENT OUTPUT MODELS													
DAC700 (CSB Code)[10]					0 to −2			*			*		mA
Output Impedance[10]					4			*			*		kΩ
DAC702 (COB Code)[10]		±1			*			*			*		mA
Output Impedance[10]		2.45			*			*			*		kΩ
Compliance Voltage		±2.5			*			*			*		V

ELECTRICAL (CONT)

MODEL	DAC702/703J			DAC700/701/702/703K			DAC700/701/702/703B, S			DAC700/701/702/703L, C			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
REFERENCE VOLTAGE													
Voltage		+6.3		+6.0	+6.3	+6.6	+6.24	+6.3	+6.36	*	*	*	V
Source Current Available for External Loads		+2.5		+1.5	*		*	*		*	*		mA
Temperature Coefficient		±10			*	±25		*	±15		*	*	ppm/°C
Short Circuit to Common Duration		Indefinite			*			*			*		
POWER SUPPLY REQUIREMENTS													
Voltage: $+V_{CC}$	13.5	15	16.5	*	*	*	*	*	*	*	*	*	V
$-V_{CC}$	13.5	15	16.5	*	*	*	*	*	*	*	*	*	V
V_{DD}	+4.5	+5	+16.5	*	*	*	*	*	*	*	*	*	V
Current (no load):													
DAC700/702													
(I_{OUT} models)													
$+V_{CC}$		+10			*	+25		*	*		*	*	mA
$-V_{CC}$		−13			*	−25		*	*		*	*	mA
V_{DD}		+4			*	+8		*	*		*	*	mA
DAC701/703													
(V_{OUT} models)													
$+V_{CC}$		+16			*	+30		*	*		*	*	mA
$-V_{CC}$		−18			*	−30		*	*		*	*	mA
V_{DD}		+4			*	+8		*	*		*	*	mA
Power Dissipation:													
(V_{DD} = +5.0V)[11]													
DAC700/702		365			*	790		*	630		*	*	mW
DAC701/703		530			*	940		*	780		*	*	mW
Power Supply Rejection:													
$+V_{CC}$		±0.0015	±0.006		*	*		*	±0.003		*	*	% of FSR/%V_{CC}
$-V_{CC}$		±0.0015	±0.006		*	*		*	±0.003		*	*	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*		*	*		*	*	% of FSR/%V_{DD}
TEMPERATURE RANGE													
Specification:													
B, C grades							−25		+85	*		*	°C
S grades							−55		+125				°C
J, K, L grades	0		+70	*		*				0		+70	°C
Storage: Ceramic				−60		+150	*		*	*		*	°C
Plastic	−60		+100	*		*							°C

*Specification same as model to the left.

NOTES: (1) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC, and 54/74HTC compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD} = +5V to +15V. As logic "0" and logic "1" inputs vary over 0V to +0.8V and +2.4V to +10V respectively, the change in the D/A converter output voltage will not exceed ±0.0015% of FSR for the LH and CH grades, ±0.003% of FSR for the BH grade and ±0.006% of FSR for the KG grade. (2) DAC700 and DAC702 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time. (3) FSR means full-scale range and is 20V for the ±10V range (DAC703), 10V for the 0 to +10V range (DAC701). FSR is 2mA for the ±1mA range (DAC700) and the 0 to +2mA range (DAC702). (4) ±0.0015% of full-scale range is equivalent to 1LSB in 15-bit resolution. ±0.003% of full-scale range is equivalent to 1LSB in 14-bit resolution. ±0.006% of full-scale range is equivalent to 1LSB in 13-bit resolution. (5) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the zero point. (6) Error at input code $FFFF_H$ for DAC700 and DAC701, $7FFF_H$ for DAC702 and DAC703. (7) With gain and zero errors adjusted to zero at +25°C. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$. (10) Tolerance on output impedance and output current is ±30%. (11) Power dissipation is an additional 40mW when V_{DD} is operated at +15V.

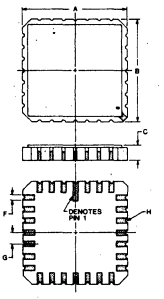
ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Common ..... 0V, +18V
$-V_{CC}$ to Common ..... 0V, −18V
V_{DD} to Common ..... 0V, +18V
Digital Data Inputs to Common ..... −1V, +18V
Reference Out to Common ..... Indefinite Short to Common
External Voltage Applied to R_F (DAC700/702) ..... ±18V
External Voltage Applied to D/A Output (DAC701/703) ..... −5V to +5V
V_{OUT} (DAC701/703) ..... Indefinite Short to Common
Power Dissipation 1000mW
Storage Temperature ..... −60°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

MECHANICAL

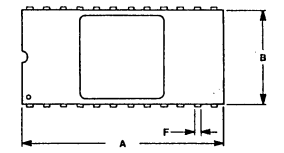
L Packages



CASE: Ceramic
CAP: Kovar, gold plated
TERMINALS: Material and composition conform to Method 2003 (solderability) of MIL-STD-883 (except Paragraph 3.2, steam aging).
WEIGHT: 0.76gm (0.026oz)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.442	.458	11.23	11.63
B	.442	.458	11.23	11.63
C	.064	.100	1.63	2.54
F	.022	.028	0.56	0.71
G	.050 BASIC		1.27 BASIC	
H	.008R TYP.		0.20R TYP.	

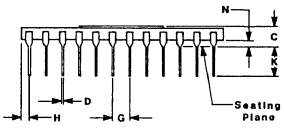
H Packages



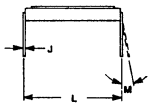
CASE: Ceramic, hermetic

MATING CONNECTOR: 0245MC

WEIGHT: 9.2gm (0.32oz)

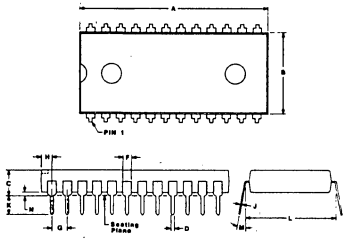


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
B	.600	.620	15.24	15.75
C	.125	.171	3.18	4.34
D	.016	.021	0.38	0.53
F	.036	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	– –	10°	– –	10°
N	.025	.060	0.64	1.52



NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

P Packages



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.233	1.283	31.32	32.59
B	.538	.575	13.67	14.61
C	.169	.224	4.29	5.70
D	.016	.023	0.38	0.58
F	.048	.062	1.08	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.016	0.20	0.38
K	.100	.132	2.54	3.36
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

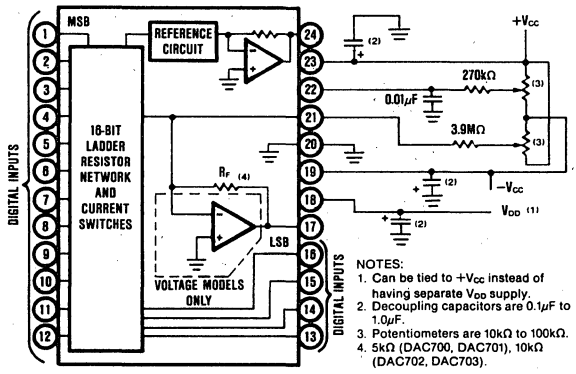
PIN ASSIGNMENTS

Pin #	H and P Packages	
	DAC700/702	DAC701/703
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 2
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 12
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	$R_{FEEDBACK}$	V_{OUT}
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	I_{OUT}	Summing Junction (Zero Adjust)
22	Gain Adjust	Gain Adjust
23	$+V_{CC}$	$+V_{CC}$
24	+6.3V Reference Output	+6.3V Reference Output

Pin #	L Packages	
	DAC700/702	DAC701/703
1	No connection	No connection
2	Bit 1 (MSB)	Bit 1 (MSB)
3	Bit 2	Bit 2
4	Bit 3	Bit 3
5	Bit 4	Bit 4
6	Bit 5	Bit 5
7	Bit 6	Bit 6
8	No connection	No connection
9	Bit 7	Bit 7
10	Bit 8	Bit 8
11	Bit 9	Bit 9
12	Bit 10	Bit 10
13	Bit 11	Bit 11
14	Bit 12	Bit 12
15	No connection	No connection
16	Bit 13	Bit 13
17	Bit 14	Bit 14
18	Bit 15	Bit 15
19	Bit 16 (LSB)	Bit 16 (LSB)
20	$R_{FEEDBACK}$	V_{OUT}
21	V_{DD}	V_{DD}
22	No connection	No connection
23	$-V_{CC}$	$-V_{CC}$
24	Common	Common
25	I_{OUT}	Summing Junction
26	Gain Adjust	Gain Adjust
27	$+V_{CC}$	$+V_{CC}$
28	+6.3V Reference Output	+6.3V Reference Output

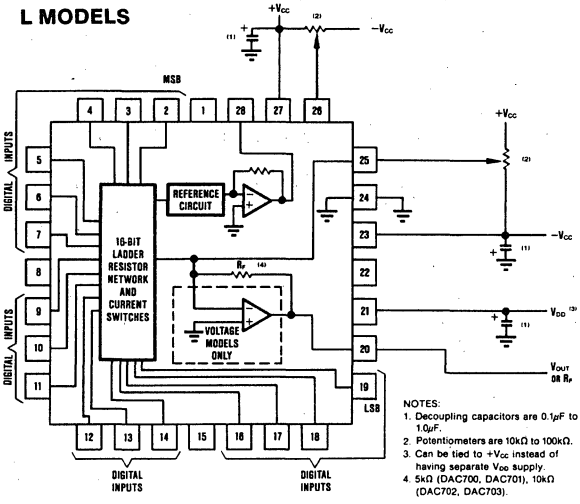
CONNECTION DIAGRAMS

H and P Models



NOTES:
1. Can be tied to $+V_{CC}$ instead of having separate V_{DD} supply.
2. Decoupling capacitors are 0.1μF to 1.0μF.
3. Potentiometers are 10kΩ to 100kΩ.
4. 5kΩ (DAC700, DAC701), 10kΩ (DAC702, DAC703).

L MODELS



NOTES:
1. Decoupling capacitors are 0.1μF to 1.0μF.
2. Potentiometers are 10kΩ to 100kΩ.
3. Can be tied to $+V_{CC}$ instead of having separate V_{DD} supply.
4. 5kΩ (DAC700, DAC701), 10kΩ (DAC702, DAC703).

ORDERING INFORMATION

Model	Package	Output Configuration	Temperature Range	Linearity Error, max at 25°C (% of FSR)	Gain Drift, max, (ppm/°C)
DAC702JP, DAC703JP	Plastic DIP	±1mA, ±10V	0 to +70°C	±0.006	±30
DAC702KP, DAC703KP	Plastic DIP	±1mA, ±10V	0 to +70°C	±0.006	±25
DAC700KH, DAC701KH	Ceramic DIP	0 to −1mA, 0 to +10V	0 to +70°C	±0.003	±25
DAC702KH, DAC703KH	Ceramic DIP	±1mA, ±10V	0 to +70°C	±0.003	±25
DAC700BH, DAC701BH	Ceramic DIP	0 to −1mA, 0 to +10V	−25 to +85°C	±0.003	±15
DAC702BH, DAC703BH	Ceramic DIP	±1mA, ±10V	−25 to +85°C	±0.003	±15
DAC700BH/QM, DAC701BH/QM	Ceramic DIP	0 to −1mA, 0 to +10V	−25 to +85°C &	±0.003	±15
DAC702BH/QM, DAC703BH/QM	Ceramic DIP	±1mA, ±10V	/QM screening	±0.003	±15
DAC700BL, DAC701BL	Ceramic LCC	0 to −1mA, 0 to +10V	−25 to +85°C	±0.003	±15
DAC702BL, DAC703BL	Ceramic LCC	±1mA, ±10V	−25 to +85°C	±0.003	±15
DAC700BL/QM, DAC701BL/QM	Ceramic LCC	0 to −1mA, 0 to +10V	−25 to +85°C &	±0.003	±15
DAC702BL/QM, DAC703BL/QM	Ceramic LCC	±1mA, ±10V	/QM screening	±0.003	±15
DAC700LH, DAC701LH	Ceramic DIP	0 to −2mA, 0 to +10V	0°C to +70°C	±0.0015	±10
DAC700CH, DAC701CH	Ceramic DIP	0 to −2mA, 0 to +10V	−25°C to +85°C	±0.0015	±10
DAC700SH, DAC701SH	Ceramic DIP	0 to −1mA, 0 to +10V	−55 to +125°C	±0.003	±15
DAC702LH, DAC703LH	Ceramic DIP	±1mA, ±10V	0°C to +70°C	±0.0015	±10
DAC702CH, DAC703CH	Ceramic DIP	±1mA, ±10V	−25°C to +85°C	±0.0015	±10
DAC702SH, DAC703SH	Ceramic DIP	±1mA, ±10V	−55 to +125°C	±0.003	±15
DAC700SH/QM, DAC701SH/QM	Ceramic DIP	0 to −1mA, 0 to +10V	−55 to +125°C &	±0.003	±15
DAC702SH/QM, DAC703SH/QM	Ceramic DIP	±1mA, ±10V	/QM screening	±0.003	±15
DAC700SL, DAC701SL	Ceramic LCC	0 to −1mA, 0 to +10V	−55 to +125°C	±0.003	±15
DAC702SL, DAC703SL	Ceramic LCC	±1mA, ±10V	−55 to +125°C	±0.006	±15
DAC700SL/QM, DAC701SL/QM	Ceramic LCC	0 to −1mA, 0 to +10V	−55 to +125°C &	±0.003	±15
DAC702SL/QM, DAC703SL/QM	Ceramic LCC	±1mA, ±10V	/QM screening	±0.003	±15

DISCUSSION OF KEY CHARACTERISTICS

DIGITAL INPUT CODES

The DAC700/701/702/703 accept complementary digital input codes in either binary format (CSB, Unipolar or COB, Bipolar). The COB models DAC702/703 may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output		
	DAC700/701 Complementary Straight Binary (CSB)	DAC702/703 Complementary Offset Binary (COB)	DAC702/703 Complementary Two's Complement (CTC)*
0000_H	+ Full Scale	+ Full Scale	−1LSB
$7FFF_H$	+1/2 Full Scale	Bipolar Zero	− Full Scale
8000_H	+1/2 Full Scale −1LSB	−1LSB	+ Full Scale
$FFFF_H$	Zero	− Full Scale	Bipolar Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2 LSB for 14 bits) for two input conditions: a full-scale range change of 20V (DAC703) or 10V (DAC701) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next).

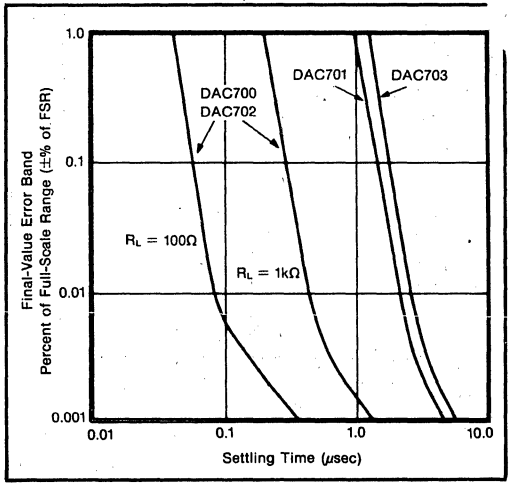


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Current Output

Settling times are specified to±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

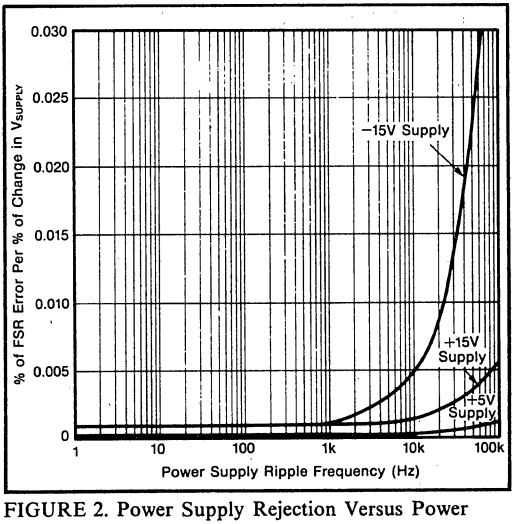


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

ENVIRONMENTAL SCREENING

/QM Screening

Screening Flow For /QM Models

Screen	MIL-STD-883 Method	Condition	Comments
Internal Visual	2010	B	
High Temperature Storage (Stabilization Bake)	1008	C	+150°C, 24hrs
Temperature Cycling	1010	C	−65 to +150°C, 10 cycles
Burn-in	1015	B	+125°C, 160hrs
Constant Acceleration	2001	E	30,000 Gs
Hermeticity Fine Leak Gross Leak	 1014 1014	 A1 or A2 C	 5×10^{-8} atm cc/sec 60psig, 2hrs
External Visual	2009		

Burr-Brown /QM models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust to Common to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar and bipolar D/A converters.

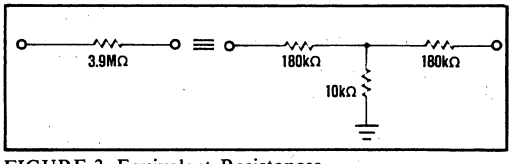


FIGURE 3. Equivalent Resistances.

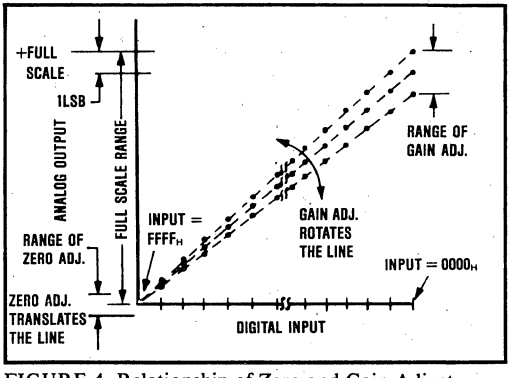


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC700 and DAC701.

Zero Adjustment

For unipolar (CSB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

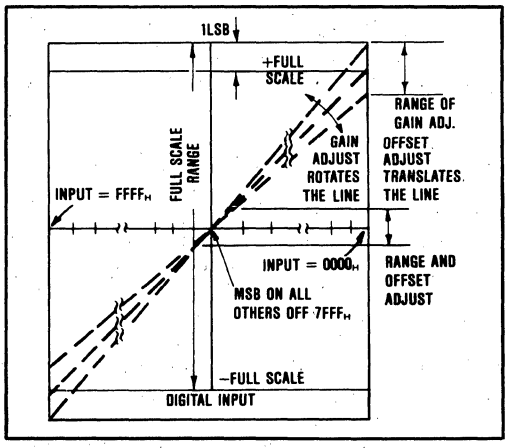


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A converters, DAC702 and DAC703.

For bipolar (COB, CTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment circuit connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 6, 7, and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and

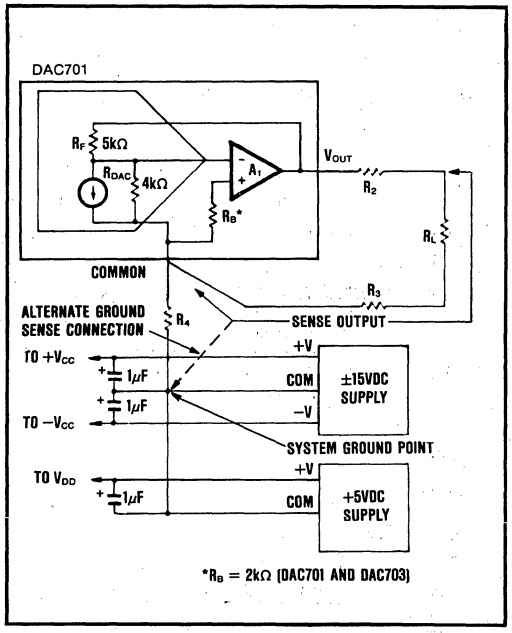


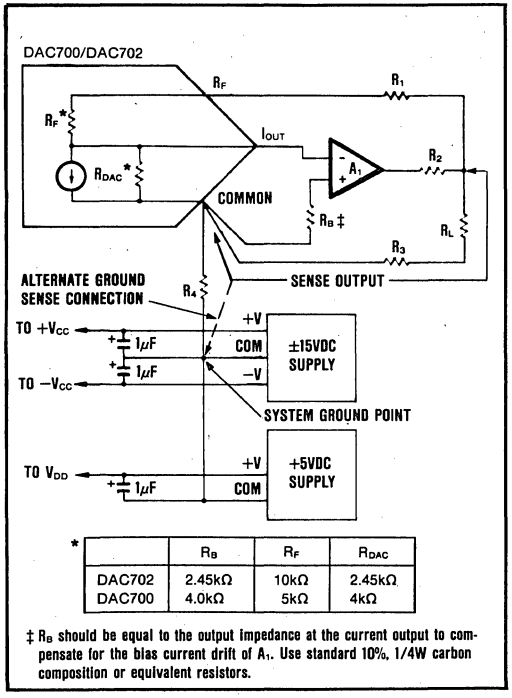
FIGURE 6. Output Circuit for Voltage Models.

TABLE II. Digital Input and Analog Output Relationships.

VOLTAGE OUTPUT MODELS						
	Analog Output					
	DAC701 Unipolar			DAC703 Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μV)	153	305	610	305	610	1224
0000$_H$ (V)	+9.99985	+9.99969	+9.99939	+9.99960	+9.99939	+9.99878
FFFF$_H$ (V)	0	0	0	–10.0000	–10.0000	–10.0000
CURRENT OUTPUT MODELS						
	Analog Output					
	DAC700 Unipolar			DAC702 Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μA)	0.031	0.061	0.122	0.031	0.061	0.122
0000$_H$ (mA)	–1.99997	–1.99994	–1.99988	–0.99997	–0.99994	–0.99988
FFFF$_H$ (mA)	0	0	0	+1.00000	+1.00000	+1.00000

therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DAC700 family because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times$ 2mA) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 6, 7, and 8.



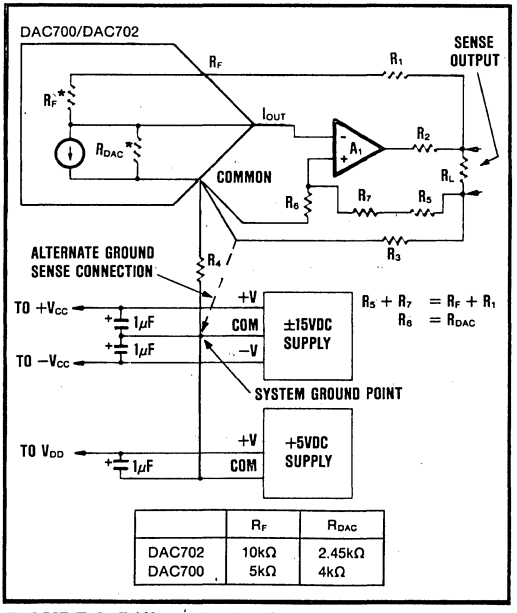
*

	R_B	R_F	R_{DAC}
DAC702	2.45kΩ	10kΩ	2.45kΩ
DAC700	4.0kΩ	5kΩ	4kΩ

‡ R_B should be equal to the output impedance at the current output to compensate for the bias current drift of A_1. Use standard 10%, 1/4W carbon composition or equivalent resistors.

FIGURE 7. Preferred External Op Amp Configuration.

Figures 7 and 8 show two methods of connecting the current output models (DAC700 or DAC702) with external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.



	R_F	R_{DAC}
DAC702	10kΩ	2.45kΩ
DAC700	5kΩ	4kΩ

FIGURE 8. Differential Sensing Output Op Amp Configuration.

If the output cannot be sensed at Common or the system ground point as mentioned above, the differential output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 7. Again the effect of R_4 is negligible.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

BURR-BROWN®

DAC705/706/707
DAC708/709

Microprocessor-Compatible 16-BIT DIGITAL-TO-ANALOG CONVERTERS

FEATURES

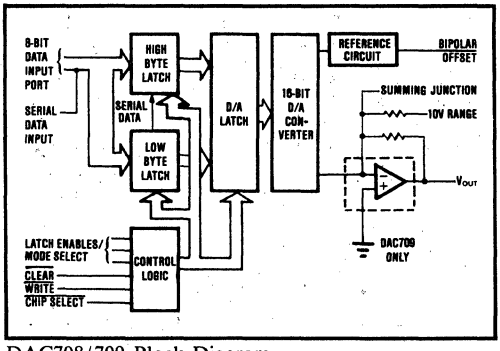
- TWO-CHIP CONSTRUCTION
- HIGH-SPEED 16-BIT PARALLEL, 8-BIT (BYTE) PARALLEL, AND SERIAL INPUT MODES
- DOUBLE-BUFFERED INPUT REGISTER CONFIGURATION
- V_{OUT} AND I_{OUT} MODELS
- HIGH ACCURACY:
  Linearity Error ±0.003% of FSR max
  Differential Linearity Error ±0.006% of FSR max
- MONOTONIC (TO 14 BITS) OVER SPECIFIED TEMPERATURE RANGE
- HERMETICALLY SEALED
- LOW COST PLASTIC VERSIONS AVAILABLE

DESCRIPTION

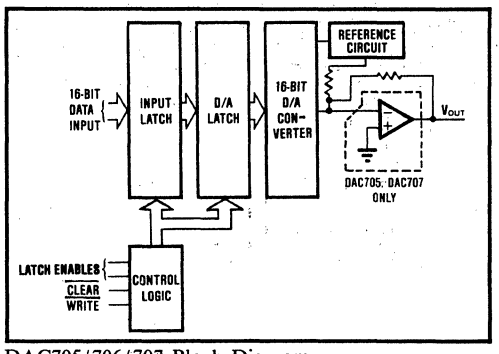
The DAC708 and DAC709 are 16-bit converters designed to interface to an 8-bit microprocessor bus. 16-bit data is loaded in two successive 8-bit bytes into parallel 8-bit latches before being transferred into the D/A latch. The DAC708 and DAC709 are current and voltage output models respectively and are in 24-pin hermetic DIPs or 24-pin plastic DIPs. Input coding is Binary Two's Complement (bipolar) or Unipolar Straight Binary (unipolar, when an external logic inverter is used to invert the MSB). In addition, the DAC708/709 can be loaded serially (MSB first). They are packaged in a 24-pin hermetic DIP or 24-pin plastic DIP.

to interface to a 16-bit bus. Data is written into a 16-bit latch and subsequently the D/A latch. The DAC705 and DAC707 are voltage output models. DAC706 is a current output model. Outputs are bipolar only (current or voltage) and input coding is Binary Two's Complement (BTC).

All models have Write and Clear control lines as well as input latch enable lines. In addition, DAC708 and DAC709 have Chip Select control lines. In the bipolar mode, the Clear input sets the D/A latch to give zero voltage or current output. They are all 14-bit accurate and are complete with reference, and, for the DAC705, DAC707, and DAC709, a voltage output amplifier.



DAC708/709 Block Diagram



DAC705/706/707 Block Diagram

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10 minute warm-up unless otherwise noted.

MODEL	DAC705/706/707/708/709KH, DAC707/709KP			DAC705/706/707/708/709BH, SH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution			16			•	Bits
Bipolar Input Code (All models)		Binary Two's Complement			•		
Unipolar Input Code[1] (DAC708/709 only)		Unipolar Straight Binary			•		
Logic Levels[2]: V_{IH}	+2.0		+5.5	•		•	V
V_{IL}	−1.0		+0.8	•		•	V
I_{IH} (V_I = +2.7V)			1			•	μA
I_{IL} (V_I = +0.4V)			1			•	μA
TRANSFER CHARACTERISTICS							
ACCURACY[3]							
Linearity Error		±0.0015	±0.003		•	•	% of FSR[4]
Differential Linearity Error[5]		±0.003	±0.006		•	•	% of FSR
at Bipolar Zero[5,6]		±0.003	±0.006		±0.0015	±0.003	% of FSR
Gain Error[7]		±0.07	±0.15		±0.05	±0.10	%
Zero Error[7]		±0.05	±0.1		•	•	% of FSR
Monotonicity Over Spec Temp Range	14			•			Bits
Power Supply Sensitivity: +V_{CC}		±0.0015	±0.006		•	±0.003	% of FSR/%V_{CC}
−V_{CC}		±0.0015	±0.006		•	±0.003	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		•	•	% of FSR/%V_{DD}
DRIFT (over specification temperature range[3])							
Gain Drift		±10	±25		±7	±15	ppm/°C
Zero Drift: Unipolar (DAC708/709 only)		±2.5	±5		±1.5	±3	ppm of FSR/°C
Bipolar (all models)		±5	±12		±4	±10	ppm of FSR/°C
Differential Linearity Over Temp[5]			+0.009, −0.006			•	% of FSR
Linearity Error Over Temp[5]			±0.006			•	% of FSR
SETTLING TIME (to ±0.003% of FSR)[8]							
Voltage Output Models							
Full Scale Step (2kΩ load)		4	8		•	•	μs
1LSB Step at Worst Case Code[9]		2.5	4		•	•	μs
Slew Rate		10			•		V/μs
Current Output Models							
Full Scale Step (2mA)							ns
10 to 100Ω load		350			•		μs
1kΩ load		1			•		
OUTPUT							
VOLTAGE OUTPUT MODELS							
Output Voltage Range							
DAC709 Unipolar (USB Code)		0 to +10			•		V
Bipolar (BTC Code)		±5, ±10			•		V
DAC707 Bipolar (BTC Code)		±10			•		V
DAC705 Bipolar (BTC Code)		±5			•		V
Output Current	±5			•			mA
Output Impedance		0.15			•		Ω
Short Circuit to Common Duration		Indefinite			•		
CURRENT OUTPUT MODELS							
Output Current Range (±30% typ)							
DAC708 Unipolar (USB Code)		0 to −2			•		mA
Bipolar (BTC Code)		±1			•		mA
DAC706 Bipolar (BTC Code)		±1					mA
Unipolar Output Impedance (±30% typ)		4.0			•		kΩ
Bipolar Output Impedance (±30% typ)		2.45			•		kΩ
Compliance Voltage		±2.5			•		V
POWER SUPPLY REQUIREMENTS							
Voltage, DAC705/706/707: +V_{CC}	+13.5	+15	+16.5	•	•	•	V
−V_{CC}	−13.5	−15	−16.5	•	•	•	V
V_{DD}	+4.5	+5	+5.5	•	•	•	V
Voltage, DAC708/709: +V_{CC}	+13.5	+15	+16.5	•	•	•	V
−V_{CC}	−13.5	−15	−16.5	•	•	•	V
V_{DD}	+4.5	+5	+5.5	•	•	•	V
Current (No load, +15V supplies)							
Current Output Models: +V_{CC}		+10	+25		•	•	mA
−V_{CC}		−13	−25		•	•	mA
V_{DD}		+5	+10		•	•	mA
Voltage Output Models: +V_{CC}		+16	+30		•	•	mA
−V_{CC}		−18	−30		•	•	mA
V_{DD}		+5	+10		•	•	mA

ELECTRICAL (CONT)

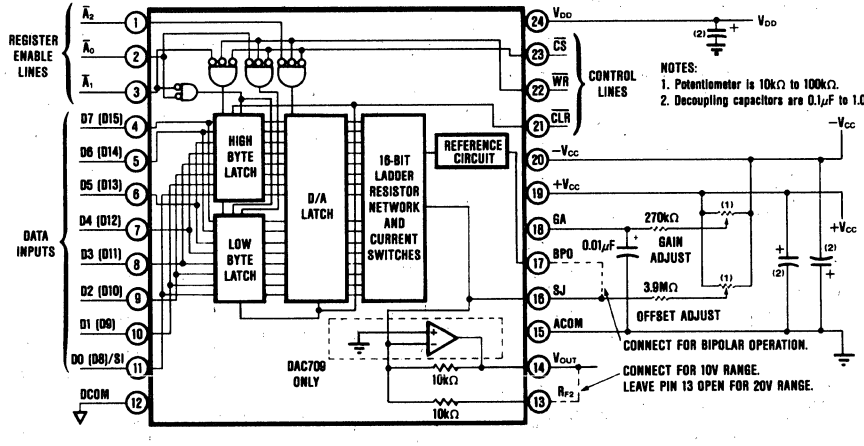
MODEL	DAC705/706/707/708/709KH, DAC707/709KP			DAC705/706/707/708/709BH, SH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS (CONT)							
Power Dissipation (±15V supplies)							
Current Output Models		370	800		•	•	mW
Voltage Output Models		535	950		•	•	mW
TEMPERATURE RANGE							
Specification: BH grades				−25		+85	°C
KP, KH grades	0		+70				°C
SH grades				−55		+125	°C
Storage, ceramic	−65		+150	•		•	°C
plastic	−60		+100				°C

*Specification same as for DAC706/707/708/709KH.

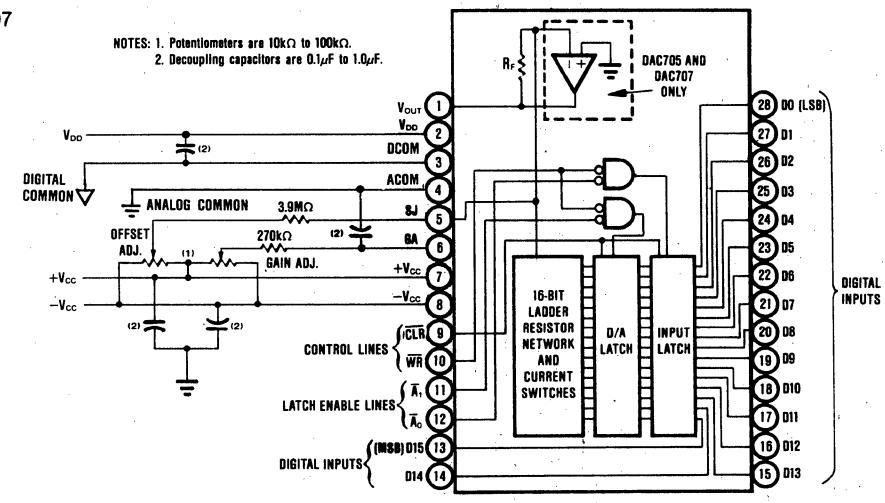
NOTES: (1) MSB must be inverted externally prior to DAC708/709 input. (2) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC and 54/74HTC compatible over the specified temperature range. (3) DAC706 and DAC708 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all tests. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) ±0.0015% of Full Scale Range is equal to 1 LSB in 16-bit resolution. ±0.003% of Full Scale Range is equal to 1 LSB in 15-bit resolution. ±0.006% of Full Scale Range is equal to 1 LSB in 14-bit resolution. (6) Error at input code 0000_H. (For unipolar connection on DAC708/709 the MSB must be inverted externally prior to D/A input.) (7) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) The bipolar worst-case code change is $FFFF_H$ to 0000_H and 0000_H to $FFFF_H$. For unipolar (DAC708/709 only) it is $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$.

CONNECTION DIAGRAMS

DAC708/709



DAC705/706/707

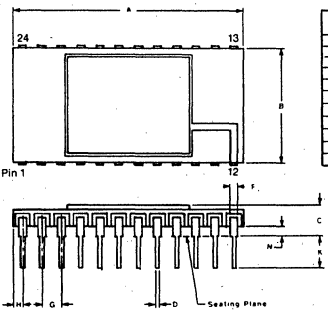


DESCRIPTION OF PIN FUNCTIONS

DAC705/706/707		Pin #	DAC708/709	
Designator	Description		Designator	Description
V_{OUT} (DAC707 and DAC705) R_F (DAC706)	Voltage output for DAC707 (±10V) and DAC705 (±5V) or an internal feedback resistor for use with an external output op amp for the DAC706.	1	$\overline{A_2}$	Latch enable for D/A latch (Active low)
V_{DD}	Logic supply (+5V)	2	$\overline{A_0}$	Latch enable for "low byte" input (Active low). When both $\overline{A_0}$ and $\overline{A_1}$ are logic "0", the serial input mode is selected and the serial input is enabled.
DCOM	Digital Common	3	$\overline{A_1}$	Latch enable for "high byte" input (Active low). When both $\overline{A_0}$ and $\overline{A_1}$ are logic "0", the serial input mode is selected and the serial input is enabled.
ACOM	Analog Common	4	D7 (D15)	Input for data bit 7 if enabling low byte (LB) latch or data bit 15 if enabling the high byte (HB) latch.
SJ (DAC705 and DAC707) I_{OUT} (DAC706)	Summing Junction of the internal output op amp for the DAC705 and DAC707, or the current output for the DAC706. Offset adjust circuit is connected to the summing junction of the output amplifier. Refer to Block Diagram.	5	D6 (D14)	Input for data bit 6 if enabling LB latch or data bit 14 if enabling the HB latch.
GA	Gain Adjust pin. Refer to Connection Diagram for gain adjust circuit.	6	D5 (D13)	Data bit 5 (LB) or data bit 13 (HB)
$+V_{CC}$	Positive supply voltage (+15V)	7	D4 (D12)	Data bit 4 (LB) or data bit 12 (HB)
$-V_{CC}$	Negative supply voltage (−15V)	8	D3 (D11)	Data bit 3 (LB) or data bit 11 (HB)
$\overline{CLR}$	Clear line. Sets the input latch to zero and sets the D/A latch to the input code that gives bipolar zero on the D/A output (Active low)	9	D2 (D10)	Data bit 2 (LB) or data bit 10 (HB)
$\overline{WR}$	Write control line (Active low)	10	D1 (D9)	Data bit 1 (LB) or data bit 9 (HB)
$\overline{A_1}$	Enable for D/A converter latch (Active low)	11	D0 (D8)/SI	Data bit 0 (LB) or data bit 8 (HB). Serial input when serial mode is selected.
$\overline{A_0}$	Enable for input latch (Active low)	12	DCOM	Digital Common
D15 (MSB)	Data bit 15 (Most Significant Bit)	13	R_{F2}	Feedback resistor for internal or external operational amplifier. Connect to pin 14 when a 10V output range is desired. Leave open for a 20V output range.
D14	Data bit 14	14	V_{OUT} R_{F1} (DAC708)	Voltage output for DAC709 or feedback resistor for use with an external output op amp for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D13	Data bit 13	15	ACOM	Analog common
D12	Data bit 12	16	SJ (DAC709) I_{OUT} (DAC708)	Summing junction of the internal output op amp for the DAC709, or the current output for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D11	Data bit 11	17	BPO	Bipolar offset. Connect to pin 16 when operating in the bipolar mode. Leave open for unipolar mode.
D10	Data bit 10	18	GA	Gain Adjust pin
D9	Data bit 9	19	$+V_{CC}$	Positive supply voltage (+15V)
D8	Data bit 8	20	$-V_{CC}$	Negative supply voltage (−15V)
D7	Data bit 7	21	$\overline{CLR}$	Clear line. Sets the high and low byte input registers to zero and, for bipolar operation, sets the D/A register to the input code that gives bipolar zero on the D/A output. (In the unipolar mode, invert the MSB prior to the D/A.)
D6	Data bit 6	22	$\overline{WR}$	Write control line
D5	Data bit 5	23	$\overline{CS}$	Chip select control line
D4	Data bit 4	24	V_{DD}	Logic supply (+5V)
D3	Data bit 3	25	No pin	
D2	Data bit 2	26	No pin	(The DAC708 and DAC709 are in 24-pin packages)
D1	Data bit 1	27	No pin	
D0 (LSB)	Data bit 0 (Least Significant Bit)	28	No pin	

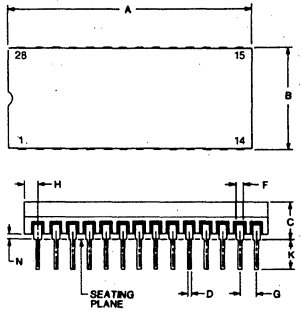
MECHANICAL

DAC708/709



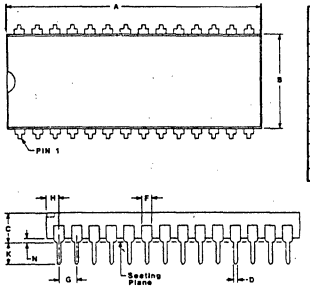
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.190	1.210	30.23	30.73
B	.580	.600	14.73	15.24
C	.140	.185	3.56	4.70
D	.016	.020	0.41	0.51
F	.030	.050	0.76	1.27
G	.100 BASIC		2.54 BASIC	
H	.035	.065	0.89	1.65
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

DAC705/706/707



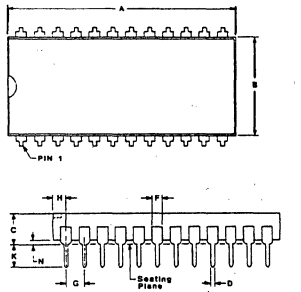
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.386	1.465	35.20	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	.38	.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.035	.095	.89	2.41
J	.009	.012	.23	.30
K	.155	.195	3.94	4.05
L	.600 BASIC		15.42 BASIC	
N	.020	.060	.51	1.52

DAC707KP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.440	1.500	36.58	38.10
B	0.475	0.520	12.07	13.20
C	0.170	0.225	4.32	5.72
D	0.016	0.024	0.40	0.60
F	0.047	0.065	1.20	1.65
G	0.100 BASIC		2.54 BASIC	
H	0.050	0.100	1.27	2.54
J	0.008	0.014	0.20	0.35
K	0.130	0.154	3.30	3.90
L	0.600 BASIC		15.24 BASIC	
M	0°C	15°C	0°C	15°C
N	0.020	0.024	0.51	0.61

DAC709KP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.250	1.300	31.75	33.02
B	0.475	0.520	12.07	13.20
C	0.170	0.225	4.32	5.72
D	0.016	0.024	0.40	0.60
F	0.047	0.065	1.20	1.65
G	0.100 BASIC		2.54 BASIC	
H	0.050	0.100	1.27	2.54
J	0.008	0.014	0.20	0.35
K	0.130	0.154	3.30	3.90
L	0.600 BASIC		15.24 BASIC	
M	0°C	15°C	0°C	15°C
N	0.020	0.024	0.51	0.61

ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON ..... 0V, +15V
+V_{CC} to COMMON ..... 0V, +18V
−V_{CC} to COMMON ..... 0V, −18V
Digital Data Inputs to COMMON ..... −0.5V, V_{DD} +0.5
DC Current any Input ..... ±10mA
Reference Out to COMMON ..... Indefinite Short to COMMON
External Voltage Applied to R_F
(pin 1, DAC706; pin 13 or 14, DAC708) ..... ±18V
External Voltage Applied to D/A Output
(pin 1, DAC707; pin 14, DAC709) ..... ±5V
V_{OUT} (DAC707, DAC709) ..... Indefinite Short to COMMON
Power Dissipation 1000mW
Storage Temperature ..... −60°C to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Model	Temperature Range	Input Configuration	Output Configuration
DAC705KH	0 to +70°C	16-bit port	±5V output
DAC705BH	−25 to +85°C	16-bit port	±5V output
DAC705BH/QM	−25 to +85°C	16-bit port	±5V output
DAC705SH	−55 to +125°C	16-bit port	±5V output
DAC705SH/QM	−55 to +125°C	16-bit port	±5V output
DAC706KH	0 to +70°C	16-bit port	±1mA output
DAC706BH	−25 to +85°C	16-bit port	±1mA output
DAC706BH/QM	25 to +85°C	16-bit port	±1mA output
DAC706SH	−55 to +125°C	16-bit port	±1mA output
DAC706SH/QM	−55 to +125°C	16-bit port	±1mA output
DAC707KH	0 to +70°C	16-bit port	±10V output
DAC707KP	0 to +70°C	16-bit port	±10V output
DAC707BH	−25 to +85°C	16-bit port	±10V output
DAC707BH/QM	−25 to +85°C	16-bit port	±10V output
DAC707SH	−55 to +125°C	16-bit port	±10V output
DAC707SH/QM	−55 to +125°C	16-bit port	±10V output
DAC708KH	0 to +70°C	8-bit port	±1mA output
DAC708BH	−25 to +85°C	8-bit port	±1mA output
DAC708BH/QM	−25 to +85°C	8-bit port	±1mA output
DAC708SH	−55 to +125°C	8-bit port	±1mA output
DAC708SH/QM	−55 to +125°C	8-bit port	±1mA output
DAC709KH	0 to +70°C	8-bit port	±10V output
DAC709KP	0 to +70°C	8-bit port	±10V output
DAC709BH	−25 to +85°C	8-bit port	±10V output
DAC709BH/QM	−25 to +85°C	8-bit port	±10V output
DAC709SH	−55 to +125°C	8-bit port	±10V output
DAC709SH/QM	−55 to +125°C	8-bit port	±10V output

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

For bipolar operation, the DAC705/706/707/708/709 accept positive-true binary two's complement input code. For unipolar operation (DAC708/709 only) the input code is positive-true straight-binary provided that the MSB input is inverted with an external inverter. See Table I.

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output	
	Unipolar Straight Binary[1] (DAC708/709 only; connected for Unipolar operation)	Binary Two's Complement (Bipolar operation; all models)
$7FFF_H$	+1/2 Full Scale −1 LSB[2]	+Full Scale
0000_H	Zero	Zero
$FFFF_H$	+Full Scale	−1LSB
8000_H	+1/2 Full Scale	−Full Scale

(1) MSB must be inverted externally. (2) Assumes MSB is inverted externally.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (−Full Scale point and +Full Scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2LSB when the input changes between adjacent codes. A negative DLE specification of −1LSB maximum (−0.0006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC705/706/707/708/709 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences at t_{min}, +25°C and t_{max}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with 0000_H applied to the D/A converter inputs over the specified temperature range. (For the DAC708/709 in unipolar mode, the MSB must be inverted.) This code corresponds to zero volts (DAC705/707 and DAC709) or zero milliamps (DAC706 and DAC708) at the analog output. The maximum change in offset at t_{min} or t_{max} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

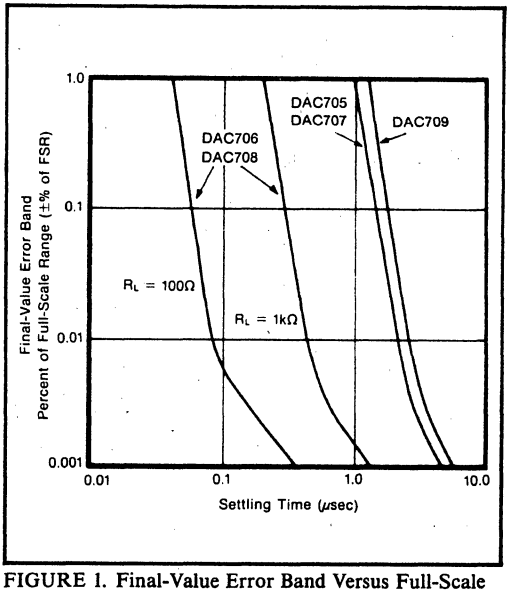


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2 LSB for 14 bits) for two input conditions: a full-scale range change of 20V (±10V) or 10V (±5V or 0 to 10V) and a 1LSB change at the "major carry", the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

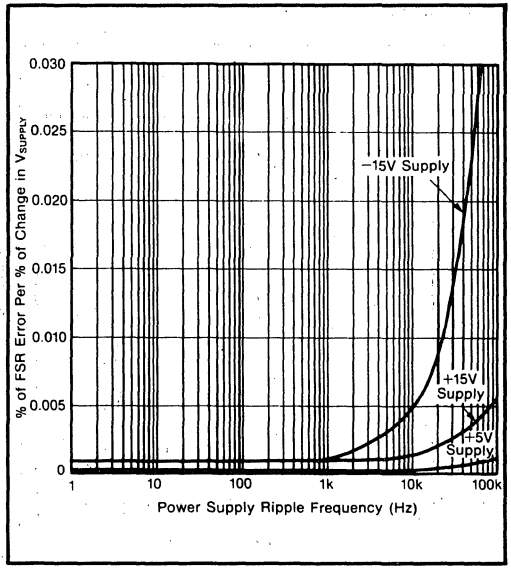


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ resistor. A 0.001μF to 0.01μF ceramic capacitor should be connected from GAIN ADJUST to ANALOG COMMON to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar D/A converters.

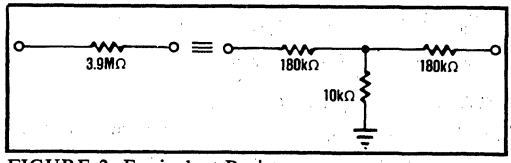


FIGURE 3. Equivalent Resistances.

Zero Adjustment

For unipolar (USB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (BTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and connection diagrams for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

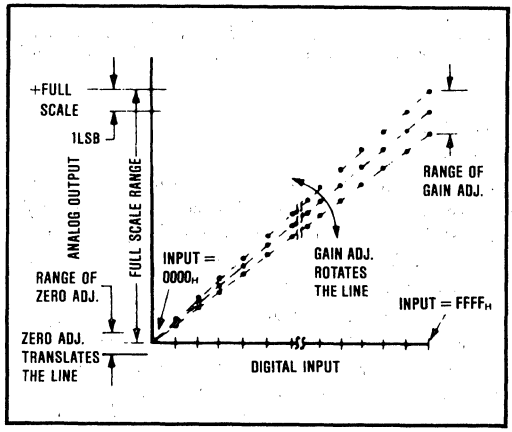


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC708 and DAC709.

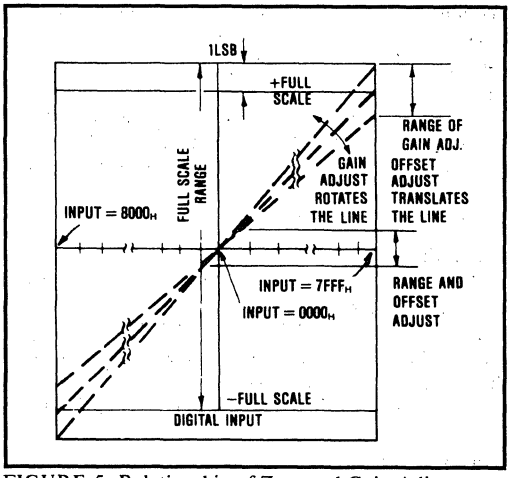


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters, DAC705/706/707 and DAC708/709.

TABLE II. Digital Input And Analog Output Voltage/Current Relationships.

VOLTAGE OUTPUT MODELS

Digital Input Code	Analog Output *Unipolar, 0 to +10V 16-Bit	15-Bit	14-Bit	Units	Digital Input Code	Analog Output Bipolar, ±10V 16-Bit	15-Bit	14-Bit	Bipolar, ±5V 16-Bit	15-Bit	14-Bit	Units
One LSB	153	305	610	μV	One LSB	305	610	1224	153	305	610	μV
$FFFF_H$	+9.99985	+9.99969	+9.99939	V	$7FFF_H$	+9.99960	+9.99939	+9.99878	+4.99980	+4.99970	+4.99939	V
0000_H	0	0	0	V	8000_H	−10.0000	−10.0000	−10.0000	−5.0000	−5.0000	−5.0000	V

CURRENT OUTPUT MODELS

Digital Input Code	Analog Output *Unipolar, 0 to −2mA 16-Bit	15-Bit	14-Bit	Units	Digital Input Code	Analog Output Bipolar, ±1mA 16-Bit	15-Bit	14-Bit	Units
One LSB	0.031	0.061	0.122	μA	One LSB	0.031	0.061	0.122	μA
$FFFF_H$	−1.99997	−1.99994	−1.99988	mA	$7FFF_H$	−0.99997	−0.99994	−0.99988	mA
0000_H	0	0	0	mA	8000_H	+1.00000	+1.00000	+1.00000	mA

*MSB assumed to be inverted externally.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and the Connection Diagrams for gain adjustment circuit connections.

INTERFACE LOGIC AND TIMING

DAC708/709

The signals CHIP SELECT ($\overline{CS}$), WRITE ($\overline{WR}$), register enables ($\overline{A_0}$, $\overline{A_1}$, and $\overline{A_2}$) and CLEAR ($\overline{CLR}$), provide the control functions for the microprocessor interface. They are all active in the "low" or logic "0" state. $\overline{CS}$ must be low to access any of the registers. $\overline{A_0}$ and $\overline{A_1}$ steer the input 8-bit data byte to the low- or high-byte input latch respectively. $\overline{A_2}$ gates the contents of the two input latches through to the D/A latch in parallel. The contents are then applied to the input of the D/A converter. When $\overline{WR}$ goes low, data is strobed into the latch or latches which have been enabled.

The serial input mode is activated when both $\overline{A_0}$ and $\overline{A_1}$ are logic "0" simultaneously. The D0 (D8)/SI input data line accepts the serial data MSB first. Each bit is clocked in by a $\overline{WR}$ pulse. Data is strobed through to the D/A latch by $\overline{A_2}$ going to logic "0" the same as in the parallel input mode.

Each of the latches can be made "transparent" by maintaining its enable signal at logic "0". However, as stated above, when both $\overline{A_0}$ and $\overline{A_1}$ are logic "0" at the same time, the serial mode is selected.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the D/A latch to 8000_H. This is the binary code that gives a null, or zero, at the output of the D/A in the bipolar mode. In the unipolar mode, activating $\overline{CLR}$ will cause the output to go to one-half of full scale.

The maximum clock rate of the latches is 10MHz. The minimum time between write (WR) pulses for successive enables is 20nsec. In the serial input mode (DAC708 and DAC709), the maximum rate at which data can be clocked into the input shift register is 10MHz.

The timing of the control signals is given in Figure 6.

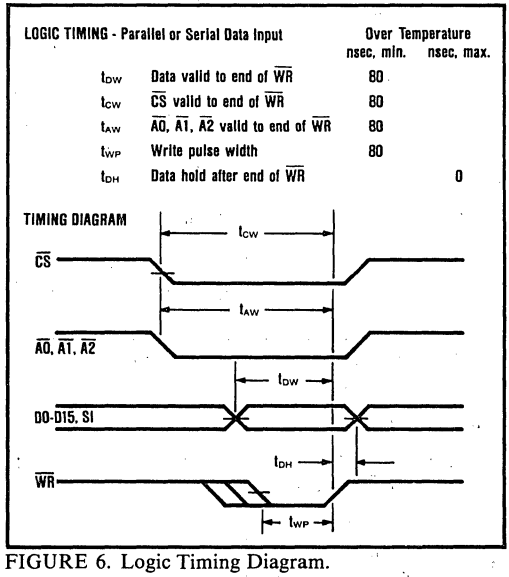


FIGURE 6. Logic Timing Diagram.

DAC706/707

The DAC705/706/707 interface timing is the same as that described above except instead of two 8-bit separately-enabled input latches, it has a single 16-bit input latch enabled by $\overline{A_0}$. The D/A latch is enabled by $\overline{A_1}$. Also, there is no serial-input mode and no CHIP SELECT ($\overline{CS}$) line.

INSTALLATION CONSIDERATIONS

Due to the extremely-high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms

of a system layout, the resistance of typical 1 ounce copper-clad printed circuit board material is approximately 1/2mΩ per square. In the example above, a 10 milliinch-wide conductor 60 milliinches long would cause a 1LSB error.

In Figures 7 and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed with gain calibration. R_3 is part of R_L if the output voltage is sensed at ANALOG COMMON.

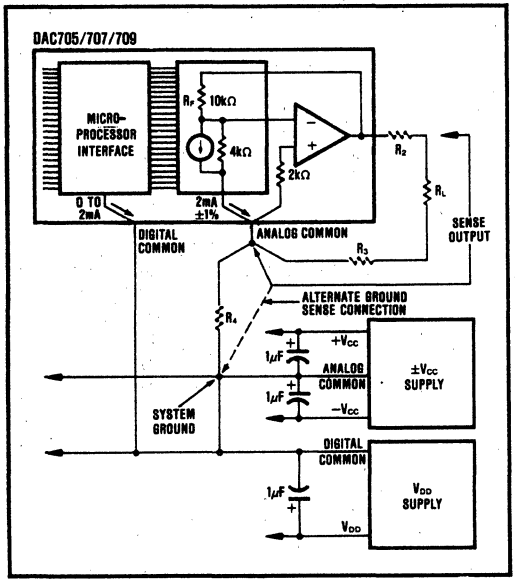


FIGURE 7. DAC705/707/709 Bipolar Output Circuit (Voltage Out).

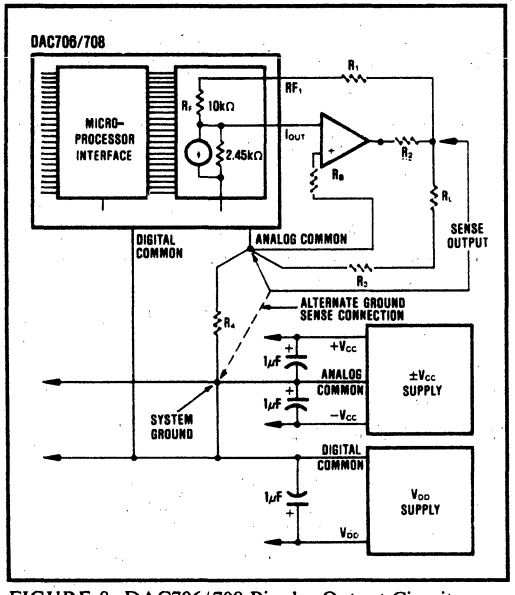


FIGURE 8. DAC706/708 Bipolar Output Circuit (with External Op Amp).

Figures 8 and 9 show two methods of connecting the currrent output model with an external precision output op amp. By sensing the output voltage at the load resistor (connecting R_F to the output of the amplifier at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

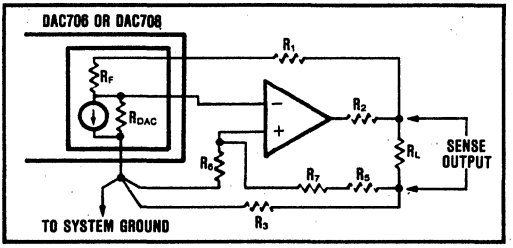


FIGURE 9. Alternate Connection for Ground Sensing at the Load (Current Output Models).

In many applications it is impractical to sense the output voltage at ANNALOG COMMON. Sensing the output voltage at the system ground point is permissible because these converters have separate analog and digital common lines and the analog return current is a near-constant 2mA and varies by only 10μA to 20μA over the entire input code range. R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 is constant and appears as a zero error that can be nulled with the zero calibration adjustment.

Another approach senses the output at the load as shown in Figure 9. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection across R_L. The effect of R_4 is negligible as explained previously.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small flux-capture cross section for any external field.

ENVIRONMENTAL SCREENING

/QM Screening

All BH and SH models are available with Burr-Brown's /QM environmental screening for enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the

screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

SCREENING FLOW FOR /QM MODELS

Screen	MIL-STD-883 Method	Condition	Comments
Internal Visual	2017	B	
High Temperature Storage (Stabilization Bake)	1008	C	+150°C, 24hrs
Temperature Cycling	1010	C	−65 to +150°C, 10 cycles
Burn-in	1015	B	+125°C, 160hrs
Constant Acceleration	2001		
28-pin pkg.		B	10,000G
24-pin pkg.		E	30,000G
Hermeticity			
Fine Leak	1014	A1 or A2	
28-pin pkg.			2×10^{-7} atmcc/sec
24-pin pkg.			5×10^{-8} atmcc/sec
Gross Leak	1014	C	60psig, 2hr
External Visual	2009		

APPLICATIONS

LOADING THE DAC709 SERIALLY ACROSS AN ISOLATION BARRIER

A very useful application of the DAC709 is in achieving low-cost isolation that preserves high accuracy. Using the serial input feature of the input register pair, only three signal lines need to be isolated. The data is applied to pin 11 in a serial bit stream, MSB first. The WR input is used as a data strobe, clocking in each data bit. A RESET signal is provided for system startup and reset. These three signals are each optically isolated. Once the 16 bits of serial data have been strobed into the input register pair, the data is strobed through to the D/A register by the "carry" signal out of a 4-bit binary synchronous counter that has counted the 16 WR pulses used to clock in the data. The circuit diagram is given in Figure 10.

CONNECTING MULTIPLE DAC707s TO A 16-BIT MICROPROCESSOR BUS

Figure 11 illustrates the method of connecting multiple DAC707s to a 16-bit microprocessor bus. The circuit shown has two DAC707s and uses only one address line to select either the input register or the D/A register. An external address decoder selects the desired converter.

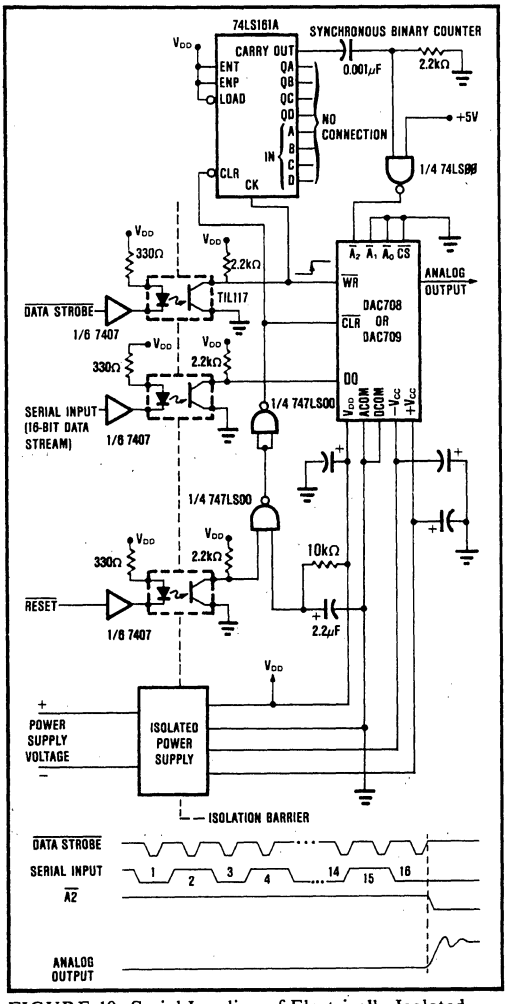


FIGURE 10. Serial Loading of Electrically Isolated DAC708/709.

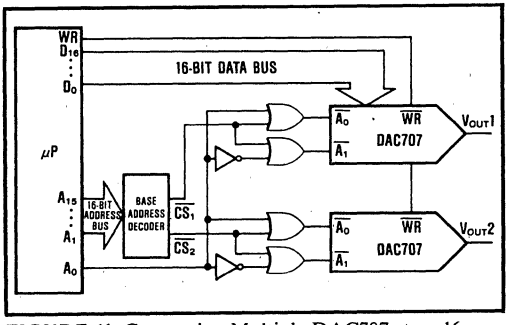


FIGURE 11. Connecting Multiple DAC707s to a 16-Bit Microprocessor.

BURR-BROWN®

DAC710
DAC711

Monolithic 16-Bit
ROBOTICS DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- DESIGNED SPECIFICALLY FOR CLOSED-LOOP SERVO-CONTROL APPLICATIONS
- MONOTONIC TO 15 BITS OVER TEMPERATURE
- MONOLITHIC CONSTRUCTION
- V_{OUT} AND I_{OUT} MODELS
- PIN-COMPATIBLE WITH DAC702, DAC703
- VERY-LOW COST FOR MULTIPLE-CHANNEL APPLICATIONS

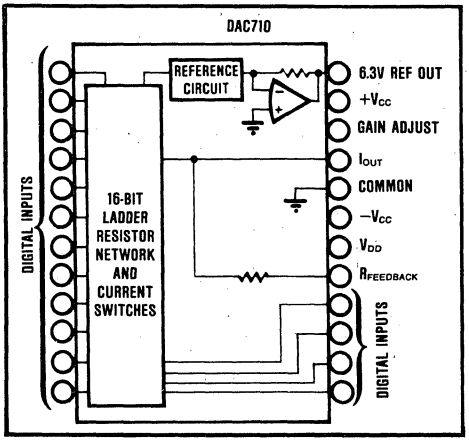
DESCRIPTION

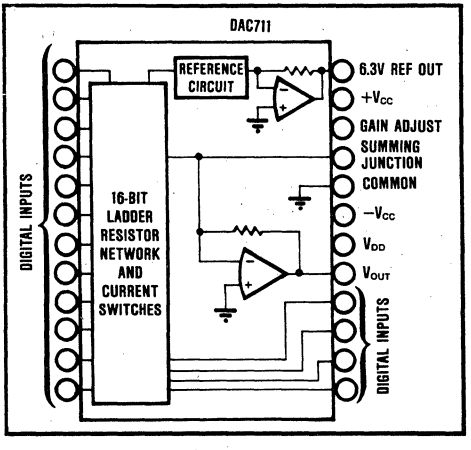
Robotics, numerical controllers, and other applications that involve the driving of servomotors require D/A converters that have very-good differential linearity around the zero output point. The DAC710KH (current output) and DAC711KH (voltage output) have been optimized for this characteristic.

DAC710 and DAC711 are complete 16-bit D/A converters on one chip. They include a precision buried-zener voltage reference, a fast settling operational amplifier (DAC711 only) as well as the D/A converter circuits. A combination of current switch design techniques accomplishes a guaranteed monotonicity of 15 bits around Bipolar Zero over the entire specification temperature range, 0°C to +70°C.

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C-, and 54/74HC-compatible over the entire temperature range. Outputs are ±10V for the DAC711KH and ±1mA for the DAC710KH.

This D/A family is pin-compatible with the voltage and current output DAC703 and DAC702 model families. These D/A converters are packaged in 24-pin ceramic side-brazed packages that are hermetically sealed.





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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and rated power supplies and after 10 minutes of warm-up time unless otherwise noted.

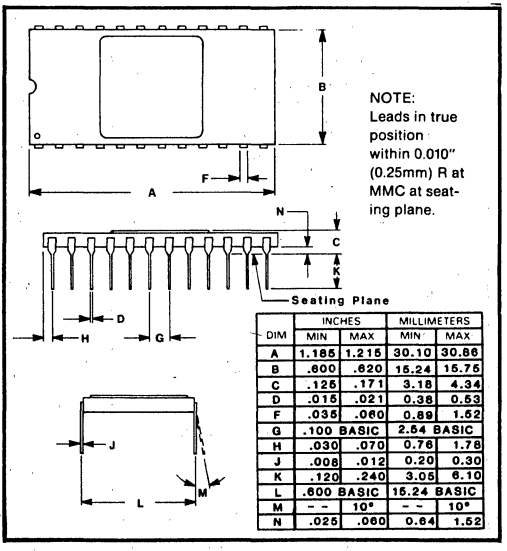
MODEL	DAC710KH/DAC711KH			UNITS
	MIN	TYP	MAX	
INPUT				
DIGITAL INPUT				
Resolution			16	Bits
Digital Inputs[1]: V_{IH}	+2.4		+V_{CC}	V
V_{IL}	−1.0		+0.8	V
I_{IH}, V_I = +2.7V			+40	µA
I_{IL}, V_I = +0.4V		−0.35	−0.5	mA
TRANSFER CHARACTERISTICS				
ACCURACY[2]				
Differential Linearity Error (near bipolar zero)[4][5]			+0.006, −0.003	% of FSR[3]
Monotonicity (near bipolar zero)[4]	15			Bits
Linearity Error			±0.0045	% of FSR
Gain Error[6]		±0.15	±0.30	%
Bipolar Zero Error[6][7]		±0.05	±0.1	% of FSR
DRIFT (over specification temperature range)				
Differential Linearity Error (near bipolar zero) over Temperature[4][5]			+0.009, −0.003	% of FSR
Monotonicity (near bipolar zero) over Temperature[4]	15			Bits
Linearity Error over Temperature			±0.009	% of FSR
Gain Drift		±25	±50	ppm/°C
Bipolar Zero Drift		±5	±12	ppm of FSR/°C
SETTLING TIME (to ±0.003% of FSR)[8]				
DAC711 (V_{OUT} Models)				
Full Scale Step (2kΩ load)		4	8	µsec
For 1LSB Step Change at Worst-Case Code[9]		2.5	4	µsec
Slew Rate		10		V/µsec
DAC710 (I_{OUT} Models)				
Full Scale Step (2mA): 10Ω to 100Ω load		350		nsec
1kΩ load		1		µsec
OUTPUT				
VOLTAGE OUTPUT				
DAC711		±10		V
Output Current	±5			mA
Output Impedance		0.15		Ω
Short Circuit to Common Duration		Indefinite		
CURRENT OUTPUT				
DAC710				
Output Range (±30% typ)		±1		mA
Output Impedance (±30% typ)		4.0		kΩ
Compliance	−2.5		+2.5	V
REFERENCE VOLTAGE				
Voltage		+6.3		V
Source Current Available for External Loads		+2.5		mA
Short Circuit to Common Duration		Indefinite		
POWER SUPPLY REQUIREMENTS				
Voltage: +V_{CC}	+13.5	+15	+16.5	V
−V_{CC}	−13.5	−15	−16.5	V
V_{DD}	+4.5	+5	+16.5	V
Current: (No Load)				
DAC711 (V_{OUT} Model): +V_{CC}		+16	+30	mA
−V_{CC}		−18	−30	mA
V_{DD}		+4	+8	mA
DAC710 (I_{OUT} Model): +V_{CC}		+10	+25	mA
−V_{CC}		−13	−25	mA
V_{DD}		+4	+8	mA
Power Dissipation (V_{DD} = +5.0V)[10]: DAC711		530	940	mW
DAC710		365	790	mW
Power Supply Rejection: +V_{CC}		±0.003	±0.006	% of FSR/%V_{CC}
−V_{CC}		±0.003	±0.006	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001	% of FSR/%V_{DD}
TEMPERATURE RANGE				
Specification	0		+70	°C
Storage	−60		+150	°C

NOTES: (1) Digital inputs are TTL-, LSTTL-, 54/74C-, 54/74HC-, and 54/74HTC-compatible over the operating voltage range of V_{DD} +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD} = +5V to +15V. As logic "0" and logic "1" inputs vary over 0V to +0.8V and +2.4V to +10V, respectively, the change in the D/A converter output voltage will not exceed +0.006% of FSR. (2) DAC710KH is specified and tested with an external output operational amplifier using the internal feedback resistor in all parameters except settling time. (3) FSR means Full Scale Range and is 20V for the DAC711KH and 2mA for the DAC710KH. (4) This specification is for +2048 consecutive codes around the bipolar zero code; that is, from $77FF_H$ to $87FF_H$. (5) ±0.003% of FSR is 1LSB for 15-bit resolution. (6) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (7) Error at input code $7FFF_H$, bipolar zero. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$. (10) Power dissipation is an additional 40mW when V_{DD} is operated at +15V.

PIN ASSIGNMENTS

Pin No.	Function	
	DAC710	DAC711
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 2
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 10
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	$R_{FEEDBACK}$	V_{OUT}
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	I_{OUT}	Summing Junction (Zero Adjust)
22	Gain Adjust	Gain Adjust
23	$+V_{CC}$	$+V_{CC}$
24	+6.3V Ref. Out.	+6.3V Ref. Out.

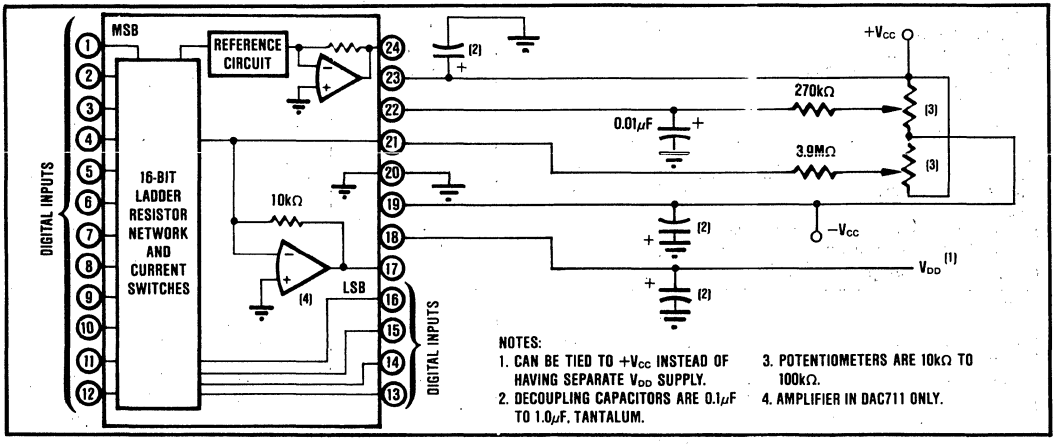
MECHANICAL



NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
B	.600	.620	15.24	15.75
C	.125	.171	3.18	4.34
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

CONNECTION DIAGRAM



NOTES:
1. CAN BE TIED TO $+V_{CC}$ INSTEAD OF HAVING SEPARATE V_{DD} SUPPLY.
2. DECOUPLING CAPACITORS ARE 0.1μF TO 1.0μF, TANTALUM.
3. POTENTIOMETERS ARE 10kΩ TO 100kΩ.
4. AMPLIFIER IN DAC711 ONLY.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON	0V to +18V
$+V_{CC}$ to COMMON	0V to +18V
$-V_{CC}$ to COMMON	0V to −18V
Digital Data Inputs (pins 1-16) to COMMON	−1V to +18V
Reference out (pin 24) to COMMON	Indefinite Short to COMMON
External Voltage Applied to R_F (pin 21, DAC710KH)	±18V
External Voltage Applied to D/A Output (pin 17, DAC711KH)	−5V to +5V
V_{OUT} (pin 17, DAC711)	Indefinite Short to COMMON
Power Dissipation	1000mW
Storage Temperature	−60°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC710/711KH accept complementary binary digital input codes in bipolar format. They may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

ACCURACY

Linearity

Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity

For servomotor control applications, differential linearity error (DLE) is one of the most important performance measures of a D/A converter. DLE is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of +0.006% of FSR maximum means that an output step size can be between 1LSB and 3LSB (at 15 bits) when the input changes between adjacent codes. A DLE specification of −0.003% maximum ensures 15-bit monotonicity.

Monotonicity

When a D/A converter is monotonic, the analog output increases or remains the same for an increasing input digital code. For ±2048 consecutive codes around bipolar zero, the DAC710KH and DAC711KH are monotonic to 15 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts-per-million per degree centigrade (ppm/°C). Gain drift is established by (1) testing the end point difference for each D/A at t_{min}, +25°C and t_{max} (2) calculating the gain error with respect to the +25°C value, and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with $7FFF_H$ (bipolar zero) applied to the digital inputs. This code corresponds to 0V (DAC711KH) or 0mA (DAC710KH) at the analog output. The maximum change in offset at t_{min} or t_{max} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in parts-per-million of full-scale range per degree centigrade (ppm of FSR/°C).

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output	
	Complementary Offset Binary (COB)	*Complementary Two's Complement (CTC)
0000_H	+ Full Scale	−1LSB
$7FFF_H$	Bipolar Zero	− Full Scale
8000_H	−1LSB	+ Full Scale
$FFFF_H$	− Full Scale	Bipolar Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

SETTLING TIME

Settling time of the D/A is the total time required for the output to settle within an error band around its final value after a change in input. Refer to Figure 1 for typical values.

Voltage Output, DAC711KH

Settling times are specified to ±0.003% of FSR for two input conditions: a full-scale range change of 20V and a ±0.006% of FSR (±1LSB in 14 bits) change at the major carry, the point at which the worst-case setting time occurs.

Current Output, DAC710KH

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output while maintaining specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2).

REFERENCE SUPPLY

All models have an internal +6.3V reference voltage derived from an on-chip buried-zener diode. This reference voltage, available at pin 24, has a tolerance of ±5%. A minimum of 1.5mA is available for external loads. Gain and Zero adjustments should be made under constant load conditions.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the bipolar offset (connected internally to the reference) from load variations.

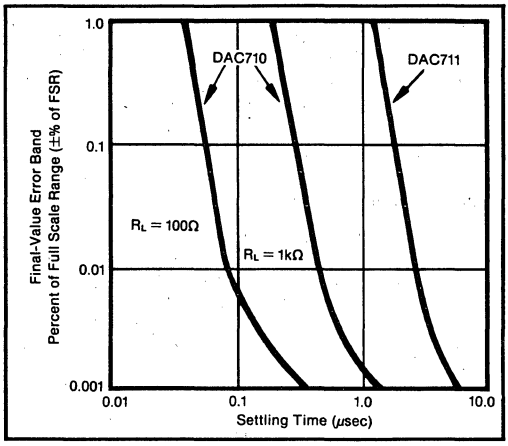


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

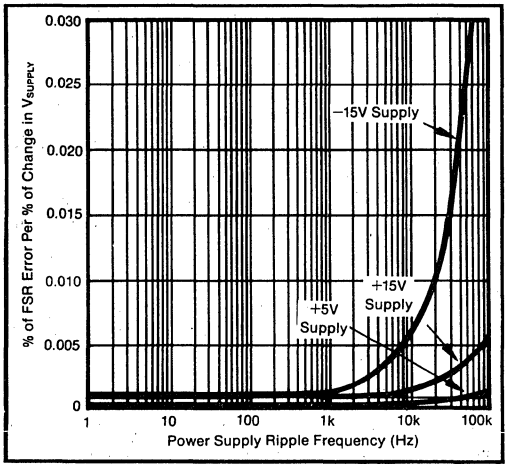


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. The 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor should be connected (even if GAIN ADJUST is not used) from GAIN ADJUST (pin 22) to COMMON to prevent noise pickup. Refer to Figure 4 for the relationship of zero and gain adjustments.

Zero Adjustment

Apply the digital input code ($7FFF_H$) that produces zero output voltage or current. See Table II for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before Gain calibration.

Gain Adjustment

Apply the digital input code (0000_H) that gives the maximum positive output voltage or current. Adjust the gain potentiometer for this positive full-scale voltage or current. See Table II for positive full-scale values and the Connection Diagram for gain adjustment circuit connections.

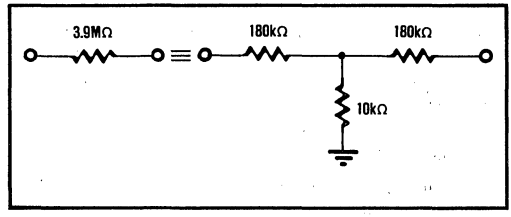


FIGURE 3. Equivalent Resistances.

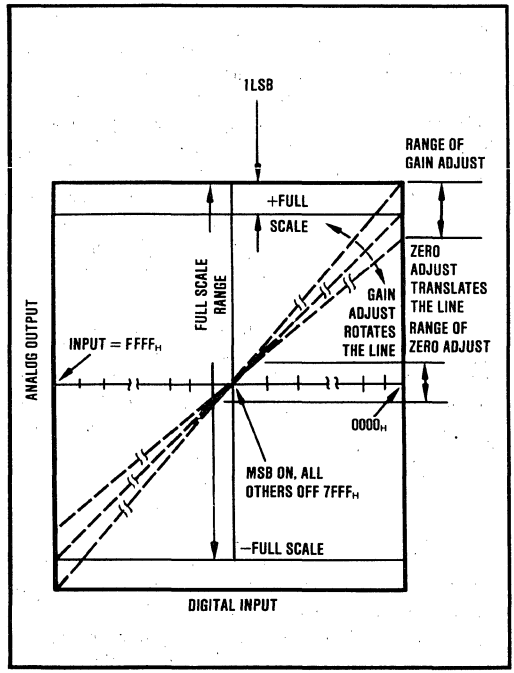


FIGURE 4. Relationship of Zero and Gain Adjustments.

TABLE II. Digital Input and Analog Output Relationships.

Digital Input Code	Analog Output							
	DAC710 Current Output				DAC711 Voltage Output			
	16-bit	15-bit	14-bit	Units	16-bit	15-bit	14-bit	Units
1LSB	0.031	0.061	0.122	μA	305	610	1224	μV
0000_H	−0.99997	−0.99994	−0.99988	mA	+9.99960	+9.99939	+9.99878	V
$7FFF_H$	0.00000	0.00000	0.00000	mA	0.00000	0.00000	0.00000	V
$FFFF_H$	+1.00000	+1.00000	+1.00000	mA	−10.0000	−10.0000	−10.0000	V

INSTALLATION CONSIDERATIONS

Due to the extremely high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Ignoring contact resistance, less than six inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 5, 6, and 7, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance (R_L) is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at COMMON (pin 20), and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at pin 20. Sensing the output voltage at the system ground point is permissible with the DAC710/711 because the D/A converter is designed to have a constant return current of approximatley 2mA flowing from pin 20. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times 2mA$) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 5, 6, and 7.

Figures 6 and 7 show two methods of connecting the current output model (DAC710KH) with external precision output operational amplifiers. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain. If the output cannot be sensed at COMMON (pin 20), or the system ground point as mentioned above, then the differential output circuit shown in Figure 7 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7

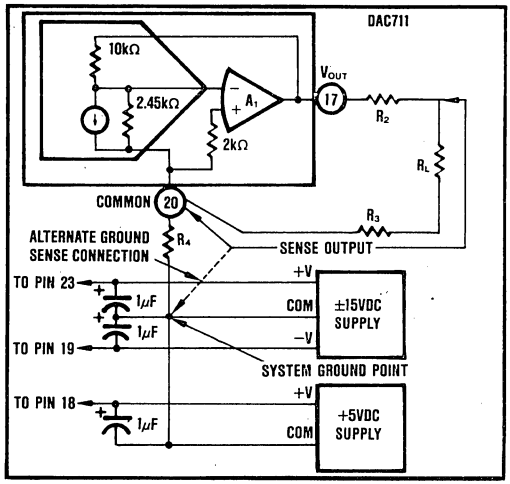


FIGURE 5. Output Circuit for DAC711.

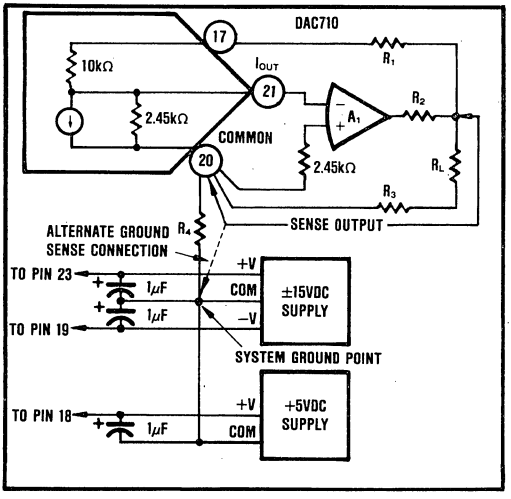


FIGURE 6. Preferred External Op Amp Configuration for DAC710.

must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 7 can be reduced to the one shown in Figure 6. Again, the effect of R_4 is negligible.

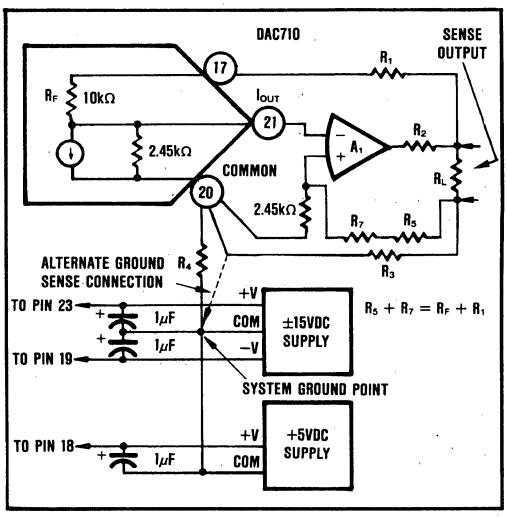


FIGURE 7. Differential Sensing Output Op Amp Configuration for DAC710.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation pickup is small loop area. If a signal lead and its return conductor are wired close together, they present a small flux-capture cross section for external fields.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT D/A'S

DAC710KH is a current output device and will drive the summing junction of an op amp to produce an output voltage as shown in Figure 8. Use of the internal feedback resistor (pin 17) is required to obtain specified gain accuracy and low gain drift.

DAC710KH can be scaled for any desired voltage range with an external feedback resistor at the expense of increased drift with temperature. The resistors in the DAC710KH ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 9.

OUTPUTS LARGER THAN 20V RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use an I_{OUT} value of ±1mA to calculate the output voltage range (see Figure 10). Use protection diodes as shown when a high voltage op amp is used.

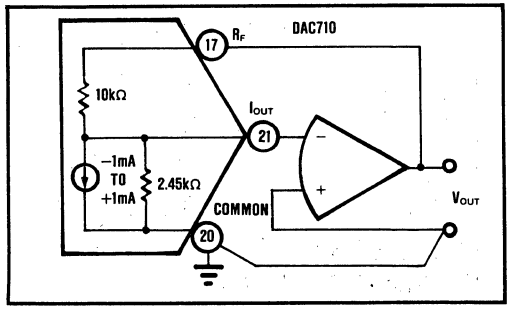


FIGURE 8. External Op Amp Using Internal Feedback Resistors (DAC710).

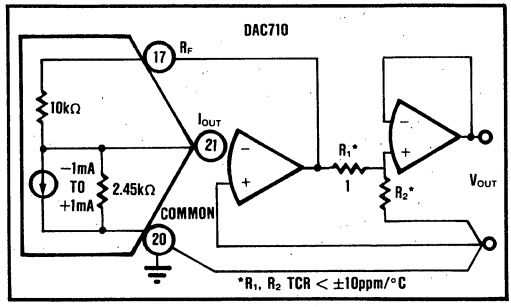


FIGURE 9. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift (DAC710).

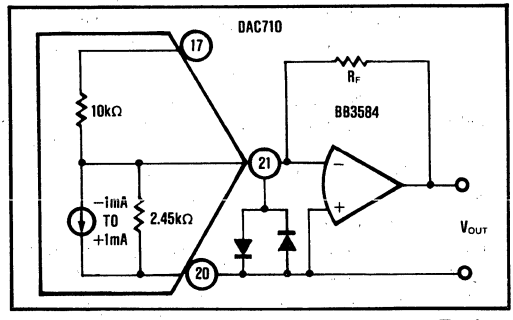


FIGURE 10. External Op Amp Using External Feedback Resistors (DAC710).

ORDERING INFORMATION

Model	Package	Temp. Range	Output
DAC710KH	Hermetic Ceramic	0°C to +70°C	Current, ±1mA
DAC711KH	Hermetic Ceramic	0°C to +70°C	Voltage, ±10V

BURR-BROWN®

DAC800
DAC800P

Integrated Circuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST HIGH RELIABILITY SINGLE-CHIP REPLACEMENT FOR INDUSTRY STANDARD DAC80
- 12-BIT RESOLUTION
- ±1/2LSB MAXIMUM NONLINEARITY, 0°C to +70°C
- GUARANTEED MONOTONICITY, 0°C to +70°C
- DUAL-IN-LINE PACKAGE WITH INDUSTRY STANDARD (DAC80) PINOUT
- HERMETIC PACKAGE (optional)
- TWO PACKAGE OPTIONS: hermetic side-brazed and molded plastic
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES

DESCRIPTION

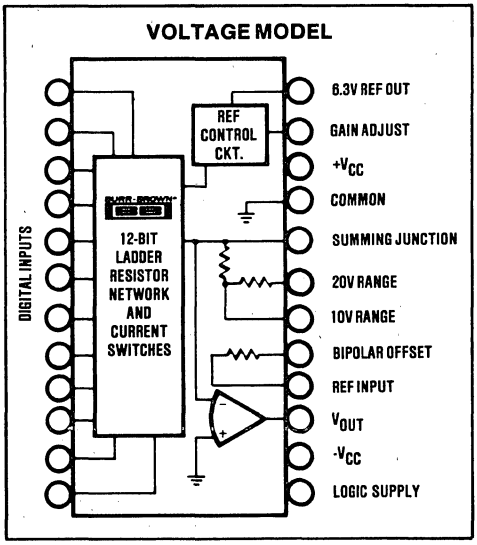
The DAC800 is a third-generation monolithic Integrated Circuit that is a pin-for-pin equivalent to the industry-standard DAC80 first introduced by Burr-Brown. It has all of the functions of its predecessor plus faster settling time and enhanced reliability because of its monolithic construction.

The current output model of the DAC800 is a single-chip integrated circuit containing a subsurface zener reference diode, high speed current switches, and laser-trimmed thin-film resistors. The DAC800 provides output voltage ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V (V models) or output current ranges of ±1.175mA or 0 to −2.35mA (I model).

This high accuracy converter offers a maximum nonlinearity error of ±1/2LSB, ±30ppm/°C maximum gain drift and guaranteed monotonicity, all over 0°C to +70°C. In the bipolar configuration, total drift is guaranteed to be less than 25ppm of FSR/°C.

The DAC800 is in a 24-pin dual-in-line package with the popular DAC80 pinout. Two package options are available: a hermetic ceramic side-brazed package and a low-cost molded plastic package.

For designs that require a wide temperature range, see Burr-Brown models DAC850 and DAC851.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

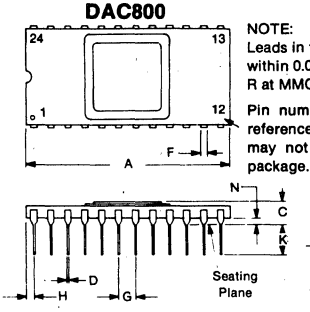
ELECTRICAL

Typical at +25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

MODEL	DAC800, DAC800P			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT				
Resolution			12	bits
Logic Levels				
(over spec. temp. range)[1]				
V_{IH} (Logic "1")	+2		16.5	VDC
V_{IL} (Logic "0")	0		+0.8	VDC
I_{IH} (V_{IN} = +2.4V)			+20	μA
I_{IL} (V_{IN} = +0.4V)			−0.36	mA
ACCURACY				
Linearity Error at 25°C		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	+1, −3/4	LSB
Gain Error[2]		±0.1	±0.3	%
Offset Error[2]		±0.05	±0.15	% of FSR[3]
POWER SUPPLY SENSITIVITY				
+15V and +5V Supplies		±0.0001	±0.001	% of FSR/%V_{CC}
−15V Supply		±0.003	±0.006	% of FSR/%V_{CC}
DRIFT[4] (0°C to +70°C)				
Bipolar Drift (±full-scale drift for the bipolar connection)		±10	±25	ppm of FSR/°C
Total Error Over 0°C to +70°C				
Unipolar		±0.06	±0.15	% of FSR
Bipolar		±0.05	±0.12	% of FSR
Gain		±10	±30	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	+1, −7/8	LSB
Linearity Error 0°C to +70°C			±1/2	LSB
Monotonicity Temp. Range, min	0		+70	°C
CONVERSION SPEED, V models				
Settling Time to ±0.01% of FSR				
For FSR Change				
20V range, 2kΩ load		3	5	μs
10V range, 2kΩ load		2.5	4	μs
For 1LSB Change, Major Carry, 2kΩ load		1.5		μs
Slew Rate, 2kΩ load	10	15		V/μs
CONVERSION SPEED, I model				
Settling Time to ±0.01% of FSR				
For FSR Change				
10Ω to 100Ω load		300		ns
1kΩ load		1		μs
ANALOG OUTPUT, V models				
Ranges ($\pm V_{CC}$ = 15V)	±2.5, ±5, ±10, 0 to +5, 0 to +10			V
Output Current[6]	±5			mA
Output Impedance (DC)		0.05		Ω
Short Circuit to Common, Duration		Indefinite		
ANALOG OUTPUT, I model				
Ranges: Bipolar	±0.88	±1.175	±1.47	mA
Unipolar	0 to −1.76	0 to −2.35	0 to −2.94	mA
Output Impedance: Bipolar		3.1		kΩ
Unipolar		7.2		kΩ
Compliance	−2.5		+2.5	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6.30	+6.37	V
Current (for external loads), Source	1.5	2.5		mA
Tempco of Drift		±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS				
$\pm V_{CC}$	±11.4	±15	±16.5	VDC
V_{DD}[7]	+4.5	+5.0	+16.5	VDC
Supply Drain				
+15V, −15V (no load)		+8, −20	+12, −25	mA
+5V (logic supply)		+7	+10	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating[8]	−25		+85	°C
Storage, DAC800P	−60		+100	°C
DAC800	−65		+150	°C

MECHANICAL

DAC800



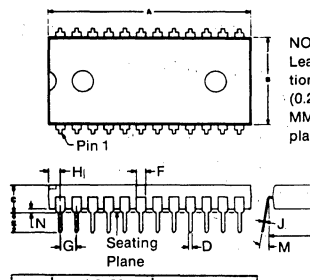
NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on kage. package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

CASE: Ceramic
MATING CONNECTOR: 0245MC
WEIGHT: 4.1 grams (0.15 oz.)

DAC800P



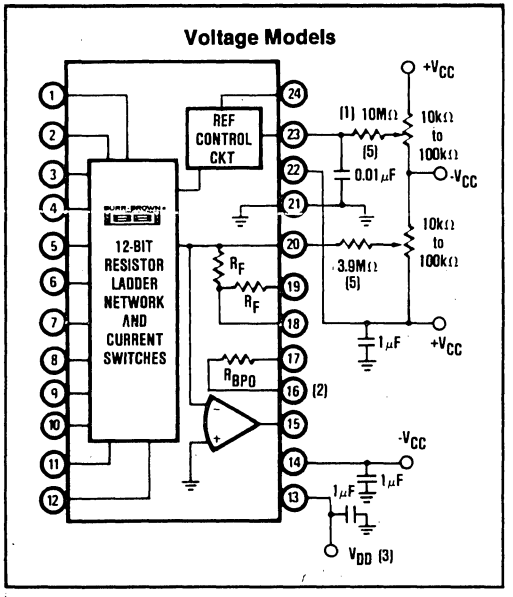
NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

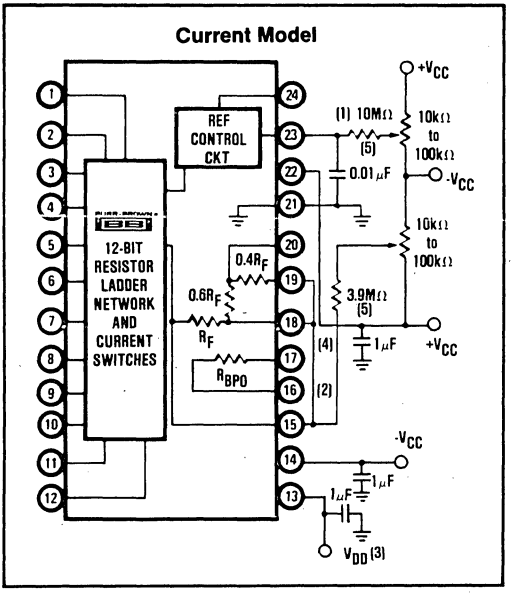
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.233	1.283	31.32	32.59
B	.538	.575	13.67	14.61
C	.169	.224	4.29	5.69
D	.015	.023	0.38	0.58
F	.043	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

CASE: Plastic
MATING CONNECTOR: 0245MC
WEIGHT: 3.7 grams (0.13 oz.)

NOTES:
(1) Refer to Logic Input Compatibility.
(2) Adjustable to zero with external trim potentiometer.
(3) FSR means "Full-Scale Range" and is 20V for ±10V range, ±10V for ±5V range, etc.
(4) To maintain drift spec internal feedback resistors must be used for current output models.
(5) Includes the effects of gain, offset and linearity drift. Gain and offset errors are adjusted to zero at +25°C.
(6) For operation of V models with supply voltages of less than ±13VDC, load current must be limited to ±1mA max.
(7) Power dissipation is an additional 100mW, max, when V_{DD} is operated at +15V.
(8) Max operating temperature for DAC800P is +70°C.

CONNECTION DIAGRAMS





PIN ASSIGNMENTS

I MODEL	PIN NO.	V MODELS
(MSB) BIT 1	1	BIT 1 (MSB)
BIT 2	2	BIT 2
BIT 3	3	BIT 3
BIT 4	4	BIT 4
BIT 5	5	BIT 5
BIT 6	6	BIT 6
BIT 7	7	BIT 7
BIT 8	8	BIT 8
BIT 9	9	BIT 9
BIT 10	10	BIT 10
BIT 11	11	BIT 11
(LSB) BIT 12	12	BIT 12 (LSB)
LOGIC SUPPLY, VDD	13	LOGIC SUPPLY, VDD
-VCC	14	-VCC
IOUT	15	VOUT
REF. INPUT	16	REF. INPUT
BIPOLAR OFFSET	17	BIPOLAR OFFSET
SCALING NETWORK	18	10V RANGE
SCALING NETWORK	19	20V RANGE
SCALING NETWORK	20	SUMMING JUNCTION
COMMON	21	COMMON
+VCC	22	+VCC
GAIN ADJUST	23	GAIN ADJUST
6.3V REF. OUT	24	6.3V REF. OUT

NOTES:

1. DAC80 which may be replaced by DAC800 requires a 33MΩ resistor. DAC800 requires a 10MΩ resistor. DAC80's may also be operated with a 10MΩ resistor resulting in increased trim range.
2. Pin 16 of DAC800 is used only to connect the bipolar offset resistor. An external reference voltage may not be used with DAC800 as is possible with DAC80.
3. If connected to +VCC, which is permissible, power dissipation increases 75mW typ, 100mW max.
4. For fastest settling time connect pins 19, 18, and 15 together.
5. Values shown are for ±15V supplies. For supplies below ±13.5V use 2.7MΩ in place of 3.9MΩ and 7.5MΩ in place of 10mΩ.

ORDERING INFORMATION

Model	Output	Package
DAC800-CBI-I	Current	Side-braze
DAC800-CBI-V	Voltage	Side-braze
DAC800P-CBI-I	Current	Molded plastic
DAC800P-CBI-V	Voltage	Molded plastic

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC800 accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes; CSB, CTC, or COB.

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB ↓ ↓	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
000000000000	+Full Scale	+Full Scale	-1LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	1/2 Full Scale -1LSB	-1LSB	+Full Scale
111111111111	Zero	-Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC800 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC800 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain Drift is established by: 1) testing the end point differences for each DAC800 model at 0°C, +25°C and +70°C; 2) calculating the gain change with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C.

Offset Drift is a measure of the change in output with all "1"s on the inputs over the specified temperature range. The Offset is measured at 0°C, +25°C and +70°C. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

Bipolar Drift is a measure of the change in plus or minus full-scale output over the specification temperature range for the bipolar connection. Because Bipolar Offset Drift and Gain Drift have canceling interactions, Bipolar Drift is not simply the sum of the two. Total bipolar error over temperature is calculated using Bipolar Drift, then adding ±1/2LSB of linearity error.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

Voltage Output Models: Three settling times are specified to ±0.01% of full-scale range (FSR); two for maximum full-scale range changes of 20V, 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Model: Two settling times are specified to ±0.01% of FSR. Each is given for the current model connected with two different resistive loads: 10Ω to 100Ω and 1000Ω. Internal resistors are provided for connecting a nominal load resistance of approximately 1000Ω for output voltage ranges of ±1V and 0 to -2V.

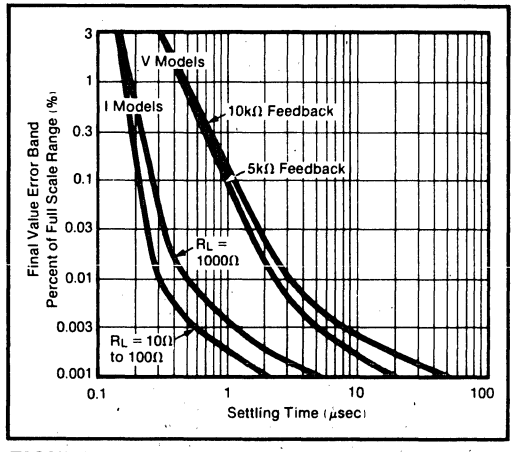


FIGURE 1. Full-Scale Range Settling Time vs Final Value Error Band.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is -2.5V to +2.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

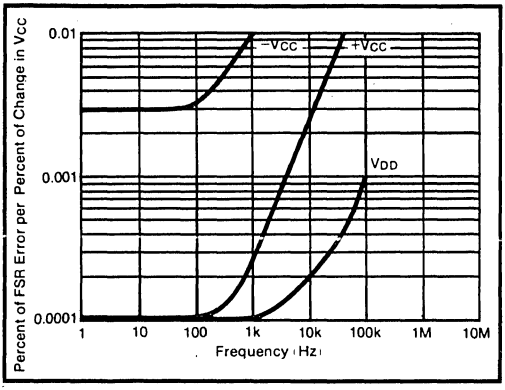


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC800 models have an on-chip +6.3 volt reference. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. Pin 16 is used only to connect the bipolar offset resistor. An external reference may not be used with DAC800. See Connection Diagrams. The reference voltage may be used to supply external circuits with 2.5mA of current (typical) in addition to the 1mA required by the bipolar offset circuit.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC800. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

±12V OPERATION

The DAC800 is fully specified for operation on ±12V power supplies. However, to use the ±10V and 0 to +10V ranges of the voltage output models, the power supplies must be ±13V or greater. All other voltage output ranges and all current output ranges provide satisfactory operation with ±11.4V supplies. The supplies should be balanced to obtain optimum performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in the connection diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC800 to prevent noise pick-up. For operation with supplies of less than ±13.5V, use 2.7MΩ and 7.5MΩ resistors in place of the 3.9MΩ and 10MΩ resistors, respectively. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in each case. The Gain Adjust (pin 23) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to reduce noise pick-up. Figures 4 and 5 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

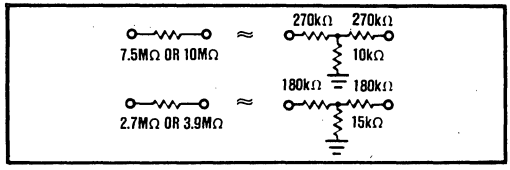


FIGURE 3. Equivalent Resistances.

Offset Adjustment: For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

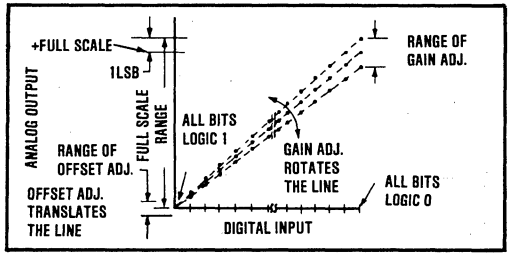


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

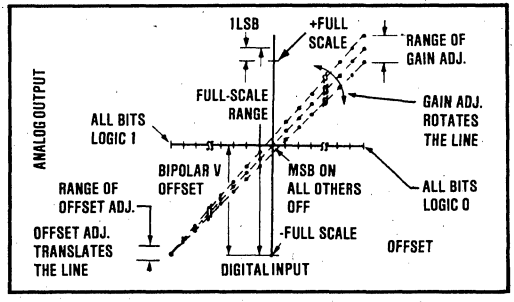


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full-scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagrams for offset adjustment connections. Offset should be adjusted prior to gain.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and the Connection Diagrams for gain adjustment connections.

TABLE II. Digital Input/Analog Output.

Digital Input	Analog Output			
	Voltage*		Current	
MSB ↓ LSB ↓	0 to +10V	±10V	0 to −2mA	±1mA
000000000000	+9.9976V	+9.9951V	−1.9995mA	−0.9995mA
011111111111	+5.0000V	0.0000V	−1.0000mA	0.0000mA
100000000000	+4.9976V	−0.0049V	−0.9995mA	+0.0005mA
111111111111	0.0000V	−10.0000V	0.0000mA	+1.0000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC800 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

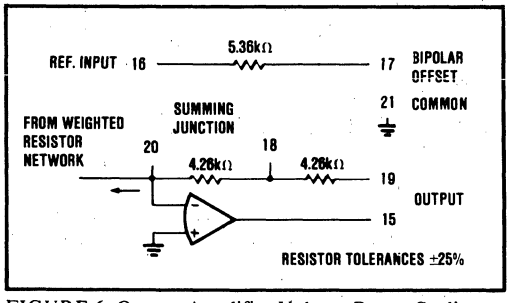


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

TABLE III. Output Voltage Range Connections - Voltage Model DAC800.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full-scale range change is specified as 3μsec for the 20-volt range and 2.5μsec for the 10-volt range.

CURRENT OUTPUT MODEL

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.

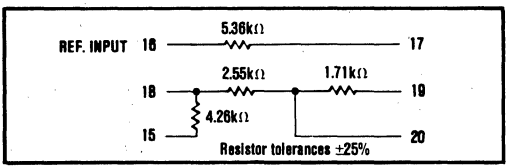


FIGURE 7. Internal Scaling Resistors.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of

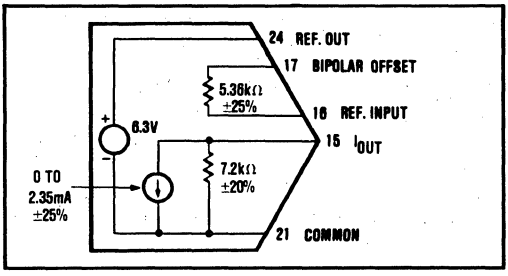


FIGURE 8. Current Output Model Equivalent Output Circuit.

±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 9 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2.35mA \left(\frac{R_L \times 7.2k\Omega}{R_L + 7.2k\Omega} \right)$$

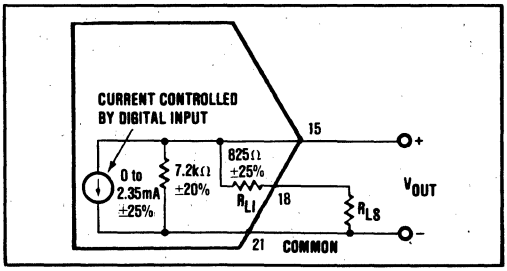


FIGURE 9. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown to an external metal film trim resistor (R_{LS}) to provide full-scale output voltage range of 0 to −2V. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift. Tolerances on internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 10; $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1.175mA\left(\frac{R_L \times 3.07k\Omega}{R_L + 3.07k\Omega}\right)$$

To achieve specified drift, connect 1.71kΩ and 2.55kΩ internal scaling resistors in parallel (R_{LI}) and add an external metal film resistor (R_{LS}) in series to obtain a full-scale output range of ±1V. The tolerances on the internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

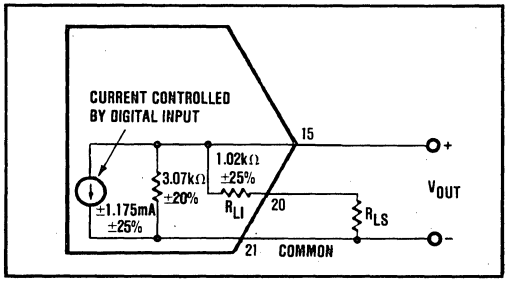


FIGURE 10. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

Driving An External Op Amp

The current output model DAC800 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. See Figure 11.

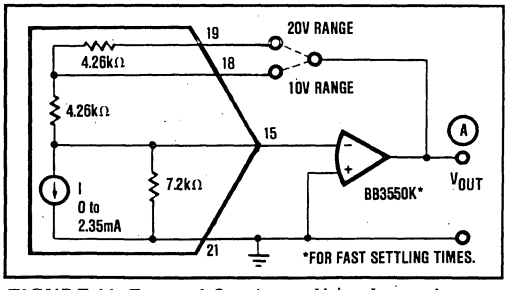


FIGURE 11. External Op Amp - Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC800 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model DAC800 provides output voltage ranges the same as the voltage model DAC800. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output DAC800.

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1.175mA ±25% for bipolar voltage ranges and -2.35mA ±25% for unipolar voltage ranges. See Figure 12. Use protection diodes when a high voltage op amp is used.

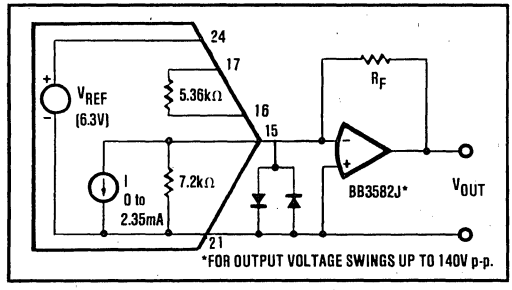


FIGURE 12. External Op Amp - Using External Feedback Resistors.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50 ppm/°C + R_F drift to total drift.

LOGIC INPUT COMPATIBILITY

DAC800 digital inputs are TTL, LSTTL and 54/74HC CMOS compatible over the operating range of V_{DD}, +5 to +15V. The input switching threshold remains at the TTL threshold over supply range of V_{DD}, +5V to +15V.

Logic "0" input current over temperature is low enough to permit driving DAC800 directly from outputs of 4000B and 54/74C CMOS devices over the logic power supply range of +5V to +15V.

BURR-BROWN®

DAC811

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- SINGLE INTEGRATED CIRCUIT CHIP
- MICROCOMPUTER INTERFACE: DOUBLE-BUFFERED LATCH
- VOLTAGE OUTPUT: ±10V, ±5V, +10V
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- ±1/2LSB MAXIMUM NONLINEARITY OVER TEMPERATURE
- GUARANTEED SPECIFICATIONS AT ±12V AND ±15V SUPPLIES
- TTL/5V CMOS-COMPATIBLE LOGIC INPUTS

DESCRIPTION

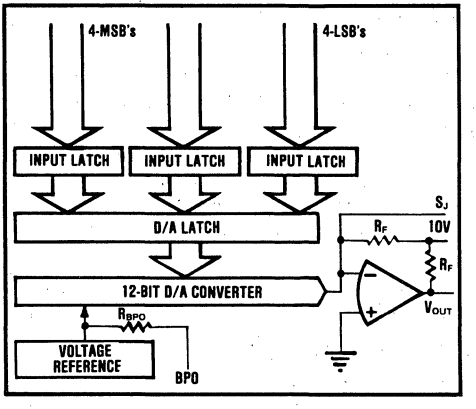
The DAC811 is a complete single-chip integrated circuit microcomputer-compatible 12-bit digital-to-analog converter. The chip includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

Microcomputer interfacing is facilitated by a double-buffered latch. The input latch is divided into three 4-bit nybbles to permit interfacing to 4-, 8-, 12- or 16-bit buses and to handle right- or left-justified data. The 12-bit data in the input latches is transferred to the D/A latch to hold the output value.

Input gating logic is designed so that loading the last nybble or byte of data can be accomplished simultaneously with the transfer of data (previously stored in adjacent latches) from adjacent input latches to the D/A latch. This feature avoids spurious analog output values while using an interface technique that saves computer instructions.

The DAC811 is laser trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (B, K, and S grades) at 25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range.

The DAC811 is available in six performance grades and three package types, as well as offering environmentally screened versions for enhanced reliability. DAC811JP and KP are specified over the temperature range of 0°C to +70°C; DAC811A and B are specified over −25°C to +85°C; DAC811R and S are specified over −55°C to +125°C. DAC811JP and KP are packaged in a reliable 28-pin plastic molded package, while DAC811A, B, R, and S are available in either a 28-pin 0.6-inch wide dual-in-line hermetically-sealed ceramic side-brazed package (H package) or a 28-terminal 0.45-inch square hermetically-sealed ceramic leadless chip carrier (L package).



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

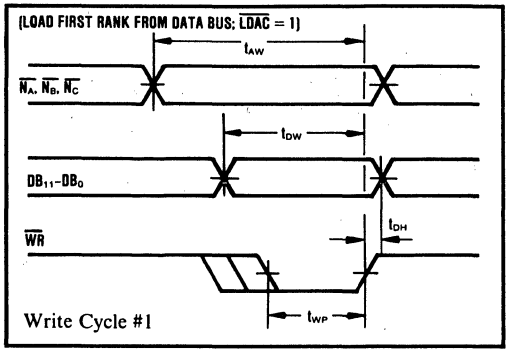
T_A = +25°C. $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

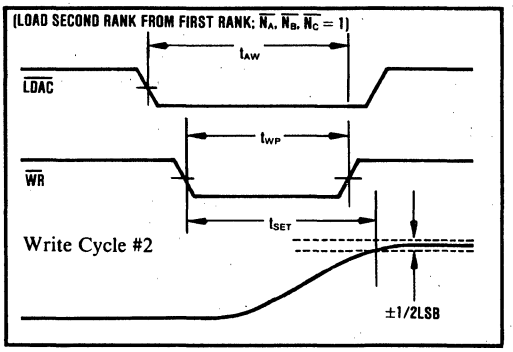
MODEL	DAC811A, JP			DAC811B, KP			DAC811R			DAC811S			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT													
DIGITAL INPUT													
Resolution			12			•			•			•	Bits
Codes[1]		USB, BOB			•			•			•		
Digital Inputs Over Temperature Range[2]													
V_{IH}	+2.0		+15	•		•	•		•	•		•	VDC
V_{IL}	0.0		+0.8	•		•	•		•	•		•	VDC
I_{IH}, V_I = +2.7V			+10			•			•			•	µA
I_{IL}, V_I = +0.4V			±20			•			•			•	µA
Digital Interface Timing Over Temperature Range													
t_{WP}, $\overline{WR}$ pulse width	50			•			•			•			nsec
$t_{AW}1$, $\overline{N_X}$ and $\overline{LDAC}$ valid to end of $\overline{WR}$	50			•			•			•			nsec
t_{DW}, data valid to end of $\overline{WR}$	80			•			•			•			nsec
t_{DH}, data valid hold time	0			•			+10			•			nsec
TRANSFER CHARACTERISTICS													
ACCURACY													
Linearity Error		±1/4	±1/2		±1/8	±1/4		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4		±1/4	±1/2	LSB
Gain Error[3]		±0.1	±0.2		•	•		•	•		•	•	%
Offset Error[3,4]		±0.05	±0.15		•	•		•	•		•	•	% of FSR[5]
Monotonicity		Guaranteed			•			•			•		
Power Supply Sensitivity, $+V_{CC}$		±0.001	±0.003		•	•		•	•		•	•	% of FSR/%V_{CC}
$-V_{CC}$		±0.002	±0.006		•	•		•	•		•	•	% of FSR/%V_{CC}
V_{DD}		±0.0005	±0.0015		•	•		•	•		•	•	% of FSR/%V_{DD}
DRIFT (over specification temperature range)													
Gain		±10	±30		±10	±20		±15	±30		±15	±30	ppm/°C
Unipolar Offset		±5	±10		±5	±7		±5	±10		±5	±7	ppm of FSR/°C
Bipolar Zero		±5	±10		±5	±7		±5	±10		±5	±7	ppm of FSR/°C
Linearity Error Over Temperature Range		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4		±1/4	±1/2	LSB
Monotonicity Over Temperature Range		Guaranteed			•			•			•		
CONVERSION SPEED													
SETTLING TIME[6] (to within ±0.01% of FSR of final value; 2kΩ load)													
For Full Scale Range Change, 20V Range		3	4		•	•		•	•		•	•	µsec
10V Range		3	4		•	•		•	•		•	•	µsec
For 1LSB Change at Major Carry[7]		1			•			•			•		µsec
Slew Rate[6]	8	12		•	•		•	•		•	•		V/µsec
OUTPUT													
ANALOG OUTPUT													
Voltage Range ($\pm V_{CC}$ = 15V)[8], Unipolar		0 to +10			•			•			•		V
Bipolar		±5, ±10			•			•			•		V
Output Current	±5			•			•			•			mA
Output Impedance (at DC)		0.2			•			•			•		Ω
Short Circuit to Common Duration		Indefinite			•			•			•		
REFERENCE VOLTAGE													
Voltage	+6.2	+6.3	+6.4	•	•	•	•	•	•	•	•	•	V
Source Current Available for External Loads	+2.0			•			•			•			mA
Temperature Coefficient		±10	±30		±10	±20		±10	±30		±10	±20	ppm/°C
Short Circuit to Common Duration		Indefinite			•			•			•		
POWER SUPPLY REQUIREMENTS													
Voltage, $+V_{CC}$	+11.4	+15	+16.5	•	•	•	•	•	•	•	•	•	VDC
$-V_{CC}$	−11.4	−15	−16.5	•	•	•	•	•	•	•	•	•	VDC
V_{DD}	+4.5	+5	+5.5	•	•	•	•	•	•	•	•	•	VDC
Current (no load), $+V_{CC}$		+16	+25		•	•	•	•	•	•	•	•	mA
$-V_{CC}$		−23	−35		•	•	•	•	•	•	•	•	mA
V_{DD}		+8	+15		•	•	•	•	•	•	•	•	mA
Potential at DCOM with Respect to ACOM[9]			±0.5			•			•			•	V
Power Dissipation		625	800		•	•		•	•		•	•	mW
TEMPERATURE RANGE													
Specification: J, K	0		+70	•		•							°C
A, B	−25		+85	•		•							°C
R, S							−55		+125	•		•	°C
Storage: J, K	−60		+100	•		•							°C
A, B, R, S	−65		+150	•		•	•		•	•		•	°C

*Same as specification to immediate left.

NOTES: (1) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (2) Refer to Logic Input Compatibility section. (3) Adjustable to zero with external trim potentiometer. (4) Error at input code 000_{16} for both unipolar and bipolar ranges. (5) FSR means Full Scale Range and is 20V for the ±10V range. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) At the major carry, $7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$. (8) Minimum supply voltage required for ±10V output swing is ±13.5V. Output swing for ±11.4V supplies is at least −8V to +8V. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

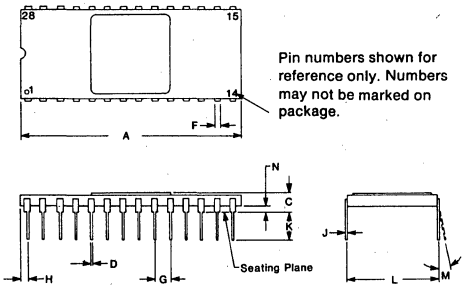
TIMING DIAGRAMS





MECHANICAL

H PACKAGE

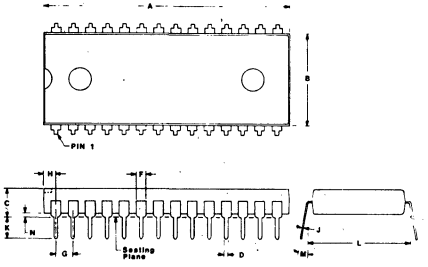


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.386	1.414	35.20	35.92
C	.106	.166	2.74	4.22
D	.016	.021	0.38	0.53
F	.036	.060	0.91	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	- -	10°	- -	10°
N	.025	.060	0.64	1.52

NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

CASE: Ceramic, hermetic
MATING CONNECTOR: 2803MC
WEIGHT: 4.8gm (0.17oz)

P PACKAGE



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.400	1.460	35.56	37.08
B	.530	.575	13.46	13.97
C	.180	.224	4.33	5.70
D	.016	.023	0.38	0.58
F	.043	.065	1.09	1.65
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.136	2.54	3.46
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

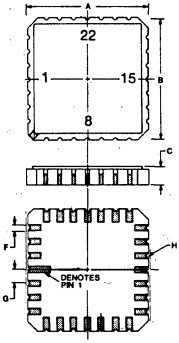
CASE: Ceramic, hermetic
MATING CONNECTOR: 2803MC
WEIGHT: 4.3gm (0.15oz)

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$	0 to +18V
$-V_{CC}$ to ACOM	0 to −18V
V_{DD} to DCOM	0 to +7V
V_{DD} to ACOM	±7V
ACOM to DCOM	±7V
Digital Inputs (pins 2-14, 16-19) to DCOM	−0.4V to +18V
External Voltage Applied to 10V Range Resistor	±12V
REF OUT	Indefinite short to ACOM
External Voltage Applied to DAC Output	−5V to +5V
Power Dissipation	1000mW
Operating Temperature:	
AH, BH	−25°C to +85°C
RH, SH	−55°C to +125°C
Storage Temperature	−65°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.
Metal lids of H and L packages are connected to $-V_{CC}$.

L PACKAGE



CASE: Ceramic

CAP: Kovar, gold plated

TERMINALS: Material and composition conform to Method 2003 (solderability) of MIL-STD-883 (except Paragraph 3.2, steam aging).

WEIGHT: 0.76gm (0.026oz)

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.442	.458	11.23	11.63
B	.442	.458	11.23	11.63
C	.064	.100	1.63	2.54
F	.022	.028	0.56	0.71
G	.050 BASIC		1.27 BASIC	
H	.008R TYP.		0.20R TYP.	

PIN NOMENCLATURE

PIN	NAME	FUNCTION
1	V_{DD}	Logic Supply, +5V
2	$\overline{WR}$	WRITE, command signal to load latches. Logic low loads latches.
3	$\overline{LDAC}$	LOAD D/A CONVERTER, enables $\overline{WR}$ to load the D/A latch. Logic low enables.
4	$\overline{N_A}$	NYBBLE A, enables $\overline{WR}$ to load input latch A (the most significant nybble. Logic low enables.
5	$\overline{N_B}$	NYBBLE B, enables $\overline{WR}$ to load input latch B. Logic low enables.
6	$\overline{N_C}$	NYBBLE C, enables $\overline{WR}$ to load input latch C (the least significant nybble). Logic low enables.
7	D_{11}	DATA, Bit 12, MSB, positive true.
8	D_{10}	DATA, Bit 11
9	D_9	DATA, Bit 10
10	D_8	DATA, Bit 9
11	D_7	DATA, Bit 8
12	D_6	DATA, Bit 7
13	D_5	DATA, Bit 6
14	D_4	DATA, Bit 5
15	DCOM	DIGITAL COMMON, V_{DD} supply return
16	D_0	DATA, Bit 1, LSB
17	D_1	DATA, Bit 2
18	D_2	DATA, Bit 3
19	D_3	DATA, Bit 4
20	$+V_{CC}$	Analog Supply Input, +15V or +12V
21	$-V_{CC}$	Analog Supply Input, −15V or −12V
22	GAIN ADJ	To externally adjust gain
23	ACOM	ANALOG COMMON, $\pm V_{CC}$ supply return
24	V_{out}	D/A converter voltage output
25	10V RANGE	Connect to pin 24 for 10V Range
26	SJ	SUMMING JUNCTION of output amplifier
27	BPO	BIPOLAR OFFSET. Connect to pin 26 for Bipolar Operation
28	REF OUT	6.3V reference output

ORDERING INFORMATION

Model	Package	Temperature Range (°C)	Linearity Error, max (+25°C)	Gain Drift, (ppm/°C)
DAC811JP	Plastic	0/+70	±1/2LSB	30
DAC811KP	Plastic	0/+70	±1/4LSB	20
DAC811AH	Ceramic	−25/+85	±1/2LSB	30
DAC811AH/QM	Ceramic	−25/+85	±1/2LSB	30
DAC811AL	LCC	−25/+85	±1/2LSB	30
DAC811AL/QM	LCC	−25/+85	±1/2LSB	30
DAC811BH	Ceramic	−25/+85	±1/4LSB	20
DAC811BH/QM	Ceramic	−25/+85	±1/4LSB	20
DAC811BL	LCC	−25/+85	±1/4LSB	20
DAC811BL/QM	LCC	−25/+85	±1/4LSB	20
DAC811RH	Ceramic	−55/+125	±1/2LSB	30
DAC811RH/QM	Ceramic	−55/+125	±1/2LSB	30
DAC811RL	LCC	−55/+125	±1/2LSB	30
DAC811RL/QM	LCC	−55/+125	±1/2LSB	30
DAC811SH	Ceramic	−55/+125	±1/4LSB	20
DAC811SH/QM	Ceramic	−55/+125	±1/4LSB	20
DAC811SL	LCC	−55/+125	±1/4LSB	20
DAC811SL/QM	LCC	−55/+125	±1/4LSB	20

DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC811 accepts positive true binary input codes. DAC811 may be connected by the user for any one of the following codes: USB (unipolar straight binary), BOB (bipolar offset binary) or, using an external inverter on the MSB line, BTC (binary two's complement). See Table I.

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB ↓ LSB ↓	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
111111111111	+Full Scale	+Full Scale	−1 LSB
100000000000	+1/2 Full Scale	Zero	−Full Scale
011111111111	1/2 Full Scale −1 LSB	−1 LSB	+Full Scale
000000000000	Zero	−Full Scale	Zero

*Invert the MSB of the BOB code with external inverter to obtain BTC code.

LINEARITY ERROR

Linearity Error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all "1's" and all "0's"). The DAC811 linearity error is specified at ±1/4LSB (max) at +25°C for B, K, and S grades and ±1/2LSB (max) for A, J, and R grades.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotoni-

city requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC811 are monotonic over their specification temperature range.

DRIFT

Gain drift is a measure of the change in the full scale range output over the specification temperature range. Drift is expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by testing the full scale range value (e.g., +FS minus −FS) at high temperature, +25°C, and low temperature; calculating the error with respect to the +25°C value and dividing by the temperature change.

Unipolar offset drift is a measure of the change in output with all 0's on the input over the specification temperature range. Offset is measured at high temperature, +25°C, and low temperature. The maximum change in offset referred to the +25°C value divided by the temperature change is the offset drift. It is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

Bipolar zero drift is measured at a digital input of 800_{16}, the code that gives zero volts output for bipolar operation.

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to ±0.01% of Full Scale Range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC811 contains an on-chip 6.3V reference. This voltage (pin 28) has a tolerance of ±0.1V. The reference output may be used to drive external loads, sourcing at least 2.0mA. This current should be constant for best performance of the D/A converter.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR output change per percent of change in either the positive, negative, or logic supply voltages about the nominal voltages. Figure 1 shows typical power supply rejection versus power supply ripple frequency.

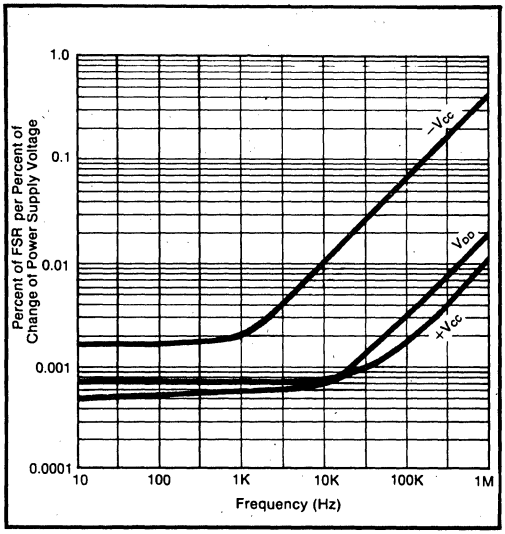


FIGURE 1. Power Supply Rejection versus Power Supply Ripple Frequency.

/QM SCREENING

Burr-Brown /QM models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

SCREENING FLOW FOR DAC811/QM

Screen	MIL-STD-883 Method	Condition
Internal Visual	2010	B
High Temperature Storage (Stabilization Bake)	1008	C (150°C, 24Hr)
Temperature Cycling	1010	C
Burn-in	1015	B
Constant Acceleration	2001	E
Hermeticity: Fine Leak Gross Leak	1014 1014	A1 or A2 C
External Visual	2009	

OPERATION

DAC811 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 2.

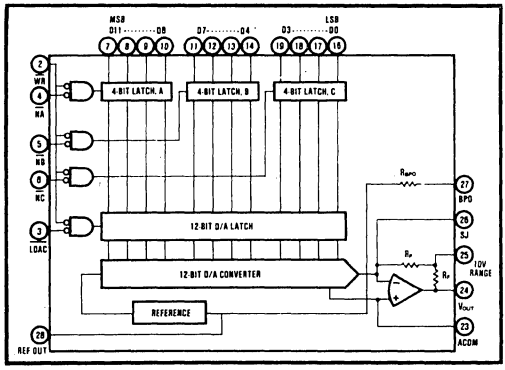


FIGURE 2. DAC811 Block Diagram.

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{WR}$. $\overline{N_A}$, $\overline{N_B}$, and $\overline{N_C}$ are internally NORed with $\overline{WR}$ so that the input latches transmit data when both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ are at logic "0". When either $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) or $\overline{WR}$ go to logic "1", the input data is latched into the input registers and held until both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ go to logic "0".

The D/A latch is controlled by $\overline{LDAC}$ and $\overline{WR}$. $\overline{LDAC}$ and $\overline{WR}$ are internally NORed so that the latches transmit data to the D/A switches when both $\overline{LDAC}$ and $\overline{WR}$ are at logic "0". When either $\overline{LDAC}$ or $\overline{WR}$ are at logic "1", the data is latched in the D/A latch and held until $\overline{LDAC}$ and $\overline{WR}$ go to logic "0".

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for all latches is given in Table II.

TABLE II. DAC811 Interface Logic Truth Table.

$\overline{WR}$	$\overline{N_A}$	$\overline{N_B}$	$\overline{N_C}$	$\overline{LDAC}$	OPERATION
1	X	X	X	X	No Operation
0	0	1	1	1	Enables Input Latch 4MSB's
0	1	0	1	1	Enables Input Latch 4 Middle Bits
0	1	1	0	1	Enables Input Latch 4 LSB's
0	1	1	1	0	Loads D/A Latch From Input Latches
0	0	0	0	0	All Latches Transparent

"X" = Don't Care.

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the Offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table III for corresponding codes.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

±12V OPERATION

The DAC811 is fully specified for operation on ±12V power supplies. However, in order for the output to swing to ±10V, the power supplies must be ±13.5V or greater. When operating with ±12V supplies, the output

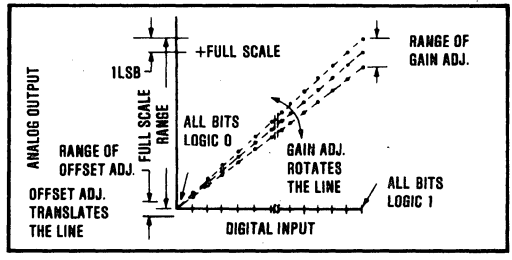


FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter

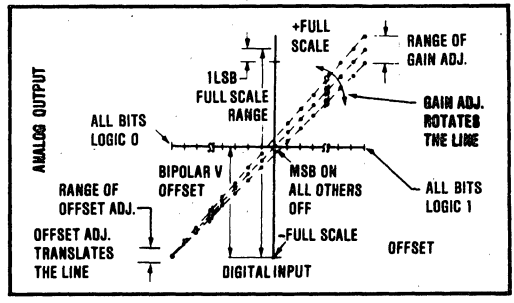


FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

TABLE III. Digital Input/Analog Output, $\pm V_{CC} = \pm 15V$.

	ANALOG OUTPUT VOLTAGE		
DIGITAL INPUT	0 to +10V	±5V	±10V
12-Bit Resolution MSB ↓ LSB ↓			
111111111111	+9.9976V	+4.9976V	+9.9951V
100000000000	+5.0000V	0.0000V	0.0000V
011111111111	+4.9976V	−0.0024V	−0.0049V
000000000000	0.0000V	−5.0000V	−10.0000V
1LSB	2.44mV	2.44mV	4.88mV

swing should be restricted to ±8V in order to meet specifications.

LOGIC INPUT COMPATIBILITY

The DAC811 digital inputs are TTL, LSTTL, and 54/74HC CMOS-compatible over the operating range of V_{DD}. The input switching threshold remains at the TTL threshold over the supply range.

The logic input current over temperature is low enough to permit driving the DAC811 directly from the outputs of 4000B and 54/74C CMOS devices.

INSTALLATION

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram, Figure 5.

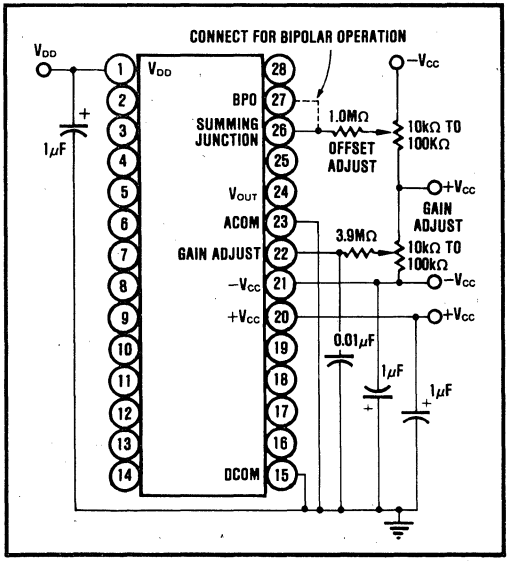


FIGURE 5. Power Supply, Gain, and Offset Potentiometer Connections.

These capacitors (1μF tantalum recommended) should be located close to the DAC811.

The DAC811 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The Analog Common (pin 23) and Digital Common (pin 15) should be connected together at one point. Separate returns minimize current flow in low level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output, therefore, some caution is required in applying these common connections.

The Analog Common is the high quality return for the D/A converter and should be connected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 5. TCR of the potentiometers should be 100 ppm/°C or less. The 1.0MΩ and 3.9MΩ resistors (20% carbon or better) should be located close to the DAC811 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 6, may be substituted in each case. The Gain Adjust (pin 22) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Analog Common to reduce noise pickup in all applications, including those not employing external gain adjustment.

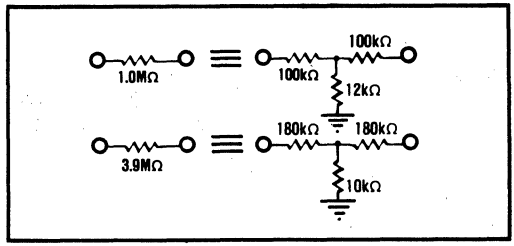


FIGURE 6. Equivalent Resistances.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC811 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 7. Connections for the output ranges are listed in Table IV.

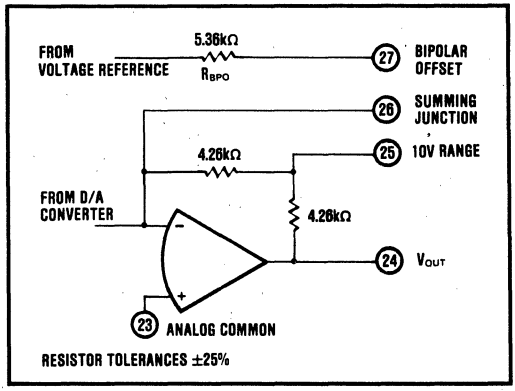


FIGURE 7. Output Amplifier Voltage Range Scaling Circuit.

Table IV. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 25 To	Connect Pin 27 To
0 to +10V	USB	24	23
±5V	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC811 interface logic allows easy interface microcomputer bus structures. The control signal $\overline{WR}$ is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{LDAC}$ determine which of the latches are enabled. It is permissible to enable two or more latches simultaneously as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC811's and later strobed into the D/A latch of all D/A's simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are unused, the base address decoder can be simplified or eliminated altogether. For instance if half the memory space is unused, address line A_{15} of the microcomputer can be used as the chip select control.

4-BIT INTERFACE

An interface to a 4-bit microcomputer is shown in Figure 8. Each DAC811 occupies four address locations. A 74LS139 provides the two to four decoder and selects these with the base address. Memory Write ($\overline{WR}$) of the microcomputer is connected directly to the $\overline{WR}$ pin of the DAC811. A 8205 decoder is an alternative device to use instead of the 74LS139.

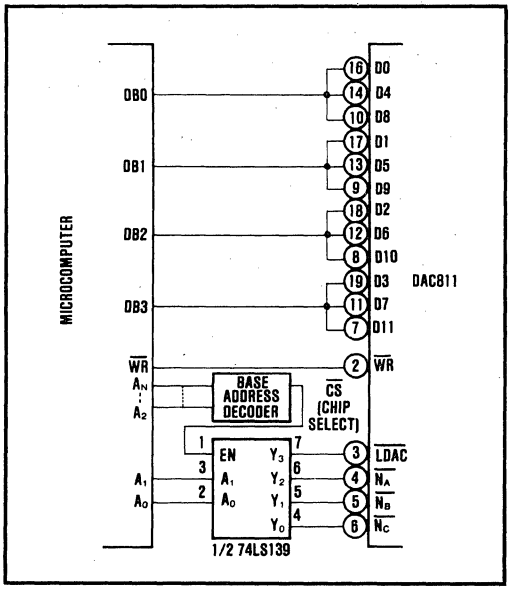


FIGURE 8. Addressing and Control for 4-Bit Microcomputer Interface.

8-BIT INTERFACE

The control logic of DAC811 permits interfacing to right- or left-justified data formats illustrated in Figure 9. When a 12-bit D/A converter is loaded from an 8-bit

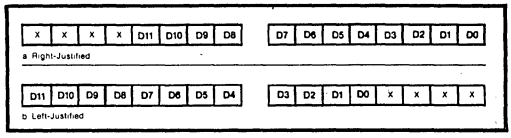


FIGURE 9. 12-Bit Data Formats for 8-Bit Systems.

bus, two bytes of data are required. Figure 10 shows an addressing scheme for right-justified data. The base address is decoded from the high-order address bits. A_0 and A_1 address the appropriate latches. Note that adjacent addresses are used. For the right-justified case $X10_{16}$ loads the 8 LSB's and $X01_{16}$ loads the 4MSB's and simultaneously transfers input latch data to the D/A latch. Addresses $X00_{16}$ and $X11_{16}$ are not used.

Left-justified data is handled in a similar manner. The DAC811 still occupies two adjacent locations in the microcomputer's memory map.

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application the input latch enable lines, $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC 811, is selected by the address decoder and strobed by $\overline{WR}$.

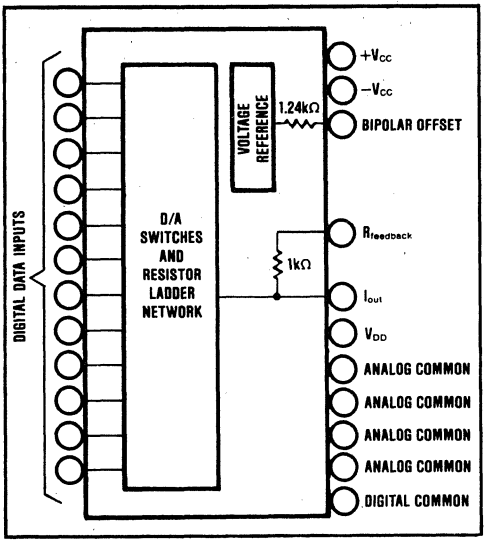
BURR-BROWN®

DAC812

Ultra-High Speed DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT RESOLUTION AND ACCURACY
- 55nsec CURRENT OUTPUT SETTLING TIME
- TTL-COMPATIBLE INPUTS
- MONOTONIC OVER ENTIRE TEMPERATURE RANGE
- LINEARITY ERROR LESS THAN ±1/2LSB OVER TEMPERATURE RANGE (C GRADE)
- HERMETIC METAL PACKAGE



DESCRIPTION

The DAC812 is an ultra-fast-settling 12-bit current-output D/A converter with TTL-compatible inputs packaged in a 24-pin dual-wide dual-in-line hermetic metal package.

The current output settles to ±0.012% of full scale range in 55nsec, typical (65nsec, max., C grade; 80nsec, max., B grade).

The DAC812 utilizes a monolithic 12-bit switch chip with stable, compatible thin-film resistors to achieve fast settling time and excellent stability over temperature and time. An internal applications resistor for use with an external op amp is included to convert the output current into a voltage for 0V to +10V or −5V to +5V ranges.

An output voltage compliance range of +4V to −4V allows the generation of an output voltage without using an external output amplifier.

The DAC812 comes in two drift grades. The linearity error of the C grade is guaranteed to be within ±1/2LSB over the temperature range of −25°C to +85°C. Gain drift of the C grade is ±20ppm/°C (max) and bipolar offset drift is ±10ppm of FSR/°C (max). The B grade has a linearity error of ±1LSB over the temperature range and a maximum gain drift and bipolar offset drift of ±40ppm/°C and ±15ppm/°C, respectively.

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SPECIFICATIONS

ELECTRICAL

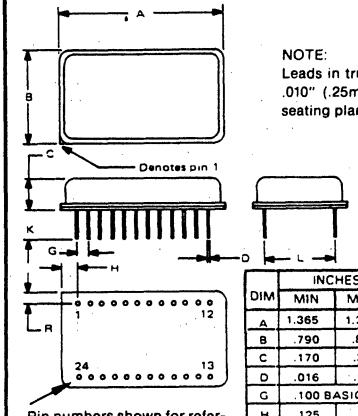
At T_A = +25°C, rated power supplies, and after 5-minute warm-up unless otherwise noted.

MODEL	DAC812CM			DAC812BM			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution; CSB, COB			12			*	Bits
Logic Inputs: V_{IH}	+2.0		+5.25	*		*	V
V_{IL}	0.0		+0.8	*		*	V
I_{IH}, V_I = +2.7V			+20			*	µA
I_{IL}, V_I = +0.4V			−800			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±0.006	±0.012		±0.009	±0.018	% of FSR[1]
Differential Linearity Error			±0.012			±0.018	% of FSR
Gain Error[2]		±0.03	±0.1		*	*	%
Offset Error[2]: Unipolar		±0.02	±0.04		*	*	% of FSR
Bipolar		±0.03	±0.1		*	*	% of FSR
Monotonicity Temp. Range (min)	−25		+85			*	°C
CONVERSION SPEED							
Settling Time to ±1/2LSB into 150Ω							
For FSR Change		55	65		*	80	nsec
For 1LSB Change		25			*		nsec
DRIFT							
Gain		±10	±20		±20	±40	ppm/°C
Offset: Unipolar		±0.25	±0.5		±0.5	±1	ppm of FSR/°C
Bipolar			±10			±15	ppm of FSR/°C
Linearity Error	±0.012 over Temp. Range (max)			±0.025 over Temp. Range (max)			% of FSR
Differential Linearity Error	±0.025 over Temp Range (max)			±0.04 over Temp. Range (max)			% of FSR
OUTPUT							
ANALOG OUTPUT							
Output Current: Unipolar		0 to −10			*		mA
Bipolar		−5 to +5			*		mA
Output Voltage Ranges							
with External Op Amp: Unipolar		0 to +10			*		V
Bipolar		−5 to +5			*		V
Output Impedance: Unipolar		170			*		Ω
Bipolar		150			*		Ω
Output Compliance	−4		+4	*		*	V
POWER SUPPLIES							
Power Supply Sensitivity: $+V_{CC}$			±0.004			*	%FSR/%V_{CC}
$-V_{CC}$			±0.001			*	%FSR/%V_{CC}
V_{DD}			±0.0002			*	%FSR/%V_{DD}
Power Supply Voltages: $+V_{CC}$	+14	+15	+18	*	*	*	V
$-V_{CC}$	−18	−15	−14	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	V
Power Supply Current: $+V_{CC}$		+30	+40		*	*	mA
$-V_{CC}$		−40	−50		*	*	mA
V_{DD}		+25	+40		*	*	mA
Power Dissipation		1.2	1.6		*	*	W
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Storage	−55		+150	*		*	°C
PACKAGE	24-pin Hermetic Metal 0.6" Pin Row Spacing						

*Specification the same as for DAC812CM.

NOTES: (1) FSR is full scale range. (2) Adjustable to zero with external potentiometer.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

PIN ASSIGNMENTS

Pin	Function	Pin	Function
1	Bit 1 (MSB, Data Input)	14	Digital Common (V_{DD} Common)
2	Bit 2	15	Analog Common ($\pm V_{CC}$ Common)
3	Bit 3	16	Analog Common
4	Bit 4	17	Analog Common
5	Bit 5	18	Analog Common
6	Bit 6	19	V_{DD} (Logic Supply)
7	Bit 7	20	I_{OUT} (Current Output)
8	Bit 8	21	R_f (Application Resistor)
9	Bit 9	22	BPO (Bipolar Offset)
10	Bit 10	23	$-V_{CC}$ (Negative Analog Supply)
11	Bit 11	24	$+V_{CC}$ (Positive Analog Supply)
12	Bit 12 (LSB)		
13	No connection		

DISCUSSION OF SPECIFICATIONS

ACCURACY

Linearity of a D/A converter is one of the true measures of its performance. The linearity error of the DAC812 is specified over its entire temperature range. The analog output will not vary by more than ±1/2LSB (±1LSB for the BM model) from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of −25°C to +85°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a −25°C to +85°C range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by 1) testing the end point differences for the DAC812 at t_{min}, +25°C, and t_{max}; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications (includes internal reference).

Offset Drift is a measure of the actual change in output around the minus full-scale point over the specified temperature range. The offset is measured at t_{min}, +25°C, and t_{max}. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of the DAC812 is ±4.0V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages. To insure precision operation, each supply lead should be bypassed to ground as close to the unit as possible with a 1μF CS-type tantalum capacitor.

GROUNDING

Care must be exercised when grounding the DAC812 (pins 14, 15, 16, 17, and 18). In order to preserve the stated linearity and accuracy specifications it is necessary to use the ground pins as the analog ground reference point. Any voltage drop that develops between any of these five pins and the actual ground reference point will degrade the performance of the DAC812. To achieve fast settling performance it is recommended that pins 14 through 18 be returned directly to a ground plane (see Figure 1). The analog ground should be located as close to the DAC812 as possible. Otherwise, the accuracy will be degraded by the voltage drop in the ground lines.

SETTLING TIME

Settling time for the DAC812 is the total time required for the output to settle within an error band around its

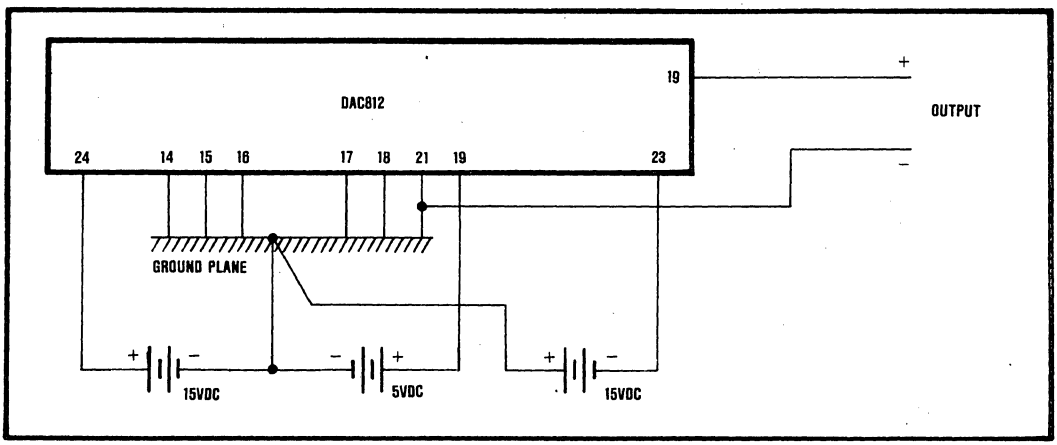


FIGURE 1. DAC812 Grounding Using Feedback Resistor to Generate Output Voltage.

final value after a digital input change. This time includes the digital delay of the internal switches.

Figure 2 shows a typical settling time curve of the DAC812 versus output error. This curve is for full-scale digital code changes. Figures 3 and 4 show typical measured settling time characteristics of the DAC812.

In order to achieve the minimum settling time, it is necessary to observe the following good high frequency construction techniques.

1. The power supplies should be bypassed by 1μF CS-type tantalum capacitors.
2. Use a ground plane to connect common ground points.
3. Remove the ground plane from underneath signal lines where it would add capacitance.
4. Keep analog and digital signal lines physically separated to avoid coupling of the digital signal into the analog paths.

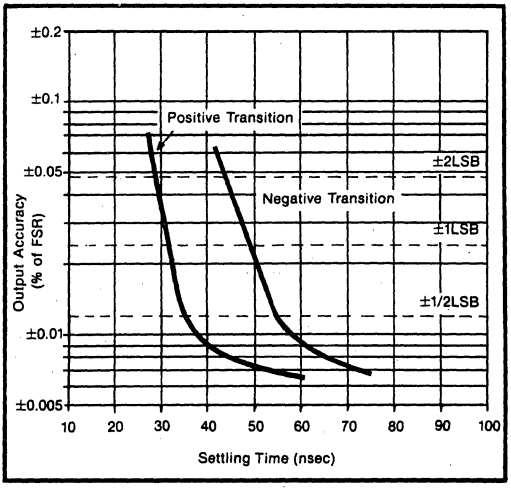


FIGURE 2. DAC812 Typical Settling Time vs. Accuracy

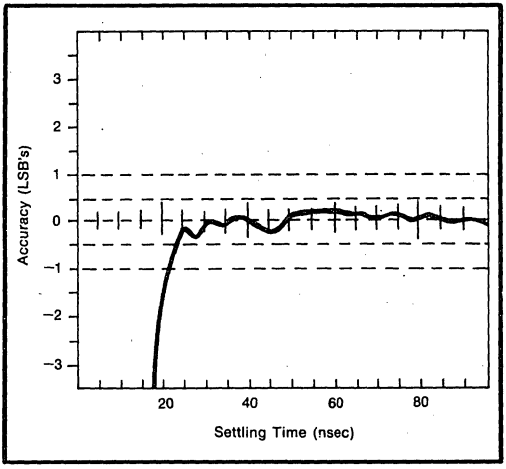


FIGURE 3. Typical DAC812 Negative-to-Positive Full-Scale Output Characteristic.

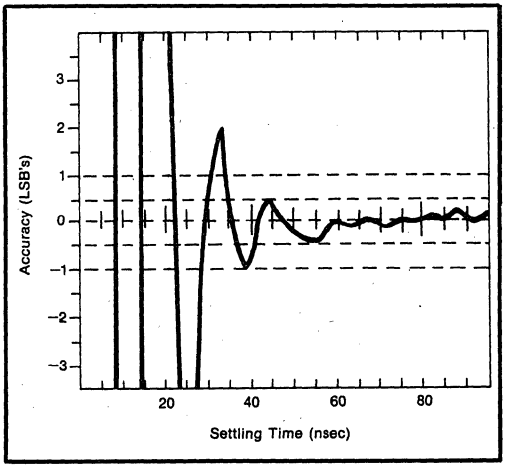


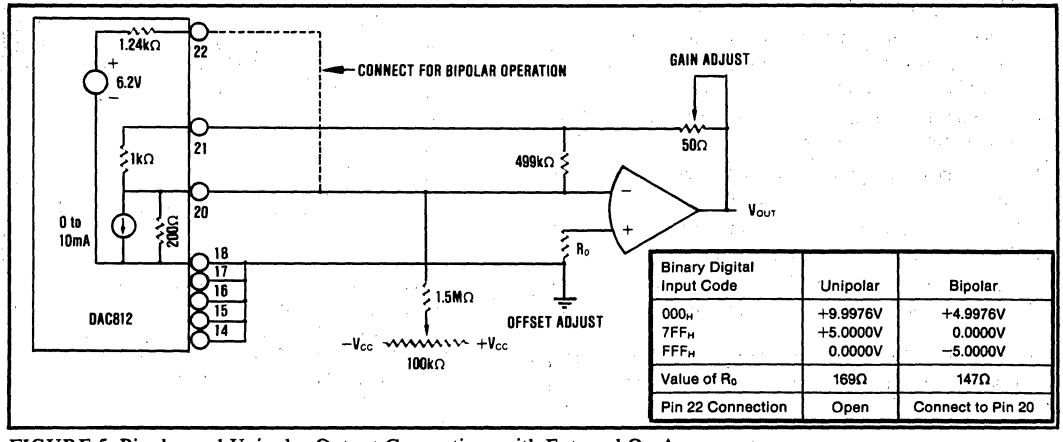
FIGURE 4. Typical Positive-to-Negative Full-Scale Output Characteristic.

5. Bring the source of the digital driving signal as close to the inputs of the DAC812 as possible. If the digital inputs are not clean it will be necessary to reshape them using registers or line drivers. It is recommended that the logic power line be bypassed near the digital logic circuitry as a further measure to achieve clean signals.
6. If possible, the DAC812 should be soldered directly into the printed circuit board since connector lead length will cause ringing in the output.

OUTPUT CONFIGURATIONS AND APPLICATIONS INFORMATION

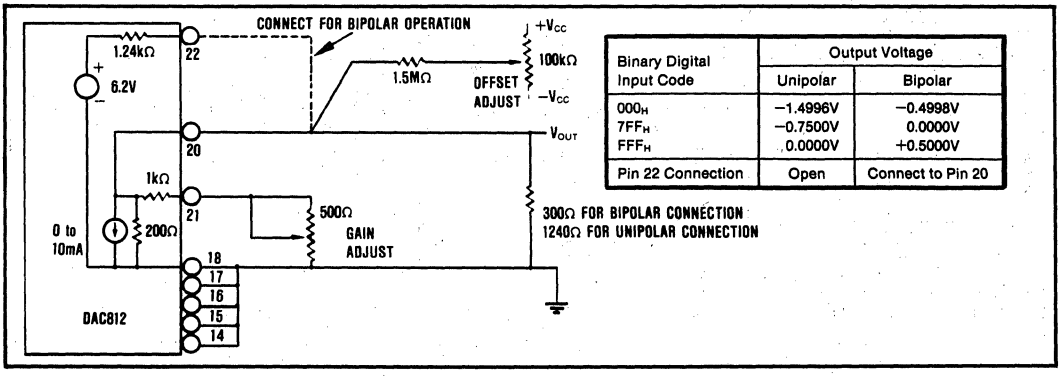
The DAC812 contains a 1.24kΩ resistor for generating the bipolar offset current and a 1kΩ resistor which is primarily used as the feedback resistor when used with an external op amp. This thin-film network is constructed on sapphire to provide excellent temperature tracking capability inherent in thin-film networks. These internal resistors along with other internal resistors cause the DAC812 output, in any mode, to be a ratiometric product of the reference. The feedback resistor has very low power sensitivity so that linearity is maintained independent of digital code changes. Because this resistor is constructed on a sapphire network, it is possible to have both superior tracking and low capacitance. Figure 5 shows the DAC812 connected to an external op amp in unipolar and bipolar modes. When the op amp is a Burr-Brown model OPA600 it is possible to achieve settling times to ±0.1% accuracy in 150nsec. Many of the output accuracy and linearity specifications are given when connected to an external op amp.

For highest speed operation, the DAC812 should be used without an external op amp. Figure 6 shows how to connect the DAC812 for bipolar and unipolar operation. Figure 7 illustrates how to connect the DAC812 to construct a fast A/D converter.



Binary Digital Input Code	Unipolar	Bipolar
000_H	+9.9976V	+4.9976V
$7FF_H$	+5.0000V	0.0000V
FFF_H	0.0000V	−5.0000V
Value of R_0	169Ω	147Ω
Pin 22 Connection	Open	Connect to Pin 20

FIGURE 5. Bipolar and Unipolar Output Connections with External Op Amp.



Binary Digital Input Code	Output Voltage	
	Unipolar	Bipolar
000_H	−1.4996V	−0.4998V
$7FF_H$	−0.7500V	0.0000V
FFF_H	0.0000V	+0.5000V
Pin 22 Connection	Open	Connect to Pin 20

FIGURE 6. Bipolar and Unipolar Output Connection with Resistor Load Only.

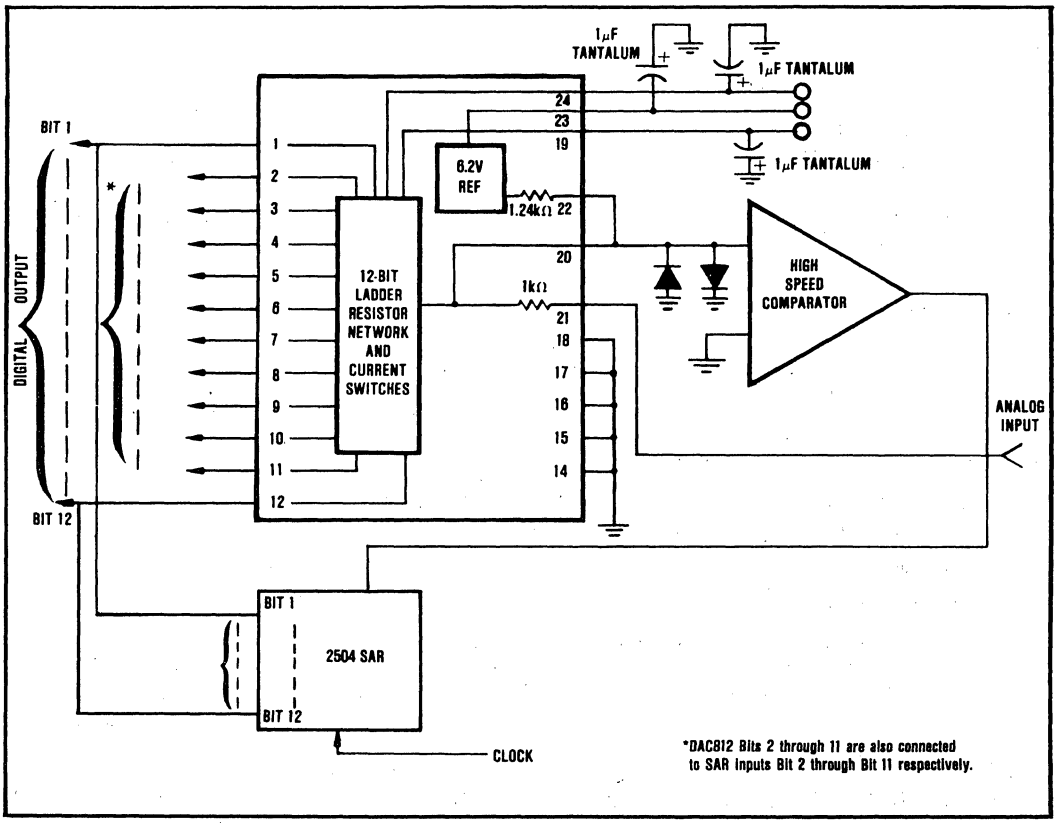


FIGURE 7. DAC812 Used in a Fast A/D Converter.

BURR-BROWN®

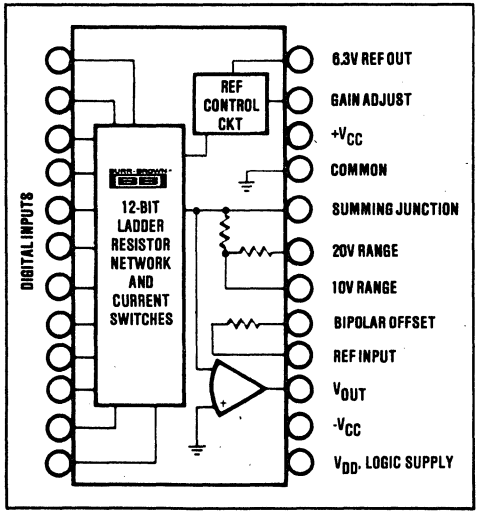
DAC850
DAC851

For a /883B version of this product, see DAC870/883B in the Military Products section.

Integrated Circuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST HIGH RELIABILITY SINGLE-CHIP REPLACEMENT FOR DAC85 AND DAC87
- 12-BIT RESOLUTION
- HIGH ACCURACY: ±1/2LSB max nonlinearity
  −25°C to +85°C (DAC850)
  −55°C to +125°C (DAC851)
- GUARANTEED MONOTONICITY
- HERMETIC PACKAGES
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES

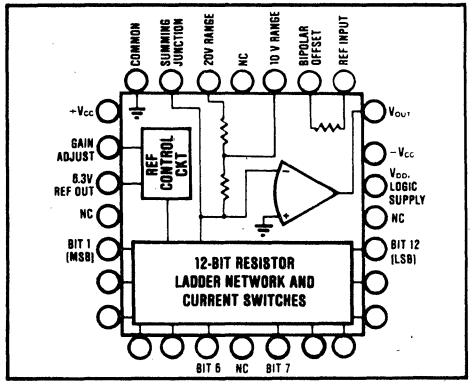


DESCRIPTION

The DAC850 and DAC851 are 12-bit single-chip (current output model) digital-to-analog converters for use in wide temperature high reliability applications.

The DAC850 and DAC851 are packaged in two hermetically-sealed packages. The DAC850 is specified with a linearity error of ±1/2LSB over −25°C to +85°C and the DAC851 has a linearity error of ±3/4LSB over −55°C to +125°C. Both converters have guaranteed monotonicity over their specification temperature range. The current output configuration of these D/A converters is a single-chip integrated circuit containing a subsurface zener reference diode, high-speed current switches, and laser-trimmed thin-film resistors.

The DAC850 and DAC851 provide output voltage ranges of ±2.5V, ±5V, ±10V, 0 to +5 and 0 to +10V (V models) or output current ranges of ±1.175mA or 0 to -2.35mA (I models).



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SPECIFICATIONS

ELECTRICAL

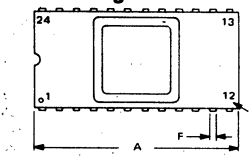
At 25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

MODEL	DAC850-CBI MIN	DAC850-CBI TYP	DAC850-CBI MAX	DAC851-CBI MIN	DAC851-CBI TYP	DAC851-CBI MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution			12			12	Bits
Logic Levels (LSTTL Compatible)[1]							
Logic "1" (at +20μA)	+2		+5.5	+2		+5.5	VDC
Logic "0" (at 0.36mA)	0		+0.8	0		+0.8	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±1/4	±1/2		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	+1, −3/4		±1/2	+1, −3/4	LSB
Gain Error[2]		±0.1	±0.2		±0.1	±0.2	%
Offset Error[2]		±0.05	±0.15		±0.05	±0.15	% of FSR[3]
Power Supply Sensitivity							
+15V and +5V Supplies		±0.0001	±0.001		±0.0001	±0.001	% of FSR/%V_{CC}
−15V Supply		±0.003	±0.006		±0.003	±0.006	% of FSR/%V_{CC}
DRIFT[4] (over spec. temp range)							
Bipolar Drift							
(± full scale drift for the bipolar connection)		±5	±17		±15	±30	ppm of FSR/°C
Total Error[5]: Unipolar		±0.1	±0.20		±0.15	±0.30	% of FSR
Bipolar		±0.06	±0.12		±0.15	±0.30	% of FSR
Gain		±10	±20		±10	±25	ppm/°C
Offset: Unipolar		±1	±3		±1	±3	ppm of FSR/°C
Bipolar		±5	±10		±5	±15	ppm of FSR/°C
Differential Linearity (over spec. temp range)		±1/2	±1		±1/2	±1	LSB
Linearity Error (over spec. temp. range)			±1/2			±1/2	LSB
Monotonicity Temp. Range, min	−25		+85	−55		+125	°C
CONVERSION SPEED							
V Model (settling time to ±0.01% of FSR)							
For FSR Change: 20V Range, 2kΩ Load		3	5		3	5	μsec
10V Range, 2kΩ Load		2.5	4		2.5	4	μsec
For 1LSB Change, Major Carry, 2kΩ Load		1.5			1.5		μsec
Slew Rate, 2kΩ Load	10	15		10	15		V/μsec
I Model (settling time to ±0.01% of FSR)							
For FSR Change: 10Ω to 100Ω Load		300			300		nsec
1kΩ Load		1			1		μsec
OUTPUT							
ANALOG OUTPUT							
V Model							
Ranges ($\pm V_{CC}$ = 15V)	±2.5, ±5, ±10, 0 to +5, 0 to +10			±2.5, ±5, ±10, 0 to +5, 0 to +10			V
Output Current[6]	±5			±5			mA
Output Impedance (DC)		0.05			0.05		Ω
Short Circuit to Common, Duration		Indefinite			Indefinite		
I Model							
Ranges	±0.88, 0 to −1.76	±1.175, 0 to −2.35	±1.47, 0 to −2.94	±0.88, 0 to −1.76	±1.175, 0 to −2.35	±1.47, 0 to −2.94	mA
Output Impedance: Bipolar	2.5	3.1	3.7	2.5	3.1	3.7	kΩ
Unipolar	5.8	7.2	8.6	5.8	7.2	8.6	kΩ
Compliance	−2.5		+2.5	−2.5		+2.5	V
POWER SUPPLIES AND REFERENCE							
Reference Voltage Output	+6.23	+6.3	+6.37	+6.23	+6.3	+6.37	V
Current (for external loads), Source	1.5	2.5		1.5	2.5		mA
Temperature Coefficient of Drift		±10	±20		±10	±25	ppm/°C
Power Supply Requirements: $\pm V_{CC}$	±11.4	±15	±16.5	±11.4	±15	±16.5	VDC
V_{DD}[7]	+4.5	+5	+16.5	+4.5	+5	+16.5	VDC
Power Supply Drain: $\pm V_{CC}$ (no load)		+8, −20	+12, −25		+8, −20	+12, −25	mA
V_{DD} (logic supply)		+7	+10		+7	+10	mA
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	°C
PACKAGE	24-pin hermetic DIP side-brazed ceramic, 28-terminal hermetic leadless chip carrier						

NOTES: (1) Adding external CMOS hex buffers CD 4094A/4050A will provide CMOS input compatibility. Refer to Logic Input Compatibility section. (2) Adjustable to zero with external trim potentiometer. (3) FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc. (4) To maintain drift spec, internal feedback resistors must be used for current output models. (5) Includes the effects of gain, offset and linearity drift. Gain and offset errors are adjusted to zero at +25°C. (6) For operation of −V models with supply voltages of less than ±13VDC, load current must be limited to ±1mA max, at V_{OUT} = ±10V. (7) Power dissipation is an additional 100mW, max, when V_{DD} is operated at +15V.

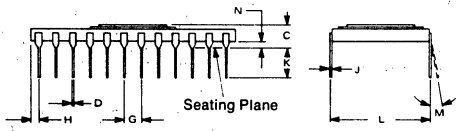
MECHANICAL

DIP Package



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

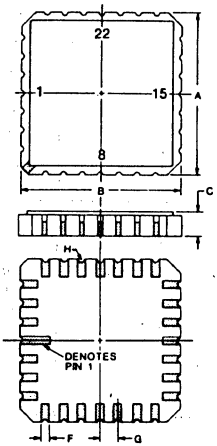


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE:
Metal Cap connected to -Vcc internally.

CASE: Ceramic
MATING CONNECTOR: 0245MC
WEIGHT: 8.4 grams (0.3oz.)

L Package



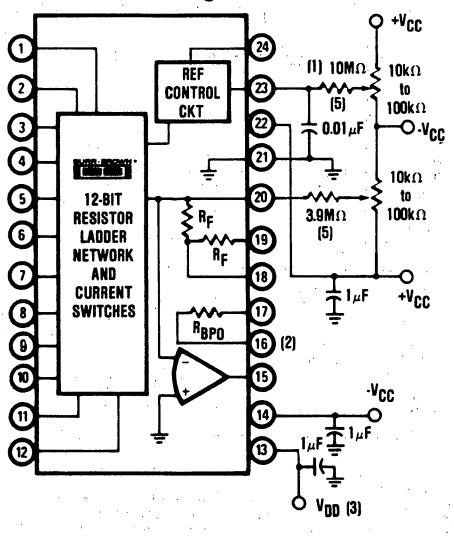
Pin numbers are for reference only. Numbers may not be marked on package.

CASE: Ceramic
CAP: Kovar, gold plated
MATING CONNECTOR: 2802MC (adapts LCC package to 24-pin DIP DAC850/851 pinout.)
WEIGHT: 0.76 grams (0.026 oz.)
CONTACTS: Material and composition conform to Method 2003 (solderability) of MIL-STD-883 (except Paragraph 3.2, steam aging).

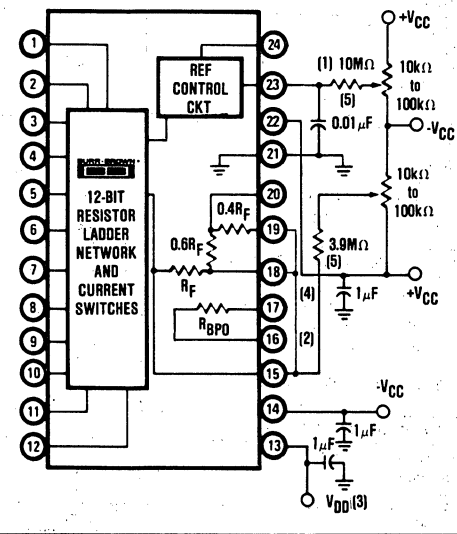
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.442	.458	11.23	11.63
B	.442	.458	11.23	11.63
C	.064	.100	1.63	2.54
F	.022	.028	0.56	0.71
G	.050 BASIC		1.27 BASIC	
H	.008R TYP.		0.20R TYP.	

CONNECTION DIAGRAMS

Voltage Model



Current Model



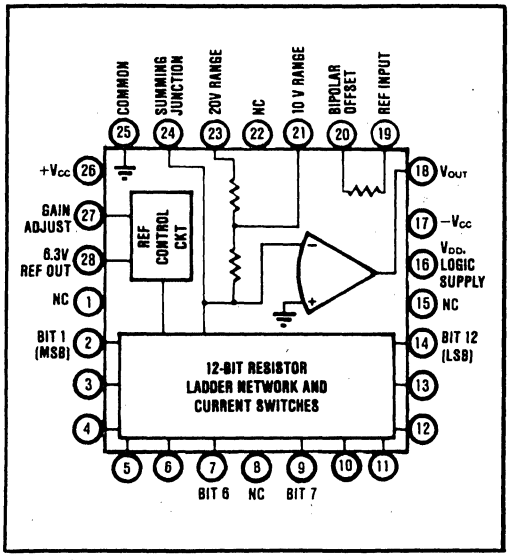
NOTES:

1. DAC850/851 use a 10MΩ resistor. These models can replace the DAC85 which uses an 18MΩ resistor and the DAC87 which uses a 33MΩ resistor.
2. Pin 16 of DAC850/851 is used only to connect the bipolar offset resistor. An external reference voltage may not be used with DAC850/851.
3. If connected to $+V_{CC}$, which is permissible, power dissipation increases 75mW typ., 100mW max.
4. For fastest settling time connect pins 19, 18, and 15 together.
5. Values shown are for ±15V supplies. For supplies below ±13.5V use 2.7MΩ in place of 3.9MΩ and 7.5MΩ in place of 10MΩ.

PIN ASSIGNMENTS (DIP PACKAGE)

I Models	Pin	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)
Logic Supply, V_{DD}	13	Logic Supply, V_{DD}
$-V_{CC}$	14	$-V_{CC}$
I_{OUT}	15	V_{OUT}
Reference Input	16	Reference Input
Bipolar Offset	17	Bipolar Offset
Scaling Network	18	10V Range
Scaling Network	19	20V Range
Scaling Network	20	Summing Junction
Common	21	Common
$+V_{CC}$	22	$+V_{CC}$
Gain Adjust	23	Gain Adjust
6.3V Reference Out	24	6.3V Reference Out

CONTACT ASSIGNMENTS



DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC850 and DAC851 accept complementary binary digital input codes. They may be connected by the user for any one of three complementary codes; CSB, CTC, or COB (see Table I).

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error is specified over its entire temperature range. This means that the analog

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
000000000000	+Full Scale	+Full Scale	-LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	Midscale -1LSB	-1LSB	+Full Scale
111111111111	Zero	-Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specification temperature range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences at -25°C, +25°C, and +85°C for the DAC850 and at -55°C, +25°C, and +125°C for the DAC851; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This is expressed in ppm/°C.

Offset drift is a measure of the actual change in output with all "1"s on the input over the specification temperature range. The offset is measured at -25°C, +25°C, and +85°C for the DAC850 and at -55°C, +25°C, and +125°C for the DAC851. The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

Current Output Models: Two settling times are specified to ±0.01% of FSR. Each is given for current models

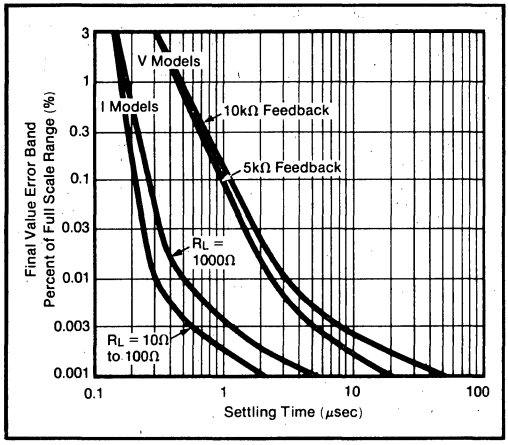


FIGURE 1. Full Scale Range Settling Time vs Final Value Error Band.

connected with two different resistive loads: 10Ω to 100Ω and 1000Ω. Internal resistors are provided for connecting a nominal load resistance of approximately 1000Ω for output voltage ranges of ±1V and 0 to -2V.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is +2.5V to -2.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

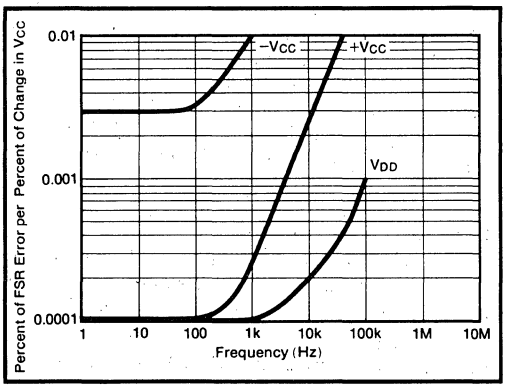


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also. The external current drain is limited to sourcing 2.5mA up to +85°C and 1mA up to +125°C not including current required by the bipolar offset circuit. An external buffer amplifier is recommended if this reference will be used to drive other system components because variations in a load driven from the reference will result in bipolar offset variations of the D/A converter. Gain and bipolar offset adjustments should be made under constant load conditions.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the case. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance. The metal cap on the top of the package is connected internally to $-V_{CC}$.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the case to prevent noise pickup. For operation with supplies of less than ±13.5V, use 2.7MΩ and 7.5MΩ resistors in place of the 3.9MΩ and 10MΩ resistors, respectively. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in each case. Figures 4 and 5 illustrate the relationship of offset and main adjustments to unipolar and bipolar D/A converter output.

Offset Adjustment: For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset poten-

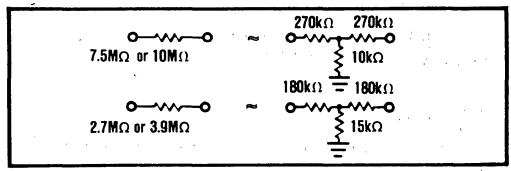


FIGURE 3. Equivalent Resistances.

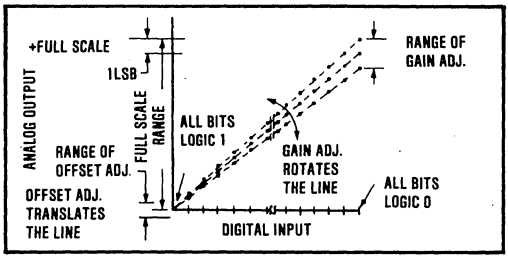


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

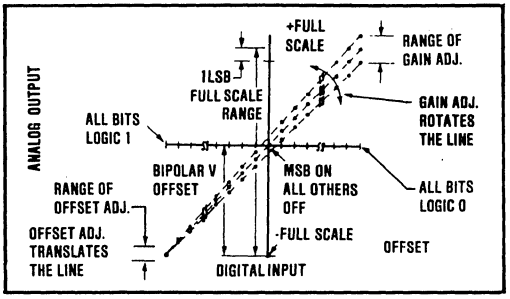


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

tiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagrams for offset adjustment connections.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagrams for gain adjustment connections.

TABLE II. Digital Input/Analog Output.

DIGITAL INPUT	ANALOG OUTPUT			
	VOLTAGE*		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC850 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

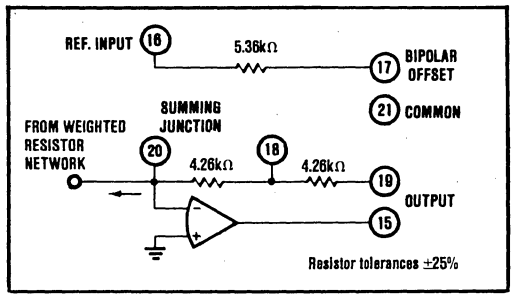


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full scale range change is specified as 3μsec for the 20 volt range and 2.5μsec for the 10 volt range.

TABLE III. Output Voltage Range Connections - Voltage Model.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

CURRENT OUTPUT MODELS

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8. It is important to note that there is a relationship between the tolerances of the current source and the scaling resistors. The magnitude of the tolerance tracks very closely but with opposite sign. The tolerance of the internal resistance of the converter (7.2kΩ unipolar, 3.07kΩ bipolar) tracks the tolerance of the scaling resistors in sign and approximately proportionately in magnitude. That is, if the scaling resistors are high by 10%, the internal impedance is high by about 8%.

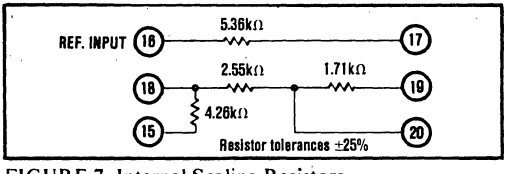


FIGURE 7. Internal Scaling Resistors.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a low drift direct voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

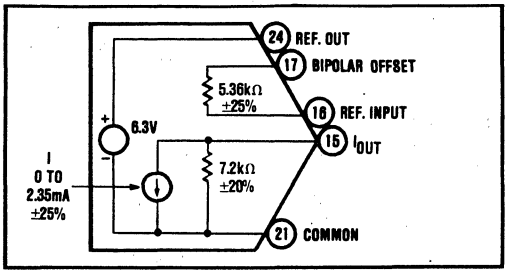


FIGURE 8. Current Output Model Equivalent Output Current.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 9 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2.35mA \left(\frac{R_L \times 7.2k\Omega}{R_L + 7.2k\Omega} \right)$$

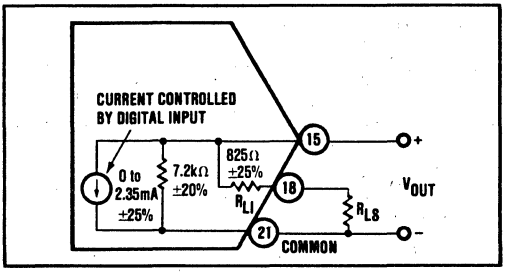


FIGURE 9. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. Tolerances on internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 10, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1.175mA \left(\frac{R_L \times 3.17k\Omega}{R_L + 3.17k\Omega} \right)$$

To achieve specified drift, connect the 1.71kΩ and 2.55kΩ internal scaling resistors in parallel (R_{LI}) and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. The tolerances on the equivalent internal resistors are wide. R_{LS} will have to be selected for each unit.

Driving An External Op Amp

The current output model will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage (see Figure 11).

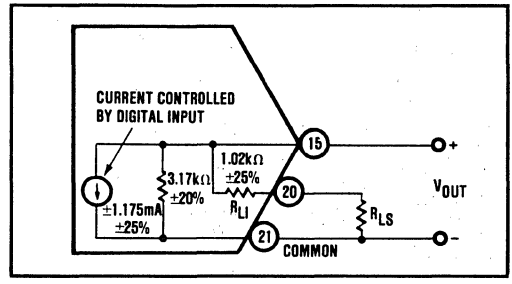


FIGURE 10. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

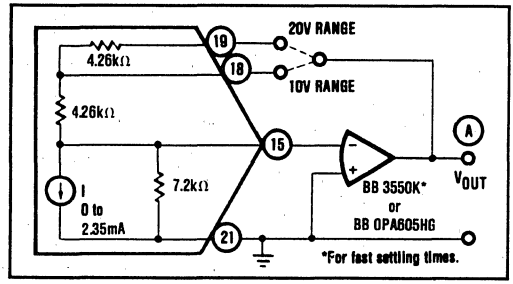


FIGURE 11. External Op Amp - Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model provides output voltage ranges the same as the voltage model. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output D/A Converter.

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

BURR-BROWN®

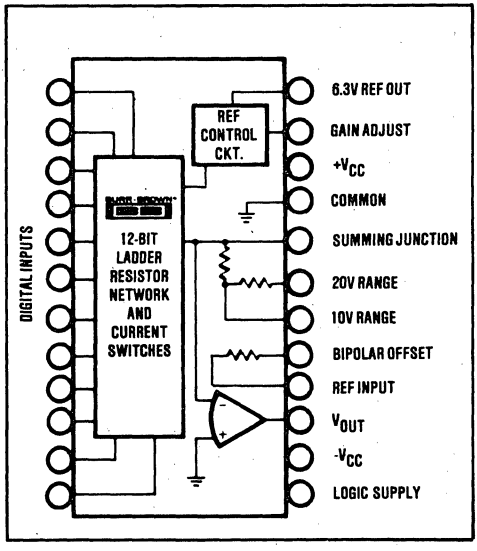
DAC1200KP-V

FOR COMMERCIAL APPLICATIONS

Integrated Circuit 12-Bit Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

- COMPLETE D/A CONVERTER:
  INTERNAL REFERENCE
  ±10V OUTPUT OPERATIONAL AMPLIFIER
- MONOTONICITY GUARANTEED 0°C TO +70°C
- SETTLING TIME 7μsec, MAX
- ±12V to ±15V POWER SUPPLY OPERATION
- 24-PIN MOLDED PLASTIC DIP



DESCRIPTION

The low price of DAC1200KP-V makes this 12-bit resolution D/A converter the best value available for commercial applications.

The DAC1200 offers TTL input compatibility, guaranteed monotonicity over 0°C to +70°C and settling time of 7μsec maximum. It comes complete with internal reference and output operational amplifier.

This precision component is made possible using Burr-Brown's proprietary monolithic integrated circuit process which has been optimized for converter circuits. A stable subsurface reference zener, laser-trimmed thin-film ladder resistors, and high speed current switches combine to give superior performance over the rated temperature range.

DAC1200 is priced and specified for applications where high resolution and monotonocity are the key application parameters and where tightly specified performance over temperature is not required. Because of the low price, it is feasible to use a 12-bit D/A converter for new applications in communications systems, control systems, medical systems, electronic games and personal computer peripherals.

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SPECIFICATIONS

ELECTRICAL

Typical at +25°C and $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise noted.

MODEL	DAC1200KP-V	UNITS
INPUTS		
DIGITAL INPUTS		
Input Code[1]	CSB, COB	
Resolution	12	Bits
Digital Logic Inputs[2]:		
V_{IH}, min to max	+2.4 to $+V_{DD}$	V
V_{IL}, min to max	0 to +0.8	V
I_{IH}, V_I = +2.7V, max	+20	μA
I_{IL}, V_I = +0.4V, max	−400	μA
TRANSFER CHARACTERISTICS		
ACCURACY		
Linearity Error, max[3]	±0.018	% of FSR[4]
Differential Linearity Error, max	±0.024	% of FSR
Gain Error, max[5][6]	±0.3	%
Unipolar Offset Error[5][7]	±20	mV
Bipolar Offset Error, max[5][8]	±40	mV
Monotonicity Over 0°C to +70°C[9]	12	Bits
Sensitivity of Gain to Power Supply Variations:		
$+V_{CC}$ and $-V_{CC}$	±0.003	% of FSR/%V_{CC}
V_{DD}	±0.0002	% of FSR/%V_{DD}
TEMPERATURE COEFFICIENTS		
Gain	±10	ppm/°C
Bipolar Offset	±8	ppm of FSR/°C
SETTLING TIME to ±0.012% of FSR[10]		
20V Step and 2kΩ Load, max	7	μsec
OUTPUT		
ANALOG OUTPUT		
Voltage Range, min	±2.5, ±5, ±10, +5, +10	V
Current, min[11][12]	±5	mA
Impedance	0.05	Ω
REFERENCE OUTPUT		
Voltage[13]	+6.3	V_{DD}
Source Current Available for External Loads, max	+1.5	mA
Temperature Coefficient	±10	ppm/°C
POWER SUPPLY REQUIREMENTS		
RATED VOLTAGE		
$+V_{CC}/-V_{CC}$[14]	+15/−15	V
V_{DD}[15]	+5	V
CURRENT (no load), max[16]		
$+V_{CC}/-V_{CC}$	+12/−25	mA
V_{DD}	+10	mA
TEMPERATURE RANGE		
For parameters specified over temp, min to max	0 to +70	°C
Storage, min to max	−60 to +100	°C

NOTES: (1) CSB = Complementary Straight Binary (unipolar), COB = Complementary Offset Binary (bipolar). (2) Digital inputs are TTL-compatible for V_{DD} over the range of +4.5V to $+V_{CC}$. Digital input specs are guaranteed over 0°C to +70°C. These specs are tested at 25°C only. (3) ±0.018% of FSR is 3/4LSB at 12 bits. (4) FSR means Full Scale Range and is 20V for a ±10V range. (5) Adjustable to zero with external potentiometer. (6) Adjusting the Gain Adjust potentiometer rotates the transfer function about 0V for unipolar operation and about minus full scale (−FS) for bipolar operation. (7) Error at input code FFF_H for unipolar operation (output at 0V). (8) Error at input code FFF_H for bipolar operation (output at minus full scale, −FS). (9) Guaranteed. Tested at 25°C only. (10) Guaranteed. Not tested. (11) For operation with supply voltages of less than ±13V, load current must be limited to 1mA. (12) Output may be indefinitely shorted to Common without damage. (13) Tolerance is ±5%. (14) Range of operation is ±11.4V to ±16.5V. (15) V_{DD} may be operated up to $+V_{CC}$. Digital input logic threshold remains at +1.4V over the V_{DD} range. (16) Typical power supply currents are about 70% of the maximum.

ABSOLUTE MAXIMUM RATINGS

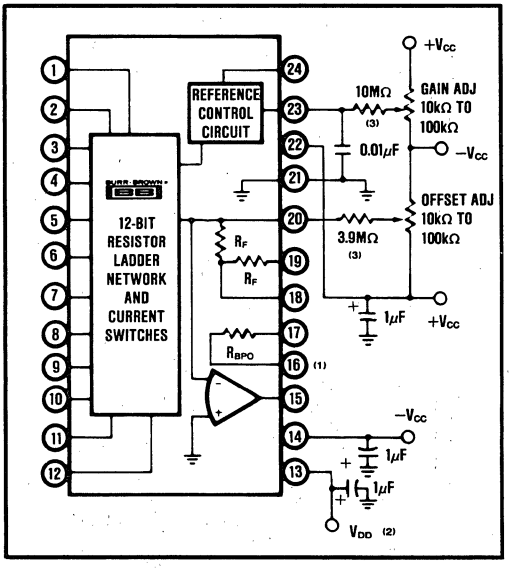
$+V_{CC}$ to Common	0 to +18V
$-V_{CC}$ to Common	0 to −18V
V_{DD} to Common	0 to +7V
Digital Inputs (pins 1—12) to Common	−0.4V to +18V
External Voltage Applied to Range Resistors	±12V
REF OUT	Indefinite short to Common
External Voltage Applied to Analog Output	−5V to +5V
Power Dissipation	1000mW
Operating Temperature	0 to +70°C
Storage Temperature	−60°C to +100°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PIN ASSIGNMENTS

Pin	Description	Pin	Description
1	Bit 1 (MSB)	13	Logic Supply, V_{DD}
2	Bit 2	14	$-V_{CC}$
3	Bit 3	15	V_{OUT}
4	Bit 4	16	Reference Input
5	Bit 5	17	Bipolar Offset
6	Bit 6	18	10V Range
7	Bit 7	19	20V Range
8	Bit 8	20	Summing Junction
9	Bit 9	21	Common
10	Bit 10	22	$+V_{CC}$
11	Bit 11	23	Gain Adjust
12	Bit 12 (LSB)	24	6.3V Reference Out

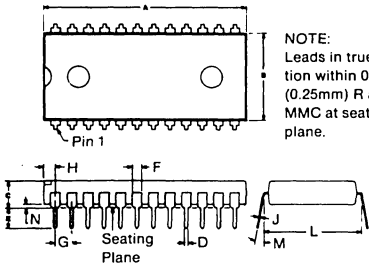
CONNECTION DIAGRAM



	Output Voltage Range Connections				
Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB	19	20	15	24
±5	COB	18	20	NC	24
±2.5V	COB	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

NOTES: (1) Pin 16 is used only to connect the bipolar offset resistor. An external reference voltage may not be used. (2) If connected to $+V_{CC}$, which is permissible, power dissipation increases 75mW typ, 100mW max. (3) Values shown are for ±15V supplies. For supplies below ±13.5V use 2.7MΩ in place of 3.9MΩ and 7.5MΩ in place of 10MΩ.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.233	1.283	31.32	32.59
B	.538	.575	13.67	14.61
C	.169	.224	4.29	5.69
D	.015	.023	0.38	0.58
F	.043	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

CASE: Plastic
MATING CONNECTOR: 0245MC
WEIGHT: 3.7 grams (0.13 oz.)

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF to 10μF tantalum) should be located close to the DAC1200.

±12V OPERATION

The DAC1200 is fully specified for operation on ±12V power supplies. However, to use the ±10V and 0 to +10V ranges of the voltage output models, the power supplies must be ±13V or greater. All other voltage output ranges and all current output ranges provide satisfactory operation with ±11.4V supplies. The supplies should be balanced to obtain optimum performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in the connection diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC1200 to prevent noise pick-up. For operation with supplies of less than ±13.5V, use 2.7MΩ and 7.5MΩ resistors in place of the 3.9MΩ and 10MΩ resistors, respectively. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 1, may be substituted in each case. The Gain Adjust (pin 23) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to reduce noise pick-up. Figures 2 and 3 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

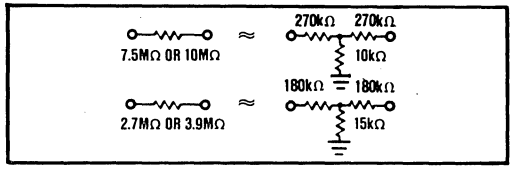


FIGURE 1. Equivalent Resistances.

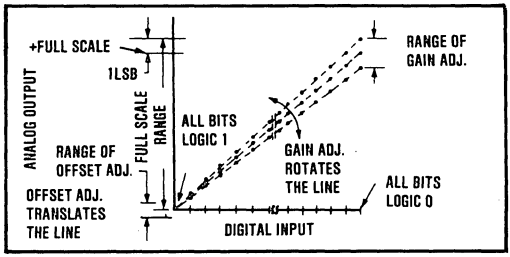


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

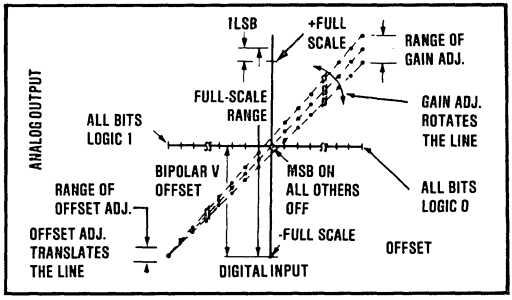


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

Offset Adjustment: For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full-scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table I for corresponding codes. Offset should be adjusted before gain.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the

maximum positive voltage output. Adjust the Gain potentiometer for this positive full-scale voltage. See Table I for positive full-scale voltages.

TABLE I. Digital Input/Analog Output.

Digital Input	Analog Output	
MSB LSB	0 to + 10V	±10V
000000000000	+9.9976V	+9.9951V
011111111111	+5.0000V	0.0000V
100000000000	+4.9976V	−0.0049V
111111111111	0.0000V	−10.0000V
One LSB	2.44mV	4.88mV

To obtain values for other ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V ragne values by 2.
±2.5V range: divide ±10V range values by 4.

BURR-BROWN®

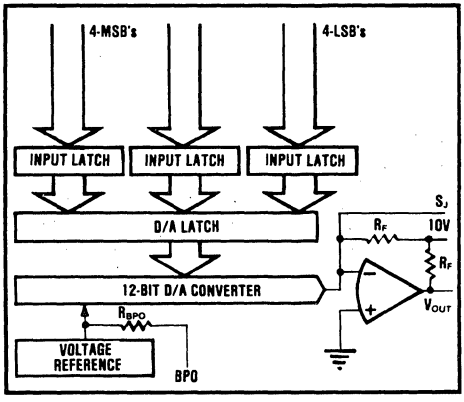
DAC1201KP

FOR COMMERCIAL APPLICATIONS

Monolithic Microprocessor-Compatible 12-Bit Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

- COMPLETE D/A CONVERTER:
  INTERNAL REFERENCE
  ±10V OUTPUT OPERATIONAL AMPLIFIER
- MICROPROCESSOR INTERFACE LOGIC FOR A 4-, 8-, 12- OR 16-BIT BUS
- MONOTONICITY GUARANTEED 0°C TO +70°C
- SETTLING TIME 7μsec, MAX
- ±12V to ±15V POWER SUPPLY OPERATION
- 28-PIN MOLDED PLASTIC DIP



DESCRIPTION

The low price of DAC1201KP makes this 12-bit resolution D/A converter the best value available for commercial applications requiring a microprocessor interface.

The DAC1201 features microprocessor interface logic, TTL input compatibility, guaranteed monotonicity over 0°C to +70°C and settling time of 7μsec maximum.

The interface logic is partitioned in 4-bit nibbles permitting 4-, 8-, 12- and 16-bit bus interface connections for right- or left-justified input words. Dual rank latches permit flexible timing operations for microprocessor control of the DAC1201.

This precision component is made possible using Burr-Brown's proprietary monolithic integrated circuit process which has been optimized for converter circuits. A stable subsurface reference zener, laser-trimmed thin-film ladder resistors, and high speed current switches combine to give superior performance over the rated temperature range.

DAC1201 is priced and specified for applications where high resolution and monotonocity are the key application parameters and where tightly specified performance over temperature is not required. Because of the low price, it is feasible to use this 12-bit D/A converter for new applications in communications systems, electronic controllers, medical instrumentation, electronic games and personal computer peripherals.

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SPECIFICATIONS

ELECTRICAL

Typical at +25°C and $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise noted.

MODEL	DAC1201KP	UNITS
INPUTS		
DIGITAL INPUTS		
Input Code[1]	USB, BOB	
Resolution	12	Bits
Digital Logic Inputs[2]:		
V_{IH}, min to max	+2.4 to $+V_{CC}$	V
V_{IL}, min to max	0 to +0.8	V
I_{IH}, V_I = +2.7V, max	+20	μA
I_{IL}, V_I = +0.4V, max	±30	μA
TRANSFER CHARACTERISTICS		
ACCURACY		
Linearity Error, max[3]	±0.018	% of FSR[4]
Differential Linearity Error, max	±0.024	% of FSR
Gain Error, max[5][6]	±0.3	%
Unipolar Offset Error[5][7]	±20	mV
Bipolar Offset Error, max[5][8]	±40	mV
Monotonicity Over 0°C to +70°C[9]	12	Bits
Sensitivity of Gain to Power Supply Variations:		
$+V_{CC}$ and $-V_{CC}$	±0.002	% of FSR/%V_{CC}
V_{DD}	±0.006	% of FSR/%V_{DD}
TEMPERATURE COEFFICIENTS		
Gain	±10	ppm/°C
Bipolar Zero[10]	±6	ppm of FSR/°C
SETTLING TIME (to ±0.012% of FSR)[11]		
20V step and 2kΩ load, max	7	μsec
OUTPUT		
ANALOG OUTPUT		
Voltage Range, min[12]	±5, ±10, +10	V
Current, min[13]	±5	mA
Impedance	0.2	Ω
REFERENCE OUTPUT		
Voltage[14]	+6.3	V
Source Current Available for External Loads, max	+1.5	mA
Temperature Coefficient	±10	ppm/°C
POWER SUPPLY REQUIREMENTS		
RATED VOLTAGE		
$+V_{CC}/-V_{CC}$[15][16]	+15/−15	V
V_{DD}[17]	+5	V
CURRENT (no load), max[18]		
$+V_{CC}/-V_{CC}$	+25/−35	mA
V_{DD}	+15	mA
TEMPERATURE RANGE		
For parameters specified over temp, min to max	0 to +70	°C
Storage, min to max	−60 to +100	°C

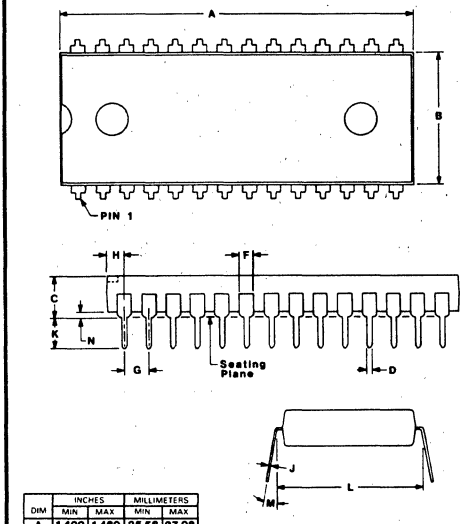
NOTES: (1) USB = Unipolar Straight Binary, BOB = Bipolar Offset Binary. (2) Digital inputs are TTL-compatible for V_{DD} over the range of +4.5V to 5.5V. Digital input specs are guaranteed over 0°C to +70°C. The specs are tested at 25°C only. (3) ±0.018% of FSR is 3/4LSB for 12 bits. (4) FSR means Full-Scale Range and is 20V for a ±10V range. (5) Adjustable to zero with external potentiometer. (6) Adjusting the Gain Adjust potentiometer rotates the transfer function about 0V for unipolar operation and about minus full scale (−FS) for bipolar operation. (7) Error at input code 000_H for unipolar operation (output at 0V). (8) Error at input code 000_H for bipolar operation (output at minus full scale, −FS). (9) Guaranteed. Tested at 25°C only. (10) Drift at 0V output for bipolar operation (input code 100_H). (11) Guaranteed. Not tested. (12) Minimum supply voltage required for ±10V output swing ±13.5V. Output swing for ±11.4V supplies is at least −8V to +8V. (13) Output may be indefinitely shorted to Common without damage. (14) Tolerance is ±5%. (15) The maximum voltage separation between ACOM and DCOM without affecting accuracy is ±0.5V. (16) Range of operation is ±11.4V to ±16.5V. (17) Range of operation is +4.5V to +5.5V. (18) Typical power supply currents are approximately 70% of the maximum.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to ACOM	0 to +18V
$-V_{CC}$ to ACOM	0 to −18V
V_{DD} to DCOM	0 to +7V
V_{DD} to ACOM	±7V
ACOM to DCOM	±7V
Digital Inputs (pins 2-14, 16-19) to DCOM	−0.4V to +18V
External Voltage Applied to 10V Range Resistor	±12V
REF OUT	Indefinite short to ACOM
External Voltage Applied to Analog Output	−5V to +5V
Power Dissipation	1000mW
Operating Temperature	0°C to +70°C
Storage Temperature	−60°C to +100°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

MECHANICAL

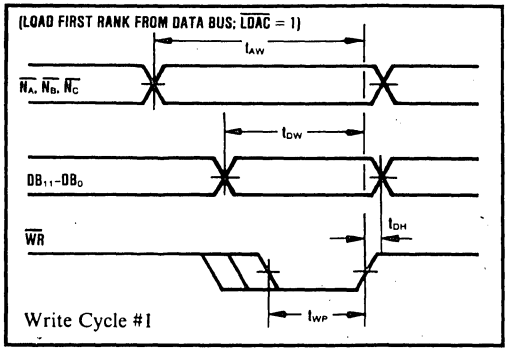


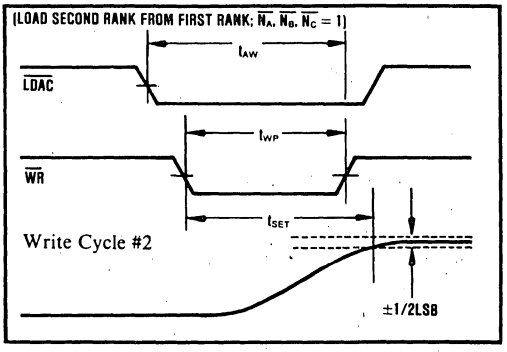
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.400	1.460	35.56	37.08
B	.530	.575	13.46	13.87
C	.160	.224	4.29	5.70
D	.015	.023	0.38	0.58
F	.043	.065	1.09	1.65
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.136	2.54	3.46
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

NOTES:
1. Leads in true position within .010" (.25mm) R at MMC at seating plane.

CASE: Plastic
MATING CONNECTOR: 2803MC
WEIGHT: 4.3gm (0.15oz)

TIMING DIAGRAMS





Digital Interface Timing Over Temperature Range:

t_{WP}, $\overline{WR}$ pulse width, min 50nsec
$t_{AW}1$, $\overline{N_X}$ and $\overline{LDAC}$ valid to end of $\overline{WR}$, min 50nsec
t_{DW}, data valid to end of $\overline{WR}$, min 80nsec
t_{DH}, data valid hold time, min 0nsec

PIN NOMENCLATURE

PIN	NAME	FUNCTION
1	V_{DD}	Logic Supply, +5V
2	$\overline{WR}$	WRITE, command signal to load latches. Logic low loads latches.
3	$\overline{LDAC}$	LOAD D/A CONVERTER, enables $\overline{WR}$ to load the D/A latch. Logic low enables.
4	$\overline{N_A}$	NYBBLE A, enables $\overline{WR}$ to load input latch A (the most significant nybble. Logic low enables.
5	$\overline{N_B}$	NYBBLE B, enables $\overline{WR}$ to load input latch B. Logic low enables.
6	$\overline{N_C}$	NYBBLE C, enables $\overline{WR}$ to load input latch C (the least significant nybble). Logic low enables.
7	D_{11}	DATA, Bit 12, MSB, positive true.
8	D_{10}	DATA, Bit 11
9	D_9	DATA, Bit 10
10	D_8	DATA, Bit 9
11	D_7	DATA, Bit 8
12	D_6	DATA, Bit 7
13	D_5	DATA, Bit 6
14	D_4	DATA, Bit 5
15	DCOM	DIGITAL COMMON, V_{DD} supply return
16	D_0	DATA, Bit 1, LSB
17	D_1	DATA, Bit 2
18	D_2	DATA, Bit 3
19	D_3	DATA, Bit 4
20	$+V_{CC}$	Analog Supply Input, +15V or +12V
21	$-V_{CC}$	Analog Supply Input, −15V or −12V
22	GAIN ADJ	To externally adjust gain
23	ACOM	ANALOG COMMON, $\pm V_{CC}$ supply return
24	V_{out}	D/A converter voltage output
25	10V RANGE	Connect to pin 24 for 10V Range
26	SJ	SUMMING JUNCTION of output amplifier
27	BPO	BIPOLAR OFFSET. Connect to pin 26 for Bipolar Operation
28	REF OUT	6.3V reference output

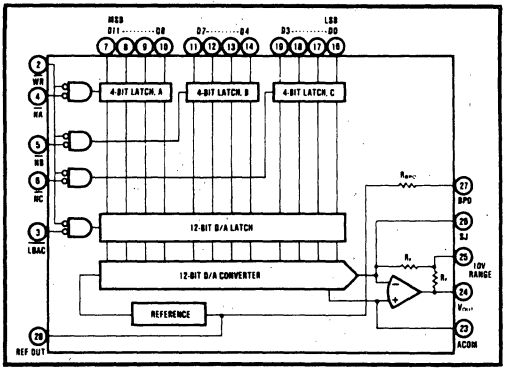


FIGURE 1. DAC1201 Block Diagram.

OPERATION

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{WR}$. $\overline{N_A}$, $\overline{N_B}$, and $\overline{N_C}$ are internally NORed with $\overline{WR}$ so that the input latches transmit data when both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ are at logic "0". When either $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) or $\overline{WR}$ go to logic "1", the input data is latched into the input registers and held until both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ go to logic "0".

The D/A latch is controlled by $\overline{LDAC}$ and $\overline{WR}$. $\overline{LDAC}$ and $\overline{WR}$ are internally NORed so that the latches

transmit data to the D/A switches when both $\overline{LDAC}$ and $\overline{WR}$ are at logic "0". When either $\overline{LDAC}$ or $\overline{WR}$ are at logic "1", the data is latched in the D/A latch and held until $\overline{LDAC}$ and $\overline{WR}$ go to logic "0".

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for all latches is given in Table I.

TABLE I. DAC1201 Interface Logic Truth Table.

WR	N_A	N_B	N_C	LDAC	Operation
1	X	X	X	X	No Operation
0	0	1	1	1	Enables Input Latch 4MSBs
0	1	0	1	1	Enables Input Latch 4 Middle Bits
0	1	1	0	1	Enables Input Latch 4LSBs
0	1	1	1	0	Loads D/A Latch From Input Latches
0	0	0	0	0	All Latches Transparent

"X" = Don't Care.

GAIN AND OFFSET ADJUSTMENTS

Figures 2 and 3 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

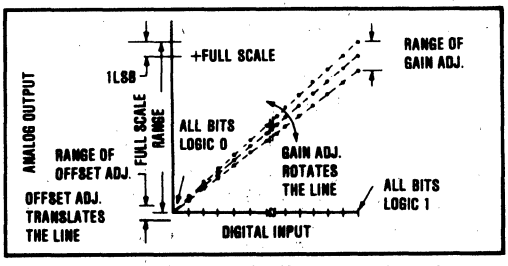


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

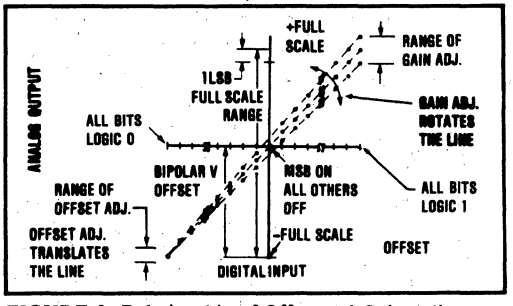


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the Offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table II for corresponding codes.

TABLE II. Digital Input/Analog Output, $\pm V_{CC} = \pm 15V$.

Digital Input	Analog Output		
12-Bit Resolution MSB ↓ LSB ↓	0 to + 10V	±5V	±10V
111111111111	+9.9976V	+4.9976V	+9.9951V
100000000000	+5.0000V	0.0000V	0.0000V
011111111111	+4.9976V	−0.0024V	−0.0049V
000000000000	0.0000V	−5.0000V	−10.0000V
1LSB	2.44mV	2.44mV	4.88mV

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages.

±12V OPERATION

The DAC1201 is fully specified for operation on ±12V power supplies. However, in order for the output to swing to ±10V, the power supplies must be ±13.5V or greater. When operating with ±12V supplies, the output swing should be restricted to ±8V in order to meet specifications.

INSTALLATION

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram, Figure 4.

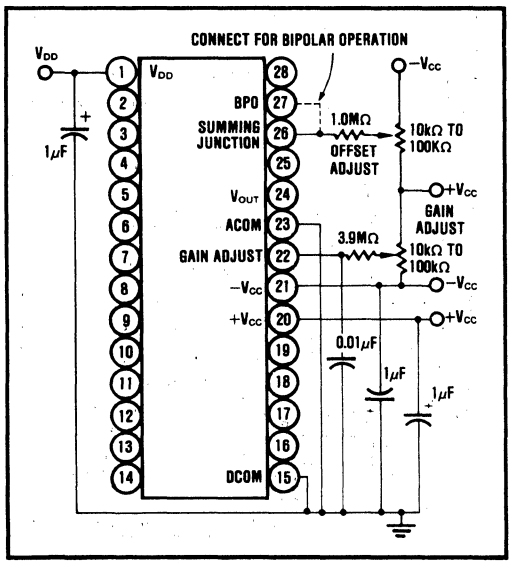


FIGURE 4. Power Supply, Gain, and Offset Potentiometer Connections.

These capacitors (1μF to 10μF tantalum recommended) should be located close to the DAC1201.

The DAC1201 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The Analog Common (pin 23) and Digital Common (pin 15) should be connected together at one point. Separate returns minimize current flow in low level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output; therefore, some caution is required in applying these common conections.

The Analog Common is the high quality return for the D/A converter and should be connected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 4. TCR of the potentiometers should be 100ppm/°C or less. The 1.0MΩ and 3.9MΩ resistors (20% carbon or better) should be located close to the DAC1201 to prevent noise pick-up. If it is not convenient to use these high value resistors, and equivalent "T" network, as shown in Figure 5, may be substituted in each case. The Gain Adjust (pin 22) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Analog Common to reduce noise pick-up in all applications, including those not employing external gain adjustment.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC1201 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 6. Connections for the output ranges are listed in Table III.

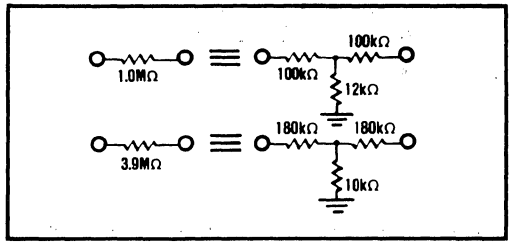


FIGURE 5. Equivalent Resistances.

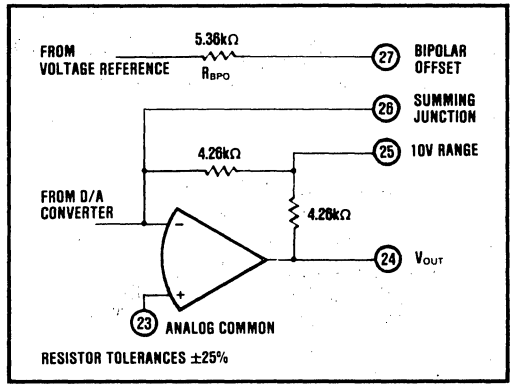


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

TABLE III. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 25 To	Connect Pin 27 To
0 to +10V	USB	24	23
±5V	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

BURR-BROWN®

DAC1600

FOR COMMERCIAL APPLICATIONS

Monolithic 16-Bit Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

- COMPLETE D/A CONVERTER:
  INTERNAL REFERENCE
  ±10V OUTPUT OPERATIONAL AMPLIFIER
- 14-BIT ACCURACY (K GRADE):
  ±0.003% FSR LINEARITY ERROR
  14-BIT MONOTONICITY GUARANTEED 0°C to +70°C
- SETTLING TIME 10μs, MAX
- ±15V POWER SUPPLY OPERATION
- 24-PIN MOLDED PLASTIC DIP

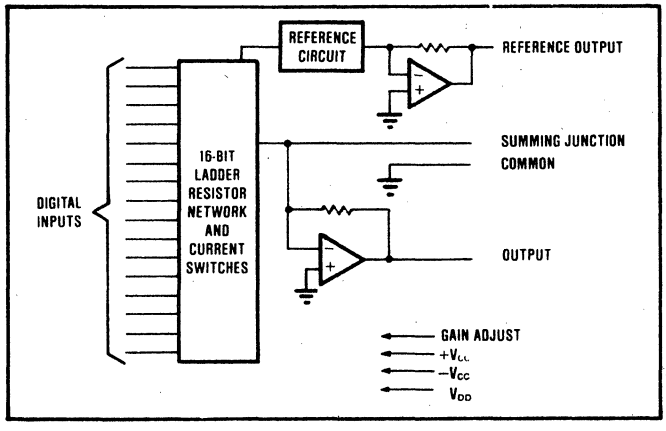
DESCRIPTION

The low prices of DAC1600JP and DAC1600KP make these very-high resolution D/A converters the best value available.

The DAC1600 family offers TTL input compatibility, guaranteed monotonicity (13-bit, J grade; 14-bit, K grade) over 0°C to +70°C and settling time of 10μsec maximum.

This precision component is made possible using Burr-Brown's proprietary monolithic integrated circuit process which has been optimized for converter circuits. A stable subsurface reference zener, laser-trimmed thin-film ladder resistors, and high speed current switches combine to give superior performance over the rated temperature range.

The DAC1600 is priced and specified for applications where high resolution and monotonocity are the key application parameters and where tightly-specified performance over temperature is not required. Because of the low price, it is feasible to use a 16-bit D/A converter for new applications in communications systems, electronic controllers, electronic games, and personal computer peripherals.



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SPECIFICATIONS

ELECTRICAL

Typical at +25°C. $\pm V_{CC}$ = 15V, V_{DD} = +5V unless otherwise noted.

MODEL	DAC1600JP-V	DAC1600KP-V	UNITS
INPUTS			
DIGITAL INPUTS			
Input Code[1]	COB		
Resolution, max	16	*	Bits
Digital Logic Inputs[2]:			
V_{IH}, min to max	+2.4 to $+V_{DD}$	*	V
V_{IL}, min to max	−1.0 to +0.8	*	V
I_{IH}, V_I = +2.7V, max	+40	*	µA
I_{IL}, V_I = +0.4V, max	−0.5	*	mA
TRANSFER CHARACTERISTICS			
ACCURACY			
Linearity Error, max[3]	±0.006	±0.003	% of FSR[4]
Differential Linearity Error, max	±0.012	±0.006	% of FSR
Gain Error, max[5][6]	±0.3	*	%
Bipolar Zero Error, max[5]	40	*	mW
Monotonicity Over 0°C to +70°C[7]	13	14	Bits
Sensitivity of Gain to Power Supply Variations:			
$\pm V_{CC}$	±0.002	*	% of FSR/%V_{CC}
V_{DD}	±0.0002	*	% of FSR/%V_{DD}
TEMPERATURE COEFFICIENTS			
Gain	±10	*	ppm/°C
Bipolar Zero	±5	*	ppm of FSR/°C
SETTLING TIME (to ±0.003% of FSR)[8], 10V step and 2kΩ load, max	10	*	µsec
OUTPUT			
ANALOG OUTPUT			
Voltage Range, min	±10	*	V
Current, min[9]	±5	*	mA
Impedance	0.15	*	Ω
REFERENCE OUTPUT			
Voltage[10]	+6.3	*	V
Source Current Available for External Loads, max	+1.5	*	mA
Temperature Coefficient	±10	*	ppm/°C
POWER SUPPLY REQUIREMENTS			
RATED VOLTAGE			
$\pm V_{CC}$[11]	15	*	V
V_{DD}[12]	+5	*	V
CURRENT, max[13]			
$\pm V_{CC}$	35	*	mA
V_{DD}	8	*	mA
TEMPERATURE RANGE			
For parameters specified over temp, min/max	0 to +70	*	°C
Storage, min/max	−60 to +100	*	°C

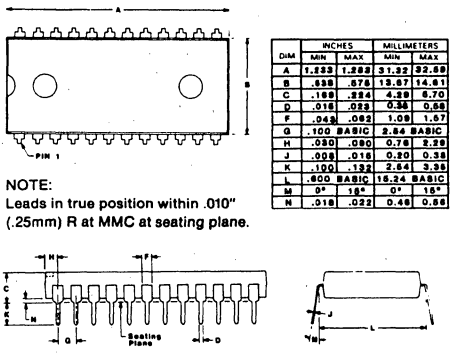
NOTES: (1) COB = Complementary Offset Binary. (2) Digital inputs are TTL-compatible for V_{DD} over the range of +4.5V to $+V_{CC}$. Digital input specs are guaranteed over 0°C to +70°C. These specs are tested at 25°C only. (3) ±0.003% of FSR is 1/2LSB at 14 bits. (4) FSR means Full Scale Range and is 20V for a ±10V range. (5) Adjustable to zero with external potentiometer. (6) Adjusting the gain potentiometer rotates the transfer function around Bipolar Zero, 0V (Input Code $7FFF_H$). (7) Guaranteed. Tested at 25°C only. (8) Guaranteed. Not tested. (9) Output may be indefinitely shorted to Common without damage. (10) Tolerance is ±5%. (11) Range of operation is ±13.5V to ±16.5V. (12) V_{DD} may be operated up to $+V_{CC}$. Digital input logic threshold remains at +1.4V over the V_{DD} range. (13) Typical power supply currents are about 50% of the maximum.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Common	0V, +18V
$-V_{CC}$ to Common	0V, −18V
V_{DD} to Common	0V, +18V
Digital Data Inputs to Common	−1V, +18V
Reference Out to Common	Indefinite Short to Common
External Voltage Applied to D/A Output	−5V to +5V
V_{OUT}	Indefinite Short to Common
Power Dissipation	1000mW
Storage Temperature	−60°C to +100°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

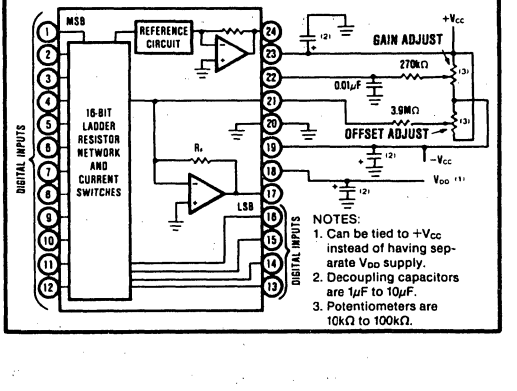
MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.233	1.283	31.32	32.69
B	.535	.575	13.67	14.61
C	.165	.224	4.29	5.70
D	.016	.023	0.36	0.58
F	.045	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.080	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.132	2.54	3.36
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.015	.022	0.46	0.56

NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

CONNECTION DIAGRAM



NOTES:
1. Can be tied to $+V_{CC}$ instead of having separate V_{DD} supply.
2. Decoupling capacitors are 1µF to 10µF.
3. Potentiometers are 10kΩ to 100kΩ.

PIN ASSIGNMENTS

Pin	Description	Pin	Description
1	Bit 1 (MSB)	13	Bit 13
2	Bit 2	14	Bit 14
3	Bit 3	15	Bit 15
4	Bit 4	16	Bit 16 (LSB)
5	Bit 5	17	V_{OUT}
6	Bit 6	18	V_{DD}
7	Bit 7	19	$-V_{CC}$
8	Bit 8	20	Common
9	Bit 9	21	Summing Junction (Zero Adjust)
10	Bit 10	22	Gain Adjust
11	Bit 11	23	$+V_{CC}$
12	Bit 12	24	+6.3V Reference Output

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF to 10μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 1, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust to Common to prevent noise pickup. See Figure 2 for relationship of zero and gain adjustment.

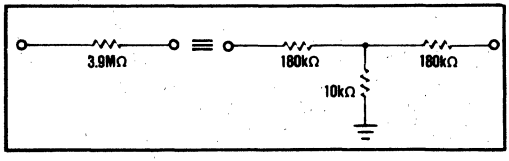


FIGURE 1. Equivalent Resistances.

Zero Adjustment

Apply the digital input code that produces zero output voltage or current. See Table I for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table I for positive full scale voltages and the Connection Diagram for gain adjustment circuit connections.

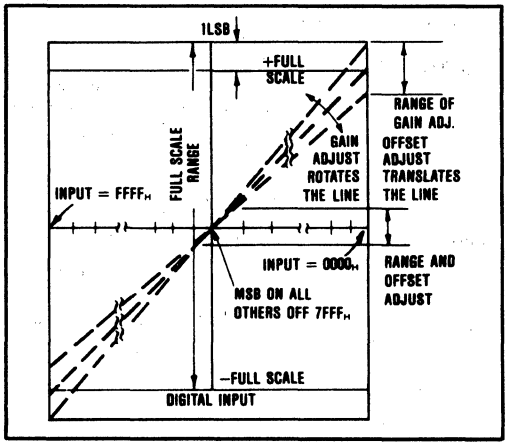


FIGURE 2. Relationship of Zero and Gain Adjustment.

TABLE I. Calibration Table.

Digital Input	Description	Analog Output		
		16-bit	15-bit	15-bit
One LSB	One LSB	305μV	610μV	1224μV
0000$_H$	+ Full Scale	+9.99960V	9.99939V	+9.99878V
7FFF$_H$	Bipolar Zero	0V	0V	0V
FFFF$_H$	– Full Scale	–10.00000V	–10.00000V	–10.00000V

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a 20V full-scale range, 1LSB is 305μV. With a load current of 5mA, series wiring and connector resistances of only 60mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a sytem layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1/2LSB error in the analog output voltage!

In Figure 3 lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed during initial calibration. R_2 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_3 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DACI600 family because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_3 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_3 ($R_3 \times 2mA$) appears as zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figure 3.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

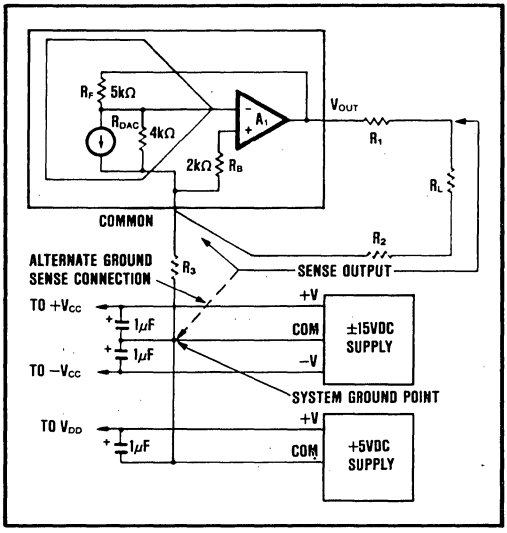


FIGURE 3. Output Circuit.

BURR-BROWN®

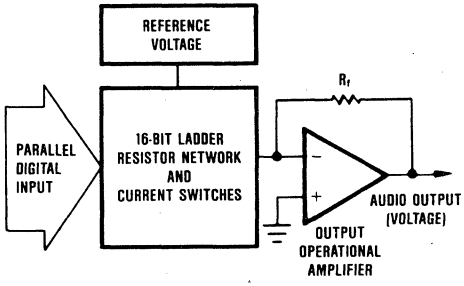
PCM53JG-V
PCM53JG-I

DESIGNED FOR AUDIO

16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 16-BIT MONOTONICITY, typ
- 0.001% OF FSR TYP DIFFERENTIAL LINEARITY ERROR
- 0.002% THD (FS Input, 16 Bits), typ
- 0.02% THD (−20dB, 16 Bits), typ
- 3μsec SETTLING TIME, typ
- 96dB DYNAMIC RANGE
- ±10V AND ±1mA AUDIO OUTPUT AVAILABLE
- EIAJ STC-007 COMPATIBLE
- INDUSTRY-STANDARD PINOUT
- COMPACT, 24-PIN DIP PACKAGE



DESCRIPTION

The PCM53 is a state-of-the-art, fully monolithic, digital-to-analog converter that is designed and specified for digital audio applications. This device employs a segmented architecture and ultra-stable, nichrome (NiCr), thin-film, well-matched resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature range.

The PCM53-V is completely self-contained with stable, low noise, internal, zener voltage reference; high speed current switches; resistor ladder network; and fast-settling, low noise, output operational amplifier all on a single monolithic chip. A special, open-loop reference circuit helps provide the fast settling time required for critical audio applications. The converter can be operated using two power supplies (±15V) instead of three separate supplies. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps to assure the user of high system reliabilty and outstanding overall system performance.

The PCM53JG-I is similar to the PCM53JG-V except it provides a current output that settles to within ±0.006% of FSR of its final value in typically 350nsec in response to a full-scale change in the digital input code.

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C rated power supplies unless otherwise noted.

MODEL	PCM53JG			
	MIN	TYP	MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution		16		Bits
Dynamic Range		96		dB
Logic Levels (TTL/CMOS Compatible): Logic "1" at +40µA	+2.4		$+V_{CC}$	VDC
Logic "0" at −0.5mA	0		+0.8	VDC
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error		±0.1	±1.0	%
Bipolar Zero Error[1]		±10	±50	mV
Differential Linearity Error at Bipolar Zero		0.001	0.005	% of FSR[2]
Noise (rms)(20Hz to 20kHz) at Bipolar Zero: PCM53-V[3]		30	60	µV
TOTAL HARMONIC DISTORTION[4] (16-Bit Resolution)				
V_O = ±FS at f = 420Hz		0.002	0.004	%
V_O = −20dB at f = 420Hz		0.02	0.04	%
V_O = −60dB at f = 420Hz		1.9	4.0	%
MONOTONICITY		16		Bits
DRIFT (0°C to +70°C)				
Total Bipolar Drift (includes gain, offset, and linearity drift)		±25	±150	ppm of FSR/°C
		±0.1	±0.68	% of FSR
		±0.01	±0.06	dB
Bipolar Zero Drift		±4	±20	ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)				
Voltage Model Output (PCM53-V): 10V Step		3		µsec
1LSB Step		1		µsec
Current Model (PCM53-I) Output (1mA Step): 10Ω to 100Ω Load		350		nsec
1kΩ Load[5]		350		nsec
Deglitcher Delay (THD Test)[4]		2.5	4.0	µsec
Slew Rate		10		V/µsec
WARM-UP TIME	1			Min
OUTPUT				
ANALOG OUTPUT				
Voltage Models				
Ranges: PCM53-V	±9.8	±10	±10.2	V
Output Current	±5			mA
Output Impedance		0.1		Ω
Short-Circuit Duration		Indefinite to Common		
Current Model				
Range, PCM53-I (±30%)		±1		mA
Output Impedance (±30%)		2.4		kΩ
POWER SUPPLY				
SENSITIVITY				
$+V_{CC}$		±0.001		% of FSR/%V_{CC}
$-V_{CC}$		±0.001		% of FSR/%V_{CC}
V_{DD}		±0.001		% of FSR/%V_{CC}
POWER SUPPLY REQUIREMENTS				
Voltage: ±V_{CC}	±14.25	±15	±15.75	VDC
V_{DD}	+4.75	+5	+15.75	VDC
(V_{DD} may be connected to +V_{CC} supply voltage. Result is slightly increased total power dissipation of approximately 40mW).				
Supply Drain (no load): +V_{CC}		+18	+30	mA
−V_{CC}		−18	−30	mA
V_{DD}		+4	+10	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating	−25		+85	°C

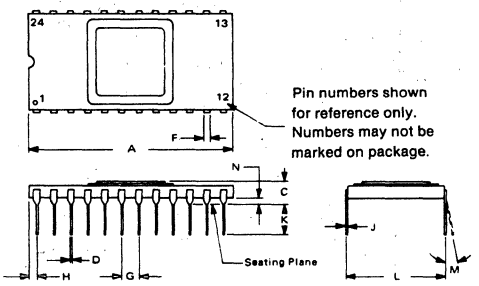
NOTES: (1) Adjustable to zero with external potentiometer. (2) FSR means Full-Scale Range and is 20V for ±10V (PCM53-V) and 10V for ±5V range (PCM52-V). (3) Characterization units show at least two sigma units to meet this specification. Not 100% final tested. (4) The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. Please contact factory for details. (5) Measured with an active clamp to provide a low impedance for approximately 200nsec.

DIGITAL INPUT AND ANALOG OUTPUT RELATIONSHIP

DIGITAL INPUT CODE	OUTPUT			
	Voltage Model		Current Model	
	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Bipolar Offset Binary (COB)				
±10V (PCM53): One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits On 00...00	+9.99969V	+9.99878V	−0.99997mA	−0.99988mA
All Bits Off 11...11	−10.00000V	−10.00000V	−1.00000mA	+1.00000mA

MECHANICAL

JG PACKAGE (TOP VIEW)



Pin numbers shown for reference only. Numbers may not be marked on package.

NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

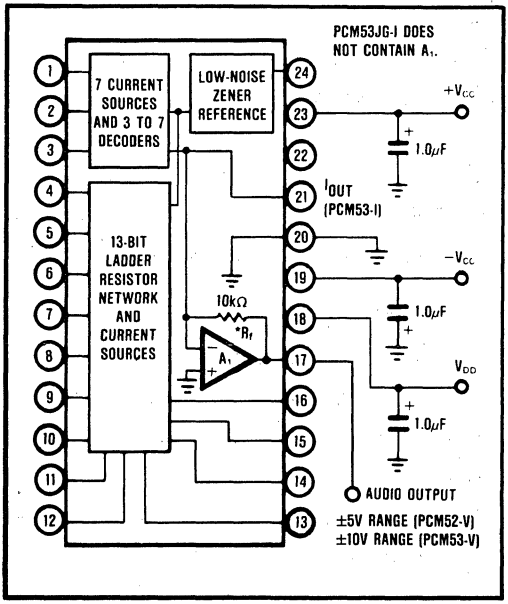
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.263	30.10	32.08
B	.514	.600	13.06	15.24
C	.105	.200	2.67	5.08
D	.015	.021	0.38	0.53
F	.035	.070	0.89	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.085	0.76	2.16
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	15°	—	15°
N	.025	.060	0.64	1.52

Actual package appearance may vary slightly from unit to unit. Pin spacing will not change.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages ..... ±18VDC
Input Logic Voltage .. −1V to +Supply Voltage
Storage Temperature ..... −55°C to +100°C
Lead Temperature
During Soldering ..... 10sec at +300°C

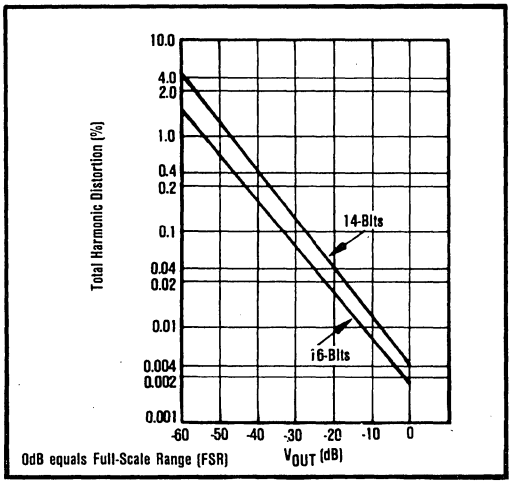
CONNECTION DIAGRAM



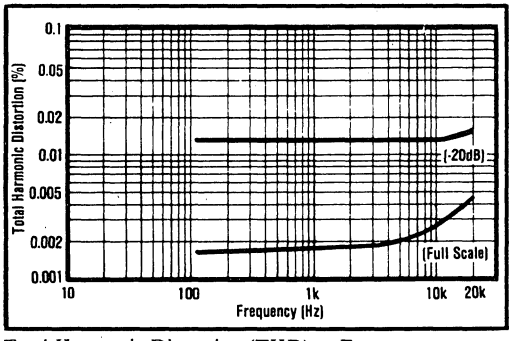
PIN ASSIGNMENTS

Pin No.	PCM52/53-V	PCM53-I
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 1
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 10
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	±10V Audio Out (PCM53-V)	R_f (10kΩ ±30%)
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	Summing Junction	I_{OUT}, ±1mA ±30% (Audio Output)
22	Test Point	Test Point
23	$+V_{CC}$	$+V_{CC}$
24	Reference Out (+6.3V)	Reference Out (+6.3V)

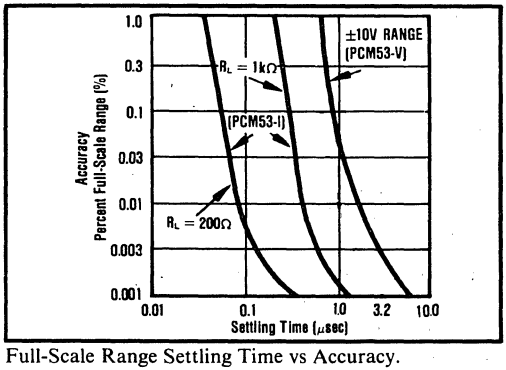
TYPICAL PERFORMANCE CURVES



Total Harmonic Distortion (THD) vs V_{OUT}.

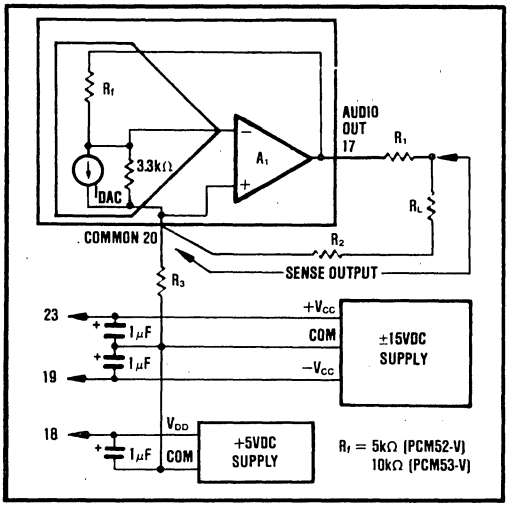


Total Harmonic Distortion (THD) vs Frequency.

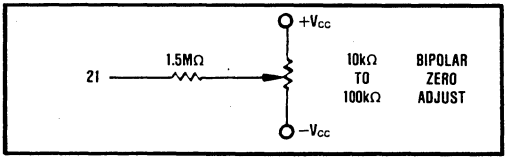


Full-Scale Range Settling Time vs Accuracy.

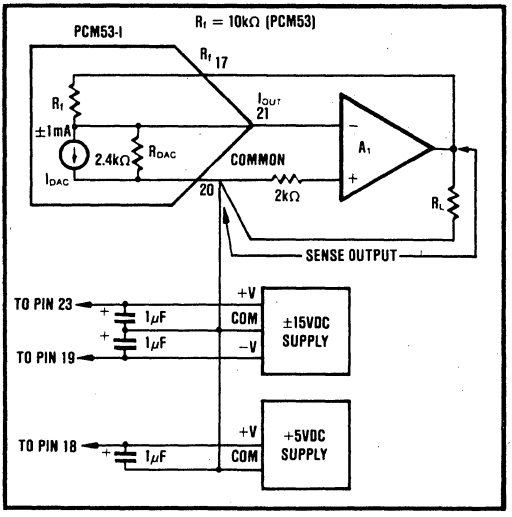
APPLICATION DIAGRAMS



Output Circuit for PCM53JG-V.



Optional External Bipolar Zero Adjust.



Preferred External Op Amp Configuration Using PCM53-I.

BURR-BROWN®

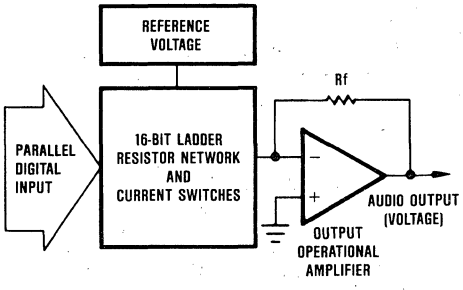
PCM53JP, KP

DESIGNED FOR AUDIO

16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 16-BIT MONOTONICITY, typ
- 0.001% OF FSR TYP DIFFERENTIAL LINEARITY ERROR
- 0.0025% max THD (FS Input, KP Grade, 16 Bits)
- 0.02% max THD (–20dB Input, KP Grade, 16 Bits)
- 3μsec SETTLING TIME, typ
- 96dB DYNAMIC RANGE
- ±10V AUDIO OUTPUT
- EIAJ STC-007 COMPATIBLE
- INDUSTRY-STANDARD PINOUT
- COMPACT, PLASTIC DIP PACKAGE



DESCRIPTION

The PCM53 family of converters are state-of-the-art, fully monolithic, digital-to-analog converters that are designed and specified for digital audio applications. These devices employ a segmented architecture and ultra-stable, nichrome (NiCr), thin-film, well-matched resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature range.

The PCM53 converters are completely self-contained with stable, low noise, internal, zener voltage reference; high speed current switches; resistor ladder network; and fast-settling, low noise, output operational amplifier all on a single monolithic chip. A special, open-loop reference circuit helps provide the fast settling time required for critical audio applications. The converters can be operated using two power supplies (±15V) instead of three separate supplies. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps to assure the user of high system reliability and outstanding overall system performance.

The current output models settle to within ±0.006% of FSR final value in typically 350nsec in response to a full-scale change in the digital input code.

These converters are packaged in a high-quality molded plastic package and have passed operating life tests under simultaneous high-pressure, high-temperature and high humidity conditions.

The letters V and I (e.g. PCM53JP-V and PCM53KP-I) refer to the voltage-output and current-output models respectively.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

T_A = +25°C rated power supplies unless otherwise noted.

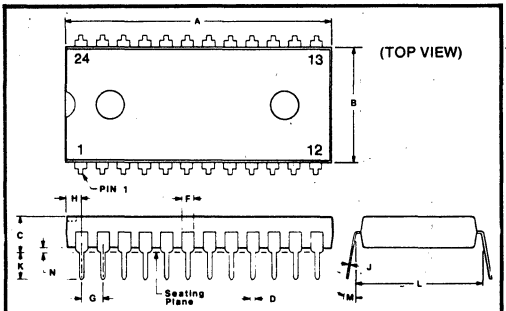
MODEL	PCM53JP-I, -V			PCM53KP-I, -V			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT							
DIGITAL INPUT							
Resolution		16			*		Bits
Dynamic Range		96			*		dB
Logic Levels (TTL/CMOS Compatible: Logic "1" at +40µA	+2.4		+V_{CC}	*		*	VDC
Logic "0" at −0.5mA	0		+0.8	*		*	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error		±0.1	±2.5		*	±1.0	%
Bipolar Zero Error[1]		±10	±200		*	±50	mV
Differential Linearity Error at Bipolar Zero		0.001	0.005		*	0.003	% of FSR[2]
Noise (rms)(20Hz to 20kHz) at Bipolar Zero (V_{OUT} models)		30	60		*		µV
TOTAL HARMONIC DISTORTION[3] (16-Bit Resolution)							
V_o = ±FS at f = 420Hz		0.002	0.004		*	0.0025	%
V_o = −20dB at f = 420Hz		0.02	0.04		*	0.02	%
V_o = −60dB at f = 420Hz		1.9	4.0		*	2.0	%
MONOTONICITY		16			*		Bits
DRIFT (0°C to +70°C)							
Total Bipolar Drift (includes gain, offset, and linearity drift)		±25	±150		*	*	ppm of FSR/°C
		±0.1	±0.68		*	*	% of FSR
		±0.01	±0.06		*	*	dB
Bipolar Zero Drift		±4	±20		*	*	ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)							
Voltage Models Output: 10V Step		3			*		µsec
1LSB Step		1			*		µsec
Current Models Output (1mA Step): 10Ω to 100Ω Load		350			*		nsec
1kΩ Load[4]		350			*		nsec
Deglitcher Delay (THD Test)[5]		2.5	4.0		*	*	µsec
Slew Rate		10			*		V/µsec
WARM-UP TIME	1			*			Min
OUTPUT							
ANALOG OUTPUT							
Voltage Models: Output Voltage Range	±9.75	±10	±10.25	±9.90	*	±10.1	V
Output Current	±5			*			mA
Output Impedance		0.1			*		Ω
Short-Circuit Duration		Indefinite to Common			*		
Current Models: Output Current Range(±30%)		±1			*		mA
Output Impedance (±30%)		2.4			*		kΩ
POWER SUPPLY							
SENSITIVITY							
+V_{CC}		±0.001			*		% of FSR/%V_{CC}
−V_{CC}		±0.001			*		% of FSR/%V_{CC}
V_{DD}		±0.001			*		% of FSR/%V_{CC}
POWER SUPPLY REQUIREMENTS							
Voltage: ±V_{CC}[6]	±14.25	±15	±15.75	*	*	*	VDC
V_{DD}[6]	+4.75	+5	+15.75	*	*	*	VDC
(V_{DD} may be connected to +V_{CC} supply voltage. Result is slightly increased total power dissipation of approximately 40mW).							
Supply Drain (no load): +V_{CC}[6]		+18	+30		*	*	mA
−V_{CC}[6]		−18	−30		*	*	mA
V_{DD}[6]		+4	+10		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Operating	−25		+85	*		*	°C

NOTES: (1) Adjustable to zero with external potentiometer. (2) FSR means Full-Scale Range and is 20V for ±10V voltage output models and 2mA for ±1mA current output models. (3) The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. A block diagram of a measurement circuit is shown in Figure 2. Burr-Brown may calculate THD from the measured linearity errors using equation 2 in the section on "Total Harmonic Distortion," but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated. (4) Measured with an active clamp to provide a low impedance for approximately 200nsec. (5) Deglitcher or Sample/Hold delay used in THD measurement test circuit. See Figures 2 and 3. (6) See Connection Diagram and Pin Assignments.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±18VDC
Input Logic Voltage	−1V to +Supply Voltage
Storage Temperature	−55°C to +100°C
Lead Temperature During Soldering	10sec at +300°C

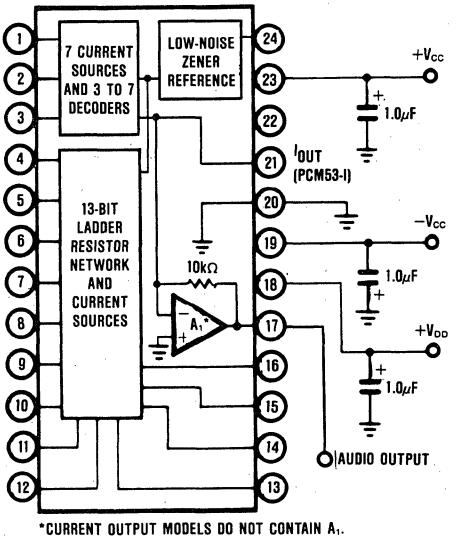
MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.233	1.263	31.32	32.69
B	.538	.575	13.67	14.61
C	.169	.224	4.29	5.70
D	.015	.023	0.38	0.58
F	.045	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

NOTE:
Leads in true position within 0.10" (0.25mm R at MMC at seating plane.

CONNECTION DIAGRAM



*CURRENT OUTPUT MODELS DO NOT CONTAIN A1.

PIN ASSIGNMENTS

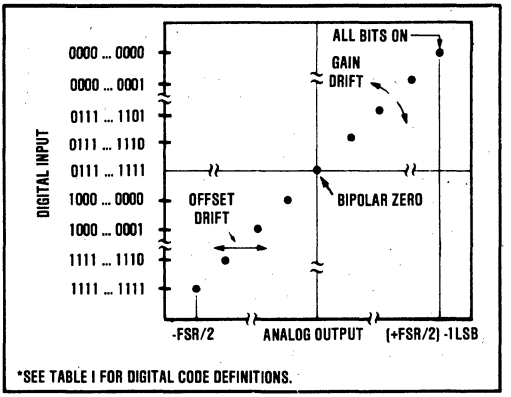
Pin No.	PCM53KP-V, PCM53JP-V	PCM53KP-I, PCM53JP-I
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 1
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 10
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	±10V Audio Out	R_f (10kΩ ±30%)
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	Summing Junction	I_{OUT}, ±1mA ±30% (Audio Output)
22	Test Point	Test Point
23	$+V_{CC}$	$+V_{CC}$
24	Reference Out (+6.3V)	Reference Out (+6.3V)

ORDERING INFORMATION

Model No.	Output Configuration
PCM53JP-I	±1mA
PCM53KP-I	±1mA
PCM53JP-V	±10V
PCM53KP-V	±10V

THEORY OF OPERATION AND AUDIO SPECIFICATIONS

The transfer function of an ideal binary D/A converter is a set of discrete output levels that lie on a straight line as shown in Figure 1. The number of possible discrete output levels, or resolution, is equal to 2^n where n is the number of digital inputs or "bits". The PCM53 has 2^{16} or 65,536 possible output levels. Another method of expressing resolution that is useful in audio applications is Dynamic Range.



*SEE TABLE I FOR DIGITAL CODE DEFINITIONS.

FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DYNAMIC RANGE

The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 × n, or about 96dB for a 16-bit converter. The actual, or useful, dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is Total Harmonic Distortion (THD).

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM53 is shown in Figure 2. A timing diagram of the control logic is shown in Figure 3.

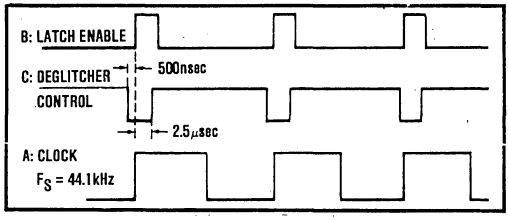


FIGURE 3. Control Logic Timing for PCM53 Distortion Test Circuit.

If we assume that the error due to the test circuit is negligible, then the rms value of the PCM53 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2} \qquad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM53 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \qquad (2)$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of

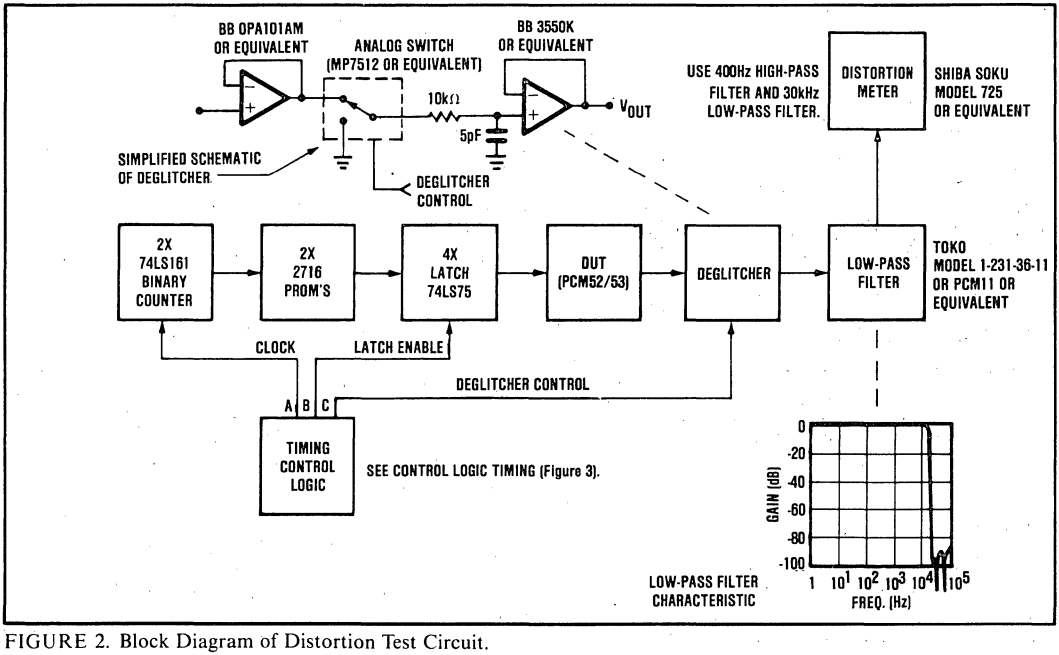


FIGURE 2. Block Diagram of Distortion Test Circuit.

the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM53 the test period was chosen to be 22.7μsec (44.1kHz) which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 420Hz and the amplitude of the input signal is 0dB, −20dB, and −60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

Figure 5 shows typical THD as a function of frequency.

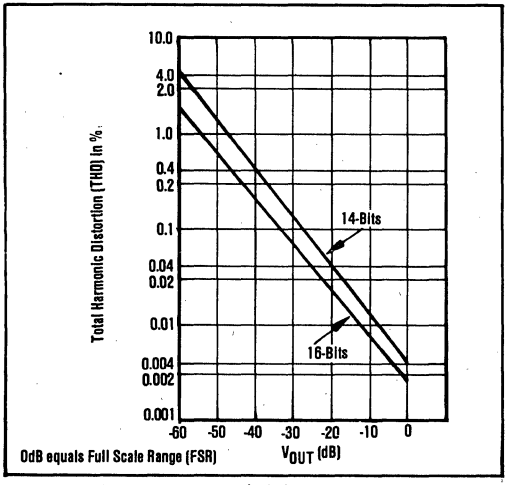


FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

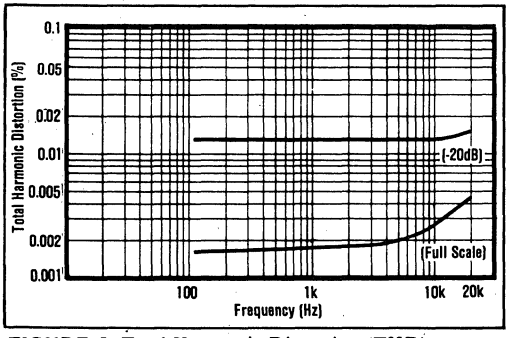


FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

DIGITAL INPUT CODES

The PCM53 accepts complementary digital input codes in binary format. It may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes. See Table I.

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES			
	MSB LSB	COB	CTC*
		Complementary Offset Binary	Complementary Two's Complement
All bits ON	0000...000	+Full Scale	-1LSB
Mid Scale	0111...111	Zero	-Full Scale
All bits OFF	1111...111	-Full Scale	Zero
	1000...000	-1LSB	+Full Scale

*A TTL inverter must be connected between the MSB input signal and bit 1 (pin 1) to obtain CTC input code.

DETAILED THEORY OF OPERATION

In the basic design, the three functions represented by the complete D/A converter—the voltage reference, the output amplifier, and the converter—are distributed among six major circuit blocks (Figure 6). Three blocks—the open loop reference, the current-offset circuit, and the reference output amplifier—perform the reference functions. The D/A conversion is performed by two circuits called the upper converter and the lower converter, which are combined into the voltage output by the on-chip output op amp.

The prime requirements for a D/A converter circuit designed for PCM audio applications are that it have low differential linearity error and monotonicity and that it stay that way over a useful temperature range. To obtain this performance at 14 to 16 bits, the converter combines segmentation with multiple R-2R networks.

The upper converter, which generates the three most significant bits, is made up of seven equal current sources (Q_1 R_{E1} through Q_7 R_{E7}), each providing 0.25mA. Together the sources form the upper converter current, I_{DACU}.

The three binary-coded MSBs (bits 1, 2, and 3) are decoded by a three-to-seven-line circuit, which sequentially selects the equal current sources as the binary code formed by the bits changes through the eight values (000 to 111). Thus, as the code ranges through its values, I_{DACU} changes from 0 to 1.75mA. This scheme ensures monotonicity, reduces initial matching and tracking requirements, and cuts the tracking errors that occur with temperature and time.

Averaging Transistor and Resistor Shifts

To further improve the tolerance of the upper converter to time and temperature change, the seven equal currents are turned on in the following order: Q_4, Q_2, Q_7, Q_5, Q_1, Q_6, Q_3. This sequence, which produces the zero-to-full-scale output, averages the shifts that occur in transistor parameters and in the value of the emitter resistors.

The 13 least significant bits are produced by the lower converter, which uses nine more equal-current sources for the nine middle bits and emitter area rationing for the 4LSBs. However, rather than being summed directly by the current of the upper converter (which would have required $2^{16} - 1$ equal current sources) the current sour-

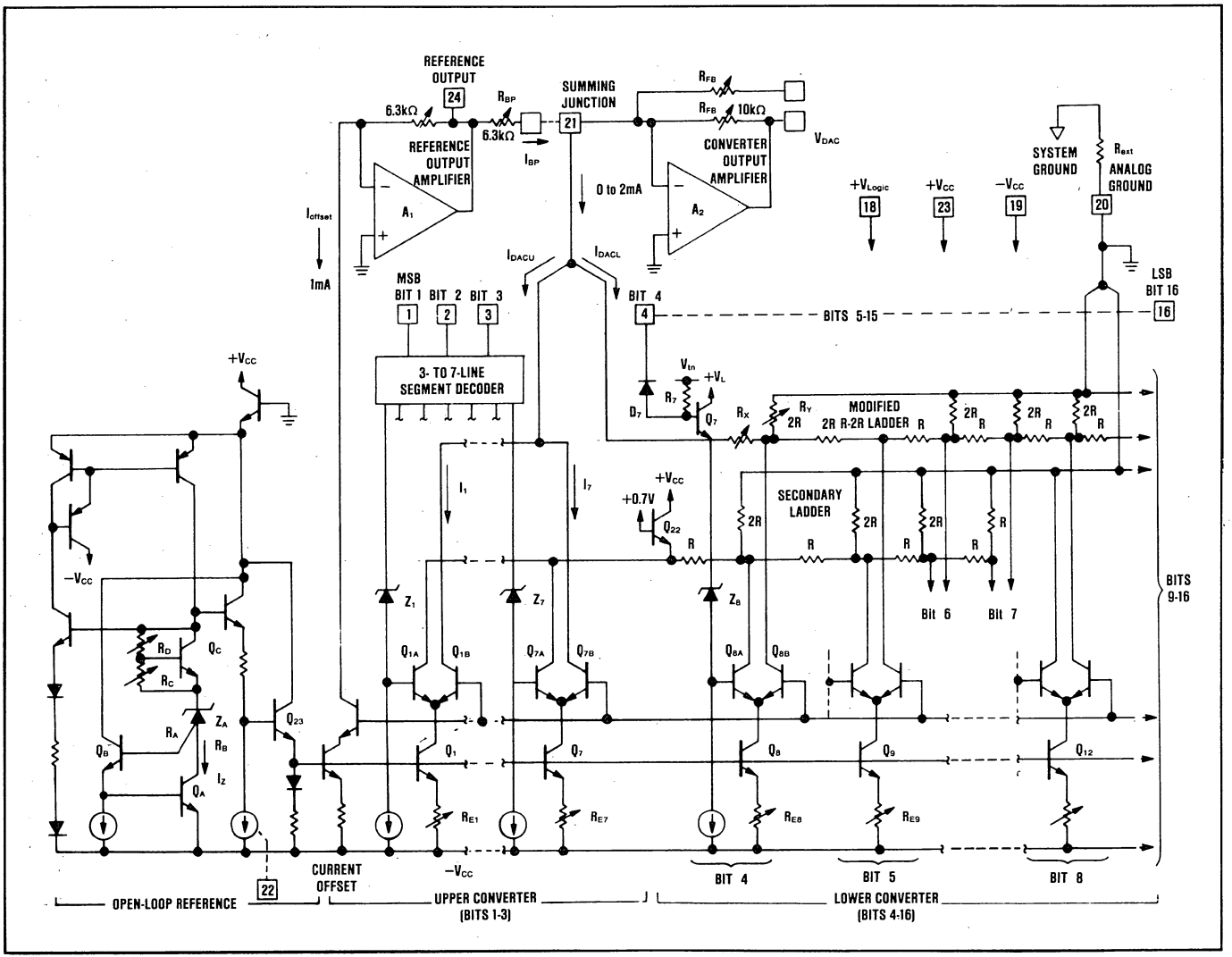


FIGURE 6. Simplified Circuit Diagram of the PCM53 16-bit Digital-to-Analog Converter.

ces are further divided binarily by a pair of R-2R networks, called the modified R-2R ladder and the secondary ladder. By diverting the LSB currents through the modified ladder, the lower converter produces I_{DACL}. This current consists of $2^{13} - 1$ discrete, 30nA steps for each 0.25mA segment of the upper converter. I_{DACU} and I_{DACL} are added at the summing junction, SJ, to form the I_{DAC}, which has a range that varies between 0 and 1.99997mA.

The modified R-2R ladder is superior to a conventional R-2R ladder because its output can be increased or decreased by laser-trimming of its output resistors (R_X and R_Y). Such trimming does not change the binary current division in the ladder. The gain of the lower converter can then be trimmed relative to the gain of the upper converter without interacting or in any way affecting the linearity of the lower converter.

The initial values of the 16 current sources are determined by the voltage at the output of the reference (the emitter of Q_{23}), but the sources are set to the same value when the emitter resistors (R_1–R_{16}) are laser-trimmed. The sources are turned on and off by a differential switch pair (such as Q_{8A}–Q_{8B}) driven by the low-power Schottky TTL-compatible input circuit (typical of D_7, R_7, Q_7, Z_8).

Constant Power

To maintain 16-bit performance, the on-chip power dissipation—and therefore the chip temperature—must be kept constant during code changes. Therefore the current from both the ON side (Q_{1B}) and the OFF side (Q_{1A}) of each differential switch pair in the upper converter should come from $+V_{CC}$, rather than one from $+V_{CC}$ and one from ground. The on-side currents (when the bits are on) come from $+V_{CC}$ and flow through A_2 and the feedback resistor, R_{FB}, to the summing junction to form I_{DACU}. Transistor Q_{22} is used to provide the off-side current with a similar path to $+V_{CC}$. In the lower converter, the secondary R-2R ladder, which is connected between the OFF side of the differential switches and Q_{22}, provides the same function by keeping the $+V_{CC}$ current and the analog ground current constant with code changes.

The secondary ladder also significantly reduces linearity errors that would otherwise be caused by external ground wiring. Indeed, the secondary ladder makes possible the use of a single ground pin, which is the only way to make all the connections in a 24-pin package.

Most converters use a closed-loop op amp for precision DC biasing of their current sources. However, switching transients can cause excessive settling time in the op amp. To ensure minimum settling time, the PCM53 uses an open-loop reference circuit, which incidentally does not require space-consuming capacitors for frequency compensation or suppression of switching transients.

The reference voltage is generated by a Kelvin-sensed buried zener diode. Kelvin sensing is used because the elements of the buried zener, R_A and R_B, have a large and nonlinear temperature coefficient. The Kelvin-sensed connection removes from the reference path the large voltage drop, R_BI_Z, caused by the 1mA zener current I_Z. Instead it substitutes the voltage drop produced across R_A by the base current of Q_B.

Since this base current is only 1μA, the drop is negligible, and the true zener breakdown, V_Z is sensed. In addition great care was taken to ensure that all temperature-sensitive parts of the open-loop reference were laid out along lines of thermal equilibrium, to prevent thermal settling tails.

High-Speed Output Amplifier

In voltage-output models, the output amplifier, A_2, which sums all of the output currents and converts them into the output voltage, V_{DAC}, must be just as accurate as the reference and current sources and just as fast as the switching circuits.

The amplifier is very fast, and it is well behaved when driving a capacitive load. It slews at 10V/μsec and typically settles to 0.003% of final value in less than 4μsec for a 20V step. For a step of 1LSB at the major carry, it settles in 1.5μsec. The thermal tails caused by temperature gradients and resistor self-heating are less than 0.001% of full scale.

Thermal tails occur when thermal gradients across the chip change as signal levels change. For example, when driving a load the output stage of the amplifier and its feedback resistor generate more heat at the full-scale output voltage than at zero. Therefore the temperature-sensitive differential input stage, which is close by on the chip, uses cross-coupled transistors and resistors to equalize thermal gradients.

To achieve a ±10V output swing when operating from ±15V, the output stage of the amplifier uses two transistor pairs connected in series. This scheme is necessary because the breakdown voltage of the npn transistors is limited to 20V by the semiconductor process.

In addition, the output stage is biased in a class AB condition, so that current is always flowing. Continuous current flow is essential to ensure that the open-loop gain, A_O, and closed-loop output impedance, R_O, remain constant for both positive and negative full-scale output swings at 103dB and 0.03Ω, respectively. With lesser performance, errors would occur. If, for example, A_O changed from 94dB to 100dB for an output swing of −10V to +10V respectively, the output error would change by 100μV, and the change would be nonlinear. Likewise a nonlinear error approaching 200μV would occur if R_O changed from 0.04Ω to 0.08Ω.

DISCUSSION OF SPECIFICATIONS

The PCM53 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are Total Harmonic Distortion, Differential Linearity Error, Bipolar Zero Error, parameter shifts with time and temperature and settling time effects on accuracy.

The PCM53 is factory-trimmed and tested for all critical key specifications.

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Offset or Bipolar Zero errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and Offset drift shifts the line left or right over the operating temperature range. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage.

BIPOLAR ZERO ERROR

Initial Bipolar Zero Error (Bit 1 "ON" and all other bits "OFF") is the deviation from zero volts out and is factory-trimmed to typically ±10mV at +25°C. This error may be trimmed to zero by connecting the external trim potentiometer shown in Figure 8.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at Bipolar Zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM53 is factory-trimmed to typically ±0.001% of FSR.

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM53 is designed so that these drifts are in opposite directions so that the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM53 was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM53 power supply sensitivity is specified for ±0.01% of FSR/%V_{CC} for all supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 7).

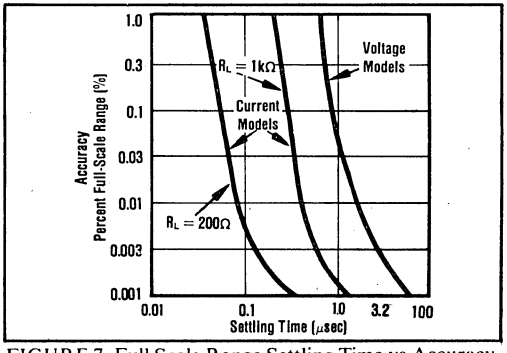


FIGURE 7. Full Scale Range Settling Time vs Accuracy.

Settling times are specified to ±0.006% of FSR; one for a large output voltage change of 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 10000...00), the point at which the worst-case settling time occurs.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the PCM53.

EXTERNAL BIPOLAR ZERO ADJUST (OPTIONAL)

In some applications the Bipolar Zero Error (offset) may require adjustment. This error may be adjusted to zero by installing an external potentiometer as shown in Figure 8. The potentiometer should have adequate resolution, at least 10 turns for full-scale adjustment.

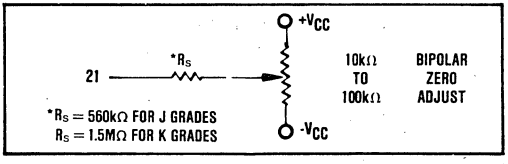


FIGURE 8. Optional External Bipolar Zero Adjust.

The TCR of the potentiometer should be 100ppm/°C or less. The series resistor, R_S (20% carbon or better) should be located close to the PCM53 to prevent noise pickup. Refer to Figure 9 for the relationship of Bipolar Zero adjust on the D/A converter transfer function.

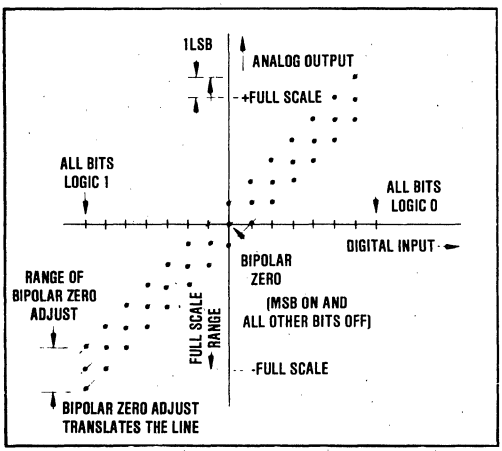


FIGURE 9. Effect of Bipolar Zero Adjustment on a Bipolar D/A Converter Transfer Function.

ADJUSTMENT PROCEDURE

Apply the digital input code that should produce zero volts output (bit 1 or MSB "ON" and all other bits "OFF"). Adjust the bipolar zero potentiometer until zero volts is obtained.

Table II shows the ideal plus and minus full scale voltages and LSB values for both 14- and 16-bits resolution.

TABLE II. Digital Input and Analog Output Relationship.

DIGITAL INPUT CODE	OUTPUT			
	Voltage Model		Current Model	
	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Bipolar Offset Binary (COB) ±10V (PCM53)				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits On 00...00	+9.99969V	+9.99878V	−0.99997mA	−0.99988mA
All Bits Off 11...11	−10.00000V	−10.00000V	−1.00000mA	+1.00000mA

INSTALLATION CONSIDERATIONS

If 14-bit resolution is desired, bit 15 (pin 15) and bit 16 (pin 16) should be connected to V_{DD} through a 1kΩ resistor to insure that these bits remain off.

Figure 10 shows the connection diagram for a PCM53-V. Figures 11 and 12 show connection diagrams for PCM53-I models.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance (R_L) is constant, R_1 simply introduces a gain error. R_2 is part of R_1 if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable, then R_1 should be less than $R_{L\min}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. R_L should be located as close as possible to the PCM53 for optimum performance.

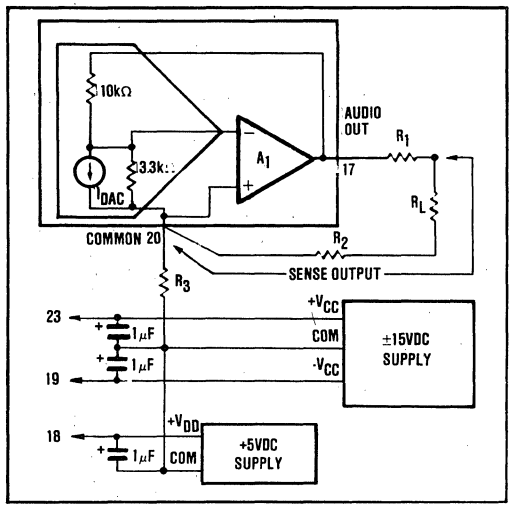


FIGURE 10. Output Circuit for PCM53-V.

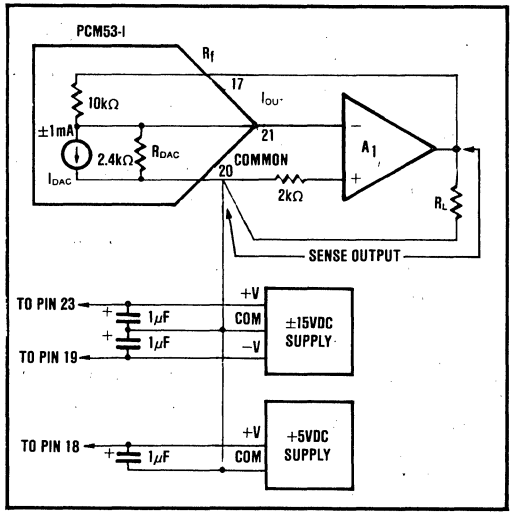


FIGURE 11. Preferred External Op Amp Configuration Using PCM53-I.

The PCM53 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

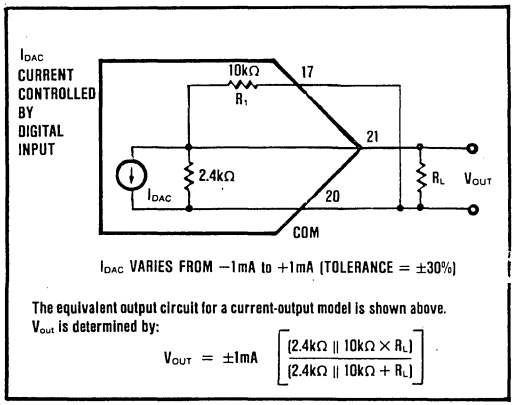


FIGURE 12. Driving a Resistive Load With PCM53-I.

Figures 11 and 12 show connection diagrams for PCM53-I models.

APPLICATIONS

Figures 13 and 14 show a circuit diagram and timing diagram of a single PCM53-V used to obtain both left and right channel audio output in a typical digital audio system. The Sony CX-7934 and associated LSI logic contain all of the required circuitry for error detection, correction, and formatting of the digital data obtained from the Compact Disc prior to sending this information to the D/A converter. The CX-7934 is used in a parallel output mode where the left and right channel parallel data are time-shared. Since the digital inputs of the PCM53 are TTL-compatible, they can be connected directly to the parallel outputs of the CX-7934. Only a single inverter is required (Bit 1) to convert the two's complement output code of the CX-7934 to offset binary. The audio output of the PCM53-V is alternately time-shared between the left and right channels. The design is greatly simplified because the PCM53-V is a complete D/A converter.

A sample/hold amplifier, or "deglitcher", is required at the output of the D/A converter for both the left and right channel, as shown in Figure 15. The S/H amplifier for the left channel is composed of A_2, SW_1, and associated circuitry. A_2 is used as an integrator to hold the analog voltage in C_1. Since the source and drain of the FET switch operates at a virtual ground when "C" and "B" are closed in the sample mode, there is no increase in distortion caused by the modulation effect of R_{on} by the audio signal.

Figure 16 shows the deglitcher control signals for both the left and right channels which are produced by the timing control logic. A delay of 2.5μsec (tω) is provided to eliminate the glitch and allow the output of the PCM53-V to settle within a small error band around its

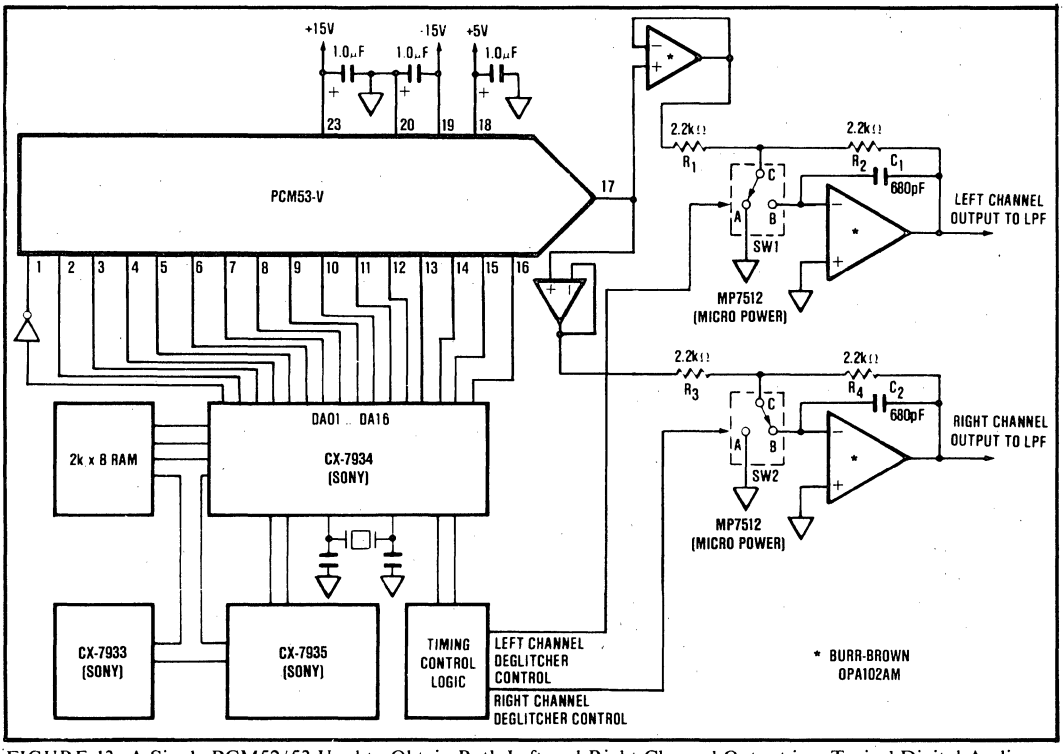


FIGURE 13. A Single PCM52/53 Used to Obtain Both Left and Right Channel Output in a Typical Digital Audio System.

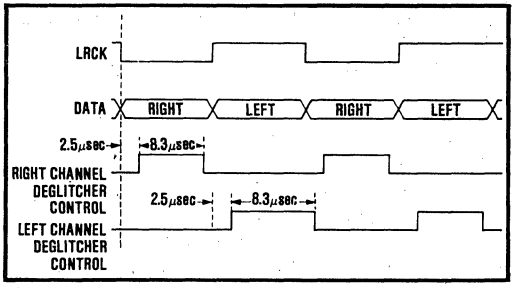


FIGURE 14. Timing Diagram for the Digital Audio System Using PCM53 and Sony LSI Logic.

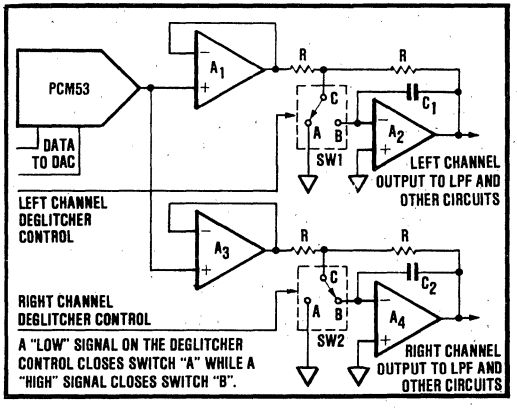


FIGURE 15. A Sample/Hold Amplifier (Deglitcher) is Required at the Digital-to-Analog Output for Both Left and Right Channels.

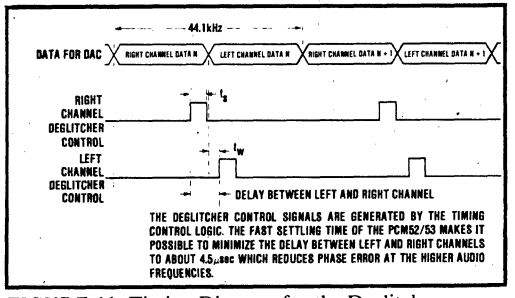


FIGURE 16. Timing Diagram for the Deglitcher Control Signals.

final value before connecting it to the channel output.

Due to the fast settling time of the PCM53-V, it is possible to minimize the delay between the left channel and right channel outputs when using a single D/A converter for both channels. This is important because the left and right channel data is recorded in phase and use of a slower D/A converter would result in significant phase error at the higher audio frequencies.

A low-pass filter is required at the S/H output to remove all unwanted frequency components caused by the sampling frequency as well as the discrete nature of the D/A converter output. The filter must have a flat amplitude response over the entire audio band (0 to 20kHz) and a very-high attenuation above 20kHz. Most previous digital audio circuits used a high-order (9-13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristics of the transients contained in music.

SECOND-GENERATION SYSTEMS

One method of avoiding this problem and obtaining a linear phase response is to use an oversampling digital filter technique as shown in Figure 17. The Yamaha YM-3511 and YM-2201 LSI chips provide all of the functions described for the Sony chip set and, in addition, contain an onboard digital oversampling filter which effectively multiplies the sampling frequency by a factor of two and sends the parallel data at a rate of 88.2kHz to the D/A converter. Since the offset binary parallel data is directly available from the YM-2201, no external inverter is required. Furthermore, since the deglitcher control signal is also available from the YM-2201, no external timing control logic is required for most applications. The timing diagram for this circuit is shown in Figure 18.

This circuit requires a very fast D/A converter since the sampling frequency is multiplied by a factor of two or more. This technique results in intermodulation products being created, by mixing the sampling frequency and components of the audio frequency, that are far outside the audio band of 0 to 20kHz. These unwanted frequencies are easily removed by a low-order linear-phase analog filter following the deglitcher circuit, since a sharp amplitude response is not required. A single PCM53-V can be used for both the left and right channel as long as the oversampling rate of the digital filter is two. An oversampling rate of four can be used if a separate PCM53 is used for each channel. This would reduce the complexities of the analog filter required even further (at the expense of an additional D/A converter).

Another factor to consider when choosing a D/A converter for digital audio applications is that the linearity of the total harmonic distortion versus output signal should be good since a change in the background noise level can be audible. The design of the PCM53 ensures that the linearity of the total harmonic distortion versus output signal level is very good over the full range of amplitude and frequencies. Also, no special grounding or shielding techniques are required to obtain good signal-to-noise ratio with the PCM53. Some converters require a high frequency clock which can couple to the analog output of the D/A converter through the output wiring and ground circuitry.

The PCM53 D/A converters provide a complete solution to one of the most critical portions of a digital audio system. Since the sound of the system can be affected by the D/A converter more than any other single component, the selection of which converter to use should be made with care.

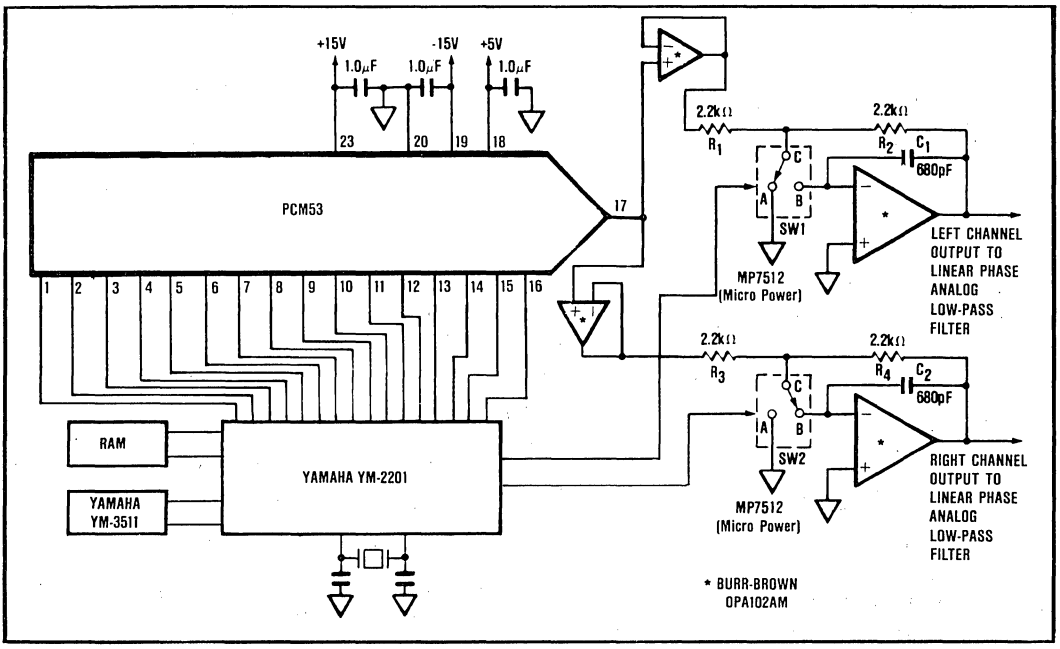


FIGURE 17. Oversampling Digital-Filter Technique Using Yamaha LSI.

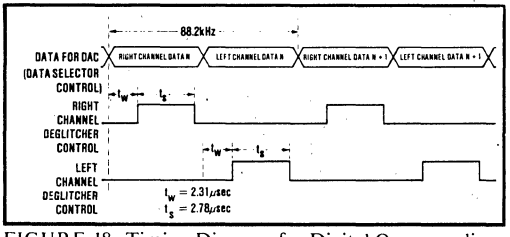


FIGURE 18. Timing Diagram for Digital Oversampling Technique when using Yamaha LSI.

BURR-BROWN®

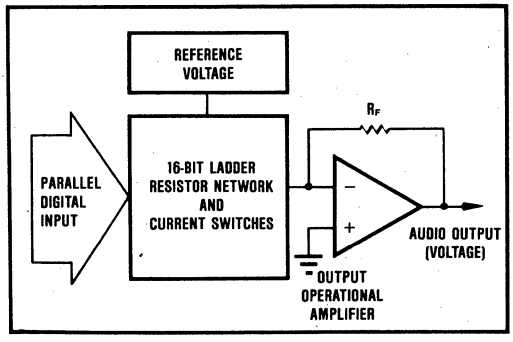
PCM54
PCM55

DESIGNED FOR AUDIO

16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- LOW COST
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 15-BIT MONOTONICITY, TYP
- 0.001% of FSR TYP DIFFERENTIAL LINEARITY ERROR
- 0.0025% MAX THD (FS Input, KP Grade, 16 Bits)
- 0.02% MAX THD (–20dB Input, KP Grade, 16 Bits)
- 3μs SETTLING TIME, TYP (Voltage Out)
- 96dB DYNAMIC RANGE
- ±3V or ±1mA AUDIO OUTPUT
- EIAJ STC-007-COMPATIBLE
- OPERATES ON ±5V (PCM55) to ±12V (PCM54) SUPPLIES
- PINOUT ALLOWS I_{OUT} OPTION
- PLASTIC DIP PACKAGE (PCM54)
- PLASTIC MINI-FLATPAK (PCM55)



DESCRIPTION

The PCM54 and PCM55 family of converters are state-of-the-art, fully monotonic, digital-to-analog converters that are designed and specified for digital audio applications. These devices employ ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

These converters are completely self-contained with a stable, low noise, internal, zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise, output operational amplifier all on a single monolithic chip. The converters are operated using two power supplies that can range from ±5V (PCM55) to ±12V (PCM54). Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero, PCM54 only) to further improve THD specifications if desired. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps assure the user of high system reliability and outstanding overall system performance.

A current output (I_{OUT}) wiring option is provided. This output typically settles to within ±0.006% of FSR final value in 350ns (in response to a full-scale change in the digital input code).

These converters are packaged in high-quality molded plastic packages and have passed operating life tests under simultaneous high-pressure, high-temperature, and high-humidity conditions.

The PCM54 is packaged in 28-pin plastic DIP package. The PCM55 is available in a 24-pin plastic mini-flatpak.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 12V, unless otherwise noted.

MODEL	PCM54HP			PCM54JP			PCM54KP			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT										
Resolution		16			*			*		Bits
Dynamic Range		96			*			*		dB
Logic Levels (TTL/CMOS Compatible):										
V_{IH}	+2.4		+5.25	*		*	*		*	V
V_{IL}	0		+0.8	*		*	*		*	V
I_{IH}, V_{IN} = +2.7V			+40			*			*	µA
I_{IL}, V_{IN} = + 0.4V			−0.5			*			*	mA
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error		±2			*			*		%
Bipolar Zero Error		±30			*			*		mV
Differential Linearity Error at Bipolar Zero[1]		±0.001			*			*		% FSR[2]
Noise (rms) (20Hz to 20kHz) at Bipolar Zero		12			*			*		µV
TOTAL HARMONIC DISTORTION[3]										
(16-bit resolution)										
V_O = ±FS at f = 991Hz		0.002	0.008		*	0.004		*	0.0025	%
V_O = −20dB at f = 991Hz		0.02	0.04		*	*		0.1	0.02	%
V_O = −60dB at f = 991Hz		2.0	4.0		*	*		1.0	2.0	%
MONOTONICITY		15			*			*		Bits
SETTLING TIME (to ±0.006% of FSR)										
Voltage Output: 6V Step		3			*			*		µs
1LSB Step		1			*			*		µs
Current Output (1mA Step): 10Ω to 100Ω Load		350			*			*		ns
1kΩ Load[4]		350			*			*		ns
Deglitcher Delay (THD Test)[5]		2.5	4.0		*	*		*	*	µs
Slew Rate		10			*			*		V/µs
WARM-UP TIME	1			*			*			Min
ANALOG OUTPUT										
Voltage Output: Bipolar Range		±3.0			*			*		V
Output Current	±2.0			*			*			mA
Output Impedance		0.1			*			*		Ω
Short-Circuit Duration		Indefinite to Common			*			*		
Current Output:[6]										
Bipolar Range (±30%)		±1			*			*		mA
Bipolar Output Impedance (±30%)		1.2			*			*		kΩ
POWER SUPPLY REQUIREMENTS										
Voltage: $+V_{CC}$	+4.75	+12	+15.75	*	*	*	*	*	*	V
$-V_{CC}$	−4.75	−12	−15.75	*	*	*	*	*	*	V
Supply Drain: $+V_{CC}$		+13	+20		*	*		*	*	mA
$-V_{CC}$		−16	−25		*	*		*	*	mA
TEMPERATURE RANGE										
Operating	0		+70	*		*	*		*	°C
Storage	−55		+100	*		*	*		*	°C

*Specification same as PCM54HP.

NOTES: (1) Externally adjustable. If external adjustment is not used, connect a 0.01µF capacitor to Common to reduce noise pickup. (2) FSR means Full-Scale Range and is 6V for ±3V output. (3) The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. Burr-Brown may calculate THD from the measured linearity errors using equation 2 in the section on "Total Harmonic Distortion" but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) Deglitcher or sample/hold delay used in THD measurement test circuit. See Figures 2 and 3. (6) Output amplifier disconnected.

SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 5V, unless otherwise noted.

MODEL	PCM55HP			PCM55JP			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DIGITAL INPUT							
Resolution		16			*		Bits
Dynamic Range		96			*		dB
Logic Levels (TTL/CMOS Compatible): V_{IH}	+2.4		+5.25	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH}, V_{IN} = +2.7V			+40			*	µA
I_{IL}, V_{IN} = + 0.4V			−0.5			*	mA
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error		±2.0			*		%
Bipolar Zero Error		±30			*		mV
Differential Linearity Error at Bipolar Zero[1]		±0.001			*		% FSR[2]
Noise (rms) (20Hz to 20kHz) at Bipolar Zero		12			*		µV
TOTAL HARMONIC DISTORTION[3](16-bit resolution)							
V_O = ±FS at f = 991Hz		0.002	0.008		*	0.004	%
V_O = −20dB at f = 991Hz		0.02	0.04		*	*	%
V_O = −60dB at f = 991Hz		1.9	4.0		*	*	%
MONOTONICITY		15			*		Bits
DRIFT							
Total Bipolar Drift		±25			*		ppm of FSR/°C
Drift Over Operating Temperature Range		±0.1			*		%
Bipolar Zero Drift		±4			*		ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)							
Voltage Output: 6V Step		3			*		µs
1LSB Step		1			*		µs
Current Output (1mA Step): 10Ω to 100Ω Load		350			*		ns
1kΩ Load[4]		350			*		ns
Deglitcher Delay (THD Test)[5]		2.5	4.0		*	*	µs
Slew Rate		10			*		V/µs
WARM-UP TIME	1			*			Min
ANALOG OUTPUT							
Voltage Output: Bipolar Range		±3.0			*		V
Output Current	±2.0			*			mA
Output Impedance		0.1			*		Ω
Short-Circuit Duration		Indefinite to Common			*		
Current Output[6]: Bipolar Range (±30%)		±1			*		mA
Bipolar Output Impedance (±30%)		1.2			*		kΩ
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	+4.75	+5	+7.5	*	*	*	V
$-V_{CC}$	−4.75	−5	−7.5	*	*	*	V
Supply Drain: $+V_{CC}$		+13	+20		*	*	mA
$-V_{CC}$		−16	−25		*	*	mA
TEMPERATURE RANGE							
Operating	0		+70	*		*	°C
Storage	−55		+100	*		*	°C

*Specification same as PCM55HP.

NOTES: (1) FSR means Full-Scale Range and is 6V for ±3V output. (2) Externally adjustable. If external adjustment is not used, connect a 0.01µF capacitor to Common to reduce noise pickup. (3) The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. Burr-Brown may calculate THD from the measured linearity errors using equation 2 in the section on "Total Harmonic Distortion" but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) Deglitcher or sample/hold delay used in THD measurement test circuit. See Figures 2 and 3. (6) Output amplifier disconnected. I_{OUT} application: Close the feedback around the amplifier by connecting output of amplifier to the minus input.

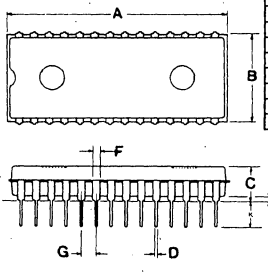
PIN ASSIGNMENTS

Pin	PCM54-DIP	Pin	PCM54-DIP
1	Trim	15	Bit 13
2	Bit 1 (MSB)	16	Bit 14
3	Bit 2	17	Bit 15
4	NC	18	Bit 16 (LSB)
5	Bit 3	19	V_{OUT}
6	Bit 4	20	R_{FB}
7	Bit 5	21	SJ
8	Bit 6	22	Common
9	Bit 7	23	I_{OUT}
10	Bit 8	24	NC
11	Bit 9	25	I_{BPO}
12	Bit 10	26	$+V_{CC}$
13	Bit 11	27	MSB Adjust
14	Bit 12	28	$-V_{CC}$

Pin	PCM55-Flatpak	Pin	PCM55-Flatpak
1	Bit 1 (MSB)	13	Bit 13
2	Bit 2	14	Bit 14
3	Bit 3	15	Bit 15
4	Bit 4	16	Bit 16
5	Bit 5	17	Voltage Output
6	Bit 6	18	Feedback Resistor
7	Bit 7	19	Summing Junction
8	Bit 8	20	Common
9	Bit 9	21	Current Output
10	Bit 10	22	Bipolar Offset
11	Bit 11	23	$+V_{CC}$
12	Bit 12	24	$-V_{CC}$

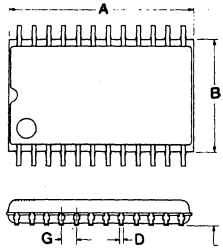
MECHANICAL OUTLINES

PCM54



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	1.441	---	36.60
B	---	.575	---	14.60
C	---	.224	---	5.70
D	.019	.019	0.47	0.49
F	.047	.055	1.20	1.40
G	.090	.110	2.29	2.79
J	.008	.015	0.20	0.38
K	.100	---	2.54	---
L	---	.600	---	15.24
M	0°	15°	0°	15°
N	.020	---	0.51	---

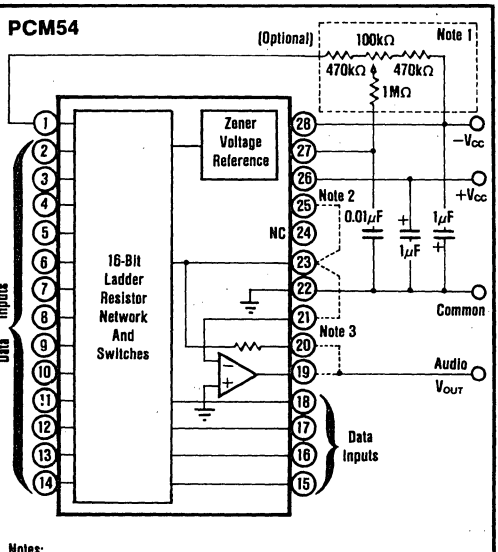
PCM55



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.614	.630	15.60	16.00
B	.346	.362	8.80	9.20
C	---	.098	---	2.50
D	.012	.020	0.30	0.50
G	.046	.054	1.17	1.37

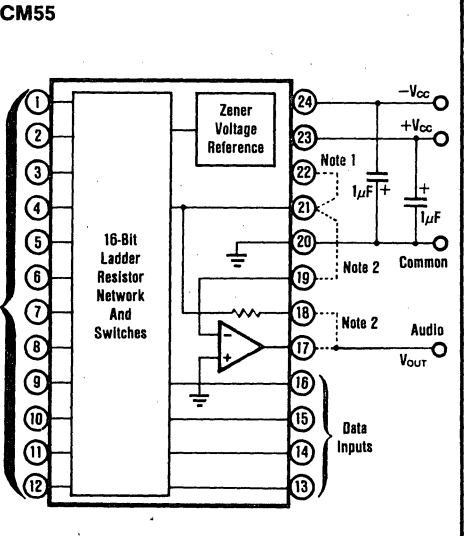
CONNECTION DIAGRAMS

PCM54



Notes:
(1) MSB error (8PZ differential linearity error) can be adjusted to zero using this external circuit.
(2) Connect for bipolar operation ($+V_{CC} \geq 8.5V$ for unipolar operation).
(3) Connect for V_{OUT} operation. When V_{OUT} amp is not being used (I_{OUT} mode), terminate with an external 3kΩ feedback resistor between pin 19 and pin 21 and a 1kΩ resistor between pin 21 and pin 22 to reduce possible noise effects.

PCM55



Notes:
(1) Connect for bipolar operation ($+V_{CC} \geq 8.5V$ for unipolar operation).
(2) Connect for V_{OUT} operation. When V_{OUT} amp is not being used (I_{OUT} mode), terminate with an external 3kΩ feedback resistor between pin 17 and pin 19 and a 1kΩ resistor between pin 19 and pin 20 to reduce possible noise effects.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±18VDC
Input Logic Voltage	−1V to +5.5V
Power Dissipation	PCM54 800mW, PCM55 400mW
Storage Temperature	−55°C to +100°C
Lead Temperature During Soldering	10s at +300°C

ORDERING INFORMATION

Model	THD at FS	Package
PCM54HP	0.008	28-pin DIP
JP	0.004	28-pin DIP
KP	0.0025	28-pin DIP
PCM55HP	0.008	24-lead mini flat pak
JP	0.004	24-lead mini flat pak

DISCUSSION OF SPECIFICATIONS

The PCM54 and PCM55 are specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are Total Harmonic Distortion, Differential Linearity Error, Bipolar Zero Error, parameter shifts with time and temperature, and settling time effects on accuracy.

The PCM54 and PCM55 are factory-trimmed and tested for all critical key specifications.

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. Digital input to analog output relationship is shown in Table I. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and Offset drift shifts the line left or right over the operating temperature range. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage.

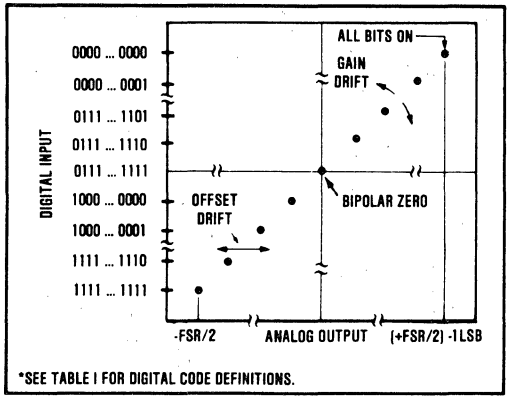


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DIGITAL INPUT CODES

The PCM54 and PCM55 accept complementary digital input codes in any of three binary formats (CSB, unipolar; or COB, bipolar; or CTC, Complementary Two's Complement, bipolar). See Table II.

TABLE II. Digital Input Codes.

Digital Input Codes	Analog Output: Complementary Straight Binary (CSB)	Analog Output: Complementary Offset Binary (COB)	Analog Output: Complementary Two's Complement (CTC)*
0000_H	+ Full Scale	+ Full Scale	−1LSB
$7FFF_H$	+1/2Full Scale	Bipolar Zero	− Full Scale
8000_H	+1/2 Full Scale −1LSB	−1LSB	+ Full Scale
$FFFF_H$	Zero	− Full Scale	Bipolar Zero

Invert the MSB of the COB code with an external inverter to obtain CTC code.

TABLE I. Digital Input to Analog Output Relationship.

	VOLTAGE OUTPUT MODE					
	Analog Output					
	Unipolar*			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μV)	91.6	183	366	91.6	183	366
0000_H (V)	+5.99991	+5.99982	+5.99963	+2.99991	+2.99982	+2.99963
$FFFF_H$ (V)	0	0	0	−3.0000	−3.0000	−3.0000
	CURRENT OUTPUT MODE					
	Analog Output					
	Unipolar			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μA)	0.031	0.061	0.122	0.031	0.061	0.122
0000_H (mA)	−1.99997	−1.99994	−1.99988	−0.99997	−0.99994	−0.99988
$FFFF_H$ (mA)	0	0	0	+1.00000	+1.00000	+1.00000

*NOTE: $+V_{CC}$ must be at least +8.5VDC to allow output to swing to +6.0VDC.

BIPOLAR ZERO ERROR

Initial Bipolar Zero Error (Bit 1 "ON" and all other bits "OFF") is the deviation from 0V out and is factory-trimmed to typically ±10mV at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at Bipolar Zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM54 and PCM55 is factory trimmed to typically ±0.001% of FSR. This error is adjustable to zero using the circuit shown in the connection diagram (PCM54 only).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy.

The PCM54 and PCM55 power supply sensitivity is shown by Figure 2. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

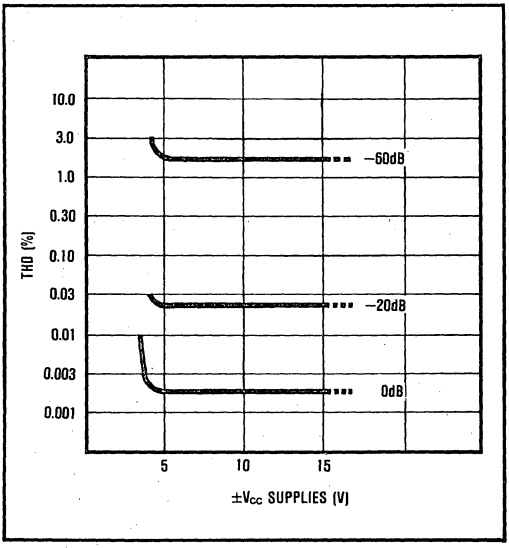


FIGURE 2. Effects of $\pm V_{CC}$ on Total Harmonic Distortion (PCM54JP; V_{CC}s with approximately 2% ripple).

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 3).

Settling times are specified to ±0.006% of FSR; one for a large output voltage change of 3V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 10000.00), the point at which the worst-case settling time occurs.

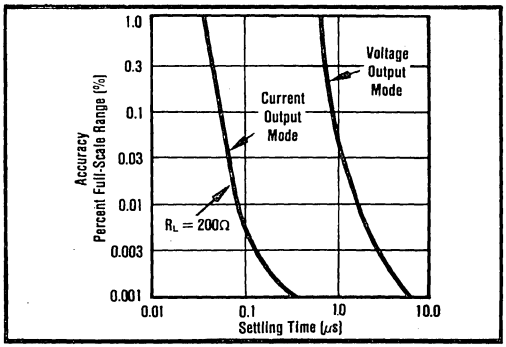


FIGURE 3. Full Scale Range Settling Time vs Accuracy.

STABILITY WITH TIME AND TEMPERAURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM54 and PCM55 are designed so that these drifts are in opposite directions so that the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM54 and PCM55 were designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

DYNAMIC RANGE

The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 × n, or about 96dB for a 16-bit converter. The actual, or useful, dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is Total Harmonic Distortion (THD).

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quan-

tization Error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. The rms value of the PCM54/55 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2} \quad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM54 or PCM55 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \quad (2)$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM54/55 the test period was chosen to be 22.7μs (44.1kHz) which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 420Hz and the amplitude of the input signal is 0dB, −20dB, and −60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

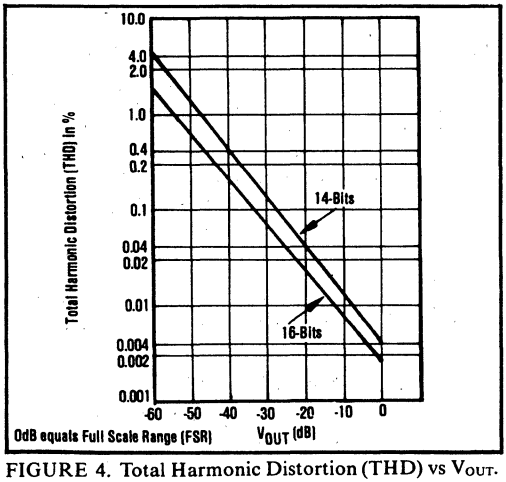


FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

Figure 5 shows typical THD as a function of frequency.

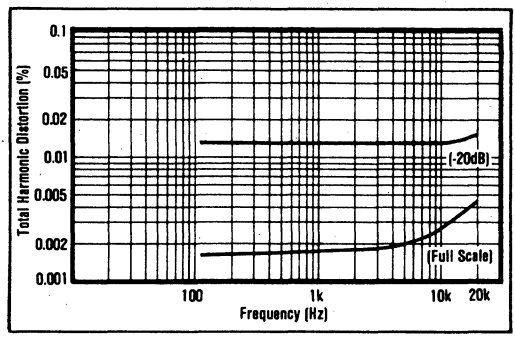


FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the converter.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM54 and PCM55 can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

Differential linearity error at bipolar zero is guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point which makes it possible to eliminate DLE error at BPZ (PCM54 only). Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 6 or the PCM54 connection diagram. After allowing ample warm-up time (20–30 minutes) to assure stable operation of the PCM54, select input code 8000 hexadecimal (all bits on except the MSB). Measure the audio output voltage using a 6-1/2 digit voltmeter and record it. Change the digital input code to 7FFF hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the audio output read 92μV more than the voltage reading of the previous code (a 1LSB step = 92μV).

A much simpler method is to dynamically adjust the DLE at BPZ. Again, refer to Figure 6 or the PCM54 connection diagram for circuitry and component values. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a −60dB level sinusoidal output. While measuring the THD of the audio circuit output, adjust the 100kΩ potentiometer until a minimum level of distortion is observed.

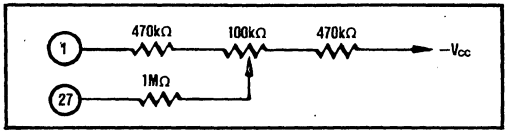


FIGURE 6. MSB Differential Linearity at Bipolar Zero Adjustment Circuit (optional).

INSTALLATION CONSIDERATIONS

If the optional external MSB error circuitry is used (PCM54), a potentiometer with adequate resolution and a TCR of 100ppm/°C or less is required. Also, extra care must be taken to insure that no leakage path (either AC or DC) exists to pin 27 (PCM54). If the circuit is not used, pin 1 (PCM54) should be terminated to common with a 0.01μF capacitor.

The PCM converter and the wiring to its connectors should be located to provide the optimum isolation from sources of RFI and EMI. The important consideration in the elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they represent a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

A sample/hold amplifier, or "deglitcher", is required at the output of the D/A converter for both the left and right channel, as shown in Figure 7. The S/H amplifier for the left channel is composed of A_2, SW_1, and associated circuitry. A_2 is used as an integrator to hold the analog voltage in C_1. Since the source and drain of the FET switch operates at a virtual ground when "C" and "B" are closed in the sample mode, there is no increase in distortion caused by the modulation effect of R_{ON} by the audio signal.

Figure 8 shows the deglitcher control signals for both the left and right channels which are produced by the timing control logic. A delay of 2.5μs (tω) is provided to eliminate the glitch and allow the output of the PCM53-V to settle within a small error band around its final value before connecting it to the channel output.

Due to the fast settling time of the PCM53-V, it is possible to minimize the delay between the left channel and right channel outputs when using a single D/A converter for both channels. This is important because the left and right channel data is recorded in phase and use of a slower D/A converter would result in signficant phase error at the higher audio frequencies.

A low-pass filter is required at the S/H output to remove all unwanted frequency components caused by the sampling frequency as well as the discrete nature of the D/A converter output. The filter must have a flat amplitude response over the entire audio band (0 to 20kHz) and a very-high attenuation above 20kHz. Most previous digital audio circuits used a high-order (9–13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristics of the transients contained in music.

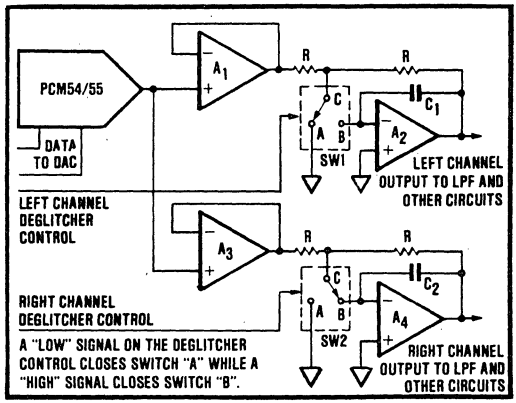


FIGURE 7. A Sample/Hold Amplifier (Deglitcher is Required at the Digital-to-Analog Output for Both Left and Right Channels.

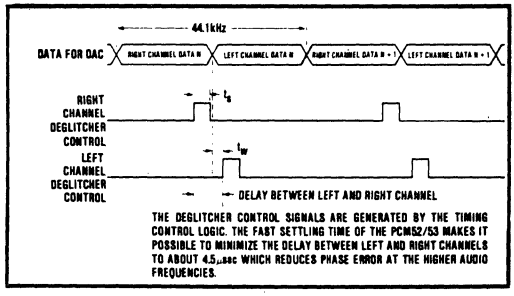
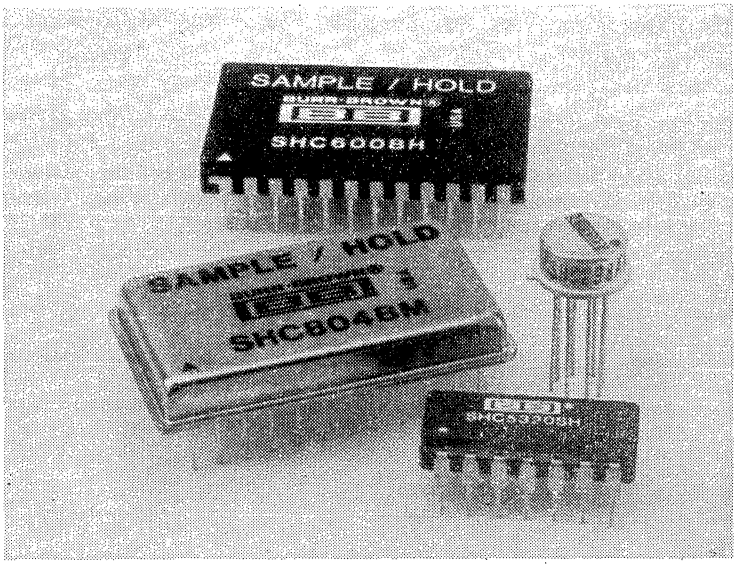


FIGURE 8. Timing Diagram for the Deglitcher Control Signals.

SAMPLE/HOLD AMPLIFIERS



For any application requiring use of a sample/hold amplifier, consider the variety of products listed in the Selection Guide in this section. The products range from SHC298, a low cost solution for your medium-speed 12-bit system, to SHC803 and SHC804, high speed sample/holds optimized for your high bandwidth requirements.

If your needs include high performance and small size over either industrial or military temperature ranges, turn to SHC80 and SHC85. These popular products are fully self-contained, including holding capacitor.

Use of a carefully selected sample/hold can increase the sampling bandwidth of an analog-to-digital converter by up to four orders of magnitude, while insuring that an accurate value of the signal is captured at a specific point in time. In many applications not viewed as requiring high bandwidth data acquisition, optimum performance and cost may still be achieved by use of combinations of very high speed multiplexers, sample/holds, and A/D converters.

Sample/hold amplifiers—another part of the complete data acquisition solution.

SELECTION GUIDE

SAMPLE/HOLD AMPLIFIERS

These sample/hold amplifiers were designed as companion products for our complete line of 12- and 16-bit resolution A/D converters. They are also useful in other analog signal processing applications, such ad D/A output deglitching.

SAMPLE/HOLD AMPLIFIERS									
Description	Model[1]	Gain Error (%)	Offset Error (mV)	Charge Offset (mV)	Droop Rate, max (mV/msec)	Gain Drift (ppm of 20V/°C)	Acquisition Time, max[2]	Package	Page
Fast, High Accuracy	SHC76KM SHC76BM	±0.02 ±0.02	±3 ±3	±6 typ ±6 typ	1 1	5 5	3μsec to 0.01% of 20V	14-pin DIP, Hermetic, Metal	7-3 7-3
Monolithic	SHC298AM	±0.01	±7 max	±25 max	10[3]	4	10μsec	TO-99	7-15
Low Cost, Monolithic	SHC5320KH SHC5320SH	NA NA	±0.5[4][5] ±0.5[4][5]	1mV typ 1mV typ	0.5 0.5	NA[4] NA[4]	1.5μsec 1.5μsec	14-pin DIP, Hermetic, Ceramic	7-30 7-30
Industry Standard	SHC85, (Q) SHC85ET, (Q)	±0.01 ±0.01	±2 max ±2 max	±2 max ±2 max	0.5 0.5	3 3	4.5μsec 4.5μsec	14-pin DIP, Hermetic, Metal	7-11 7-11
High Speed With Input Buffer	SHC803BM SHC803CM SHC804BM SHC804CM	±0.1 ±0.1 ±0.1 ±0.1	±5 max ±3 max ±5 max ±3 max	±10 max ±5 max ±10 max ±5 max	±5 ±5 ±5 ±5	±10 max ±5 max ±10 max ±5 max	350nsec 350nsec 350nsec 350nsec	24-pin DIP, Metal	7-24 7-24 7-24 7-24
Ultra-High Speed, ±1.25V_{IN} Range	SHC600BH	±0.1	±5mV	±10 max	±0.18	±20 max	1%, 25nsec 0.1%, 35nsec 0.02%, 50nsec	24-pin DIP, Ceramic	7-21

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, section 12. (2) 10V step to ±0.01% of final value. (3) With 1000pF external holding capacitor. (4) Input amplifier is uncommitted. (5) Input amplifier offset voltage.

BURR-BROWN®

SHC76

SAMPLE/HOLD AMPLIFIER

FEATURES

- FAST (6μs max) ACQUISITION TIME (14-bit)
- APERTURE JITTER 400ps
- TYPICAL POWER DISSIPATION LESS THAN 250mW
- COMPATIBLE WITH HIGH RESOLUTION A/D CONVERTERS ADC76, PCM75, AND ADC71

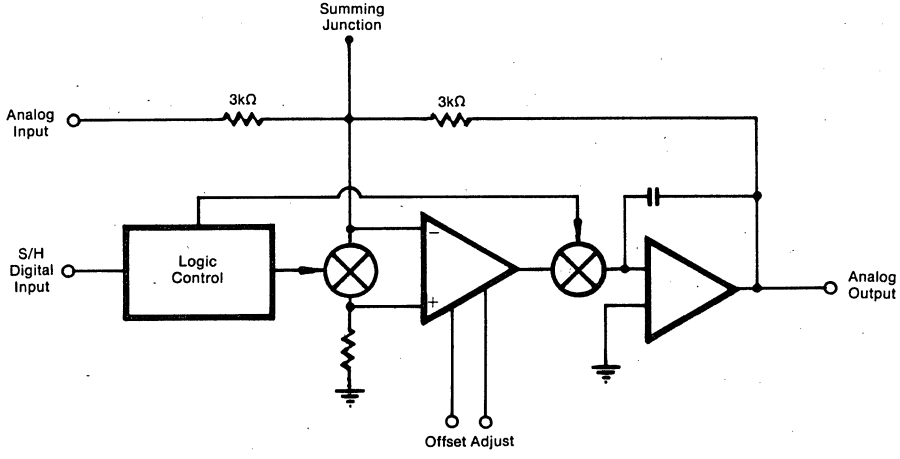
DESCRIPTION

The SHC76 is a fast, high-accuracy hybrid sample/-hold circuit suitable for use in high-resolution data acquisition systems.

The SHC76 is complete with internal hold capacitor and incorporates an internal compensation network which minimizes sample-to-hold charge offset. The SHC76 is configured as a unity-gain inverter.

High-resolution converters such as the ADC76 and ADC71 are compatible with SHC76 in forming complete, 14-bit accurate analog-to-digital conversion systems.

The SHC76 comes in a 14-pin single-wide hermetic metal DIP. Power supply requirements are specified from ±14.5 V to ±15.5V with guaranteed operation from ±11.4V to ±18V. Input voltage range is ±10V. The SHC76 is available in two temperature ranges: KM, for 0°C to +70°C; and BM, for −25°C to +85°C operation.



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SPECIFICATIONS

ELECTRICAL

Typical at +25°C and nominal power supply voltage of ±15V unless otherwise noted.

MODEL	SHC76KM/BM			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG INPUT				
Voltage Range	±10			V
Overvoltage, no damage			±15	V
Impedance		3000		Ω
DIGITAL INPUT				
(TTL-Compatible)				
Track Mode, Logic "1"	2.0		5.5	V
Hold Mode, Logic "0"	0		0.8	V
I_{IH}, V_{IH} = 2.4V			400	μA
I_{IL}, V_{IL} = 0.4V			1000	μA
ANALOG OUTPUT				
Voltage		±10		V
Current		5		mA
Short-Circuit Current		20		mA
Impedance		1		Ω
DC ACCURACY/STABILITY				
Gain		−1.00		V/V
Gain Error		±0.01	±0.02	%
Gain Nonlinearity				
(±10V Output Track)		±0.001		%
Gain Temperature Coefficient		1	5	ppm/°C
Offset Voltage[1]			±3	mV
Output Offset at T_{MIN}, T_{MAX}				
(Track)		±6		mV
TRACK MODE DYNAMICS				
Frequency Response				
Small Signal (−3dB)		1.5		MHz
Full Power Bandwidth		0.5		MHz
Slew Rate		30		V/μs
Noise in Track Mode				
(DC to 1.0MHz)		200		μV rms
TRACK-TO-HOLD SWITCHING				
Aperture Time		30		ns
Aperture Uncertainty (Jitter)		0.4		ns
Offset Step (Pedestal)		±2	±4	mV
Pedestal at Temp				
KM grade		±4		mV
BM grade		±6		mV
Switching Transient				
Amplitude		200		mV
Settling to 1mV		0.5	2	μs
Settling to 0.3mV		1.0	3	μs
HOLD MODE DYNAMICS				
Droop Rate		0.1	1.0	μV/μs
Droop Rate at T_{MAX}			100	μV/μs
Feedthrough Rejection				
(10V p-p, 20kHz)	74	86		dB
HOLD-TO-TRACK DYNAMICS				
Acquisition Time				
To ±0.01% of 20V		1.5	3.0	μs
To ±0.003% of 20V		4.0	6.0	μs
POWER REQUIREMENTS				
Nominal Voltages for Rated				
Performance	±14.5	±15.0	±15.5	V
Operating Range[2]	±11.4		±18.0	V
Power Supply Rejection		100		μV/V
Supply Current: $+V_S$		15	20	mA
$-V_S$		−4	−10	mA
Power Dissipation		300	500	mW
TEMPERATURE RANGE				
Operating: KM grade	0		+70	°C
BM grade	−25		+85	°C
Storage	−55		+125	°C

NOTES: (1) Adjustable to zero with external circuit. (2) Operating to derated performance with $V_{IN} < V_S - 5V$.

ABSOLUTE MAXIMUM RATINGS[1]

Voltage Between $+V_{CC}$ and $-V_{CC}$ Terminals 40V
Input Voltage ..... Actual Supply Voltage
Differential Input Voltage ..... ±24V
Digital Input Voltage ..... −0.5V to +5.5V
Output Current, continuous[2] ..... ±20mA
Internal Power Dissipation 450mW
Storage Temperature Range ..... −65°C < T_A < +150°C
Output Short-Circuit Duration[3] ..... Momentary to Common
Lead Temperature (soldering, 10 seconds) ..... 300°C

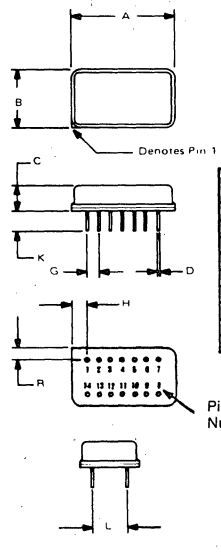
CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

NOTES: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. (2) Internal power dissipation may limit output current to less than +20mA. (3) **WARNING: This device cannot withstand even a momentary short circuit to either supply.**

PIN ASSIGNMENTS

Pin	Description	Pin	Description
1	Digital Input	8	Analog Output
2	No Connection	9	Offset Adjust
3	No Connection	10	No Connection
4	Digital Ground	11	+15V Supply
5	No Connection	12	Summing Junction
6	Analog Ground	13	Analog Input
7	Offset Adjust	14	−15V Supply

MECHANICAL

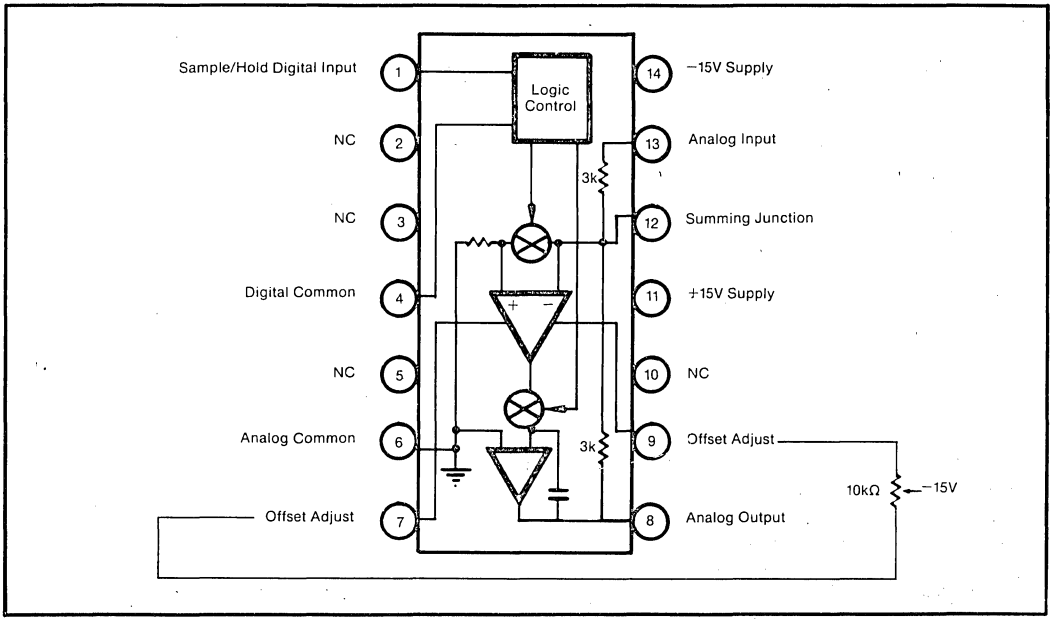


NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	860	880	21 84	22 35
B	490	510	12 45	12 95
C	170	250	4 32	6 35
D	016	021	0 41	0 53
G	100 BASIC		2 54 BASIC	
H	115	155	2 92	3 94
K	150	300	3 81	7 62
L	300 BASIC		7 62 BASIC	
R	080	120	2 03	3 05

Pin numbers shown for reference only. Numbers are not marked on package.

MECHANICAL



DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

Defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by Offset and Gain adjustments.

GAIN ERROR

The difference between the input and output voltage magnitude (in the Sample mode) due to the amplifier gain errors.

DROOP RATE

The voltage decay at the output when in the Hold mode due to storage capacitor and FET switch leakage current and the input bias current of the output amplifier.

FEEDTHROUGH

The amount of output voltage change caused by an input voltage change when the sample/hold is in the Hold mode.

APERTURE DELAY TIME

The time required to switch from Sample to Hold. The time is measured from the 50% point of the Hold mode control transisition to the time at which the output stops tracking the input.

APERTURE UNCERTAINTY TIME

The nonrepeatibility of aperture delay time.

ACQUISITION TIME

The time required for the sample/hold output to settle within a given error band of its final value when the sample/hold is switched from Hold to Sample.

CHARGE OFFSET (PEDESTAL)

The output voltage change that results from charge coupled into the Hold capacitor through the gate capacitance of the switching field effect transistor. This charge appears as an offset at the output.

SAMPLE-TO-HOLD SWITCHING TRANSIENT

The switching transient which appears on the output when the sample/hold is switched from Sample to Hold. Both the magnitude and the settling time of the transient are specified.

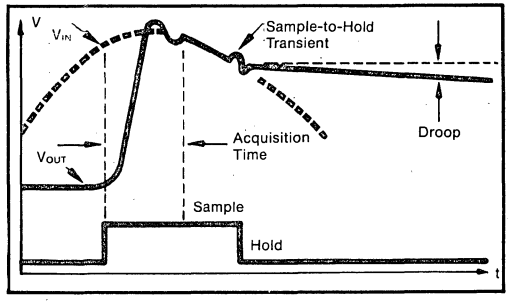


FIGURE 1. Definition of Acquisition Time, Droop and Sample-to-Hold Transient.

SAMPLED DATA ACQUISITION SYSTEM CALCULATIONS

The rated accuracy of an A/D converter in combination with the aperture uncertainty of a sample/hold determine the maximum theoretical input slew rate (frequency) of a given sampled data system.

Sine Wave $f_{MAX} = (2^{-N}\ FSR) \div (2\ \pi\ A\ t)$

A = max Input Signal Amplitude (peak-to-peak)
FSR = Full-Scale Range of A/D Converter
t = Aperture Uncertainty of S/H (jitter)
N = Number of Bits Accuracy

Given below are the maximum input frequencies of two A/D converters in conjunction with the SHC76:

SHC76 **13-bit** Sine Wave f_{MAX} =

$(0.000122 \times 20V) \div (2 \times \pi \times 20V \times 0.4ns)$

= 48.6kHz

SHC76 **14-bit** Sine Wave f_{MAX} =

$(0.000061 \times 20V) \div (2 \times \pi \times 20V \times 0.4ns)$

= 24.3kHz

The maximum throughput rate is determined by adding all critical conversion process times together. Throughput rate cannot exceed the maximum input frequency determined by the accuracy and jitter specs without degrading system performance. Two samples per period of a sine wave are required to satisfy the Nyquist sampling theorem. A low-pass filter is required to cut off frequencies higher than the maximum throughput frequency to prevent aliasing errors from occurring.

Throughput f_{MAX} (2 samples) =

1 ÷ [2 (S/H acquisition time + S/H settling time + A/D conversion time)]

Table I is a listing of various A/D throughput rates using the SHC76 S/H amplifier (assuming two samples per period).

TABLE I. A/D Converter Throughput Rates.

Converter	Accuracy (Bits)	Conversion Speed (μs)	Resolution (Bits)	Throughput f_{MAX} (kHz)
ADC76KG	14	17	16	19.2
	14	16	15	20.0
	14	15	14	20.8
ADC76JG	13	17	16	23.8
	13	16	15	25.0
	13	15	14	26.3
ADC71KG	14	57	16	7.58
	14	54	15	7.94
	14	50	14	8.47
ADC71JG	13	57	16	8.20
	13	54	15	8.62
	13	50	14	9.26

APPLICATIONS

Figures 2 and 3 show the SHC76 in combination with an ADC76 and ADC71 to provide 14-bit accurate A/D conversion systems.

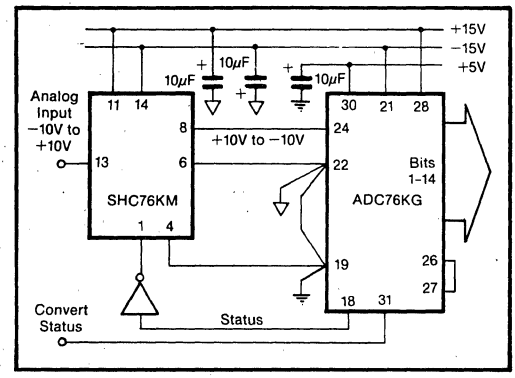


FIGURE 2. A 20kHz A/D Conversion System (14-bit accurate).

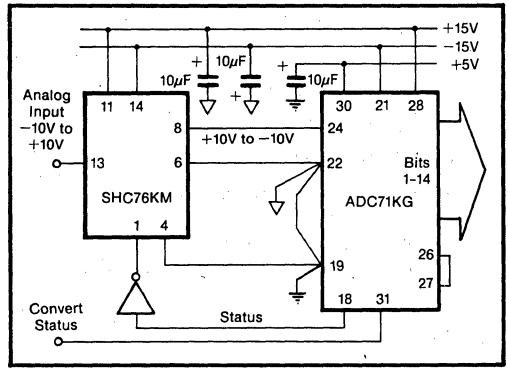


FIGURE 3. An 8.47kHz A/D Conversion System (14-bit accurate).

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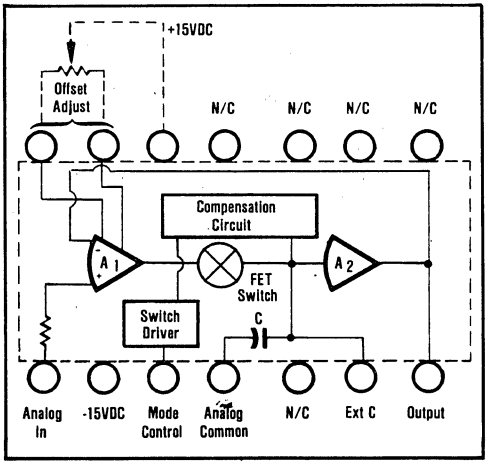
BURR-BROWN®

SHC85
SHC85ET

Fast IC
SAMPLE/HOLD AMPLIFIERS

FEATURES

- 14-PIN DIP PACKAGE
- 5μsec ACQUISITION TIME
- COMPLETE WITH HOLDING CAPACITOR
- ±0.01% ACCURACY
- −55°C TO +125°C TEMPERATURE RANGE (SHC85ET)



DESCRIPTION

The SHC85 is designed to acquire and hold up to ±10VDC analog signals to an accuracy of ±0.01% of full scale range in 5μsec for a 20-volt step or 4.5μsec for a 10VDC step. Featuring internally compensated circuits normally found only in more expensive and larger sample/holds, the SHC85 offers ultra-liner performance and fast acquisition speeds for the most demanding data acquisition and control applications.

Two models are available: the SHC85 is specified for 0°C to 70°C operation, and the SHC85ET is specified for -55°C to +125°C operation.

The SHC85/SHC85ET are well suited for use in:

Data Acquisition Systems
Data Distribution Systems
Analog Delay Circuits
Pulse Amplitude Modulation Circuits
Waveform Amplitude Measurement

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SPECIFICATIONS

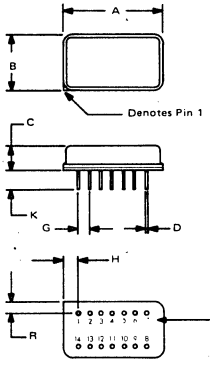
Typical at 25°C with rated supply and a 1000pF internal capacitor unless otherwise noted.

ELECTRICAL

MODELS	SHC85	SCH85ET	UNITS
INPUT			
ANALOG INPUT			
Voltage Range	±10	±10	V
Maximum Safe Input Signal	±15	±15	V
Resistance	10^8	10^8	Ω
Bias Current	50	50	nA
DIGITAL INPUT (TTL Compatible)			
Mode Control	Voltage	Current	
"Sample" - Logic "1"	+2.0V < e < +8V	50nA	
"Hold" - Logic "0"	0V < e < +0.8V	-50μA	
TRANSFER CHARACTERISTICS			
ACCURACY (25°C)			
Dynamic Nonlinearity, max	±0.01	±0.01	% of 20V
At min. "Hold" Time	1000	1000	μsec
Gain	+1.0	+1.0	V/V
Gain Error	±0.01	±0.01	% of 20V
Throughput Offset, max (adjust to zero)	2	2	mV
Droop Rate, max	0.5	0.5	mV/msec
Droop Rate, typical	0.125	0.125	mV/msec
Throughput Nonlinearity	±0.005	±0.005	% of 20V
Noise, rms (10Hz to 100kHz	100	100	μV
Supply Rejection (0 to 50kHz)	100	100	μV/V
ACCURACY DRIFT			
Gain Drift	±2	±2	ppm of 20V/°C
Offset Drift	±25	±25	μV/°C
Droop Rate			
At 70°C, max	10	10	mV/msec
At +125°C, max	--	200	mV/msec
DYNAMIC CHARACTERISTICS			
Bandwidth (Full Power (1))	200	200	kHz
Output Slew Rate	20	20	V/μsec
Aperture Time	30	30	nsec
Acquisition Time (to ±0.01%			
10V Step, max	4.5	4.5	μsec
20V Step, max	5.0	5.0	μsec
Feedthrough in Hold Mode	±0.005	±0.005	% of step change
Charge Offset, max, at 0V Input	±2	±2	mV
Sample-to-Hold Transient			
Peak Amplitude	50	50	mV
Settling to 1mV	0.5	0.5	μsec
OUTPUT			
ANALOG OUTPUT			
Voltage Range	±10	±10	V
Current Range	±10	±10	mA
Impedance	0.1	0.1	Ω
TEMPERATURE			
Specification	0 to +70	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C
POWER SUPPLY			
Rated Voltage	±15	±15	VDC
Range	±14.5 to ±15.5	±14.5 to ±15.5	VDC
Current	±13	±13	mA

NOTE:
1. Small signal bandwidth is 3MHz.

MECHANICAL



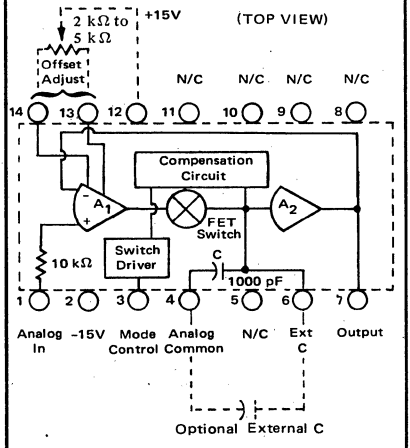
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

Case: Kovar
Pin material and plating composition conform to method 2003 solderability of MIL-STD-883 except paragraph 3.2. Mating Connector: 0145MC

CONNECTION DIAGRAM



NOTE: Pins 5, 8, 9, 10 and 11 are not internally connected.

DEFINITION OF SPECIFICATIONS

DYNAMIC NONLINEARITY
This is the total nonadjustable input to output error. This specification includes throughput nonlinearity and errors due to droop, thermal transients and feedthrough, in short, all errors that cannot be adjusted to zero for a 10V input change after a 5μsec acquisition time and a 1msec hold time. Offset errors must be adjusted to zero by the offset control and gain errors must be adjusted to zero by a gain adjustment elsewhere in the system (gain adjust not included in SHC85).

GAIN ACCURACY
The difference due to amplifier gain errors between Input and Output voltage when in the "sample" mode.

DROOP RATE
The voltage decay at the output when in the "hold" mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH
The amount of the input voltage change that appears at the output when the amplifier is in the "hold" mode (see Figure 1).

THROUGHPUT - NONLINEARITY
The total charge offset and gain nonlinearity. That is, the inaccuracy due to these two errors that cannot be corrected by gain and offset adjustments. Throughput - nonlinearity is specified over the 20V input range.

THROUGHPUT OFFSET
The sum of sample offset and charge offset.

CHARGE OFFSET
The offset that results from charge transferred from the holding capacitor to the gate capacitance of the switching FET. This charge is partially restored by a special compensation circuit when the unit goes into the "hold" mode.

ACQUISITION TIME
The time required for the output to settle to its final value within a given error band, when the Mode control is switched from "hold" to "sample" (see Figure 2).

APERTURE TIME
The time required to switch from "sample" to "hold". The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

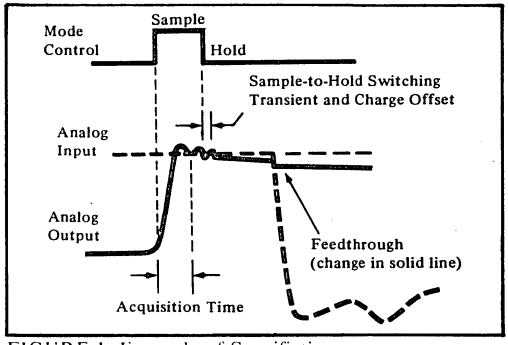


FIGURE 1. Example of Specifictions.

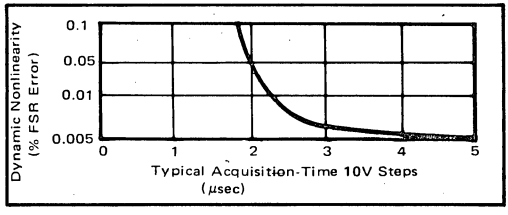


FIGURE 2. Acquisition Time vs Full Scale Range Error.

OPERATING INSTRUCTIONS

OPTIONAL EXTERNAL CAPACITOR SELECTION
The value of the external capacitor determines the droop, charge offset and acquisiiton time of the sample/hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table.

Figure 3 shows the behavior of acquisition time with added external capacitance. The behavior of droop with external C is determined by:

$$\text{Droop} = dv/dt = (0.5 \times 10^{-9})/(1000\text{pF} + C_{ext})$$

Capacitors with high insulation resistance and low dielectric absorption, such as teflon or polystyrene should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor; this will minimize droop errors.

OFFSET ADJUSTMENT
Connect a 2kΩ to 5kΩ multiturn potentiometer with a TCR of 150ppm °C or less as shown in the Connection Diagram. The offset should be adjusted with the input grounded. During the adjustment, the sample hold should be switching continuously between the "sample" and the "hold" mode. The error should then be adjusted to zero where the unit is in the "hold" mode. In this way, charge offset as well as amplifier offset will be adjusted.

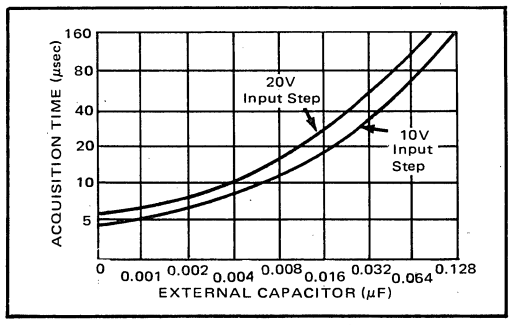
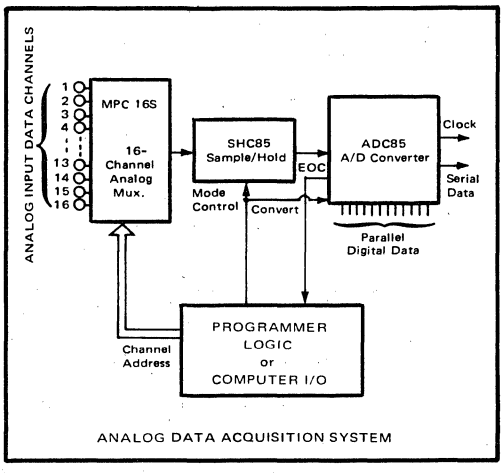


FIGURE 3. Acquisition Time vs External Capacitor.

APPLICATIONS

DATA ACQUISITION SYSTEM

The SHC85 makes an excellent device for reducing aperture time in a data acquisition system. When combined with Burr-Brown's 16-channel MPC-16S Analog Multiplexer and ADC85 10- or 12-bit A D Converter, you can have a compact 16-channel data acquisition system with 50kHz to 65kHz throughput sampling rates and 0.02 percent (RSS) system accuracy.



ANALOG DATA ACQUISITION SYSTEM

SIMULTANEOUS SAMPLE/HOLD

Time correlation of sampled data signals may be implemented by using one sample/hold for each analog signal prior to input to an analog multiplexer. The SCH85 low aperture time of 30nsec practically eliminated channel-to-channel time slew. The throughput sampling rate and the number of data channels will determine the maximum Hold time and hence, the worst-case droop error of the sample/hold in the last channel to be sampled prior to the next "refresh" or sample hold command. This droop error may be minimized by adding external capacitance to the SHC85 as shown in Figure 3.

The droop error is computed by:

MAX DROOP ERROR (CHANNEL N)=(T x n) (Droop rate)

Where T = 1 System Sampling Rate and n = number of multiplexer data channels.

EXAMPLE:

For a 10-bit, 32-channel system with throughput sample rate of 50kHz, assuming no external capacitance, the droop error of channel N is:

Droop Error (E_D) = [(1 50kΩ) x 32] [(500 x 10^{-1})] = 320μV.

For $\pm$10V input signal range and 10-bit resolution, the resolution of $\pm$1 2LSB is $\pm$9.77mV. This droop error is less than 0.016LSB (negligible), and no external C need be added to reduce the droop of the SHC85.

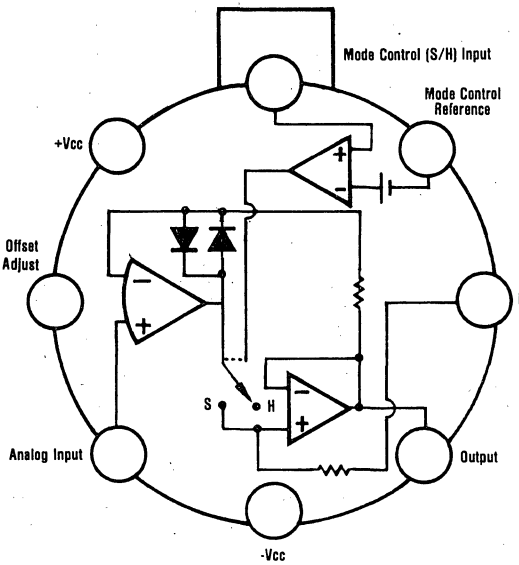
BURR-BROWN®

SHC298AM

Low Cost Monolithic SAMPLE/HOLD AMPLIFIER

FEATURES

- 12-BIT THROUGHPUT ACCURACY
- LESS THAN 10μsec ACQUISITION TIME
- WIDEBAND NOISE LESS THAN 20μV, rms
- RELIABLE MONOLITHIC CONSTRUCTION
- $10^{10}\Omega$ INPUT RESISTANCE
- TTL/CMOS-COMPATIBLE LOGIC INPUT



DESCRIPTION

The SHC298AM is a high performance monolithic sample/hold circuit which features very-high DC accuracy with fast acquisition times and a low droop rate. With the addition of one external holding capacitor, 12-bit accuracy can be achieved with a 6μsec acquisition time. Droop rates less than 5mV/min can be achieved with a 1μF holding capacitor.

The fully differential logic inputs have low input current, and are compatible with TTL, PMOS, and CMOS logic families. The input offset adjustment can be made using a single external potentiometer and resistor, and the adjustment does not degrade input offset drift.

The SHC298AM will operate with power supplies ranging from ±5VDC to ±18VDC. It is available in a hermetically sealed 8-lead low profile package, and is specified for a temperature range from -25°C to +85°C. The SHC298AM is the best price/performance bargain in its class. It is well suited for use in data acquisition systems, data distribution systems, analog delay circuits, and pulse amplitude modulation circuits.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

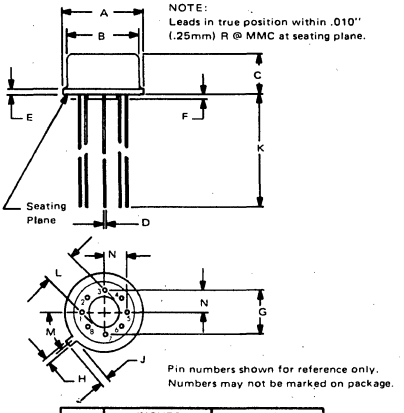
Specifications at $T_J = +25°C$, ±15V supplies, 1000pF holding capacitor, $-11.5V \leq V_{IN} \leq +11.5$, $R_L = 10k\Omega$, Logic Reference Voltage = 0V, and Logic Voltage = 2.5V unless otherwise noted.

	SHC298AM			
MODEL	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
ANALOG INPUT				
Resistance		10^{10}		Ω
Bias Current (1)		10	50	nA
DIGITAL INPUT	Pin 7	Pin 8	Circuit State	
Mode Control Truth Table	0V	+2.4V	Sample (Track)	
	0V	+0.8V	Hold	
	+2.4V	+2.8V	Hold	
	+0.8V	+2.8V	Sample (Track)	
Mode Control and Mode Control Reference Input Current			10	μA
Differential Logic Threshold	0.8	1.4	2.4	V
TRANSFER CHARACTERISTICS				
ACCURACY (+25°C)				
Throughput Nonlinearity for Hold Time < 1msec		±0.010	±0.015	% of 20V
Gain		+1.0		V/V
Gain Error		±0.004	±0.010	%
Input Voltage Offset (adjust to zero) (1)		±2	±7	mV
Droop Rate (1)		±30	±200	μV/msec
Charge Offset (2)		±15	±25	mV
Noise (rms) 10Hz to 100kHz		10	20	μV
Power Supply Rejection		±25	±100	μV/V
ACCURACY DRIFT				
Gain Drift		3	4	ppm/°C
Input Offset Drift		15	70	μV/°C
Charge Offset Drift C = 1000pF		50	150	μV/°C
Charge Offset Drift C = 10,000pF		20	50	μV/°C
Droop Rate at $T_J = +85°C$		1	10	mV/msec
DYNAMIC CHARACTERISTICS				
Full Power Bandwidth, C = 1000pF	75	125		kHz
Full Power Bandwidth, C = 10,000pF	10	16		kHz
Output Slew Rate, C = 1000pF	7	10		V/μsec
Output Slew Rate, C = 10,000pF	1.4	2		V/μsec
Aperture Time				
Negative Input Step		125	200	nsec
Positive Input Step		30	45	nsec
Acquisition Time (C = 1000pF)				
to ±0.01%, 10V step		6	10	μsec
to ±0.01%, 20V step		8	12	μsec
to ±0.1%, 10V step		5	9	μsec
to ±0.1%, 20V step		7	11	μsec
Sample/Hold Transient				
Peak Amplitude		160		mV
Settling to 1mV		1.0	1.5	μsec
Feedthrough (Response to 10V Input Step)		±0.007	±0.015	% of 20V
OUTPUT				
ANALOG OUTPUT				
Voltage Range	±11.5			V
Current Range	±2			mA
Impedance (In hold mode)		0.5	4	Ω
POWER SUPPLY				
Rated Voltage		±15		VDC
Range	±5.0		±18	VDC
Current (1)		±4.5	±6.5	mA

NOTES:

1. These parameters guaranteed over a supply voltage range of ±5V to = ±18V.
2. Charge offset is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the charge offset is inversely proportional to hold capacitor value.

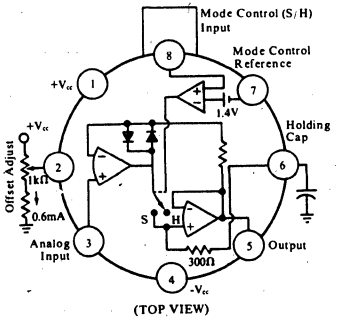
MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	---	12.7	---
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin Material and Plating Composition: Conforms to MIL-STD-883 method 2003 (solderability).
Hermeticity: Conforms to MIL-STD-883, method 1014, condition C, step 1, Fluorocarbon (gross leak) and method 1014, condition A, Helium, 5 x 10^{-8}cc/sec (fine leak).
Connector: None.

PIN CONFIGURATION



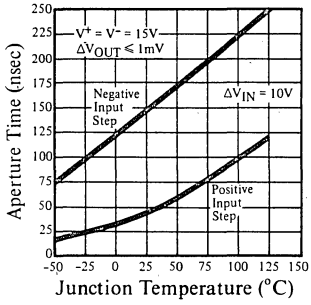
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Power Dissipation (Package Limitation) (Note 1) 500mW
Operating Temperature Range ..... -25°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Input Voltage ..... Equal to Supply Voltage
Logic-to-Logic Reference Differential Voltage (Note2) ..... +7V, -30V
Output Short Circuit Duration ..... Indefinite
Hold Capacitor Short Circuit Duration 10sec
Lead Temperature (soldering, 10 seconds) ..... 300°C

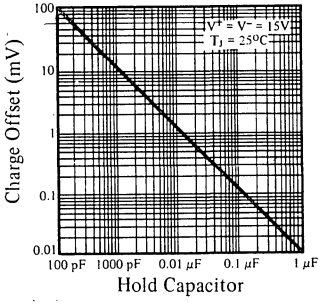
NOTES:
1. The maximum junction temperature is +100°C, when operating at elevated ambient temperature, the power dissipation must be derated based on a thermal resistance (θ_{JA}) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

TYPICAL PERFORMANCE CURVES

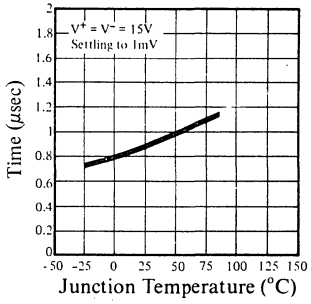
APERTURE TIME



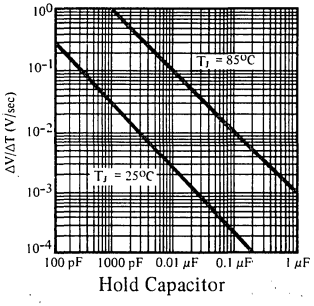
CHARGE OFFSET



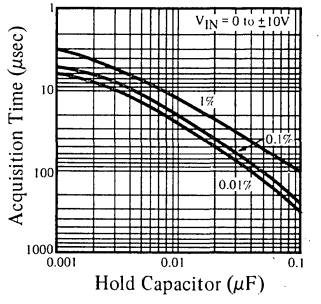
SAMPLE/HOLD TRANSIENT SETTLING TIME



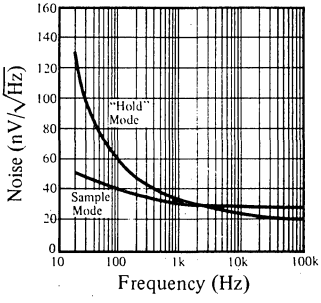
OUTPUT DROOP RATE



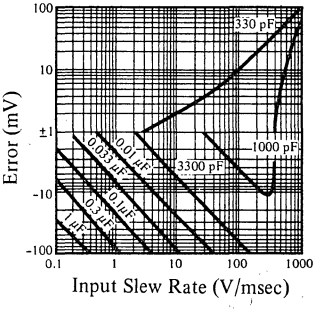
ACQUISITION TIME



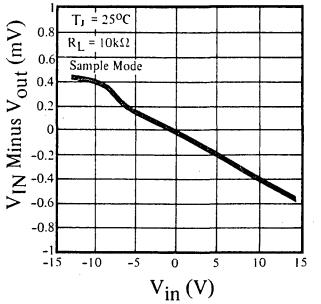
OUTPUT NOISE



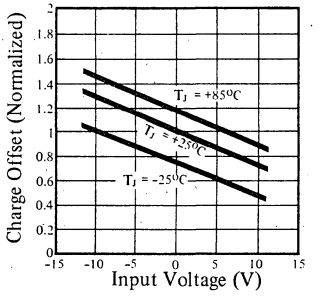
DYNAMIC SAMPLING ERROR



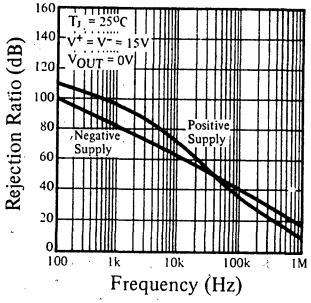
GAIN ERROR



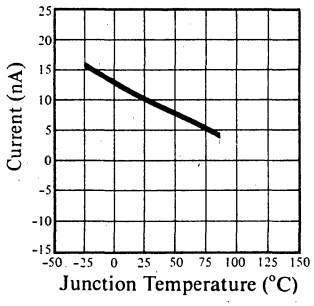
CHARGE OFFSET



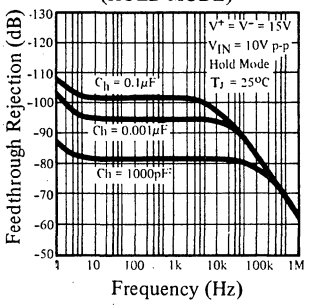
POWER SUPPLY REJECTION



INPUT BIAS CURRENT



FEEDTHROUGH REJECTION (HOLD MODE)



DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

Throughput nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, 1msec of droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by offset and gain adjustments. Throughput nonlinearity is tested with a 1000pF holding capacitor, 10V input changes, 10μsec acquisition time, and 1msec Hold time (see Figure 1).

GAIN ACCURACY

Gain Accuracy is the difference between Input and Output voltage (when in the Sample mode) due to amplifier gain errors.

DROOP RATE

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

Feedthrough is the amount of the input voltage change that appears at the output when the amplifier is in the Hold mode.

APERTURE TIME

Aperture Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

ACQUISITION TIME

Acquisition Time is the time required for the sample/hold output to settle within a given error band of its final value when the mode control is switched from Hold to Sample.

CHARGE OFFSET

Charge Offset is the offset that results from the charge coupled through the gate capacitance of the switching FET. This charge is coupled into the storage capacitor when the FET is switched to the "hold" mode.

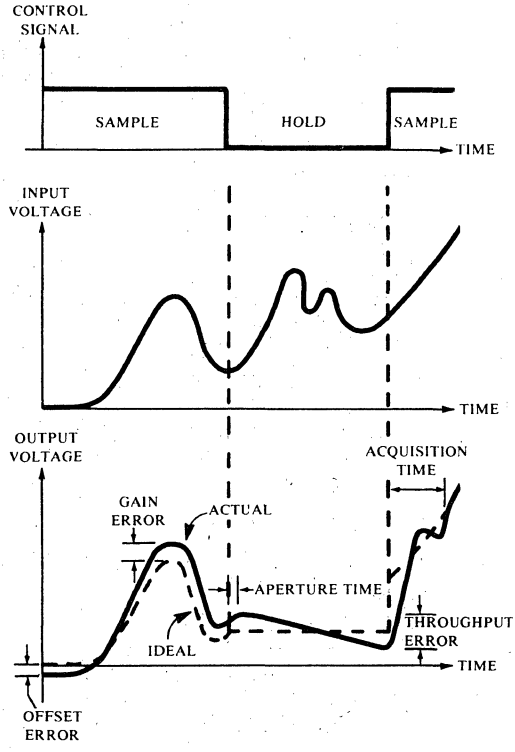


FIGURE 1. Sample/Hold Errors.

OPERATING INSTRUCTIONS

EXTERNAL CAPACITOR SELECTION

Capacitors with high insulation resistance and low dielectric absorption, such as teflon, polystyrene or polypropylene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize AC and DC leakage currents from the capacitor to reduce chage offset and droop errors.

The value of the external capacitor determines the droop, charge offset and acquisition time of the Sample/Hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table for a 0.001μF capacitor. With a capacitor of 0.01μF the droop will reduce to approximately 2.5μV/msec and the charge offset to approximately 1.5mV. The behavior of acquisition time with changes in external capacitance is shown in Typical Performance Curves.

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold mode. The error should then be adjusted to zero when the unit is in the Hold mode. In this way, charge offset as well as amplifier offset will be adjusted. When a 0.001μF capacitor is used, it will not be possible to adjust the full offset error at the sample/hold. It should be adjusted elsewhere in the system.

APPLICATIONS

DATA ACQUISITION

The SHC298AM may be used to hold data for conversion with an analog-to-digital converter or used to provide Pulse Amplitude Modulation (PAM) data output (see Figures 2 and 3).

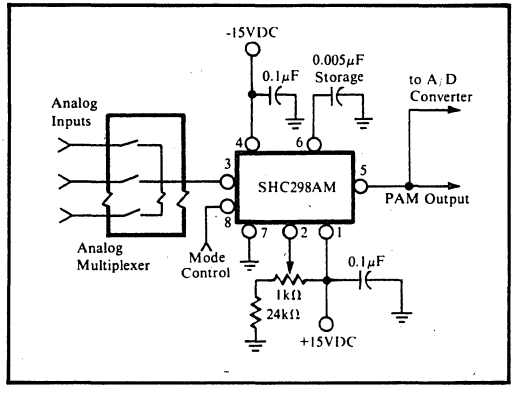


FIGURE 2. Data Acquisition.

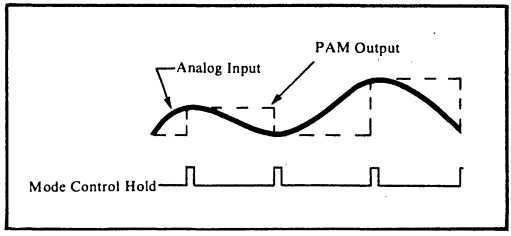


FIGURE 3. PAM Output.

DATA DISTRIBUTION

The SHC298AM may be used to hold the output of a digital-to-analog converter whose digital inputs are multiplexed (see Figure 4).

TEST SYSTEMS

The SHC298AM is also well suited for use in test systems to acquire and hold data transients for human operators or for other parts of the test system such as comparators, digital voltmeters, etc.

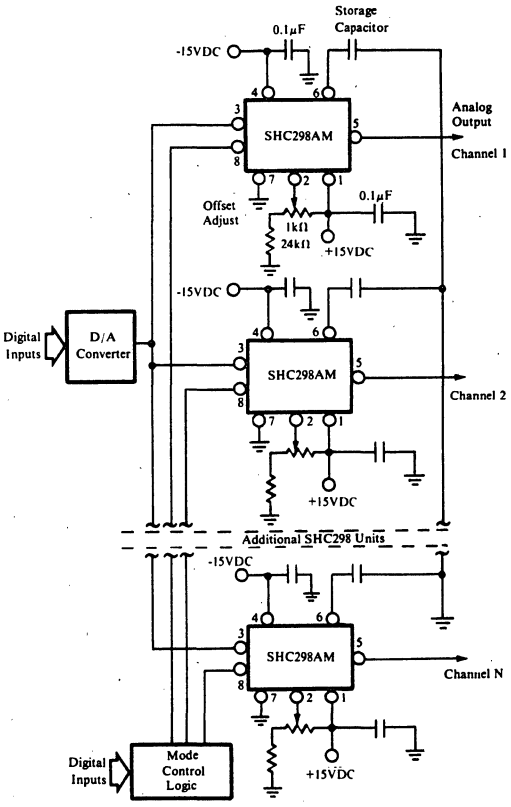


FIGURE 4. Data Distribution.

With a 0.1μF storage capacitor, the output may be held 10sec with less than 0.1% error. With a 1μF storage capacitor, the output may be held more than 15 minutes with less than 1% error.

CAPACITIVE LOADING

SHC298 is sensitive to capacitive loading on the output and may oscillate. When driving long lines, a buffer should be used.

HIGH SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the analog-to-digital converter. If two or more sample/holds are used with a high speed multiplexer, the acquisition time of the sample/hold can be virtually eliminated. While the first channel is in hold and switched on to the ADC, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this data by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed (see Figure 5). For low level systems, an instrumentation amplifier and double-ended multiplexer may be connected to the sample/hold inputs. The settling time of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the channel conversion time as before.

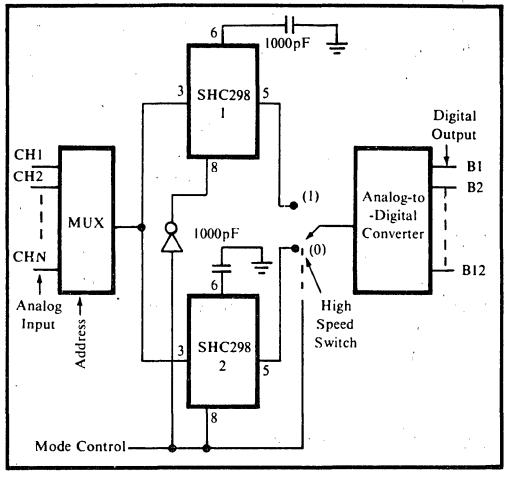


FIGURE 5. "Ping-Pong" Sample/Holds.

BURR-BROWN®

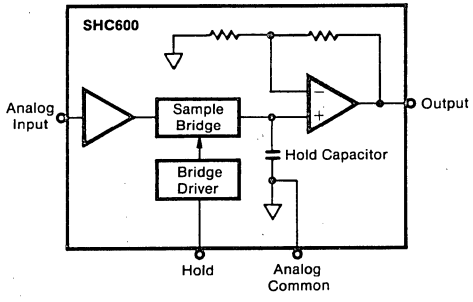
SHC600BH

ADVANCE INFORMATION
Subject to Change

Ultra-High Speed SAMPLE/HOLD AMPLIFIER

FEATURES

- CLOSED-LOOP OUTPUT AMPLIFIER
- ±0.01% FSR LINEARITY max
- ACQUISITION TIME (2.5V STEP):
  1% FSR 17ns typ
  0.1% FSR 27ns typ
  0.02% FSR 40ns typ
- 300V/μs SLEW RATE
- 24-PIN DIP



DESCRIPTION

The SHC600 is a high speed sample/hold amplifier designed for use in ultra-fast, 12-bit data acquisition and signal processing systems. It acquires input step changes of 2.5V to 1% accuracy in 17ns and 0.02% accuracy in 40ns, typically. The closed-loop output amplifier provides a maximum linearity error of ±0.01% with a low output impedance of 0.4Ω. The gain has been optimized to drive 100Ω loads with a gain error of less than ±0.1%.

In the sample mode the SHC600 operates as a unity-gain buffer with a minimum small signal bandwidth of 70MHz. Input voltage range is ±2V.

The hold command is ECL-compatible. Power supply requirements are ±15V, +5V, and −5.2V and the specification temperature range is −25°C to +85°C.

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SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies and 100Ω in parallel with 3pF load unless otherwise specified.

PARAMETER	SHC600BH MIN	SHC600BH TYP	SHC600BH MAX	UNITS
SAMPLE/HOLD INPUTS				
ANALOG				
Voltage Range[1]		±1.25	±2	V
R_{IN}		1.5		MΩ
Input Bias Current		20	35	μA
DIGITAL (ECL Compatible)				
V_{IH} (HOLD)	−1.1		−0.8	V
V_{IL} (SAMPLE)	−1.8		−1.5	V
I_{IH}, V_{IN} = −1.1V			265	μA
I_{IL}, V_{IN} = −1.8V	0.5			μA
SAMPLE/HOLD OUTPUT				
Voltage Range		±1.25	±2	V
Output Current	±40			mA
Short Circuit Protection		Momentary (1 sec.)		
Output Impedance (at DC)		0.4		Ω
Noise in Track Mode (wideband 200MHz into 50Ω load)		400		μV rms
SAMPLE/HOLD TRANSFER CHARACTERISTICS				
DC ACCURACY/STABILITY				
Gain		+1		V/V
Gain Error		±0.1		%
Temperature Coefficient		±5	±20	ppm/°C
Linearity Error (±1.25V Input)		±0.002	±0.01	% of FSR[2]
Zero Offset		±2	±5	mV
Temperature Coefficient		±50	±150	μV/°C
Power Supply Sensitivity of Offset: V_{DD1} (+5V)		±1	±3	mV/V
V_{DD2} (−5.2V)		±4	±13	mV/V
$+V_{CC}$ (+15V)		±5	±10	mV/V
$-V_{CC}$ (−15V)		±9	±15	mV/V
HOLD-TO-TRACK (SAMPLE) DYNAMICS				
Acquisition Time (with 2.5V step)[2]: To within ±1% of FSR (25mV)		17	25	ns
To within ±0.1% of FSR (2.5mV)		27	35	ns
To within ±0.02% of FSR (0.5mV)		40	50	ns
Switch Delay Time		2		ns
TRACK (SAMPLE)-TO-HOLD DYNAMICS				
Aperture Delay Time[3]		4	8	ns
Aperture Uncertainty (jitter)		5	9	ps (rms)
Offset Step (pedestal)		±2	±10	mV
Temperature Coefficient		±30	±60	μV/°C
Sensitivity to V_{DD2} (−5.2V)		±2.5	±10	mV/V
Switch Delay Time		2		ns
SwitchingTransient: Amplitude		7	20	mV_{PEAK}
Settling to within ±1mV		10	15	ns
TRACK (SAMPLE) MODE DYNAMICS				
Frequency Response: Full Power Bandwidth		40		MHz
Small Signal Bandwidth		70		MHz
Output Slew Rate		300	200	V/μs
Harmonic Distortion (2.5V p-p input at 4MHz): R_L = 200Ω			−68	dB
R_L = 50Ω			−60	dB
HOLD MODE DYNAMICS				
Droop Rate: at +25°C		±60	±180	μV/μs
at +85°C		±1.5	±4	mV/μs
Feedthrough Rejection: 2.5V p-p input at 1MHz	62			dB
at 10MHz	58			dB
POWER SUPPLY REQUIREMENTS				
Quiescent Current: V_{DD1} (+5.0V, ±0.25V)		40	55	mA
V_{DD2} (−5.2V, ±0.25V)		−93	−120	mA
$+V_{CC}$ (+15V, ±0.5V)		30	45	mA
$-V_{CC}$ (−15V, ±0.5V)		−15	−25	mA
Power Dissipation		1.3	2.0	W
TEMPERATURE RANGE				
Specification (case temperature)	−25		+85	°C
Storage	−55		+125	°C

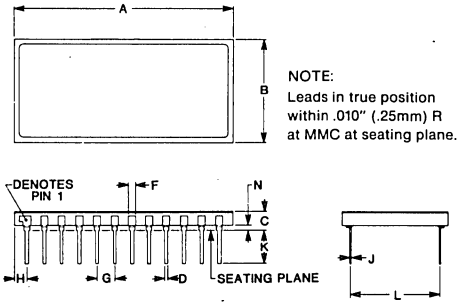
NOTES: (1) Maximum input without damage, ±5V. (2) FSR means Full-Scale Range. For SHC600 FSR= 2.5V. (3) Measurements are made with R_L = 100Ω and C_L = 3pF.

PIN ASSIGNMENTS

1	V_{DD1} (+5V, ±5%)	13	Analog Input
2	V_{DD2} (−5.2V, ±5%)	14	NIC*
3	NIC*	15	NIC*
4	V_{DD2} (−5.2V, ±5%)	16	NIC*
5	Hold Command	17	NIC*
6	Digital Common	18	Analog Common
7	Power Common	19	Analog Common
8	$+V_{CC}$ (+15V)	20	NIC*
9	NIC*	21	NIC*
10	V_{DD2} (−5.2V)	22	$+V_{CC}$ (+15V)
11	Power Common	23	NIC*
12	$-V_{CC}$ (−15V)	24	Analog Output

* NIC = No Internal Connection

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.280	1.310	32.51	33.27
B	.780	.800	19.81	20.32
C	.153	.207	3.89	5.26
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.007	.091	2.21	2.31
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.600 BASIC		15.24 BASIC	
N	.015	.035	.38	.89

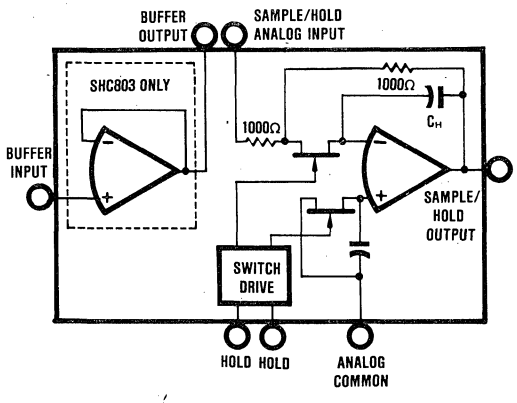
BURR-BROWN®

SHC803BM, CM
SHC804BM, CM

Ultra-High Speed SAMPLE/HOLD AMPLIFIER

FEATURES

- 350nsec max ACQUISITION TIME
- ±0.01% THROUGHPUT NONLINEARITY
- 150nsec max SAMPLE-TO-HOLD SETTLING TIME
- INPUT BUFFER (SHC803)
- 24-PIN HERMETICALLY-SEALED METAL PACKAGE



DESCRIPTION

The SHC803 and SHC804 are high speed sample/hold amplifiers designed for use in fast 12-bit data acquisition systems and signal processing systems. The SHC803 contains a fast-settling unity-gain amplifier for buffering high impedance sources or for use with CMOS multiplexers.

The SHC804 acquires a 10V signal change in less than 350nsec to ±1/2LSB at 12 bits. Throughput nonlinearity error is guaranteed to be within ±1/2LSB for 12-bit systems. Stability over temperature is excellent, with only ±5ppm/°C of gain drift and ±4ppm of FSR/°C of charge offset drift over the −25 to +85°C temperature range.

The ±25psec maximum aperture uncertainty of SHC803 and SHC804 permits sampling (to ±0.01% of Full Scale Range) of signals with rates of change of up to 100V/μsec. These sample/holds have been optimized for use with Burr-Brown's high speed 12-bit analog-to-digital converter, model ADC803. Together these components are capable of accurately digitizing fast changing signals at sample rates as high as 500k samples per second.

The digital inputs (HOLD and $\overline{\text{HOLD}}$) are TTL-compatible. Power supply requirements are ±15V and +5V and the specification temperature range is −25°C to +85°C. The SHC803 and SHC804 are packaged in a 24-pin dual-in-line hermetic metal package. SHC804 is pin-compatible with other sample/holds on the market with similar performance characteristics.

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PDS-512C

SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies and a 1kΩ output load unless otherwise specified.

MODEL	SHC803/SHC804BM			SHC803/804CM			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
SAMPLE/HOLD INPUTS [without input buffer]							
ANALOG							
Voltage Range	±10.25	±11		•	•		V
R_{IN}		1.00			•		kΩ
DIGITAL [HOLD, $\overline{HOLD}$]							
V_{IH}	+2.0			•			V
V_{IL}			+0.8			•	V
I_{IH}, V_{IN} = +2.7V			+60			•	µA
I_{IL}, V_{IN} = +0.4V			−1.2			•	mA
SAMPLE/HOLD TRANSFER CHARACTERISTICS [without input buffer]							
ACCURACY							
Sample Mode							
Gain		−1			•		V/V
Gain Error			±0.1			•	%
Temperature Coefficient		±3	±10		±1	±5	ppm/°C
Linearity Error		±0.001	±0.005		•	•	% of FSR[1]
Zero Offset		±1	±5		±0.5	±3	mV
Temperature Coefficient		±1	±2.5		±0.5	±1.5	ppm of FSR/°C
Hold Mode							
Charge Offset		±2	±10		±1	±5	mV
Temperature Coefficient		±3	±10		±2	±4	ppm of FSR/°C
Droop Rate: at +25°C		±0.5	±5		•	•	µV/µsec
+85°C			±0.5			±0.1	mV/µsec
Throughput Nonlinearity			±0.01			•	% of FSR
Power Supply Sensitivity[2]: ±V_{CC}			±0.002			•	% of FSR/%V_{CC}
V_{DD}			±0.003			•	% of FSR/%V_{DD}
DYNAMIC CHARACTERISTICS							
Acquisition Time (with 10V step)							
to within: ±0.1% (±10mV)		220			•		nsec
±0.01% (±1mV)		250	350		•	•	nsec
Sample-to-Hold Settling Time							
to within ±0.01% (±1mV)		100	150		•	•	nsec
Sample-to-Hold Transient Amplitude		60	150		•	•	mV_{peak}
Aperture Delay Time[3]		15	25		•	•	nsec
Aperture Uncertainty		±10	±25		•	•	psec
Sample Mode: Output Slew Rate		160			•		V/µsec
Full Power Bandwidth		1			•		MHz
Small Signal Bandwidth		16			•		MHz
Hold Mode Feedthrough Rejection							
(10V square wave input)	±0.03	±0.005		•	•		%
SAMPLE/HOLD OUTPUT							
Voltage Range	±10.25	±11		•	•		V
Output Current	±50			•			mA
Short Circuit Protection		Indefinite to Common			•		
Output Impedance (at DC)		0.01	0.1		•	•	Ω
INPUT BUFFER CHARACTERISTICS [SHC803 only]							
INPUT							
Offset Voltage		±1/2	±5		•	•	mV
vs Temperature		±1.5	±2.5		•	•	ppm of FSR/°C
Bias Current			±25			•	nA
Impedance		10^8‖5			•		Ω‖pF
V_{IN} Range	±10.25	±11		•	•		V
DYNAMIC CHARACTERISTICS							
Full Power Bandwidth		320			•		kHz
Slew Rate[4]		10			•		V/µsec
Settling Time[4] to ±2mV for 10V Step		2.5			•		µsec
OUTPUT							
V_{OUT} Range	±10.25			•			V
Output Current	±10.25			•			mA

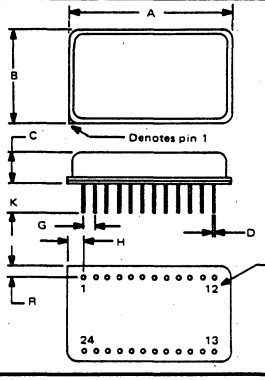
ELECTRICAL [CONT]

MODEL	SHC803/SHC804BM			SHC803/804CM			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY REQUIREMENTS							
Rated Voltage: $\pm V_{CC}$	±13.5	±15	±16.5	*	*	*	V
V_{DD}	+4.75	+5.00	+5.25	*	*	*	V
Quiescent Current (no load)							
SHC804: $+V_{CC}$		30	35		*	*	mA
$-V_{CC}$		15	20		*	*	mA
V_{DD}		5	10		*	*	mA
SHC803: $+V_{CC}$		33	40		*	*	mA
$-V_{CC}$		18	25		*	*	mA
V_{DD}		5	10		*	*	mA
Power Dissipation: SHC804		700	875		*	*	mW
SHC803		790	1100		*	*	mW
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Storage	−55		+125	*		*	°C

*Specification same as SHC803/SHC804BM.

NOTES: (1) FSR means Full Scale Range and is 20V for SHC803 and SHC804. (2) Sensitivity of Offset plus Charge Offset. (3) With respect to $\overline{HOLD}$. For HOLD add 5nsec typical. (4) With buffer connected to the sample/hold amplifier.

MECHANICAL



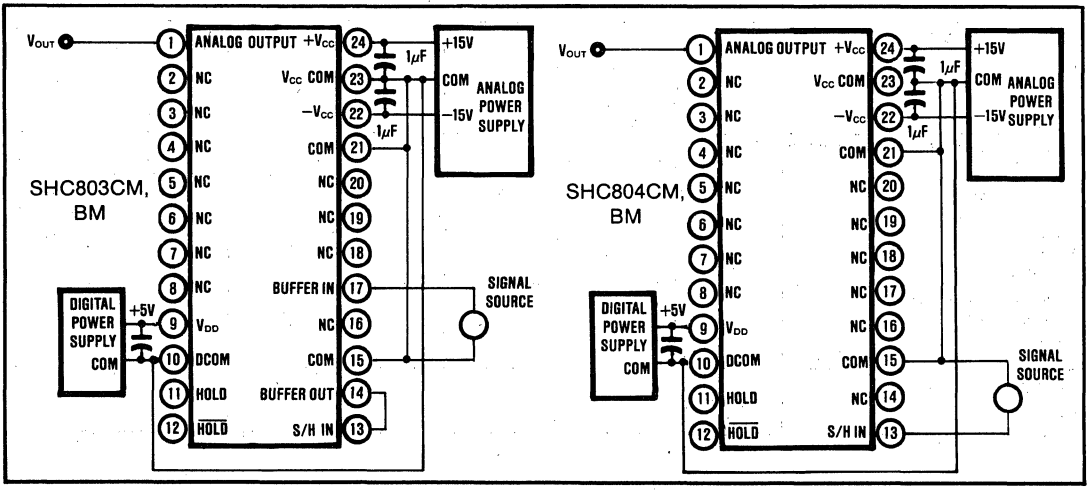
CASE: Nickel-plated steel
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3oz)
HERMETICITY: Conforms to method 1014 Condition C Step 1 (fluorocarbon) of MIL-STD-883 (gross leak)

Pin numbers shown for reference only. Numbers may not be marked on package.

NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Input Overvoltage ..... ±15V
$+V_{CC}$ to V_{CC} COMMON ..... 0 to +18V
$-V_{CC}$ to V_{CC} COMMON ..... 0 to −18V
Voltage on Digital Inputs
(pins 11 and 12) .....−0.5V to +7V
Power Dissipation 1500mW
V_{DD} to DCOM .....−0.5V
Analog Output .... Indefinite Short to V_{CC} COM

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PIN ASSIGNMENTS

Pin	Name	Description
1	Sample/Hold Output	Analog voltage output
2	NC	Not connected
3	NC	Not connected
4	NC	Not connected
5	NC	Not connected
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	V_{DD}	Logic supply
10	DCOM	Logic supply common
11	HOLD	Logic "1" = HOLD
12	$\overline{\text{HOLD}}$	Logic "0" = HOLD
13	S/H In	SHC804 input; for SHC803 connect pin 13 to pin 14
14	Buffer Out, SHC803 only	Not connected for SHC804
15	COM	Signal common
16	NC	Not connected
17	Buffer In, SHC803 only	Not connected for SHC804
18	NC	Not connected
19	NC	Not connected
20	NC	Not connected
21	COM	Signal Common
22	$-V_{CC}$	−15V supply
23	V_{CC} COM	Analog power common, connected to case
24	$+V_{CC}$	+15V supply

DISCUSSION OF SPECIFICATIONS

Throughput Nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by Offset and Gain adjustments.

Gain Error is the difference between the input and output voltage magnitude (in the Sample mode) due to the amplifier gain errors.

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor and FET switch leakage current and the input bias current of the output amplifier.

Feedthrough is the amount of output voltage change caused by an input voltage change when the sample/hold is in the Hold mode.

Aperture Delay Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the Hold mode control transition to the time at which the output stops tracking the input.

Aperture Uncertainty Time is the nonrepeatibility of aperture delay time.

Acquisition Time is the time required for the sample/hold output to settle to within a given error band of its final value when the sample/hold is switched from Hold to Sample.

Charge Offset (Pedestal) is the output voltage change that results from charge coupled into the Hold capacitor through the gate capacitance of the switching field effect transistor. This charge appears as an offset at the output.

Sample-to-Hold Switching Transient is the switching transient which appears on the output when the sample/hold is switched from Sample to Hold. Both the magnitude and the settling time of the transient are specified.

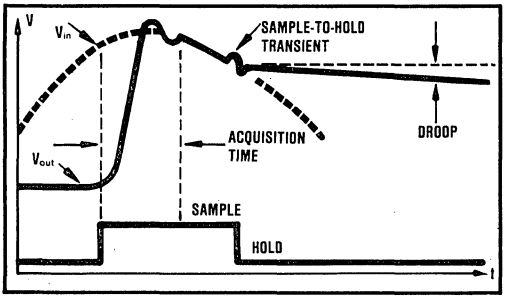


FIGURE 1. Definition of Acquisition Time, Droop and Sample-to-Hold Transient.

OPERATION

A simplified circuit diagram of SHC803/804 is shown on page 1. The SHC803 includes a noninverting unity-gain op amp to serve as a source-impedance buffer when the sample/hold is used with CMOS analog multiplexers. The SHC804 and SHC803 are identical except for this buffer.

In the Sample (track) mode the circuit acts as a unity-gain inverting amplifier. In the Hold mode, the capacitor, C_H, holds the value of the output at the time the unit was switched to the Hold mode. Additional circuits compensate for switching transients and provide switch leakage current cancellation. The amplifier provides high current drive and low output impedance to external loads.

GAIN, OFFSET, CHARGE OFFSET

SHC803 and SHC804 have been internally-trimmed to eliminate the need for external trim potentiometers for Gain, Offset (in Sample mode) and Charge Offset (Pedestal). System Gain and Offset errors can be adjusted elsewhere in the system, at an input amplifier preceding the sample/hold, or at an analog-to-digital converter following the sample/hold.

INSTALLATION

GROUNDING AND BYPASSING

SHC803 and SHC804 have four COMMON pins (pins 10, 15, 21, and 23) and all must be tied together and connected to the system analog common ($V_{CC}COM$) as close to the package as possible. It is preferable to have a large ground plane surrounding the sample/hold and have all four common pins soldered directly to it. Note that the metal case is internally connected to pin 23; therefore, care must be taken to avoid a ground loop if the case is allowed to contact the ground plane.

Most digital return currents pass through pin 10. Noise from the switch-drive circuit may couple directly into the main op amp summing junction, a very noise-sensitive node. Care must be taken to insure that no voltage differences occur between pin 10 and the other common pins. This is the reason pin 10 must be connected directly to the ground plane.

For the same reason, the logic supply should be kept as free of noise as possible. $\pm V_{CC}$ supply lines (pins 24 and 22) are internally bypassed to common with 0.01μF capacitors. It is recommended that the user install additional external 0.1μF to 1μF tantalum bypass capacitors at each supply pin.

SAMPLE/HOLD CONTROL

A TTL logic "0" at pin 11 (or a logic "1" at pin 12) switches the SHC803/804 into the Sample (track) mode. In this mode, the device acts as a unity-gain inverting amplifier, the output following the inverse of the input. A logic "1" at pin 11 (or a logic "0" at pin 12) will switch the SHC803/804 into the Hold mode. The output voltages will be held constant at the value present when the Hold command is given.

If pin 11 is used, pin 12 must be connected to the DCOM (pin 10). If pin 12 is used, pin 11 must be tied to V_{DD}. Using the HOLD and $\overline{\text{HOLD}}$ inputs as a logic function may adversely affect the charge offset (pedestal). A clean digital signal (no overshoot) at the HOLD or $\overline{\text{HOLD}}$ inputs will also reduce charge offset errors. Pins 11 and 12 present less than one standard TTL load (two LSTTL loads) to the digital drive circuit.

OUTPUT LOADING

Care must be taken when loading the output of the SHC803/804 to avoid possible oscillations, current limiting and performance variations over temperature.

The maximum capacitive load to avoid oscillations is about 300pF. Recommended resistive load is 500Ω or more, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω in parallel with capacitive loads up to 100pF. Higher capacitances will affect acquisition and settling times.

ANALOG SIGNAL SOURCE CONSIDERATIONS

The output impedance of the signal source driving the SHC804 will affect the accuracy of the sample and hold operation both statically (at DC) and dynamically. The ouput impedance of the signal source should be low and remain low over a wide bandwidth. A small capacitor at the driving source may help to improve the charge offset errors that are affected by dynamic source impedance.

SHC803 BUFFER AMPLIFIER

The buffer amplifier incorporated in the SHC803 provides appropriate drive characteristics to the sample/hold amplifier. Again a 20pF to 50pF capacitor added to the output of the buffer amplifier may improve charge offset performance.

The buffer amplifier is optimized for fast settling with $10V_{p-p}$ signals. However, for step input signals greater than 10V, a protection network (Figure 2) is required to prevent the buffer from overload, resulting in excessive settling time.

The data sheet for the Burr-Brown model ADC803 analog-to-digital converter contains a sample printed circuit board layout incorporating many of the above considerations.

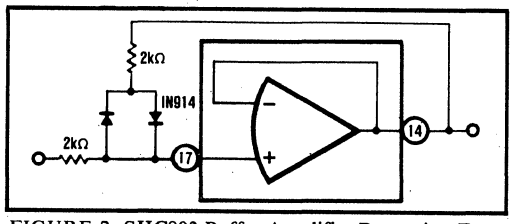


FIGURE 2. SHC803 Buffer Amplifier Protection For Input Steps Greater Than 10V.

APPLICATIONS

SIGNAL DIGITIZATION

Sample/hold amplifiers are commonly used to hold input voltages to an A/D converter constant during conversion. Digitizing errors result if the analog signal being digitized varies excessively during conversion.

For example, the Burr-Brown ADC803 is a 12-bit successive-approximation converter with a 1.5μsec conversion time. To insure the accuracy of the output data, the analog input signal to the A/D converter must not change more than 1/2LSB during the conversion.

The maximum rate of change for sine wave inputs is $dv/dt\ (max) = 2\pi Af(V/sec)$. If one allows a 1/2LSB change (2.44mV) for a ±10V input swing to the A/D converter, the allowable input rate-of-change limit would be 2.44mV/1.5μsec = 1.63mV/μsec. Thus the sampled sinusoidal signal frequency limit is

$$f = (1.63 \times 10^3)/2\pi A = 259/A(Hz)$$

where A is the amplitude of the sine wave. For a ±10V sine wave this corresponds to a frequency of 26Hz.

A sample/hold in front of the A/D converter "freezes" the converter's input signal whenever it is necessary to make a conversion. The rate-of-change limitation calculated above no longer exists. If a sample/hold has acquired an input signal and is tracking it, the sample/hold can be commanded to hold at any instant. There is

a short delay between the time the hold command is asserted and the time the circuit actually holds. This delay is called aperture delay. The hold command signal can usually be advanced in time to cause the amplifier to hold when one wants it to hold.

The uncertainty in aperture delay, called aperture jitter, is a key consideration. For the SHC803/804 there is a 25psec maximum period during which the input signal should not change, for example, more than 1/2LSB for 12-bit systems. For a ±10V input range (1/2LSB = 2.44mV), the input signal rate of change limitation is 2.44mV/25psec = 97.6V/μsec. The equivalent input sine wave frequency is

$$f = 97.6 \times 10^6/2\pi A = 15.5/A(MHz),$$

60,000 times higher than using the A/D alone.

However, there are other considerations. The resampling rate of an ADC803 is 1.5μsec (A/D conversion time) + 0.3μsec (sample/hold acquisition time) = 1.8μsec. If one samples a sine wave at the Nyquist rate this permits sampling a frequency of 278kHz. The above analysis assumed that the droop rate of the sample/hold is negligible—less than 1/2LSB during the conversion time—and that the large signal bandwidth response of the sample/hold causes negligible waveform distortion.

USING THE SHC804 WITH THE ADC803

ADC803 is a 1.5μsec, 12-bit successive approximation A/D converter. Its input circuitry has been designed to minimize high frequency current transients that appear at the input of successive approximation A/D converters. The SHC803 and SHC804 have been designed with a fast-settling, low output-impedance amplifier to further minimize the effects of high frequency transient currents present in an output load.

A typical SHC804/ADC803 connection for high-speed digitization is illustrated in Figure 3. A short delay must occur before the A/D start command is asserted since the ADC803 makes its first conversion decision 100nsec after the start command is asserted. Because the SHC804 sample-to-hold settling time is 150nsec (maximum) the additional delay required is about 50nsec. This can be achieved using a one-shot or by using the delay provided by the six inverters of a hex inverter integrated circuit. This combination can be triggered at rates of over 500k samples per second.

Using the input buffer of the SHC803 provides a high input impedance sample/hold for CMOS analog multiplexers such as the high speed Burr-Brown MPC800. The high input impedance of the SHC803 buffer minimizes DC errors caused by the ON resistance of the multiplexer switches and/or relatively high impedance signal sources (Figure 4). The multiplexer can be switched to a new channel as soon as the SHC803 is switched to the Hold mode. The multiplexer/buffer combination settles to the new input value during the sample/hold acquisition time and A/D conversion time. This "overlap" technique results in little or no loss in throughput rate.

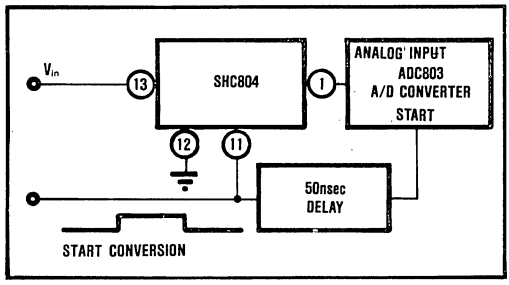


FIGURE 3. SHC804 and ADC803 Provide Sampling Rates Over 500k Samples Per Second.

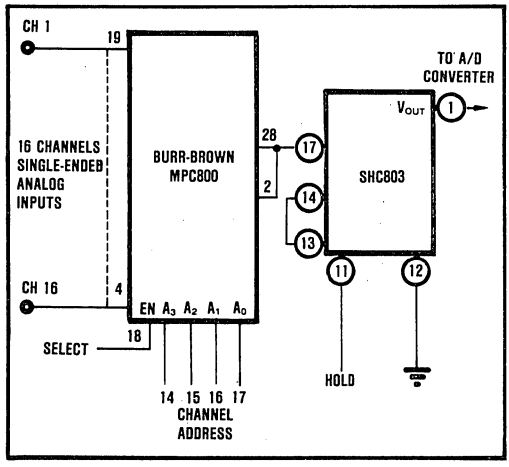


FIGURE 4. Using SHC803 With The MPC800 Analog Multiplexer.

BURR-BROWN®

SHC5320

High Speed Bipolar Monolithic SAMPLE/HOLD AMPLIFIER

FEATURES

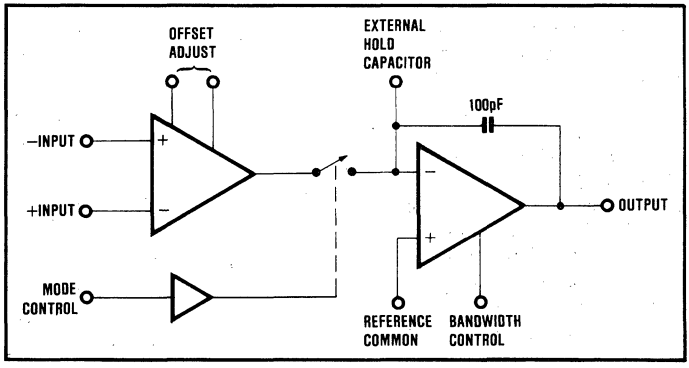
- 1.5μsec max ACQUISITION TIME TO 0.01%
- 250nsec max HOLD MODE SETTLING TIME
- 0.5μV/μsec max DROOP RATE AT +25°C
- TWO TEMPERATURE RANGES:
  0°C to +75°C (KH)
  −55°C to +125°C (SH)
- FULL DIFFERENTIAL INPUTS
- INTERNAL HOLDING CAPACITOR
- 14-PIN CERAMIC DIP PACKAGE

DESCRIPTION

The SHC5320 is a bipolar monolithic sample/hold circuit designed for use in precision high-speed data acquisition applications.

The circuit employs an input tranconductance amplifier capable of providing large amounts of charging current to the holding capacitor, thus enabling fast acquisition times. It also incorporates a low leakage analog switch and an output integrating amplifier with input bias current optimized to assure low droop rates. Since the analog switch always drives into a load at virtual ground, charge injection into the holding capacitor is constant over the entire input voltage range. As a result, the charge offset (pedestal voltage) resulting from this charge injection can be adjusted to zero by use of the offset adjustment capability. The device includes an internal holding capacitor to simplify ease of application; however, provision is also made to add additional external capacitance to improve the output voltage droop rate.

The SHC5320 is manufactured using a dielectric isolation process which minimizes stray capacitance (enabling higher-speed operation), and eliminates latch-up associated with substrate SCRs. The SHC5320KH features fully specified operation over the temperature range of 0°C to +75°C, while the SHC5320SH operates over the temperature range of −55°C to +125°C. The device requires ±15V supplies for operation, and is packaged in a reliable 14-pin ceramic dual-in-line package.



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SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies, gain = +1, and with internal holding capacitor, unless otherwise noted.

MODEL	SHC5320KH			SHC5320SH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
ANALOG							
Voltage Range	±10			•			V
Common-Mode Range	±10			•			V
Input Resistance	1	5		•	•		MΩ
Input Capacitance			3			•	pF
Bias Current		±100	±300		±70	±200	nA
Bias Current Over Temperature Range			±300			±200	nA
Offset Current		±30	±300		•	±100	nA
Offset Current Over Temperature Range			±300			±100	nA
DIGITAL (over temperature range)							
V_{IH} (Logic "1")	2.0			•			V
V_{IL} (Logic "0")			0.8			•	V
I_{IH} (V_I = +5V)			0.1			•	μA
I_{IL} (V_I = 0V)			4			•	μA
Logic "0" = SAMPLE							
Logic "1" = HOLD							
OUTPUT CHARACTERISTICS							
Voltage Range	±10			•			V
Current	±10			•			mA
Output Impedance (Hold Mode)		1			•		Ω
Capacitance Load for Stability		300			•		pF
Noise, DC to 10MHz: Sample Mode		125	200		•	•	μV rms
Hold Mode		125	200		•	•	μV rms
DC ACCURACY/STABILITY							
Gain, Open Loop, DC	3×10^5	2×10^6		10^6	•		V/V
Input Offset Voltage		±0.5			±0.2		mV
Input Offset Voltage Over Temperature Range			±1.5			±2	mV
Input Offset Voltage Drift		±5	±20		•	±15	μV/°C
CMRR[1]	72	90		80	•		dB
Power Supply Rejection[2]: $+V_{CC}$	80			•			dB
$-V_{CC}$	65			•			dB
HOLD-TO-SAMPLE MODE DYNAMIC CHARACTERISTICS							
Acquisition Time, A = −1, 10V Step[3]:							
to ±0.01%		1	1.5		•	•	μsec
to ±0.1%		0.8	1.2		•	•	μsec
SAMPLE MODE							
Gain-bandwidth Product (Gain = +1)[4]:							
C_H = 100pF		2			•		MHz
C_H = 1000pF		180			•		kHz
Full Power Bandwidth[5]		600			•		kHz
Slew Rate[6]		45			•		V/μsec
Rise Time[4]		100			•		nsec
Overshoot[4]		15			•		%
SAMPLE-TO-HOLD MODE DYNAMIC CHARACTERISTICS							
Aperture Time[7]		25			•		nsec
Effective Aperture Time	−50	−25	0	•	•	•	nsec
Aperture Uncertainty (Aperture Jitter)		0.3			•		nsec
Charge Offset (Pedestal)[8] (adjustable to zero)		1			•		mV
Charge Transfer[8]		0.1	0.5		•	•	pC
Sample-to-Hold Transient Settling Time to ±0.01% of FSR		165	250		•	•	nsec
HOLD MODE							
Droop[8]		0.08	0.5		•	•	μV/μsec
Droop at Maximum Temperature		1.2	100		17	•	μV/μsec
Drift Current[8]		8	50		•	•	pA
Drift Current at Maximum Temperature		0.12	10		1.7	•	nA
Feedthrough, 10V p-p, 100kHz sinewave		2			•		mV
POWER SUPPLIES							
$+V_{CC}$	+14.5	+15	+16	•	•	•	V
$-V_{CC}$	−14.5	−15	−16	•	•	•	V
$+I_{CC}$ ($+V_{CC}$ = 15V)[9]		11	13		•	•	mA
$-I_{CC}$ ($-V_{CC}$ = 15V)[9]		−11	−13		•	•	mA

ELECTRICAL (CONT)

MODEL	SHC5320KH			SHC5320SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE							
Specification	0		+75	−55		+125	°C
Storage	−65		+150	*		*	°C
PACKAGE	Hermetic Ceramic			Hermetic Ceramic			

*Specification same as grade to the left.

NOTES: (1) V_{CM} = ±5VDC. (2) Based on a ±0.5V swing for each supply with all other supplies held constant. (3) V_O = 10V step, R_L = 2kΩ, C_L = 50pF. (4) V_O = 200mV p-p, R_L = 2kΩ, C_L = 50pF. (5) V_{IN} = 20V p-p, R_L = 2kΩ, C_L = 50pF, unattenuated output. (6) V_O = 20V step, R_L = 2kΩ, C_L = 50pF. (7) Simulated only, not tested. (8) V_{IN} = 0V, V_{IH} = +3.5V, t_R < 20nsec (V_{IL} to V_{IH}). (9) Specified for zero differential input voltage between pins 1 and 2. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±28mA average at 20V differential.

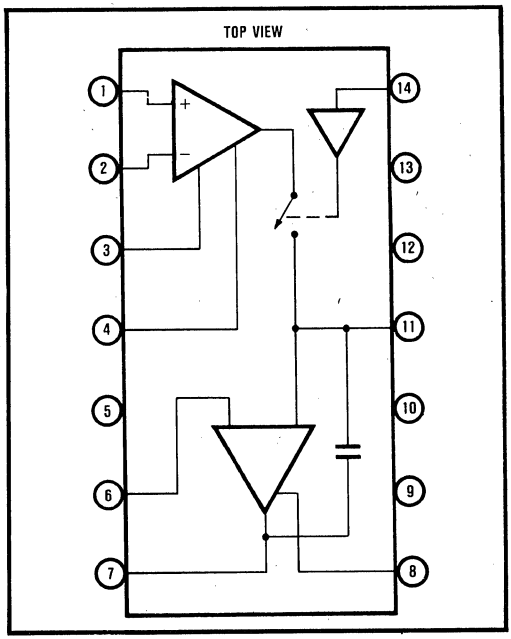
ABSOLUTE MAXIMUM RATINGS(1)

Voltage Between $+V_{CC}$ and $-V_{CC}$ Terminals 40V
Input Voltage ..... Actual Supply Voltage
Differential Input Voltage ..... ±24V
Digital Input Voltage ..... +8V, −15V
Output Current, continuous(2) ..... ±20mA
Internal Power Dissipation 450mW
Storage Temperature Range ..... −65°C < T_A < +150°C
Output Short-circuit Duration(3) ..... Momentary to Common
Lead Temperature (soldering, 10 seconds) ..... 300°C

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

NOTES: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. (2) Internal power dissipation may limit output current to less than +20mA (3) **WARNING: This device cannot withstand even a momentary short circuit to either supply.**

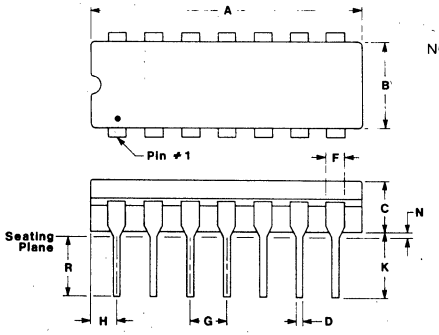
CONNECTION DIAGRAM



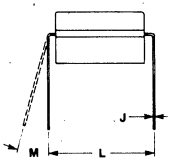
PIN ASSIGNMENTS

Pin 1	−Input	14	Mode Control
2	+Input	13	Supply Common
3	Offset Adjust	12	NC
4	Offset Adjust	11	External Hold Capacitor
5	$-V_{CC}$	10	NC
6	Reference Common	9	$+V_{CC}$
7	Output	8	Bandwidth Control

MECHANICAL



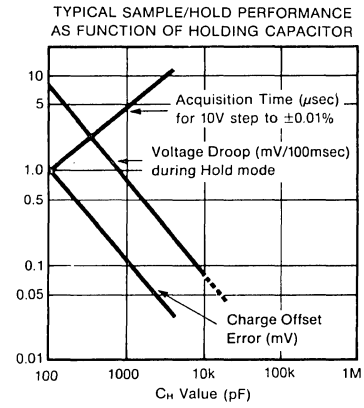
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

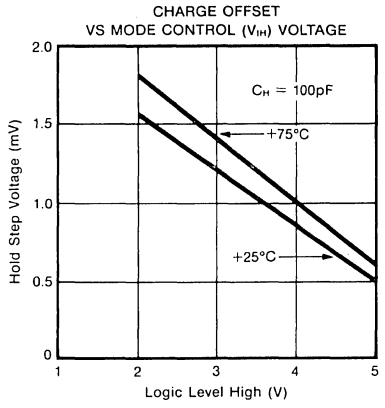


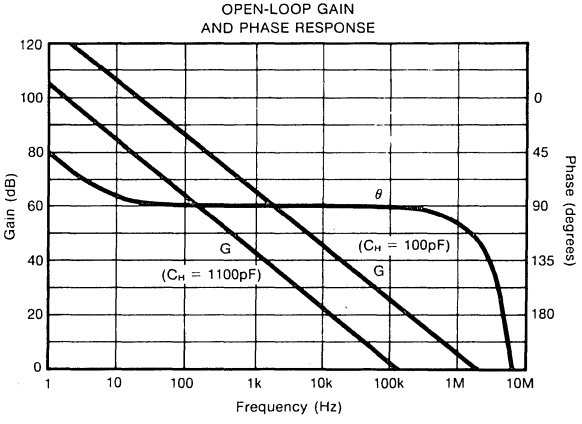
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	.790	–	20.07
B	.220	.310	5.59	7.87
C	–	.185	–	4.70
D	.014	.023	0.36	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	–	.098	–	2.49
J	.008	.012	0.20	0.30
K	.140	.260	3.56	6.60
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52
R	.125	.200	3.18	5.08

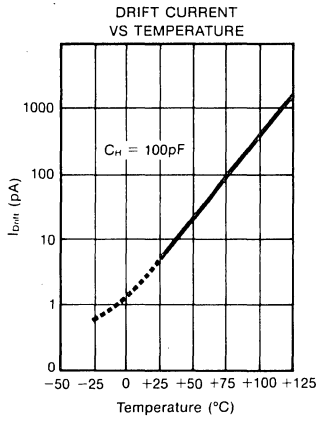
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$ = 15V.









DISCUSSION OF SPECIFICATIONS

WHAT IS A SAMPLE/HOLD AMPLIFIER?

A sample/hold amplifier (also sometimes called a track-and-hold amplifier) is a circuit that captures and holds an analog voltage at a specific point in time under control of an external circuit, such as a microprocessor. This type of circuit has many applications; however, its primary use is in data acquisition systems which require that the voltage be captured and held during the analog-to-digital conversion process. Use of a sample/hold effectively increases the bandwidth of a data acquisition system by a significant amount. For further discussion of this capability, refer to "Signal Digitization" in the Applications section of this data sheet.

The ideal sample/hold amplifier in its simplest form contains four primary components as illustrated in Figure 1, although in actual practice they may not be internally connected exactly as shown. Amplifier A_1, the input buffer, provides a high impedance load to the source circuit and supplies charging current to the holding capacitor C_H. Switch S_1 opens and closes under external control to gate the buffered input signal to the holding circuit or to remove it so that the most recently sampled signal will be held. Amplifier A_2 serves to present a high impedance load to the holding capacitor and to provide a low impedance voltage source for external loads. A

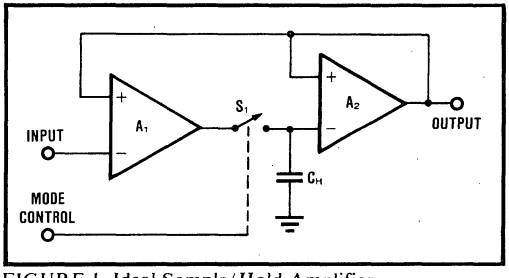


FIGURE 1. Ideal Sample/Hold Amplifier.

minimum of three terminals are provided for the user: input, output, and mode control (or sample/hold control). When S_1 is closed, the output signal follows the input signal, subject to errors imposed by amplifier bandwidth and other errors as discussed below. When S_1 is opened, the voltage stored on the holding capacitor will be held indefinitely (in the ideal case), and will appear at the output of the circuit until S_1 is again closed under command of the mode control signal.

The following discussion of specifications covers the critical types of errors which may be experienced in applications of a sample/hold amplifier. These errors are depicted graphically in Figure 2, and in the Typical Performance Curves.

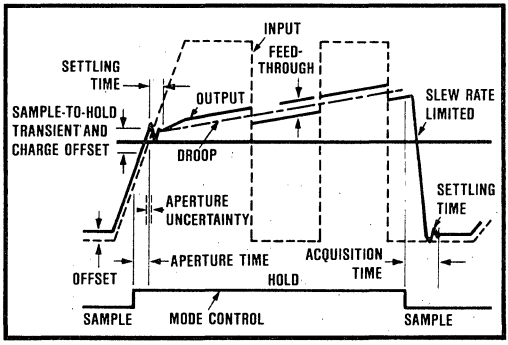


FIGURE 2. Illustration of Sample/Hold Specifications.

Acquisition Time is the time required for the sample/hold output to settle within a given error band of its final value after the sample mode is initiated. Included in this time are effects of switch delay time, slew rate of the buffer amplifier, and settling time for a specified change in held voltage value. Slew rate limitations of the buffer amplifier will cause actual acquisition time to be highly dependent on the amplitude of the voltage to be acquired, relative to the value already held by the capacitor. Therefore, proper specification of sample/hold amplifier performance includes definition of both output value step size and required error band accuracy.

Aperture Time (or aperture delay time) is the time required for switch S_1 to open and remove the charging signal from the capacitor after the mode control signal has changed from "sample" to "hold". This time is measured from the 50% point of the Hold mode transition to the time at which the output stops tracking the input. This parameter is very important in applications for which the input signal is changing very rapidly when the Hold mode is initiated.

Effective Aperture Time is the difference in propagation delay times of the analog signal and the mode control signal from their respective input pins to switch S_1. This time may be negative, zero, or positive. A negative value indicates that the mode control propagation delay is shorter than the analog propagation delay, with the result that the analog value present on the capacitor at the time the switch opens occurred earlier than the application of the mode control signal by the amount of the effective aperture delay time.

Aperture Uncertainty (or aperture jitter) is the variation observed in the aperture time over a large number of observations. This parameter is important when the analog input is a rapidly changing signal, as aperture uncertainty contributes to lack of knowledge (at the output) about the true value of the input at the precise time the Hold mode is initiated. The maximum input frequency for a given acceptable error contribution due to aperture uncertainty is

$$f_{max} = \text{Maximum Fractional Error} / 2\pi t_u$$

where Maximum Fractional Error (MFE) is the ratio of the maximum allowable error voltage to peak voltage, and t_u is the aperture uncertainty time. For a bipolar ±10V signal and a maximum uncertainty error of 1/2LSB in a 12-bit system, the MFE is equal to $1/2LSB \div V_{PEAK}$ = 2.44mV ÷ 10V = 0.000244V/V, since 1/2LSB = 2.44mV for a 20V full-scale range.

For the same system operating with a unipolar 0V to 10V signal, MFE would be 0.000122V/V.

Charge Offset (pedestal) is the output voltage change that results from charge transfer into the hold capacitor through stray capacitance when the Hold mode command is given. This charge appears as an offset voltage at the output, and in some sample/hold amplifiers may be a function of the input voltage.

Charge offset is specified for the SHC5320 using only the internal holding capacitor. When an external capacitor is added, charge offset is calculated as Charge Transfer (pC) divided by total hold capacitance. Charge Transfer is also specified for the SHC5320, and total hold capacitance is the sum of the internal hold capacitor value (100pF) and the external hold capacitor. Since charge transfer is not a function of analog input voltage for the SHC5320, this error may be removed by means of the offset adjustment capability of the amplifier.

Droop Rate is the change in output voltage over time during the Hold mode as a result of hold capacitor leakage, switch leakage, and bias current of the output amplifier. Droop rate varies with temperature and the quality of the external holding capacitor, if used. Careful circuit layout is also required to minimize droop.

Drift Current is the net leakage current affecting the hold capacitor during the Hold mode. With knowledge of the drift current, droop can be calculated as:

$$\text{Droop (V/sec)} = I_D(pA) / C_H(pF)$$

Hold Mode Feedthrough is the fraction of the input signal which appears at the output while in the Hold mode. It is primarily a function of switch capacitance, but may also be increased by poor layout practices.

Hold Mode Settling Time is the time required for the sample-to-hold transient to settle within a specified error band.

OPERATING INSTRUCTIONS

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold modes. The offset should then be adjusted to zero output for the periods when the amplifier is in the Hold mode. In this way, the effects of both amplifier offset and charge offset will be accounted for.

SAMPLE/HOLD CONTROL

A TTL logic "0" applied to pin 14 switches the SHC5320 into the Sample (track) mode. In this mode, the device acts as an amplifier which exhibits normal operational amplifier behavior, with the relationship of output to input signal depending upon the circuit configuration selected (see the Installation section below). Application of a logic "1" to pin 14 switches the SHC5320 into the Hold mode, with the output voltage held constant at the value present when the hold command is given. Pin 14 presents less than one LSTTL load to the driving circuit throughout the full operating temperature range.

ADDITION OF AN EXTERNAL CAPACITOR

The SHC5320 contains an internal 100pF MOS holding capacitor, sufficient for most high-speed applications. If improved droop performance is desired (with increased acquisition time), additional capacitance may be added between pins 7 and 11. If an external holding capacitor C_H is used, then a noise-bandwidth capacitor with a value of $0.1C_H$ should be connected from pin 8 to ground. The exact value and type of this bandwidth capacitor are not critical.

Capacitors with high insulation resistance and low dielectric absorption, such as Teflon® or polystyrene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor to minimize droop errors.

The value of the external capacitor determines the droop, charge offset, and acquisition time of the sample/hold. Both droop and charge offset will vary linearly with total hold capacitance from the values given in the specification table for the internal 100pF capacitor. The behavior of acquisition time versus total hold capacitance is shown in the Typical Performance Curves.

OUTPUT PROTECTION

In order to optimize high-frequency performance of this device, output protection is not included. This high-frequency performance is mandatory for a good sample/hold, which must absorb high-frequency changes in load current when driving a successive-approximation A/D converter. Due to the lack of output protection, the output circuit will not tolerate an indefinite short to common, but a momentary short is permissible. The output should never be shorted to supply.

Teflon® DuPont Corporation

INSTALLATION

LAYOUT PRECAUTIONS

Since the holding capacitor is connected to virtual ground at one end (pin 11) and to a low-impedance voltage source at the other (pin 7), the SHC5320 does not require the use of guard rings and other careful layout techniques which are required by many sample/hold circuits. However, normal good layout practice should be observed, minimizing the possibility of leakage paths across the holding capacitor. As in all digital-analog circuits, analog signal lines on the circuit board should cross digital signal paths at right angles whenever possible.

GROUNDING AND BYPASSING

Pin 6 (REFERENCE COMMON) should be connected to the system analog signal common as close to the unit as possible. Likewise, pin 13 (SUPPLY COMMON) should be connected to the system supply common. If the system design prevents running these two common lines separately, they should be connected together close to the unit, preferably to a large ground plane surrounding the sample/hold. Bypass capacitors (0.01μF to 0.1μF ceramic in parallel with 1μF to 10μF tantalum) should be connected from each power supply terminal of the device to pin 13 (SUPPLY COMMON).

OFFSET ADJUSTMENT

Offset adjustment capability may be achieved by connecting a 10kΩ, 10-turn potentiometer as illustrated in Figure 3.

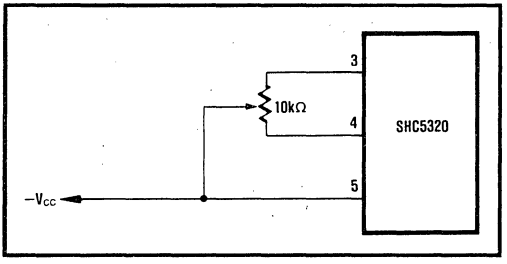


FIGURE 3. Connection of Offset Adjustment Potentiometer.

NONINVERTING MODE

The most common application of the SHC5320 will utilize the connection illustrated in Figure 4. In this mode of operation, the sample/hold will operate as a unity-gain noninverting amplifier when in the Sample mode, and the output signal will track the input. The high bandwidth of the SHC5320 and the large open-loop gain assure that gain error will be minimized.

When sampling lower-amplitude signals, the SHC5320 may also be connected as a noninverting amplifier with gain, as illustrated in Figure 5. In this circuit the gain of the amplifier is equal to $1 + R_2/R_1$ when sampling.

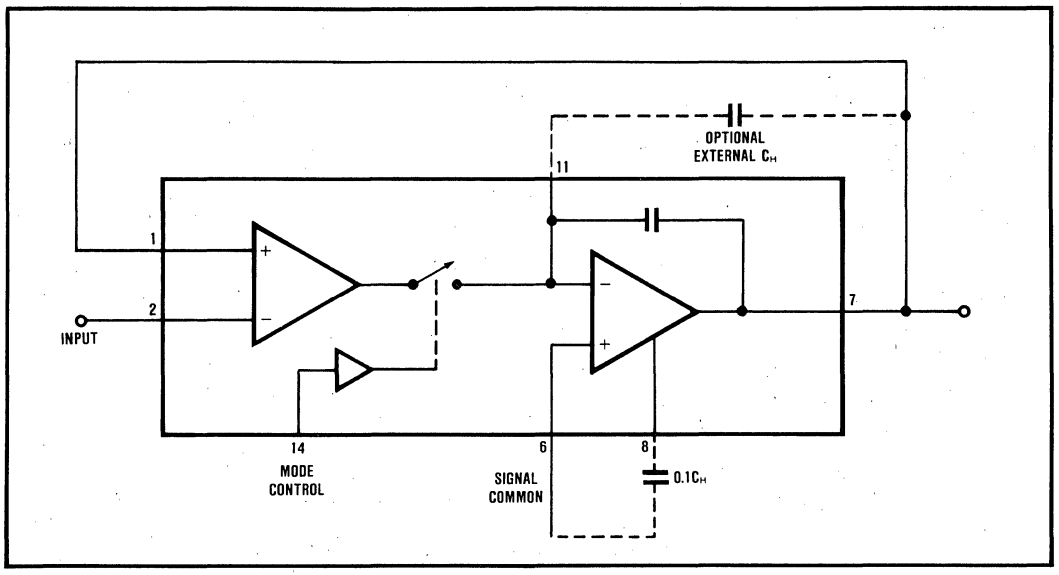


FIGURE 4. Noninverting Unity-Gain Connections.

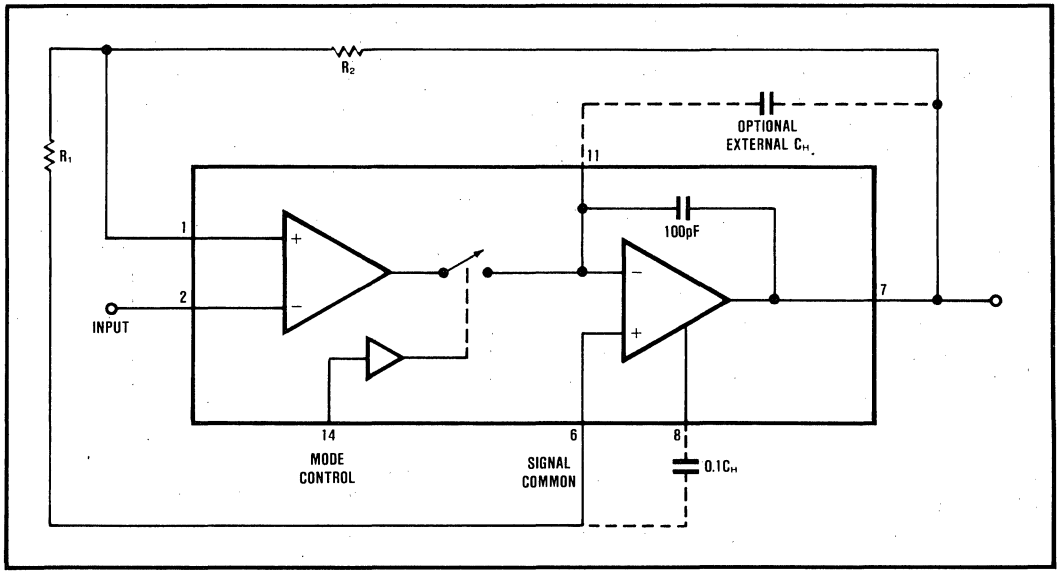


FIGURE 5. Noninverting Configuration with Gain = $1 + R_2/R_1$.

INVERTING MODE

Unlike most sample/holds, the SHC5320 may also be connected to act as an inverting amplifier, as shown in Figure 6. For this configuration, the gain is equal to $-R_2/R_1$.

For further discussions of operational amplifiers and how to use them, consult the Burr-Brown/ McGraw-Hill Electronics Series of reference books, available through your local Burr-Brown sales office.

INPUT OVERLOAD PROTECTION

It is possible that the input transconductance amplifier of the SHC5320 will saturate when the unit is in the Hold mode, due to a nonzero differential signal appearing between pins 1 and 2. This differential signal may be the result of a rapidly changing input signal or application of a new channel from an input multiplexer. When the input buffer is saturated in this fashion, acquisition time may be degraded because of the time required for

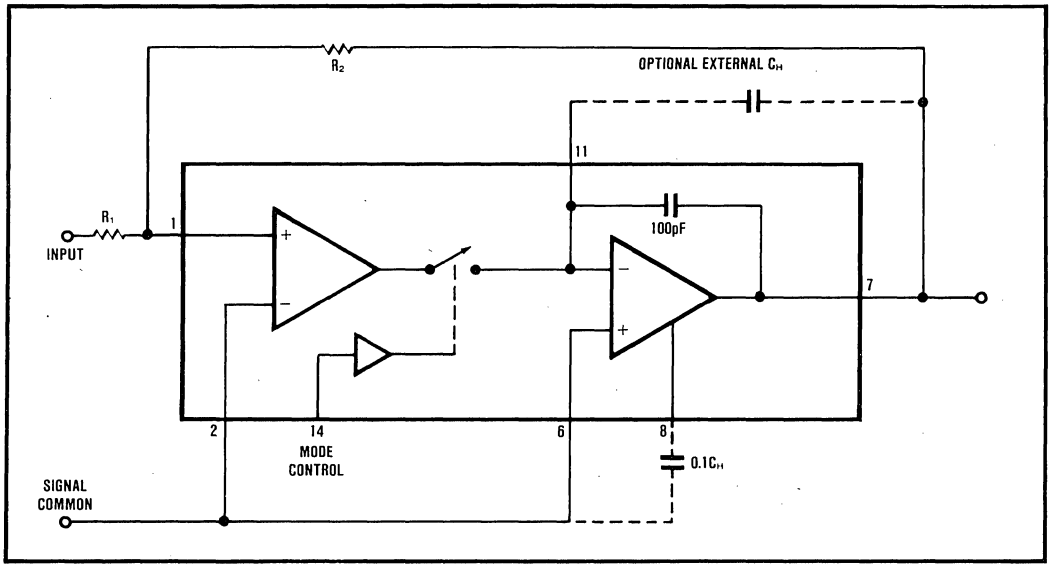


FIGURE 6. Inverting Configuration with Gain = $-(R_2/R_1)$.

the buffer to recover from saturation. In addition, the input buffer, which is designed to provide large amounts of charging current to the output integrator, may draw large amounts of supply current which may exceed 40mA peak in some applications. For these reasons, it is desirable to limit the differential voltage which may appear at the summing junction of the input buffer. Figures 7 and 8 illustrate possible methods of providing this

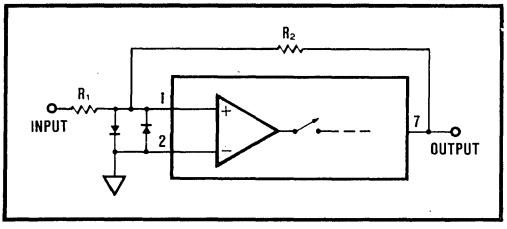


FIGURE 7. Input Overload Protection—Inverting Configuration.

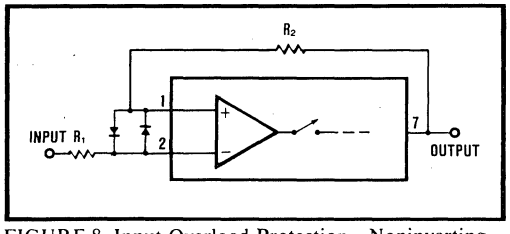


FIGURE 8. Input Overload Protection—Noninverting Configuration.

voltage limitation for the inverting and noninverting configurations. The diodes may be Schottky diodes, which will provide the fastest clamping action and lowest clamping voltage, but fast signal diodes such as 1N914 will also work in most applications. In each configuration the value of R_1 should be large enough to avoid excessive loading of the input signal source. Similarly, R_2 should have a value of 2kΩ or greater to insure sufficient load current capability from the sample/hold. If the value of R_2 becomes too large, however, the added capacitance of the diodes may change the sample/hold phase response enough to cause oscillation.

APPLICATIONS

SIGNAL DIGITIZATION

Sample/hold amplifiers are normally used to hold input voltages to an A/D converter constant during conversion. Digitizing errors result if the analog signal being digitized varies excessively during conversion.

For example, the Burr-Brown ADC80H-AH-12 is a 12-bit successive-approximation converter with a 25μsec conversion time. To insure the accuracy of the output data, the analog input signal to the A/D converter must not change more than 1/2LSB during conversion.

The maximum rate of change of a sine wave of frequency, f, is dv/dt (max) = $2\pi Af$(V/sec). If one allows a 1/2LSB change (2.44mV) for a ±10V input swing to the A/D converter, the allowable input rate-of-change limit would be 2.44mV/25μsec = 0.0976mV/μsec. Thus the sampled sinusoidal signal frequency limit is

$$f = (0.0976 \times 10^3)/2\pi A = 15.5/A \text{ (Hz)},$$

where A is the peak amplitude of the sine wave. For a ±10V sine wave, this corresponds to a frequency of 1.6Hz, hardly acceptable for the majority of sampled data systems.

However, a sample/hold in front of the A/D converter "freezes" the converter's input signal whenever it is necessary to make a conversion. The rate-of-change limitation calculated above no longer exists. If a sample/hold has acquired an input signal and is tracking it, the sample/hold can be commanded to hold it at any instant in time. There is a short delay (aperture delay) between the time the hold command is asserted and the time the circuit actually holds. The hold command signal can usually be advanced in time (or delayed, in the case of negative effective aperture delay) to cause the amplifier to hold the signal actually desired.

Aperture uncertainty (also called aperture jitter) is also a key consideration. For the SHC5320 there is a 300psec period during which the signal should not change more than the amount allowed for aperture uncertainty in the system error budget, perhaps 1/2LSB for a 12-bit system. For a ±10V input range (1/2LSB = 2.44mV), the input signal rate of change limitation is 2.44mV/0.3nsec = 8.13mV/nsec. The equivalent input sine wave frequency is

$$f = 8.13 \times 10^6 / 2\pi A = 1.29/A \text{ (MHz)},$$

a factor of almost 84,000 higher than using the A/D alone.

However, there are other considerations. The resampling rate of an ADC80H/SHC5320 combination is 26.5μsec (25μsec A/D conversion time plus 1.5μsec S/H acquisition time). Sampling a sine wave at the Nyquist rate, this permits a maximum input signal frequency of 37.7kHz. The above analysis assumes that the droop rate of the sample/hold is negligible—less than 1/2LSB during the conversion time—and that the large signal bandwidth response of the sample/hold causes negligible waveform distortion. Both of these assumptions are valid for the SHC5320 in this application.

DATA ACQUISITION

The SHC5320 may be used to hold data for analog-to-digital conversion or may be used to provide pulse-amplitude modulation (PAM) data output (see Figures 9 and 10).

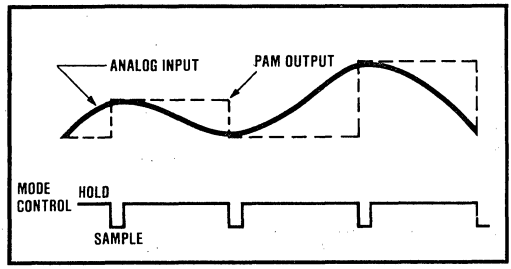


FIGURE 10. PAM Output.

DATA DISTRIBUTION

The SHC5320 may be used to hold the output of a digital-to-analog converter and distribute several different analog voltages to different loads (see Figure 11).

HIGH-SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the A/D converter. If two or more sample/holds are used with a multiplexer (such as the Burr-Brown MPC8S or MPC16S) as shown in Figure 12, the acquisition time of the sample/hold can be virtually eliminated. While the first channel is in hold and switched into the A/D converter, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this signal by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed. In low level systems an instrumentation amplifier (such as the Burr-Brown INA101) and a differential multiplexer (such as the Burr-Brown MPC4D or MPC8D) may be required in front of the sample/hold. The settling and acquisition times of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the total conversion time as before by operating in this overlapped mode with the sample/holds.

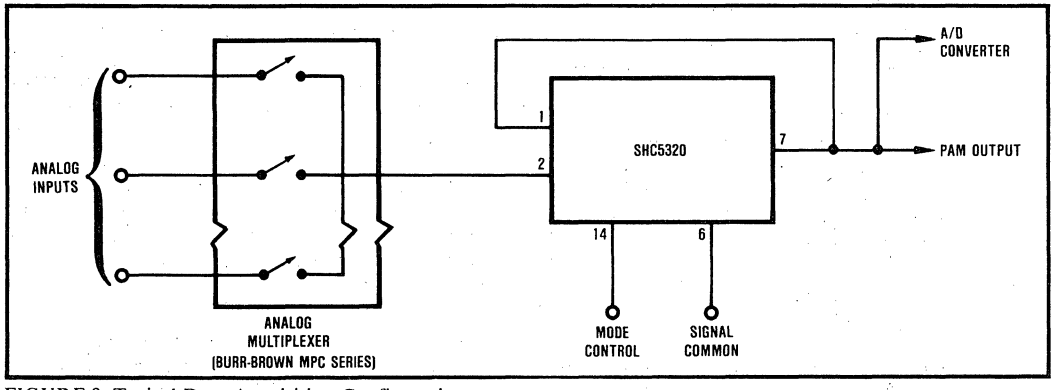


FIGURE 9. Typical Data Acquisition Configuration.

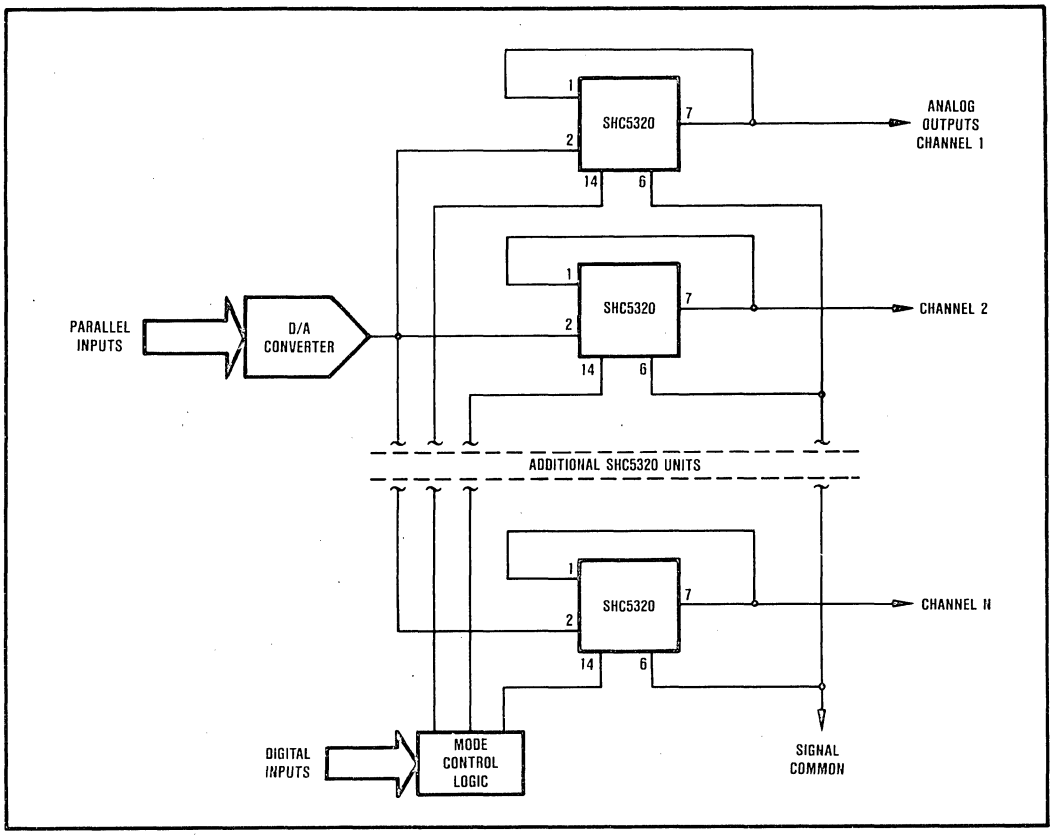


FIGURE 11. Typical Data Distribution Configuration.

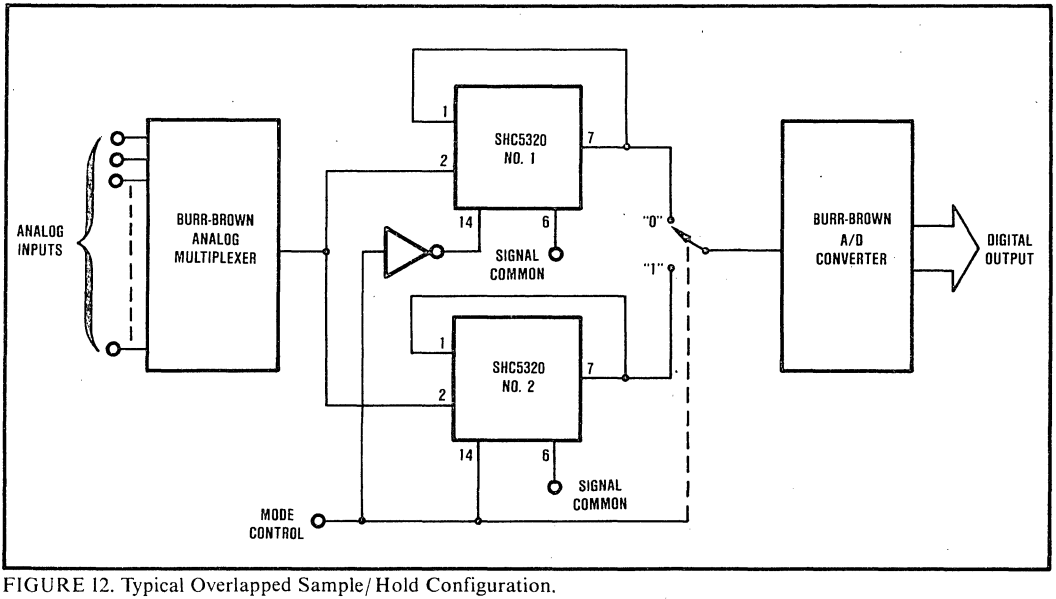
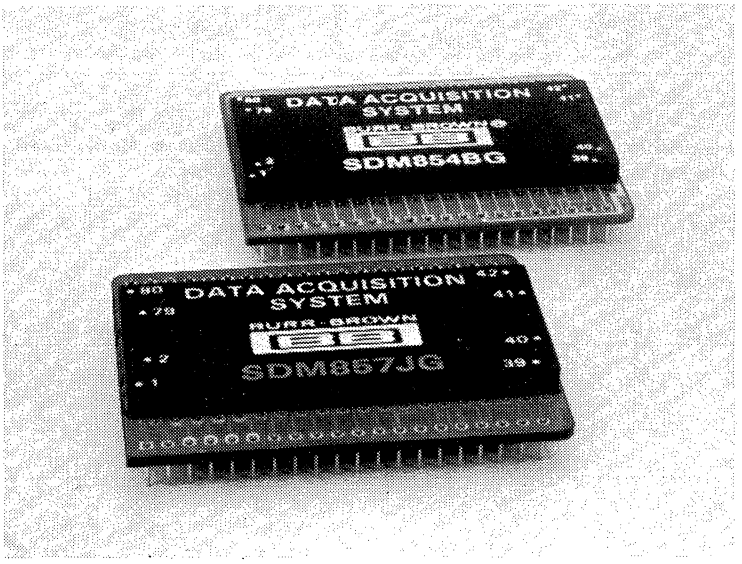


FIGURE 12. Typical Overlapped Sample/Hold Configuration.

DATA ACQUISITION SUBSYSTEMS



If your system requires data acquisition and conversion, you may want to consider one of our system data modules (SDM) or microprocessor compatible modules (MP). Each contains a multiplexer, A/D converter, and timing and control logic, with instrumentation amplifiers and sample/hold circuits also available in some modules for use in capturing low-level and high-frequency signals. The microprocessor compatible modules (MPs) are SDMs which contain address decoding and specialized control logic, making them compatible with most available microprocessors. These subsystems, fully tested at the factory, have a proven record of reliability.

Modules of this type are very popular in applications requiring rapid design turn-around, and also where the user lacks the necessary skill and experience in performing fully optimized analog circuit layouts and component performance matching. Typical applications include industrial measurement and control (such as process monitoring), test equipment, and any other application requiring total guaranteed performance with a minimum of utilized space.

As with all Burr-Brown conversion products, these units are designed to provide a total solution.

SELECTION GUIDE

DATA ACQUISITION COMPONENTS

These components provide a complete data acquisition function in one small package. You can devote your design efforts to other tasks because the totally self-contained component includes input multiplexer, sample-and-hold amplifier and 12-bit A/D converter. Timing and control logic, clock, and reference are all included.

DATA ACQUISITION COMPONENTS							
Description	Model	Channels	Resolution (Bits)	Throughput Accuracy (% of FSR)	Throughput Rate, min (kHz)	Package	Page
Hybrid, ±10V Input	SDM854AG SDM854BG	16 single-ended, 8 differential	12 12	±0.048 ±0.024	33 25	QIP[1] QIP	8-7 8-7
Hybrid	SDM856JG SDM856KG	16 single-ended, 8 differential	12 12	±0.048 ±0.024	33 25	QIP QIP	8-12 8-12
Hybrid, Low Level	SDM857JG SDM857KG	16 single-ended, 8 differential	12 12	±0.048 ±0.024	22 18	QIP QIP	8-12 8-12

NOTES: (1) Quad in-line package.

MICROPROCESSOR INTERFACED ANALOG INPUT SYSTEMS							
Description	Model	Channels	Resolution (Bits)	Accuracy, max (% of FSR)	Throughput max (ppm/°C)	Tempco, Package	Page
High Accuracy	MP32BG MP32CG	16 single-ended 8 differential	12 12	±0.05 ±0.025	±60 ±60	QIP QIP	8-3 8-3

BURR-BROWN®

MP32

FOR A COMPLETE DATA SHEET, SEE PDS-424B

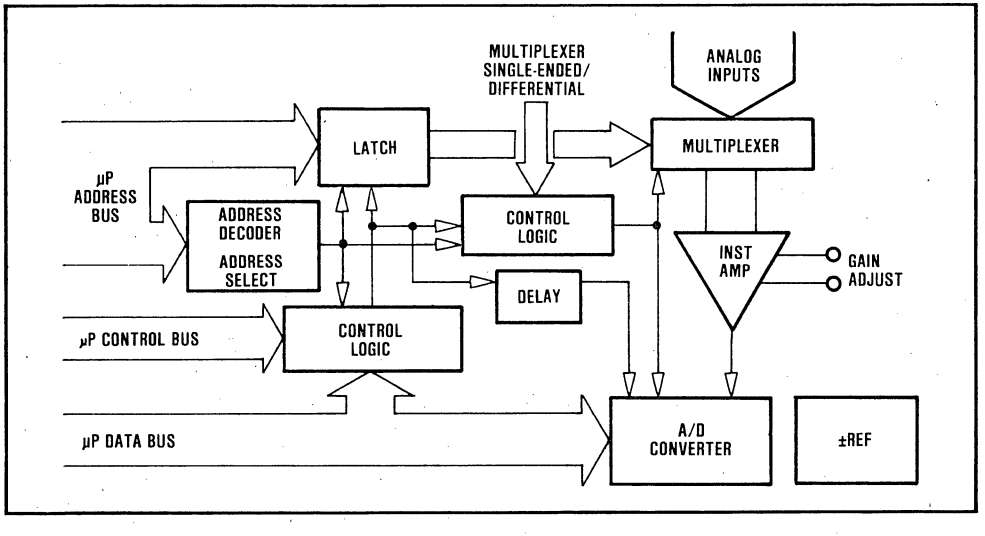
Microprocessor-Interfaced 12-BIT DATA ACQUISITION SYSTEM

FEATURES

- INTERFACES WITH SEVERAL MICROPROCESSOR TYPES WITHOUT ADDITIONAL COMPONENTS
- COMPATIBLE WITH SEVERAL MINICOMPUTERS
- EASY TO PROGRAM
  - One instruction acquires data as a memory-mapped device
  - Two instructions acquire data as an accumulator I/O device

DESCRIPTION

The MP32 is a complete analog input system and interfaces to many microprocessors without additional external components. Contained in an 80-pin quad-in-line package, it includes a 12-bit CMOS A/D converter, instrumentation amplifier, input multiplexer that accepts up to 16 single-ended signals or 8 differential signals, an addess decoder, and control logic. Logic to generate interrupt, halt, and direct memory access request signals is also included. The system can digitize low level or high level analog signals. Gain of the internal instrumentation amplifier can be programmed with a single external resistor allowing input ranges as low as ±10mV.



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DESCRIPTION (CONT)

ANALOG MULTIPLEXERS

Two 8-channel CMOS analog multiplexers are used on the input which permits selection of 16 single-ended or 8 differential inputs. A 16-channel pseudo-differential mode of operation can also be achieved by connecting the amplifier's inverting input to a common, remote signal ground. Channels are addressed by the address decoder which is connected directly to the microprocessor address bus. The number of input channels can be expanded without limit using external multiplexers.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is a low drift, differential amplifier featuring high speed at gains above unity and gain programming with an external resistor. Gain may be selected from unity to 500.

ANALOG-TO-DIGITAL CONVERTER

The 12-bit A/D converter is a CMOS, successive approximation device with 40μsec conversion time and three-state outputs. Laser-trimmed, compatible thin-film networks are used to assure linearity and stability over wide temperature ranges.

ADDRESS DECODER

The 12-bit address decoder has been included in the MP32 so the device can be uniquely specified within 4k bands of the address field. If further decoding is required, the chip select (CS) pin can provide a 13th bit or the output of an external decoder can be connected to the internal address decoder output "wired-AND" node.

DELAY TIMER

A time delay between channel selection and start of conversion is built into the MP32 and is described in detail in the Analog Input Configuration section.

CONTROL LOGIC

The control logic generates signals to halt or interrupt the CPU while conversion takes place and to signal the CPU when conversion is complete and data can be read. Enable signals are also generated to gate the data onto the data bus.

REFERENCE

The internal voltage reference of the MP32 has been optimized for stable outputs with respect to temperature. Output current up to 2mA can be drawn externally from the reference outputs.

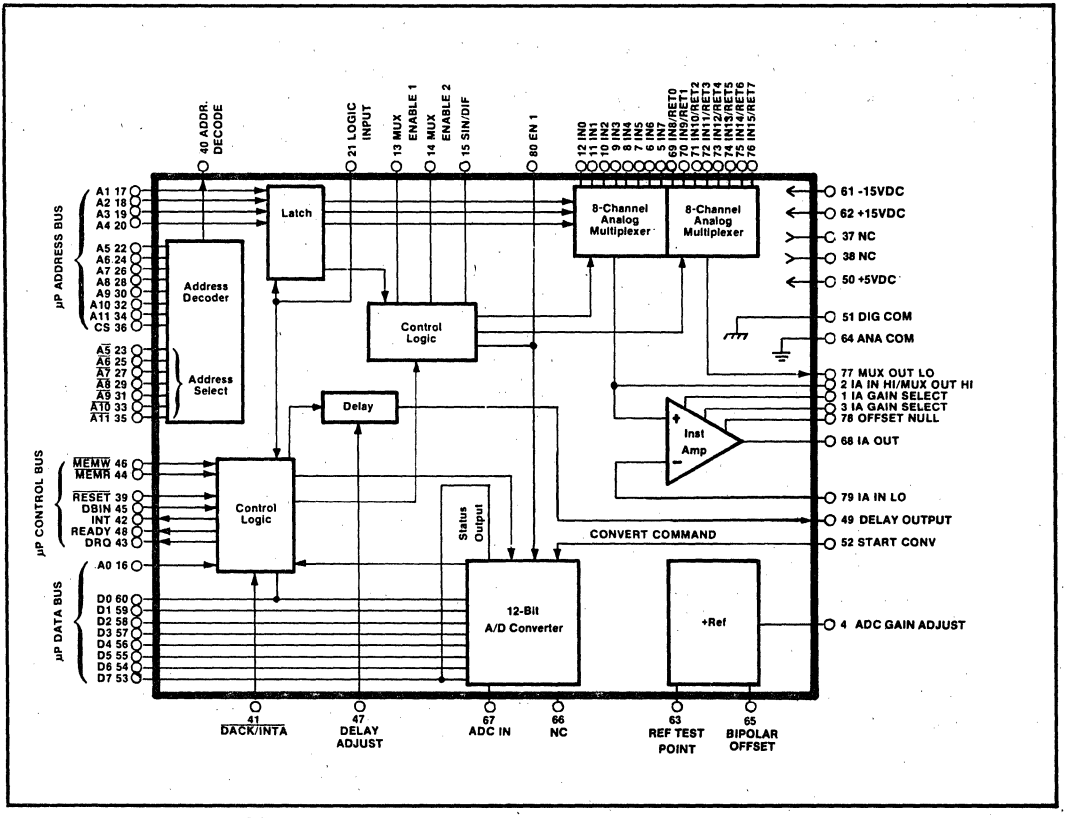


FIGURE 1. System Block Diagram.

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated supplies unless otherwise noted.

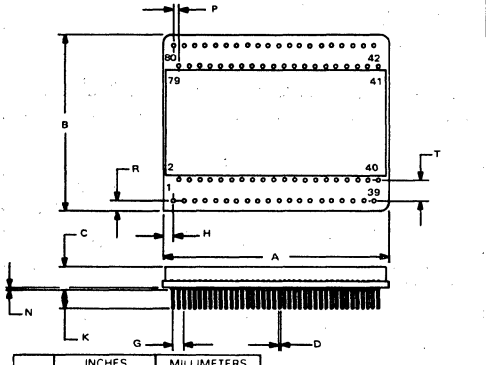
MODEL	MP32BG AND MP32CG MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS				
Resolution(1)	12	12	12	Bits
Number of Channels		16 Single-ended/8 Differential		
Throughput Rate(1) at G = 1	50	70	80	µsec/Channel
ANALOG INPUT/OUTPUT				
ADC Voltage Input Ranges(2)				
Bipolar(3)		±10		V
Unipolar(1)		0 to +10		V
Amplifier Gain Range		1 to 500		V/V
Gain Equation		1 + (25kΩ/R_{EXT})		
Input Voltage Without Damage			±35	V
Input Voltage for Multiplexer Operation			±10	V
Input Impedance				
Off Channel			10^{18}	Ω
On Channel		1.5	1.8	kΩ
Bias Current				
+25°C			300	nA
0°C to +70°C			400	nA
Amplifier Output Noise G = 100, R_S = 1500Ω		1.2		mV, rms
		7.0		mV, p-p
Amplifier Input Offset		±0.5	±7.0	mV
Amplifier Input Offset Drift (R_{source} = 1.5kΩ max)		±[7 + (90/G)]	±[26 + (190/G)]	µV/°C
Amplifier Gain Drift, (R_{EXT} ≤ 10ppm/°C)				
G = 1			±10	ppm/°C
G = 10			±110	ppm/°C
G = 100			±120	ppm/°C
G = 500			±120	ppm/°C
Amplifier Settling Time to ±0.01% of FSR				
G = 1(1)			15	µsec
G = 10		20		µsec
G = 100		25		µsec
G = 500		100		µsec
CMRR for Differential Inputs DC to 60Hz	80	84		dB
Instrumentation Amplifier				
Power Supply Sensitivity			[1 + (2/G)] 10-4	% FSR/%ΔV
ACCURACY				
System RSS Accuracy(4) at 25kHz Throughput				
G = 1, BG			±0.05	
CG			±0.025	
Linearity, BG			±0.025	% FSR
CG			±0.0125	% FSR
Differential Linearity, BG		±0.025		% FSR
CG		±0.0125		% FSR
Gain Error		Adjustable to Zero		
Offset Error		Adjustable to Zero		
System RSS Accuracy at 1kHz Throughput				
G = 500			±0.39	%FSR
ADC Accuracy Drift				
Linearity			±3	ppm/°C
Gain			±10	ppm/°
Reference Drift				
Ref Out (Pin 63)			±15	ppm/°C
Bipolar Offset (Pin 65)			±25	ppm/°C
System Accuracy Drift (Excluding IA)				
Unipolar			±25	ppm/°C
Bipolar			±60	ppm/°C
No Missing Codes (-25°C to +85°C)(Bits 1 thru 12)CG		Guaranteed		
(Bits 1 thru 11)BG		Guaranteed		

ELECTRICAL (CONT)

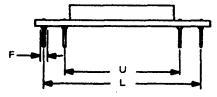
MODEL	MP32BG AND MP32CG			
	MIN	TYP	MAX	UNITS
Power Supply Sensitivity (Excluding IA)				
±15VDC			±0.008	% FSR/%ΔV
+5VDC			±0.0002	% FSR/%ΔV
DIGITAL INPUT/OUTPUT				
Biopolar Code		Bipolar Offset Binary		
Unipolar Code		Unipolar Straight Binary		
Logic Loading Pin (21)			3LSTTL	
Logic Loading Pin (60)			2LSTTL	
All Other Digital Inputs			1LSTTL	
Output Drive	1TTL Load			
Analog Input Channels Selected By:		A1-A4		
Output Data		D0-D7		
POWER REQUIREMENTS				
Rated Power Supply Voltages(1)		±15, +5		VDC
Power Supply Ranges for Rated Accuracy		+4.75 to +5.25 and ±11.4 to ±15.75		VDC
Power Supply Operating Range (±15VDC only)	±10		±18	VDC
Supply Drain				
+15VDC		10	20	mA
-15VDC		15	20	mA
+5VDC		80	160	mA
Power Dissipation (at rated supplies)		700	1300	mW
TEMPERATURE RANGE				
Specification	-25		+85	°C
Operating	-40		+100	°C
Storage	-55		+125	°C

NOTES:
1. These parameters are 100% tested. 2. Input voltage must be kept 2V below supply voltage. 3. External amplifier required. 4. Gain and offset adjust to zero.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	



NOTE:
LEADS IN TRUE POSITION WITHIN 0.015" 0.38mm R @ MMC AT SEATING PLANE.

Pin numbers shown for reference only. Numbers may not be marked on package.

MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz.)
MATING CONNECTOR: 2350MC (set of four 20 pin strips)

PIN ASSIGNMENTS

	Pin No.	
IA GAIN SELECT	1	41 DACK/INTA
IA IN HI/MUX OUT HI	2	42 INT
IA GAIN SELECT	3	43 DRQ
ADC GAIN ADJUST	4	44 MEMR
IN7	5	45 DBIN
IN6	6	46 MEMW
IN5	7	47 DELAY ADJUST
IN4	8	48 READY
IN3	9	49 DELAY OUTPUT
IN2	10	50 +5VDC
IN1	11	51 DIG COM
IN0	12	52 START CONV
MUX ENABLE 1	13	53 D7 MSB
MUX ENABLE 2	14	54 D6
SIN/DIF	15	55 D5
A0	16	56 D4
A1	17	57 D3
A2	18	58 D2
A3	19	59 D1
A4	20	60 D0 LSB
LOGIC INPUT	21	61 -15VDC
A5	22	62 +15VDC
$\overline{A5}$	23	63 REF TEST POINT
A6	24	64 ANA COM
$\overline{A6}$	25	65 BIPOLAR OFFSET
A7	26	66 NC
$\overline{A7}$	27	67 ADC IN
A8	28	68 IA OUT
$\overline{A8}$	29	69 IN8/RET0
A9	30	70 IN9/RET1
$\overline{A9}$	31	71 IN10/RET2
A10	32	72 IN11/RET3
$\overline{A10}$	33	73 IN12/RET4
A11	34	74 IN13/RET5
$\overline{A11}$	35	75 IN14/RET6
CHIP SELECT CS	36	76 IN15/RET7
NC	37	77 MUX OUT LO
NC	38	78 OFFSET NULL
RESET	39	79 IA IN LO
ADDR DECODE	40	80 EN1

BURR-BROWN®

SDM854

FOR A COMPLETE DATA SHEET, SEE PDS-423D

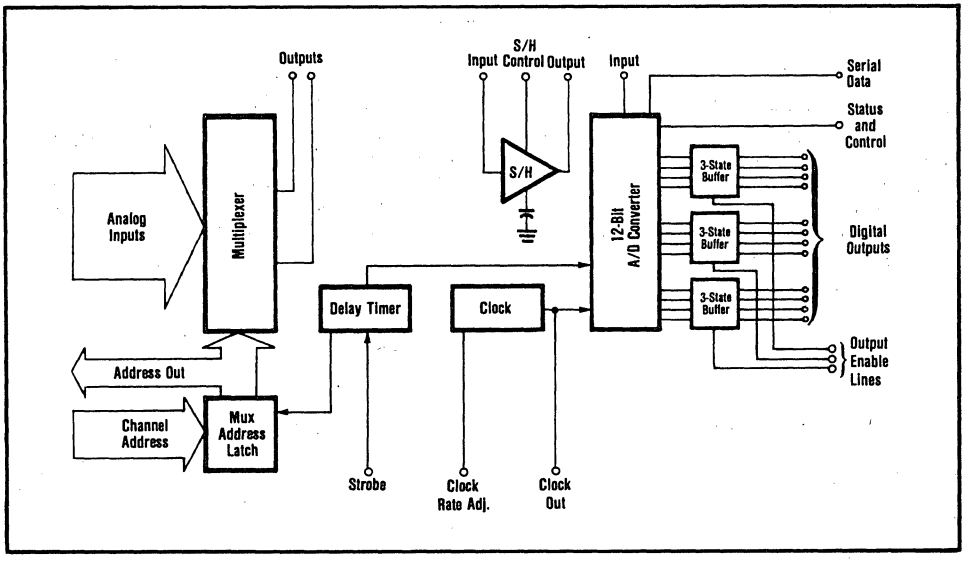
HYBRID DATA ACQUISITION SYSTEM

FEATURES

- 12-BIT, ±0.012% LINEARITY ERROR
- INPUTS UP TO ±10 VOLTS
- WIDE TEMPERATURE RANGE
- SELECTABLE 16 SINGLE, 8 DIFFERENTIAL INPUTS
- THREE-STATE OUTPUT BUFFERS

DESCRIPTION

The SDM854 is a complete data acquisition system contained in a miniature 2.2" x 1.7" x 0.22" (55.9mm x 43.2mm x 5.6mm) ceramic package. This system offers all the functions available in large modular data acquisition systems. Inputs up to ±10V can be accepted and low-level inputs can be accommodated by connecting an external instrumentation amplifier to the output of the multiplexer and to the input of the sample/hold amplifier. Digital resolution is 12 bits with accuracy of ±0.024% at a throughput rate of 27kHz.



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SYSTEM DESCRIPTION

The SDM854 contains all components necessary to multiplex and convert analog signals up to ±10V into equivalent digital outputs. Throughput sampling rates are from 27kHz (12-bit resolution) to 70kHz (8-bit resolution) in the overlap mode of operation. The SDM854 can be configured to accept either 8-channel differential or 16-channel single-ended signals and can be expanded almost without limit with external multiplexers. Three-state outputs are provided for easy interface to microprocessor and other bus-structure systems. The system components are illustrated in Figure 1 and described in the following paragraphs.

ANALOG MULTIPLEXER

The analog multiplexer consists of two CMOS integrated circuits. Pin interconnects are used to select 16-channel single-ended or 8-channel differential operation. In single-ended operation the multiplexer can be used in a pseudo-differential mode by connecting an external amplifier's inverting input to common remote signal ground. Channel selection is made by an internally latched 3- or 4-bit binary word, for differential or single-ended operation respectively.

SAMPLE/HOLD

A complete stand-alone circuit, the sample/hold amplifier features buffered output, 10μsec acquisition time, and 100nsec aperture time.

Input, output, and mode control lines are brought out to separate pins. This allows maximum system flexibility for performing functions, such as automatic gain ranging, with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a 12-bit, 25μsec converter with 0.01% linearity error. Its features include positive and negative reference voltage outputs, external gain and offset adjustments, straight binary or two's complement output, serial data and clock outputs, status output, a short cycle feature, and a clock rate control for higher throughput rates at lower resolution or accuracy.

THREE-STATE OUTPUT BUFFERS

Digital outputs of the ADC are internally buffered by LSTTL three-state buffers. Three separate enable lines are brought out for easy interfacing to 4-, 8- or 16-bit data buses. $\overline{\text{MSB}}$ and BUSY are also buffered by separate three-state devices, each with its own enable line.

ADDRESS LATCH

Outputs of the 4-bit LSTTL register latch are connected to the address inputs of the multiplexer. This latch serves as an address storage register for the selected analog input. It may be loaded through 4 address inputs. Other inputs are LOAD and CLEAR. The 3 least significant bits are used for 8-channel differential mode addressing.

DELAY TIMER

A delay timer allows settling time for the multiplexer and sample/hold circuits before conversion begins. The delay is adjustable over a wide range by use of an external resistor or capacitor. This allows for longer settling time if an external instrumentation amplifier is used and is operating at high gains, or shorter settling time for lower resolution operation.

CHANNEL EXPANSION

The number of analog input channels of the SDM854 can be easily increased by using Burr-Brown's MPC8D (8-channel differential) and MPC16S (16-channel single-ended) multiplexers. These are latch-free devices which contain internal binary decoding at TTL or MOS levels and may be integrated into a system with minimal external logic.

SYSTEM PERFORMANCE

The SDM854 is configured for random channel selection. With the addition of an external counter they can be configured to continuously sequence through all analog channels or sequence through all analog channels on command from an external trigger.

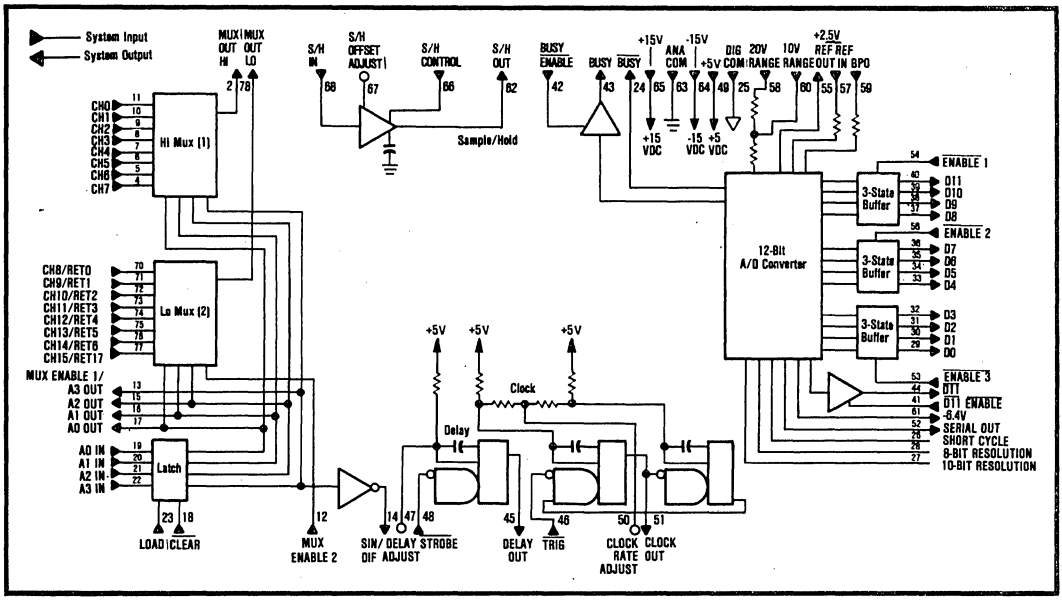


FIGURE 1. SDM854 Block Diagram.

With the appropriate 4-bit (single-ended) or 3-bit (differential) channel address on the latch inputs, and DELAY OUT (pin 45) tied to the LOAD input (pin 23), a negative going edge is applied to the $\overline{\text{STROBE}}$ input (pin 48). This starts the delay timer, latches the multiplexer address, and allows the input signal to pass through the multiplexer, and sample/hold before starting the A/D conversion. The DELAY OUT signal (pin 45) is also connected to the $\overline{\text{TRIG}}$ input (pin 46) and the A/D conversion is initiated on the negative-going edge. The S/H CONTROL input (pin 66) is connected to $\overline{\text{BUSY}}$ (pin 24) so that the sample/hold is in the HOLD mode during the A/D conversion.

By using overlap programming the settling time effects of the analog multiplexer and external instrumentation amplifier (if used) can be reduced, extending throughput sampling rates up to 27kHz for 12-bit and 70kHz for 8-bit resolution (ADC short-cycled). This mode of operation is most useful when converting low-level inputs to accommodate the increased settling time of the external instrumentation amplifier. Overlap programming is accomplished by connecting $\overline{\text{BUSY}}$ to $\overline{\text{STROBE}}$ and S/H CONTROL; DELAY OUT to LOAD and $\overline{\text{TRIG}}$. In this mode of operation the address of the next channel to be converted is latched and the output of the external instrumentation amplifier allowed to settle to a new value during the present conversion.

DIGITAL INPUT SPECIFICATIONS

Address Inputs (A0 - A3)	One standard LSTTL load, positive true
Address Coding	4-bit binary
LOAD	One standard LSTTL load, positive true, address loaded on positive edge.
$\overline{\text{CLEAR}}$	One standard LSTTL load, negative true, low level clears address latch.
$\overline{\text{STROBE}}$	One standard TTL load, high-to-low transition triggers the delay timer.
$\overline{\text{TRIG}}$	One standard TTL load, a negative going edge initiates the A/D conversion.
SHORT CYCLE	One standard LSTTL load, logic 1 for 12-bit resolution. Connect to "8-bit" or "10-bit" for 8- or 10-bit resolution.
$\overline{\text{ENABLE 1}}$, $\overline{\text{ENABLE 2}}$, $\overline{\text{ENABLE 3}}$, $\overline{\text{D11 ENABLE}}$, $\overline{\text{BUSY ENABLE}}$	One standard LSTTL load, a low level enables the 3-state output.
S/H CONTROL	TTL compatible, 10μA maximum input current. Logic 0 = Hold mode, Logic 1 = Sample (track) mode.
MUX ENABLE 2	TTL compatible, 2μA input current, logic 0 enables multiplexer 2 (channels 8-15).

DIGITAL OUTPUT SPECIFICATIONS

Parallel Data Outputs	5 standard TTL loads, positive true 3-state.
Serial Output	2 standard TTL loads, positive true, NRZ, time serial data output beginning with D11 (see Timing Diagram).
$\overline{\text{D11}}$	5 standard TTL loads, positive true, 3-state.
$\overline{\text{BUSY}}$	5 standard TTL loads, low during A/D conversion.
BUSY	5 standard TTL loads, high during A/D conversion, 3-state
CLOCK OUT	5 standard TTL loads, for synchronizing serial out data (see Timing Diagram).
Address Outputs (A0 - A3)	5 LSTTL or 2 standard TTL loads, positive true
DELAY OUT	5 standard TTL loads, high during delay period, triggered by Strobe input.
SIN/DIF	5 LSTTL or 2 standard TTL loads, high while addressing channels 0-7, low while addressing channels 8-15.

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS				
Resolution	12			Bits
Number of Analog Channels		16SIN/8DIF		
Throughput Rate (Normal mode)				
SDM854AG	33	35		kHz
SDM854BG	25	27		kHz
Throughput Rate (Overlap mode)				
SDM854AG	38	40		kHz
SDM854BG	27	29		kHz
ANALOG INPUTS				
ADC Input Voltage Ranges		0 to +10, ±5, ±10		V
Mux Input Voltage Range				
Absolute max without damage			±35	V
For linear operation			±15	V
Mux Input Impedance, OFF Channel			10^{11}	Ω
Mux Input Impedance, ON Channel		1.5	1.8	kΩ
Input Leakage, OFF Channel		0.02		nA
Output Leakage, All Channels Disabled		0.2		nA
Output Leakage with Input Overvoltage of				
+35V		1		nA
-35V		1		μA
TEMPERATURE STABILITY				
System Accuracy				
Unipolar		±15	±25	ppm/°C
Bipolar		±10	±20	ppm/°C
Linearity Drift			±2	ppm/°C of FSR
REFERENCE VOLTAGES				
Positive Output	+2.490	+2.500	+2.510	V
Positive Output Drift		±5	±10	ppm/°C
Negative Output	-6.0	-6.4	-6.8	V
Negative Output Drift		±15	±10	ppm/°C
ACCURACY				
Throughput Accuracy				
0 to +10V, ±5V, ±10V, AG			±0.048	% of FSR(1)
0 to +10V, ±5V, ±10V, BG			±0.024	% of FSR
Linearity				
AG			±0.024	% of FSR
BG			±0.012	% of FSR
Differential Linearity				
AG		±0.024	±0.048	% of FSR
BG		±0.012	±0.024	% of FSR
Quantizing Error			±0.012	% of FSR
System Gain Error(2)		±0.1	±0.3	%
System Offset Error(2)		±0.1	±0.3	% of FSR
Power Supply Sensitivity +15V		±0.0007		%/%ΔV
Power Supply Sensitivity -15V		±0.0007		%/%ΔV
Power Supply Sensitivity +5V		±0.001		%/%ΔV
DYNAMIC ACCURACY				
Sample/Hold Characteristics				
Aperture Time		100		nsec
Acquisition Time		10		μsec
Feedthrough (10V step)		±1.4		mV
OUTPUTS				
Digital Output Coding		Binary, Offset Binary, Two's Complement		
Serial Output Coding		Nonreturn to zero (NRZ)		
ADC Conversion Time(3)		25	30	μsec
Clock Frequency(3)		520		kHz
Delay(4)		15		μsec

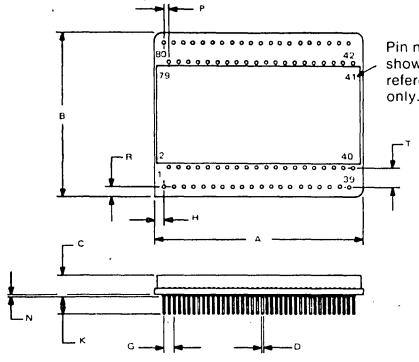
PARAMETER	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS				
Rated Voltage for Specified Accuracy	±14.5 +4.75	±15 +5	±15.5 +5.25	V V
Quiescent Current				
+15VDC		+10	+20	mA
-15VDC		-35	-50	mA
+5VDC		+170	+220	mA
Power Dissipation		1300	1750	mW
ENVIRONMENTAL				
Specification Temperature Range	-25		+85	°C
Operating Temperature Range	-40		+85	°C
Storage Temperature Range	-55		+125	°C

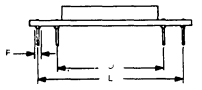
NOTES:
1. FSR means Full Scale Range (FSR is 20V for ±10V range).
2. Adjustable to zero.
3. Conversion time and clock frequency can be externally adjusted from 13μsec (fclock = 1.0MHz) to 110μsec (fclock = 118kHz). (Conv. times are for 12-bit resolution.)
4. Can be externally adjusted from 3μsec to 300μsec.

PIN DESIGNATIONS

NC	1	80	NC
MUX OUT HI	2	79	NC
NC	3	78	MUX OUT LO
CH7	4	77	CH15/RET7
CH6	5	76	CH14/RET6
CH5	6	75	CH13/RET5
CH4	7	74	CH12/RET4
CH3	8	73	CH11/RET3
CH2	9	72	CH10/RET2
CH1	10	71	CH9/RET1
CH0	11	70	CH8/RET0
MUX ENABLE 2	12	69	NC
MUX ENABLE I/A3 OUT	13	68	S/H IN
SIN/DIF	14	67	S/H OFFSET ADJUST
A2 OUT	15	66	S/H CONTROL
A1 OUT	16	65	+15VDC
A0 OUT	17	64	-15VDC
CLEAR	18	63	ANA COM
A0 IN	19	62	S/H OUT
A1 IN	20	61	-6.4V REF OUT
A2 IN	21	60	10V RANGE
A3 IN	22	59	BIPOLAR OFFSET
LOAD	23	58	20V RANGE
BUSY	24	57	+2.5V REF IN
DIG COM	25	56	ENABLE 2
SHORT CYCLE	26	55	+2.5V REF OUT
10-BIT RESOLUTION	27	54	ENABLE 1
8-BIT RESOLUTION	28	53	ENABLE 3
D0 LSB	29	52	SERIAL OUT
D1	30	51	CLOCK OUT
D2	31	50	CLOCK RATE ADJUST
D3	32	49	+5VDC
D4	33	48	STROBE
D5	34	47	DELAY ADJUST
D6	35	46	TRIG
D7	36	45	DELAY OUT
D8	37	44	D11
D9	38	43	BUSY
D10	39	42	BUSY ENABLE
D11 MSB	40	41	D11 ENABLE

MECHANICAL





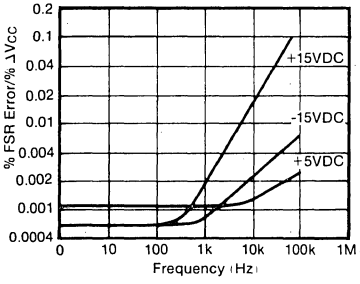
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	

NOTE:
Leads in true position within 0.015" (0.38mm) R at MMC at seating plane.

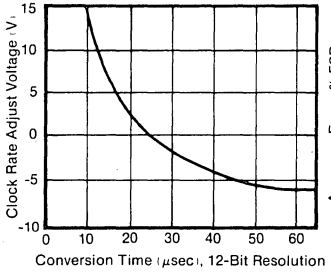
MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz)
MATING CONNECTOR:
2350MC (set of four 20-pin strips) or
0422MC (assembled unit)

TYPICAL PERFORMANCE CURVES

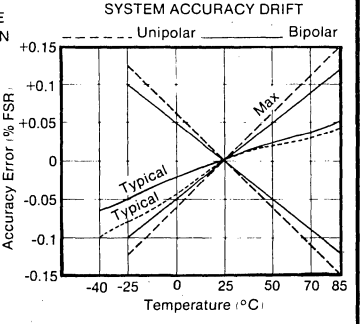
POWER SUPPLY REJECTION VS POWER SUPPLY RIPPLE FREQUENCY



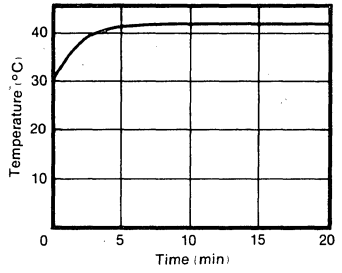
A/D CONVERSION TIME VS CLOCK RATE CONTROL VOLTAGE, 12-BIT RESOLUTION



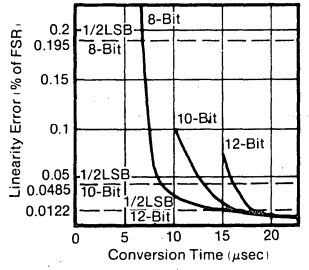
SYSTEM ACCURACY DRIFT



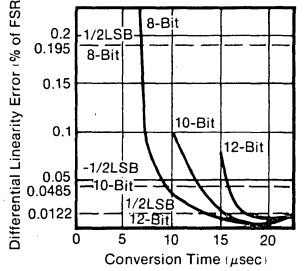
CASE TEMPERATURE VS TIME WITH NO HEAT SINK OR AIR FLOW



A/D CONVERTER LINEARITY ERROR VS CONVERSION TIME



A/D CONVERTER DIFFERENTIAL LINEARITY ERROR VS CONVERSION TIME



BURR-BROWN®

SDM856
SDM857

FOR A COMPLETE DATA SHEET, SEE PDS-402B

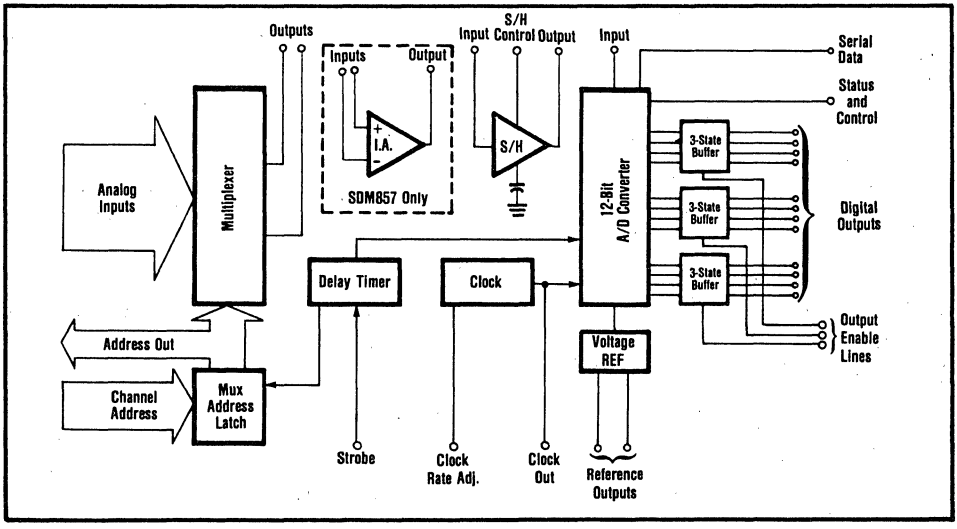
HYBRID DATA ACQUISITION SYSTEM

FEATURES

- 12-BIT, ±0.012% LINEARITY ERROR
- INSTRUMENT AMP OPTION
- LOW LEVEL INPUTS (SDM857)
- SELECTABLE 16 SINGLE, 8 DIFFERENTIAL INPUTS
- THREE-STATE OUTPUT BUFFERS
- THROUGHPUT RATES (SDM857 Overlap Mode)
  - 8-Bit Accuracy: 70kHz
  - 10-Bit Accuracy: 32kHz
  - 12-Bit Accuracy: 29kHz

DESCRIPTION

The SDM856 and SDM857 are complete data acquisition systems contained in a miniature 2.2" x 1.7" x 0.22" ceramic package. These systems offer all the functions available in large modular data acquisition systems and are available with an optional internal instrumentation amplifier (SDM857). Inputs as low as ±10mV can be accepted by the SDM857; thermocouples, strain gages, and other low level signal sensors don't require external signal conditioning. Both models are fully expandable from the basic 16 channel single-ended or 8 channel differential input capability. Digital resolution is 12 bits with accuracy of ±0.024% at a throughput rate of 29kHz (SDM856KG).



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SYSTEM DESCRIPTION

SDM857 contains all components necessary to multiplex and convert analog signals as low as ±10mV and as high as ±5V into equivalent digital outputs. Throughput sampling rates are from 29kHz (12-bit resolution) to 70kHz (8-bit resolution) in the overlap mode of operation. A complete low drift instrumentation amplifier allows selection of gains from 2 to 500 with one external resistor. SDM856 is identical to SDM857, but does not include the instrumentation amplifier. This provides the option of adding an external instrumentation amplifier for specific requirements such as high speed, digital programming, etc. Both models can be configured to accept either 8-channel differential or 16-channel single-ended signals and can be expanded almost without limit with external multiplexers. Three-state outputs are provided for easy interface to microprocessor and other bus-structured systems. Figure 1 illustrates all system components which are described in the following paragraphs.

ANALOG MULTIPLEXER

The analog multiplexer consists of two CMOS integrated circuits. Pin interconnects are used to select 16-channel single-ended or 8-channel differential operation. In single-ended operation the multiplexer can be used in a pseudo-differential mode by connecting the amplifier inverting input to common remote signal ground. Channel selection is made by an internally latched 3- or 4-bit binary word, for differential or single-ended operation respectively.

INSTRUMENTATION AMPLIFIER (SDM857 only)

Offering low drift and high accuracy, the internal instrumentation amplifier may be programmed by a single external resistor for gains from 2 to 500. With gain programming pins open, the gain is 2.

SAMPLE/HOLD

A complete stand-alone circuit, the sample/hold amplifier features buffered output, 10μsec acquisition time, and 100nsec aperture time.

Input, output, and mode control lines are brought out to separate pins. This allows maximum system flexibility for performing functions, such as automatic gain ranging, with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a 12-bit, 25μsec converter with 0.01% linearity error. Its features include positive and negative reference voltage outputs, external gain and offset adjustments, straight binary or two's complement output, serial data and clock outputs, status output, a short cycle feature, and a clock rate control for higher throughput rates at lower resolution or accuracy.

THREE-STATE OUTPUT BUFFERS

Digital outputs of the ADC are internally buffered by LSTTL three-state buffers. Three separate enable lines are brought out for easy interfacing to 4-, 8- or 16-bit data buses. $\overline{\text{MSB}}$ and BUSY are also buffered by separate three-state devices, each with its own enable line.

ADDRESS LATCH

Outputs of the 4-bit LSTTL register latch are connected to the address inputs of the multiplexer. This latch serves as an address storage register for the selected analog input. It may be loaded through 4 address inputs. Other inputs are LOAD and $\overline{\text{CLEAR}}$. The 3 least significant bits are used for 8-channel differential mode addressing.

DELAY TIMER

A delay timer allows settling time for the multiplexer, amplifier, and sample/hold circuits before conversion begins. The delay is adjustable over a wide range by use of an external resistor or capacitor. This allows for longer settling time of the instrumentation amplifier when operating at high gains, or shorter settling time for lower resolution operation.

CHANNEL EXPANSION

The number of analog input channels of the SDM856 and SDM857 can be easily increased by using Burr-Brown's MPC8D (8-channel differential) and MPC16S (16-channel single-ended) multiplexers. These are latch-free devices which contain internal binary decoding at TTL or MOS levels and may be integrated into a system with minimal external logic.

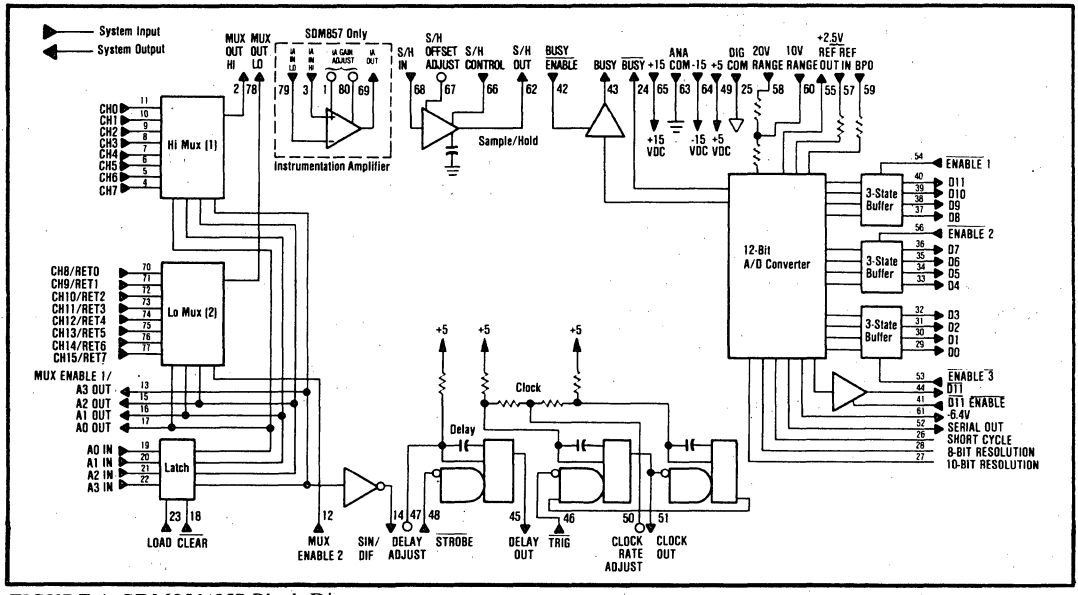


FIGURE 1. SDM856/857 Block Diagram.

SYSTEM PERFORMANCE

SDM856 and SDM857 are configured for random channel selection. With the addition of an external counter they can be configured to continuously sequence through all analog channels or sequence through all analog channels on command from an external trigger.

With the appropriate 4-bit (single-ended) or 3-bit (differential) channel address on the latch inputs, and DELAY OUT (pin 45) tied to the LOAD input (pin 23), a negative going edge is applied to the $\overline{\text{STROBE}}$ input (pin 48). This starts the delay timer, latches the multiplexer address, and allows the input signal to pass through the multiplexer, instrumentation amplifier and sample/hold and settle to its final value before starting the A/D conversion. The DELAY OUT signal (pin 45) is also connected to the $\overline{\text{TRIG}}$ input (pin 46) and the A/D conversion is initiated on the negative-going edge. The S/H CONTROL input (pin 66) is connected to $\overline{\text{BUSY}}$ (pin 24) so that the sample/hold is in the HOLD mode during the A/D conversion.

By using overlap programming the settling time effects of the analog multiplexer and instrumentation amplifier can be reduced, extending throughput sampling rates up to 29kHz for 12-bit and 70kHz for 8-bit resolution (ADC short-cycled). This mode of operation is most useful when converting low level inputs to accommodate the increased settling time of the instrumentation amplifier. Overlap programming is accomplished by connecting $\overline{\text{BUSY}}$ to $\overline{\text{STROBE}}$ and S/H CONTROL; DELAY OUT to LOAD and $\overline{\text{TRIG}}$. In this mode of operation the address of the next channel to be converted is latched and the output of the instrumentation amplifier allowed to settle to a new value during the present conversion.

DIGITAL INPUT SPECIFICATIONS

Address Inputs (A0 - A3)	One standard LSTTL load, positive true
Address Coding	4-bit binary
LOAD	One standard LSTTL load, positive true, address loaded on positive edge.
$\overline{\text{CLEAR}}$	One standard LSTTL load, negative true, low level clears address latch.
$\overline{\text{STROBE}}$	One standard LSTTL load, high-to-low transition triggers the delay timer.
$\overline{\text{TRIG}}$	One standard LSTTL load, a negative going edge initiates the A D conversion.
SHORT CYCLE	One standard LSTTL load, logic 1 for 12-bit resolution. Connect to "8-bit" or "10-bit" for 8- or 10-bit resolution.
$\overline{\text{ENABLE 1}}$, $\overline{\text{ENABLE 2}}$, $\overline{\text{ENABLE 3}}$, $\overline{\text{D11 ENABLE}}$, BUSY $\overline{\text{ENABLE}}$	One standard LSTTL load, a low level enables the 3-state output.
S/H CONTROL	TTL compatible, 10μA maximum input current. Logic 0 = Hold mode, Logic 1 = Sample (track) mode.
MUX ENABLE 2	TTL compatible, 2μA input current, Logic 0 enables multiplexer 2 (channels 8-15).

DIGITAL OUTPUT SPECIFICATIONS

Parallel Data Outputs	5 standard TTL loads, positive true, 3-state.
Serial Output	2 standard TTL loads, positive true, NRZ, time serial data output beginning with D11 (see Timing Diagram).
$\overline{\text{D11}}$	5 standard TTL loads, positive true, 3-state.
$\overline{\text{BUSY}}$	5 standard TTL loads, low during A D conversion.
BUSY	5 standard TTL loads, high during A D conversion, 3-state
CLOCK OUT	5 standard TTL loads, for synchronizing serial out data (see Timing Diagram).
Address Outputs (A0 - A3)	2 standard TTL loads, high during delay period, triggered by Strobe input.
DELAY OUT	5 standard TTL loads, high during delay period, triggered by Strobe input.
SIN/DIF	2 standard TTL loads, high while addressing channels 0-7, low while addressing channels 8-15.

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	SDM856/SDM857			
TRANSFER CHARACTERISTICS	MIN	TYP	MAX	UNITS
Resolution	12			Bits
Number of Analog Channels		16SIN/8DIF		
Throughput Rate (Normal Mode)				
SDM856JG	33	35		kHz
SDM856KG	25	27		kHz
SDM857JG	22	24		kHz
SDM857KG	18	20		kHz
Throughput Rate (Overlap mode)				
SDM856JG	38	40		kHz
SDM856KG	27	29		kHz
SDM857JG	38	40		kHz
SDM857KG	27	29		kHz
ANALOG INPUTS				
ADC Input Voltage Ranges		0 to +10, ±5, ±10		V
Mux Input Voltage Range				
Absolute max without damage			±20	V
For linear operation			±6	V
Mux Input Impedance, OFF Channel		$5 \times 10^9 \| 10$		Ω||pF
Mux Input Impedance, ON Channel		1800||7		Ω||pF
Amplifier Characteristics				
(SDM857 only)				
Input Impedance		$5 \times 10^9 \| 3$		Ω||pF
Gain Range	2		500	
Gain Equation		$G = 2 + (20k\Omega/R_{EXT}$[1])		
Input Bias Current at +25°C			±50	nA
0°C to +70°C		±1.1		nA/°C
Offset Current at +25°C			±20	nA
0°C to +70°C		±0.6		nA/°C
Input Offset Voltage		±0.1		mV
Input Offset Voltage Drift (G > 100)		±4	±6	μV/°C
Output Noise (10Hz − 10kHz)				
G = 100, R_S − 500Ω		400		μV, rms
Common-mode Rejection (DC)				
G = 2		90		dB
G = 1000		97		dB
Sample/Hold DC Characteristics				
Input Impedance		$10^{10} \| 3$		Ω||pF
Bias Current		50		nA
Output Offset Voltage		7		mV
REFERENCE VOLTAGES				
Output Voltage: Positive	+2.490	+2.500	+2.510	V
Negative	−6.0	−6.4	−6.8	V
Temperature Coefficient				
(each output)		±5	±10	ppm/°C
Current Available for External Loads				
Positive[2]	0			μA
Negative	−200			μA
ACCURACY				
Throughput Accuracy				
0 to +5V, ±5V ranges JG			±0.048	% of FSR[3]
0 to +5V, ±5V ranges KG			±0.024	% of FSR
0 to +20mV, ±10mV JG				
(SDM857 only)			±0.11	% of FSR
0 to +20mV, ±10mV KG				
(SDM857 only)			±0.08	% of FSR
Linearity (G = 1): JG			±0.024	% of FSR
KG			±0.012	% of FSR
Differential Linearity (G = 1): JG		±0.024	±0.048	% of FSR
KG		±0.012	±0.024	% of FSR
Quantizing Error			±0.012	% of FSR
System Gain Error[4]		±0.1	±0.3	%
System Offset Error[4]		±0.1	±0.3	% of FSR
Power Supply Sensitivity: +15V		±0.0007		%/%ΔV
−15V		±0.0007		%/%ΔV
+5V		±0.001		%/%ΔV

TEMPERATURE STABILITY	MIN	TYP	MAX	UNITS
System Accuracy Drift[5]: Unipolar			±25	ppm/°C
Bipolar			±20	ppm/°C
Linearity Drift			±2	ppm of FSR/°C
DYNAMIC ACCURACY				
Sample/Hold Characteristics				
Aperture Time		100		nsec
Acquisition Time		10		μsec
Feedthrough (10V step)		±1.4		mV
Amplifier Characteristics				
(SMD857 only)				
Amplifier CMRR at 60Hz, G = 2		90		dB
G = 500		95		dB
Amplifier Overload Recovery Time		200		μsec
OUTPUTS				
Digital Output Coding		Binary, Offset Binary, Two's Complement		
Serial Output Coding		Non-return to zero (NRZ)		
ADC Conversion Time[6]		25	30	μsec
Clock Frequency[6]		520		kHz
Delay[7]: SDM856		15		μsec
SDM857		30		μsec
POWER REQUIREMENTS				
Rated Voltage for Specified Accuracy	±14.5	±15	±15.5	V
	+4.75	+5	+5.25	V
Quiescent Current				
SDM856, +15VDC		+10	+20	mA
SDM856, −15VDC		−35	−50	mA
SDM856, +5VDC		+120	+140	mA
SDM857, +15VDC		+15	+25	mA
SDM857, −15VDC		−40	−55	mA
SDM857, +5VDC		+120	+140	mA
Power Dissipation: SDM856		1300	1750	mW
SDM857		1400	1900	mW
ENVIRONMENTAL				
Specification Temperature Range	0		+70	°C
Storage Temperature Range	−55		+100	°C

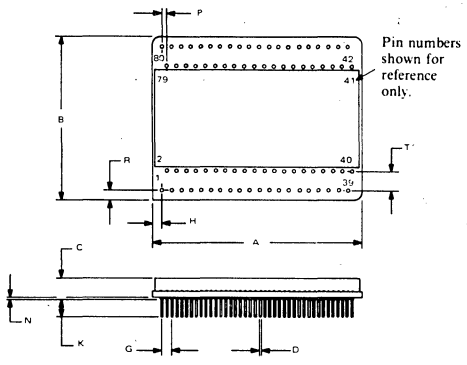
NOTES:
1. R_{EXT} is the external gain-setting resistor. (Connect between pins 1 and 80.)
2. External loading of the +2.5V reference output is not recommended.
3. FSR means Full Scale Range, e.g., FSR is 10V for ±5V range.
4. Adjustable to zero.
5. Includes gain, offset, and linearity drifts.
6. Conversion time and clock frequency can be externally adjusted from 13μsec (f_{clock} = 1.0MHz) to 110μsec (f_{clock} = 118kHz). Conversion times are for 12-bit resolution.
7. Can be externally adjusted from 3μsec to 300μsec.

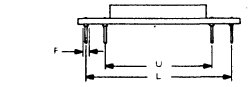
PIN DESIGNATIONS

IA GAIN ADJUST	*1	*80	IA GAIN ADJUST
MUX OUT HI	2	*79	IA IN LO
IA IN HI	*3	78	MUX OUT LO
CH7	4	77	CH15 RET 7
CH6	5	76	CH14 RET6
CH5	6	75	CH13 RET5
CH4	7	74	CH12 RET4
CH3	8	73	CH11 RET3
CH2	9	72	CH10 RET2
CH1	10	71	CH9 RET1
CH0	11	70	CH8 RET0
MUX ENABLE 2	12	*69	IA OUT
MUX ENABLE 1/A3 OUT	13	68	S/H IN
SIN DIF	14	67	S/H OFFSET ADJUST
A2 OUT	15	66	S/H CONTROL
A1 OUT	16	65	+15VDC
A0 OUT	17	64	-15VDC
$\overline{\text{CLEAR}}$	18	63	ANA COM
A0 IN	19	62	S/H OUT
A1 IN	20	61	-6.4V REF OUT
A2 IN	21	60	10V RANGE
A3 IN	22	59	BPO
$\overline{\text{LOAD}}$	23	58	20V RANGE
$\overline{\text{BUSY}}$	24	57	+2.5V REF IN
DIG COM	25	56	$\overline{\text{ENABLE 2}}$
SHORT CYCLE	26	55	+2.5V REF OUT
10-BIT RESOLUTION	27	54	$\overline{\text{ENABLE 1}}$
8-BIT RESOLUTION	28	53	$\overline{\text{ENABLE 3}}$
D0 (LSB)	29	52	SERIAL OUT
D1	30	51	CLOCK OUT
D2	31	50	CLOCK RATE ADJUST
D3	32	49	+5VDC
D4	33	48	$\overline{\text{STROBE}}$
D5	34	47	DELAY ADJUST
D6	35	46	$\overline{\text{TRIG}}$
D7	36	45	DELAY OUT
D8	37	44	$\overline{\text{D11}}$
D9	38	43	BUSY
D10	39	42	BUSY $\overline{\text{ENABLE}}$
D11 (MSB)	40	41	$\overline{\text{D11}}$ ENABLE

*For SDM857 only. Make no connection in SDM856.

MECHANICAL





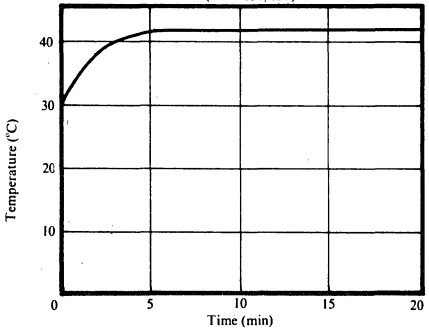
NOTE:
Leads in true position within .015" (.38mm)R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	

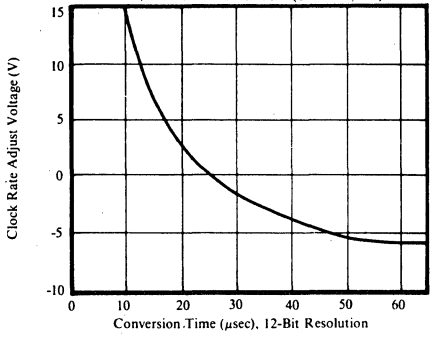
MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz.)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 2350MC (Set of four 20-pin strips) or 0422MC (assembled unit).

TYPICAL PERFORMANCE CURVES

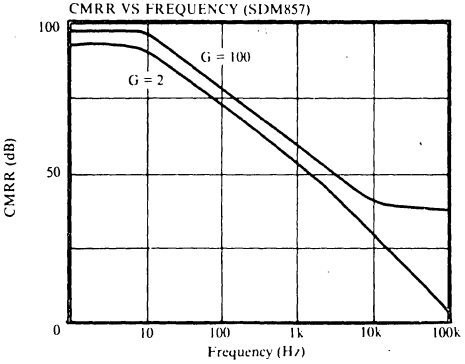
CASE TEMPERATURE VS TIME WITH NO HEAT SINK OR AIR FLOW (SDM856/857)



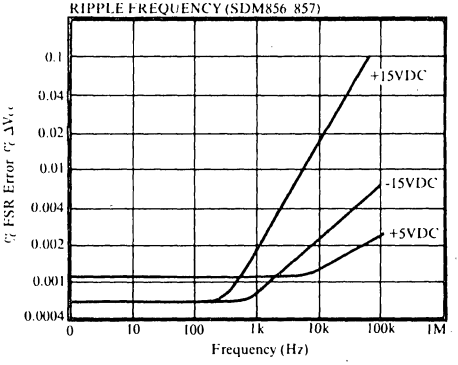
A/D CONVERSION TIME VS CLOCK RATE CONTROL VOLTAGE, 12-BIT RESOLUTION (SDM856/857)



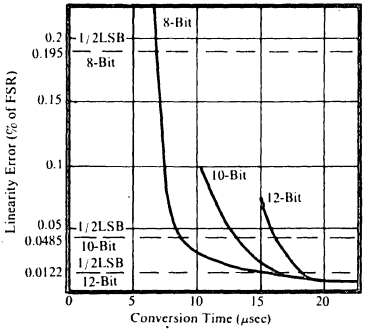
INSTRUMENTATION AMPLIFIER MULTIPLEXER CMRR VS FREQUENCY (SDM857)



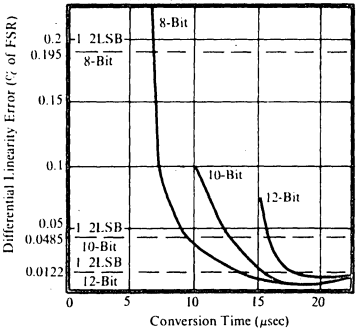
POWER SUPPLY REJECTION VS POWER SUPPLY RIPPLE FREQUENCY (SDM856 857)



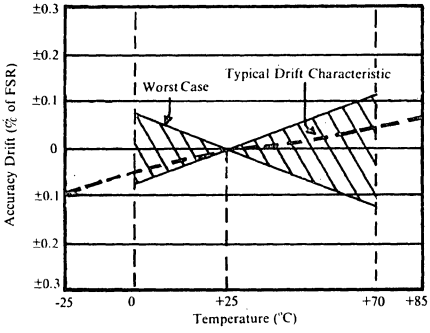
A/D CONVERTER LINEARITY ERROR VS CONVERSION TIME (SDM856 857)



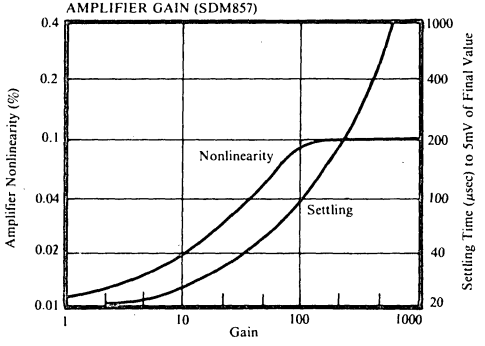
A/D CONVERTER DIFFERENTIAL LINEARITY ERROR VS CONVERSION TIME (SDM856 857)



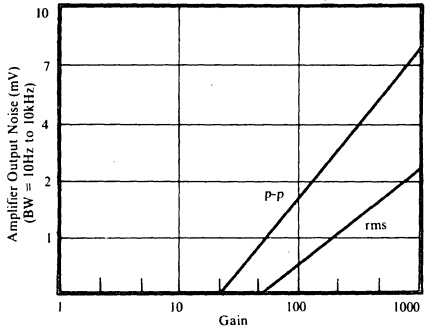
ACCURACY DRIFT VS TEMPERATURE (SDM856/857)



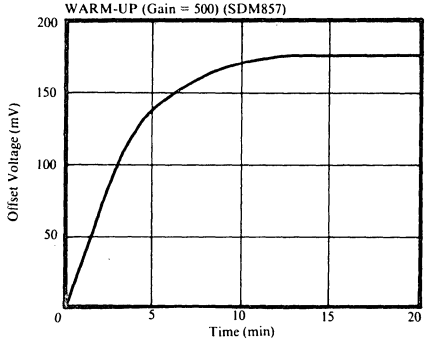
NONLINEARITY AND SETTLING TIME VS AMPLIFIER GAIN (SDM857)



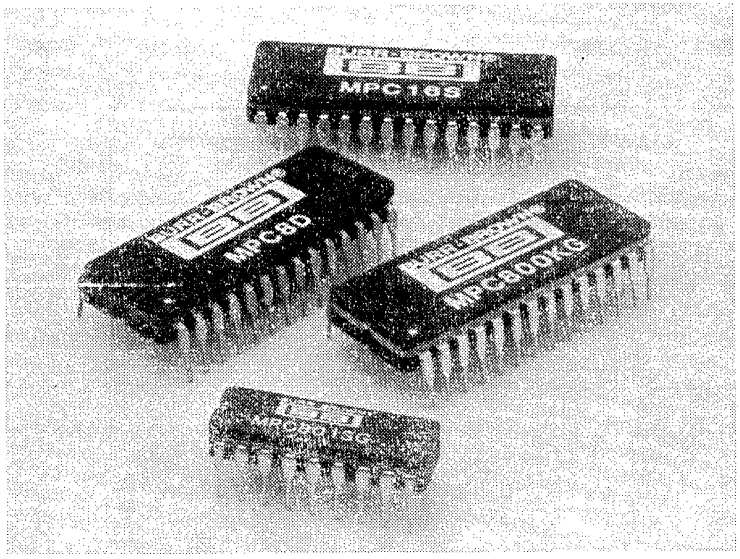
OUTPUT NOISE VS AMPLIFIER GAIN (SDM857)



INSTRUMENTATION AMPLIFIER OFFSET WARM-UP (Gain = 500) (SDM857)



MULTIPLEXERS



Burr-Brown multiplexers allow for a very low cost-per-channel figure in multiple-channel data conversion or data distribution systems. Two types are offered—a low-cost, high quality family of devices that range from 4 to 16 channels and can accommodate either single-ended or differential signals and a very-fast-switching family, again single-ended or differential, for high throughput rate applications. All are TTL-and CMOS-compatible, have input protection in excess of the maximum power supply voltages, and can be operated singly or in multitiered matrices.

SELECTION GUIDE

MULTIPLEXERS

These multiplexers are companion products for Burr-Brown's line of 12-and 16-bit A/D converters. One family offers protected inputs (MPC8S, 4D, 16S, 8D) while the other family offers high speed (MPC800 family).

MULTIPLEXERS								
Description	Model	Channels	Input Range (V)	On Resistance, max	Crosstalk (% of OFF Channel Signal)	Settling Time (to 0.01%)	Package	Page
Protected Inputs	MPC8S	8 single	±15	1.8kΩ	0.005	5μsec	DIP	9-3
	MPC4D	4 differential	±15	1.8kΩ	0.005	5μsec	DIP	9-3
	MPC16S	16 single	±15	1.8kΩ	0.005	7μsec	DIP	9-10
	MPC8D	8 differential	±15	1.8kΩ	0.005	7μsec	DIP	9-10
High Speed	MPC800KG	16 single or	±15	750Ω	0.004	800nsec	DIP	9-17
	MPC800SG	8 differential	±15	750Ω	0.004	800nsec	DIP	9-17
	MPC801KG	8 single or	±15	750Ω	0.004	800nsec	DIP	9-24
	MPC801SG	4 differential	±15	750Ω	0.004	800nsec	DIP	9-24

BURR-BROWN®

MPC4D
MPC8S

CMOS ANALOG MULTIPLEXERS

FEATURES

- LOW POWER CONSUMPTION
  CMOS analog switches
  15mW at 100kHz
- PROTECTS SIGNAL SOURCES
  Break-before-make switching
- HIGH THROUGHPUT RATE
- RELIABLE MONOLITHIC CONSTRUCTION

DESCRIPTION

The MPC8S is a single-ended monolithic 8-channel analog multiplexer and the MPC4D is a monolithic 4-channel differential input/output multiplexer. The digital and analog inputs are protected from overvoltage inputs that exceed either power supply. These CMOS devices feature self-contained binary channel address decoding and are compatible with TTL, or CMOS input levels. Channel interaction is eliminated during overvoltage conditions and also in the event of a power loss. They are packaged in a 16-pin DIP and dissipate typically 7.5mW.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

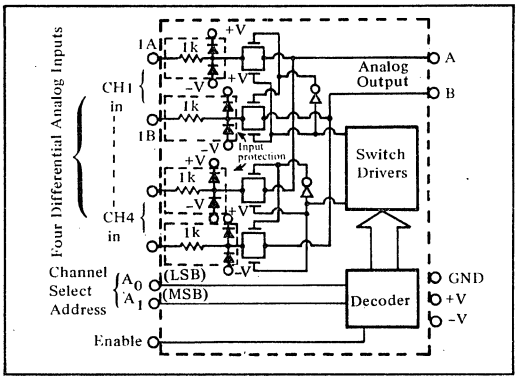
The MPC8S is a single-ended monolithic 8-channel analog multiplexer and the MPC4D is a monolithic differential input/output channel analog multiplexer constructed with failure-protected CMOS devices. Transfer accuracies of better than 0.01% can be achieved at sampling rates up to 200kHz from signal sources of up to ±10 volts amplitude.

These TTL/CMOS compatible devices feature self-contained binary channel address decoding. An ENABLE line is also made available which allows the user to individually enable an 8-channel group (MPC8S) or a 4-channel group (MPC4D) facilitating channel expansion in either single-mode or multitiered matrix configurations.

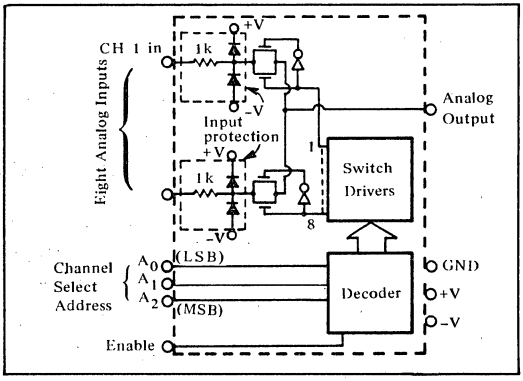
Digital and analog inputs are failure protected from either overvoltages that exceed the power supplies or from the loss of power.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, high OFF resistance, low feedthrough capacitance and fast settling time.

These devices are housed in compact 16-pin dual-in-line packages, and are specified for operation over a 0°C to +75°C temperature range. They are pin and package compatible with the 508/509 series.



FUNCTIONAL BLOCK DIAGRAM – MPC4D



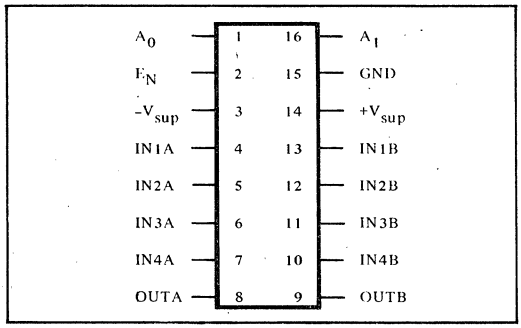
FUNCTIONAL BLOCK DIAGRAM – MPC8S

A_1	A_0	E_N	"On" Switch Pair
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

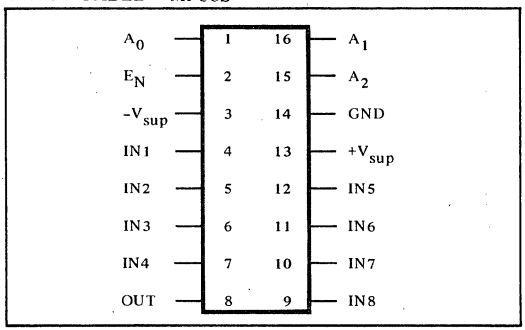
TRUTH TABLE –MPC4D

A_2	A_1	A_0	E_N	On Switch
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

TRUTH TABLE – MPC8S



MPC4D PIN DIAGRAM



MPC8S PIN DIAGRAM

SPECIFICATIONS

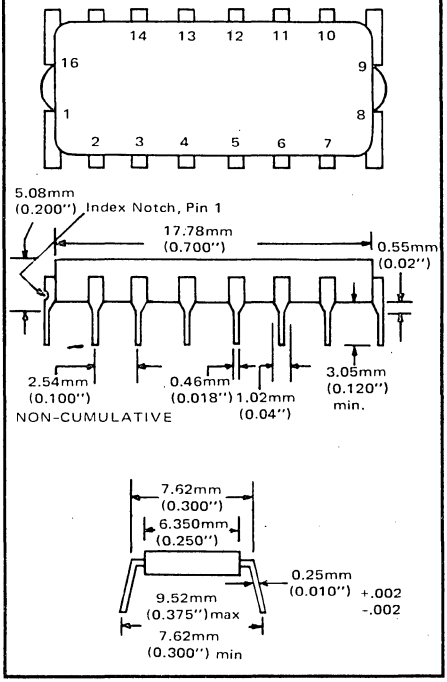
Typical for following conditions: V + = +15V, V - = -15V, $R_{source} \leq 1000\ \Omega$, $T_A = 25°C$ unless otherwise noted.

ELECTRICAL

MODELS	MPC8S	MPC4D	Units
INPUT			
ANALOG INPUT			
Voltage Range	±15		V
Maximum Overvoltage	+V supply +20 -V supply -20		V V
Current at Maximum Overvoltage per channel[1]	±18		mA
Number of Input Channels			
Single-ended	8		
Differential		4	
ON Characteristics			
ON Resistance (R_{ON})			
Typical	1.5		kΩ
Maximum	1.8		kΩ
R_{ON} Drift vs. Temperature (0°C to +75°C)	0.25		%/°C
R_{ON} Mismatch			
Channel-to-channel	50	50	Ω
Differential	N/A	50	Ω
Input Leakage (I_L)	0.1		nA
Input Leakage Drift	See Figure 9		
OFF Characteristics			
OFF Resistance	10^{11}		Ω
Output Leakage			
(All channels disabled)	0.2		nA
Input Leakage[6]	0.02		nA
Leakage Drift	See Figure 9		
Output Leakage with Input Overvoltage			
of +35V	1		nA
of -35V	1		μA
DIGITAL INPUTS			
Logic "0" (V_L)[1][2]	-V supply ≤ V_L < 0.8 at 1 nA		V
Logic "1" (V_H)[1][2]	+4V ≤ V_H ≤ + V supply at 1 nA		V
Channel Select	3 bit binary code - one of eight	2 bit binary code - one of four	
Enable	Logic "0" (low) disables all channels. Logic "1" (high) enables channel select to turn on selected channel.		
POWER REQUIREMENTS			
Rated Power Supply Voltages	±15		V
Supply Range			
+Supply	+10 to ±20		V
-Supply	-10 to -20		V
Supply Drain			
At 1 MHz Switching Speed	+4, -2		mA
AT 100 kHz Switching Speed	±0.5		mA
Typical Power Consumption DC to 10 kHz	7.5		mW
DYNAMIC CHARACTERISTICS			
Gain Error (20 MΩ load) maximum	0.01		%
Crosstalk[1]	0.005		% of OFF channel signal
Settling Time[4]			
To ±2mV ±(0.01%)	5		μs
To ±20mV ±(0.10%)	2		μs
Common-mode Rejection (minimum)	N/A	120	dB
Switching Time			
Turn ON	0.5		μs
Turn OFF	0.3		μs
Recovery Time from Input Overvoltage Pulse of 35V for 100 μsec			
To 0.01%	150		μs
To 0.10%	15		μs
OUTPUT			
Voltage Range	±15		V
Capacitance to Ground	25	12[5]	pF
Capacitance Mismatch	N/A	±10	%
TEMPERATURE			
Specification	0 to +75		°C
Storage	-65 to +150		°C

MPC4D AND MPC8S

16 Pin Ceramic Lead Frame TOP VIEW



NOTES:

1. Total power dissipation due to input overvoltage current flowing in the input protection circuitry must be limited to 0.75 watt for both (a) normal operation with power supplies turned on or (b) during a fault condition when the supplies are shorted to ground.
2. Maximum overvoltage is ±Vsupply ±4 volts at ±15 mA.
3. 20 volt peak-to-peak 1000 Hz sinewave; R_{SOURCE} = 1000Ω, same signal on all unused channels.
4. For 20 volts between switched channels, R_{SOURCE} = 1000Ω. See Figure 5 for settling time vs. source impedance (R_S).
5. From each side of MPC4D to ground.
6. Leakage measurement made with all OFF channel inputs fed in parallel to +20 volts.

DISCUSSION OF PERFORMANCE

Static Transfer Accuracy

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

SINGLE-ENDED MULTIPLEXER STATIC ACCURACY

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of 10^8 ohms or greater will keep resistive loading errors to 0.002% or less for 1000 ohm source impedances. A 10^6 ohm load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000 ohm source resistance will present less than 0.001% loading error and 10,000 ohm source resistance will increase source loading error to 0.01% with a 10^8 ohm load impedance.

Input resistive loading errors are determined by the following relationship: (see Figure 1)

Source and Multiplexer Resistive Loading Error

$$\in_{(R_S + R_{ON})} = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

INPUT OFFSET VOLTAGE

Bias current generates an input OFFSET voltage as result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10 nanoamperes will generate an offset voltage of 20μV if a 1000 ohm source is used, and 200μV if a 10,000 ohm source is used. In general, for the MPC8S, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_b + I_L)(R_{ON} + R_S)$$

where I_b = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{SOURCE} = Source resistance

DIFFERENTIAL MULTIPLEXER STATIC ACCURACY

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full scale ranges of 10 to 100 millivolts.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

The effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications. Refer to Figure 2.

LOAD (OUTPUT DEVICE) CHARACTERISTICS

- Use devices with very low bias current. Generaly, FET input amplifiers should be used for low level signals less than 50mV RSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be 10^{10} ohms or higher.

SOURCE CHARACTERISTICS

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC4D is used for multiplexing high-level signals of ±1 volt to ±10 volts full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

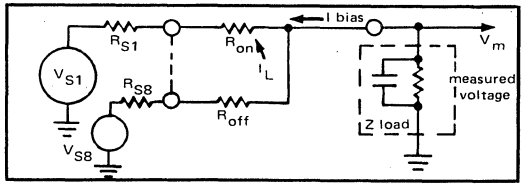


FIGURE 1: MPC8S Static Accuracy Equivalent Circuit.

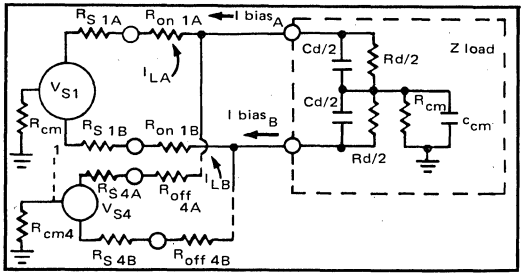


FIGURE 2: MPC4D Static Accuracy Equivalent Circuit.

SETTLING TIME

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C\frac{dV}{dt}$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figure 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. If effect, the amplitude of the transients seen at the source and load are:

$$dV_{load} = \frac{i}{C}\,dt$$

where $i = C\frac{dV}{dt}$ of the CMOS FET switches

C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in Figure 5. This graph shows the settling time for a 20 volt step change on the input. The settling time for smaller step changes on the input will be less than that shown in Figure 5.

SWITCHING TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10 volt signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the three (MPC4D) or seven (MPC8S) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel OFF resistance and junction capacitances in series with the R_{ON} and R_{SOURCE} impedances of the ON channel. Crosstalk is measured with a 20 volt pk-pk 1000 Hertz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in Figure 6.

COMMON-MODE REJECTION (MPC4D ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC4D, protection is provided for common-mode signals of ±20 volts above the power supply voltages with no damage to the analog switches.

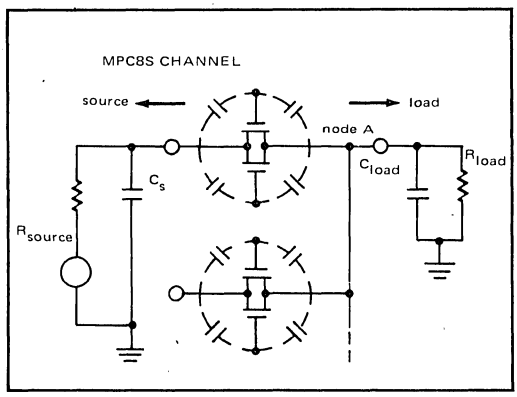


FIGURE 3: Settling Time Effects – MPC8S

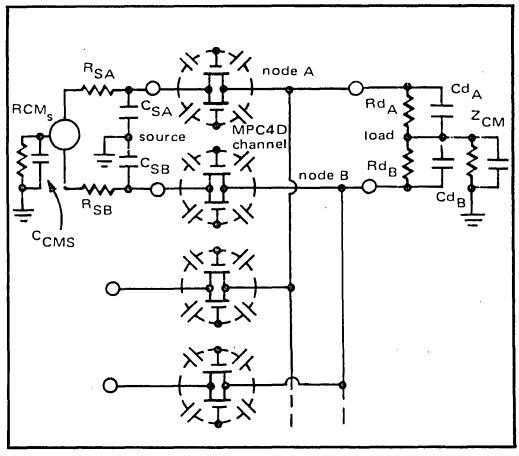


FIGURE 4: Settling & Common-Mode Effects – MPC4D.

The CMR of the MPC4D and Burr-Brown's model 3660 Instrumentation Amplifier is 120 dB at DC to 1 Hz with a 6 dB/octave rolloff to 70 dB at 1000 Hz. This measurement of CMR is shown in Figure 8 and is made with a Burr-Brown model 3660 Instrumentation Amplifier connected for a gain of 1000 and with source unbalance of 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

TYPICAL PERFORMANCE CURVES

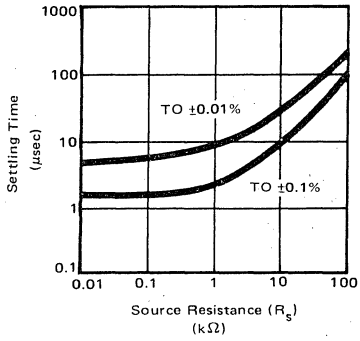


FIGURE 5. Settling time vs source resistance for 20 volt step change.

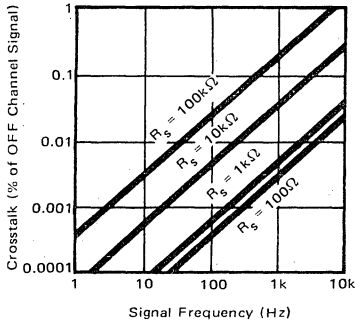


FIGURE 6. Crosstalk vs signal frequency.

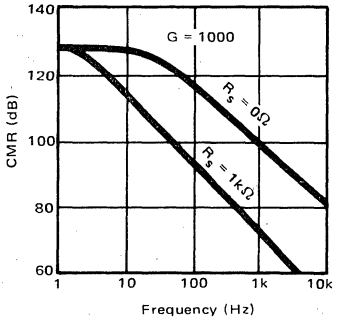


FIGURE 7. CMR vs frequency for Model 3660 IA and MPC4D (G = 1000).

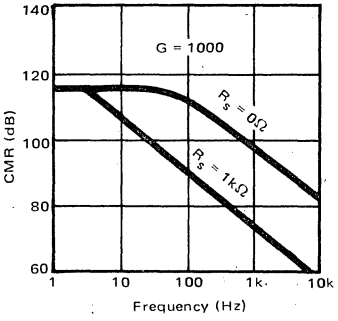


FIGURE 8. Combined CMR vs frequency for Model 3670 IA (G = 1000) and MPC4D.

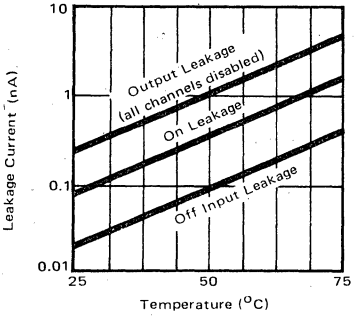


FIGURE 9. Leakage current vs temperature.

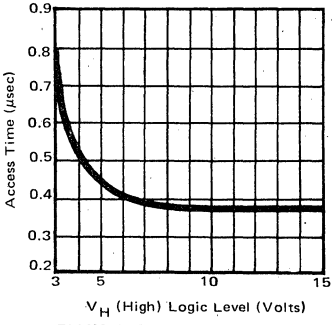


FIGURE 10. Access time vs logic level (high).

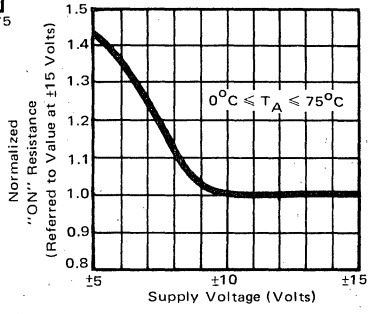


FIGURE 11. Normalized "ON" resistance vs supply voltage.

OPERATION & INSTALLATION INSTRUCTIONS

The ENABLE input, pin 2, is included for expansion of the number of channels on a single node as illustrated in Figure 12. With ENABLE line at a logic 1, the channel is selected by the 2 bit (MPC4D) or 3 bit (MPC8S) Channel Select Address (shown in the Truth Tables on page 9-4) **If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.**

If the +15 volt and/or -15 volt supply voltage is absent or shorted to ground, the MPC4D and MPC8S multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded (see Footnote 1, page 9-5).

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended. See Figure 10 (access time).

To preserve common-mode rejection of the MPC4D, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as closely as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

SINGLE-ENDED MULTIPLEXER (MPC8S)

Up to 32 channels (4 multiplexers) can be connected to a single node, or up to 64 channels using 9 MPC8S multiplexers on a two-tiered structure as shown in Figure 12 and 13.

DIFFERENTIAL MULTIPLEXER (MPC4D)

Single or multi-tiered configurations can be used to expand multiplexer channel capacity up to 32 channels using a 32 x 1 or 16 channels using a 4 x 4 configuration.

SINGLE NODE EXPANSION

The 32 x 1 configuration is simply eight MPC4D units tied to a single node. Programming is accomplished with a 5 bit counter, using the 2 LSB's of the counter to control Channel Address inputs A_0 and A_1 and the 3 MSB's of the counter to drive a 1 of 8 decoder. The 1 of 8 decoder then is used to drive the ENABLE inputs (pin 2) of the MPC4D multiplexers.

TWO TIER EXPANSION

Using a 4 x 4 2-tier structure for expansion to 16 channels, the programming is simplified A 4-bit counter output does not require a 1 of 8 decoder. The 2 LSB's of the counter drive the A_0 and A_1 inputs of the four first tier multiplexers and the 2 MSB's of the counter are applied to the A_0 and A_1 inputs of the second tier multiplexer.

Single vs. Multi-Tiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single node configuration, data cannot be taken from any channel, where as only one channel group is failed (4 or 8) in the multi-tiered configuration.

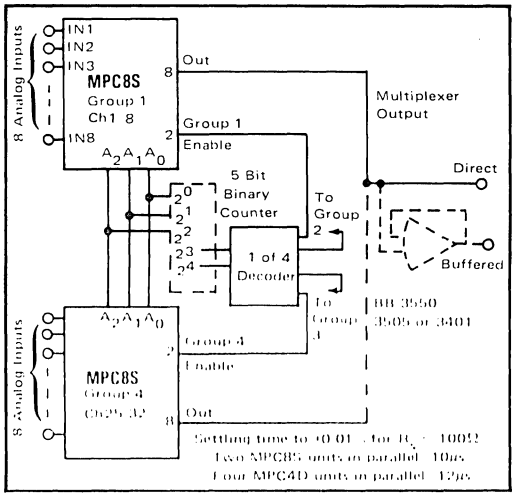


FIGURE 12. 32 Channel, Single-Tier Expansion.

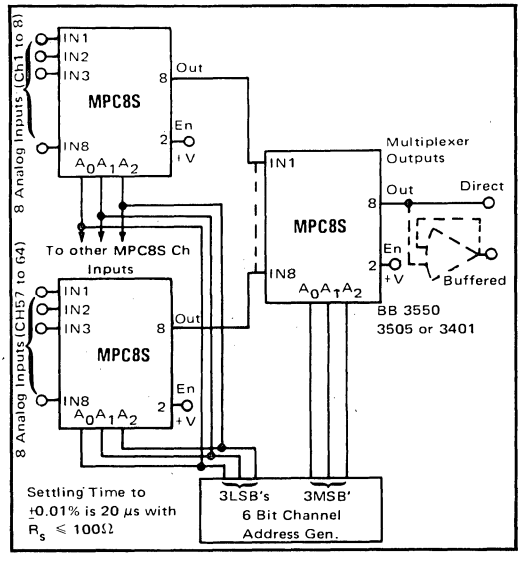


FIGURE 13. Channel Expansion Up to 64 Channels Using 8X8 Two-Tiered Expansion.

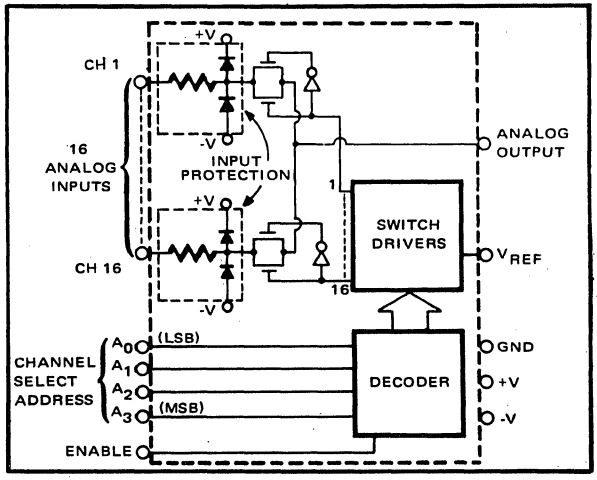
BURR-BROWN®

MPC8D
MPC16S

CMOS ANALOG MULTIPLEXERS

FEATURES

- LOW POWER CONSUMPTION
  CMOS analog switches
  15mW at 100kHz
  7.5mW standby power
- COMPACT DESIGN
  Self-contained with internal channel address decoder
  8-channel dual (MPC8D) for differential inputs or
  16-channel (MPC16S) for single-ended inputs
  28-pin 0.600 inch-wide space-saving package
- WILL NOT SHORT SIGNAL SOURCES
  Break-before-make switching
- FAST SWITCHING SPEEDS PROVIDE HIGH THROUGHPUT RATES
  7μsec settling to 0.01%
  3μsec settling to 0.1%
- WIDE SUPPLY RANGE
  ±10VDC to ±20VDC



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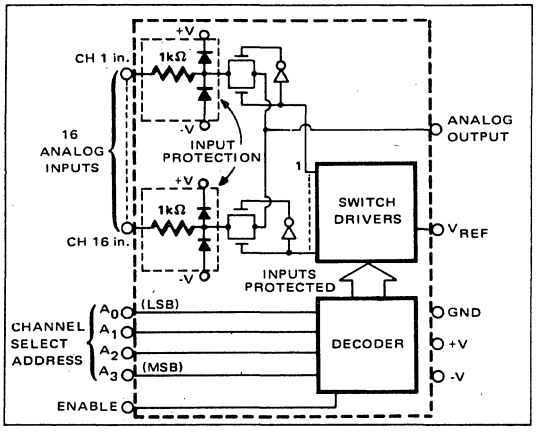
DESCRIPTION

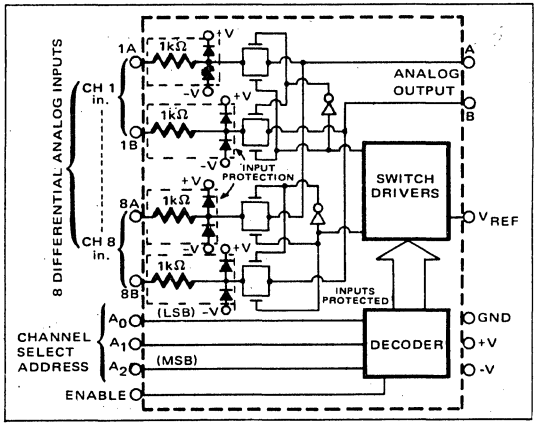
The MPC16S is a single-ended monolithic 16-channel analog multiplexer and the MPC8D is a monolithic dual 8-channel analog multiplexer constructed with failure protected CMOS devices. Transfer accuracies of better than 0.01% can be achieved at sampling rates up to 200kHz from signal sources of up to ±10V amplitude.

These TTL/CMOS compatible devices feature self-contained binary channel address decoding. An ENABLE line is also made available which allows the user to individually enable an 8-channel group (MPC8S) or a 4-channel group (MPC4D) facilitating channel expansion in either single-mode or multitiered matrix configurations.

Digital and analog inputs are failure protected from



FUNCTIONAL BLOCK DIAGRAM–MPC16S

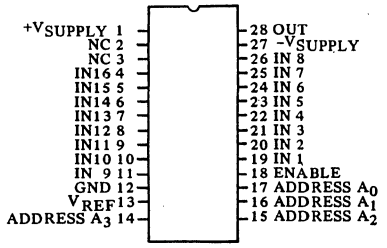


FUNCTIONAL BLOCK DIAGRAM–MPC8D

either overvoltages that exceed the power supplies or from the loss of power.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, high OFF resistance, low feedthrough capacitance and fast settling time.

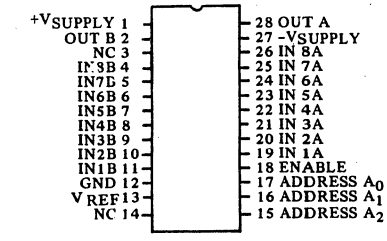
These devices are housed in compact 28-pin dual-in-line packages, and are specified for operation over a 0°C to +75°C temperature range. They are pin and package compatible with the 506/507 series.



MPC16S PIN DIAGRAM

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

TRUTH TABLE–MPC16S



MPC8D PIN DIAGRAM

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

TRUTH TABLE–MPC8D

SPECIFICATIONS

ELECTRICAL

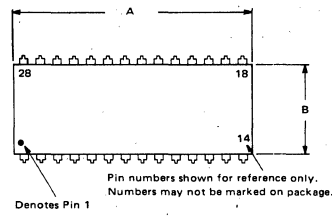
Typical for following conditions:

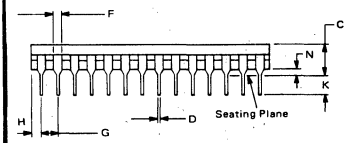
V+ = +15V, V- = -15V, $R_{source} \leq 1000\Omega$, $T_A = 25°C$ unless otherwise noted.

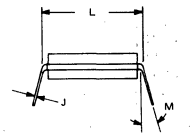
MODELS	MPC16S	MPC8D	UNITS
INPUT			
ANALOG INPUT			
Voltage Range	±15V		V
Maximum Overvoltage	+V supply +20		V
	-V supply -20		V
Current at Maximum Overvoltage per Channel(1)	±18		mA
Number of Input Channels			
Single-Ended	16		
Differential		8	
Reference Voltage Range(2)	+6 to +10		V
ON Characteristics			
ON Resistance (R_{ON})			
Typical	1.3		kΩ
Maximum	1.8		kΩ
R_{ON} Drift vs. Temperature (0°C to +75°C)	0.25		%/°C
R_{ON} Mismatch			
Channel-to-channel	50	50	Ω
Differential	N/A	50	Ω
Input Leakage (I_L)	1.0		nA
Input Leakage Drift	See Typical Performance Curves		
OFF Characteristics			
OFF Resistance	10^{11}		Ω
Output Leakage			
(all channels disabled)	0.2		nA
Input Leakage(3)	0.02		nA
Leakage Drift	See Typical Performance Curves		
Output Leakage with Input Overvoltage			
of +35V	1		nA
of -35V	1		μA
DIGITAL INPUTS			
Logic "0" (V_{IL})(1)(4)	-V supply ≤ V_L < 0.8 at 1nA		V
Logic "1" (V_{IH})(1)(4)	+4 ≤ V_H ≤ +V supply at 1nA		V
Channel Select	4-bit binary code - one of sixteen	3-bit binary code - one of eight	
Enable	Logic "0" (low) disables all channels. Logic "1" (high) enables channel select to turn on selected channel.		
POWER REQUIREMENTS			
Rated Power Supply Voltages	±15		V
Supply Range			
+Supply	+10 to +20		V
-Supply	−10 to −20		V
Supply Drain			
At 1MHz Switching Speed	+4, -2		mA
At 100kHz Switching Speed	±0.5		mA
Typical Power Consumption Dc to 10kHz	7.5		mW
DYNAMIC CHARACTERISTICS			
Gain Error (20MΩ load) maximum	0.01		%
Crosstalk(5)	0.005		% of OFF channel signal
Settling Time(6)			
To 2mV (0.01%)	7		μsec
To 20mV (0.10%)	3		μsec
Common-mode Rejection, min	N/A	120	dB
Switching Time			
Turn ON	0.5		μsec
Turn OFF	0.3		μsec
Recovery Time from Input Overvoltage Pulse of 35V for 100μsec			
To 0.01%	150		μsec
To 0.10%	15		μsec
OUTPUT			
Voltage Range	±15		V
Capacitance to Ground	50	30(7)	pF
Capacitance Mismatch	N/A	±10	%
TEMPERATURE			
Specification	0 to +75		°C
Storage	-65 to +150		°C

MECHANICAL

NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.







DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.360	1.470	34.54	37.34
B	.500	.550	12.70	13.97
C	— —	.200	— —	5.08
D	.015	.021	0.38	0.53
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.007	.013	0.18	0.33
K	.100	— —	2.54	— —
L	.600 BASIC		15.24 BASIC	
M	— —	15°	— —	15°
N	.020	.090	0.51	2.29

NOTES:
1. Total power dissipation due to input overvoltage current flowing in the input protection circuitry must be limited to one watt for both (a) normal operation with power supplies turned on or (b) during a fault condition when the supplies are shorted to ground.
2. Reference voltage controls noise immunity level. Normally not used (pin 13 left open).
3. Leakage measurement made with all OFF channel inputs fed in parallel to +20V.
4. Maximum overvoltage is $\pm V_{supply}$ ±4V at ±15mA. Logic levels specified are for V_{REF} pin 13) open. For V_{REF} = +10V, $V_{H\ MIN}$ = +6V.
5. 20V, pk-pk 1000Hz sinewave; R_{source} = 1000Ω, same signal on all unused channels.
6. For 20V between switched channels, R_{source} = 1000Ω. See Typical Performance Curves for settling time vs. source impedance (R_S).
7. From each side of MPC8D to ground.

DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and mulitplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.001% loading error and $10k\Omega$ source resistance will increase source loading error to 0.01% with a $10^8\Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\in_{(R_S + R_{ON})} = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\% \text{ where } \begin{array}{l} R_S = R_{source} \\ R_L = \text{load resistance} \\ R_{ON} = \text{multiplexer ON resistance.} \end{array}$$

Input Offset Voltage

Bias current generates an input Offset voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA will generate an offset voltage of $20\mu V$ if a 1000Ω source is used, and $200\mu V$ if a $10k\Omega$ source is used. In general, for the MPC16S, the Offset voltage at the output is determined by:

$$V_{OFFSET} = (I_b + I_L)(R_{ON} + R_{source}) \quad \text{where}$$

I_b = Bias current of device multiplexer is driving
I_l = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{source} = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC8D is used for multiplexing high-level signals of 1V to 10V full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

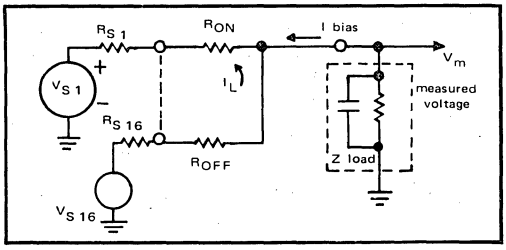


FIGURE 1. MPC16S State Accuracy Equivalent Circuit.

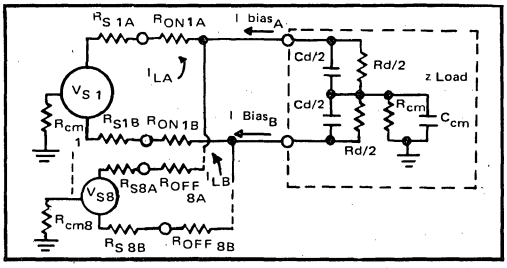


FIGURE 2. MPC8D Static Accuracy Equivalent Circuit.

SETTLING TIME

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C(dV/dt)$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figures 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$dV_{load} = (i/C)dt$
where $i = C(dV/dt)$ of the CMOS FET switches
C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in the Typical Performance Curves. This graph shows the settling time for a 20V step change on the input. The settling time for smaller step changes on the input will be less than that shown in the graph.

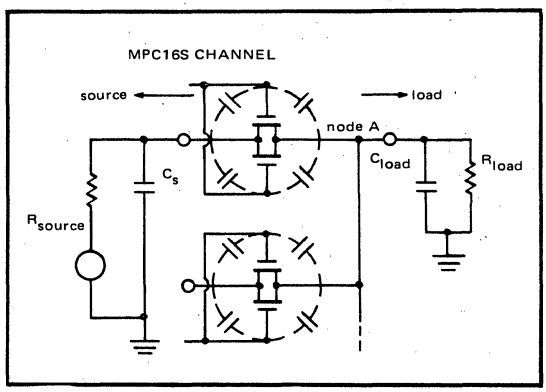


FIGURE 3. Settling Time Effects–MPC16S.

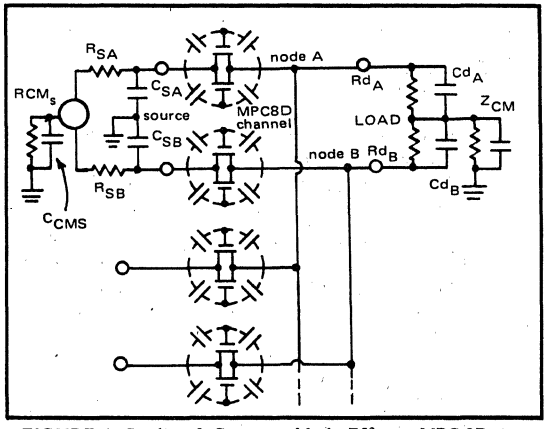


FIGURE 4. Settling & Common-Mode Effects– MPC-8D.

SWITCHING TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 7 (MPC8D) or 15 (MPC16S) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance, and junction capacitances in series with the R_{ON} and R_{source} impedances of the ON channel. Crosstalk is measured with a 20V, pk-pk 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION (MPC8D ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC8D, protection is provided for common-mode signals of ±20V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC8D and Burr-Brown's model 3660 instrumentation amplifier is 110dB at DC to 1Hz with a 6dB/octave rolloff to 70dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3660 instrumentation amplifier connected for a gain of 1000 and with source unbalance of 10kΩ, 1kΩ and no unbalance.

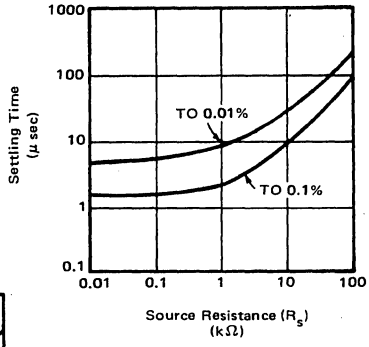
Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance.

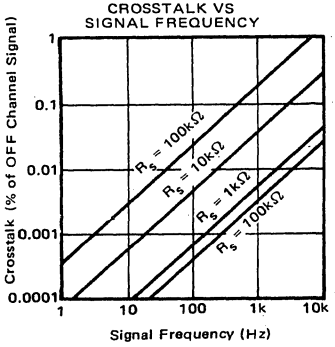
AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

TYPICAL PERFORMANCE CURVES

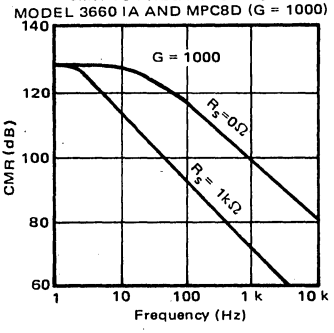
SETTLING TIME VS SOURCE RESISTANCE FOR 20V STEP CHANGE



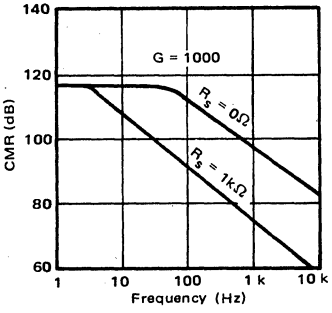
CROSSTALK VS SIGNAL FREQUENCY



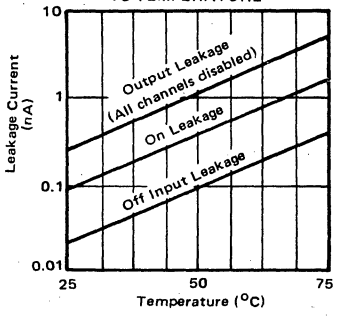
CMR VS FREQUENCY FOR MODEL 3660 IA AND MPC8D (G = 1000)



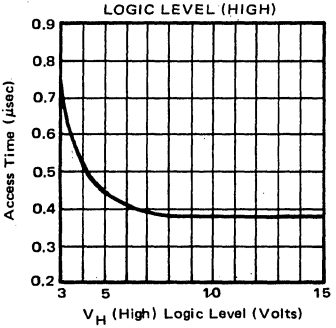
COMBINED CMR VS FREQUENCY FOR MODEL 3660 IA AND MPC8D (G = 1000)



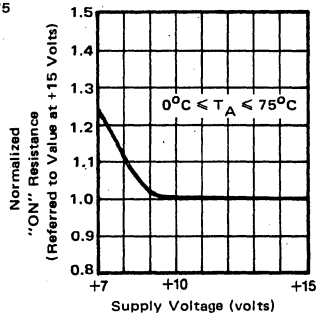
LEAKAGE CURRENT VS TEMPERATURE



ACCESS TIME VS LOGIC LEVEL (HIGH)



NORMALIZED "ON" RESISTANCE VS SUPPLY VOLTAGE



INSTALLATION & OPERATING INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the 3-bit (MPC8D) or 4-bit (MPC16S) Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15V and/or -15V supply voltage is absent or shorted to ground, the MPC8D and MPC16S multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded (see Note 1 of Electrical Specifications).

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended (see Typical Performance Curves, access time).

To preserve common-mode rejection of the MPC8D, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

SINGLE-ENDED MULTIPLEXER (MPC16S)

Up to 64 channels (4 multiplexers) can be connected to a single-node, or up to 256 channels using 17 MPC16S multiplexers on a two-tiered structure as shown in Figures 5 and 6.

DIFFERENTIAL MULTIPLEXER (MPC8D)

Single or multi-tiered configurations can be used to expand multiplexer channel capacity up to 64 channels using a 64 x 1 or 8 x 8 configuration.

SINGLE-NODE EXPANSION

The 64 x 1 configuration is simply eight MPC8D units tied to a single-node. Programming is accomplished with a 6-bit counter, using the 3LSB of the counter to control Channel Address inputs A_0, A_1 and A_2 and the 3MSB of the counter to drive an 8 of 1 decoder. The 8 of 1 decoder then is used to drive the ENABLE inputs (pin 18) of the MPC8D multiplexers.

TWO-TIER EXPANSION

Using an 8 x 8 two-tier structure for expansion to 64 channels, the programming is simplified. The 6-bit counter output does not require an 8 of 1 decoder. The 3LSB of the counter drive the A_0, A_1, and A_2 inputs of the eight first tier multiplexers and the 3MSB of the counter are applied to the A_0, A_1, and A_2 inputs of the second tier multiplexer.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced Offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one channel group is failed (8 or 16) in the multitiered configuration.

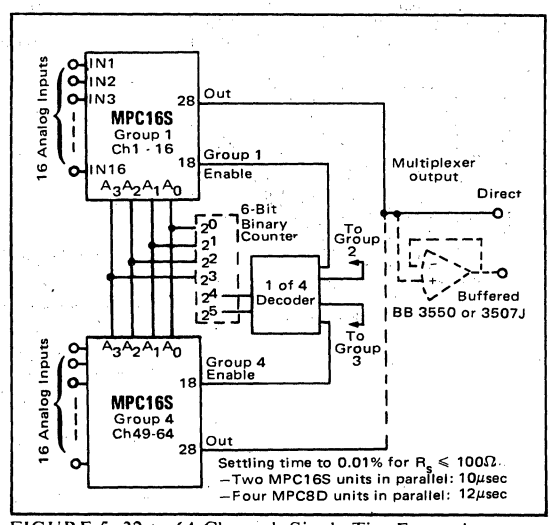


FIGURE 5. 32 to 64 Channel, Single-Tier Expansion.

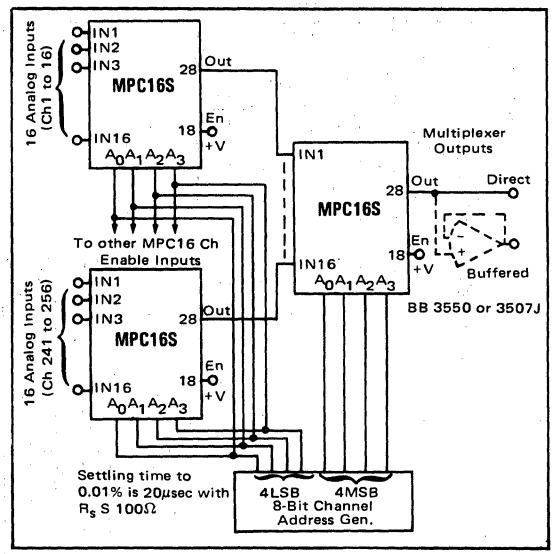


FIGURE 6. Channel Expansion up to 256 Channels Using 16 x 16 Two-Tiered Expansion.

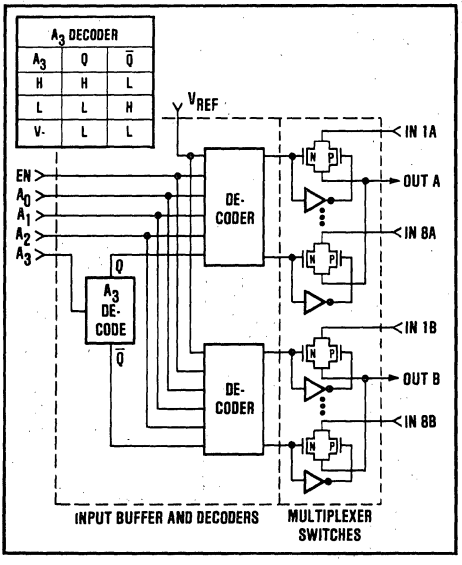
BURR-BROWN®

MPC800

High Speed
CMOS ANALOG MULTIPLEXER

FEATURES

- HIGH SPEED
  - 100nsec access time
  - 800nsec settling to 0.01%
  - 250nsec settling to 0.1%
- USER-PROGRAMMABLE
  - 16-channel single-ended or
  - 8-channel differential
- SELECTABLE TTL or CMOS COMPATIBILITY
- WILL NOT SHORT SIGNAL SOURCES
  - Break-before-make switching
- SELF-CONTAINED WITH INTERNAL CHANNEL ADDRESS DECODER
- 28-PIN HERMETIC DUAL-IN-LINE PACKAGE



DESCRIPTION

The MPC800 is a high speed multiplexer that is user-programmable for 16-channel single-ended operation or 8-channel differential operation and for TTL or CMOS compatibility.

The MPC800 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC800KG for operation from 0°C to +75°C and the MPC800SG for operation from -55°C to +125°C.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

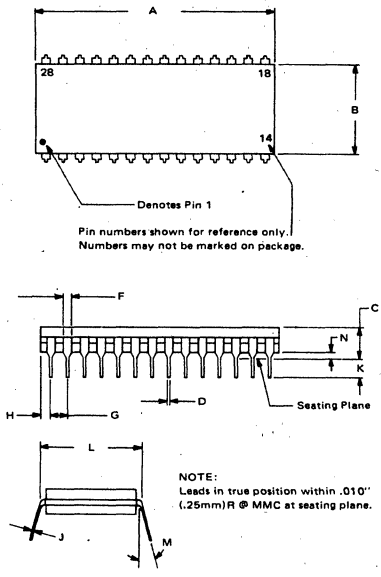
SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±V_{CC} = 15V, unless otherwise noted.

MODEL	MPC800KG, MPC800SG			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
ANALOG INPUT				
Voltage Range	-15		+15	V
Maximum Overvoltage	-V_{CC} -2		+V_{CC}, +2	V
Number of Input Channels				
Differential	8			
Single-Ended	16			
Reference Voltage Range(1)	6		10	V
ON Characteristics(2)				
ON Resistance (R_{ON}) at +25°C		620	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature	See Typical Performance Curves			
R_{ON} Mismatch		< 10		Ω
ON Channel Leakage		0.04		nA
Over Temperature Range		0.6	100	nA
ON Channel Leakage Drift	See Typical Performance Curves			
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0.01		nA
Over Temperature Range		0.38	50	nA
OFF Channel Input Leakage Drift	See Typical Performance Curves			
OFF Channel Output Leakage		0.035		nA
Over Temperature Range		0.48	100	nA
OFF Channel Output Leakage Drift	See Typical Performance Curves			
Output Leakage (All channels disabled)(3)		0.02		nA
Output Leakage with Overvoltage				
+16V Input		< 0.35		mA
-16V Input		< 0.65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL(4)				
Logic "0" (V_{AL})			0.8	V
Logic "1" (V_{AH})	2.4			V
I_{AH}		0.05	1	μA
I_{AL}		4	25	μA
TTL Input Overvoltage	-6		6	V
CMOS				
Logic "0" (V_{AL})			0.3V_{REF}	V
Logic "1" (V_{AH})	0.7 V_{REF}			V
CMOS Input Overvoltage	-2		+V_{CC} +2	V
Address A_3 Overvoltage	-V_{CC} -2		+V_{CC} +2	V
Digital Input Capacitance		5		pF
Channel Select(5)				
Single-Ended	4-bit binary code one of 16			
Differential	3-bit binary code one of 8			
Enable	Logic "0" inhibits all channels			
POWER REQUIREMENTS				
Over Temperature Range				
Rated Supply Voltage		±15		V
Maximum Voltage Between Supply Pins			33	V
Total Power Dissipation		525		mW
Allowable Total Power Dissipation(6)			1200	mW
Supply Drain (+25°C)				
At 1MHz Switching Speed		+35, -39		mA
At 100kHz Switching Speed		+25, -29		mA
DYNAMIC CHARACTERISTICS				
Gain Error		< 0.0003		%
Cross Talk(7)	See Typical Performance Curves			
T_{OPEN} (Break before make delay)		20		nsec
Access Time at +25°C		100	150	nsec
Over Temperature Range		120	200	nsec
Settling Time(8)				
to 0.1% (20mV)		250		nsec
to 0.01% (2mV)		800		nsec
Common-Mode Rejection (Differential)				
DC		> 125		dB
60Hz		> 75		dB
Channel Input Capacitance, C_S (off)		2.5		pF
Channel Output Capacitance, C_O (off)		18		pF
Input to Output Capacitance, C_{DS} (off)		0.02		pF

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.360	1.475	34.54	37.47
B	.500	.550	12.70	13.97
C	—	.220	—	5.59
D	.015	.021	0.38	0.53
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.007	.013	0.18	0.33
K	.100	—	2.54	—
L	.600 BASIC		15.24 BASIC	
M	—	15°	—	15°
N	.020	.090	0.51	2.29

PIN CONFIGURATION

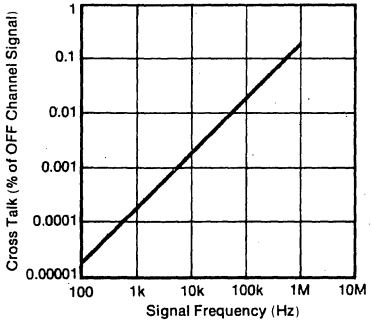
TOP VIEW

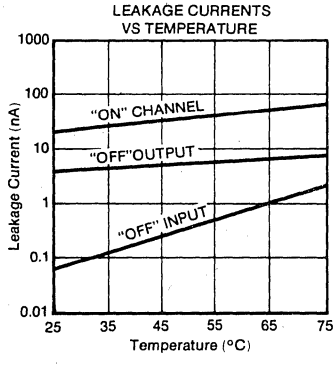
+V_{CC}	1	28	OUT A
OUT B	2	27	-V_{CC}
NC	3	26	IN 8/8A
IN16/8B	4	25	IN7/7A
IN15/7B	5	24	IN6/6A
IN14/6B	6	23	IN5/5A
IN13/5B	7	22	IN4/4A
IN12/4B	8	21	IN3/3A
IN11/3B	9	20	IN2/2A
IN10/2B	10	19	IN1/1A
IN9/1B	11	18	ENABLE
GND	12	17	A_0
V_{REF}	13	16	A_1
A_3	14	15	A_2

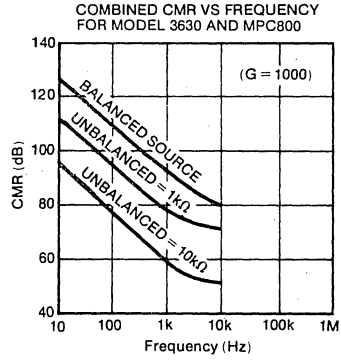
MODEL	MPC800KG, MPC800SG			
PARAMETER	MIN	TYP	MAX	UNITS
TEMPERATURE				
MPC800KG				
Specification	0		+75	°C
Storage	-65		+150	°C
MPC800SG				
Specification	-55		+125	°C
Storage	-65		+150	°C

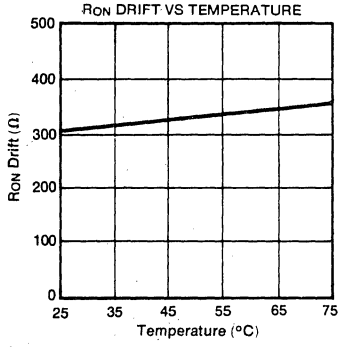
NOTES:
1. Reference voltage controls noise immunity, normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility.
2. $V_{IN} = \pm 10V$, $I_{OUT} = 100\mu A$.
3. Single-ended mode.
4. Logic levels specified for V_{REF} (pin 13) open.
5. For single-ended operation, connect output A (pin 28) to output B (pin 2) and use A_3 (pin 14) as an address line. For differential operation connect A_3 to $-V_{CC}$.
6. Derate 8mW/°C above $T_A = +75°C$.
7. 10V, p-p, sine wave on all unused channels. See Typical Performance Curves.
8. For 20V step input to ON channel, into 1kΩ load.

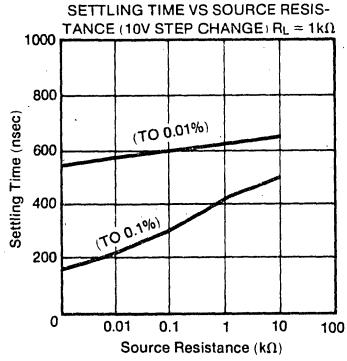
TYPICAL PERFORMANCE CURVES











DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current, and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

RESISTIVE LOADING ERRORS

The source and load impedances will determine the ON resistance loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.002% loading error and 10kΩ source resistance will increase source loading error 0.02% with a $10^8\Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\epsilon\ (R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = R_{source}
R_L = Load Resistance
R_{ON} = Multiplexer ON resistance

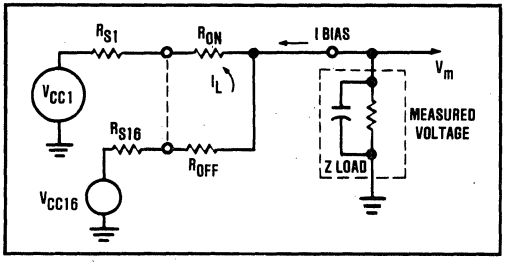


FIGURE 1. MPC800 Static Accuracy Equivalent Circuit (Single-ended Operation).

Input Offset Voltage

Bias and leakage currents generate an input Offset voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA, a leakage current of 1nA, and an ON resistance of 700Ω will generate an offset voltage of 19μV if a 1000Ω source is used, and 118μV if a 10kΩ source is used. In general, for the MPC800 the Offset voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_{source}) \text{ where}$$

I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{source} = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

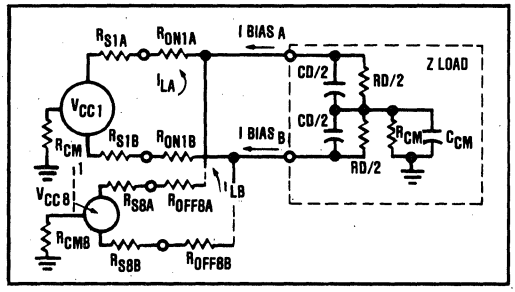


FIGURE 2. MPC800 Static Accuracy Equivalent Circuit (Differential Operation).

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC800 is used for multiplexing high level signals of 1V to 10V full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low level signal applications

SETTLING TIME

Settling time is the time required for the multiplexer to reach and maintain an output within a specified error band of its final value in response to a step input. The settling time of the MPC800 is primarily due to the channel capacitance and a combination of resistances which include the source and load resistances.

If the parallel combination of the source and load resistance times the total channel capacitance is kept small, then the settling time is primarily affected by internal RC's. For the MPC800 the internal capacitance is approximately 20pF differential or 40pF single-ended. With external capacitance neglected, the time constant of source resistance in parallel with load resistance and the internal capacitance should be kept less than 40nsec. This means the source resistance should be kept to less than 2kΩ (assume high load resistance) to maintain fast settling times.

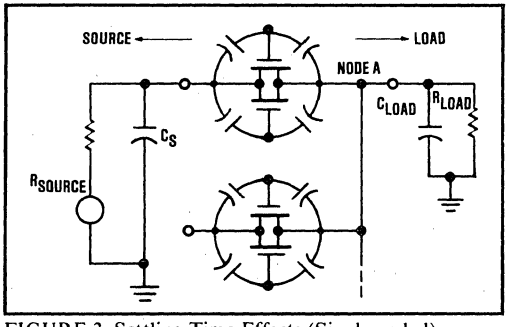


FIGURE 3. Settling Time Effects (Single-ended).

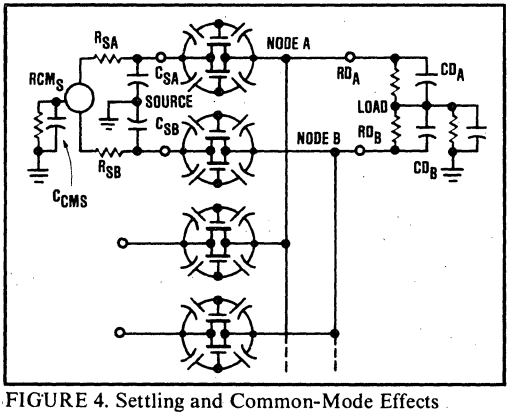


FIGURE 4. Settling and Common-Mode Effects (Differential).

ACCESS TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 7 differential or 15 single-ended OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance, and junction capacitances in series with the R_{ON} and R_{source} impedances of the ON channel. Crosstalk is measured with a 20V, pk-pk, 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION (DIFFERENTIAL MODE ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. Protection is provided for common-mode signals of ±2V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC800 and Burr-Brown's model 3630 Instrumentation Amplifier is 120dB at DC to 10Hz with a 6dB/octave rolloff to 80dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3630 instrumentation amplifier connected for a gain of 1000 and with source unbalance of 10kΩ, 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch.

- Load impedance mismatch.
- Multiplexer impedance and leakage current mismatch.
- Load and source common-mode impedance.

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

INSTALLATION & OPERATING INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to logic 1.

For the best settling time, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pullup resistors are recommended.

To preserve common-mode rejection of the MPC800 use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

LOGIC LEVELS

The logic level is user-programmable as either TTL-compatible by leaving the V_{REF} (pin 13) open or CMOS-compatible by connecting the V_{REF} to V_{DD} (CMOS supply voltage).

16-CHANNEL SINGLE-ENDED OPERATION

To use the MPC800 as a 16-channel single-ended multiplexer, output A (pin 28) is connected to output B (pin 2) to form a single output, then all four address lines (A_0, A_1, A_2 and A_3) are used to address the correct channel.

The MPC800 can also be used as a dual 8-channel single-ended multiplexer by not connecting output A and B, but then only one channel in one of the multiplexers can be addressed at a time.

8-CHANNEL DIFFERENTIAL OPERATION

To use the MPC800 as an 8-channel differential multiplexer, connect address line A_3 to $-V_{CC}$ then use the remaining three address lines (A_0, A_1 and A_2) to address the correct channel. The differential inputs are the pairs of A_1 and B_1, A_2 and B_2, etc.

TRUTH TABLES

MPC800 used as 16-channel single-ended multiplexer or 8-channel dual multiplexer.

USE A_3 AS DIGITAL ADDRESS INPUT					"ON" CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	NONE	NONE
H	L	L	L	L	1A	NONE
H	L	L	L	H	2A	NONE
H	L	L	H	L	3A	NONE
H	L	L	H	H	4A	NONE
H	L	H	L	L	5A	NONE
H	L	H	L	H	6A	NONE
H	L	H	H	L	7A	NONE
H	L	H	H	H	8A	NONE
H	H	L	L	L	NONE	1B
H	H	L	L	H	NONE	2B
H	H	L	H	L	NONE	3B
H	H	L	H	H	NONE	4B
H	H	H	L	L	NONE	5B
H	H	H	L	H	NONE	6B
H	H	H	H	L	NONE	7B
H	H	H	H	H	NONE	8B

For 16-channel single-ended function, tie "out A" to "out B, for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

MPC800 used as 8-channel differential multiplexer.

A_3 CONNECT TO $-V_{CC}$				"ON" CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

CHANNEL EXPANSION

Single-tier Expansion

Up to four MPC800's can be connected to a single node to form a 64-channel single-ended multiplexer or up to eight MPC800's can be connected to two nodes to form a 64-channel differential multiplexer. Programming is accomplished with a six-bit address and a 1 of 4 decoder for 64-channel single-ended expansion (see Figure 5) or an eight-bit address and a 1 of 8 decoder for 64-channel

differential expansion. The decoder drives the enable inputs of the MPC800, turning on only one multiplexer at a time.

Two-tier Expansion

Up to seventeen MPC800's can be connected in a two-tier structure to form a 256-channel single-ended multiplexer (see Figure 6) or up to nine MPC800's can be connected in a two-tier structure to form a 64-channel differential multiplexer. Programming is accomplished with a 8-bit address.

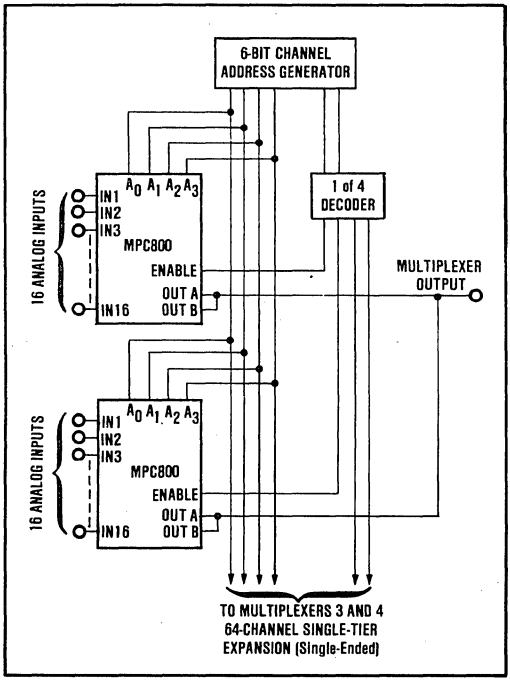


FIGURE 5. 32- to 64-Channel, Single-tier Expansion.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced Offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one-channel group is failed (8 or 16) in the multitiered configuration.

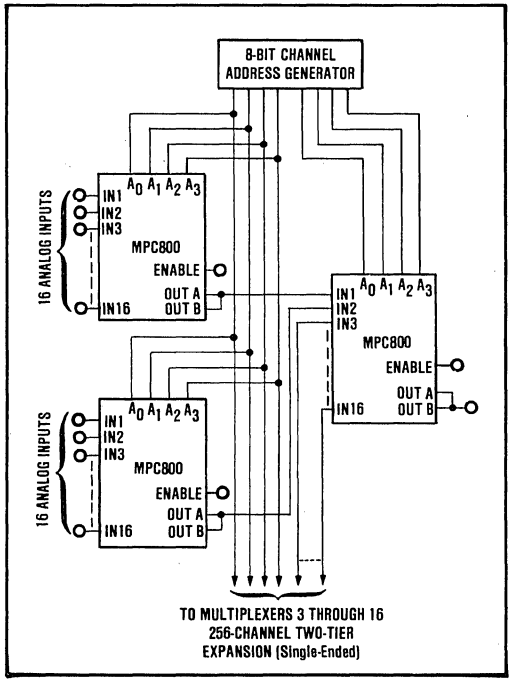


FIGURE 6. Channel Expansion up to 256 Channels using 16 x 16 Two-tiered Expansion.

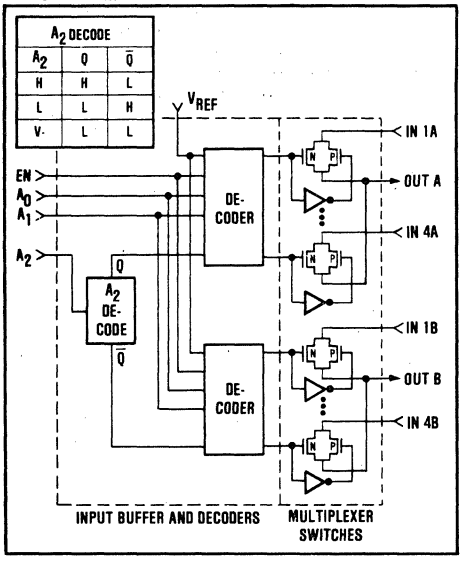
BURR-BROWN®

MPC801

High Speed CMOS ANALOG MULTIPLEXER

FEATURES

- HIGH SPEED
  - 80nsec access time
  - 800nsec settling to 0.01%
  - 250nsec settling to 0.1%
- USER-PROGRAMMABLE
  - 8-channel single-ended or
  - 4-channel differential
- SELECTABLE TTL or CMOS COMPATIBILITY
- WILL NOT SHORT SIGNAL SOURCES
  - Break-before-make switching
- SELF-CONTAINED WITH INTERNAL CHANNEL ADDRESS DECODER
- 18-PIN HERMETIC DUAL-IN-LINE PACKAGE



DESCRIPTION

The MPC801 is a high speed multiplexer that is user-programmable for 8-channel single-ended operation or 4-channel differential operation and for TTL or CMOS compatibility.

The MPC801 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC801KG for operation from 0°C to +75°C and the MPC801SG for operation from -55°C to +125°C.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

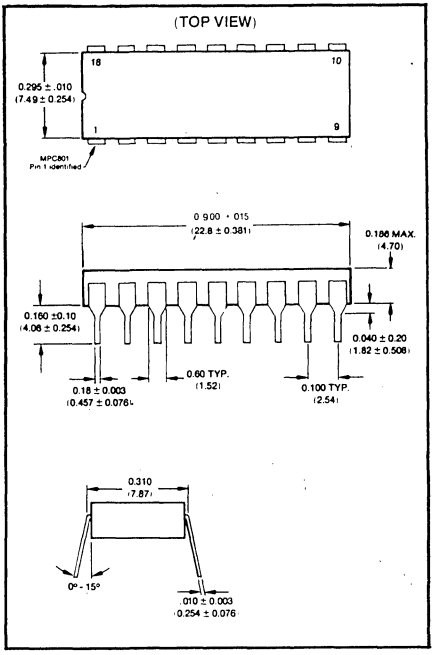
SPECIFICATIONS

ELECTRICAL

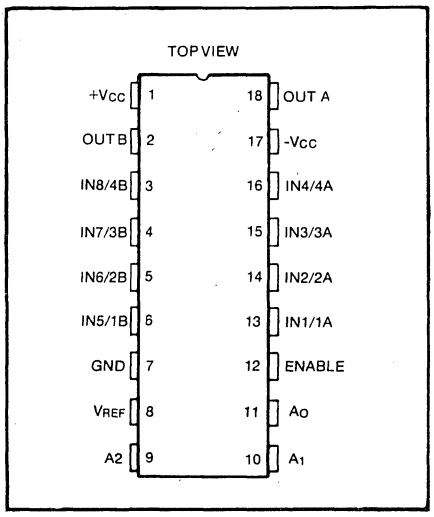
At T_A = +25°C and ±V_{CC} = 15VDC unless otherwise noted.

MODEL	MPC801KG, MPC801SG			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
ANALOG INPUT				
Voltage Range	-15		+15	V
Maximum Overvoltage	-V_{CC} -2		+V_{CC} +2	V
Number of Input Channels				
Differential	4			
Single-Ended	8			
Reference Voltage Range(1)	6		10	V
ON Characteristics(2)				
ON Resistance (R_{ON}) at +25°C		500	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature	See Typical Performance Curves			
R_{ON} Mismatch		< 10		Ω
ON Channel Leakage		0.1		nA
Over Temperature Range		0.3	50	nA
ON Channel Leakage Drift	See Typical Performance Curves			
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0.05		nA
Over Temperature Range		0.6	50	nA
OFF Channel Input Leakage Drift	See Typical Performance Curves			
OFF Channel Output Leakage		0.1		nA
Over Temperature Range		0.30	50	nA
OFF Channel Output Leakage Drift	See Typical Performance Curves			
Output Leakage (All channels disabled)(3)		0.02		nA
Output Leakage with Overvoltage				
+16V Input		< 0.35		mA
-16V Input		< 0.65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL(4)				
Logic "0" (V_{AL})			0.8	V
Logic "1" (V_{AH})	2.4			V
I_{AH}		0.05	1	µA
I_{AL}		4	20	µA
TTL Input Overvoltage	-6		6	V
CMOS				
Logic "0" (V_{AL})			0.3V_{REF}	V
Logic "1" (V_{AH})	0.7 V_{REF}			V
CMOS Input Overvoltage	-2		+V_{CC} +2	V
Address A_2 Overvoltage	-V_{CC} -2		+V_{CC} +2	V
Digital Input Capacitance		5		pF
Channel Select(5)				
Single-Ended	3-bit binary code one of 8			
Differential	2-bit binary code on of 4			
Enable	Logic "0" inhibits all channels			
POWER REQUIREMENTS				
Over Temperature Range				
Rated Supply Voltage		±15		V
Maximum Voltage Between Supply Pins			33	V
Total Power Dissipation		360		mW
Allowable Total Power Dissipation(6)			725	mW
Supply Drain (+25°C)				
At 1MHz Switching Speed		+14, -12.5		mA
At 100kHz Switching Speed		+12.5,-12.5		mA
DYNAMIC CHARACTERISTICS				
Gain Error		< 0.0003		%
Cross Talk(7)	See Typical Performance Curves			
T_{OPEN} (Break before make delay)		20		nsec
Access Time at 25°C		80	125	nsec
Over Temperature Range		110	150	nsec
Settling Time(8)				
to 0.1% (20mV)		250		nsec
to 0.01% (2mV)		800		nsec
Common-Mode Rejection (Differential)				
DC		> 125		dB
60Hz		> 75		dB
OFF Channel Input Capacitance, C_S (off)		1.9		pF
OFF Channel Output Capacitance, C_O (off)		10		pF
OFF Input to Output Capacitance, C_{DS} (off)		0.02		pF

MECHANICAL



PIN CONFIGURATION

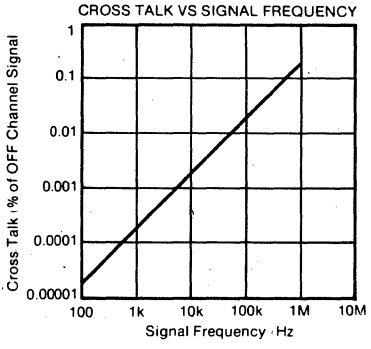


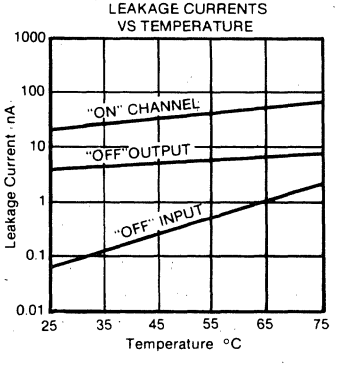
ELECTRICAL (CONT)

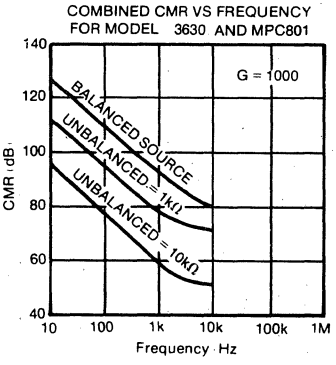
MODEL	MPC801KG, MPC801SG			
PARAMETER	MIN	TYP	MAX	UNITS
TEMPERATURE				
MPC801KG				
Specification	0		+75	°C
Storage	-65		+150	°C
MPC801SG				
Specification	-55		+125	°C
Storage	-65		+150	°C

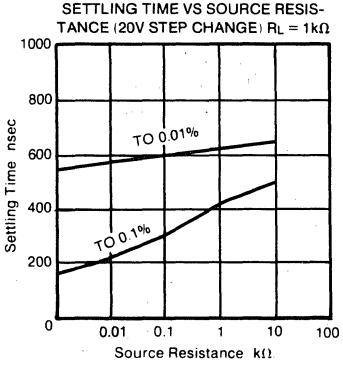
NOTES:
1. Reference voltage controls noise immunity, normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility.
2. $V_{IN} = \pm 10V$, $I_{OUT} = 100\mu A$.
3. Single-ended mode.
4. Logic levels specified for V_{REF} (pin 8) open.
5. For single-ended operation, connect output A (pin 18) to output B pin 2, and use A_2 (pin 9) as an address line. For differential operation connect A_2 to $-V_{CC}$.
6. Derate 8mW/°C above $T_A = +75°C$.
7. 10V, p-p. sine wave on all unused channels. See Typical Performance Curves.
8. For 20V step input to ON channel, into 1kΩ load.

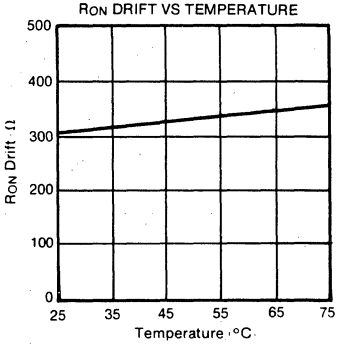
TYPICAL PERFORMANCE CURVES











DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current, and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

RESISTIVE LOADING ERRORS

The source and load impedances will determine the ON resistance loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.002% loading error and $10k\Omega$ source resistance will increase source loading error 0.02% with a $10^8\Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\epsilon\,(R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\% \text{ where}$$

$R_S = R_{source}$
R_L = Load resistance
R_{ON} = Multiplexer ON resistance.

Input Offset Voltage

Bias and leakage currents generate an input Offset voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA, a leakage current of 1nA, and an ON resistance of 700Ω will generate an offset voltage of $19\mu V$ if a 1000Ω source is used, and $118\mu V$ if a $10k\Omega$ is used. In general, for the MPC801 the Offset voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_{source}) \text{ where}$$

I_B = Bias Current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{source} = Source resistance.

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

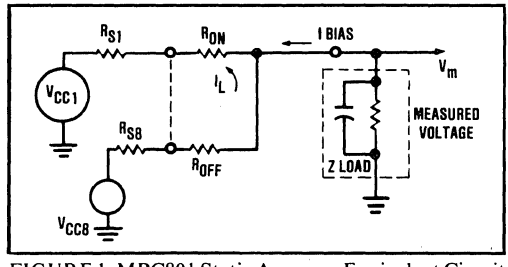


FIGURE 1. MPC801 Static Accuracy Equivalent Circuit (Single-ended Operation).

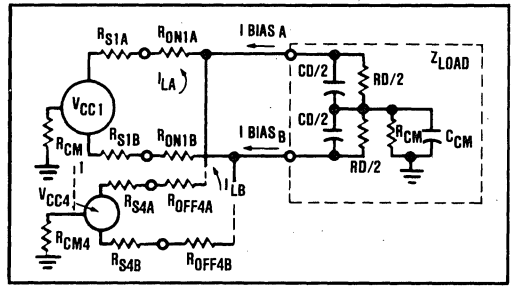


FIGURE 2. MPC801 Static Accuracy Equivalent Circuit (Differential Operation).

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC801 is used for multiplexing high level signals of 1V to 10V full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low level signal applications

SETTLING TIME

Settling time is the time required for the multiplexer to reach and maintain an output within a specified error band of its final value in response to a step input. The settling time of the MPC801 is primarily due to the channel capacitance and a combination of resistances which include the source and load resistances.

If the parallel combination of the source and load resistance times the total channel capacitance is kept small, then the settling time is primarily affected by internal RC's. For the MPC801 the internal capacitance is approximately 10pF differential or 20pF single-ended.

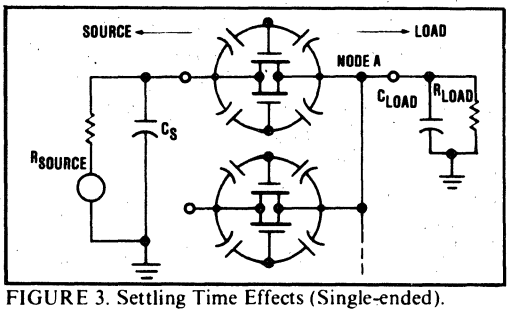


FIGURE 3. Settling Time Effects (Single-ended).

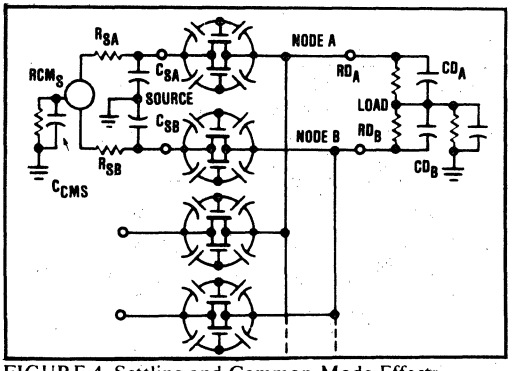


FIGURE 4. Settling and Common-Mode Effects (Differential).

With external capacitance neglected, the time constant of source resistance in parallel with load resistance and the internal capacitance should be kept less than 40nsec. This means the source resistance should be kept to less than 4kΩ (assume high load resistance) to maintain fast settling times.

ACCESS TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 3 differential or 7 single-ended OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance, and junction capacitances in series with the R_{ON} and R_{source} impedances of the ON channel. Crosstalk is measured with a 20V, pk-pk, 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION (DIFFERENTIAL MODE ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. Protection is provided for common-mode signals of ±2V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC801 and Burr-Brown's model 3630 Instrumentation Amplifier is 120dB at DC to 10Hz with a 6dB/octave rolloff to 80dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3630 instrumentation amplifier connected for a gain of 1000 and with source unbalance of 10kΩ, 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch.
- Load impedance mismatch.
- Multiplexer impedance and leakage current mismatch.

- Load and source common-mode impedance.

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

INSTALLATION & OPERATING INSTRUCTIONS

The ENABLE input, pin 12, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to logic 1.

For the best settling time, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pullup resistors are recommended.

To preserve common-mode rejection of the MPC801 use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

LOGIC LEVELS

The logic level is user-programmable as either TTL-compatible by leaving the V_{REF} (pin 8) open or CMOS-compatible by connecting the V_{REF} to V_{DD} (CMOS supply voltage).

8-CHANNEL SINGLE-ENDED OPERATION

To use the MPC801 as an 8-channel single-ended multiplexer, output A (pin 18) is connected to output B (pin 2) to form a single output, then all three address lines (A_0, A_1, and A_2) are used to address the correct channel.

The MPC801 can also be used as a dual channel single-ended multiplexer by not connecting output A and B, but then only one channel in one of the multiplexers can be addressed at a time.

4-CHANNEL DIFFERENTIAL OPERATION

To use the MPC801 as an 4-channel differential multiplexer, connect address line A_2 to $-V_{CC}$ then use the remaining two address lines (A_0 and A_1) to address the correct channel. The differential inputs are the pairs of A_1 and B_1, A_2 and B_2, etc.

TRUTH TABLES

MPC801 used as 8-channel single-ended multiplexer or 4-channel dual multiplexer.

USE A_2 AS DIGITAL ADDRESS INPUT				"ON" CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	NONE
H	L	L	H	2A	NONE
H	L	H	L	3A	NONE
H	L	H	H	4A	NONE
H	H	L	L	NONE	1B
H	H	L	H	NONE	2B
H	H	H	L	NONE	3B
H	H	H	H	NONE	4B

For 8-channel single-ended function, tie "out A" to "out B", for dual 4-channel function use the A_2 address pin to select between MUX A and MUX B, where MUX A is selected with A_2 low.

MPC801 used as 4-channel differential multiplexer.

A_2 CONNECT TO $-V_{CC}$			"ON" CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	NONE	NONE
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

CHANNEL EXPANSION

Single-tier Expansion

Up to eight MPC801's can be connected to a single node to form a 64-channel single-ended multiplexer or up to eight MPC801's can be connected to two nodes to form a 32-channel differential multiplexer. Programming is accomplished with a 6-bit address and a 1 of 8 decoder (Figure 5). The decoder drives the enable inputs of the MPC801, turning on only one multiplexer at a time.

Two-tier Expansion

Up to nine MPC801's can be connected in a two-tier structure to form a 64-channel single-ended multiplexer (Figure 6) or up to five MPC801's can be connected in a two-tier structure to form a 16-channel differential multiplexer. Programming is accomplished with a 6-bit address.

SINGLE VS MULTITIERED CHANNEL EXPANSION

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced Offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-

node configuration, data cannot be taken from any channel, whereas only one channel group is failed (4 or 8) in the multitiered configuration.

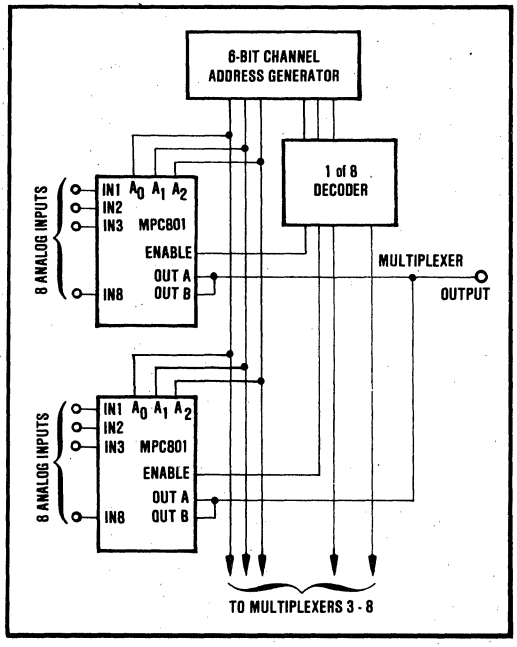


FIGURE 5. 64-Channel, Single-Tier, Single-Ended Expansion.

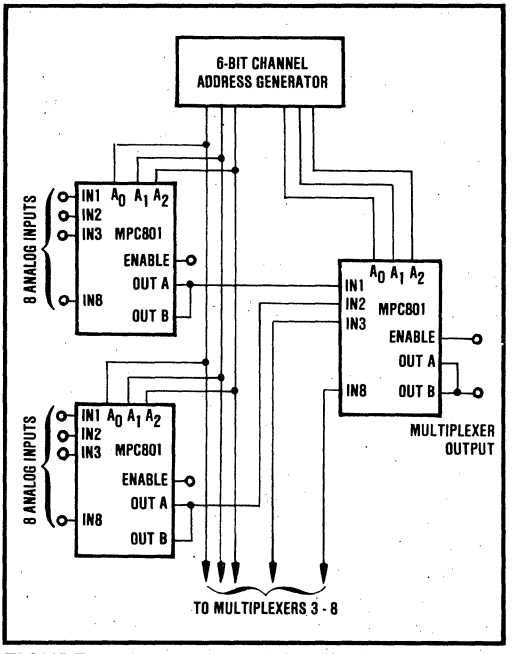
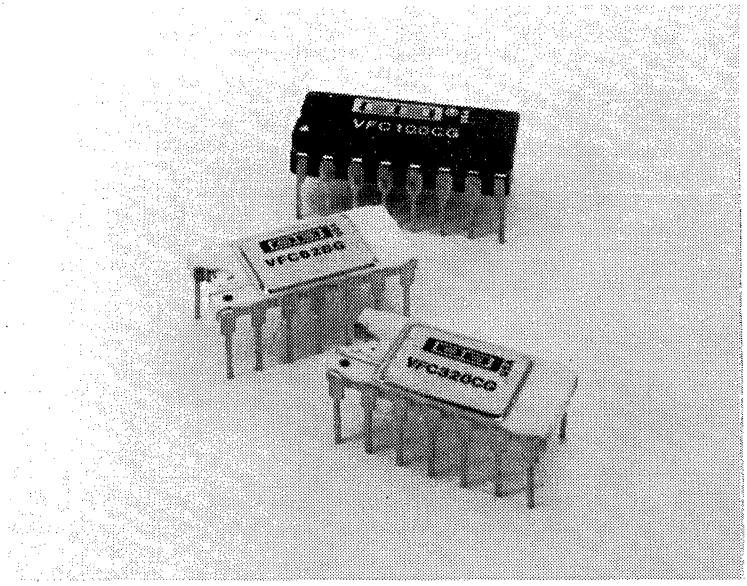


FIGURE 6. 64-channel, Two-Tier, Single-Ended Expansion.

VOLTAGE TO FREQUENCY CONVERTERS



VFC's provide a simple, low cost way of converting analog signals into digital form. They provide an important alternative to other analog to digital conversion techniques. Their integrating input properties make them an appropriate choice when operating in noisy environments. The combination of high accuracy and linearity, low temperature drift, and monotonicity often provide performance characteristics unattainable with other techniques.

Since an analog quantity represented as a frequency is inherently serial data, it is easily handled in large multi-channel systems. Frequency information can be transmitted over long lines with excellent noise immunity using low cost digital line transmitters and receivers. Isolation can be accomplished with optical or transformer couplers without loss in accuracy. Outputs from multiple VFC's can be gated to common counter circuitry with simple digital logic.

Burr-Brown monolithic VFC's include the VFC32, VFC62, and VFC320 which provide industry standard performance and reliability in such applications as precision test and measurement equipment, data acquisition systems, and communications equipment.

SELECTION GUIDE

VOLTAGE-TO-FREQUENCY CONVERTERS

VFCs provide a simple low cost way of converting analog signals into digital form. They produce a pulse train with a repetition rate proportional to the amplitude of the analog input. The combination of accuracy, linearity, and low temperature drift make these units some of the best available. Simple low cost isolation is obtained when a VFC is used together with a DC/DC converter and a single optical coupler.

V/F CONVERTERS								
Description	Model[1]	Frequency Range (kHz)	V_{IN} Range (V)	Linearity, max (% of FSR)	Tempco, max (ppm of FSR/°C)	Temp Range[2]	Package	Page
Low Cost, Monolithic	VFC32KP	User-selected, 500kHz, max	User-selected	±0.01 at 10kHz	75 typ	Com	DIP	10-3
	VFC32BM, (Q)			±0.05 at 100kHz	±100	Ind	TO-100	10-3
	VFC32SM, (Q)			±0.2 at 500kHz	±150	MIL	TO-100	10-3
Military	VFC32/MIL Series	See Military Products, section 12.						
Low Cost Complete	VFC42BP	0 to 10	0 to +10	±0.01	±100	Ind	DIP	10-11
	VFC42SM	0 to 10	0 to +10	±0.01	±100	MIL	DIP	10-11
	VFC52BP	0 to 100	0 to +10	±0.05	±150	Ind	DIP	10-11
	VFC52SM	0 to 100	0 to +10	±0.05	±150	MIL	DIP	10-11
Precision Monolithic	VFC62BG	User-selected, 1MHz max	User-selected	±0.005 at 10kHz	±50	Ind	DIP	10-17
	VFC62BM			±0.005 at 10kHz	±50	Ind	TO-100	10-17
	VFC62SM			±0.005 at 10kHz	±50	MIL	TO100	10-17
	VFC62CG			±0.002 at 10kHz	±20	Ind	DIP	10-17
	VFC62CM			±0.002 at 10kHz	±20	Ind	TO-100	10-17
	VFC320BG	User-selected, 1MHz max	User-selected	±0.005 at 10kHz	±50	Ind	DIP	10-40
	VFC320BM			±0.005 at 10kHz	±50	Ind	TO-100	10-40
	VFC320SM			±0.005 at 10kHz	±50	MIL	TO-100	10-40
	VFC320CG			±0.002 at 10kHz	±20	Ind	DIP	10-40
	VFC320CM			±0.002 at 10kHz	±20	Ind	TO-100	10-40
Synchronized Monolithic	VFC100AG	Clock Programmed, 2MHz max	0 to +10	0.025 at 100kHz	±100	Ind	DIP	10-25
	VFC100BG		0 to +10	0.1 at 1MHz	±50	Ind	DIP	10-25
	VFC100SG		0 to +10	0.025 at 100kHz	±100	MIL	DIP	10-25

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See High Reliability Screening, section 12. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

BURR-BROWN®

VFC32

For a /883B version of this product, see VFC32/883B in the Military Products section.

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- RELIABLE MONOLITHIC CONSTRUCTION
- HIGH LINEARITY
  ±0.01% max at 10kHz FS
  ±0.05% max at 100kHz FS
- V/F OR F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- VOLTAGE OR CURRENT INPUT
- OUTPUT DTL/TTL/CMOS COMPATIBLE

APPLICATIONS

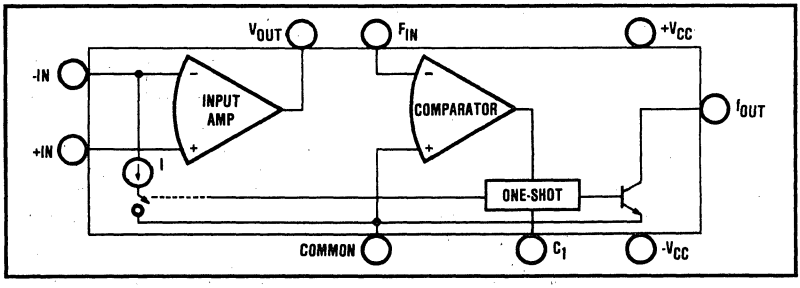
- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC32 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with DTL, TTL, and CMOS logic families.

The converter requires two external resistors and two external capacitors to operate. Full scale frequency and input voltage are determined by one resistor (in series with -IN) and two capacitors (one-shot timing and input amplifier integration). High linearity is achieved with relatively few external components, e.g., ±0.01% at 10kHz. The other resistor is a non-critical open collector pull-up (f_{OUT} to $+V_{CC}$).

The VFC32 is available in three models and two package configurations. The TO-100 versions are hermetically sealed, and specified for the -25°C to +85°C and -55°C to +125°C ranges, and the epoxy dual-in-line unit is specified from 0°C to +70°C.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted.

CHARACTERISTICS	CONDITIONS	VFC32KP MIN	VFC32KP TYP	VFC32KP MAX	VFC32BM MIN	VFC32BM TYP	VFC32BM MAX	VFC32SM MIN	VFC32SM TYP	VFC32SM MAX	UNITS
INPUT (V/F CONVERTER)	$F_{OUT} = V_{IN} / 7.5\ R_1C_1$, Figure 6										
Voltage Range[1]											
Positive Input		>0		+0.25mA x R_1	*		*	*		*	V
Negative Input		>0		-10	*		*	*		*	V
Current Range[1]		>0		+0.25	*		*	*		*	mA
Bias Current											
Inverting Input			20	100		*	*		*	*	nA
Noninverting Input			100	250		*	*		*	*	nA
Offset Voltage[2]			1	4		*	*		*	*	mV
Differential Impedance		300 || 10	650 ||10		*	*		*		kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		*	*		*		MΩ || pF
INPUT (F/V CONVERTER)	$V_{OUT} = 7.5\ R_1C_1\ F_{IN}$, Figure 9										
Impedance		50 || 10	150 || 10		*	*		*	*		kΩ || pF
Logic "1"			+1.0		*		*	*		*	V
Logic "0"			−0.05		*		*	*		*	V
Pulse-width Range		0.1		150k/F_{MAX}	*		*	*		*	µsec
ACCURACY											
Linearity Error[3]	0.01Hz ≤ oper freq ≤ 10kHz		±0.005	±0.010[4]		*	*		*	*	% of FSR[5]
	0.1Hz ≤ oper freq ≤ 100kHz		±0.025	±0.05		*	*		*	*	% of FSR
	0.5Hz ≤ oper freq ≤ 500kHz		±0.05			*			*		% of FSR
Offset Error Input											
Offset Voltage[2]			1	4		*	*		*	*	mV
Offset Drift[6]			±3			*			*		ppm of FSR/°C
Gain Error[2]			5			*	*		*	*	% of FSR
Gain Drift[6]	f = 10kHz		±75			±50	±100		±70	±150	ppm/°C
Full Scale Drift (offset drift & gain drift)[6][7]	f = 10kHz		±75			±50	±100		±70	±150	ppm of FSR/°C
Power Supply Sensitivity	f = DC, $\pm V_{CC}$ = 12VDC to 18VDC			±0.015			*			*	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, Logic "0"	I_{SINK} = 8mA	0	0.2	0.4	*	*	*	*	*	*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*		*	*	µA
Voltage, Logic "1"	External pull-up resistor required (see Figure 4)			V_{PU}			*			*	V
Pulse Width	For Best Linearity		0.25/F_{MAX}			*			*		sec
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF			400			*			*	nsec
OUTPUT (F/V CONVERTER) V_{OUT}											
Voltage	$I_O \leq$ 7mA	0 to +10			*			*			V
Current	$V_O \leq$ 7VDC	+10			*			*			mA
Impedance	Closed loop			1			*			*	Ω
Capacitive Load	Without oscillation			100			*			*	pF
DYNAMIC RESPONSE											
Full Scale Frequency				500[8]	*			*			kHz
Dynamic Range		6			*			*			decades
Settling Time	(V/F) to specified linearity for a full scale input step		[9]			*			*		
Overload Recovery	< 50% overload		[9]			*			*		
POWER SUPPLY											
Rated Voltage			±15								V
Voltage Range		±11		±20					*		V
Quiescent Current			±5.5	±6.0		*	*		*		mA
TEMPERATURE RANGE											
Specification		0		+70	-25		+85	-55		+125	°C
Operating		-25		+85	-55		+125	-55		+125	°C
Storage		-25		+85	-65		+150	-65		+150	°C

*Specification the same as VFC32KP

NOTES:
1. A 25% duty cycle (0.25mA input current) is recommended where possible to achieve best linearity.
2. Adjustable to zero. See Offset and Gain Adjustment section.
3. Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. Above 200kHz, it is recommended all grades be operated below +85°C.
4. ±0.015% of FSR for negative inputs shown in Figure 7. Positive inputs are shown in Figure 6.
5. FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage).
6. Exclusive of external components' drift.
7. Positive drift is defined to be increasing frequency with increasing temperature.
8. For operation above 200kHz up to 500kHz, see Discussion of Specifications and Installation and Operation sections.
9. One pulse of new frequency plus 1μsec.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±22
Output Sink Current (F_{OUT})	50mA
Output Current (V_{OUT})	+20mA
Input Voltage, −Input	±Supply
Input Voltage, +Input	±Supply
Comparator Input	±Supply
Storage Temperature Range	
VFC32BM, SM	−65°C to +150°C
VFC32KP	−25°C to +85°C

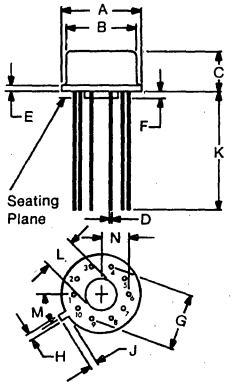
MECHANICAL

VFC32BM, VFC32SM TO-100 PACKAGE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only, Numbers may not be marked on package.

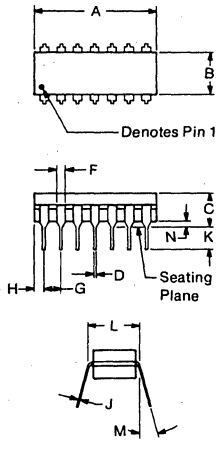
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.70	—
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05



VFC32KP EPOXY DUAL-IN-LINE

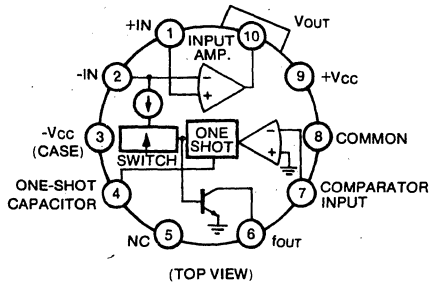
NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.660	.785	16.76	19.94
B	.220	.280	5.59	7.11
C	—	.200	—	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100	—	2.54	—
L	.300 BASIC		7.62 BASIC	
M	—	15°	—	15°
N	.020	.050	0.51	1.27



PIN CONFIGURATIONS

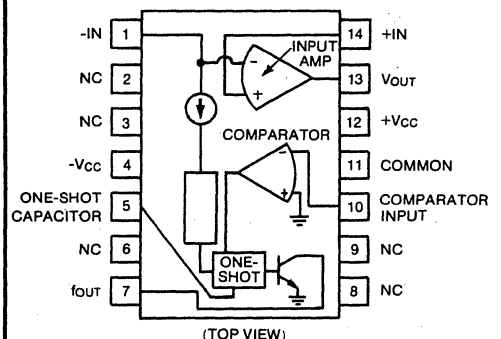
VFC32BM, VFC32SM
TO-100 PACKAGE



(TOP VIEW)

NC = NO INTERNAL CONNECTION.
EXTERNAL CONNECTION PERMITTED.

VFC32KP
EPOXY DUAL-IN-LINE PACKAGE



(TOP VIEW)

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (90% of full scale input or frequency and 0.1% of full scale called zero). Linearity is the true measure of voltage-to-frequency converter's performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. For a given full scale frequency, the linearity error decreases with decreasing operating frequency as shown in Figure 2. Also, best linearity is achieved at lower gains ($\Delta F_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC32 makes the device an excellent choice for use as the front end of A/D converters with 8- to 12-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire serial data transmission).

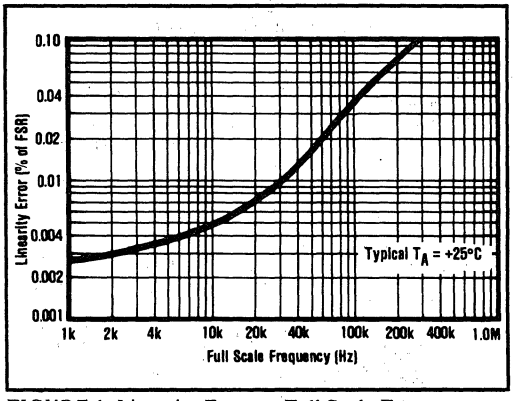


FIGURE 1. Linearity Error vs Full Scale Frequency. (25% Duty Cycle)

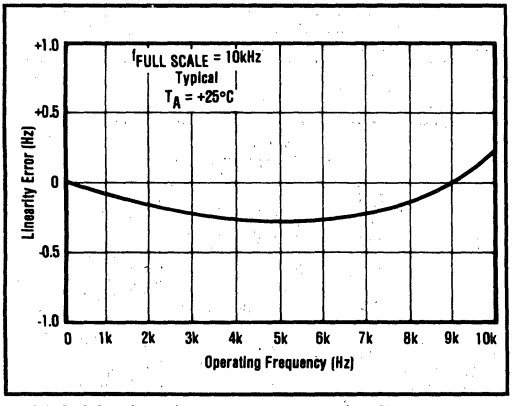


FIGURE 2. Linearity Error vs Operating Frequency. (25% Duty Cycle)

FREQUENCY STABILITY vs TEMPERATURE

The full scale frequency drift of the VFC32 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 100kHz, and this should be taken into account for specific applications. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC32. Above 200kHz, it is recommended all grades be operated below +85°C. Higher duty cycle (up to 50%) and higher output transistor collector current (up to 15mA) will be required. Linearity will, however, be degraded.

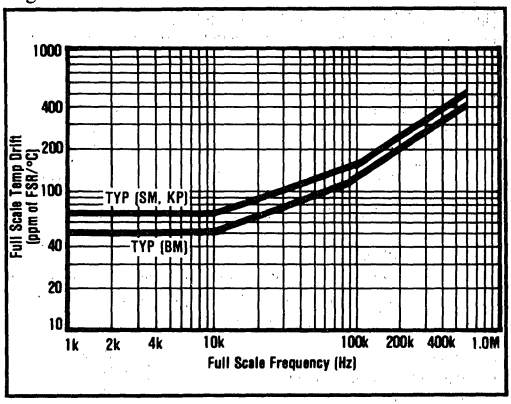


FIGURE 3. Full Scale Drift vs Full Scale Frequency. (25% Duty Cycle)

RESPONSE

Response of the VFC32 to changes in input signal level is specified for a full scale step, and is 1 microsecond plus 1 pulse of the new frequency. For a 10 volt input signal step with the VFC32 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 11 microseconds.

THEORY OF OPERATION

The VFC32 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage in Figure 4.

Essentially, the input amplifier acts as an integrator that produces a 2-part ramp. The first part is a function of the input voltage, and the second part dependent on the current sink. When a positive input voltage is applied at V_{IN}, a constant current will flow through the input resistor, causing the voltage at f_{IN} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time, the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and integrating components. When the ramp reaches a voltage close to zero, the comparator will cause the one-shot to fire. The one-shot period is determined by an internal 7.5V reference and C_1. The f_{OUT} signal will then change logic states, going from a "0" to a "1", and the switch will close, enabling the constant current sink. The ramp voltage will then change direction and begin to ramp up. Since V_{IN}/R_1 is always set up to be less than 1mA, the current in the integrating capacitor will flow toward the summing junction, and the ramp voltage rate of change will be;

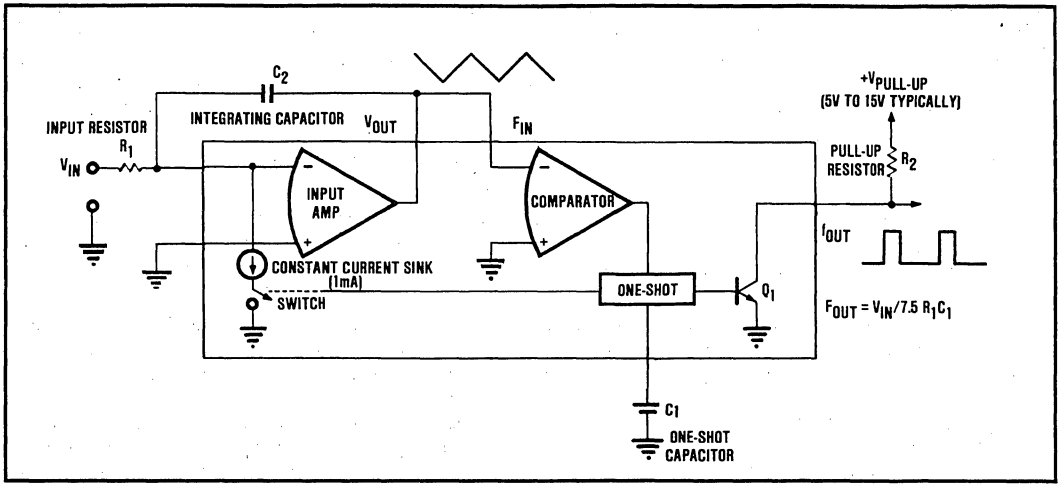


FIGURE 4. Functional Block Diagram of the VFC32.

$$\frac{dV}{dt} = \frac{\frac{V_{IN}}{R_1} - 1mA}{C_2}$$

Before the ramp voltage can saturate the input amplifier, the one-shot will reset, disabling the current sink, changing the output state back to logic "0", and restarting the cycle. Since the integrating capacitor C_2 affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to V_{IN}/R_1, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

To operate the VFC32 as a highly linear frequency-to-voltage converter, open the connection between V_{OUT} and f_{IN}, and connect V_{IN} to V_{OUT}. The input frequency should be coupled through a capacitor to f_{IN}, and a positive output voltage proportional to f_{IN} will be generated at the V_{OUT} connection. For details see Installation and Operating Instructions.

The total VFC period is determined by the following equations, which is shown graphically in Figure 5.

$$f_o = \frac{1}{t}$$

$$t = t_1 + t_2 \text{ and } i = c\, dv/dt$$

$$t = \Delta V_{OUT}\, t_1 \frac{C_2}{V_{IN}/(R_1)} + \Delta V_{OUT}\, t_2 \frac{C_2}{V_{IN}/(R_1) - 1mA}$$

and:

$$-\Delta V_{OUT} t_1 = +\Delta V_{OUT} t_2$$

$$t_2 = C_1 \frac{7.5V}{1mA}$$

The equations reduce to:

$$f_o = \frac{V_{IN}}{7.5(R_1)\, C_1}$$

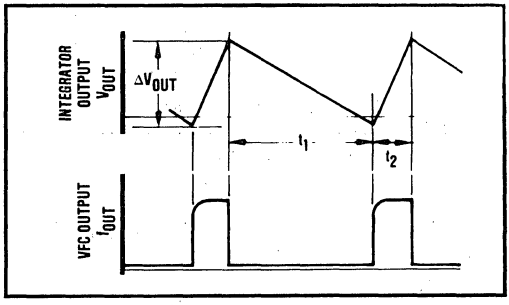


FIGURE 5. Integrator and VFC Output Timing.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). It is measured at the full scale input voltage, which gives the full scale output frequency, F_{FS}.

$$D = \frac{t_2}{t_1 + t_2} = PW \times F_{FS}$$

$$PW = \frac{D}{F_{FS}}$$

Duty cycle is related to the maximum input current and the 1mA (nominal) current sink. By reducing the equations for t_2 and f_o:

$$D = \frac{V_{IN}\ max/(R_1)}{1mA} = \frac{I_{IN}\ max}{1mA}$$

A 25% duty cycle or less is recommended to achieve the best linearity. This corresponds to a maximum input

current of 0.25mA. However, for frequencies above 200kHz a higher duty cycle (up to 50%) will provide more stable high temperature operation at a sacrifice in linearity.

In general, designs with the VFC32 include: (1) Choosing F_{MAX}, (2) Choosing the duty cycle (D = 0.25 typically), (3) Determining the one-shot PW, and (4) Calculating C_1, C_2, R_1, R_2, and R_3.

INSTALLATION AND OPERATING INSTRUCTIONS

The VFC32 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

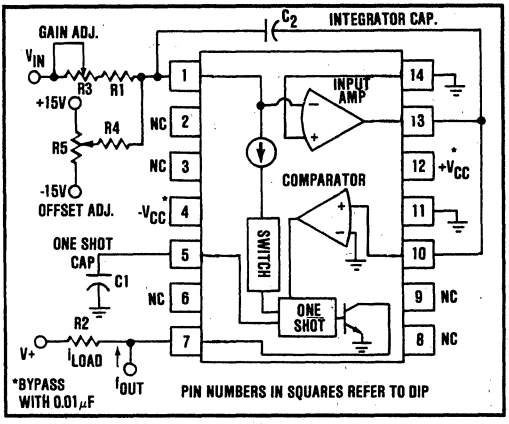


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

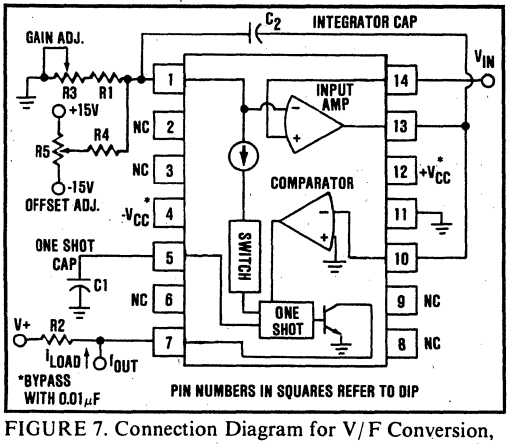


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

Differential inputs are also possible (in Figure 7 lift ground on R_3 and drive R_3 and pin 14 differentially). Note, no CMR will be present.

The full scale frequency and full scale input voltage (current) are established by the selection of values for R1, C2, and C1. Most applications will require a gain adjustment pot (R3), but the offset adjust network (R4, R5) can be omitted if input offset voltages of 1mV to 4mV can be tolerated. R2 is an output pull up resistor and its value depends on the pull up voltage and output drive requirements.

EXTERNAL COMPONENT SELECTION CRITERIA

One-shot Capacitor, C1. This capacitor determines the duration of the output pulse, and is a function of the full scale frequency, according to this equation:

$$C1(pF) = 33 \times 10^6 / f_{MAX} - 30$$

Above 425kHz use 47pF

Select the closest standard value to the capacitance given by the equation. The initial tolerance of this capacitor is not critical since R3 will be adjusted to remove initial gain errors. The temperature drift is critical, since it will add directly to the errors in the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize the parasitic capacitance at this connection to the VFC32 and C1 should be mounted as close as possible. Figure 8 shows pulse width and FS frequency for various values of C1.

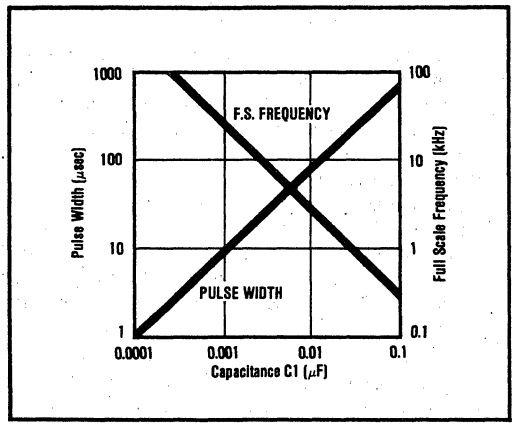


FIGURE 8. Output Pulse Width (D = 0.25) and Full Scale Frequency vs External One-shot Capacitance.

Input Resistor R1 and R3. R1 and R3 determine the magnitude of the current which charges the integrator capacitor. It is a function of the full scale input voltage, according to this equation for 25% duty cycle.

$$R1\ (k\Omega)\ [90\% - \%\ \text{tolerance C1}] \times V_{IN}\ \text{max}/0.25mA$$

R1 is scaled down by [1-(initial C1 tolerance + 0.1)] to allow the addition of a series gain adjusting pot, R3.

$$R_3\ (k\Omega) = V_{IN}\ \text{max}/0.25mA - R_1$$

R1 should have a very low temperature coefficient since this drift adds directly to the errors in the transfer function. If the input signal is a current rather than a voltage, R1 and R3 should be replaced with a short circuit, and the full scale input current should be 0.25mA (25% duty cycle). Removal of gain error then requires adjustment of C1.

Integrating Capacitor C2. C2 is a function of the full scale frequency, according to this equation:

$C_2(\mu F) = 10^2 / f_{MAX}$ below 100kHz
$0.001\mu F$ min above 100kHz

Select the closest standard value to the capacitance given by the equation. The initial tolerance and temperature stability are not critical since these errors do no affect the transfer function. Since the leakage current of the capacitor introduces a gain error, select a capacitor with leakage that is small compared to the full scale input current e.g., 0.25mA. A mylar type is recommended.

Output Pull Up Resistor R2. The open collector output can sink up to 8mA and still be TTL-compatible. Select R2 according to this equation:

$$R_2 \text{ min } (\Omega) = V_{PULLUP}/(8mA - i_{LOAD})$$

A 10% carbon composition resistor is suitable for use as R2.

Operation above 200kHz up to 500kHz requires higher duty cycles up to 50% ($I_{IN} = 0.5mA$) and a pull-up resistor that permits 15mA to flow in the output transistor. At this speed, capacitive loading should be minimized to 100pF or less to allow the output voltage time to rise to logic one. Due to the large collector current, the logic zero may rise above +0.4V. This may require an interface circuit such as diode clamp or voltage comparator for coupling to TTL inputs. Note, that linearity will degrade. Also, it is recommended to stay below +85°C at high frequencies.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC32 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses -0.6V. Choose C3 for appropriate value of t (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero, to insure that the input signal at pin 10 crosses the -0.6V threshold. Errors are nulled following the procedure given on this page, using 0.001X full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC32 is 0.015% of FSR/% max. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with $0.01\mu F$ capacitors.

Current in the f_{OUT} pin (logic sink current) flows in the common connection (pin 11 of DIP package). It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by logic current flowing through any ground return impedance.

Trimming Components R3, R4, R5.

R5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R4 can be a 20% carbon composition resistor with a value of 10MΩ.

R3 nulls the gain errors of the converter and compensates for initial tolerances of R1 and C1. Its total resistance should be at least 20% of R1, if R1 is selected 10% low (see R1 equation). Its temperature coefficient should be no greater than five times that of R1, to maintain a low drift of the R3 - R1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 X full scale.
2. Adjust R5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

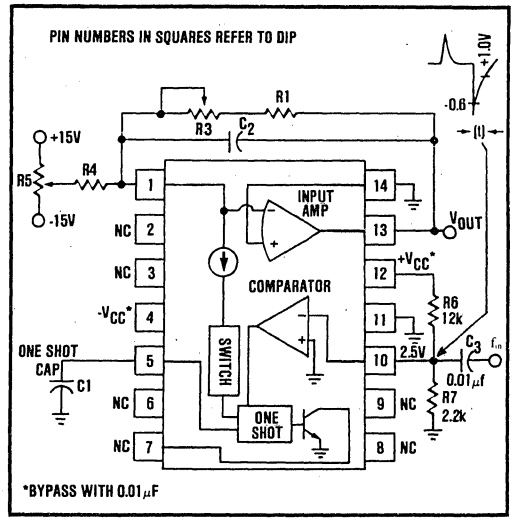


FIGURE 9. Connection Diagram for F/V Conversion.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1

$C_1 = 33 \times 10^6 / f_{MAX} - 30$
$= 33 \times 10^6 / 100kHz - 30$
$= 300pF$

Choose a 300pF NPO ceramic capacitor with ±1% tolerance.

Selecting R_1 and R_3 (for D = 0.25; for D = 0.5 use 0.5mA)

$R_1 = [90\% - \%$ tolerance of $C_1] \times V_{IN}$ max / 0.25mA
$= [0.9 - 0.1] \times 10V/0.25mA$
$= 32k\Omega$

Choose a 32.4kΩ metal film resistor with ±1% tolerance.

$R_3 = 10V/0.25mA - R_1$
$= 8k\Omega$

Choose a 10kΩ cermet potentiometer

Selecting C_2

$C_2 = 10^2/F_{MAX}$
$= 10^2/100kHz$
$= 0.001\mu F$

Choose a 0.001μF mylar capacitor with ±5% tolerance.

Selecting R_2

$R_2 = V_{PULLUP}/(8mA - i_{LOAD})$
$= 5V/(8mA - 1.6mA)$, one TTL-load = 1.6mA
$= 781\Omega$

Choose a 750Ω 1/4-watt carbon composition resistor with ±5% tolerance.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC32 ideal for a variety of VFC applications. High accuracy allows the VFC32 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 12-bits.

Figures 10 - 14 show typical applications of the VFC32.

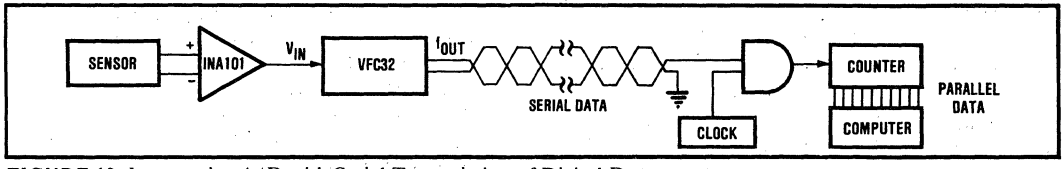


FIGURE 10. Inexpensive A/D with Serial Transmission of Digital Data.

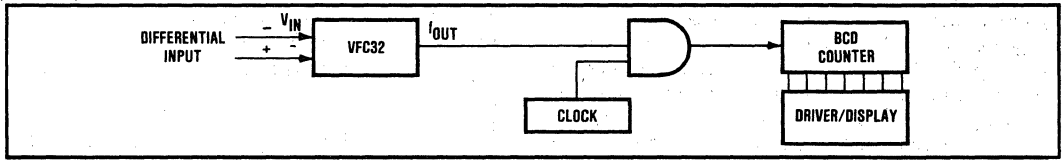


FIGURE 11. Inexpensive Digital Panel Meter.

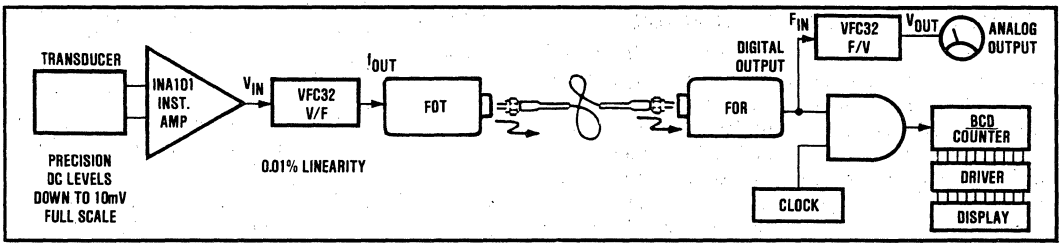


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

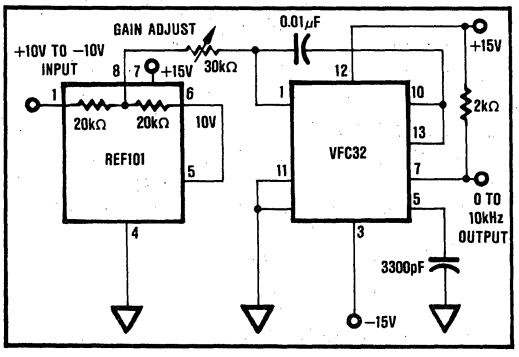


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

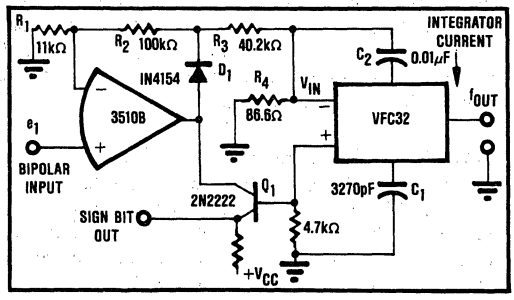


FIGURE 14. Absolute value circuit with the VFC32. Op amp, D_1 and Q_1 (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $|e_1|$. The sign bit output provides indication of the input polarity.

BURR-BROWN®

VFC42
VFC52

VOLTAGE-TO-FREQUENCY AND FREQUENCY-TO-VOLTAGE CONVERTER

FEATURES

- V/F OR F/V CONVERSION
- TWO FREQUENCY RANGES
  - 10kHz (VFC42)
  - 100kHz (VFC52)
- LOW NONLINEARITY
  - ±0.01% max (VFC42)
  - ±0.05% max (VFC52)
- MINIMAL EXTERNAL COMPONENTS REQUIRED
  - Add only one external resistor for V/F operation
- 6 DECADE DYNAMIC RANGE
- OUTPUT DTL/TTL/CMOS COMPATIBLE

DESCRIPTION

VFC42 and VFC52 are hybrid microcircuits which can be connected as voltage-to-frequency or frequency-to-voltage converters. They provide a simple, low cost method of converting analog signals into an equivalent digital form. The digital output is an open collector which can be made compatible with DTL, TTL, or CMOS logic. The output is a train of constant-amplitude, constant-width pulses whose repetition rate is proportional to the amplitude of the analog input voltage. In the frequency-to-voltage mode the pulses become the input and the proportional DC voltage, the output.

Both models are offered in epoxy (−25°C to +85°C) and hermetic metal (−25°C to +85°C and −55°C to +125°C) 14-pin DIP packages.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

THEORY OF OPERATION

VFC42 and VFC52 hybrid voltage-to-frequency converters provide a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. To understand the circuit's operation see Figure 1.

The input amplifier is connected in an integrator configuration. When a positive input voltage is applied at V_{IN}, a constant current flows through the input resistor causing voltage at f_{IN} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_2$. During this time the constant current sink is disabled by the switch. When the ramp reaches zero volts, the comparator causes the one-shot to fire. The f_{out} signal then changes states, going from logic 0 to logic 1 and the switch closes, enabling the constant current sink. Ramp voltage then changes direction and begins to ramp up. Since V_{IN}/R_1 is always set to be less than 1mA, current in the integrating capacitor flows toward the summing junction and ramp voltage range of change will be

$$\frac{dV}{dt} = \frac{\left(\frac{V_{in}}{R_1}\right) - 1mA}{C_2}$$

Before the ramp voltage can saturate the input amplifier, the one-shot resets, disabling the current sink, changing the output state back to logic 0 and restarting the cycle.

To operate VFC42 and VFC52 as highly linear frequency-to-voltage converters, open the connection between V_{OUT} and F_{IN} and connect V_{IN} to V_{OUT}. The input frequency should be coupled through a capacitor to f_{IN}. A positive output voltage proportional to f_{IN} will be generated at the V_{OUT} connection. An external capacitor connected between pins 13 and 14 (paralleling C2) should be added to reduce output ripple. Refer to Operating Instructions for detailed information on F/V operation.

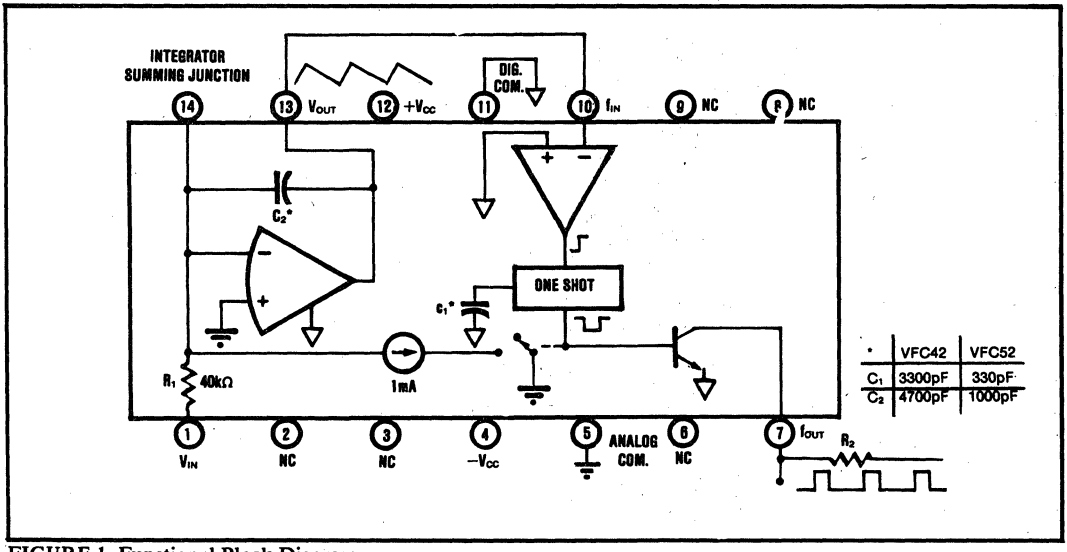


FIGURE 1. Functional Block Diagram.

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity, the maximum deviation of the actual transfer function from a straight line drawn between the end points (full scale input and zero input), is the true measure of a FVC's performance and is a function of full scale frequency. The high linearity of VFC42 and VFC52 makes these devices an excellent choice for use in A/D converters with 10 (0.05%) and 12 bit (0.012%) accuracy and for highly accurate analog data transfer over long lines in noisy environments.

FREQUENCY STABILITY VS TEMPERATURE

Frequency stability vs temperature is expressed as parts per million of full scale range per °C. Since frequency drift is a function of the specified temperature range, the "SM" models will meet the lower drift specifications of the "BM" models over the narrower −25°C to +85°C temperature range. Error sources do not drift linearly over temperature, consequently the units drift much less at higher temperatures.

RESPONSE TIME

Response time of VFC42 and VFC52 to input signal level changes is specified for a full scale step and is 1μsec plus 1 period of the new frequency. Typical settling time to within rated linearity for a positive input voltage step of +10V is 101μsec for VFC42 and 11μsec for VFC52.

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C, and ±15VDC power supplies unless otherwise noted.

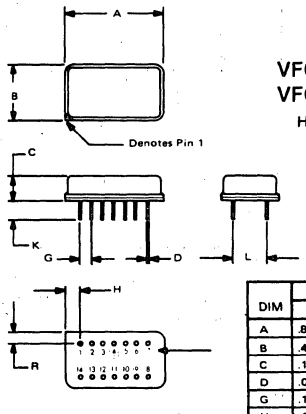
MODEL	VFC42			VFC52			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Full Scale Frequency		10			100		kHz
INPUT							
Analog Input (V/F)							
Voltage Range	0		10	0		+10	V
Current Range	0		+0.25	0		+0.25	mA
Input Bias Current (pin 14) Inverting Input		6	8		6	8	nA
Input Offset Voltage (trimmable to zero)		100	200		100	200	µV
Input Impedance (pin 1)	32	40	48	32	40	48	kΩ
Frequency Input (F/V) (pin 10)							
Logic Levels: Logic "0"	$-V_{CC}$		−0.6	$-V_{CC}$		−0.6	V
Logic "1"	+1.0		$+V_{CC}$	+1.0		$+V_{CC}$	V
Pulse Width Range (t_2, Fig. 6)	0.1		15	0.1		1.5	µsec
Impedance	1 ‖ 10	1.2 ‖ 10		1 ‖ 10	1.2 ‖ 10		MΩ ‖ pF
TRANSFER CHARACTERISTICS							
Transfer Functions	$f_{OUT} = V_{IN}$ (1.00 × 10^3) $V_{OUT} = f_{IN}$ (10 × 10^{-4})			$f_{OUT} = V_{IN}$ (1.00 × 10^4) $V_{OUT} = f_{IN}$ (10 × 10^{-5})			Hz VDC
Accuracy							
Full Scale Gain (adjustable to zero)		0.1	0.2		0.1	0.2	%
Linearity Error: 0.01Hz ≤ F ≤ 10kHz		0.005	0.01				% of FSR[1]
0.1Hz ≤ F ≤ 100kHz					0.025	0.05	% of FSR
Offset Error (pin 1)		0.001	0.002		0.001	0.002	% of FSR
Power Supply Sensitivity[2]			0.015			0.015	% of FSR/%
Temperature Stability							
Analog Input							
Full Scale Drift (gain and offset)							
Grade: BP (hot/cold)[3]		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
BM		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
SM		±30/±60	±50/±100		±30/±60	±50/±150	ppm/°C
Offset Drift							
Grade: BP		±1	±3		±1	±3	ppm of FSR/°C
BM		±1	±3		±1	±3	ppm of FSR/°C
SM		±1	±3		±1	±3	ppm of FSR/°C
Frequency Input							
Full Scale Drift (gain and offset)							
Grade: BP (hot/cold)[3]		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
BM		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
SM		±30/±60	±50/±100		±30/±60	±50/±150	ppm/°C
Dynamic Response							
Settling Time to within linearity specification for full scale input step	1 period of new frequency + 1µsec			1 period of new frequency + 1µsec			
Overload Recovery Time	1 period of new frequency + 1µsec			1 period of new frequency + 1µsec			
OUTPUT							
Voltage Output							
Voltage Range (I_O ≤ 5mA)	0 to +10			0 to +10			V
Output Current (V_O ≤ 7V)	+10			+10			mA
Output Impedance (closed loop)			1			1	Ω
Capacitive Load			100			100	pF
Frequency Output (open collector)							
Pulse Characteristics: Logic "1"			$+V_{PULL-UP}$			$+V_{PULL-UP}$	V
Logic "0" (at I_O ≤ −8mA)	0		+0.4	0		+0.4	V
Pulse Width	20	25		2.0	2.5		µsec
Output Sink Current (Logic "0", ≤ 0.4V)			8			8	mA
Output Leakage Current (Logic "1")			1			1	µA
Fall Time (I_{OUT} = −5mA, C_{LOAD} = 500pF)			400			400	nsec
POWER SUPPLY REQUIREMENTS							
Rated Supplies		±15			±15		V
Supply Range	±9		±20	±9		±20	V
Supply Drain (independent of operating frequency)		±6.5	±7.5		±6.5	±7.5	mA
TEMPERATURE RANGE							
Specification: BP, BM	−25		+85	−25		+85	°C
SM	−55		+125	−55		+125	°C
Operating: BM, SM	−55		+125	−55		+125	°C
BP	−55		+100	−55		+100	°C
Storage: BM, SM	−55		+125	−55		+125	°C
BP	−25		+85	−25		+85	°C

NOTES: (1) % of FSR = % of Full Scale Range. (2) Rated at full scale input and ±15V supplies. (3) Hot = +20°C to highest rated temperature; cold = lowest rated temperature to +20°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±22V
Output Sink Current (F_{output})	50mA
Output Current (V_{output})	+20mA
Input Voltage, Pin 14	±Supply
Input Voltage, Pin 1	±Supply
Storage Temperature Range	
Grade: BM, SM	−55°C to +125°C
BP	−25°C to +85°C

MECHANICAL



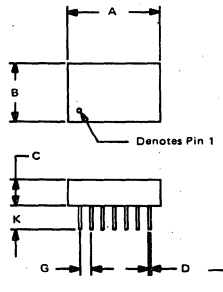
VFC42BM, VFC42SM
VFC52BM, VFC52SM

Hermetic Metal Package
14-Pin DIP

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

Pin numbers shown for reference only.
Numbers are not marked on package.

Tolerance (inches): .xxx ±0.005; .xx ±0.02
Connector: 14-pin DIP (145MC)
Case Material: Base - gold plated kovar, Cap - nickel-plated kovar or steel
Pin material and plating compositions: Conforms to MIL-STD-883, Method 2003 (solderability) except paragraph 3.2 (aging).
Hermeticity: Conforms to MIL-STD-883, Method 1014, Condition C, Step 1, Fluorocarbon (gross leak).



VFC42BP, VFC52BP

Epoxy Package
14-Pin DIP

Pin material and plating composition:
Conform to Method 2003 (solderability)
of MIL-STD-883 (except paragraph 3.2).

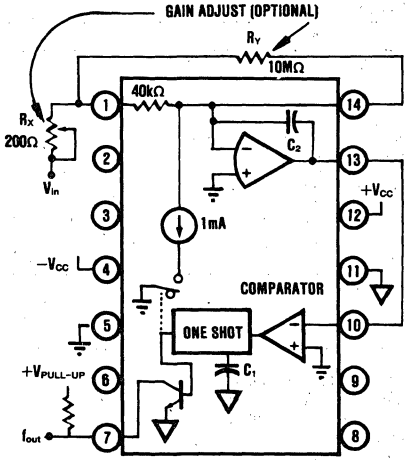
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

Pin numbers shown for reference only.
Numbers are not marked on package.

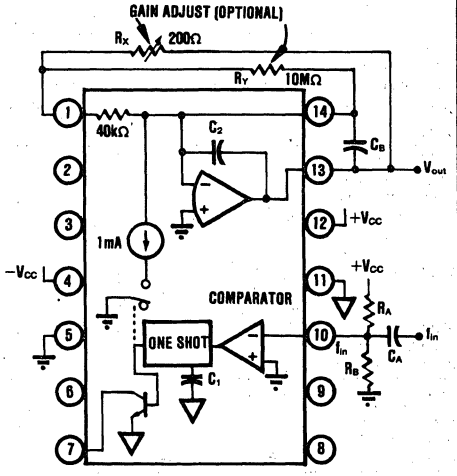
Tolerance (inches): .xxx ±0.005
.xx ±0.02
Connector: 14-pin DIP (145MC)
Case Material: Epoxy

CONNECTION DIAGRAMS

V/F Operation



F/V Operation



OPERATING INSTRUCTIONS

VFC42 and VFC52 can be connected for either V/F or F/V operation. Only one external component, the output pull-up resistor, is required for V/F operation. F/V operation requires the pull-up resistor and input biasing components. Gain error is the most significant error in either configuration and may be nulled out with the optional trim circuit (R_X and R_Y). The offset error is laser trimmed at the factory and no external adjustment is required.

Power Supply Consideration: Power supplies stable to within ±1% are recommended to maintain conversion accuracy. Each supply should be bypassed with 0.01μF capacitors located as close to the VFC as possible.

VOLTAGE-TO-FREQUENCY OPERATION

Calculating the Value of Pull-Up Resistor, R_P: The open collector output can be used to drive DTL, TTL, CMOS or discrete circuits. The maximum collector current allowed for TTL circuits in logic 0 is 8mA. R_P may be calculated by this equation:

$$R_P \text{ min} = \text{V pull-up}/(8\text{mA} - i_{LOAD}).$$

A 10% carbon composition resistor is suitable for this purpose. The collector current may be as great as 30mA if a logic 0 voltage of 1.0V is tolerable.

Gain Adjustment Procedure: Connect R_X and R_Y as shown in Connection Diagram. Apply positive full scale voltage to the input and adjust R_X until 10kHz ±1Hz (VFC42) or 100kHz ±10Hz (VFC52) is obtained at f_{OUT}. R_X and R_Y should have temperature coefficients of <500ppm. These external components will add less than 5ppm/°C to temperature drift.

FREQUENCY-TO-VOLTAGE OPERATION

Input Characteristics: VFC42 and VFC52 can be connected as frequency-to-voltage converters as shown in Connection Diagram. f_{IN} should be a positive pulse train with minimum pulse width of 1.0μsec and rise and fall times of ≤ 300nsec. The input train (f_{IN}) is differential and applied to the input of the comparator (pin 10) (see Figure 2). Threshold voltage of the comparator lies between −0.6 and +1.0V. When comparator input is less than −0.6V it triggers the one-shot.

Selecting R_A, R_B, and C_A Input components R_A, R_B and C_A are selected so that the trigger voltage (V_T) is more negative than −0.6V and transition time (t_2) is between 0.3μsec and 15μsec for VFC42 and between 0.3μsec and 1.5μsec for VFC52. Table I give values for input components for several common signal sources. Values for R_A, R_B and C_A may be selected by the user when input signal characteristics differ from those listed. Conditions described above for trigger voltage and transition time must be observed.

TABLE I. F/V Input Component Selection

Input Type	V_{INPUT} (V)		V_{BIAS} (V)	VFC42			VFC52		
	Low	High		R_A (kΩ)	R_B (kΩ)	C_A (pF)	R_A (kΩ)	R_B (Ω)	C_A (pF)
TTL	≤+0.4	≥+2.8	+1.1	12	1.0	1000	8.2	680	680
5V CMOS	≤+0.5	≥+4.5	+1.2	18	1.6	2200	9.1	820	680
10V CMOS	≤+1.0	≥+9.0	+1.1	12	1.0	2200	6.2	510	680
15V CMOS	≤+1.5	≥+13.5	+1.1	12	1.0	2200	6.2	510	680

Equations to calculate trigger voltage and transition time are:

$$V_T = V_B + V_{in}(e^{-t_1/\tau} - 1)$$

$$t_2 = -\tau \ln\left[\frac{1 - V_B}{V_{in}(e^{-t_1/\tau} - 1)}\right]$$

V_B = Bias voltage on pin 10

V_{in} = Input pulse amplitude

t_1 = Input pulse width

τ = Time constant of R_A, R_B C_A as connected

If input pulse amplitude is greater than $+V_{CC} - 1V$, a voltage larger than $+V_{CC}$ will be applied to pin 10. Since this may damage the unit, a diode connected across R_A with the cathode tied to $+V_{CC}$ is required.

Output Characteristics: Selecting C_B: Output ripple voltage amplitude is inversely proportional to the input frequency and to the value of the integrating capacitance, $C_2 + C_B$. Conversely, time required for the output to settle is directly proportional to the value of $C_2 + C_B$ and is least with small values of $C_2 + C_B$. There is, therefore, a trade-off between output ripple amplitude and output settling time.

Because ripple amplitude is greatest at lowest input frequency it is at this point where the trade-off will usually be made. Ripple voltage and integrating capacitance value are related in this manner:

$$C_B = \frac{-(25 \times 10^{-6})t_{sec}}{\ln\left[1 - \frac{V_{Ripple}}{30V}\right]} \text{ farads}$$

where t is equal to 25μsec in the VFC42 and 2.5μsec in the VFC52 and C is the integrating capacitance.

Calculating output response time versus integrating capacitance is an iterative process and is plotted in Figure 3. These curves are for zero to full scale input frequency transitions. If faster response time with lower ripple voltage is desired, a low-pass filter can be connected in series with the output.

Gain Adjustment Procedure: Connect R_X and R_Y as shown in Connection Diagram. Apply full scale frequency to the input and adjust R_X until the full scale voltage is +10V ±1mV (discounting ripple). R_X and R_Y should have temperature coefficients of < 500ppm. These external components will add less than 5ppm/°C to temperature drift.

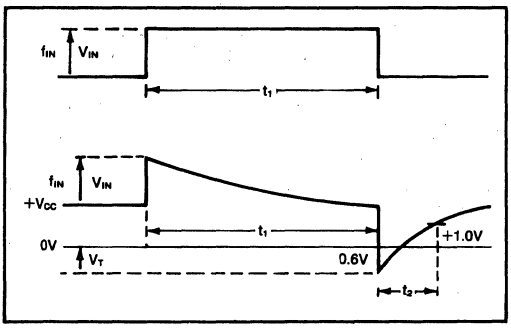


FIGURE 2. F/V Input Waveforms.

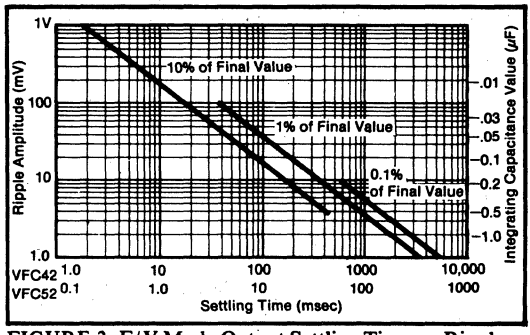


FIGURE 3. F/V Mode Output Settling Time vs. Ripple Voltage Amplitude for Full Scale Frequency Change.

APPLICATION

VFC42 and VFC52 can be used to convert analog data into a digital pulse train for transmission over long lines through high EMI environments. Illustrated in Figure 4 is a V/F, F/V combination that can be used to transmit analog data of 0 to +10V over a 100Ω shielded, twisted-pair. The voltage ripple amplitude at the output will be 10mV for a 10V output and the settling time for a full scale 0 to +10V change is 60 milliseconds.

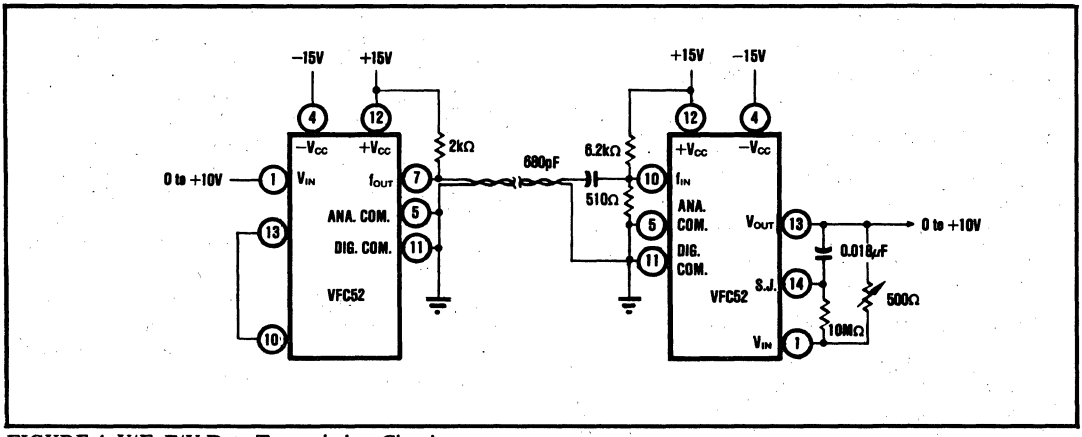


FIGURE 4. V/F, F/V Data Transmission Circuit.

BURR-BROWN®

VFC62

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- HIGH LINEARITY, 12 to 14 bits
  - ±0.005% max at 10kHz FS
  - ±0.03% max at 100kHz FS
  - ±0.1% typ at 1MHz FS
- 6-DECADE DYNAMIC RANGE
- 20ppm/°C max GAIN DRIFT
- OUTPUT DTL/TTL/CMOS COMPATIBLE
- ACTIVE PULL-UP OUTPUT

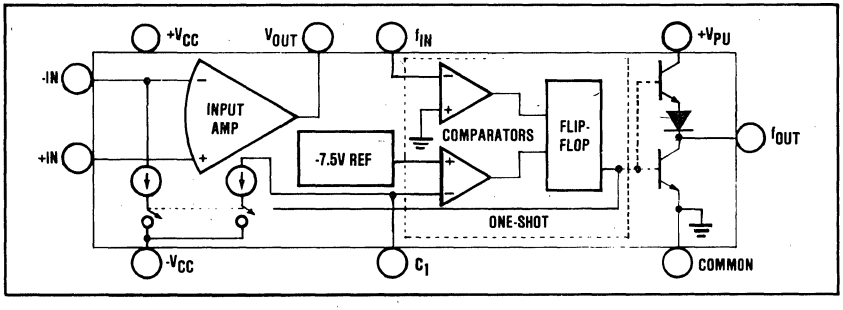
APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- 2-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC62 monolithic voltage-to-frequency and frequency-to voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. In the noise-immune digital form the analog signal may be transmitted long distances without degradation. It may be converted to a binary number with a counter or microprocessor or may be returned to analog form using a frequency-to-voltage converter.

The digital output is an active pull-up type which provides better load driving capability than the usual open collector outputs. Output pulses are DTL, TTL and CMOS compatible. High accuracy (±0.005% max nonlinearity at 10kHz) is achieved with relatively few external components. Only one resistor and two capacitors are required.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted.

CHARACTERISTICS	CONDITIONS	VFC62BG/BM/SM MIN	VFC62BG/BM/SM TYP	VFC62BG/BM/SM MAX	VFC62CG/CM MIN	VFC62CG/CM TYP	VFC62CG/CM MAX	UNITS
V/F CONVERTER $f_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range(1)	Fig. 4 with $e_2 = 0$	> 0		Note 2	*		*	V
	Fig. 4 with $e_1 = 0$	< 0		-10	*		*	V
Current Range(1)	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	*		*	µA
Bias Current								
Inverting Input			4	8		*	*	nA
Noninverting Input			10	30		*	*	nA
Offset Voltage(3)				±0.15			*	mV
Offset Voltage Drift			±5			*		µV/°C
Differential Impedance		300 || 5	650 || 5		*	*		kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		*	*		kΩ || pF
ACCURACY								
Linearity Error(1)(4)(5)	Fig. 4 with e_2 + = 0(6)							
	0.01Hz ≤ f_{OUT} ≤ 10kHz		±0.004	±0.005		±0.0015	±0.002	% of FSR
	0.1Hz ≤ f_{OUT} ≤ 100kHz		±0.008	±0.03		*	*	% of FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0.1			*		% of FSR
Offset Error	Input Offset Voltage(3)			±15			*	ppm of FSR
Offset Drift(7)			±0.5			*		ppm of FSR/°C
Gain Error(3)			±5	±10		*	*	% of FSR
Gain Drift(7)	f = 10kHz			50			20	ppm of FSR/°C
Full Scale Drift (offset drift & gain drift(7)(8)(9)	f = 10kHz			50			20	ppm of FSR/°C
Power Supply Sensitivity	±V_{CC} = 14VDC to 18VDC			±0.015			*	% of FSR/%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			*	MHz
Dynamic Range		6			*			decades
Settling Time	(V/F) to specified linearity for a full scale input step		Note 10			*		
Overload Recovery	< 50% overload		Note 10			*		
ACTIVE PULL-UP OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0.4			*	V
Voltage, Logic "1"		V_{PU} - 2.6		V_{PU}	*		*	V
Duty Cycle at FS	For Best Linearity		25			*		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100			*		nsec
F/V CONVERTER $V_{OUT} = 7.5\ R_1C_1\ F_{IN}$, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 || 10	150 || 10		*	*		kΩ || pF
Logic "1"		+1.0		+V_{CC}	*		*	V
Logic "0"		-V_{CC}		-0.05	*		*	V
Pulse-width Range		0.25			*			µsec
OUTPUT FROM OP AMP								
Voltage	I_O = 7mA	0 to +10			*			V
Current	V_O = 7VDC	+10			*			mA
Impedance	Closed-loop			0.1			*	Ω
Capacitive Load	Without oscillation			100			*	pF
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range, V_{CC}		±13		±20	*		*	V
Pull-up Voltage		+3.5		+V_{CC}	*		*	V
Quiescent Current	not including load current		±6	±6.7		*	*	mA
TEMPERATURE RANGE								
Specification								
B and C Grades				-25 to +85				°C
S Grade				-55 to +125				°C
Operating								
B and C Grades				-25 to +85				°C
S Grade				-55 to +125				°C
Storage		-65		+150	-65		+150	°C

*Specification the same as for VFC62BG/BM/SM.

NOTES:
1. A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity.
2. Determined by R_{IN} and full scale current range constraints.
3. Adjustable to zero. See Offset and Gain Adjustment section.
4. Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section.
5. When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy.
6. For $e_1 = 0$ typical linearity errors are 0.01% at 10kHz, 0.2% at 100kHz.
7. Exclusive of external components drift.
8. FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage).
9. Positive drift is defined to be increasing frequency with increasing temperature.
10. One pulse of new frequency plus 50nsec typical.

ABSOLUTE MAXIMUM RATINGS

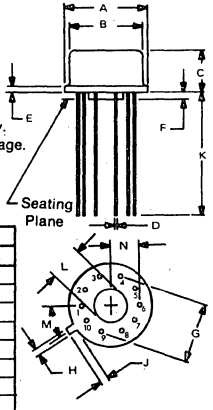
Supply Voltages	±20V
Output Sink Current at f_{OUT}	50mA
Output Current at V_{OUT}	+20mA
Input Voltage, -Input	±V_{CC}
Input Voltage, +Input	±V_{CC}
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

MECHANICAL

VFC62BM, CM/SM TO-100 PACKAGE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

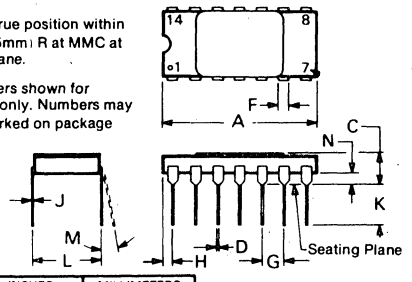


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
	.335	.370	8.51	9.40
	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	---	12.70	---
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

VFC62BG/CG CERAMIC DUAL-IN-LINE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

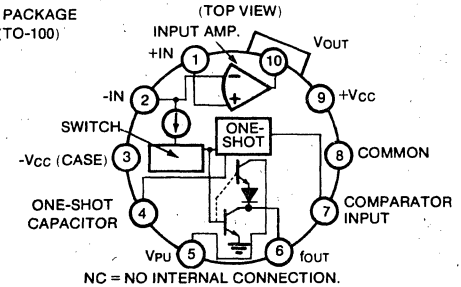
Pin numbers shown for reference only. Numbers may not be marked on package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	---	10°	---	10°
N	.009	.060	0.23	1.52

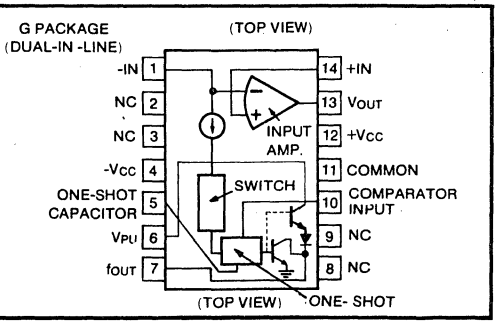
PIN CONFIGURATIONS

M PACKAGE (TO-100) (TOP VIEW)



NC = NO INTERNAL CONNECTION.
EXTERNAL CONNECTION PERMITTED.

G PACKAGE (DUAL-IN-LINE) (TOP VIEW)



DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero). Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ($\Delta f_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC62 makes the device an excellent choice for use as the front end of A/D converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission).

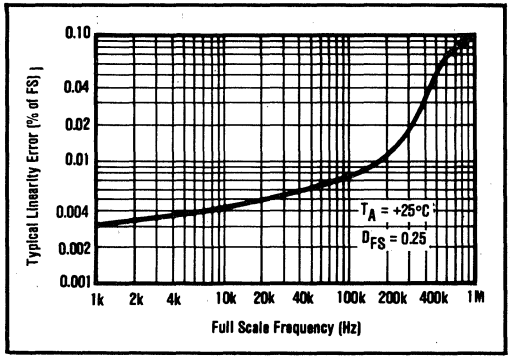


FIGURE 1. Linearity Error vs Full Scale Frequency.

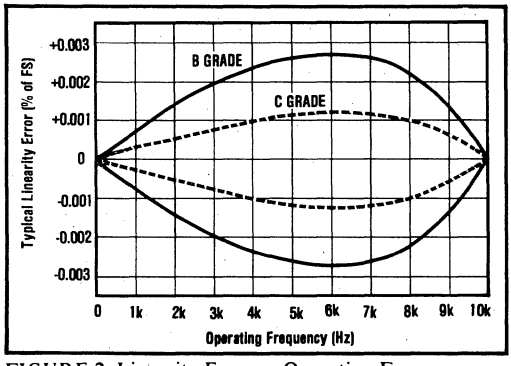


FIGURE 2. Linearity Error vs Operating Frequency.

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC62 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC62.

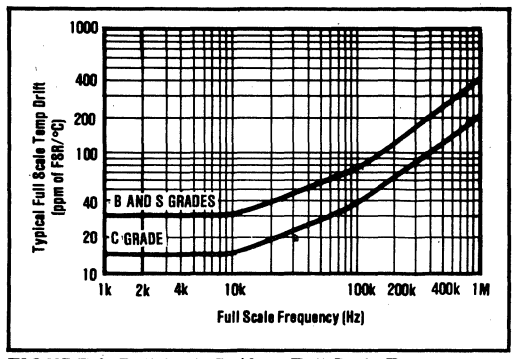


FIGURE 3. Full Scale Drift vs Full Scale Frequency.

RESPONSE

Response of the VFC62 to changes in input signal level is specified for a full scale step, and is 50nsec plus 1 pulse of the new frequency. For a 10V input signal step with the VFC62 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 10μsec.

THEORY OF OPERATION

The VFC62 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a one-shot), two switched current sinks, and an active pull-up output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at V_{IN}, a current will flow through the input resistor, causing the voltage at V_{OUT} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_1 until V_{C1} = -7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this -7.5V threshold comparator B resets the flip-flop, and the ramp voltage begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor, C_1. After the one-shot resets, f_{OUT} changes back to logic 0 and the cycle begins again.

The transfer function for the VFC62 is derived as follows

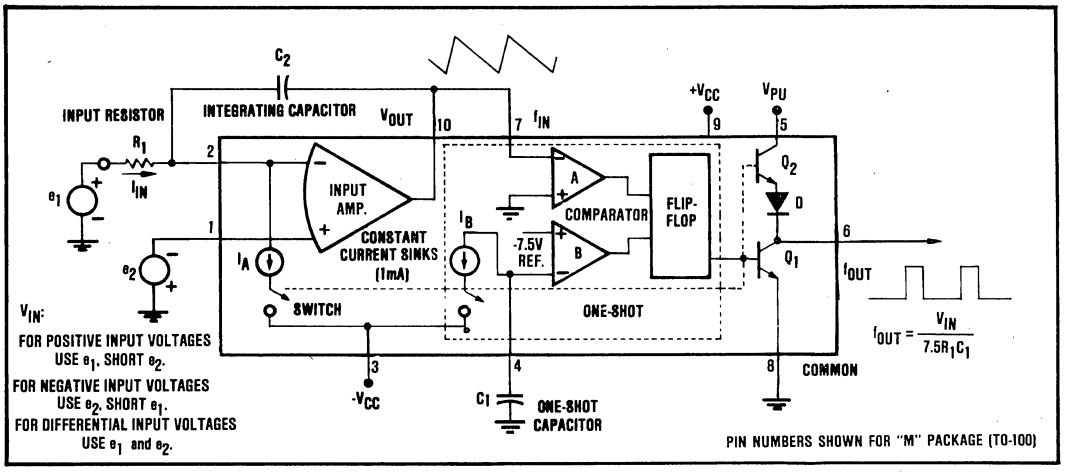


FIGURE 4. Functional Block Diagram of the VFC62.

for the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \quad (1)$$

In the time $t_1 + t_2$, the integrator capacitor C_2 charges and discharges but the net voltage change is zero.

$$\text{Thus } \Delta Q = 0 = I_{IN}\, t_1 + (I_{IN} - I_A)\, t_2 \quad (2)$$

$$\text{So that } I_{IN}(t_1 + t_2) = I_A\, t_2 \quad (3)$$

$$\text{But since } t_1 + t_2 = \frac{1}{f_{OUT}} \text{ and } I_{IN} = \frac{V_{IN}}{R_1} \quad (4), (5)$$

$$f_{OUT} = \frac{V_{IN}}{I_A R_1 t_2} \quad (6)$$

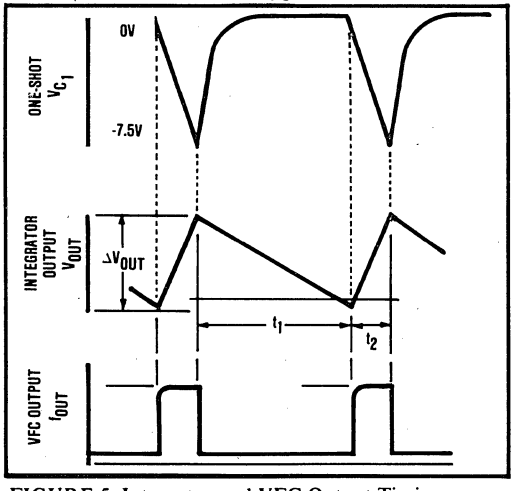


FIGURE 5. Integrator and VFC Output Timing.

In the time t_2, I_B charges the one-shot capacitor C_1 until its voltage reaches -7.5V and trips comparator B.

$$\text{Thus } t_2 = \frac{C_1\, 7.5}{I_B} \quad (7)$$

$$\text{Using (7) in (6) yields } f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \times \frac{I_B}{I_A} \quad (8)$$

Since $I_A = I_B$ the result is

$$f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \quad (9)$$

Since the integrating capacitor, C_2, affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to I_{IN}, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC62 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. e_1 and e_2 are shorted and F_{IN} is disconnected from V_{OUT}. F_{IN} is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by C_1 as before, but the cycle repetition frequency will be dictated by the digital input at F_{IN}.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). For the VFC62, t_2 is fixed and $t_1 + t_2$ varies as the input voltage. Thus the duty cycle is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, D_{FS}, which occurs at full scale input. D_{FS} is a user-determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = PW \times f_{FS}$$

Best linearity is achieved when D_{FS} is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN}\ max\ /\ R_1}{1mA} = \frac{I_{IN}\ max}{1mA}$$

Thus $D_{FS} = 0.25$ corresponds to $I_{IN}\ max = 0.25mA$.

INSTALLATION AND OPERATING INSTRUCTIONS

VOLTAGE-TO-FREQUENCY CONVERSION

The VFC62 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

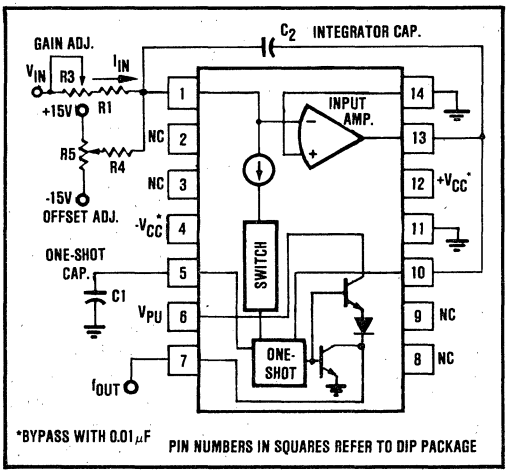


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

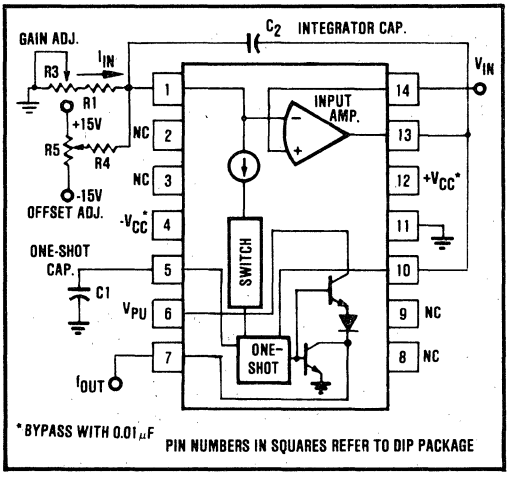


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

EXTERNAL COMPONENT SELECTION

In general the design sequence consists of: (1) choosing f_{MAX}, (2) choosing the duty cycle at full scale ($D_{FS} = 0.25$ typically), (3) determining the input resistor, R_1 (Figure 4), (4) calculating the one-shot capacitor, C_1, and (5) selecting the integrator capacitor C_2.

Input Resistors R_1 and R_3

The input resistance (R_1 and R_3 in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than $D_{FS} = 0.25$ may be used but linearity will be affected. The nominal value of R_1 is

$$R_1 = \frac{V_{IN}\ max}{0.25mA} \qquad (10)$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of C_1 and the desired trim range. R_1 should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

One-Shot Capacitor, C_1

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_{1\ nom} = \frac{V_{IN}}{7.5\ R_1\ f_{OUT}} \qquad (11)$$

For the usual 25% duty at $f_{MAX} = V_{IN}/R_1 = 0.25mA$ there is approximately 15pF of residual capacitance so that the design value is

$$C_1\ (pF) = \frac{33 \times 10^6}{f_{FS}} - 15 \qquad (12)$$

where f_{FS} is the full scale output frequency in Hz. The temperature drift of C_1 is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with C_1. It should be mounted as close to the VFC62 as possible. Figure 8 shows pulse width and full scale frequency for various values of C_1 at $D_{FS} = 25\%$.

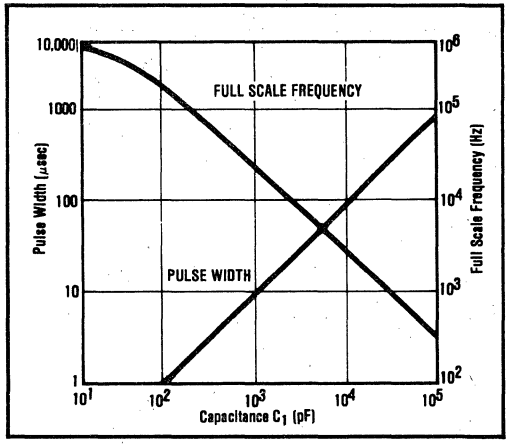


FIGURE 8. Output Pulse Width ($D_{FS} = 0.25$) and Full Scale Frequency vs External One-shot Capacitance.

Integrating Capacitor, C_2

Since C_2 does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in C_2 causes a gain error. A ceramic type is sufficient for most applications. The value of C_2 determines the amplitude of V_{OUT}. Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator

determine a range of acceptable values,

$$C_2\ (\mu F) = \begin{cases} \frac{100}{f_{FS}}\ ;\ \text{if } f_{FS} \leq 100\text{kHz} \\ 0.001;\ \text{if } 100\text{kHz} < f_{FS} \leq 500\text{kHz} \\ 0.0005;\ \text{if } f_{FS} > 500\text{kHz} \end{cases} \quad (13)$$

Trimming Components R_3, R_4, R_5

R_5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R_4 can be a 10% carbon film resistor with a value of 10MΩ.

R_3 nulls the gain errors of the converter and compensates for intitial tolerances of R_1 and C_1. Its total resistance should be at least 20% of R_1, if R_1 is selected 10% low. Its temperature coefficient should be no greater than five times that of R_1, to maintain a low drift of the R_3 - R_1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 x full scale.
2. Adjust R_5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R_3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC62 is 0.015% of FSR/% maximum. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

Internal circuitry causes some current to flow in the common connection (pin 11 on DIP package). Current flowing into the f_{OUT} pin (logic sink current) will also contribute to this current. It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by these currents flowing through any ground return impedance.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1 ($D_{FS} = 0.25$)

$C_1 = [(33 \times 10^6)/f_{MAX}] - 15$ $\quad [(66 \times 10^6)/f_{MAX}] - 15$ if $D_{FS} = 0.5$

$= [(33 \times 10^6)/100\text{kHz}] - 15$

$= 315\text{pF}$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

Selecting R_1 and R_3 ($D_{FS} = 0.25$)

$R_1 + R_3 = V_{IN}\ \text{max}/0.25\text{mA}$ $\quad V_{IN}\ \text{max}/0.5\text{mA}$ if $D_{FS} = 0.5$

$= 10\text{V}/0.25\text{mA}$

$= 40\text{k}\Omega$

Choose 32.4kΩ metal film resistor with 1% tolerance and R_3 = 10kΩ cermet potentiometer.

Selecting C_2

$C_2 = 10^2/F_{max}$

$= 10^2/100\text{kHz}$

$= 0.001\mu\text{F}$

Choose a 0.001μF capacitor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC62 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C_3 to make t = 0.1T (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero to insure that the input signal at pin 10 crosses the zero threshold. Errors are nulled following the procedure given on this page, using 0.001 x full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

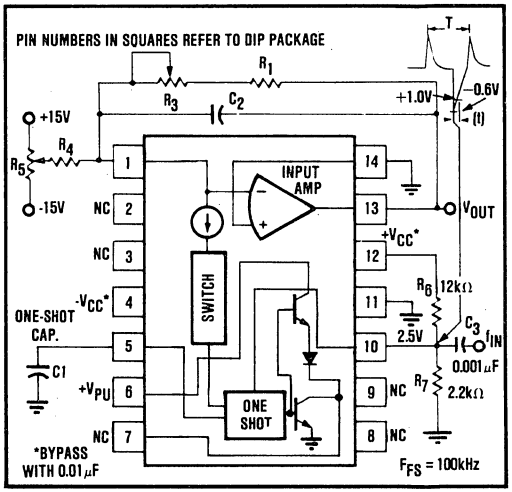


FIGURE 9. Connection Diagram for F/V Conversion.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC62 ideal for a variety of VFC applications. High accuracy allows the VFC62 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits.

Figures 10 - 14 show typical applications of the VFC62.

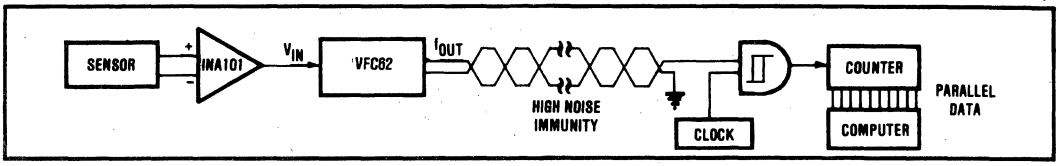


FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.

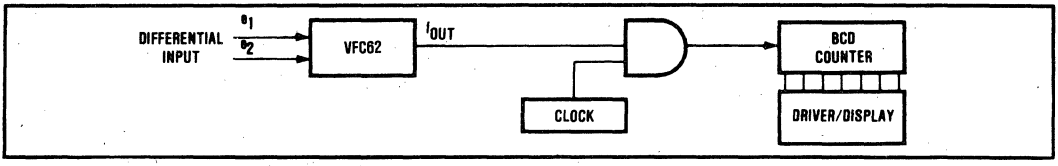


FIGURE 11. Inexpensive Digital Panel Meter.

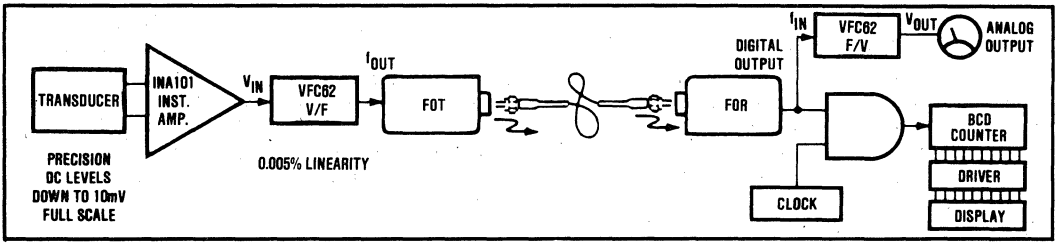


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

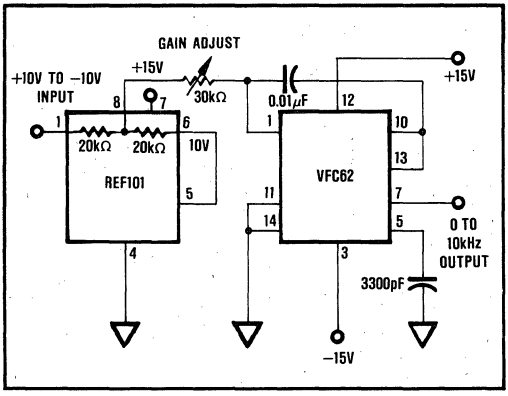


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

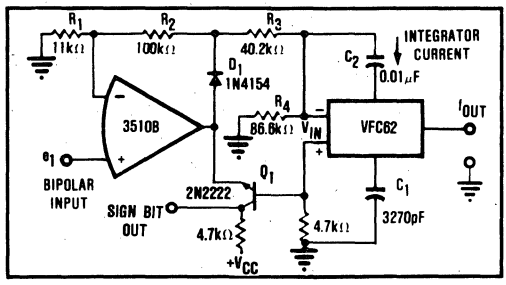


FIGURE 14. Absolute value circuit with the VFC62. Op amp, D_1 and Q_1 (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $|e_1|$. The sign bit output provides indication of the input polarity.

BURR-BROWN®

VFC100

Synchronized VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- FULL-SCALE FREQUENCY SET BY SYSTEM CLOCK, NO CRITICAL EXTERNAL COMPONENTS REQUIRED
- PRECISION 10V FULL-SCALE INPUT, 0.5% MAX GAIN ERROR
- ACCURATE 5V REFERENCE VOLTAGE
- EXCELLENT LINEARITY, 0.02% MAX AT 100kHz FS
  0.1% MAX AT 1MHz FS
- VERY-LOW GAIN DRIFT, 50ppm/°C

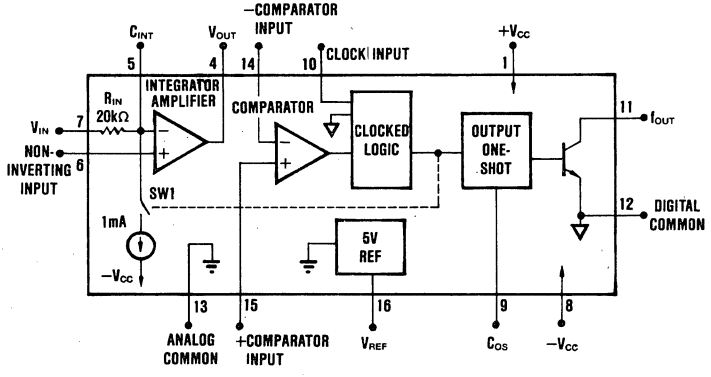
APPLICATIONS

- A/D CONVERSION
- PROCESS CONTROL
- DATA ACQUISITION
- VOLTAGE ISOLATION

DESCRIPTION

The VFC100 voltage-to-frequency converter is an important advance in VFCs. The well-proven charge balance technique is used, however, the critical reset integration period is derived from an external clock frequency. The external clock accurately sets an output full-scale frequency, eliminating error and drift from the external timing components required for other VFCs. A precision input resistor is provided which accurately sets a 10V full-scale input voltage. In many applications the required accuracy can be achieved without external adjustment.

The open collector active-low output provides fast fall time on the important leading edge of output pulses, and interfaces easily with TTL and CMOS circuitry. An output one-shot circuit is particularly useful to provide optimum output pulse widths for optical couplers and transformers to achieve voltage isolation. An accurate 5V reference is also provided which is useful for applications such as offsetting for bipolar input voltages, exciting bridges and sensors, and autocalibration schemes.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC supplies unless otherwise noted.

PARAMETER	CONDITIONS	VFC100AG/SG MIN	VFC100AG/SG TYP	VFC100AG/SG MAX	VFC100BG MIN	VFC100BG TYP	VFC100BG MAX	UNITS
TRANSFER FUNCTION								
Voltage-to-Frequency Mode	$f_{OUT} = f_{CLOCK} \times (V_{IN}/20V)$							
Gain Error[1]	FSR = 100kHz		±0.5	±1		±0.2	±0.5	% of FSR
Linearity Error	FSR = 100kHz,		±0.01	±0.025		"	±0.02	% of FSR
	over temp.							
	FSR = 500kHz, C_{OS} = 60pF		±0.015			"	±0.05	% of FSR
	FSR = 1MHz, C_{OS} = 60pF		±0.025			"	±0.1	% of FSR
Gain Drift[2]	FSR = 100kHz		±70	±100		±30	±50	ppm of FSR/°C
Referred to Internal V_{REF}			10	±25		10	±15	ppm of FSR/°C
Offset Referred to Input			±1	±3		±1	±2	mV
Offset Drift			±12	±100		±6.5	±25	µV/°C
Power Supply Rejection	Full supply range			0.01			"	%/V
Response Time	to Step Input Change		One period of new output frequency plus one clock period					
Current-to-Frequency Mode	$f_{OUT} = f_{CLOCK} \times (I_{IN}/1mA)$							
Gain Error			±0.5	±1		±0.2	±0.5	% of FSR
Gain Drift[2]			±120	±200		±80	±140	ppm of FSR/°C
Frequency-to-Voltage Mode[3]	$V_{OUT} = 20V \times (f_{IN}/f_{CLOCK})$							
Gain Accuracy[1]	FSR = 100kHz		±0.5	±1		±0.2	±0.5	%
Linearity	FSR = 100kHz		±0.01	±0.025		"	±0.02	%
Input Resistor (R_{IN})								
Resistance		19.8	20	20.2	"	"	"	kΩ
Temperature Coefficient (T_C)[2]			±50	±100		"	"	ppm/°C
INTEGRATOR OP AMP								
V_{OS}[1]			±150	±1000		"	"	µV
V_{OS} Drift			±5			"		µV/°C
I_B			±50	±100		±25	±50	nA
I_{OS}			100	200		50	100	nA
A_{OL}	Z_{LOAD} = 5KΩ/10000pF	100	120		"	"		dB
CMRR		80	105		"	"		dBV
CM Range		−7.5		+0.1	"		"	V
V_{OUT} Range	Z_{LOAD} = 5kΩ/10000pF	−0.2		+12		"	"	V
Bandwidth			14			"		MHz
COMPARATOR INPUTS								
Input Current (operating)	$-11V < V_{COMPARATOR} < +V_{CC} - 2V$			5			"	µA
CLOCK INPUT (referenced to digital common)								
Frequency (maximum operating)			4.0			"		MHz
Threshold Voltage			1.4			"		V
	Over temperature	0.8		2.0	"		"	V
Voltage Range (operating)		$-V_{CC}$ + 2V		$+V_{CC}$ − 2V	"		"	V
Input Current	$-V_{CC} < V_{CLOCK} < +V_{CC}$		0.5	5		"	"	µA
Rise Time				2			"	µsec
OPEN COLLECTOR OUTPUT (referenced to digital common)								
V_{OL}	I_{OUT} = 10mA			0.4			"	V
I_{OL}				15			"	mA
I_{OH} (off leakage)	V_{OH} = 30V		.01	10		"	"	µA
Delay Time, positive clock edge to output pulse			300			"		nsec
Fall Time			100			"		nsec
Output Capacitance			5			"		pF
OUTPUT ONE-SHOT								
	Nominal PW_{OUT} = (5nsec/pF) × C_{OS} − 90nsec							
Pulse Width Out	C_{OS} = 300pF	1	1.4	2	"	"	"	µsec
REFERENCE VOLTAGE								
Accuracy	No load	4.90	5.0	5.10	4.95	"	5.05	V
Drift[2]			±60	±150		±40	±100	ppm/°C
Current Output	(Sourcing capability)	10				"		mA
Power Supply Rejection				0.015			0.015	%/V
Output Impedance			0.5	2		"	"	Ω
POWER SUPPLY								
Rated Voltage			±15			"		V
Operating Voltage Range (see Figure 9)								
	$+V_{CC}$	+7.5		+28.5	"		"	V
	$-V_{CC}$	−7.5		−28.5	"		"	V
Total Supply	$+V_{CC} - (-V_{CC})$	15		36	"		"	V
Digital Common		$-V_{CC}$ + 2		$+V_{CC}$ − 4	"		"	V
Quiescent Current: $+I_{CC}$	Over temperature		10.6	15		"	"	mA
$-I_{CC}$			9.6	15		"	"	mA

ELECTRICAL (CONT)

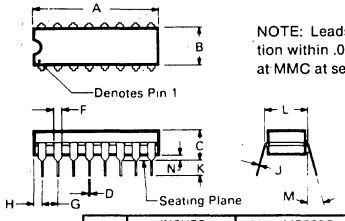
At T_A = +25°C and ±15VDC supplies unless otherwise noted.

PARAMETER	CONDITIONS	VFC100AG/SG			VFC100BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	AG/BG	−25		+85	*		*	°C
	SG	−55		+125				°C
Storage	AG/BG/SG	−65		+150	*		*	°C
θ Junction—ambient			150			*		°C/W
θ Junction—case			100			*		°C/W

*Specification same as AG grade.

NOTES: (1) Offset and gain error can be trimmed to zero. See text. (2) Specified by the box method: (Max. − Min.) ÷ (Avg. × ΔT). (3) Refer to detailed timing diagram in Figure 16 for frequency input signal timing requirements.

MECHANICAL



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.760	.885	19.30	22.48
B	.220	.280	5.59	7.11
C	---	.200	---	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100		2.54	
L	.300 BASIC		7.62 BASIC	
M	---	15°		15°
N	.020	.050	0.51	1.27

ABSOLUTE MAXIMUM RATINGS

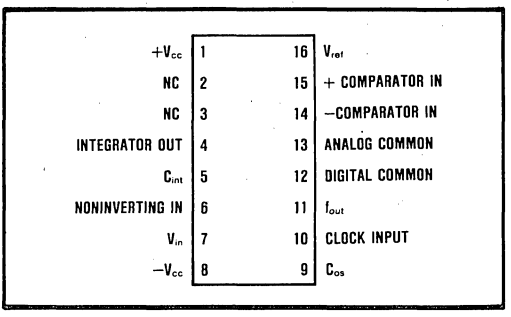
Power Supply Voltage (+V_{CC} to −V_{CC})	36V
+V_{CC} to Analog Common	28V
−V_{CC} to Analog Common	28V
Integrator Out Short-Circuit-to-Ground	Indefinite
Integrator Differential Input	±10V
Integrator Common-Mode Input	−V_{CC} +5V to +2V
V_{IN} (pin 7)	±V_{CC}
Clock Input	±V_{CC}
V_{REF} Out Short-Circuit-to-Ground	Indefinite
Pin 9 (C_{OS})	0 to +V_{CC}
f_{OUT} (referred to digital common)	−0.5V to 36V
Digital Common	±V_{CC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering 10sec)	300°C

ORDERING INFORMATION

VFC100 (X) G

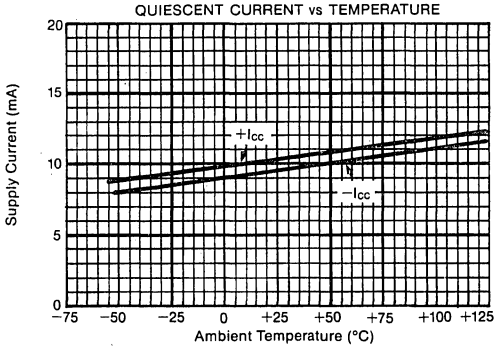
- Basic Model Number
- Performance Code
  - A, B = −25°C to +85°C
  - S = −55°C to +125°C
- Ceramic Package

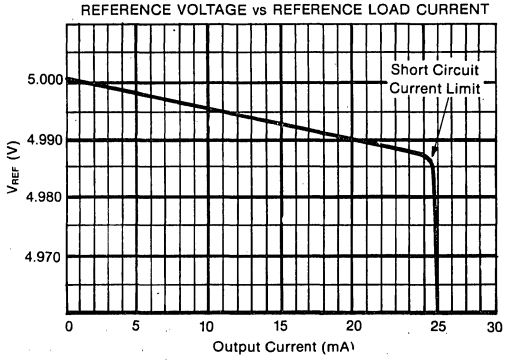
PIN CONFIGURATION



TYPICAL PERFORMANCE CURVES

At +25°C, ±V_{CC} = 15VDC, and in circuit of Figure 1 unless otherwise specified.





THEORY OF OPERATION

The VFC100 monolithic voltage-to-frequency converter provides a digital pulse train output with an average frequency proportional to the analog input voltage. The output is an active low pulse of constant duration, with a repetition rate determined by the input voltage. Falling edges of the output pulses are synchronized with rising edges of the clock input.

Operation is similar to a conventional charge balance VFC. An input operational amplifier (Figure 1) is configured as an integrator so that a positive input voltage causes an input current to flow in R_{IN}. This forces the integrator output to ramp negatively. When the output of the integrator crosses the reference voltage (5V), the comparator trips, activating the clocked logic circuit. Once activated, the clocked logic awaits a falling edge of the clock input, followed by a rising edge (see Figure 2). On the rising edge, switch S1 is closed for one complete clock cycle, causing the reset current, I_1 to switch to the integrator input. Since I_1 is larger than the input current, I_{IN}, the output of the integrator ramps positively during the one clock cycle reset period. The clocked logic circuitry also generates a VFC output pulse during the reset period.

Unlike conventional VFC circuits, the VFC100 accurately derives its reset period from an external clock frequency. This eliminates the critical timing capacitor required by other VFC circuits. One period (from rising edge to rising edge) of the clock input determines the integrator reset period.

When the negative-going integration of the input signal crosses the comparator threshold, integration of the input signal will continue until the reset period can start (awaiting the necessary transitions of the clock). Output pulses are thus made to align with rising edges of the external clock. This causes the instantaneous output frequency to be a subharmonic of the clock frequency. The average frequency, however, will be an accurate analog of the input voltage.

A full scale input of 10V (or an input current of 0.5mA) causes a nominal output frequency equal to one half the

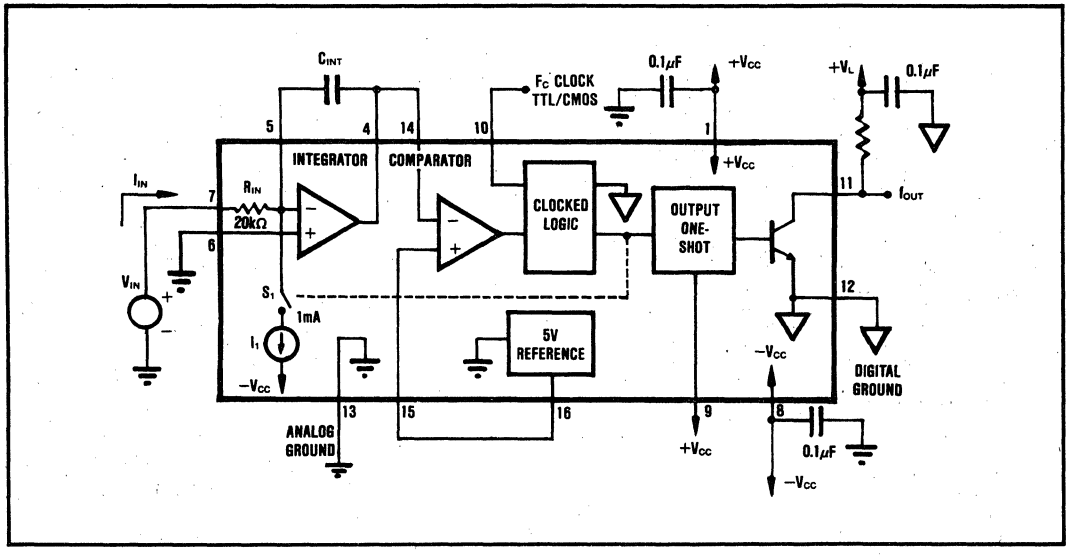


FIGURE 1. Circuit Diagram for Voltage-to-Frequency Mode.

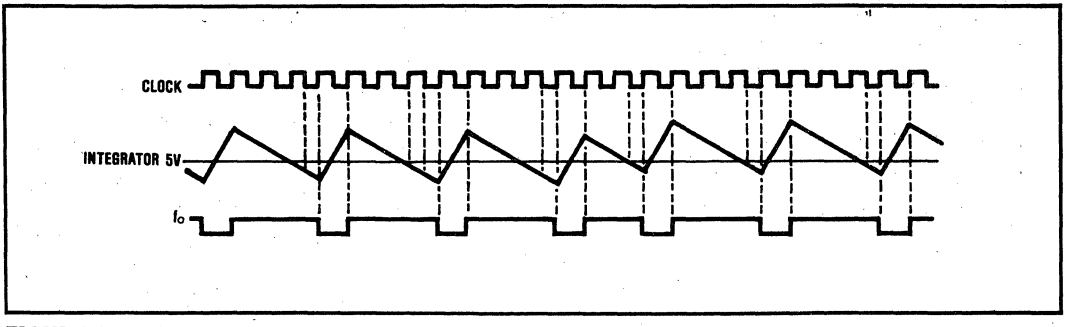


FIGURE 2. Timing Diagram for Voltage-to-Frequency Mode.

clock frequency. The transfer function is

$$f_{OUT} = (V_{IN}/20V)\, f_{CLOCK}$$

Figure 3 shows the transfer function graphically. Note that inputs above 10V (or 0.5mA) do not cause an increase in the output frequency. This is an easily detectable indication of an overrange input. In the overrange condition, the integrator amplifier will ramp to its negative output swing limit. When the input signal returns to within the linear range, the integrator amplifier will recover and begin ramping upward during the reset period.

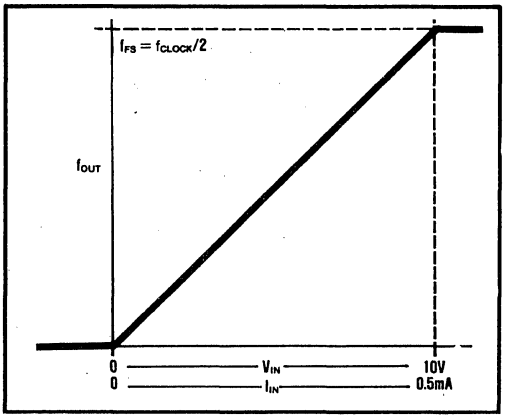


FIGURE 3. Transfer Function for Voltage-to-Frequency Mode.

INSTALLATION AND OPERATING INSTRUCTIONS

The integrator capacitor C_{INT} (see Figure 1) affects the magnitude of the integrator voltage waveform. Its absolute accuracy is not critical since it does not affect the transfer function. This allows a wide range of capacitance to produce excellent results. Figure 4 facilitates choosing an appropriate standard value to assure that the integrator waveform voltage is within acceptable limits. Good dielectric absorption properties are required to achieve best linearity. Mylar®, polycarbonate, mica, polystyrene, Teflon® and glass types are appropriate choices. The choice in a given application will depend on the particular value and size considerations. Ceramic capacitors vary considerably from type to type and some produce significant nonlinearities. Polarized capacitors should not be used.

Deviation from the nominal recommended +1V to −0.75V integrator voltage (as controlled by the integrator capacitor value) is permissible and will have a negligible effect on VFC operation. Certain situations may make deviations from the suggested integrator swing highly desirable. Smaller integrator voltages, for instance, allow more "headroom" for averaging noisy input signals. The VFC is a fully integrating input converter, able to reject large levels of interfering noise. This ability is limited only by the output voltage swing range of the integrator amplifier. By setting a small integrator voltage swing using a large C_{INT} value, larger levels of noise can be integrated without output saturation and loss of accuracy. For instance, with a 50kHz full-scale output and $C_{INT} = 0.1\mu F$, the circuit in Figure 1 can accurately average an input through the full 0 to 10V input range with 1V p-p superimposed 60Hz noise.

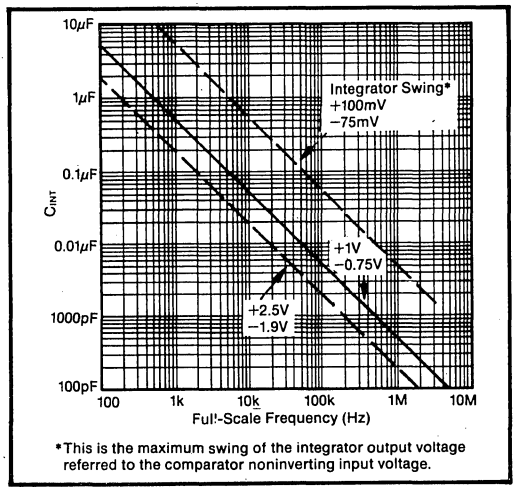


FIGURE 4. Integrator Capacitor Selection Graph.

The integrator output voltage should not be allowed to exceed +12V or −0.2V, otherwise saturation of the operational amplifier could cause inaccuracies. Operation with positive power supplies less than +15V will limit the output swing of the integrator operational amplifier. Smaller integrator voltage waveforms may be required to avoid output saturation of the integrator amplifier. See "Power Supply Considerations" for information on low voltage operation.

The maximum integrator voltage swing requirement is nearly symmetrical about the comparator threshold voltage (see Figure 12). One-third greater swing is required above the threshold than below it. Maximum demand on positive integrator swing occurs at low scale, while the negative swing is greatest just below full scale.

CLOCK INPUT

The clock input is TTL- and CMOS-compatible. Its input threshold is approximately 1.4V (two diode voltage drops) referenced to digital ground (pin 12). The clock "high" input may be standard TLL or may be as high as $+V_{CC} - 2V$. A CMOS clock should be powered from a voltage source at least 2V below the VFC100's $+V_{CC}$ to prevent overdriving the clock input. Alternatively, a resistive voltage divider may be used to limit the clock voltage swing to $+V_{CC} - 2V$ maximum. The clock input has a high input impedance, so no special drivers are required. Rise time in the transition region from 0.5V to 2V must be less than 2μsec for proper operation.

OUTPUT

The frequency output is an open collector current-sink transistor. Output pulses are active low such that the

output transistor is on only during the reset integration period (see Shortened Output Pulses). This minimizes power dissipation over the full frequency range and provides the fastest logic edge at the beginning of the output pulse where it is most desirable.

Interface to a logic circuit would normally be made using a pull-up resistor to the logic power supply. Selection of the pull-up resistor should be made such that no more than 15mA flows in the output transistor. The actual choice of the pull-up resistor may depend on the full-scale frequency and the stray capacitance on the output line. The rising edge of an output pulse is determined by the RC time constant of the pull-up resistor and the stray capacitance. Excessive capacitance will produce a rounding of the output pulse rising edge, which may create problems driving some logic circuits. If long lines must be driven, a buffer or digital line transmitter circuit should be used.

The synchronized nature of the VFC100 makes viewing its output on an oscilloscope somewhat tricky. Since all output pulses align with the clock, it is best to trigger and view the clock on one of the input channels and the output can then be viewed on another oscilloscope channel. Depending on the VFC input voltage, the output waveform may appear as if the oscilloscope is not properly triggered. The output might best be visualized by imagining a constant output frequency which is locked to a submultiple of the clock frequency with occasional extra pulses or missing pulses to create the necessary average frequency. It is these extra or missing pulses that make the output waveform appear as if the oscilloscope is not properly triggered. This is normal. Experimentation with the input voltage and oscilloscope triggering will generally allow a stable view of the output and provides an understanding of its nature.

SHORTENED OUTPUT PULSES

In normal operation, the negative output pulse duration is equal to one period of the clock input. Shorter output pulses may be useful in driving optical couplers or transformers for voltage isolation or noise rejection. This can be accomplished by connecting capacitor C_{OS} as shown in Figure 5. Pin 9 may be connected to $+V_{CC}$, deactivating the output one-shot circuit. The value of C_{OS} is chosen according to the curve in Figure 6. Output pulses cannot be made to exceed one clock period in duration. Thus, a C_{OS} value which would create an output pulse which is longer than one period of the clock will have the same effect as disabling the one-shot, causing the output pulse to last one clock period. The minimum practical pulse width of the one-shot circuit is approximately 100nsec. Using C_{OS} to generate shorter output pulses does not affect the output frequency or the gain equation.

REFERENCE VOLTAGE

Excellent gain drift is achieved by use of a precision internal 5V reference. This reference is brought to an external pin and can be used for a variety of purposes. It is used to offset the noninverting comparator input in voltage-to-frequency mode (although a precise voltage is not requried for this function). It is very useful in many other applications such as offsetting the input to handle bipolar input signals. It can source up to 10mA and sink

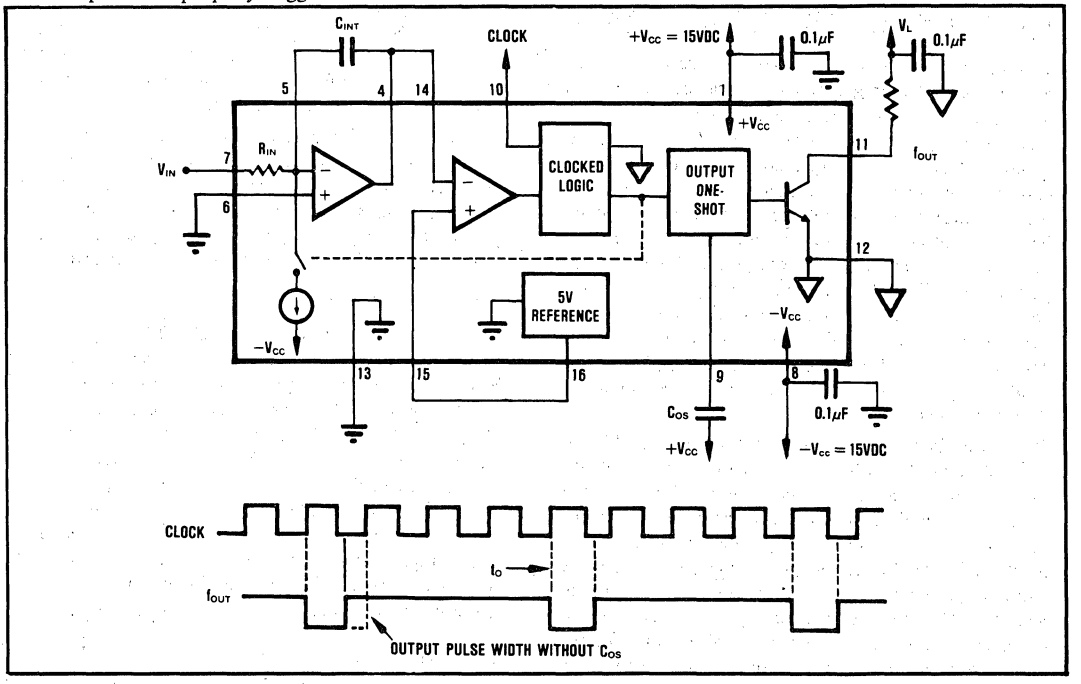


FIGURE 5. Circuit and Timing Diagram for Shortened Output Pulses.

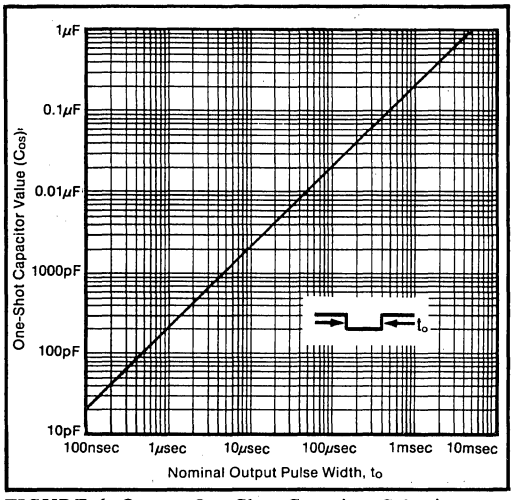


FIGURE 6. Output One-Shot Capacitor Selection Graph.

100μA. Heavy loading of the reference will change the gain of the VFC as well as affecting the external reference voltage. For instance, a 10mA load interacting with a 0.5Ω typical output impedance will change the VFC gain equation and reference voltage by 0.1%.

Figure 7 shows the reference used to offset the VFC transfer function to convert a −5V to +5V input to zero to 500kHz output. The circuit in Figure 8 uses the reference to excite a 300Ω bridge transducer. R_1 provides the majority of the current to the bridge while the V_{REF} output supplies the balance and accurately controls the bridge voltage. The VFC gain is inversely proportional to the reference voltage, V_{REF}. Since the bridge gain is directly proportional to its excitation voltage, the two equal and opposite effects cancel the effect of reference voltage drift on gain.

The reference output amplifier is specifically designed for excellent transient response to provide precision in a noisy environment. Although not required for normal operation, a 0.05μF bypasss capacitor from the reference

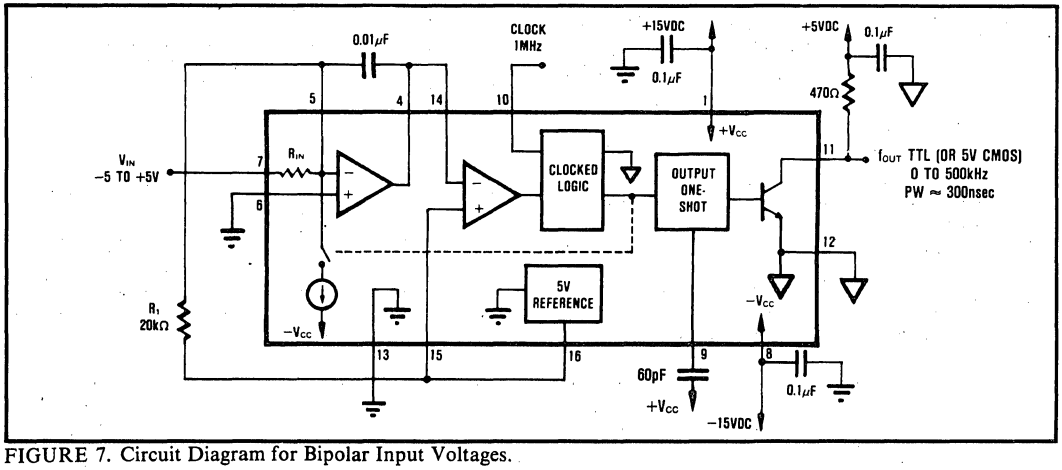


FIGURE 7. Circuit Diagram for Bipolar Input Voltages.

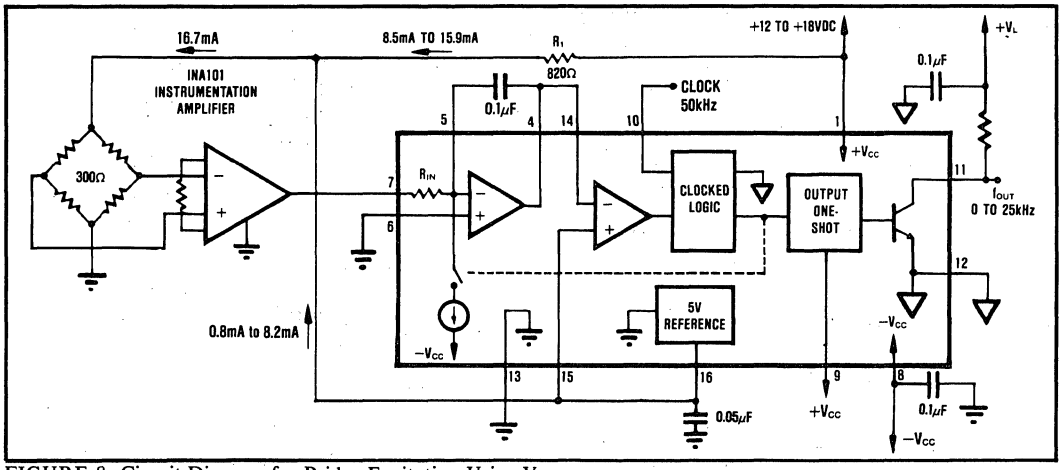


FIGURE 8. Circuit Diagram for Bridge Excitation Using V_{REF}.

output to analog ground (pin 13) may improve the rejection of digital noise from external circuitry.

OTHER INPUT VOLTAGE RANGES

The internal input resistor, $R_{IN} = 20k\Omega$, sets a full-scale input of 10V. Other input ranges can be created by using an external gain set resistor connected to pin 5. Since the excellent temperature drifts of the VFC100 are achieved by careful matching of internal temperature coefficients, use of an external gain set resistor will generally degrade this drift. Using an external resistor to set the gain, the resulting gain drift would be equal to the sum of the external resistor drift and the specified current gain drift of the VFC100. Different voltage input ranges are best implemented by using the internal input resistor, R_{IN}, in series or parallel with a high quality external resistor, thus maintaining as much of the precision temperature tracking as possible.

For best drift performance, the adjustment range of a fine gain trim should be made as narrow as practical. R_1 and R_2 in Figure 9 allow gain adjustment over a ±1% range (adequate to trim the 100kHz FS gain error to zero) and will not significantly affect the drift performance of the VFC100. R_3,R_4,and R_5 allow trimming of the integrator amplifier input offset voltage. The adjustment range is determined by the ratio of R_4 to R_5. Accurate end-point calibration would be performed by first adjusting the offset trim so that zero volts input just causes all output pulses to cease. The gain trim is then adjusted for the proper full-scale output frequency with an accurate full-scale output frequency with an accurate full scale input voltage.

A different input voltage range could also be made by using only a portion of the normal input range of the VFC. For instance, a 2V full-scale input could be created by using the internal input resistor and a clock frequency of 10 times the desired full-scale output frequency.

LINEARITY PERFORMANCE

The linearity of the VFC100 is specified as the worst-case deviation from a straight line defined by low scale and high scale endpoint measurements. This worst-case deviation is expressed as a percentage of the 10V full-scale input. All units are tested and guaranteed for the specified level of performance.

Linearity performance and gain error change with full-scale operating fequency as shown in Figure 10. Figure 11 shows the typical shape of the nonlinearity at 100kHz full scale. Integrator voltage swing (determined by C_{INT}) has a minor effect on linearity. Small integrator voltage swing typically leads to best linearity performance.

Best linearity performance at high full-scale frequencies (above 500kHz) is obtained by using short output pulses

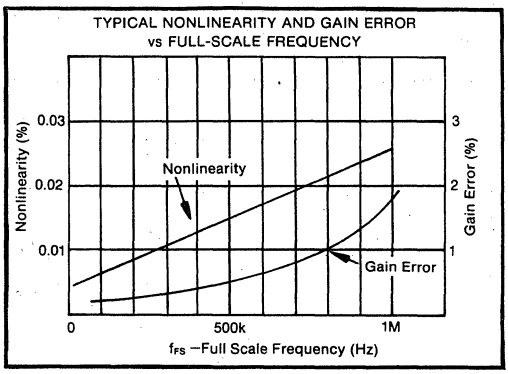


FIGURE 10. Nonlinearity and Gain Error vs Full Scale Frequency.

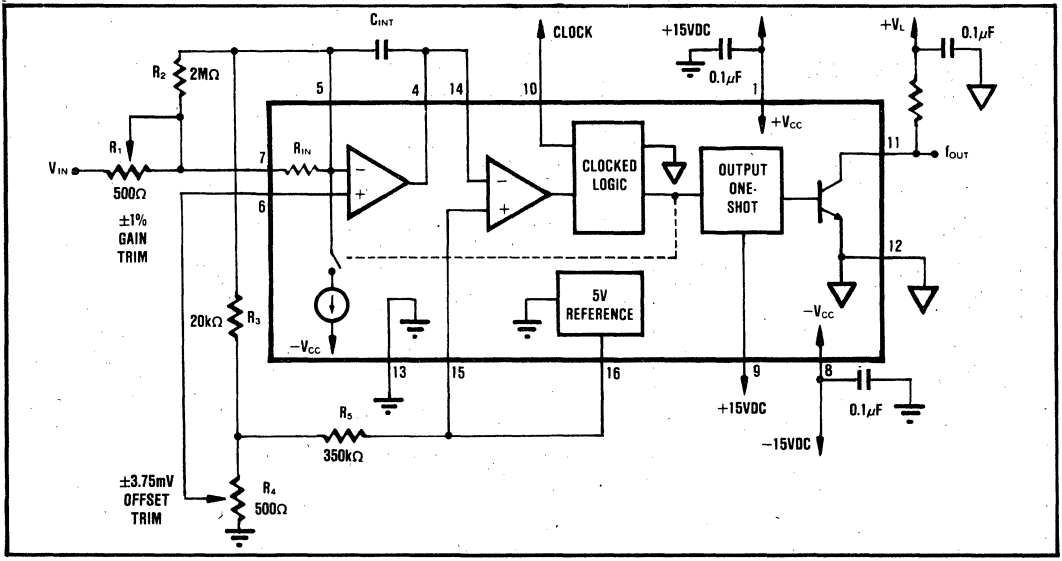


FIGURE 9. Circuit Diagram for Fine Offset and Gain Trim.

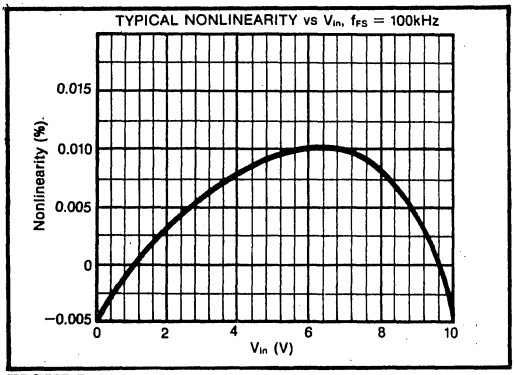


FIGURE 11. Typical Nonlinearity vs V_{IN}.

with a one-shot capacitor of 60pF. As with any high-frequency circuit, careful attention to good power supply bypassing techniques (see "Power Supplies and Grounding") is also required.

TEMPERATURE DRIFT

Conventional VFC circuits are affected significantly by external component temperature drift. Drift of the external input resistor and timing capacitor required with these devices may easily exceed the specified drift of the VFC itself.

When used with its internal input resistor, the gain drift of the complete VFC100 circuit is totally determined by the performance of the VFC100. Gain drift is specified at a full scale output frequency of 100kHz. Conventional VFC circuits usually specify drift at 10kHz and degrade significantly at higher operating frequency. The VFC-100's gain drift remains excellent at higher operating frequency, typically remaining within specification at f_{FS} = 1MHz.

Drift of the external clock frequency directly affects the output frequency, but by using a common clock for the VFC and counting circuitry this drift can be cancelled (see Counting the Output).

POWER SUPPLIES AND GROUNDING

Separate analog and digital grounds are provided on the VFC100 and it is important to separate these grounds to attain greatest accuracy. Logic sink current flowing in the f_{OUT} pin is returned to the digital ground. If this "noisy" current were allowed to flow in analog ground, errors could be created. Although analog and digital grounds may eventually be connected together at a common point in the circuitry, separate circuit connections to this common point can reduce the error voltages created by varying currents flowing through the ground return impedance. The +5V V_{REF} pin is referenced to analog ground.

The power supplies should be well bypassed using capacitors with low impedance at high frequency. A value of 0.1μF is adequate for most circuit layouts.

The VFC100 is specified for a nominal supply voltage of ±15V. Supply voltages ranging from ±7.5V to ±18V may be used. Either supply can be up to 28V as long as the total of both does not exceed 36V. Steps must be taken, however, to assure that the integrator output does not exceed its linear range. Although the integrator output is capable of 12V output swing with 15V power supplies, with 7.5V supplies, output swing will be limited to approximately 4.5V. In this case, the comparator input

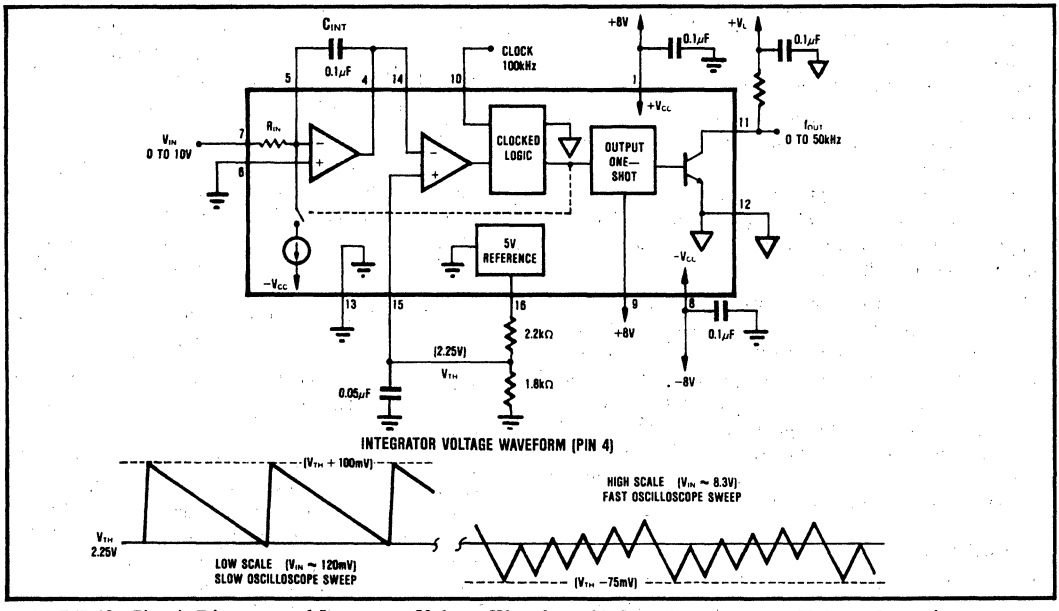


FIGURE 12. Circuit Diagram and Integrator Voltage Waveform for Low Power Supply Voltage Operation.

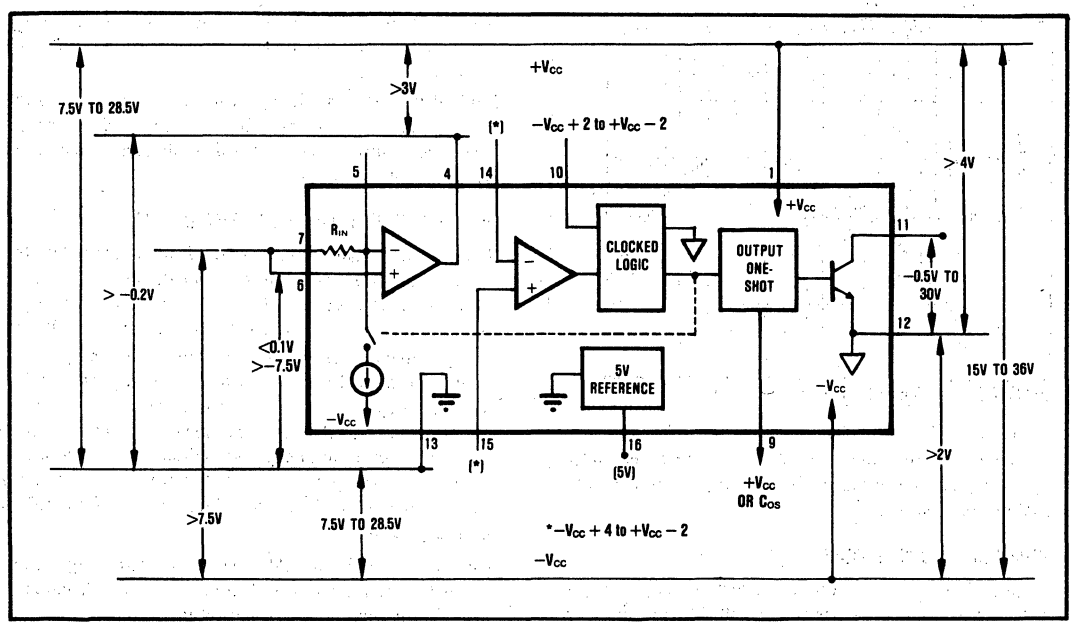


FIGURE 13. Relationships of Allowable Voltages.

cannot be offset by directly connecting to the 5V reference output pin. The comparator input must be connected to a lower voltage point (approximately 2V). This allows the integrator output to operate around a lower voltage point, assuring linear operation. This threshold voltage does not affect the accuracy or drift of the VFC as long as it is not noisy. It should not be made too small, however, or the negative output limitation of the integrator (−0.2V) may cause saturation. Additionally, a large integrator capacitor may be used to limit the required integrator waveform swing to approximately 100mV (see Integrator Capacitor).

Figure 12 shows a circuit for operating from the minimum power supplies, avoiding saturation of the integrator amplifier and loss of accuracy. C_{INT} is chosen for a +100mV to −75mV integrator voltage swing (referred to the noninverting comparator input). The offset voltage applied to the comparator's noninverting input is derived from a resistive voltage divider from V_{REF}.

The relationships of the allowable operating voltage ranges on important pins is shown in Figure 13. Note that the integrator amplifier output cannot swing more than 0.2V below ground. Although this is not "normal" for an operational amplifier, a special internal design of this type optimizes high frequency performance. It is this charactersitic which necessitates the offsetting of the noninverting comparator input in voltage-to-frequency mode to avoid negative output swing.

COUNTING THE OUTPUT

In evaluation and use of the VFC100, you may want to measure the output frequency with a frequency counter. Since synchronization of the VFC100 causes it to await a clock edge for any given output pulse, the output frequency is essentially quantized. The quantized steps are equal to one clock period of the counting gate period. The quantizing error can be made arbitrarily small by counting with long gate times. For instance, a one second counter gate period and a 100kHz full-scale frequency has a one part in 100,000 resolution. Many of the more sophisticated laboratory frequency counters, however, use period measurement schemes to count the input frequency quickly. These instruments work equally well, but the gate period must be set appropriately to achieve the desired count resolution. Short gate periods will produce many digits of "accuracy" in the display, but the results may be very inaccurate.

Figure 14 is a typical system application showing a basic counting technique. A 0 to 10V input is converted to a 0 to 100kHz frequency output. The VFC's clock is divided by M = 4000 to produce a gate period for the counter circuit. The resulting VFC count, N, is insensitive to variations in the actual clock frequency. The input voltage represented by the resulting count is

$$V_{IN} = (N/M)\ 20V$$

Resolution is related to the number of counts at full scale, or one-half the number of clock pulses in the gate period.

The integrating nature of the VFC is important in achieving accurate conversions. The integrating period is equal to the counting period. This can be used to great advantage to reject unwanted signals of a known frequency. Figure 15 shows that response nulls occur at the inverse of the integration period and its multiples. If 60Hz is to be rejected, for instance, the counting period

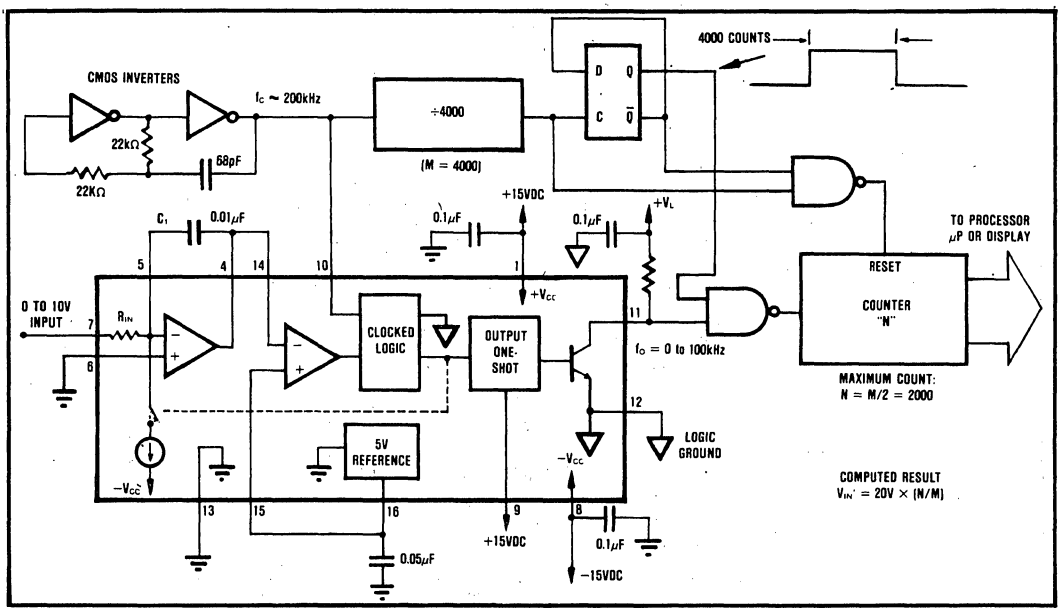


FIGURE 14. Diagram of a Voltage-to-Frequency Converter and Counter System.

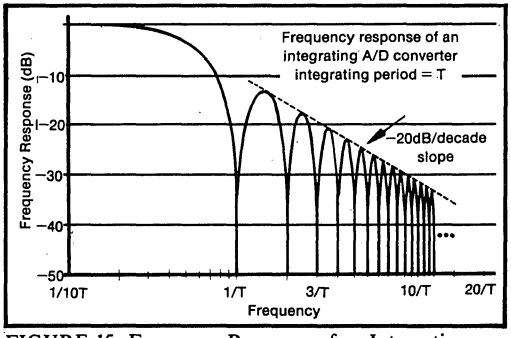


FIGURE 15. Frequency Response of an Integrating Analog-to-Digital Converter.

should be made equal to, or a multiple of 1/60 of a second.

FREQUENCY-TO-VOLTAGE MODE

The VFC100 can also function as a frequency-to-voltage converter by applying an input frequency to the comparator input as shown in Figure 16. The input resistor, R_{IN}, is connected as a feedback resistor. The voltage at the integrator amp output is proportional to the ratio of the input frequency to the clock frequency. The transfer function is

$$V_{OUT} = (f_{IN}/f_{CLOCK})\ 20V$$

This transfer function is complementary to the voltage-to-frequency mode transfer function, making voltage-to-frequency-to-voltage conversions simple and accurate.

Direct coupling of the input frequency to the comparator is easily accomplished by driving both comparators with complementary frequency input signals. Alternatively, one of the comparator inputs can be biased at half the logic voltage (using V_{REF} and a voltage divider) and the other input driven directly.

The proper timing of the input frequency waveform is shown in Figure 16. The input pulse should go low for one clock cycle, centered around a falling edge of the clock. The minimum acceptable input pulse width must fall no later than 200nsec before a negative clock edge and rise no sooner than 200nsec after the falling clock edge. An input pulse which remains low for more than one falling edge of the clock will produce incorrect output voltages. Positive (active high) input pulses can be accepted by reversing the connections to pins 14 and 15. Figure 17 shows a digital conditioning circuit which will accept any input duty cycle and provide the proper pulse width to the comparator. Each rising edge at this circuit's input generates the required negative pulse at the inverting comparator input. The noninverting comparator is driven by a complementary signal.

The integrator amplifier output is designed to drive up to 10,000pF and 5kΩ loads in frequency-to-voltage mode. This allows driving long lines in a large system.

Ripple voltage in the voltage output is unavoidable and is inversely proportional to the value of the integrator capacitor. Figure 18 shows the output ripple and settling time as a function of the C_{INT} value.

The ripple frequency is equal to the input frequency. Its magnitude can be reduced by using a large integrator capacitor value, but at the sacrifice of slow settling time at the voltage output in response to an input frequency change. The settling time constant is equal to $R_{IN} \times C_{INT}$. A better compromise between output ripple and settling time can be achieved by using a moderately low integra-

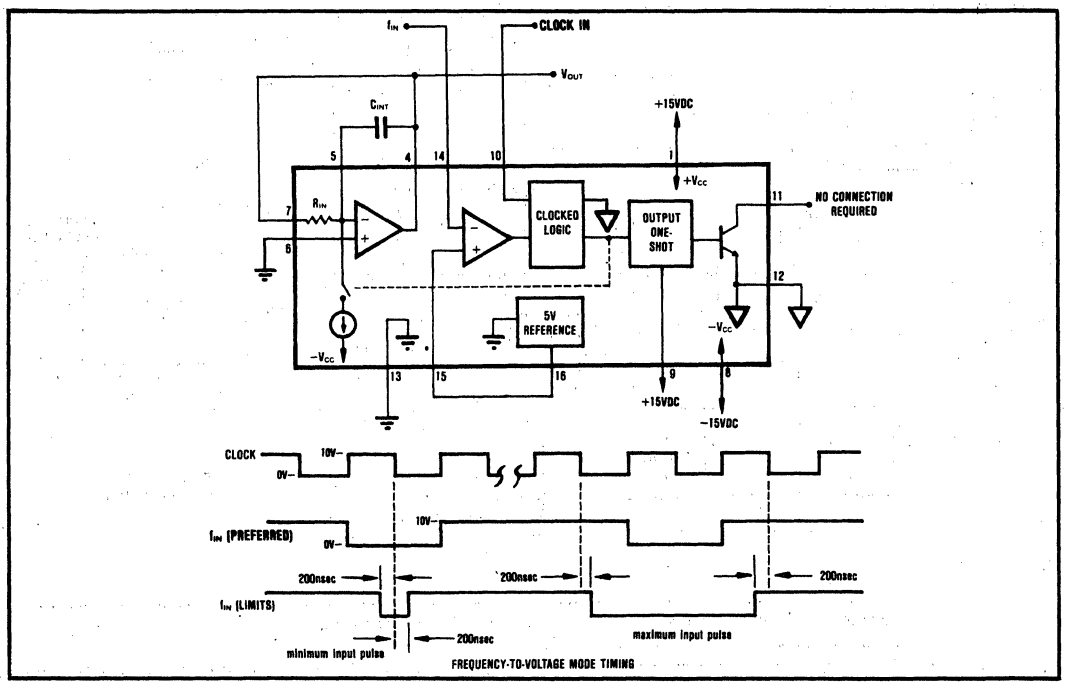


FIGURE 16. Circuit and Timing Diagram of a Frequency-to-Voltage Converter.

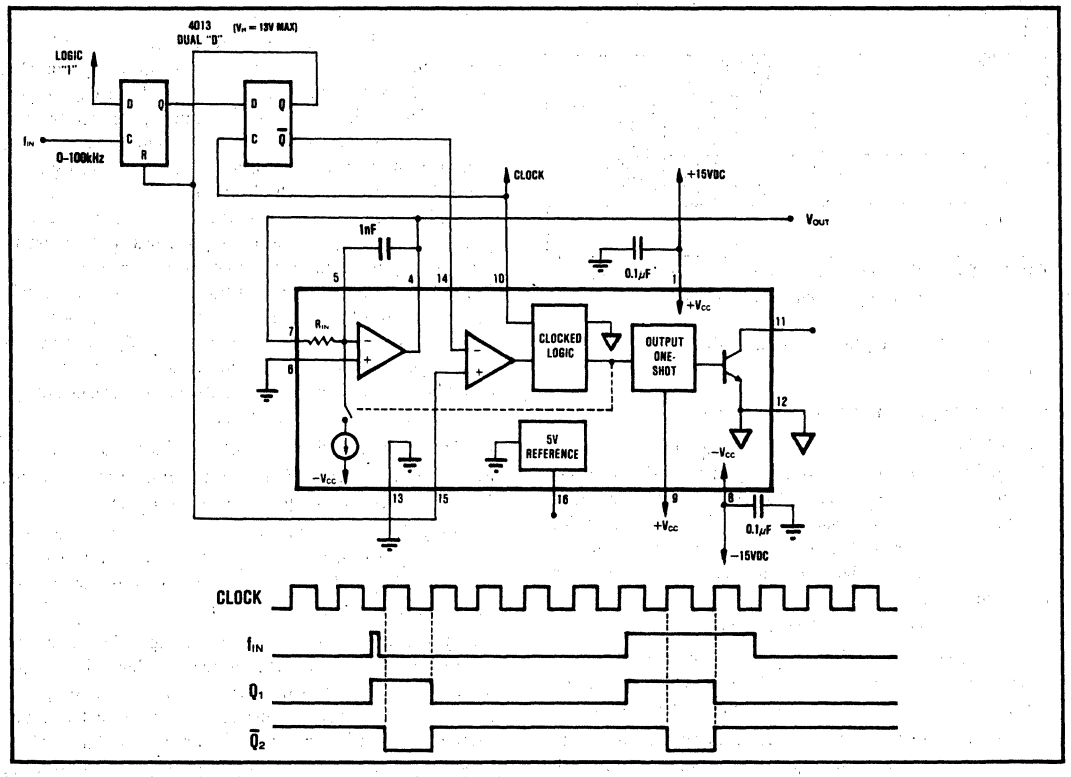


FIGURE 17. Digital Timing Input Conditioning Circuit for Frequency-to-Voltage Operation.

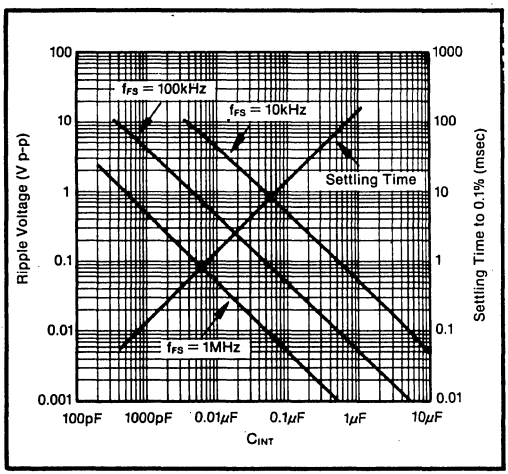


FIGURE 18. Frequency-to-Voltage Mode Output Ripple and Settling Time vs Integrator Capacitance.

tor capacitor value and adding a low-pass filter on the analog output. The cutoff frequency of the filter should be made below the lowest expected input frequency to the frequency-to-voltage converter.

The system in Figure 20 makes use of both voltage-to-frequency and frequency-to-voltage mode to send a signal across an optically-isolated barrier. This technique is useful not only for providing safety in the presence of high voltages, but for creating high noise rejection in electrically noisy environments. The use of a common clock frequency causes the two devices to have complementary transfer functions, which minimizes errors.

Optical coupling is facilitated by use of the output one-shot feature. The output pulse is shortened (see Shortened Output Pulses) to allow for the relatively slow turn-off time of the LED. The timing diagram in Figure 19 shows how the accumulated delay of both optical couplers could produce too long an input pulse for the frequency-to-voltage converter, VFC_2 of Figure 20.

An output filter is used to reduce the ripple in the output of VFC_2. In order to most effectively filter the output, both input and output VFCs are offset. By connecting R_1 to V_{REF}, an accurate offset is created in the voltage-to-frequency function. Zero volts input now creates a 10kHz output. This offset is subtracted in the frequency-to-voltage conversion on the output side, by V_{REF} and R_5.

MORE PULSE POSITION RESOLUTION

Since output pulses must always align with clock edges, the instantaneous output frequency is quantized and

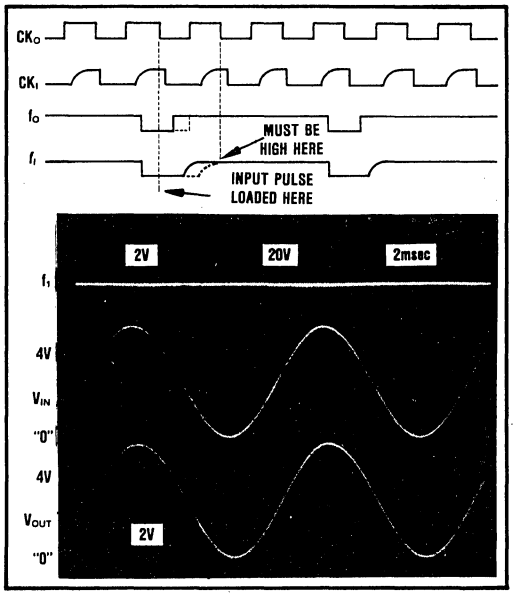


FIGURE 19. Timing Diagram and Oscilloscope Photo of Isolated Voltage-to-Frequency/ Frequency-to-Voltage System.

appears to have phase jitter. This effect can be greatly reduced by using a high speed clock so that available clock edges come more frequently. This would also create a high full-scale frequency, but the technique shown in Figure 21 offers an alternative. A high speed clock is used to produce high resolution of the output pulse position, but a low full-scale frequency can be programmed.

When an output pulse is generated, the next rising edge of the high frequency clock is delayed for a programmable number of clock counts. Since the integrator reset period (which sets the full-scale range) is determined by the time from rising edge to rising edge at the VFC's clock input once the comparator is tripped, the effective clock frequency is $f_{CLOCK}/16$. The circuit shown can be programmed for any N from 2 to 16. Since an output pulse must propagate through the VFC before the next rising edge of the clock arrives, maximum clock frequency is limited by the delay time shown in the timing diagram.

With output pulses now able to align with greater resolution, the output has lower phase jitter. Using this technique, the output is suitable for ratiometric (period measurement) type counting. This counting technique achieves the maximum possible resolution for short gate periods (see Burr-Brown Application Note AN-130).

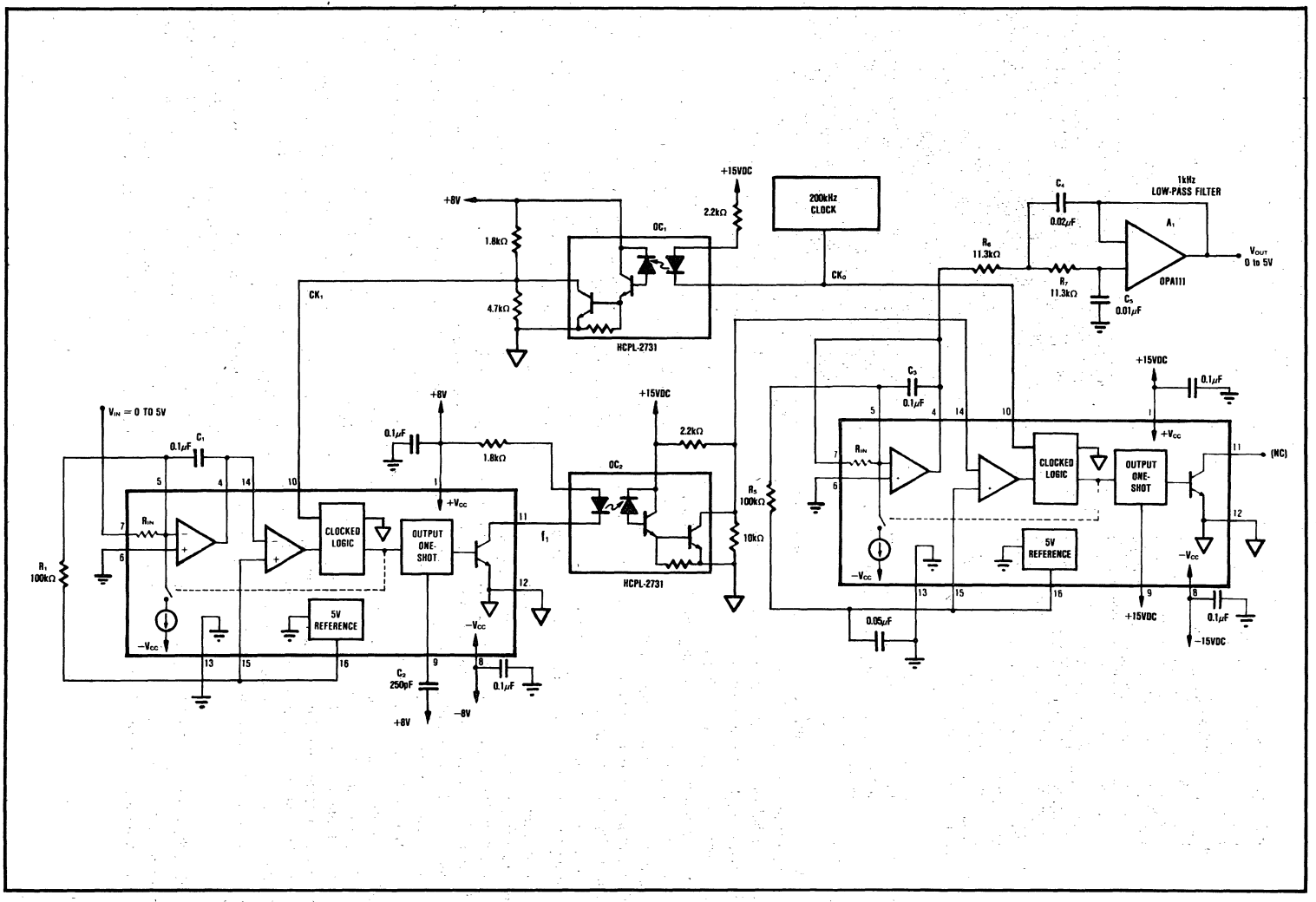


FIGURE 20. Circuit Diagram of Isolated Voltage-to-Frequency/Frequency-to-Voltage System.

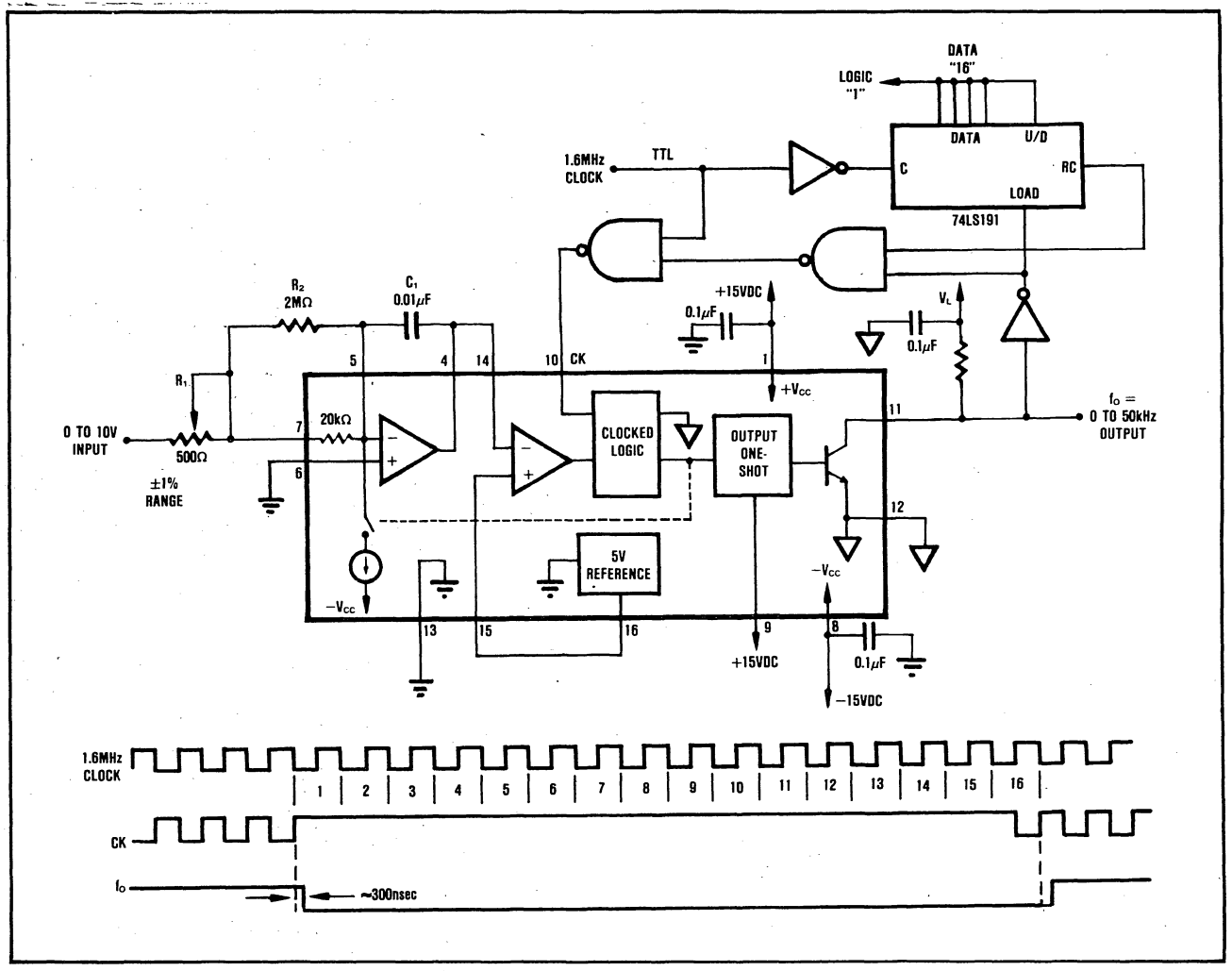


FIGURE 21. Circuit Diagram for Increased Pulse Position Resolution.

BURR-BROWN®

VFC320

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- HIGH LINEARITY, 12 to 14 bits
  - ±0.005% max at 10kHz FS
  - ±0.03% max at 100kHz FS
  - ±0.1% typ at 1MHz FS
- V/F OR F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- 20ppm/°C max GAIN DRIFT
- OUTPUT DTL/TTL/CMOS COMPATIBLE

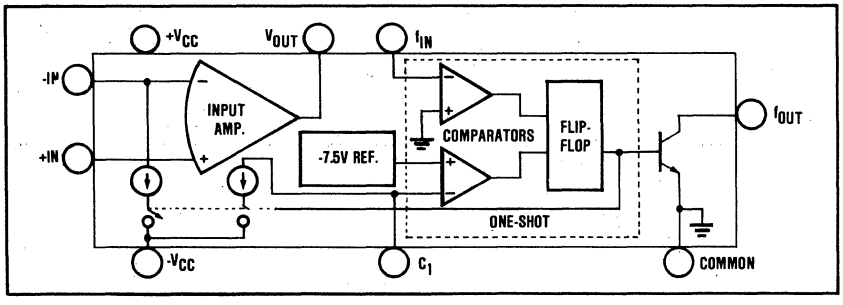
APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC320 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with DTL, TTL, and CMOS logic families.

High linearity (0.005%, max at 10kHz FS) is achieved with relatively few external components. Two external resistors and two external capacitors are required to operate. Full scale frequency and input voltage are determined by a resistor in series with -IN and two capacitors (one-shot timing and input amplifier integration). The other resistor is a non-critical open collector pull-up (f_{OUT} to $+V_{CC}$). The VFC320 is available in three performance/temperature grades and two package configurations. The TO-100 versions are hermetically sealed, and specified for the -25°C to +85°C and -55°C to +125°C ranges, and the dual-in-line units are specified from -25°C to +85°C.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted.

CHARACTERISTICS	CONDITIONS	VFC320BG/BM/SM MIN	VFC320BG/BM/SM TYP	VFC320BG/BM/SM MAX	VFC320CG/CM MIN	VFC320CG/CM TYP	VFC320CG/CM MAX	UNITS
V/F CONVERTER $F_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range(1)	Fig. 4 with $e_2 = 0$	> 0		Note 2				V
	Fig. 4 with $e_1 = 0$	< 0		-10				V
Current Range(1)	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	*		*	µA
Bias Current								
Inverting Input			4	8		*	*	nA
Noninverting Input			10	30		*	*	nA
Offset Voltage(3)				±0.15			*	mV
Offset Voltage Drift			±5			*		µV/°C
Differential Impedance		300 ‖ 5	650 ‖ 5		*	*		kΩ ‖ pF
Common-mode Impedance		300 ‖ 3	500 ‖ 3		*	*		kΩ ‖ pF
ACCURACY								
Linearity Error(1)(4)(5)	Fig. 4 with $e_2 = 0$(6)							
	0.01Hz ≤ f_{OUT} ≤ 10kHz		±0.004	±0.005		±0.0015	±0.002	% of FSR
	0.1Hz ≤ f_{OUT} ≤ 100kHz		±0.008	±0.030		*	*	% of FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0.1			*		% of FSR
Offset Error Input Offset Voltage(3)				±15			*	ppm of FSR
Offset Drift(7)			±0.5			*		ppm of FSR/°C
Gain Error(3)			±5	±10		*	*	% of FSR
Gain Drift(7)	f = 10kHz			50			20	ppm of FSR/°C
Full Scale Drift (offset drift & gain drift)(7)(8)(9)	f = 10kHz			50			20	ppm of FSR/°C
Power Supply Sensitivity	±V_{CC} = 14VDC to 18VDC			±0.015			*	% of FSR/%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			*	MHz
Dynamic Range		6			*			decades
Settling Time	(V/F) to specified linearity for a full scale input step		Note 10			*		
Overload Recovery	< 50% overload		Note 10			*		
OPEN COLLECTOR OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0.4			*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*	µA
Voltage, Logic "1"	External pull-up resistor required (see Figure 4)			V_{PU}			*	V
Duty Cycle at FS	For Best Linearity		25			*		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100			*		ns
F/V CONVERTER $V_{OUT} = 7.5\ R_1C_1\ F_{IN}$, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 ‖ 10	150 ‖ 10		*	*		kΩ ‖ pF
Logic "1"		+1.0		+V_{CC}	*		*	V
Logic "0"		-V_{CC}		-0.05	*		*	V
Pulse-width Range		0.25			*			µs
OUTPUT FROM OP AMP								
Voltage	I_O = 7mA	0 to +10			*			V
Current	V_O = 7VDC	+10			*			mA
Impedance	Closed-loop			0.1			*	Ω
Capacitive Load	Without oscillation			100			*	pF
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range		±13		±20	*		*	V
Quiescent Current			±6.5	±7.5		*	*	mA
TEMPERATURE RANGE								
Specification								
B and C Grades		−25		+85	*		*	°C
S Grade		−55		+125				°C
Operating								
B and C Grades		−25		+85	*		*	°C
S Grade		−55		+125				°C
Storage		−65		+150	*		*	°C

*Specification the same as for VFC320BG/BM/SM.

NOTES:
1. A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity.
2. Determined by R_{IN} and full scale current range constraints.
3. Adjustable to zero. See Offset and Gain Adjustment section.
4. Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section.
5. When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy.
6. For $e_1 = 0$ typical linearity errors are: 0.01% at 10kHz, 0.2% at 100kHz, 0.1% at 1MHz.
7. Exclusive of external components' drift.
8. FSR = Full Scale Range (corresponds to full scale and full scale input voltage.
9. Positive drift is defined to be increasing frequency with increasing temperature.
10. One pulse of new frequency plus 50nsec typical.

ABSOLUTE MAXIMUM RATINGS

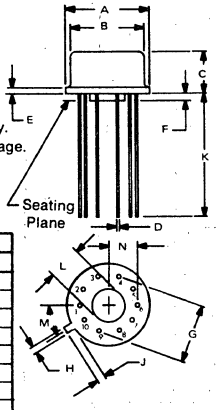
Supply Voltages	±20V
Output Sink Current at f_{OUT}	50mA
Output Current at V_{OUT}	+20mA
Input Voltage, -Input	$\pm V_{CC}$
Input Voltage, +Input	$\pm V_{CC}$
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

MECHANICAL

VFC320BM/CM/SM TO-100 PACKAGE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

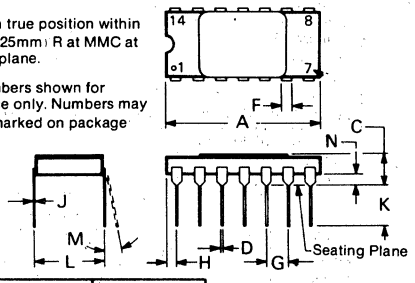


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
	.335	.370	8.51	9.40
	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

VFC320BG/CG CERAMIC DUAL-IN-LINE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

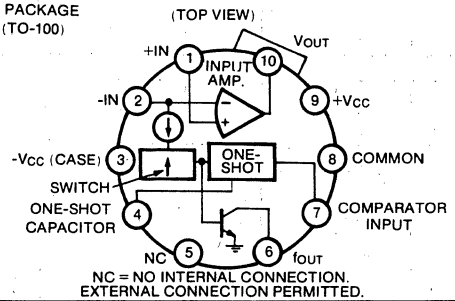
Pin numbers shown for reference only. Numbers may not be marked on package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M		10°		10°
N	.009	.060	0.23	1.52

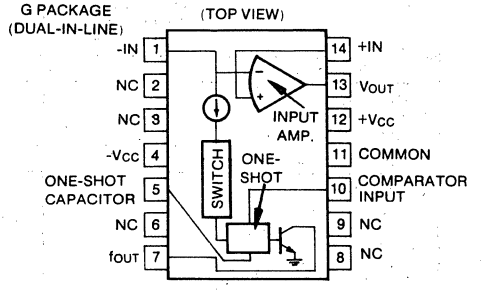
PIN CONFIGURATIONS

M PACKAGE (TO-100) (TOP VIEW)



NC = NO INTERNAL CONNECTION.
EXTERNAL CONNECTION PERMITTED.

G PACKAGE (DUAL-IN-LINE) (TOP VIEW)



DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero). Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ($\Delta f_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC320 makes the device an excellent choice for use as the front end of A/D converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission).

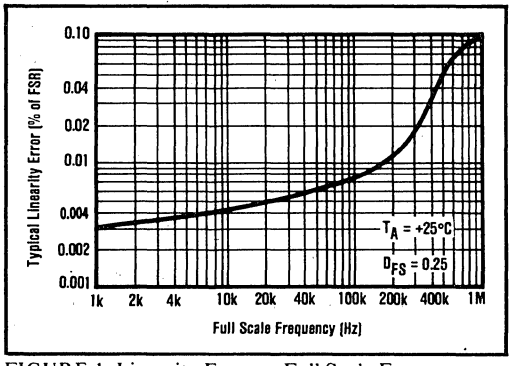


FIGURE 1. Linearity Error vs Full Scale Frequency.

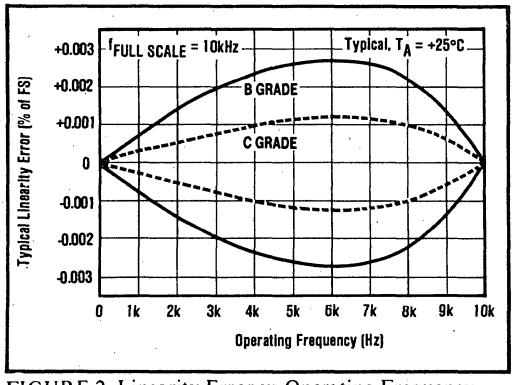


FIGURE 2. Linearity Error vs Operating Frequency.

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC320 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC320.

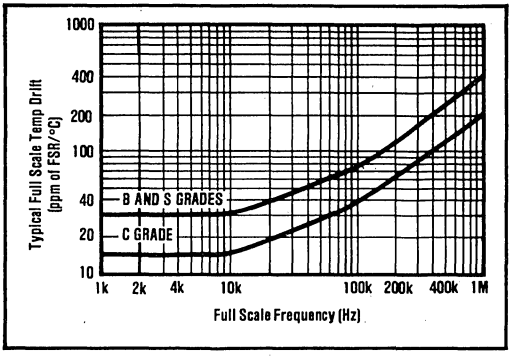


FIGURE 3. Full Scale Drift vs Full Scale Frequency.

RESPONSE

Response of the VFC320 to changes in input signal level is specified for a full scale step, and is 50nsec plus 1 pulse of the new frequency. For a 10V input signal step with the VFC320 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 10μs.

THEORY OF OPERATION

The VFC320 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a one-shot), two switched current sinks, and an open collector output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at V_{IN}, a current will flow through the input resistor, causing the voltage at V_{OUT} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_1 until V_{C1} = -7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this -7.5V threshold point at C_1, comparator B resets the flip-flop, and the ramp voltage begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor, C_1. After the one-shot resets, f_{OUT} changes back to logic 0 and the cycle begins again.

The transfer function for the VFC320 is derived for the

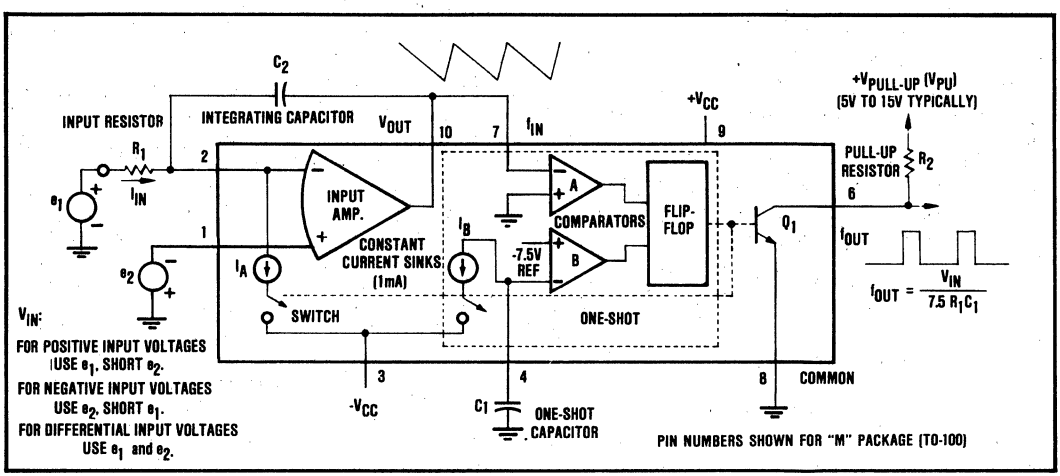


FIGURE 4. Functional Block Diagram of the VFC320.

the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \quad (1)$$

In the time $t_1 + t_2$ the integrator capacitor C_2 charges and discharges but the net voltage change is zero.

$$\text{Thus } \Delta Q = 0 = I_{IN}\, t_1 + (I_{IN} - I_A)\, t_2 \quad (2)$$

$$\text{So that } I_{IN}\,(t_1 + t_2) = I_A\, t_2 \quad (3)$$

$$\text{But since } t_1 + t_2 = \frac{1}{f_{OUT}} \text{ and } I_{IN} = \frac{V_{IN}}{R_1} \quad (4), (5)$$

$$f_{OUT} = \frac{V_{IN}}{I_A R_1 t_2} \quad (6)$$

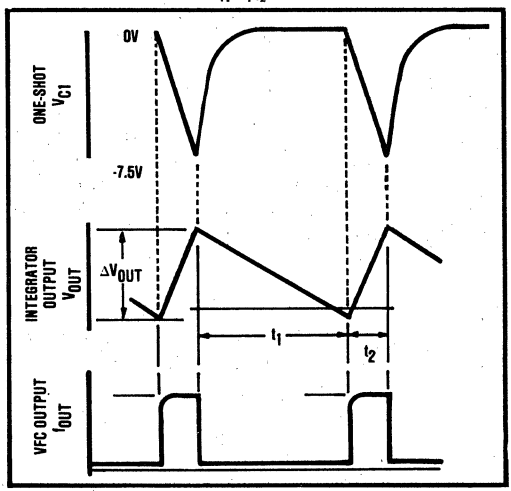


FIGURE 5. Integrator and VFC Output Timing.

In the time t_2, I_B charges the one-shot capacitor C_1 until its voltage reaches -7.5V and trips comparator B.

$$\text{Thus } t_2 = \frac{C_1\, 7.5}{I_B} \quad (7)$$

$$\text{Using (7) in (6) yield } f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \times \frac{I_B}{I_A} \quad (8)$$

Since $I_A = I_B$ the result is

$$f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \quad (9)$$

Since the integrating capacitor, C_2, affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to I_{IN}, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC320 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. e_1 and e_2 are shorted and F_{IN} is disconnected from V_{OUT}. F_{IN} is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by C_1 as before, but the cycle repetition frequency will be dictated by the digital input at F_{IN}.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). For the VFC320, t_2 is fixed and $t_1 + t_2$ varies as the input voltage. Thus the duty cycle, D, is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, D_{FS}, which occurs at full scale input. D_{FS} is a user determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = PW \times f_{FS}$$

Best linearity is achieved when D_{FS} is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN}\ max\ /\ R_1}{1mA} = \frac{I_{IN}\ max}{1mA}$$

Thus $D_{FS} = 0.25$ corresponds to I_{IN} max = 0.25mA.

INSTALLATION AND OPERATING INSTRUCTIONS

VOLTAGE-TO-FREQUENCY CONVERSION

The VFC320 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

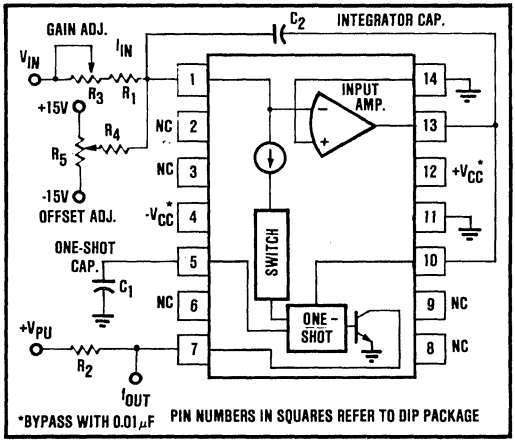


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

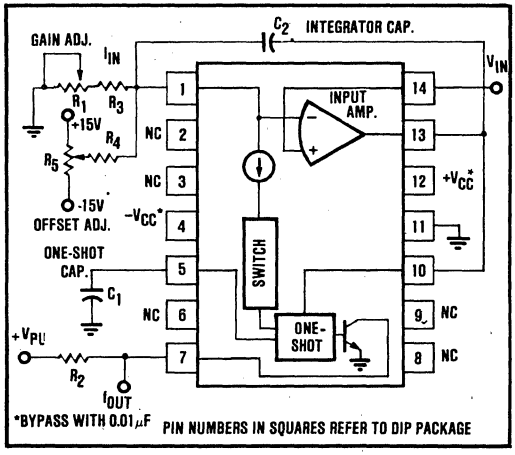


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

EXTERNAL COMPONENT SELECTION

In general the design sequence consists of: (1) choosing f_{MAX}, (2) choosing the duty cycle at full scale ($D_{FS} = 0.25$ typically), (3) determining the input resistor, R_1 (Figure 4), (4) calculating the one-shot capacitor, C_1, (5) selecting the integrator capacitor C_2, and (6) selecting the output pull-up resistor, R_2.

Input Resistors R_1 and R_3

The input resistance (R_1 and R_3 in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than $D_{FS} = 0.25$ may be used but linearity will be affected. The nominal value is R_1 is

$$R_1 = \frac{V_{IN}\ max}{0.25mA} \qquad (10)$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of C_1 and the desired trim range. R_1 should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

One-Shot Capacitor, C_1

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_{1\ nom} = \frac{V_{IN}}{7.5\ R_1\ f_{OUT}} \qquad (11)$$

For the usual 25% duty at $f_{MAX} = V_{IN}/R_1 = 0.25mA$ there is approximately 15pF of residual capacitance so that the design value is

$$C_1(pF) = \frac{33 \times 10^6}{f_{FS}} - 15 \qquad (12)$$

where f_{FS} is the full scale output frequency in Hz. The temperature drift of C_1 is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with C_1. It should be mounted as close to the VFC320 as possible. Figure 8 shows pulse width and full scale frequency for various values of C_1 at $D_{FS} = 25\%$.

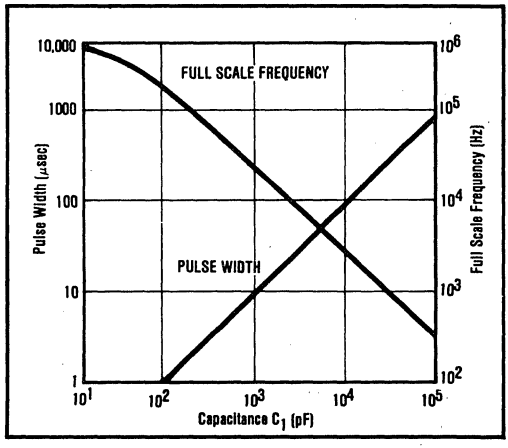


FIGURE 8. Output Pulse Width ($D_{FS} = 0.25$) and Full Scale Frequency vs External One-shot Capacitance.

Integrating Capacitor, C_2

Since C_2 does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in C_2 causes a gain error. A ceramic type is sufficient for most applications. The value of C_2 determines the amplitude of V_{OUT}. Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator

determine a range of acceptable values,

$$C_2\ (\mu F) = \begin{cases} 100/f_{FS};\ \text{if } f_{FS} \leq 100kHz \\ 0.001;\ \text{if } 100kHz < f_{FS} \leq 500kHz \\ 0.0005;\ \text{if } f_{FS} > 500kHz \end{cases} \quad (13)$$

Output Pull Up Resistor R_2.

The open collector output can sink up to 8mA and still be TTL-compatible. Select R_2 according to this equation:

$$R_2\ \text{min}\ (\Omega) = V_{PULLUP}/(8mA - i_{LOAD})$$

A 10% carbon film resistor is suitable for use as R_2.

Trimming Components R_3, R_4, R_5

R_5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R_4 can be a 10% carbon film resistor with a value of 10MΩ.

R_3 nulls the gain errors of the converter and compensates for intitial tolerances of R_1 and C_1. Its total resistance should be at least 20% of R_1, if R_1 is selected 10% low. Its temperature coefficient should be no greater than five times that of R_1, to maintain a low drift of the R_3 - R_1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 x full scale.
2. Adjust R_5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R_3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC320 is 0.015% of FSR/% max. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommeded. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

Internal circuitry causes some current to flow in the common connection (pin 11 on DIP package). Current flowing into the f_{OUT} pin (logic sink current) will also contribute to this current. It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by these currents flowing through any ground return impedance.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1 ($D_{FS} = 0.25$)

$C_1 = [(33 \times 10^6)/f_{MAX}] - 15$ $\quad [(66 \times 10^6)/f_{MAX}] - 15$ if $D_{FS} = 0.5$

$= [(33 \times 10^6)/100kHz] - 15$

$= 315pF$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

Selecting R_1 and R_3 ($D_{FS} = 0.25$)

$R_1 + R_3 = V_{IN}\ \text{max}/0.25mA$ $\quad V_{IN}\ \text{max}/0.5mA$ if $D_{FS} = 0.5$

$= 10V/0.25mA$

$= 40k\Omega$

Choose 32.4kΩ metal film resistor with 1% tolerance and R_3 = 10kΩ cermet potentiometer.

Selecting C_2

$C_2 = 10^2/F_{max}$

$= 10^2/100kHz$

$= 0.001\mu F$

Choose a 0.001μF capacitor with ±5% tolerance.

Selecting R_2

$R_2 = V_{PULLUP}/(8mA - i_{LOAD})$

$= 5V/(8mA - 1.6mA)$, one TTL-load = 1.6mA

$= 781\Omega$

Choose a 750Ω 1/4-watt carbon compensation resistor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC320 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C_3 to make t = 0.1t (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero, to insure that the input signal at pin 10 crosses the zero threshold. Errors are nulled following the procedure given on this page, using 0.001 x full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

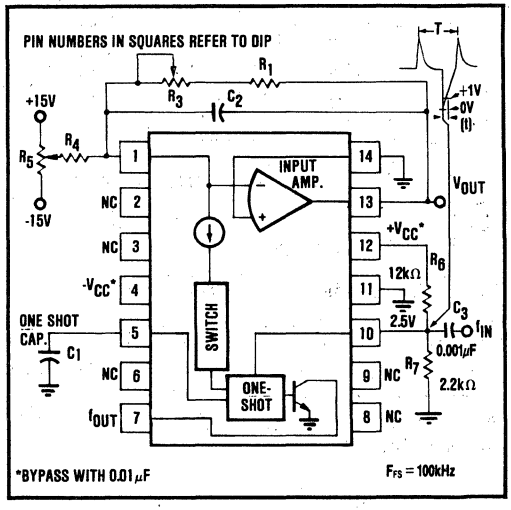


FIGURE 9. Connection Diagram for F/V Conversion.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC320 ideal for a variety of VFC applications. High accuracy allows the VFC320 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits.

Figures 10 - 14 show typical applications of the VFC320.

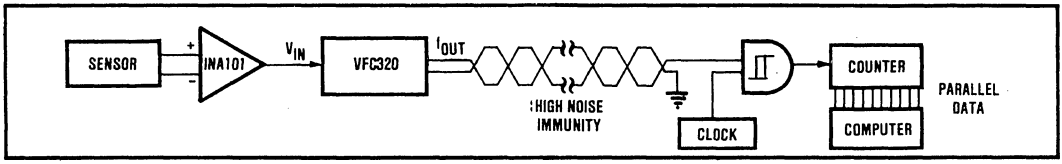


FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.

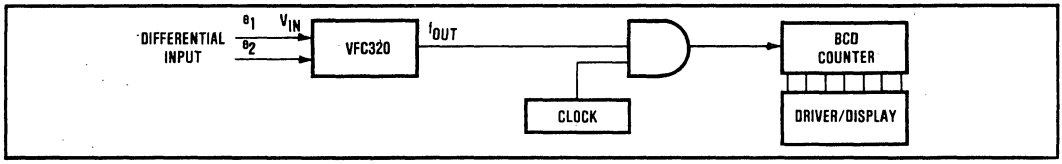


FIGURE 11. Inexpensive Digital Panel Meter.

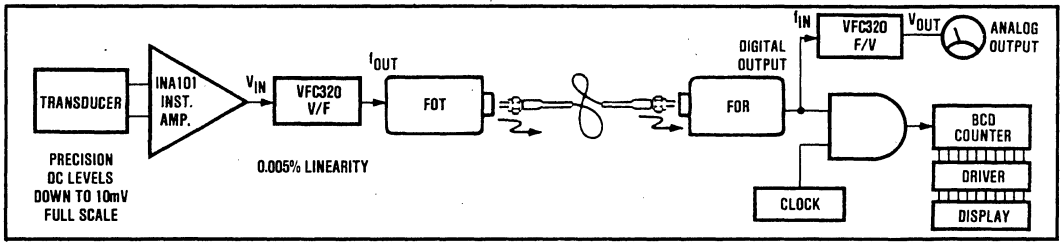


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

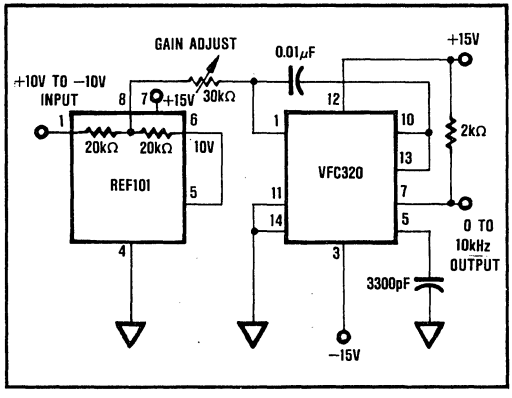


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

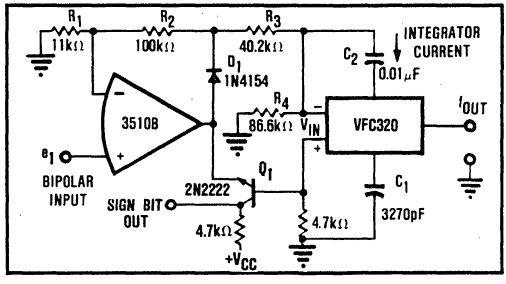


FIGURE 14. Absolute value circuit with the VFC320. Op amp, D_1 and Q_1 (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $|e_1|$. The sign bit output provides indication of the input polarity.

HIGH PERFORMANCE CHIPS

HIGH PERFORMANCE DICE BACKED BY BURR-BROWN'S TRADITION OF QUALITY

Many of Burr-Brown's high-performance monolithic products are available in die form.

All Burr-Brown dice products are the same as those used in our high quality, high performance monolithic and hybrid devices and are proven in demanding applications throughout the world. The dice are manufactured and tested at our Tucson Microtechnology facility using the most advanced equipment and methods available, assuring total control of quality and reliability for every product.

The state-of-the-art performance achieved by these precision monolithic products reflects Burr-Brown's unmatched technical capabilities in:

Low-noise processing / High-stability nichrome thin-film resistors / Active laser trimming / Dielectric isolation / Patented circuit design

At Burr-Brown, concern for quality is a fundamental part of wafer processing. Dice are 100% visually inspected according to MIL-STD-883, Method 2010 Condition B. All wafers are 100% probe tested to specified electrical test limits.

The data sheets and process descriptions provide detailed information on these quality dice.

INTEGRATED CIRCUIT DICE

QUALITY

Visual Inspection: All dice and wafers are 100% visually inspected to MIL-STD-883, Method 2010, Condition B. Dice receive an additional in-process Quality Control inspection to 0.65% AQL.

Probe Tests: All wafers are 100% electrically probe tested to the electrical probe test limits specified in the die data sheet. Due to possible parametric shifts during die separation and assembly, these specifications are not guaranteed after assembly.

Unprobed Parameters: Parameters not specified on the device data sheet are not probed or guaranteed. The dice performance will typically be equivalent to its corresponding part numbered packaged device.

PACKAGING

Package: Dice are packaged face-up in individually compartmented anti-static plastic carriers (waffle packs) and are oriented for automated assembly. Carriers are heat sealed in plastic bags with a dry atmosphere.

Marking: Each die carrier is marked with:

1. Burr-Brown part number
2. Lot number
3. Wafer number
4. QA seal and date
5. Quantity
6. QC identification number

If required, customer part number and order number can be marked on each package.

Storage: High humidity and corrosive atmospheres can cause oxidation or corrosion of the aluminum metalization on wire bond pads. Dice should be stored in a clean dry environment and should be protected from static damage. Storage in a dust-free cabinet with a dry nitrogen atmosphere is recommended.

DIE HANDLING PRECAUTIONS

Static Damage: All integrated circuits can suffer damage from electrostatic discharge. Even precision bipolar devices can suffer subtle parametric damage (increased offset voltage, drift, noise, etc.) if precautions are not adequate. Anti-static work stations are recommended when handling or assembling precision semiconductor devices.

Atmosphere: Die carriers should be opened only in a dust-free environment with a dry non-corrosive atmosphere.

Handling: Although each die is protected by a thick (8000Å minimum) glassivation layer, care should be taken to keep from scratching the surface of the die. Carriers must not be opened for inspection by unqualified personnel. Anti-static protection is recommended when handling or assembling dice.

HYBRID CIRCUIT ASSEMBLY RECOMMENDATIONS

Die Attach: Die attach with silver conductive epoxy or polyimide is recommended to minimize assembly shifts and preserve the accuracy and precision inherent in the die.

Burr-Brown dice are gold-backed and can be eutectically die-attached using a 98/2 gold/silicon preform and a die/substrate temperature of 400°C to 430°C. Exposure time to die attach temperatures should be minimized as permanent parametric shifts can occur.

Assembly in hermetic packages under adequate moisture control is recommended in order to preserve parametric performance and stability.

Wire Bond: Wire bonding may be done with 1.25 mil 99.99% pure gold wire using thermo-sonic techniques or by ultrasonic bonders using 1.25 mil 99/1 aluminum/silicon wire. Wire bond pad size is 4 × 4 mils minimum and aluminum metalization thickness is 8000Å minimum.

ORDERING INFORMATION

Part Number: **OPA27 C D**

Basic device part number — OPA27
Grade/Temperature Range — C
(see data sheet for proper suffix)
Designation: Dice — D

Minimum Order: Dice are subject to minimum order quantities. Consult your local sales office for details on minimum order size and for pricing.

Returns: Returns must be authorized by Burr-Brown. If dice fail visual inspection according to MIL-STD-883, Method 2010, Condition B and 0.65% AQL the entire lot must be returned in their original carriers along with detailed documentation showing reason for rejection.

WAFER PROCESSING

Process Wafer

Gold Back Wafer

100% Wafer Visual Inspection

Sample Parametric Test

100% Probe Test/Laser Trim to
Data Sheet Electrical Limits

Saw Wafer

Deionized Water Rinse

Die Separation

Die Sort

100% Visual Inspection
MIL-STD-883, Method 2010, Condition B

Load In Carrier

In-Process QC Visual Inspection
MIL-STD-883, Method 2010, Condition B
(0.65 AQL)

In-Process QC Documentation Inspection

Seal In Carrier

Ship

BURR-BROWN®

DAC811 DIE

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER DIE

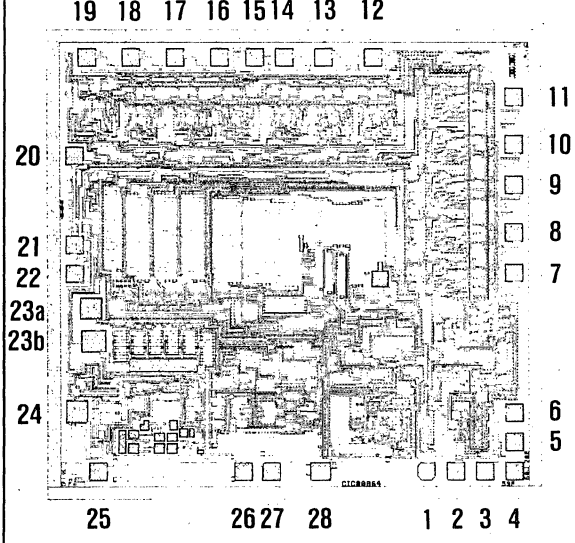
DESCRIPTION

The DAC811 is a complete single-chip integrated circuit microcomputer-compatible 12-bit digital-to-analog converter. The chip includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

Microcomputer interfacing is facilitated by a double-buffered latch. The input latch is divided into three 4-bit nybbles to permit interfacing to 4-, 8-, 12- or 16-bit buses and to handle right- or left-justified data. The 12-bit data in the input latches is transferred to the D/A latch to hold the output value.

Input gating logic is designed so that loading the last nybble or byte of data can be accomplished simultaneously with the transfer of data (previously stored in adjacent latches) from adjacent input latches to the D/A latch. This feature avoids spurious analog output values while using an interface technique that saves computer instructions.

DIE TOPOGRAPHY



Die Size: 134 × 128 mils
Bonding Pad Size: 4 × 4 mils
Backside Contact: Gold (Must be connected to $-V_{CC}$)

Pad	Name	Function
1	V_{DD}	Logic Supply, +5V.
2	$\overline{WR}$	WRITE, command signal to load latches. Logic low loads latches.
3	$\overline{LDAC}$	LOAD D/A CONVERTER, enables $\overline{WR}$ to load the D/A latch. Logic low enables.
4	$\overline{N_A}$	NYBBLE A, enables $\overline{WR}$ to load input latch A (the most significant nybble). Logic low enables.
5	$\overline{N_B}$	NYBBLE B, enables $\overline{WR}$ to load input latch B. Logic low enables.
6	$\overline{N_C}$	NYBBLE C, enables $\overline{WR}$ to load input latch C (the least significant nybble). Logic low enables.
7	D_{11}	DATA, Bit 12, MSB, positive true.
8	D_{10}	DATA, Bit 11.
9	D_9	DATA, Bit 10.
10	D_8	DATA, Bit 9.
11	D_7	DATA, Bit 8.
12	D_6	DATA, Bit 7.
13	D_5	DATA, Bit 6.
14	D_4	DATA, Bit 5.
15	DCOM	DIGITAL COMMON, V_{DD} supply return.
16	D_0	DATA, Bit 1, LSB.
17	D_1	DATA, Bit 2.
18	D_2	DATA, Bit 3.
19	D_3	DATA, Bit 4.
20	$+V_{CC}$	Analog Supply Input, +15V or +12V.
21	$-V_{CC}$	Analog Supply Input, −15V or −12V.
22	GAIN ADJ	To externally adjust gain.
23a, 23b	ACOM	ANALOG COMMON, $\pm V_{CC}$ supply return (connect together).
24	V_{OUT}	D/A converter voltage output.
25	10V RANGE	Connect to pin 24 for 10V Range.
26	SJ	SUMMING JUNCTION of output amplifier.
27	BPO	BIPOLAR OFFSET. Connect to pin 26 for Bipolar Operation.
28	REF OUT	6.3V reference output.

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

T_A = +25°C. $\pm V_{CC}$ = 15V unless otherwise noted.

MODEL	DAC811JD			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
DIGITAL INPUT				
Resolution			12	Bits
Codes[2]		USB, BOB		
V_{IH}	+2.0		+15	VDC
V_{IL}	0.0		+0.8	VDC
I_{IH}, V_I = +2.7V			+10	μA
I_{IL}, V_I = +0.4V			±20	μA
TRANSFER CHARACTERISTICS				
ACCURACY				
Linearity Error		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	±1	LSB
Gain Error[3]		±0.1	±0.2	%
Offset Error[3][4]		±10	±30	mV
OUTPUT				
ANALOG OUTPUT				
Voltage Range ($\pm V_{CC}$ =15V)[6]:				
Unipolar		0 to +10		V
Bipolar		±5, ±10		V
Output Current	±5			mA
Short Circuit to Common Duration		Indefinite		
REFERENCE VOLTAGE				
Voltage	+6.2	+6.3	+6.4	V
Source Current Available for External Loads	+2.0			mA
Short Circuit to Common Duration		Indefinite		
POWER SUPPLY REQUIREMENTS				
Voltage: $+V_{CC}$	+11.4	+15	+16.5	VDC
$-V_{CC}$	−11.4	−15	−16.5	VDC
V_{DD}	+4.5	+5	+5.5	VDC
Current (no load):				
$+V_{CC}$		+16	+25	mA
$-V_{CC}$		−23	−35	mA
V_{DD}		+8	+15	mA
Potential at DCOM with Respect to ACOM[7]			±0.5	V
Power Dissipation		625	800	mW
TEMPERATURE RANGE				
Specification:	0		+70	°C

NOTES: (1) All dice are 100% probe tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (3) Adjustable to zero with external trim potentiometer. (4) Error at input code 000_{16} for both unipolar and bipolar ranges. (5) FSR means Full Scale Range and is 20V for the ±10V range. (6) Minimum supply voltage required for ±10V output swing is ±13.5V. Output swing for ±11.4V supplies is at least −8V to +8V. (7) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$	0 to +18V
$-V_{CC}$ to ACOM	0 to −18V
V_{DD} to DCOM	0 to +7V
V_{DD} to ACOM	±7V
ACOM to DCOM	±7V
Digital Inputs to DCOM	−0.4V to +18V
External Voltage Applied to 10V Range Resistor	±12V
REF OUT	Indefinite short to ACOM
External Voltage Applied to DAC Output	−5V to +5V
Storage Temperature	−65°C to +150°C
Junction Temperature	+175°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGING

DAC811 dice are visually inspected to MIL-STD-883, method 2010, Test Condition B and are shipped in sealed carriers.

ORDERING INFORMATION

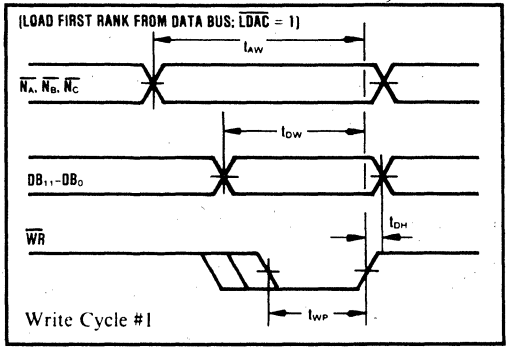
DAC811 J D

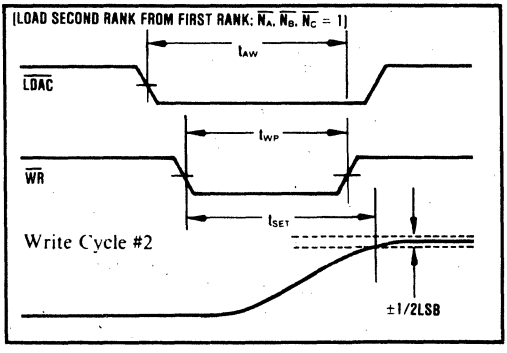
Basic model number

Grade/temperature range
J = 0°C to 70°C

Package code
D = die

TIMING DIAGRAMS





TIMING SPECIFICATIONS

Digital Interface Timing	
T_{WP}, $\overline{WR}$ pulse width (min)	50ns
T_{AW1}, $\overline{N_X}$ and $\overline{LDAC}$ valid to end of $\overline{WR}$ (min)	50ns
T_{DW}, data valid to end of $\overline{WR}$ (min)	80ns
T_{DM}, data valid hold time (min)	0ns

OPERATION

DAC811 is a complete single IC chip12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 1.

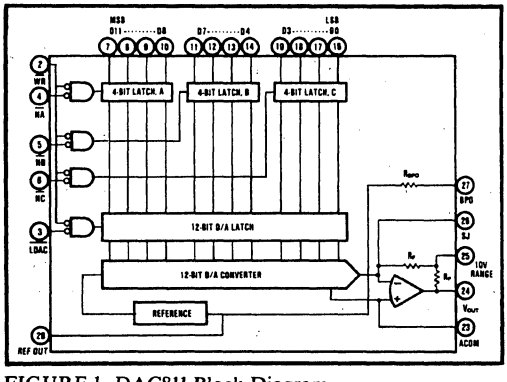


FIGURE 1. DAC811 Block Diagram.

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by N_A, N_B, N_C and WR. N_A, N_B, and N_C are internally NORed with WR so that the input latches transmit data when both N_A (or N_B, N_C) and WR are at logic "0". When either N_A (or N_B, N_C) or WR go to logic "1", the input data is latched into the input registers and held until both N_A (or N_B, N_C) and WR go to logic "0".

The D/A latch is controlled by LDAC and WR. LDAC and WR are internally NORed so that the latches transmit data to the D/A switches when both LDAC and WR are at logic "0". When either LDAC or WR are at logic "1", the data is latched in the D/A latch and held until LDAC and WR go to logic "0".

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for all latches is given in Table I.

GAIN AND OFFSET ADJUSTMENTS

Figures 2 and 3 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

TABLE I. DAC811 Interface Logic Truth Table.

$\overline{WR}$	$\overline{N_A}$	$\overline{N_B}$	$\overline{N_C}$	$\overline{LDAC}$	OPERATION
1	X	X	X	X	No Operation
0	0	1	1	1	Enables Input Latch 4MSB's
0	1	0	1	1	Enables Input Latch 4 Middle Bits
0	1	1	0	1	Enables Input Latch 4 LSB's
0	1	1	1	0	Loads D/A Latch From Input Latches
0	0	0	0	0	All Latches Transparent

"X" = Don't Care.

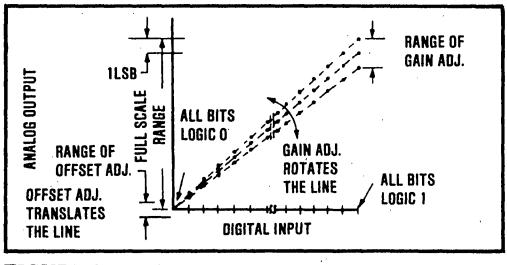


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter

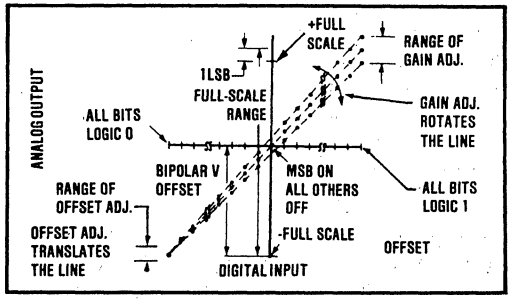


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the Offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table II for corresponding codes.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages.

TABLE II. Digital Input/Analog Output, $\pm V_{CC} = \pm 15V$.

DIGITAL INPUT	ANALOG OUTPUT VOLTAGE		
	0 to +10V	±5V	±10V
12-Bit Resolution MSB LSB ↓ ↓			
111111111111	+9.9976V	+4.9976V	+9.9951V
100000000000	+5.0000V	0.0000V	0.0000V
011111111111	+4.9976V	−0.0024V	−0.0049V
000000000000	0.0000V	−5.0000V	−10.0000V
1LSB	2.44mV	2.44mV	4.88mV

±12V OPERATION

The DAC811 is fully specified for operation on ±12V power supplies. However, in order for the output to swing to ±10V, the power supplies must be ±13.5V or greater. When operating with ±12V supplies, the output swing should be restricted to ±8V in order to meet specifications.

LOGIC INPUT COMPATIBILITY

The DAC811 digital inputs are TTL, LSTTL, and 54/74HC CMOS-compatible over the operating range of V_{DD}. The input switching threshold remains at the TTL threshold over the supply range.

The logic input current over temperature is low enough to permit driving the DAC811 directly from the outputs of 4000B 54/74C CMOS devices.

INSTALLATION

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram, Figure 4. These capacitors (1μF to 10μF tantalum recommended) should be located close to the DAC811.

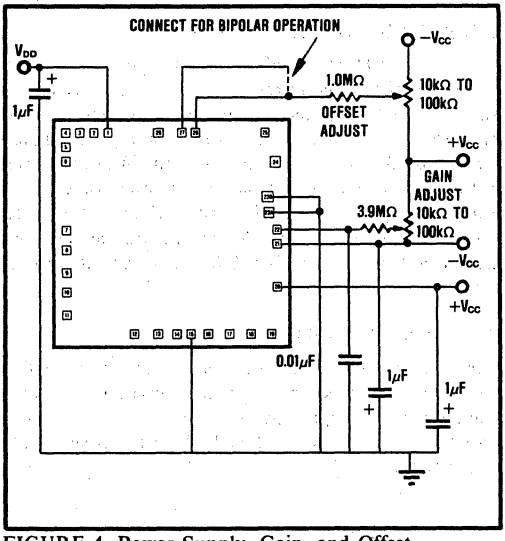


FIGURE 4. Power Supply, Gain, and Offset Potentiometer Connections.

The DAC811 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The Analog Common (pad 23) and Digital Common (pad 15) should be connected together at one point. Separate returns minimize current flow in low level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output, therefore, some caution is required in applying these common connections. The Analog Common is the high quality return for the D/A converter and should be connnected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 4. TCR of the potentiometers should be 100ppm/°C or less. The 1.0MΩ and 3.9MΩ resistors (20% tolerance or better) should be located close to the DAC811 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 5; may be substituted in each case. The Gain Adjust is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Analog Common to reduce noise pickup in all applications, including those not employing external gain adjustment.

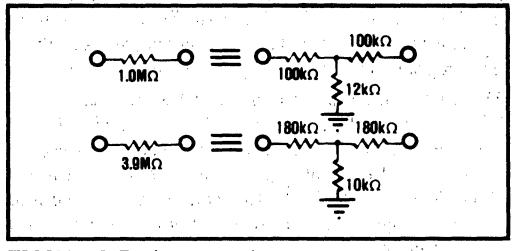


FIGURE 5. Equivalent Resistances.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC811 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 6. Connections for the output ranges are listed in Table III.

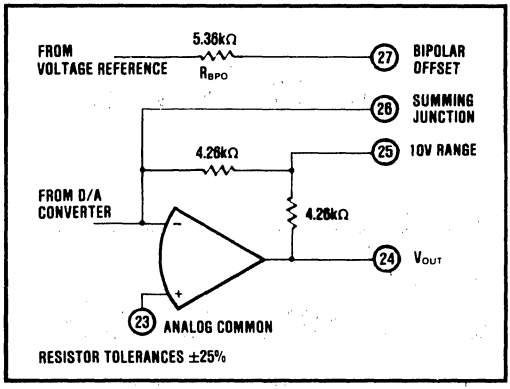


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

TABLE III. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 25 To	Connect Pin 27 To
0 to +10V	USB	24	23
±5V	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

BURR-BROWN®

DAC7700 DIE

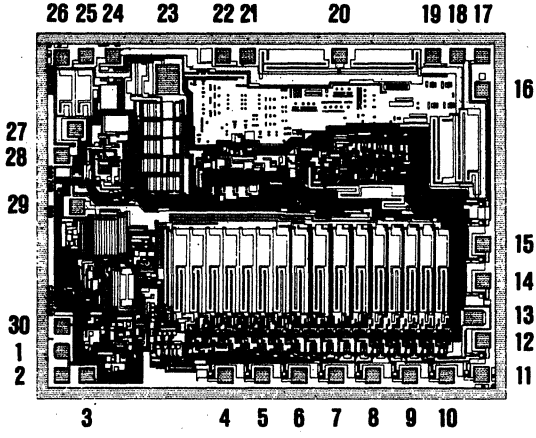
Current Output
16-BIT DIGITAL-TO-ANALOG CONVERTER DIE

DESCRIPTION

The DAC7700KD is complete 16-bit digital-to-analog converter that includes a precision buried-zener voltage reference on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 14-bit monotonicity over the entire specified temperature range but also a maximum end-point linearity error of ±0.003% of full-scale range.

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs of 0 to −2mA and ±1mA are available.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Bit 1 (MSB) Input	16	Bit 15 Input
2	Bit 2 Input	17	Bit 16 Input
3	Bit 3 Input	18	R_{FB} − 10kΩ
4	Bit 4 Input	19	No Connection
5	Bit 5 Input	20	R_{FB} − 10kΩ
6	Bit 6 Input	21	+5V Supply
7	Bit 7 Input	22	Digital Ground
8	Bit 8 Input	23	Analog Ground
9	Bit 9 Input	24	Current Output
10	Bit 10 Input	25	Bipolar Offset
11	Bit 11 Input	26	Gain Adjust
12	Bit 12 Input	27	+15V Supply
13	−15V Supply	28	Reference Output
14	Bit 13 Input	29	−15V Supply
15	Bit 14 Input	30	Zener test point. Do not use.

Die size: 153 × 120 mils

Bonding pad size: 4 × 4 mils

Backside Contact: Gold (Must be connected to $-V_{CC}$)

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS [1]

At T_A = +25°C and $\pm V_{CC}$ = 15V, V_{DD} = +5V unless otherwise noted.

MODEL	DAC7700KD			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
DIGITAL INPUT				
Resolution			16	Bits
Digital Inputs				
V_{IH}	+2.4		$+V_{CC}$	V
V_{IL}	−1.0		+0.8	V
I_{IH}, V_I = +2.7V			+40	µA
I_{IL}, V_I = +0.4V		−0.35	−0.5	mA
TRANSFER CHARACTERISTICS				
ACCURACY[2]				
Linearity Error[3]		±0.0015	±0.003	% of FSR[4]
Differential Linearity Error[3]		±0.003	±0.006	% of FSR
Gain Error[5]		±0.07	±0.15	%
Zero Error[5] [6]		+1	+2	µA
Monotonicity	14	15		Bits
OUTPUT				
Unipolar (CSB Code)[6]		0 to −2		mA
Output Impedance[8]		4		kΩ
Bipolar (COB Code)[8]		±1		mA
Output Impedance[6]		2.45		kΩ
Compliance Voltage		±2.5		V
REFERENCE VOLTAGE				
Voltage	+6.0	+6.3	+6.6	V
Source Current Available for External Loads		+2.5		mA
POWER SUPPLY REQUIREMENTS				
Voltage:				
$+V_{CC}$	11.4	15	16.5	V
$-V_{CC}$	11.4	15	16.5	V
V_{DD}	+4.5	+5	+16.5	V
Current (no load)				
$+V_{CC}$		+10	+25	mA
$-V_{CC}$		−13	−25	mA
V_{DD}			+8	mA
Power Dissipation (V_{DD} = +5.0V)[9]		365	790	mW
TEMPERATURE RANGE				
Specification:	0		70	°C

PERFORMANCE CHARACTERISTICS

Parameters included are for design information and are not guaranteed or subject to test.

PARAMETER	MIN	TYP	MAX	UNITS
DRIFT(over specification temperature range)				
Total Error Over Temperature Range (all models)[10]		±.08	±0.15	% of FSR
Total Full Scale Drift:				
Unipolar models		±10	±30	ppm of FSR/°C
Bipolar models		±10	±25	ppm of FSR/°C
Gain Drift (all models)		±10	±25	ppm/°C
Zero Drift:				
Unipolar models		±2.5	±5	ppm of FSR/°C
Bipolar models		±5	±12	ppm of FSR/°C
Differential Linearity Over Temp.[3]			+0.009, −0.006	% of FSR
Linearity Error Over Temp.[3]			±0.006	% of FSR

PERFORMANCE CHARACTERISTICS (CONT)

PARAMETER	MIN	TYP	MAX	UNITS
Reference Temperature Coefficient			25	ppm/°C
SETTLING TIME (to ±0.003% of FSR)[7]				
Full Scale Step (2mA), 10 to 100Ω load		350	1000	nsec
1kΩ load		1	3	µsec

NOTES: (1) All dice are 100% probe tested and guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) DAC7700KD is specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time. (3) ±0.0015% of full-scale range is equivalent to 1LSB in 16-bit resolution. ±0.003% of full-scale range is equivalent to 1LSB in 15-bit resolution. ±0.006% of full-scale range is equivalent to 1LSB in 14-bit resolution. (4) FSR means full-scale range and is 20V for the ±10V range, 10V for the 0 to +10V range. FSR is 2mA for the ±1mA range and the 0 to +2mA range. (5) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the zero point. (6) Error at input code $FFFF_H$ for CSB operation, $7FFF_H$ for COB operation. (7) Maximum represents the 3σ limit. Not 100% tested for this parameter. (8) Tolerance on output impedance and output current is ±30%. (9) Power dissipation is an additional 40mW when V_{DD} is operated at +15V. (10) With gain and zero errors adjusted to zero at +25°C.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Common	0V, +18V
$-V_{CC}$ to Common	0V, −18V
V_{DD} to Common	0V, +18V
Digital Data Inputs to Common	−1V, +18V
Reference Out to Common	Indefinite Short to Common
External Voltage Applied to R_F	±18V
Power Dissipation	1000mW
Storage Temperature	−60°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGING

DAC7700 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B, and are shipped in sealed carriers.

ORDERING INFORMATION

DAC7700 K D

Basic Model Number

Grade/Temperature Range
K = 0°C to +70°C

Package Code
D = Die

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1µF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 1, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor may be needed from Gain Adjust to Common to reduce noise pickup. Refer to Figures 2 and 3 for the relationship of zero and gain adjustments to unipolar and bipolar D/A converters.

Zero Adjustment

For unipolar (CSB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that produces zero output voltage or current. See Table I for corresponding codes and the Connection Diagram, Figure 4, for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

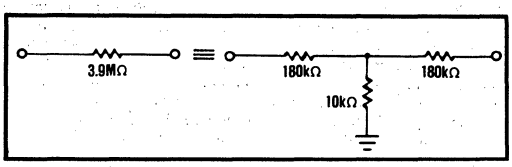


FIGURE 1. Equivalent Resistances.

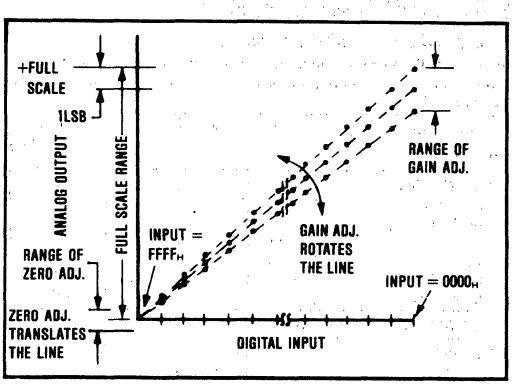


FIGURE 2. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters.

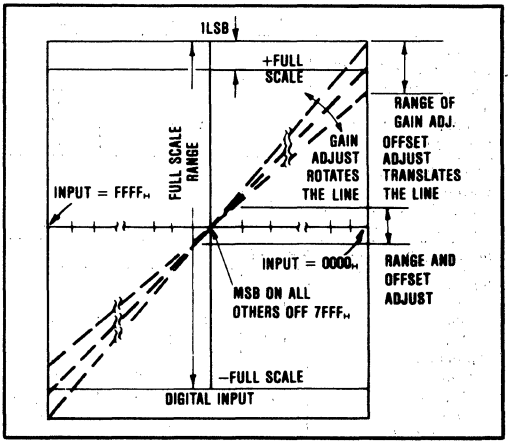


FIGURE 3. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters.

TABLE I. Digital Input and Analog Output Relationships.

CURRENT OUTPUT MODES							
	Analog Output						
	Unipolar, 0 to −2mA			Bipolar, ±1mA			
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	Units
One LSB	0.031	0.061	0.122	0.031	0.061	0.122	μA
0000$_H$	−1.99997	−1.99994	−1.99988	−0.99997	−0.99994	−0.99988	mA
FFFF$_H$	0	0	0	+1.00000	+1.00000	+1.00000	mA
7FFF$_H$	−1.00000	−1.00000	−1.00000	0	0	0	mA

VOLTAGE OUTPUT MODES (WITH EXTERNAL OP-AMP)										
	Analog Output									
	Unipolar, 0 to +10V			Bipolar, ±10V			Bipolar, ±5V			
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	Units
One LSB	153	305	610	305	610	1224	153	305	610	μV
0000$_H$	+9.99985	+9.99969	+9.99939	+9.99969	+9.99939	+9.99878	+4.99985	+4.99969	+4.99939	V
FFFF$_H$	0	0	0	−10.0000	−10.0000	−10.0000	−5.0000	−5.0000	−5.0000	V
7FFF$_H$	+5.00000	+5.00000	+5.00000	0	0	0	0	0	0	V

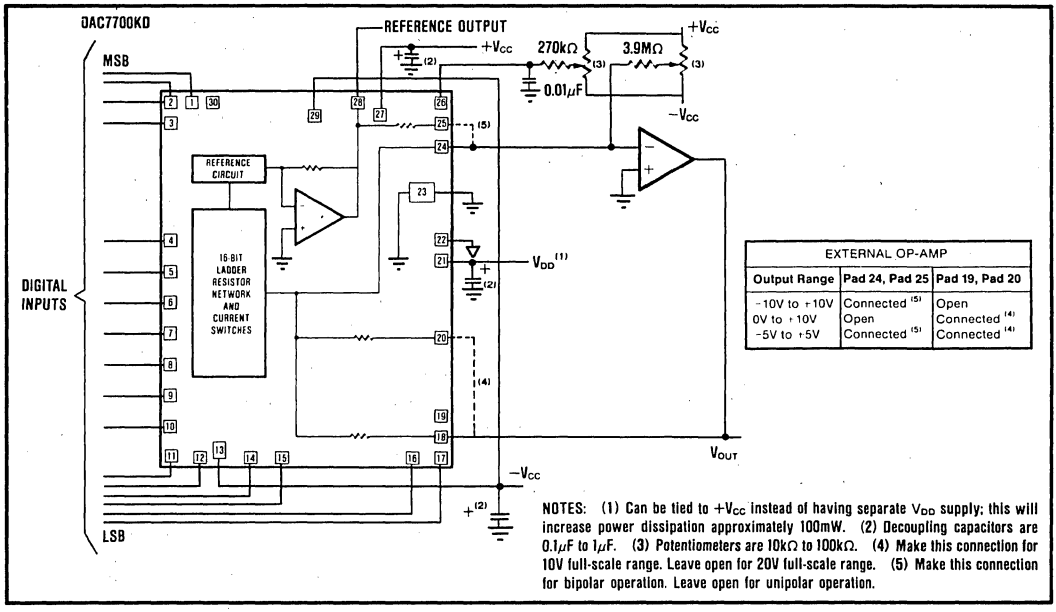


FIGURE 4. Connection Diagram.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table I for positive full scale voltages and Figure 4 for gain adjustment circuit connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter connected for a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 5 and 6, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located

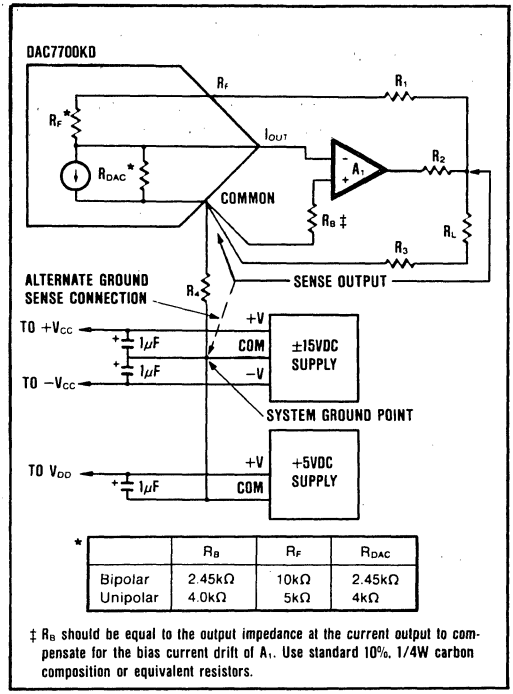


FIGURE 5. Preferred External Op Amp Configuration.

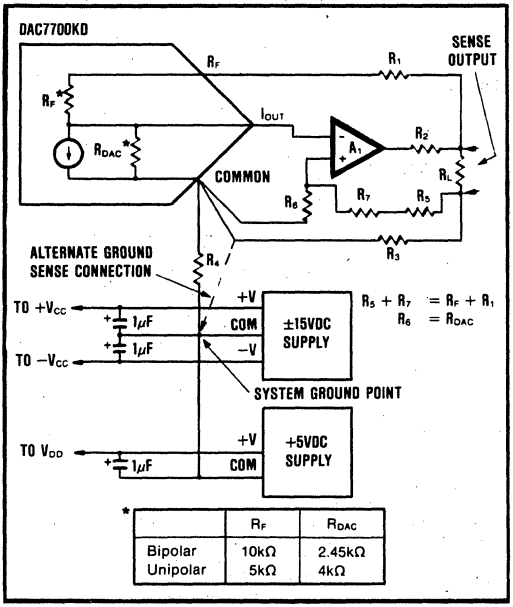


FIGURE 6. Differential Sensing Output Op Amp Configuration.

as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the common pad. Sensing the output voltage at the system ground point is permissible with the DAC7700 because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times$ 2mA) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 5 and 6.

Figures 5 and 6 show two methods of connecting the current output model DAC7700 with external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

If the output cannot be sensed at Common or the system ground point as mentioned above, the differential output circuit shown in Figure 6 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 6 can be reduced to the one shown in Figure 5. Again the effect of R_4 is negligible.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

BURR-BROWN®

DAC7701 DIE

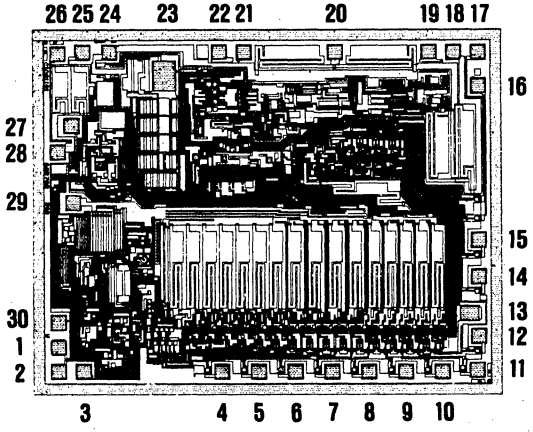
Voltage Output
16-BIT DIGITAL-TO-ANALOG CONVERTER DIE

DESCRIPTION

The DAC7701KD is a complete 16-bit digital-to-analog converter that includes a precision buried-zener voltage reference and a low-noise, fast-settling output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 14-bit monotonicity over the entire specified temperature range but also a maximum end-point linearity error of ±0.003% of full-scale range.

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V and ±10V are available.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Bit 1 (MSB) Input	16	Bit 15 Input
2	Bit 2 Input	17	Bit 16 Input
3	Bit 3 Input	18	R_{FB} – 10kΩ
4	Bit 4 Input	19	Voltage Output
5	Bit 5 Input	20	R_{FB} – 10kΩ
6	Bit 6 Input	21	+5V Supply
7	Bit 7 Input	22	Digital Ground
8	Bit 8 Input	23	Analog Ground
9	Bit 9 Input	24	Current Output
10	Bit 10 Input	25	Bipolar Offset
11	Bit 11 Input	26	Gain Adjust
12	Bit 12 Input	27	+15V Supply
13	–15V Supply	28	Reference Output
14	Bit 13 Input	29	–15V Supply
15	Bit 14 Input	30	Zener test point. Do not use.

Die size: 153 × 120 mils

Bonding pad size: 4 × 4 mils

Backside Contact: Gold (Must be connected to $-V_{CC}$)

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS

At T_A = +25°C and $\pm V_{CC}$ = 15V, V_{DD} = +5V unless otherwise noted.

MODEL	DAC7701KD			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
DIGITAL INPUT				
Resolution			16	Bits
Digital Inputs				
V_{IH}	+2.4		+V_{CC}	V
V_{IL}	−1.0		+0.8	V
I_{IH}, V_I = +2.7V			+40	μA
I_{IL}, V_I = +0.4V		−0.35	−0.5	mA
TRANSFER CHARACTERISTICS				
ACCURACY				
Linearity Error[2]		±0.0015	±0.003	% of FSR[3]
Differential Linearity Error[2]		±0.003	±0.006	% of FSR
Gain Error[4]		±0.07	±0.15	%
Zero Error[3] [5]		±10	±20	mV
Monotonicity	14	15		Bits
OUTPUT				
Unipolar (CSB Code)		0 to +10		V
Bipolar (COB Code)		±10		V
Output Current		±5		mA
Output Impedance		0.15		Ω
Short Circuit to Common Duration		Indefinite		
REFERENCE VOLTAGE				
Voltage	+6.0	+6.3	+6.6	V
Source Current Available for External Loads		+2.5		mA
POWER SUPPLY REQUIREMENTS				
Voltage				
+V_{CC}	11.4	15	16.5	V
−V_{CC}	11.4	15	16.5	V
V_{DD}	+4.5	+5	+16.5	V
Current (no load)				
+V_{CC}		+16	+30	mA
−V_{CC}		−18	−30	mA
V_{DD}		+4	+8	mA
Power Dissipation (V_{DD} = +5.0V)[8]		530	940	mW
TEMPERATURE RANGE				
Specification	0		70	°C

PERFORMANCE CHARACTERISTICS

Parameters included are for design information and are not guaranteed or subject to test.

PARAMETER	MIN	TYP	MAX	UNITS
DRIFT(over specification temperature range)				
Total Error Over Temperature Range (all models)[9]		±.08	±0.15	% of FSR
Total Full Scale Drift:				
Unipolar models		±10	±30	ppm of FSR/°C
Bipolar models		±10	±25	ppm of FSR/°C
Gain Drift (all models)		±10	±25	ppm/°C
Zero Drift:				
Unipolar models		±2.5	±5	ppm of FSR/°C
Bipolar models		±5	±12	ppm of FSR/°C
Differential Linearity Over Temp.[6]			+0.009, −0.006	% of FSR

PERFORMANCE CHARACTERISTICS (CONT)

PARAMETER	MIN	TYP	MAX	UNITS
Linearity Error Over Temp.[2]			±0.006	% of FSR
Reference Temperature Coefficient			25	ppm/°C
SETTLING TIME (to ±0.003% of FSR)[6]				
Full Scale Step 2kΩ load		4	8	μsec
1LSB Step at Worst-Case Code[7]		2.5		μsec
Slew Rate		10		V/μsec

NOTES: (1) All dice are 100% probe tested and guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) ±0.0015% of full-scale range is equivalent to 1LSB in 16-bit resolution. ±0.003% of full-scale range is equivalent to 1LSB in 15-bit resolution. ±0.006% of full-scale range is equivalent to 1LSB in 14-bit resolution. (3) FSR means full-scale range and is 20V for the ±10V range, 10V for the 0 to +10V range. FSR is 2mA for the ±1mA range and the 0 to +2mA range. (4) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the zero point. (5) Error at input code $FFFF_H$ for CSB operation, $7FFF_H$ for COB operation. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$. (8) Power dissipation is an additional 40mW when V_{DD} is operated at +15V. (9) With gain and zero errors adjusted to zero at +25°C.

ABSOLUTE MAXIMUM RATINGS

+V_{CC} to Common	0V, +18V
−V_{CC} to Common	0V, −18V
V_{DD} to Common	0V, +18V
Digital Data Inputs to Common	−1V, +18V
Reference Out to Common	Indefinite Short to Common
External Voltage Applied to R_F	±18V
External Voltage Applied to D/A Output	−5V to +5V
V_{OUT}	Indefinite Short to Common
Power Dissipation	1000mW
Storage Temperature	−60°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGING

DAC7701KD dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B, and are shipped in sealed carriers.

ORDERING INFORMATION

DAC7701 K D

Basic Model Number

Grade/Temperature Range
K = 0°C to +70°C

Package Code
D = Die

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 1, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor may be needed from Gain Adjust to Common to reduce noise pickup. Refer to Figures 2 and 3 for the relationship of zero and gain adjustments to unipolar and bipolar D/A converters.

Zero Adjustment

For unipolar (CSB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that produces zero output voltage or current. See Table I for corresponding codes and the Connection Diagram, Figure 4, for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

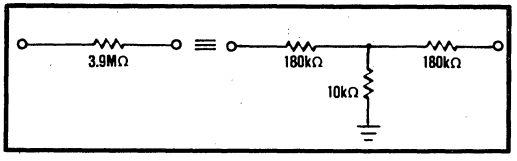


FIGURE 1. Equivalent Resistances.

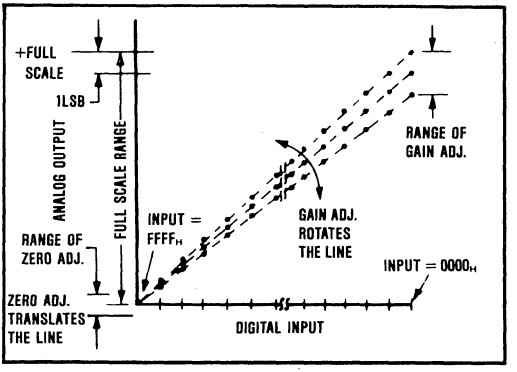


FIGURE 2. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters.

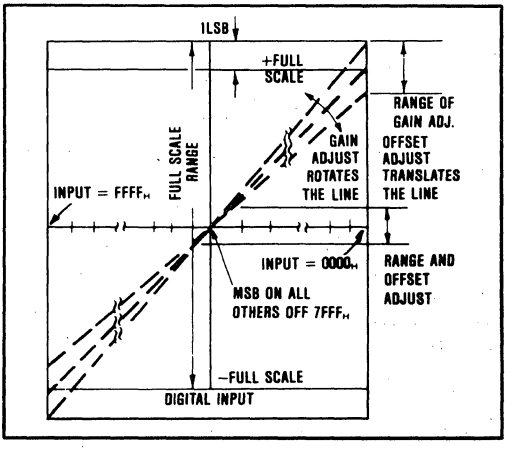


FIGURE 3. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters.

TABLE I. Digital Input and Analog Output Relationships.

VOLTAGE OUTPUT MODES										
Digital Input Code	Analog Output									Units
	Unipolar, 0 to +10V			Bipolar, ±10V			Bipolar, ±5V			
	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	
One LSB	153	305	610	305	610	1224	153	305	610	μV
0000$_H$	+9.99985	+9.99969	+9.99939	+9.99969	+9.99939	+9.99878	+4.99985	+4.99969	+4.99939	V
FFFF$_H$	0	0	0	−10.0000	−10.0000	−10.0000	−5.0000	−5.0000	−5.0000	V.
7FFF$_H$	+5.00000	+5.00000	+5.00000	0	0	0	0	0	0	V

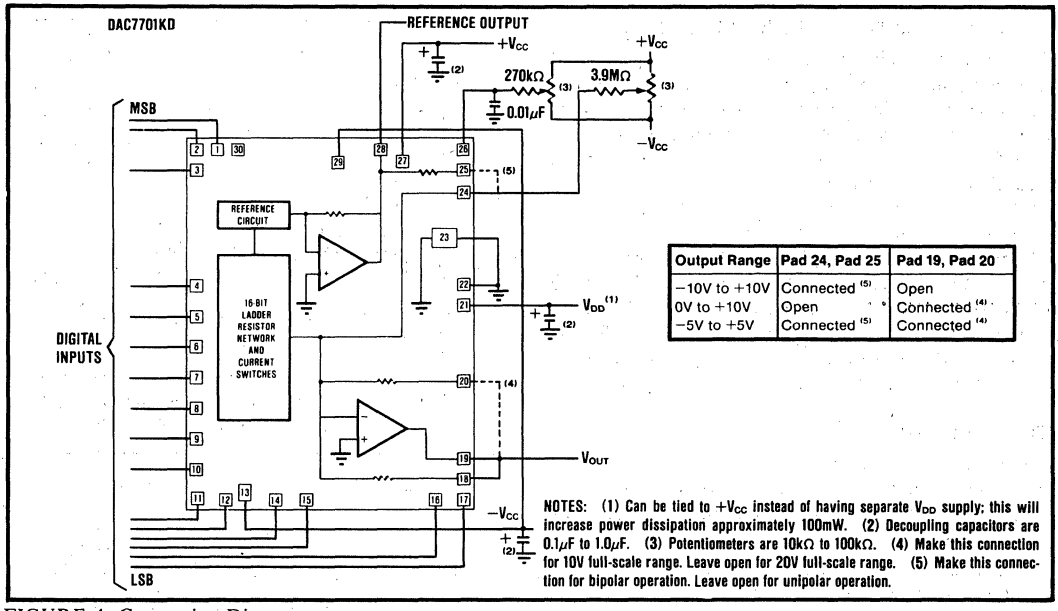


FIGURE 4. Connection Diagram.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table I for positive full scale voltages and Figure 4 for gain adjustment circuit connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter connected for a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figure 5, lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed during initial calibration. R_2 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_1 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_1 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_3 is negligible.

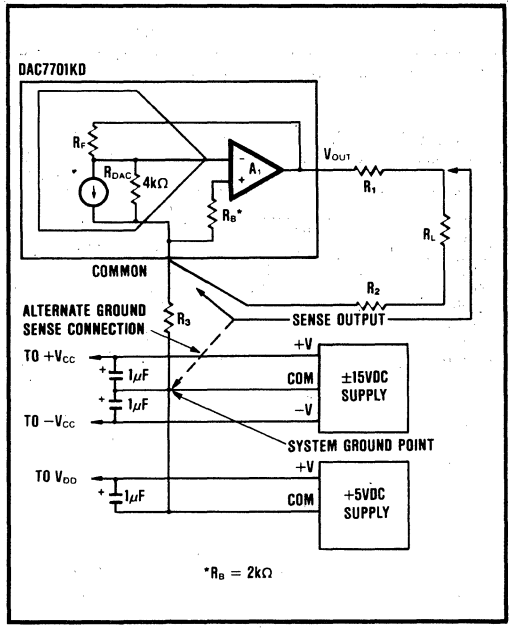


FIGURE 5. Output Circuit for Voltage Models.

In many applications it is impractical to sense the output voltage at the common pad. Sensing the output voltage at the system ground point is permissible with the DAC7701 because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_3 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_3 ($R_3 \times$ 2mA) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figure 5.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

BURR-BROWN®

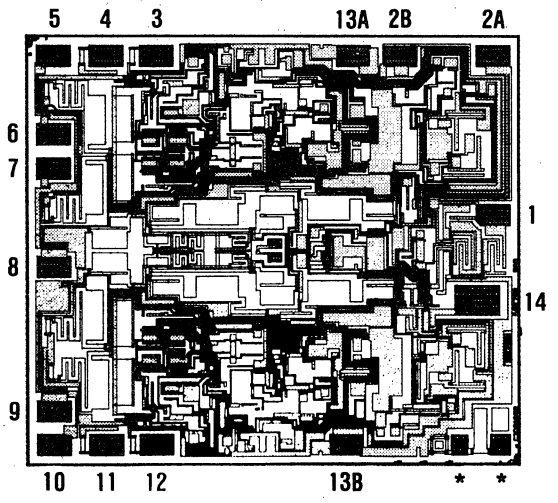
INA101 DIE

Very-High Accuracy INSTRUMENTATION AMPLIFIER DIE

DESCRIPTION

The INA101 is a high accuracy, monolithic instrumentation amplifier. It consists of three precision operational amplifiers featuring a laser-trimmed thin-film resistor network. High input impedance, low noise, very-low drift, and high accuracy give outstanding performance in demanding instrumentation applications.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Output	8	A_1 Output
2A	$+V_{CC}$	9	A_2 Output
2B	$+V_{CC}$	10	Gain Set A_2
3	−Input	11	Gain Sense A_2
4	Gain Sense A_1	12	+Input
5	Gain Set A_1	13A	$-V_{CC}$
6	V_{OS} Trim A_1	13B	$-V_{CC}$
7	V_{OS} Trim A_1	14	Common

Die Size: 120 × 106 mils
Bonding Pad Size: 5 × 5 mils
Backside Contact: Gold

*Do Not Connect

NOTES: (1) The back of the die should not be used for the $-V_{CC}$ connection. (2) Bond from either pad 13A or pad 13B to $-V_{CC}$. (3) Bond from pad 2A and pad 2B separately to $+V_{CC}$.

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_{DIE} = +45°C and $\pm V_{CC}$ = 15V unless otherwise specified.[2]

PARAMETER	CONDITIONS	INA101AD MIN	INA101AD TYP	INA101AD MAX	UNITS
GAIN EQUATION	Gain = 1 + (40k/R_G)				
GAIN ERROR	Gain = 1			±0.1	% of FS
	Gain = 10			±0.2	% of FS
	Gain = 100			±0.25	% of FS
	Gain = 1000			±0.5	% of FS
RATED OUTPUT					
Voltage		±10			V
Current	V_O = ± 10V	±5			mA
OFFSET					
Input Stage	G = 1000			±100	µV
vs Temperature	G = 1000			±4	µV/°C
vs Supply (PSR)	G = 1	90			dB
Output Stage				±600	µV
vs Temperature				±30	µV/°C
INPUT BIAS CURRENT				±30	nA
COMMON-MODE REJECTION	V_{IN} = ±10VDC				
	G = 1 DC	76			dB
	G = 1000	100			dB
POWER SUPPLY					
Voltage	Derated	±5		±18	V
Current	I_O = 0mADC			±8.5	mA

NOTES: (1) All dice are 100% probe tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) +45°C is used to simulate die temperature of an assembled part at ambient temperature of +25°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±V_{CC}
Differential Input Voltage	±V_{CC}
Storage Temperature Range	−65°C to +150°C
Output Short-Circuit Duration	Continuous
Junction Temperature	+150°C

ORDERING INFORMATION

INA101 A D

Basic model number

Grade/temperature range
A = −25°C to +85°C

Package code
D = Die

PACKAGING

INA101 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

BURR-BROWN®

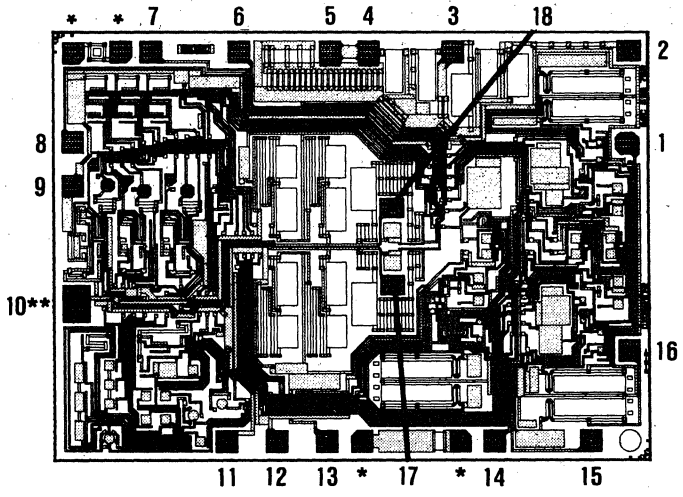
INA102 DIE

Low Power High Accuracy INSTRUMENTATION AMPLIFIER DIE

DESCRIPTION

The INA102 is a high accuracy, monolithic instrumentation amplifier designed for signal conditioning applications where low quiescent power is desired. On-chip laser-trimmed thin-film resistors provide excellent gain/temperature stability and excellent CMRR. Gains of 1, 10, 100, or 1000 may be conveniently selected by strapping appropriate pads together.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Offset Adjust	10	Common
2	× 10	11	Output
3	× 100	12	$+V_{CC}$
4	× 1000	13	Filter
5	× 1000 Gain Sense	14	−In
6	Gain Sense	15	+In
7	Gain Set	16	Offset Adjust
8	CMR Trim	17	A_1 Output
9	$-V_{CC}$	18	A_2 Output

Die Size: 142 × 104 mils

Bonding Pad Size: 5 × 5 mils

Backside Contact: Gold

*Do Not Connect

**Glass covers the lower 1/3 of this pad.

NOTE: The back of the die should not be used for the $-V_{CC}$ connection.

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_{DIE} = +25°C $\pm V_{CC}$ = 15V unless otherwise specified.

PARAMETER	CONDITIONS	INA102AD MIN	INA102AD TYP	INA102AD MAX	UNITS
GAIN EQUATION[2]	Externally Set		1 + (40k/R_G)		V/V
PAD-STRAPPABLE GAINS			× 1, 10, 100, 1000		V/V
GAIN ERROR[2]	Gain = 1 = 10 = 100 = 1000			±0.1 ±0.1 ±0.25 ±0.75	% of FS % of FS % of FS % of FS
RATED OUTPUT Voltage Current	 V_O = 10V	 ±10 ±1			 V mA
OFFSET Input Stage Output Stage	G = 1000			 ±300 ±400	 μV μV
INPUT BIAS CURRENT				50	nA
COMMON MODE REJECTION	V_{IN} = ±10VDC G = 1 G = 1000	 74 80			 dB dB
POWER SUPPLY Voltage Current	 Derated I_O = 0mADC	 ±3.5		 ±18 ±750	 V μA

NOTES: (1) All dice are 100% probe-tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) If an external gain set resistor (R_G) is used for intermediate gains, it can be a major source of gain error. Gain error specifications are for pin-strapped gains only.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range, Differential & Common-mode	±V_{CC}
Storage Temperature Range	−65°C to +150°C
Output Short-Circuit Duration	Continuous
Junction Temperature	+150°C

PACKAGING

INA102 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

ORDERING INFORMATION

INA102 A D

Basic model number

Grade/temperature range
A = −25°C to +85°C

Package code
D = Die

BURR-BROWN®

OPA27 DIE

Ultra-Low Noise Precision OPERATIONAL AMPLIFIER DIE

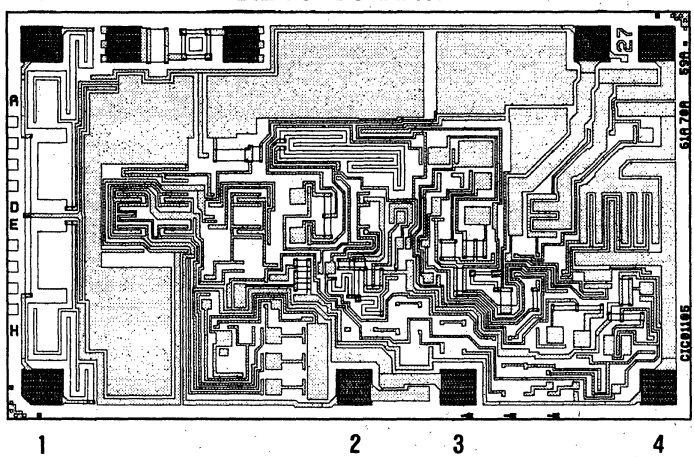
DESCRIPTION

The OPA27 is an ultra-low noise, high precision operational amplifier. It is an improved replacement for the industry-standard OP-27.

Laser-trimmed thin-film resistors provide excellent long-term stability and allow superior offset voltage compared to common zener-zap trim techniques.

A unique bias current cancellation circuit (patent pending) allows bias and offset current specifications to be met over the full −55°C to +125°C temperature range.

DIE TOPOGRAPHY



Pad	Function
1	Offset Trim
2	Inverting Input
3	Noninverting Input
4	Negative Supply and Substrate
5	None
6	Output
7	Positive Supply
8	Offset Trim

Die Size: 99 × 61 mils
Bonding Pad Size: 5 × 5 mils
Backside Contact: Gold

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_{DIE} = +25°C and $\pm V_{CC}$ = 15V unless otherwise specified.

PARAMETER	CONDITIONS	OPA27CD/OPA27GD			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE					
Input Offset Voltage				±60	µV
Average Drift			±0.3		µV/°C
Supply Rejection	$\pm V_{CC}$ = 4V to 18V	95			dB
				18	µV/V
BIAS CURRENT					
Input Bias Current				±80	nA
Input Offset Current				75	nA
VOLTAGE RANGE					
Common-Mode Input Range			±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	100			dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	118			dB
RATED OUTPUT					
Voltage Output	$R_L \geq 2k\Omega$	±11.5			V
	$R_L \geq 600\Omega$	±10.0			V
Short-Circuit Current		±17		±60	mA
POWER SUPPLY					
Current, Quiescent	I_O = 0mADC			±5.7	mA

NOTE: (1) All dice are 100% probe tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22VDC
Input Voltage[1]	±22VDC
Differential Input Voltage[2]	±0.7VDC
Differential Input Current[2]	±25mA
Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration	Continuous
Junction Temperature	+150°C

(1) For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage. (2) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

ORDERING INFORMATION

OPA27 X D

Basic model number

Grade/temperature range
- C = −55°C to +125°C
- G = −25°C to +85°C

Package code
- D = die

PACKAGING

OPA27 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

BURR-BROWN®

OPA37 DIE

Ultra-Low Noise Precision OPERATIONAL AMPLIFIER DIE

DESCRIPTION

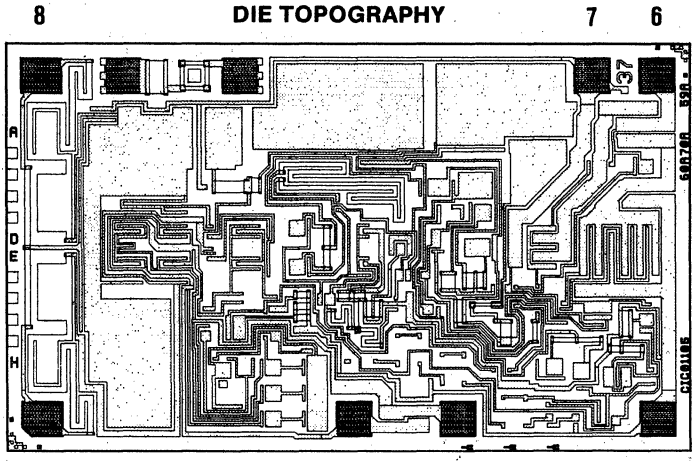
The OPA37 is an ultra-low noise, high precision operational amplifier. It is an improved replacement for the industry-standard OP-37.

Laser-trimmed thin-film resistors provide excellent long term stability and allow superior offset voltage compared to common zener-zap trim techniques.

A unique bias current cancellation circuit (patent pending) allows bias and offset current specifications to be met over the full −55°C to +125°C temperature range.

The uncompensated OPA37 requires a gain ≥5 for loop stability.

DIE TOPOGRAPHY



Pad	Function
1	Offset Trim
2	Inverting Input
3	Noninverting Input
4	Negative Supply and Substrate
5	None
6	Output
7	Positive Supply
8	Offset Trim

Die Size: 99 × 61 mils
Bonding Pad Size: 5 × 5 mils
Backside Contact: Gold

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_{DIE} = +25°C and $\pm V_{CC}$ = 15V unless otherwise specified.

PARAMETER	CONDITIONS	OPA37CD/OPA37GD MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage				±60	µV
Average Drift			±0.3		µV/°C
Supply Rejection	$\pm V_{CC}$ = 4V to 18V	95			dB
				18	µV/V
BIAS CURRENT					
Input Bias Current				±80	nA
Input Offset Current				75	nA
VOLTAGE RANGE					
Common-Mode Input Range			±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	100			dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	118			dB
RATED OUTPUT					
Voltage Output	$R_L \geq 2k\Omega$	±11.5			V
	$R_L \geq 600\Omega$	±10.0			V
Short-Circuit Current		±17		±60	mA
POWER SUPPLY					
Current, Quiescent	I_O = 0mADC			±5.7	mA

NOTE: (1) All dice are 100% probe tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22VDC
Differential Input Voltage[1]	±0.7VDC
Differential Input Current[1]	±25mA
Input Voltage Range[2]	±22VDC
Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration	Continuous
Junction Temperature	+150°C

(1) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
(2) For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING INFORMATION

OPA37 X D

Basic model number

Grade/temperature range
- C = −55°C to +125°C
- G = −25°C to +85°C

Package code
- D = die

PACKAGING

OPA37 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

BURR-BROWN®

OPA111 DIE

Precision Dielectrically-Isolated FET
Difet®
OPERATIONAL AMPLIFIER DIE

DESCRIPTION

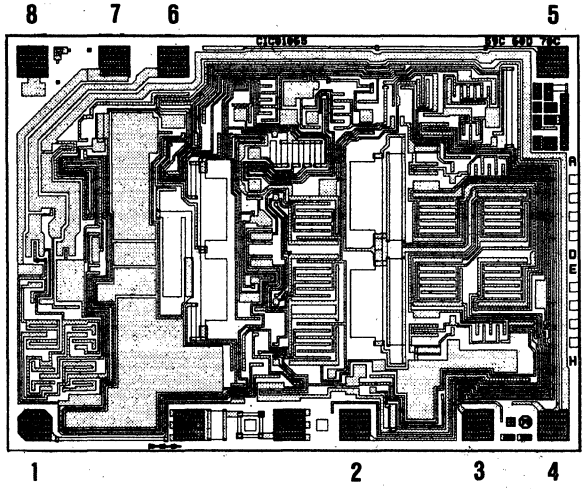
The OPA111 is a precision monolithic dielectrically-isolated FET (*Difet*®) operational amplifier.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser-trimming of thin film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Offset Trim	5	Offset Trim
2	Inverting Input	6	Output
3	Noninverting Input	7	Positive Supply
4	Negative Supply	8	Substrate*

Die Size: 96 × 71 mils
Bonding Pad Size: 5 × 5 mils
Backside Contact: Gold

*This dielectrically-isolated substrate is normally connected to common.

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_{DIE} = +25°C and $\pm V_{CC}$ = 15V unless otherwise specified. Pad 8 connected to common.

PARAMETER	CONDITIONS	OPA111AD MIN	OPA111AD TYP	OPA111AD MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage	V_{CM} = 0VDC			±500	µV
Average Drift	T_{DIE} = +25°C to +85°C			±15	µV/°C
Supply Rejection	$\pm V_{CC}$ = 5V to 15V	86			dB
				50	µV/V
BIAS CURRENT					
Input Bias Current	V_{CM} = 0VDC				
	T_{DIE} = +85°C			±750	pA
	T_{DIE} = +25°C		±0.8		pA
VOLTAGE RANGE					
Common-Mode Input Range		±10			V
Common-Mode Rejection	V_{IN} = ±10VDC	86			dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	105			dB
RATED OUTPUT					
Voltage Output	R_L = 2kΩ	±10			V
Short-Circuit Current		±10		±60	mA
POWER SUPPLY					
Current, Quiescent	I_O = 0mADC			±4.5	mA

NOTE: (1) All dice are 100% probe tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18VDC
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration	Continuous
Junction Temperature	+175°C

ORDERING INFORMATION

OPA111 A D

Basic model number

Grade/temperature range
A = −25°C to +85°C

Package code
D = die

PACKAGING

OPA111 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

BURR-BROWN®

OPA606 DIE

High-Speed Dielectrically-Isolated FET
Difet®
OPERATIONAL AMPLIFIER DIE

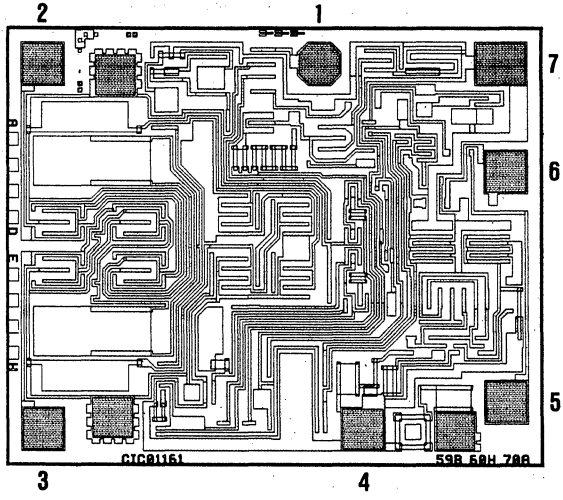
DESCRIPTION

The OPA606 is a dielectrically isolated FET (*Difet*®) operational amplifier that is an improved replacement for the industry-standard LF156A BIFET® operational amplifier.

The OPA606 features wider bandwidth, higher slew rate, and lower bias current. Noise performance is far superior to MOSFET-input operational amplifiers.

The OPA606 design features laser-trimmed thin-film resistors for low offset voltage and drift. It is internally compensated for unity-gain stability.

OPA606 DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Offset Trim	5	Offset Trim
2	Inverting Input	6	Output
3	Noninverting Input	7	Positive Supply and Substrate
4	Negative Supply		

Die Size: 65 × 54 mils

Bonding Pad Size: 5 × 5 mils

Backside Contact: Gold

BIFET® National Semiconductor Corp., *Difet*® Burr-Brown Corp.

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_{DIE} = +25°C and $\pm V_{CC}$ = 15V unless otherwise specified.

PARAMETER	CONDITIONS	OPA606KD/OPA606SD MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage	V_{CM} = 0VDC			±2	mV
Average Drift	T_{DIE} = +25°C to +85°C			±15	µV/°C
Supply Rejection	$\pm V_{CC}$ = 10V to 18V	80			dB
				100	µV/V
BIAS CURRENT					
Input Bias Current	V_{CM} = 0VDC				
	T_{DIE} = +85°C			±5	nA
	T_{DIE} = +25°C		±8		pA
VOLTAGE RANGE					
Common-Mode Input Range		±10			V
Common-Mode Rejection	V_{IN} = ±10VDC	80			dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	94			dB
RATED OUTPUT					
Voltage Output	$R_L \geq 2k\Omega$	±10			V
Short-Circuit Current		±5		±60	mA
POWER SUPPLY					
Current, Quiescent	I_O = 0mADC			±7.5	mA

NOTE: (1) All dice are 100% probe tested and guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18VDC
Differential Input Voltage	±36VDC
Input Voltage Range[1]	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Output Short Circuit Duration	Continuous
Junction Temperature	+175°C

(1) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to the negative supply voltage.

ORDERING INFORMATION

OPA606 X D

- Basic model number
- Grade/temperature range
  - K = 0°C to +70°C
  - S = −55°C to +125°C
- Package code
  - D = die

PACKAGING

OPA606 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

BURR-BROWN®

OPA2111 DIE

Precision Dielectrically-Isolated FET
Difet®
DUAL OPERATIONAL AMPLIFIER DIE

DESCRIPTION

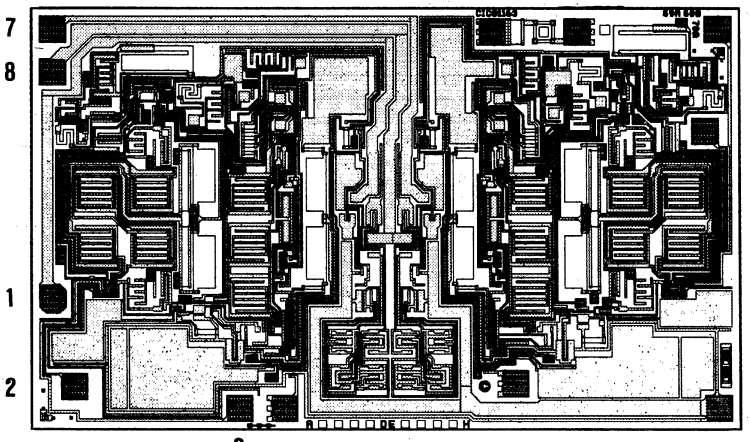
The OPA2111 is a precision dual monolithic dielectrically-isolated FET (*Difet*®) operational amplifier.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Output A	5	Noninverting Input B
2	Inverting Input A	6	Inverting Input B
3	Noninverting Input A	7	Output B
4	Negative Supply	8	Positive Supply

Die Size: 138 × 84 mils
Bonding Pad Size: 5 × 5 mils
Backside Contact: Gold

NOTE: This dielectrically-isolated substrate is normally connected to positive supply

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_{DIE} = +25°C and $\pm V_{CC}$ = 15V unless otherwise specified.

PARAMETER	CONDITIONS	OPA2111AD MIN	OPA2111AD TYP	OPA2111AD MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage	V_{CM} = 0VDC			±500	µV
Average Drift	T_{DIE} = +25°C to +85°C			±15	µV/°C
Supply Rejection	$\pm V_{CC}$ = 10V to 18V	84			dB
				63	µV/V
BIAS CURRENT					
Input Bias Current	V_{CM} = 0VDC				
	T_{DIE} = +85°C			±1	nA
	T_{DIE} = +25°C		±2		pA
VOLTAGE RANGE					
Common-Mode Input Range		±10			V
Common-Mode Rejection	V_{IN} = ±10VDC	88			dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	105			dB
RATED OUTPUT					
Voltage Output	R_L = 2kΩ	±10			V
Short-Circuit Current		±10		±60	mA
POWER SUPPLY					
Current, Quiescent	I_O = 0mADC			±9	mA

NOTE: (1) All dice are 100% probe tested and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18VDC
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration	Continuous
Junction Temperature	+175°C

PACKAGING

OPA2111 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

ORDERING INFORMATION

OPA2111 A D

Basic model number

Grade/temperature range
A = −25°C to +85°C

Package code
D = die

BURR-BROWN®

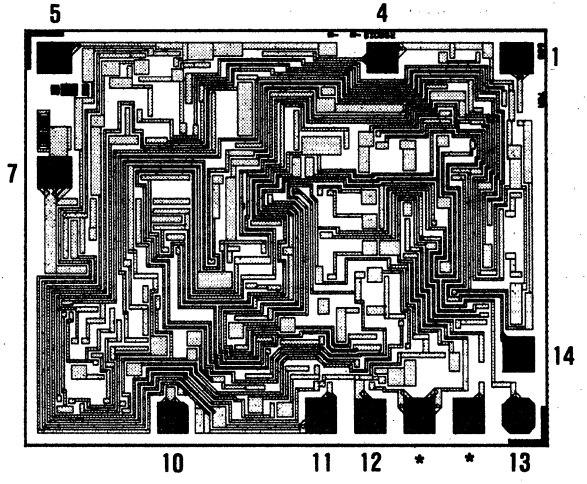
VFC32 DIE

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER DIE

DESCRIPTION

The VFC32 is a monolithic voltage-to-frequency converter circuit including precision input integrator op amp, comparator, one-shot, and switched current source. It is capable of accurate voltage-to-frequency and frequency-to-voltage conversion at frequencies to 500kHz.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Inverting Integrator Input	11	Common
4	$-V_{CC}$	12	$+V_{CC}$
5	One-shot Capacitor	13	V_{OUT}
7	f_{OUT}	14	Noninverting Integrator Input
10	Comparator Input	*	DO NOT CONNECT

Die Size: 89 × 72 mils (2.26 × 1.83mm)

Bonding Pad Size: 5 × 5 mils (0.127 × 0.127mm)

Backside Contact: Gold

NOTE: The junction-isolated substrate is connected to $-V_{CC}$. Any electrical connection to the back side must be returned to the die's $-V_{CC}$ connection.

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SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_{DIE} = +25°C and $\pm V_{CC}$ = 15V unless otherwise noted.

PARAMETER	CONDITIONS	VFC32BD MIN	VFC32BD TYP	VFC32BD MAX	UNITS
V/F TRANSFER FUNCTION					
Input Range		0		0.25	mA
Gain Error	f = 10kHz		5		%
Nonlinearity	f = 10 kHz		0.005		%
Gain Drift	f = 10 kHz		50		ppm/°C
Maximum Operating Frequency				500	kHz
INTEGRATOR AMPLIFIER					
V_{OS}			1	4	mV
V_{OS} Drift			5		µV/C
I_B Inverting Input			20	100	nA
Noninverting Input			100	250	nA
CM Range		−10		0	V
V_{OUT} Range		0		10	V
OPEN COLLECTOR OUTPUT					
V_{OL}	I_{OUT} = 8mA		0.2	0.4	V
I_{OH}, (off leakage)			0.01	2	µA
POWER SUPPLY					
Operating Range		±11		±20	V
Quiescent Current			5.5	6.5	mA

NOTE: (1) All dice are 100% probe tested to the above specification limits. Due to possible wafer saw and assembly shifts, parameters are not guaranteed for assembled units.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±22V
F_{OUT} Currrent Sink	50mA
Output Current, V_{OUT}	20mA
Input Voltage, ±In	$\pm V_{CC}$
Comparator Input	$\pm V_{CC}$
Temperature Range, Storage	−65°C to 150°C

ORDERING INFORMATION

VFC32 B D

Basic model number

Grade/temperature range
B = −25°C to +85°C

Package code
D = Die

PACKAGING

Die are visually inspected to MIL-STD-883, method 2010, Test condition B. and are shipped in sealed carriers.

BURR-BROWN®

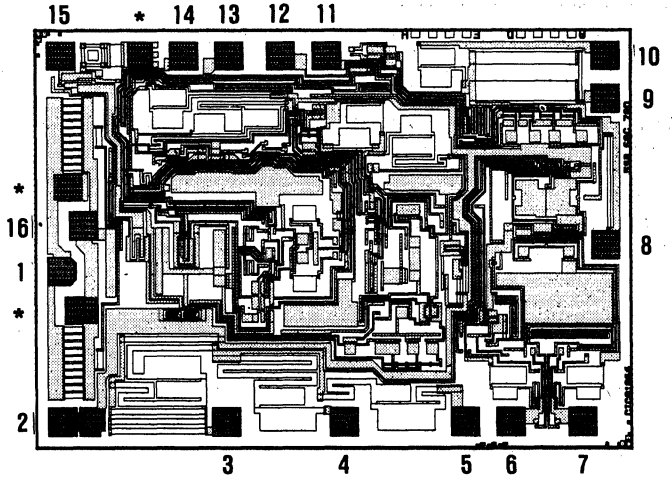
XTR110 DIE

Precision VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER DIE

DESCRIPTION

The XTR110 is a precision monolithic voltage-to-current converter. It can convert standard 0V to +10V or 0V to +5V inputs into 4mA to 20mA, or 5mA to 25mA outputs. The required external MOS transistor keeps heat outside the die to optimize performance under all output conditions. The XTR110 features a precision +10V reference output. The XTR110 can be used as a current-mode transmitter or a programmable current source.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Source Resistor	9	16mA Span
2	Common	10	4mA Span
3	V_{REF} In	11	V_{REF} Adjust
4	$V_{IN\ 1}$ (10V)	12	V_{REF} Sense
5	$V_{IN\ 2}$ (5V)	13	Source Sense
6	Offset Adjust	14	Gate Drive
7	Offset Adjust	15	V_{REF} Force
8	Span Adjust	16	$+V_{CC}$

Die Size: 109 × 78 mils
Bonding Pad Size: 5 × 5 mils
Backside Contact: Gold

*Do Not Connect

NOTE: The back of the die should not be used for the common connection.

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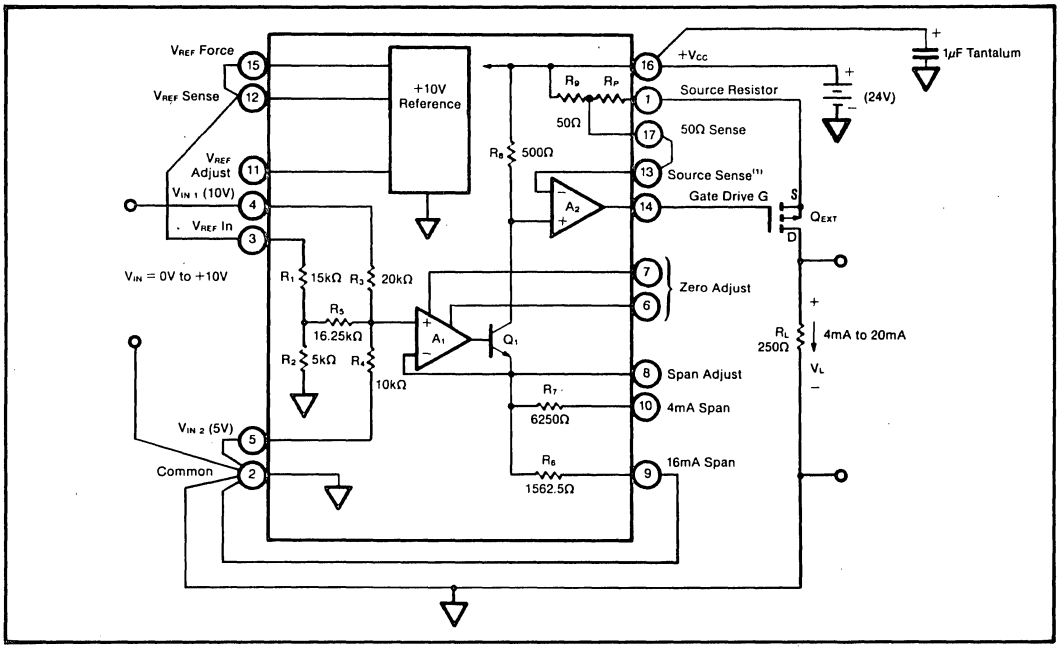


FIGURE 1. Recommended Connection for the XTR110AD with 50Ω Sense.

Functionally, the XTR110AD is compatible with the XTR110AG, BG, and KP (packaged parts). The XTR-110AD, however, has an extra bond pad designated 50Ω sense. This is a Kelvin point for the feedback. It eliminates the parasitic wire bond and interconnect resistance, R_P that occurs during assembly. Because it is outside the feedback loop, R_P now adds no error to the span. This maintains the high accuracy trimmed during manufacturing of the die.

SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_{DIE} = +25°C and $+V_{CC}$ = 24V and R_L = 250Ω and connected as shown in Figure 1 unless otherwise specified.

PARAMETER	CONDITIONS	XTR110AD MIN	XTR110AD TYP	XTR110AD MAX	UNITS
TRANSFER FUNCTION	$I_O = 10\ [(V_{REF}\ IN/16) + (V_{IN\ 1}/4) + V_{IN\ 2}/2)]/R_{SPAN}$				
INPUT RANGE					
$V_{IN\ 1}$	I_O = Specified Range	0		+10	V
$V_{IN\ 2}$		0		+5	V
OUTPUT CURRENT	[2]	4		20	mA
OFFSET CURRENT ERROR	[2] I_O = 4mA			±0.1	% of Span
SPAN ERROR[3]	[2] I_O = 20mA			±0.2	% of Span
NONLINEARITY	4mA ≤ I_O ≤ 20mA		±0.005	±0.025	% of Span
VOLTAGE REFERENCE					
Output Voltage		+9.98	+10	+10.02	V
Output Current[4]		+10			mA
POWER SUPPLY					
Voltage		+13.5		+40	V
Current	Excluding I_O			+4.5	mA

NOTES: (1) All die are 100% probe tested at wafer level and are guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) Including internal reference. External transistor is required. (3) Span is the change in output current resulting from a full scale change in input voltage. (4) Reference current drive can be extended by using an external NPN transistor.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+40V
Input Voltage Range	$+V_{CC}$
Storage Temperature Range	−65°C to 150°C
Output Short-Circuit Duration	
Drive and V_{REF} Force	Continuous to common and $+V_{CC}$
Output Current Using Internal 50Ω resistor	40mA
Junction Temperature	+150°C

PACKAGING

XTR110 die are visually inspected to MIL-STD-883, Method 2010, Test Condition B and are shipped in sealed carriers.

ORDERING INFORMATION

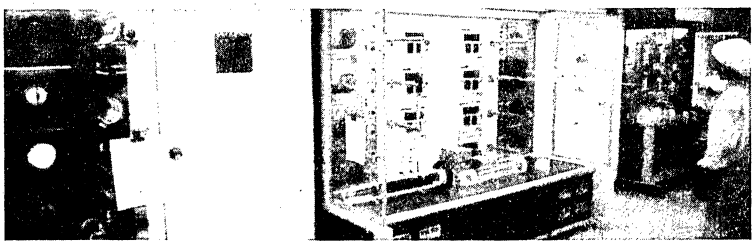
XTR110 A D

Basic model number

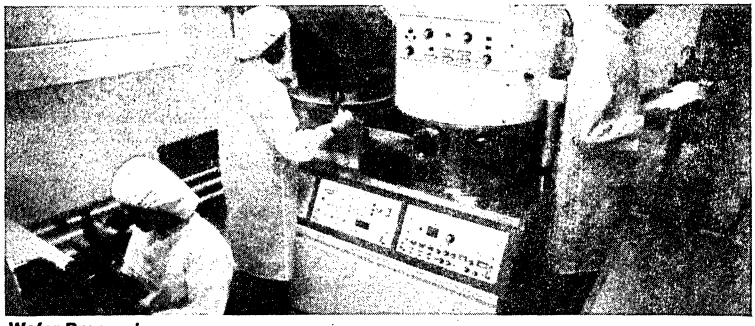
Grade/temperature range
A = −25°C to +85°C

Package code
D = Die

MILITARY PRODUCTS DIVISION



Wafer Processing



Wafer Processing

High quality products for demanding military and industrial applications are produced by our Military Products Division in a totally separate facility within Burr-Brown's complex. Burr-Brown's facilities have been certified to both MIL-STD-976 and MIL-STD-1772.

Reliability is designed and manufactured-into our Military Products under the guidance of MIL-M-38510.

All product families are fully specified from −55°C to +125°C with up to three performance grades and two product assurance levels (/883B and standard).

The "/883B" or "/B" models are compliant to the requirements of MIL-STD-883, Methods 5004 or 5008 with Quality Conformance Inspection (QCI) compliant to the requirements of Methods 5005 or 5008. The standard models are products which have been subjected to many of the screening steps of the "/883B" product. For details see individual product data sheets.

How stringently our Military Products group controls and documents the assembly and testing of its products is described in the product flow section that follows.

All materials used by the Military Products group have unique component specifications to assure their conformity to MIL-STD-883, methods 2010 and 2017.

Environmental control in our clean room areas meets and often exceeds Federal Standard 209B requirements for particle count. ESD (electrostatic discharge) procedures are fully observed through every stage of material handling, product assembly, testing, storage and shipment. Operator training, certification and re-certification conform to MIL-M-38510.

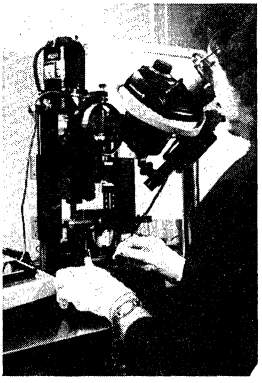
MTTF data is based on actual product performance, not just calculated values. Qualification reports and test data are available. All data sheets follow military slash sheet format and, because of their completeness, can be transferred directly to your drawings with minimal modification. This standard QPL slash sheet format simplifies your requests to government agencies for non-standard parts approval.

A CONTROLLED MANUFACTURING FACILITY DEDICATED EXCLUSIVELY TO MILITARY QUALITY PRODUCTION

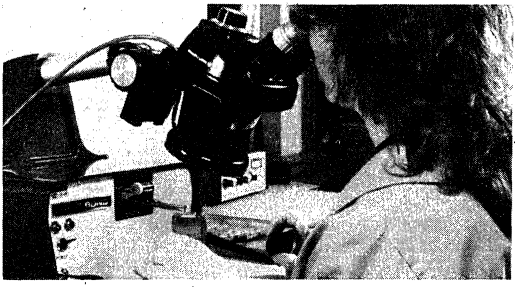
- PERSONNEL—All production and quality control personnel directly involved with fabrication, inspection, testing and handling perform their functions according to appropriate MIL specs.
- TRAINING—Operator training and certification programs provide trained personnel qualified to assemble and test the products. Certification requires classroom training and written examinations for initial certification. Periodic written exams must be passed to maintain certification.
- WORK-IN-PROCESS ENVIRONMENT—All work-in-process is stored in a nitrogen environment. Critical assembly processes, die visual, die attach, wirebond and all inspections are performed under laminar flow hoods—equipped with ion grids—in a class 100 environment.
- ENVIRONMENTAL CONTROL—Clean room procedures, which conform to Federal Standard 209B, provide clean air meeting or exceeding the requirement of MIL-STD-883.
- MATERIAL CONTROL—Each product has a complete and current flow chart and flow sheet to assure accurate processing through assembly and test. Each manufacturing lot contains the lot numbers of its components listed by the quality control inspection identification (QCID number), all traceable back to the incoming vendor's lot number.
- MANUFACTURING LOT CONTROL—Each lot has a unique flow sheet which documents lot number, parts list, operation, quantity, data of operation and operator's identification.
- EQUIPMENT CALIBRATION—Performed under the guidance of MIL-STD-45662.
- QUALIFICATION—All /MIL models are initially qualified per MIL-STD-883, method 5005 or 5008, groups A, B, C and D as described in the products' detailed specification.
- STATIC CONTROL—To minimize static (ESD) damage, antistatic smocks, stainless steel table tops, stainless steel work-in-process trays, ground straps, ion grids under laminar flow hoods and anti-static shipping materials are used.
- RECORD RETENTION—All flow sheets containing process data and inspection records are retained for three years.

Assembly Under Laminar Hood

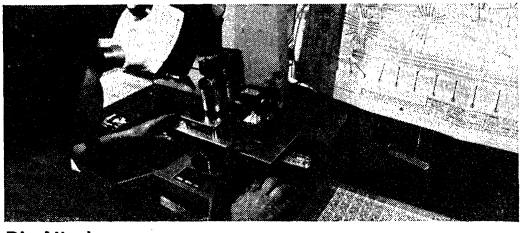
Wirebond (Gold)



Die Shear

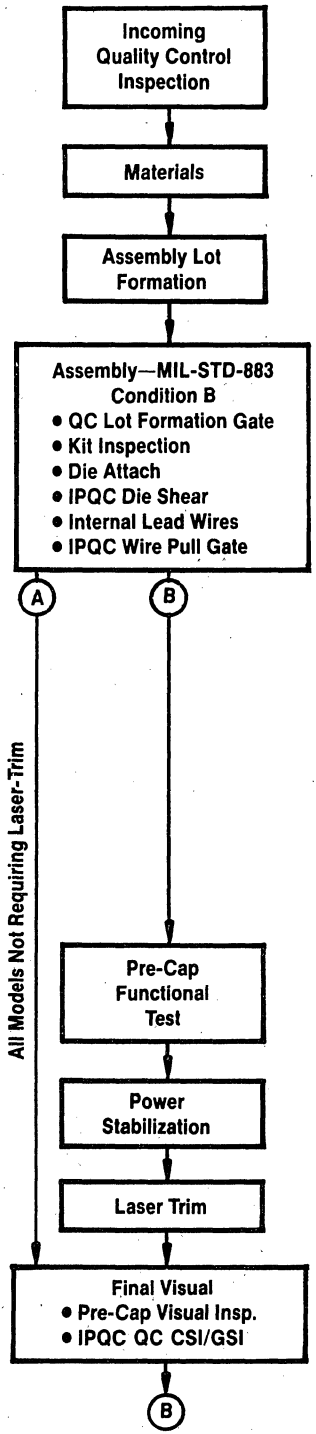


Wirebond (Aluminum)



Die Attach

PRODUCT FLOW



Assures that all materials meet requirements of the applicable component specification. Usage tests are performed and vendor lot traceability begins.

All material is maintained in a bonded stockroom to assure traceability.

Origination of manufacturing flow sheets, bill of material, materials and lot traceability records.

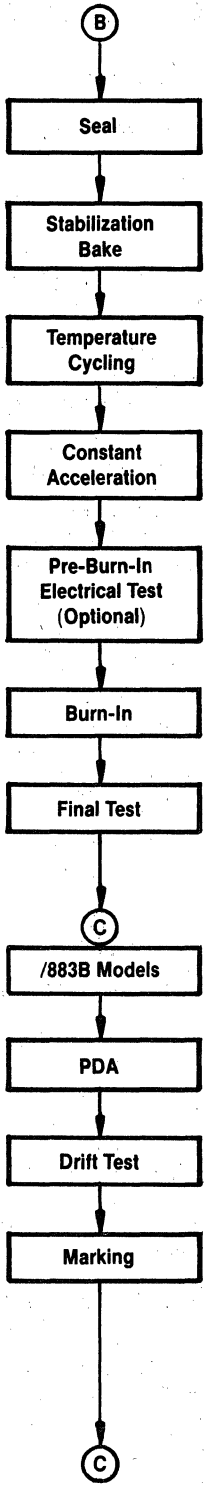
- QC Lot Formation Gate—matches flow sheet, bill of materials and traceability records with materials issued from the stockroom.
- Kit Inspection—piece parts and die are 100% visually inspected to methods 2010 and 2017.
- Die Attach—eutectic (providing low ohmic contact) and non-conductive epoxy (cured at 25°C above storage temperature in nitrogen).
- In Process Die Shear Gate—perfomed to method 2019 on each manufacturing lot. Assures the integrity of the die attach method.
- Internal Lead Wires—Wires are of the same metal as the die metalization. Aluminum ultrasonic wirebond machines are mounted on shock tables to insure quality bonds. Gold-to-gold wirebonds are performed with thermosonic wirebond machines.
- In Process Wire Pull Gates—bonding operations are monitored at the beginning of each shift, every four hours, with a new lot, new operator or a machine adjustment. Both destruct and nondestruct tests are performed and the length and width of each wirebond is measured to verify conformance to method 2010 or 2017.

Performed on all products that require laser trimming.

All products that require laser-trimming receive a 72-hour burn-in, in nitrogen, at +125°C.

Resistor networks are laser-trimmed to meet applicable specifications.

- Pre-Cap Visual Inspection—a 100% visual inspection to method 2010 or 2017.
- In Process QC Pre-Cap Visual Gate—performed to method 2010 or 2017. (Source Inspection performed if required.)



Following a vacuum bake at +125°C (to meet method 5004 or 5008 moisture content requirements), products are welded, gold/tin or glass sealed.

A 24-hour minimum bake at +150°C per MIL-STD-883, method 1008, condition C.

Ten cycles, from −65°C to +150°C per MIL-STD-883, method 1010, condition C.

Performed to MIL-STD-883, method 2001, in the Y_1 axis only.

Product performance is compared to the specified DC parameters at 25°C.

Total burn-in time is 160 hours minimum at an ambient temperature of +125°C per MIL-STD-883, method 1015.

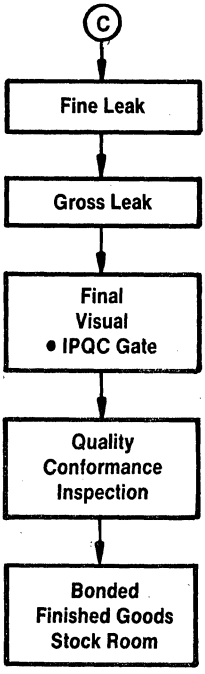
Product performance is compared to the specified DC parameters at 25°C. All 25°C parameters specified in the data sheets are read and recorded.

The assembly lot PDA (percent defective allowable) cannot exceed the PDA specified.

All drift parameters as specified in the data sheet are 100% tested at −55°C, −25°C, +25°C, +85°C and +125°C.

Marking is in accordance with MIL-M-38510 and consists of:

- Part number
- Seal date code
- Manufacturer's identification (Burr-Brown logo)
- Manufacturer's designating symbol (CEBS)
- Country of origin



100% test to MIL-STD-883, method 1014, test condition A.

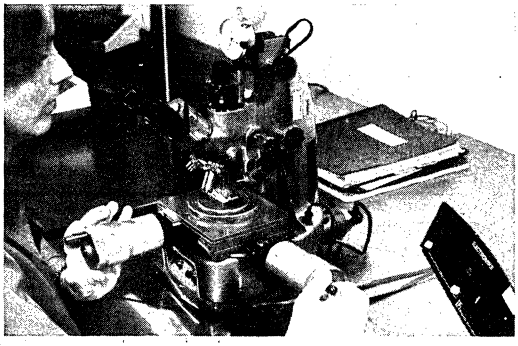
100% test to MIL-STD-883, method 1014, condition C.

100% external visual inspection to MIL-STD-883, method 2009.

- Final Visual Quality Control Gate—to MIL-STD-883, method 2009.

Groups A and B inspection of MIL-STD-883, method 5005 or 5008 are performed on each inspection lot. Groups C and D inspections are performed as required by MIL-STD-883. A report of the most recent Groups C and D inspections is available from Burr-Brown at a nominal charge.

This product flow illustrates major operations only. Space does not allow a complete description of the numerous details of all operations. Processes and flows may change to conform to latest revisions or to improve product performance and quality.



Bond Measurement

Wire Pull

SELECTION GUIDE

ANALOG-TO-DIGITAL CONVERTERS								
Model	Resolution (Bits)	Linearity, max (±LSB)	Conversion Time, max (μsec)	Gain Drift, max (±ppm/°C)	Input Range (V)	Operating Temperature Range[1]	Package	Page
ADC87/883B	12	1/2	10	15	±2.5, ±5, ±10, 0 to +5, 0 to +10	MIL	32-pin DIP	12-8
ADC87	12	1/2	10	15		MIL		12-8
ADC87U/883B	12	1/2	10	15		MIL		12-8
ADC87U	12	1/2	10	15		MIL		12-8
ADC87V/883B	12	1/2	10	15		MIL		12-8
ADC87V	12	1/2	10	15		MIL		12-8

DIGITAL-TO-ANALOG CONVERTERS									
Model	Resolution (Bits)	Linearity, max (±LSB)	Monotonicity	Gain Drift, max (±ppm/°C)	Settling Time, max	Output Ranges (V)	Operating Temperature Range[1]	Package	Page
DAC87-CBI-V/B	12	1/2	−55°C/+125°C	20	7μsec	±2.5, ±5, ±10, +5, +10	MIL	24-pin DIP	12-24
DAC87-CBI-V	12	1/2	−55°C/+125°C	20	7μsec		MIL	24-pin DIP	12-24
DAC87U-CBI-V/B	12	1/2	−25°C/+85°C	20	7μsec		MIL	24-pin DIP	12-24
DAC87U-CBI-V	12	1/2	−25°C/+85°C	20	7μsec		MIL	24-pin DIP	12-24
DAC87-CBI-I/B	12	1/2	−55°C/+125°C	20	400nsec	0 to 2mA, ±1mA	MIL	24-pin DIP	12-36
DAC87-CBI-I	12	1/2	−55°C/+125°C	20	400nsec		MIL	24-pin DIP	12-36
DAC87U-CBI-I/B	12	1/2	−25°C/+85°C	20	400nsec		MIL	24-pin DIP	12-36
DAC87U-CBI-I	12	1/2	−25°C/+85°C	20	400nsec		MIL	24-pin DIP	12-36
DAC870V/883B	12	1/2	−55°C/+125°C	25	7μsec	±2.5, ±5, ±10, 0 to +5, 0 to +10	MIL	24-pin DIP ceramic	12-48
DAC870V	12	1/2	−55°C/+125°C	25	7μsec		MIL		12-48
DAC870U/883B	12	1/2	−25°C/+85°C	20	7μsec		MIL		12-48
DAC870U	12	1/2	−25°C/+85°C	20	7μsec		MIL		12-48
DAC870VL/883B	12	1/2	−55°C/+125°C	25	7μsec		MIL	28-term. leadless chip carrier	12-48
DAC870VL	12	1/2	−55°C/+125°C	25	7μsec		MIL		12-48
DAC870UL/883B	12	1/2	−25°C/+85°C	20	7μsec		MIL		12-48
DAC870UL	12	1/2	−25°C/+85°C	20	7μsec		MIL		12-48

VOLTAGE-TO-FREQUENCY CONVERTERS							
Model	V_{IN} Range (V)	F_{OUT} Range, max (kHz)	Linearity, max (% FSR)	Full Scale Drift, max (ppm FSR/°C)	Operating Temperature Range[1]	Package	Page
VFC32WM/883B	±10	200	±0.006 at 10kHz	±100 at 10kHz	MIL	TO-100	12-135
VFC32WM	±10	200	±0.006 at 10kHz	±100 at 10kHz	MIL	TO-100	12-135
VFC32VM/883B	±10	200	±0.01 at 10kHz	−400, +150 at 200kHz	MIL	TO-100	12-135
VFC32VM	±10	200	±0.01 at 10kHz	−400, +150 at 200kHz	MIL	TO-100	12-135
VFC32UM/883B	±10	200	±0.01 at 10kHz	±150 at 10kHz	MIL	TO-100	12-135
VFC32UM	±10	200	±0.01 at 10kHz	±150 at 10kHz	MIL	TO-100	12-135

MULTIPLIERS								
Model	Accuracy at 25°C, max (±%)	Accuracy at 125°C, max (±%)	Feedthrough, max (±mV)	Output Offset, max (±mV)	Output, min (V, mA)	Operating Temperature Range[1]	Package	Page
4213WM/883B	1/2	4	50	25	±10, ±5	MIL	TO-100	12-166
4213WM	1/2	4	50	25	±10, ±5	MIL	TO-100	12-166
4213VM/883B	1	4	100	30	±10, ±5	MIL	TO-100	12-166
4213VM	1	4	100	50	±10, ±5	MIL	TO-100	12-166
4213UM/883B	1	2[2]	100	50	±10, ±5	MIL	TO-100	12-166
4213UM	1	2[2]	100	50	±10, ±5	MIL	TO-100	12-166

NOTES: (1) U grade specified temperature range is −25°C to +85°C; all others specified over MIL temp range. (2) At +85°C.

OPERATIONAL AMPLIFIERS

Description	Model	Offset Voltage: At 25°C, max (±mV)	Offset Voltage: Drift, max (±μV/°C)	Bias Current, max (nA)	Bandwidth Unity Gain, min (MHz)	Slew Rate, min (V/μsec)	ts ±0.01% (nsec)	Compensation	Output, min (V, mA)	Operating Temp. Range[1]	Package	Page
Wideband	OPA600VM/883B	2	20	−100pA	5000,[3] A = 1000	400	125	external	±10, ±200	MIL	16-pin DIP	12-94
	OPA600VM	2	20	−100pA		400	125	external	±10, ±200	MIL		12-94
	OPA600UM/883B	5	80	−100pA		400	150	external	±10, ±200	MIL		12-94
	OPA600UM	5	80	−100pA		400	150	external	±10, ±200	MIL		12-94
General Purpose Bipolar	3500R/883B	5	20	±30	1	0.6	—	internal	±10, ±10	MIL	TO-99	12-147
	3500U/883B	5	20[2]	±30	1	0.6	—	internal	±10, ±10	MIL	TO-99	12-147
Precision Bipolar	3510VM/883B	0.12	2	±25	0.25	0.5	—	internal	±10, ±10	MIL	TO-99	12-158
Low Drift, Low Bias	OPA105WM/883B	.250	2	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	12-74
	OPA105WM	.250	2	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	12-74
	OPA105VM/883B	.250	5	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	12-74
	OPA105VM	.250	5	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	12-74
	OPA105UM/883B	.250	15[2]	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	12-74
	OPA105UM	.250	15[2]	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	12-74
Ultra Low Bias Current	OPA106WM/883B	.250	5	−100fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	12-84
	OPA106WM	.250	5	−100fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	12-84
	OPA106VM/883B	.250	10	−150fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	12-84
	OPA106VM	.250	10	−150fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	12-84
	OPA106UM/883B	.250	20[2]	−300fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	12-84
	OPA106UM	.250	20[2]	−300fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	12-84
Power	OPA8780VM/883B	10	30	−.05	5	15	—	internal	±30, ±60	MIL	TO-3	12-110
	OPA8780VM	10	30	−.05	5	15	—	internal	±30, ±60	MIL	TO-3	12-110
	OPA8780UM/883B	10	50	−.05	5	15	—	internal	±30, ±60	MIL	TO-3	12-110
	OPA8780UM	10	50	−.05	5	15	—	internal	±30, ±60	MIL	TO-3	12-110
	OPA8785VM/883B	5	40	20	1	1.5	—	internal	±30, 10A	MIL	TO-3	12-120
	OPA8785VM	5	40	20	1	1.5	—	internal	±30, 10A	MIL	TO-3	12-120
	OPA8785UM/883B	5	40	20	1	1.5	—	internal	±30, 10A	MIL	TO-3	12-120
	OPA8785UM	5	40	20	1	1.5	—	internal	±30, 10A	MIL	TO-3	12-120

NOTES: (1) U grade specified temperature range is −25°C to +85°C; all others specified over MIL temp range. (2) −25°C to +85°C. (3) Gain-bandwidth product.

INSTRUMENTATION AMPLIFIERS

Description	Model	Gain Range[1]	Gain Accuracy, G = 100, At 25°C, max	Gain Drift, G = 100, typ (ppm/°C)	Non-linearity G = 100 max	Input Parameters: CMR, DC to 60Hz, G = 10, min, 1kΩ Unbal. (dB)	Input Parameters: Offset Voltage vs Temp, G = 100, max (μV/°C)	Dynamic Response, G = 100, ±3dB BW (kHz)	Temp Range[2]	Package	Page
Very High Accuracy	INA258WG/883B	1-1000	0.10	22	0.007	96	0.5	25	MIL	DIP	12-61
	INA258WG	1-1000	0.10	22	0.007	96	0.5	25	MIL	DIP	12-61
	INA258VG/883B	1-1000	0.10	22	0.007	96	1.0	25	MIL	DIP	12-61
	INA258VG	1-1000	0.10	22	0.007	96	1.0	25	MIL	DIP	12-61
	INA258UG/883B	1-1000	0.10	22	0.007	96	3.0	25	MIL	DIP	12-61
	INA258UG	1-1000	0.10	22	0.007	96	3.0	25	MIL	DIP	12-61
	INA258WL/883B	1-1000	0.10	22	0.007	96	0.5	25	MIL	20-terminal leadless chip carrier	12-61
	INA258WL	1-1000	0.10	22	0.007	96	0.5	25	MIL		12-61
	INA258VL/883B	1-1000	0.10	22	0.007	96	1.0	25	MIL		12-61
	INA258VL	1-1000	0.10	22	0.007	96	3.0	25	MIL		12-61
	INA258UL/883B	1-1000	0.10	22	0.007	96	3.0	25	MIL		12-61
	INA258UL	1-1000	0.10	22	0.007	96	3.0	25	MIL		12-61

NOTES: (1) Set with external resistor. (2) U grade specified temperature range is −25°C to +85°C; all others specified over MIL temperature range.

BURR-BROWN®

ADC87/883B SERIES

ADC87/883B ADC87V/883B ADC87U/883B
ADC87 ADC87V ADC87U

REVISION C
JANUARY, 1986

12-Bit −55°C to +125°C Military ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **HI-REL MANUFACTURE**
- **ACCURATE**
  - **±1/2LSB max Linearity Error**
  - **±0.1% FSR max Full-Scale Absolute Accuracy**
  - **±15ppm max Gain Drift**
- **10μsec MAX CONVERSION TIME**
- **-55°C TO +125°C OPERATION**
- **COMPLETE**
  - **Internal Reference**
  - **Internal Buffer**
  - **Internal Clock**
- **MIL-STD-883 SCREENING**

DESCRIPTION

The ADC87/883B Series is a high performance, analog-to-digital converter. It features ±1/2LSB linearity, ±0.1% full-scale accuracy, ±15ppm drift, 8μsec conversion time, −55°C to +125°C operation and optional MIL-STD-883 screening.

The ADC87 uses successive approximation. It resolves the most significant bit firsy, then the second bit, then the third, etc. Successive approximation is the most popular high performance design as it is fast and accurate.

The ADC87 is a hybrid microcircuit. It is complete with an internal reference, an input buffer amplifier and an internal clock. The converter may be short cycled to provide faster conversion to less resolution. Five analog input ranges—±2.5V, ±5V, ±10V, 0 to +10V, and 0 to +20V are available, and the digital output data is available in parallel and serial format. All digital outputs and inputs are TTL-compatible. Standard power supply voltages (±15VDC and +5VDC) are required.

Three electrical performance grades are available. The premium grade and the "V" operate from −55°C to +125°C and are designed for military, aerospace, and demanding industrial applications. The U grade is specified from −25°C to +85°C and from −55°C to +125°C. Applications include test equipment, shipboard, and ground support equipment where operation is normally between −25°C and +85°C and full temperature range operation must be assured.

The ADC87/883B Series is manufactured on a separate Hi-Rel manufacturing line with impeccable clean room conditions which assures inherent quality and provides for long product life. The ADC87 is hermetically-sealed in a metal, welded, dual-in-line package.

Two product assurance levels are available: Standard, and /883B. The Standard product assurance level offers Hi-Rel manufacturing where many MIL-STD-883 screens are performed routinely. The /883B product assurance level, /883B suffix, offers Hi-Rel manufacturing, 100% screening per MIL-STD-883B method 5008 and 10% PDA. Quality assurance further processes /883B devices, by performing group A and B inspections on each inspection lot and group C and D inspections periodically and when specified on the customer's purchase order. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
ANALOG-TO-DIGITAL CONVERTER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detailed requirements for a precision 12-bit, integrated circuit, analog-to-digital converter.

1.2 Part number. The complete part number is as shown below.

ADC87		/883B
Basic model number	Grade (see 1.2.1)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, 12-bit, analog-to-digital converter. There are two electrical performance grades. The premium grade has no grade designation in the part number and features specifications and tests from −55°C to +125°C. The V grade has a V grade designation in the part number and features specifications and tests from −55°C to +125°C. The U grade has a U grade designation in the part number and features specifications and tests from −25°C to +85°C, and specifications from −55°C to +125°C.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:

Hi-Rel Product Designator	Requirements
/883B	Standard model, plus 100% MIL-STD-883, method 5008, Class B screening with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed per the requirements of MIL-STD-883.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is as defined in Figure 1. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage, V_{CC}	±18VDC
Supply voltage, V_{DD}	+7VDC
Analog inputs (pins 24 and 25)	±25VDC
Buffer input	±18VDC
Digital inputs	+5.5VDC
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60sec)	+300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	V_{CC}: ±14.5VDC to ±15.5VDC V_{DD}: +4.75VDC to +5.25VDC
Case temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ C-A	Maximum θ J-A
32-lead can	Figure 1	1500mW at T_A = 125°C	7°C/W	25°C/W	32°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510, except that organic and polymeric materials may be used for substrate and die attach. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-STD-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. All dice utilized are glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

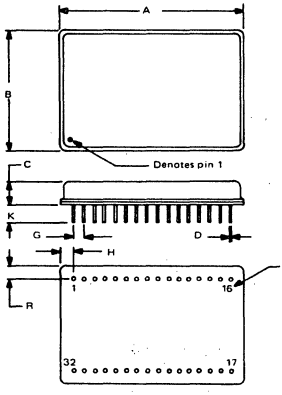
3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connection. The circuit diagram and terminal connections are shown in Figure 2.

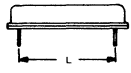
3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating case temperature range of -55°C to +125°C unless otherwise specified.

3.3.1 Input Range. The analog input range is as specified in Table V when externally connected as shown therein.

3.3.2 Output Code. Coding is complementary binary. The digital output codes corresponding to analog input voltages are shown in Table VI.



NOTE:
Leads in true position within 0.010"
(0.25mm) R at MMC at seating plane.



Pin numbers shown for reference only.
Numbers may not be marked on package.

Weight: 25 grams max.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

FIGURE 1. Case Outline (Triple-Wide DIP Configuration).

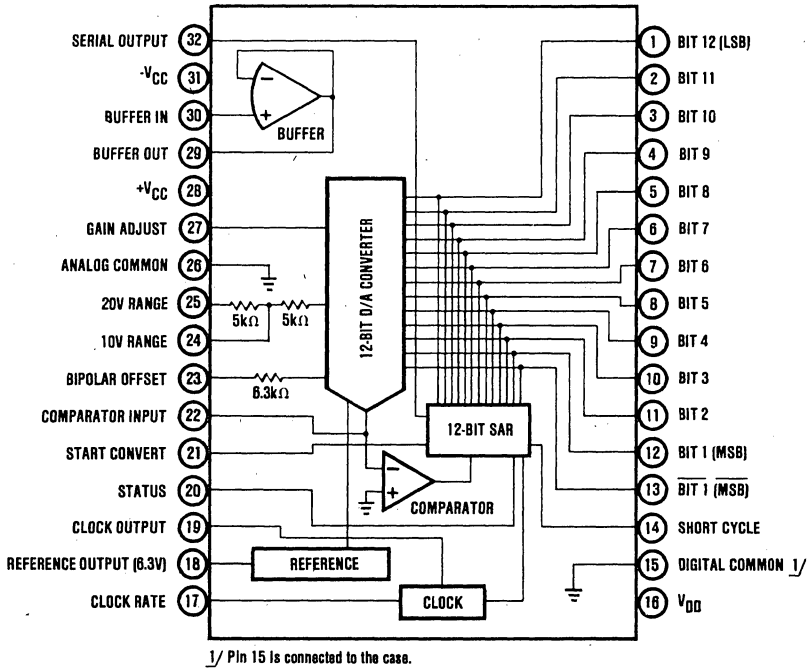


FIGURE 2. Circuit Diagram and Terminal Connections (Bottom View).

3.3.3 Transfer Function. An A/D converter represents an analog input voltage in a digital output format. The converter resolves the analog input into 12 bits of resolution, or 2^{12}, or 4096 voltage segments. For each voltage segment there is a unique digital output code.

The ideal transfer curve, as shown in Figure 3, is a "stair-case" connecting the extremes of the analog input range. Minus full scale (-FS) corresponds to digital 1111 1111 1111, the first transition occurs at -FS +1/2LSB, each bit is 1LSB wide, and +FS -1LSB corresponds to digital 0000 0000 0000. An ideal straight line connects each end point and the center of each bit. A best fit straight line is parallel to the ideal straight line and biased to minimize linearity errors. Note, the coding is complementary.

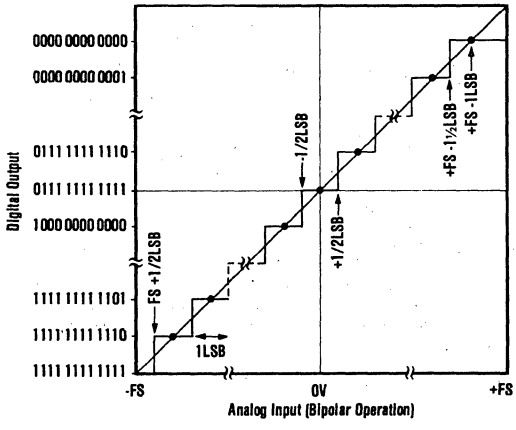
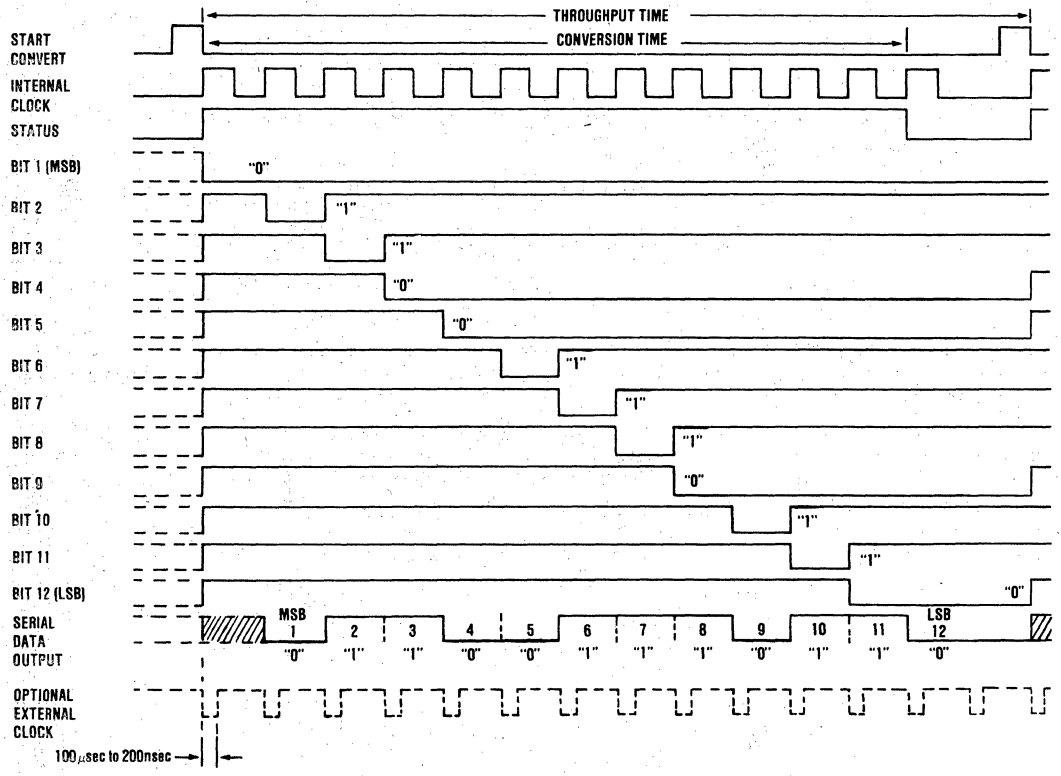


FIGURE 3. Ideal A/D Converter Transfer Function.

The 'basic' converter is unipolar in design; that is, 0VDC analog input produces one digital extreme and plus full scale VDC produces the other digital extreme. There are two unipolar input ranges. For bipolar operation, a bias (bipolar offset) is introduced into the input such that 0VDC analog input produces midscale digital output. This allows plus and minus analog inputs (see Figure 3). There are three bipolar input ranges.

The errors from the best fit transfer function are specified in Table I. Linearity and Differential Linearity are the most meaningful ADC87 accuracy indicators, as they are not externally adjustable. They are factory laser-trimmed. Zero error and gain error are laser-trimmed and may be externally nulled if necessary for the application. The inherent quantization uncertainty due to resolving or quantizing the analog input into bits is ±1/2LSB.

3.3.4 Timing Considerations. The timing diagram is shown in Figure 4. A start convert, positive going pulse, initiates a conversion. The most significant bit (MSB) is determined during the second clock pulse, and each successive bit is determined during the next 11 clock pulses. When conversion is complete, Status output drops to Logic 0. Digital output data is available in parallel or serial format. Serial output data may be strobed out bit-by-bit, during the clock period after the bit is determined. If desired, an external clock may be used. Further information is available in Applications Information, paragraph 7.



1. Start Convert must be at least 50nsec wide and must remain low during conversion. Conversion is initiated by the Start Convert trailing edge. Once a conversion has begun, a second start pulse will not reset the converter.
2. Parallel data will be valid 140nsec after status goes low and remains valid until another conversion is initiated.
3. Serial data will be valid 140nsec after an internal clock rising edge and 200nsec after an external clock falling edge.
4. When using an external clock, conversion is initiated by the falling edge of the first clock pulse following status going low. The converter will continuously convert.

FIGURE 4. Timing Diagram.

3.3.5 Zero error and gain error adjustment. Zero error and gain error may be externally nulled using the circuits shown in Figure 6. See Applications Information, paragraph 7.4.

3.3.6 Required external connections. For specified accuracy and speed, connect Clock Rate, pin 17, to 0VDC, pin 15.

For a 12-bit conversion cycle, connect Short Cycle, pin 14, to Logic 1, pin 16. See Applications Information, paragraph 7, for additional information.

3.4 Electrical test requirements. Electrical test requirements are as specified in Table II. The subgroups of Table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, are specified in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Index point
b. Part number (see paragraph 1.2)
c. Inspection lot identification code 1/
d. Manufacturer's identification (BURR-BROWN®)
e. Manufacturer's designating symbol (CEBS)
f. Country of origin

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /883B Hi-Rel product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability, for /883B, is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening, for the /883B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), constant acceleration (condition A), temperature cycle, and external visual inspection per MIL-STD-883, method 5008, class B.

For the /883B Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /883B Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

1/ A 4-digit date code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each microcircuit.

TABLE I. Electrical Performance Characteristics.

(T_A = −55°C to +125°C, Supply Voltages ±15VDC and +5VDC, unless otherwise specified.)

Characteristics	Conditions	Limits									Units
		ADC87/883B ADC87			ADC87V/883B ADC87V			ADC87U/883B ADC87U			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION		12			•			•			Bits
ANALOG INPUTS											
Input Voltage Ranges											
Unipolar			0 to +5, 0 to +10			•			•		V
Bipolar			±2.5, ±5, ±10			•			•		V
Direct Input Impedance											
0 to +5V, ±2.5V			2.5			•			•		kΩ
0 to +10V, ±5V			5			•			•		KΩ
±10V			10			•			•		kΩ
Buffer Amplifier											
Gain Accuracy			±0.01			•			•		%
Input Impedance	T_A = +25°C		10^{12}			•			•		Ω
Input Bias Current	T_A = +25°C		80			•			•		nA
Offset Voltage	T_A = +25°C		1	5		•			•		mV
Settling Time	20V step to ±0.01% FSR		3			•			•		µsec
DIGITAL INPUTS											
Start Convert Command 1/											
Positive Pulse Width		50			•			•			nsec
Logic Loading				1			•			•	TTL Load 2/
Short Cycle Logic Loading				1			•			•	TTL Load
Logic Levels (all digital inputs)											
Logic "1"		2			•			•			V
Logic "0"				0.8			•			•	V
DIGITAL OUTPUTS											
Parallel Data Coding 3/											
Unipolar Ranges			CSB			•			•		
Bipolar Ranges			COB, CTC			•			•		
Output Drive		2			•			•			TTL Loads
Serial Data Coding (NRZ) 3/			CSB, COB				•				
Output Drive		2			•			•			TTL Loads
Status Bit Coding					Logic 1 During Conversion						
Output Drive		2			•			•			TTL Loads
Internal Clock Output Drive		2			•			•			TTL Loads
Logic Levels (all outputs)											
Logic "1"		2.4			•			•			V
Logic "0"				0.4			•			•	V
TRANSFER CHARACTERISTICS**											
Zero Error, Bipolar 4/ (Bipolar-Major Transition Error)	+25°C		±0.02	±0.05		•	•		•	±0.07	% FSR 5/
	−25°C to +85°C								±0.05	±0.15	% FSR
	−55°C to +125°C		±0.05	±0.1		•	•			±0.3	% FSR
Full Scale Absolute Accuracy Error 4/	+25°C		±0.05	±0.1		•	•		•	±0.15	% FSR
Bipolar 6/	−25°C to +85°C								±0.1	±0.25	% FSR
Gain Error 4/	+25°C		±0.05	±0.1		•	•		•	•	%
	Drift 7/		±10	±15		•	•		•	•	ppm/°C
Zero Error, Unipolar 4/	+25°C		±0.10	±0.15		•	•		•	+0.2	% FSR
	−25°C to 85°C					•	•		±0.15	±0.3	% FSR
	−55°C to +125°C		±0.15	±0.2		•	•			±0.6	% FSR
Full Scale Absolute Accuracy Error	+25°C		±0.1	±0.2		•	•		•	±0.25	% FSR
Unipolar 4/	−25°C to +85°C								±0.2	±0.4	% FSR
	−55°C to +125°C		±0.2	±0.3		•	•			±0.9	% FSR
Linearity Error	+25°C		±1/4	±1/2		•	•		•	•	LSB 8/
	−25°C to +85°C								±1/2	±1	LSB
	−55°C to +125°C		±1/2	±1		•	•			±4	LSB
	Drift			±2						•	ppm of FSR/°C
Inherent Quantization Uncertainty			±1/2			•			•		LSB
Differential Linearity Error	+25°C		±1/4	±1/2		•	•		•	•	LSB
	−25°C to +85°C									±1	LSB
	−55°C to +125°C			±1			•			±3	LSB
	Drift		±2			•			•		ppm of FSR/°C

TABLE I. Electrical Performance Characteristics (cont).

(T_A = −55°C to +125°C, Supply Voltages ±15VDC and +5VDC, unless otherwise specified.)

Characteristics	Conditions	Limits									Units
		ADC87/883B ADC87			ADC87V/883B ADC87V			ADC87U/883B ADC87U			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
No Missing Codes		−55		+125							°C
Monotonicity		−55		+125	•		•	−25		+85	°C
Zero Adjustment Range		0.3	0.4		•	•		•	•		% FSR
Gain Adjustment Range		0.5	0.55		•	•		•	•		% FSR
DYNAMIC CHARACTERISTICS**											
Conversion Time 9/				10			•			•	µsec
Internal Clock Frequency 9/		1.5	1.6		•	•		•	•		MHz
REFERENCE											
Internal Reference Voltage		6.0	+6.3	6.6	•	•	•	•	•	•	V
Drift	−55°C to +125°C		±5			•					ppm/°C
	−25°C to +85°C								±5		ppm/°C
External Current				200			•			•	µA
POWER SUPPLY											
Power Supply Range											
±15V Supply		±14.5	±15	±15.5	•	•	•	•	•	•	V
+5V Supply		+4.75	+5	+5.25	•	•	•	•	•	•	V
Quiescent Current											
+15V			35	45		•	•		•	•	mA
−15V			35	45		•	•		•	•	mA
+5V			40	50		•	•		•	•	mA
Power Consumption	Quiescent		1300	1500		•	•		•	•	mW
Power Supply Rejection											
+15VDC			±0.002			•			•		% FSR/%V_{CC}
−15VDC			±0.002			•			•		% FSR/%V_{CC}
+5VDC			±0.001			•			•		% FSR/% V_{CC}
THERMAL CHARACTERISTICS											
Operating Temperature Range	Ambient	−55		+125	•		•	•		•	°C
Storage Temperature Range	Ambient	−65		+150	•		•	•		•	°C
Thermal Impedance											
Case to Ambient, θ_{CA}			20			•			•		°C/W
Junction to Case, θ_{JC}			5			•			•		°C

* Specifications the same as ADC87/883B.

** Transfer and dynamic characteristics are specified without the optional buffer amplifiers.

NOTES:

1/ Trailing edge (logic 1 to logic 0) initiates conversion.

2/ A TTL Load is defined as 40µA max at V_{IN} = 2.4VDC (logic 1) and −1.6mA max at V_{IN} = 0.4VDC (logic 0).

3/ CSB = Complementary Straight Binary; COB = Complementary Offset Binary; CTC = Complementary Two's Complement. Serial and parallel output data is in Nonreturn to Zero (NRZ) format. See Output Coding and Timing Diagram.

4/ Externally adjustable to zero. This specification is without external adjustment.

5/ FSR = Full Scale Range. The ±10V analog input range is a 20V FSR. The ±5V or 0 to 10V input range is a 10V FSR.

6/ Applies to +Full Scale and to −Full Scale.

7/ Gain drift is defined as the absolute value of the change from +25°C to the hot temperature, plus the absolute value of the change from +25°C to the cold temperature, and that quantity is divided by the temperature span. This is a 3-point drift. The hot temperature change is usually greater than the cold temperature change.

8/ ±1LSB = ±0.024% FSR.

9/ Conversion time is defined as the width of the status pulse. It is specified using the internal clock, with Clock Rate, pin 17, connected to 0VDC and Short Cycle, pin 14, connected to logic 1.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III.)

Models	ADC87/883B ADC87V/883B	ADC87 ADC87V	ADC87U/883B	ADC87U
MIL-STD-883 Test Requirements (Hybrid Class)		Subgroups (see Table III).		
Interim electrical parameters (preburn-in) (method 5008)	1, 4, 7	1, 4, 7	1, 4, 7	1, 4, 7
Final electrical test parameters (method 5008)	1*, 2, 3, 4, 5, 6, 7	1, 2, 3, 4, 5, 6, 7	1*, 2U, 3U, 4, 7	1, 2U, 3U, 4, 7
Group A test requirements (method 5008)	1, 2, 3, 4, 5, 6, 7	—	1, 2U, 3U, 4, 7	—
Group C end point electrical parameters (method 5008)	1	—	1	—

*PDA applies to subgroup 1 (see 4.3.d).

TABLE III. Group A Inspection.

Subgroup	Parameters	Conditions 1/	Limits						Units
			ADC87/883B ADC87		ADC87V/883B ADC87V		ADC87U/883B ADC87U		
			Min	Max	Min	Max	Min	Max	
1	Zero error, bipolar 2/	±10V range 3/		±10		*		±14	mV
T_A = +25°C	Full scale error, −FS bipolar 2/	±10V range 3/		±20		*		±30	mV
	Full scale error, +FS bipolar 2/	±10V range 3/		±20		*		±30	mV
	Gain error 2/	±10V range		±20		*		*	mV
	Linearity error			±1/2		*		*	LSB
	Differential linearity error 4/			±1/2		*		*	LSB
	No missing codes		Pass		*		*		Pass/fail
	Internal reference voltage		+6.0	+6.6	*	*	*	*	V
	Zero error, unipolar 2/	0 to +10V range 3/	0	+15	*	*	*	*	mV
	Full scale error, unipolar 2/	0 to +10V range 3/		±20		*		*	mV
	Gain error, unipolar 2/	0 to +10V range		±10		*		*	mV
2	Zero error, bipolar	±10V range 3/		±20		*			mV
T_A = +125°C	Full scale error, −FS bipolar 2/	±10V range 3/		±40		*			mV
	Full scale error, +FS bipolar 2/	±10V range 3/		±40		*			mV
	Gain drift	See subgroup 3							
	Linearity error			±1		*			LSB
	Differential linearity error			±1		*			LSB
	No missing codes		Pass		*				Pass/fail
2U	Zero error, bipolar 2/	±10V range 3/						±30	mV
T_A = +85°C	Full scale error, −FS bipolar 2/	±10V range 3/						±50	mV
	Full scale error, +FS bipolar 2/	±10V range 3/						±50	mV
	Gain drift	See subgroup 3U							
	Linearity error							±1	LSB
	Differential linearity error							±1	LSB
	No missing codes						Pass		Pass/fail
3	Zero error, bipolar 2/	±10V range 3/		±20		*			mV
T_A = −55°C	Full scale error, −FS bipolar 2/	±10V range 3/		±40		*			mV
	Full scale error, +FS bipolar 2/	±10V range 3/		±40		*			mV
	Gain drift	5/		±54		*			mV
	Linearity error			±1		*			LSB
	Differential linearity error			±1		*			LSB
	No missing codes		Pass		*				Pass/fail
3U	Zero error, bipolar 2/	±10V range 3/						±30	mV
T_A = −25°C	Full scale error, −FS bipolar 2/	±10V range 3/						±50	mV
	Full scale error, +FS bipolar 2/	±10V range 3/						±50	mV
	Gain drift	6/						±33	mV
	Linearity error							±1	LSB
	Differential linearity error							±1	LSB
	No missing codes						Pass		Pass/fail
4									
T_A = +25°C	Conversion time			10		*		*	µsec
5									
T_A = +125°C	Conversion time			10		*		*	µsec
6									
T_A = −55°C	Conversion time			10		*		*	µsec
7	Quiescent Current	No load, all bits logic 1							
T_A = +25°C	$+V_{CC}$			45		*		*	mA
	$-V_{CC}$			45		*		*	mA
	V_{DD}			50		*		*	mA
	Power consumption	Quiescent		1500		*		*	mW
	Zero adjustment range	±10V range	±60		*		*		mV
	Gain adjustment range	±10V	±100		*		*		mV
	MSB inverted output		Pass		*		*		Pass/fail
	Serial output		Pass		*		*		Pass/fail

*Specifications the same as ADC87/883B.

NOTES:

1/ $\pm V_{CC}$ = 15VDC, V_{DD} = 5VDC, no load, without the optional buffer amplifier, unless otherwise specified. The internal clock is used. Clock Rate, pin 17, is connected to 0VDC. Short Cycle, pin 14, is connected to logic 1.

2/ Without external adjustment.

3/ For the ±10V range: bipolar +FS is ideally at +9.995117VDC; bipolar zero is ideally at 0.000VDC; bipolar −FS is ideally at −10.000VDC. For the 0 to +10V range: unipolar +FS is ideally at +9.997559VDC; unipolar zero is ideally at 0.000VDC. Refer to Figure 3 and Table V.

4/ Monotonicity is assured by differential linearity ≤ ±1LSB.

5/ The absolute value of the gain change from +25°C to +125°C is added to the absolute value of the gain change from +25°C to −55°C. This provides a 3-point drift.

6/ The absolute value of the gain change from +25°C to +85°C is added to the absolute value of the gain change from +25°C to −25°C. This provides a 3-point drift.

TABLE IV. Analog Input Range Selection Connections.

Input Range	DIRECT INPUT						BUFFERED INPUT				
	Input Signal to Pin	Input Impedance	Required External Pin Connections				Input Signal to Pin	Input Impedance	Required External Pin Connections		
±2.5V	24	2.5kΩ	30 to 26	29 open	23 to 22	22 to 25	30	50MΩ	29 to 24	23 to 22	22 to 25
±5V	24	5kΩ	30 to 26	29 open	23 to 22		30	50MΩ	29 to 24	23 to 22	
±10V	25	10kΩ	30 to 26	29 open	23 to 22		30	50MΩ	29 to 25	23 to 22	
0 to +5V	24	2.5kΩ	30 to 26	29 open	23 to 26	22 to 25	30	50MΩ	29 to 24	23 to 26	22 to 25
0 to +10V	24	5kΩ	30 to 26	29 open	23 to 26		30	50MΩ	29 to 24	23 to 26	

TABLE V. Ideal Analog Input Voltage vs Digital Output Code.

Input Range	DIGITAL OUTPUT CODE			1LSB
	MSB LSB 1111 1111 1111	MSB LSB 0111 1111 1111	MSB LSB 0000 0000 0000	
±2.5V	-2.500V	0V	+2.498779V	1.2207mV
±5V	-5.000V	0V	+4.997559V	2.4414mV
±10V	-10.000V	0V	+9.995117V	4.8828mV
0 to +5V	0V	+2.500V	+4.998779V	1.2207mV
0 to +10V	0V	+5.000V	+9.997559V	2.4414mV

NOTE:

Analog voltages are the center of the bit range. Transitions occur 1/2LSB before and 1/2LSB after the bit center.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, class B, except as modified herein.

4.2 Qualification. Qualification is not required unless specified by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. the qualification report is available from Burr-Brown.

4.3 Screening. Screening for the /883B Hi-Rel product designation is in accordance with MIL-STD-883, method 5008, class B, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition A, Y_1 axis only.
b. Interim and final electrical test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = 125°C$ minimum
   (4) Test duration is 160 hours minimum

d. Percent defective allowable (PDA). The PDA, for the /883B Hi-Rel product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

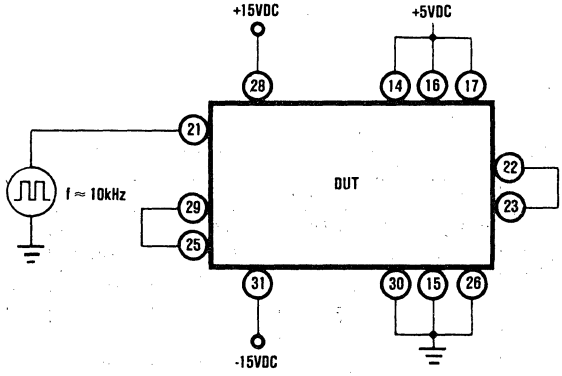


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, are performed as required by MIL-STD-883. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test conditions B
   (2) Test circuit is Figure 5 herein
   (3) T_A = 125°C minimum
   (4) Test duration is 1000 hours minimum

b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:
a. Complete part number (see paragraph 1.2).
b. Requirements for certificate of compliance, if desired.

6.4 Definitions.

Full Scale Absolute Accuracy Error. Full scale absolute accuracy error is the difference between the ideal and the actual, unadjusted, analog input voltage at the full scale points. It applies to unipolar plus full scale, bipolar minus full scale, and bipolar plus full scale. Absolute accuracy includes zero, gain, linearity, and noise errors and, when specified over temperature, includes the drifts of these errors. It is measured at the first or last transition, as appropriate. The error is expressed in LSBs or % of FSR.

Bipolar Zero Error. Bipolar zero error is the difference between the ideal and the actual analog input voltage for the digital output code 0111 1111 1111. It is measured at the 1000 0000 0000 to 0111 1111 1111 transition which ideally occurs at 0VDC -1/2LSB.

Bipolar zero error is also known as bipolar major transition error.

Unipolar Zero Error. Unipolar zero error is the difference between the ideal and the actual analog input voltage for the digital output code 1111 1111 1111 (unipolar). It is measured at the 1111 1111 1111 to 1111 1111 1110 transition which ideally occurs at 0VDC +1/2LSB.

Gain Error. Gain error is the difference between the ideal and the actual analog input voltage span. It applies to both unipolar and bipolar input ranges. It is measured between the first transition and the last transition which is ideally FSR -2LSB.

Gain error in some literature describes what is defined herein to be unipolar full scale error and bipolar plus full scale error.

Offset Error. This term is not used with the ADC87. Offset error in some literature describes what is defined herein to be unipolar zero error and/or bipolar minus full scale error.

Linearity Error. Linearity error is the difference between the ideal and the actual bit transition when zero error and gain error equal zero.

Differential Linearity Error. Differential linearity error is the difference between the ideal and the actual bit step width. Zero differential linearity error means each bit step width is 1LSB. A maximum differential linearity error of ±1/2LSB means a bit step width may be between 1/2LSB and 3/2LSB.

Monotonicity. Monotonicity is the condition where the digital output code remains the same or increases for an increasing analog input signal.

Quantization Uncertainty. Quantization uncertainty is the inherent uncertainty of being able to determine the analog voltage which produces a digital code. Because the analog input voltage is divided or quantized into a finite number of bits, each digital code represents an analog voltage span equal to 1LSB. Quantization uncertainty is ±1/2LSB. Its magnitude may be reduced only by using a higher resolution converter.

6.5 Microcircuit group assignment. These microcircuits are Technology Group I as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. APPLICATIONS INFORMATION

7.1 Layout. To produce clean, noise-free, accurate conversions, high frequency layout techniques should be used. Wide, low inductance conductor patterns, short and direct external component leads, power supply decoupling, and a ground plane are recommended. Long runs should be avoided. Coupling and runs, which might cause input-to-output coupling, should be avoided. High impedance points should be given special consideration. The input to the buffer, the comparator input (particularly sensitive) and the external adjustment pins are sensitive. Shielding by Analog Common or ±15VDC supply patterns my be helpful.

7.2 Grounding. A ground plane under the ADC87 is recommended.

Analog Common (pin 26) and Digital Common (pin 15) must be connected together and to the analog system ground. Preferably, connect both commons directly to the ground plane under the ADC87. If these commons must be run separately, use wide conductor patterns and connect a 0.01μF ceramic capacitor between the commons at the unit. The case is connected to Digital Common, pin 15.

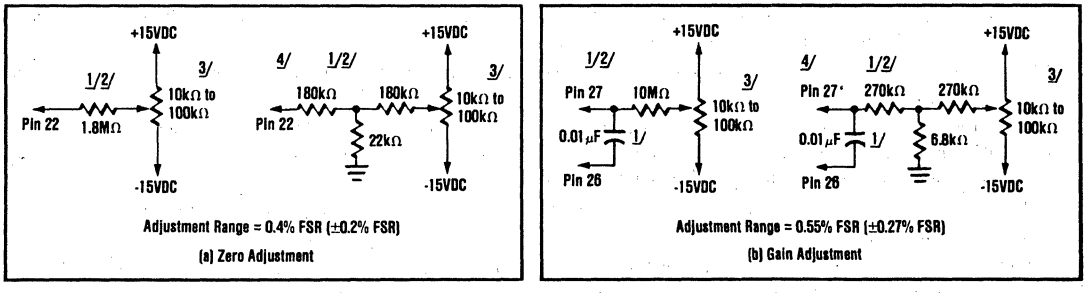
7.3 Power Supply Decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1μF tantalum capacitor and a 0.01μF ceramic capacitor from each power supply to the ground plane. Locate the capacitors close to the converter.

7.4 Optional External Zero and Gain Adjustments. The ADC87 zero error and gain error are factory laser-trimmed to position the staircase transfer function within Table I specifications. Optionally, two adjustments null zero error and gain error (see Figure 6).

Zero adjustment moves the entire staircase left-to-right. For unipolar ranges, -FS, 0VDC, is nulled. For bipolar ranges, midscale, 0VDC, is nulled. (Alternately, bipolar -FS may be nulled.)

Gain adjustment adjusts the span of the staircase. Adjustment effectively rotates the staircase about -FS. For unipolar and bipolar ranges, zero adjustment should be made first, then +FS error is nulled.

Adjustments should be made after a 10 minute warm-up. Fixed, selected resistors may be substituted for the potentiometers after the adjustments have been determined, if desired. If adjustments are not used, pin 22 (zero adjust) should only be connected as required for analog input range selection and pin 27 (gain adjust) should be either grounded (recommended) or open.



Notes:
1/ Locate as close as possible to the converter to minimize noise pickup.
2/ 5% carbon composition or better.
3/ Use multiturn potentiometers with 100ppm/°C TCR or less to minimize drift with temperature.
4/ An attentuator network may be substituted for the series resistor for lower impedance and lower noise susceptibility.

FIGURE 6. Optional External Zero and Gain Adjustment Circuits.

7.4.1 Zero Adjustment Procedure. For the selected unipolar range, apply the analog input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition ideally occurs, 0VDC +1/2LSB. While continuously converting, adjust the zero potentiometer until the transition "flickers".

For the selected bipolar range, apply the analog input voltage at which the 1000 0000 0000 to 0111 1111 1111 transition ideally occurs, 0VDC -1/2LSB. While continuously converting, adjust the zero potentiometer until the transition "flickers".

7.4.2 Gain Adjustment Procedure. Make zero adjustment first. For all input ranges, apply the analog input voltage at which the 0000 0000 0001 to 0000 0000 0000 transition ideally occurs, +FS -3/2LSB. While continuously converting, adjust the gain potentiometer until the transition "flickers". For bipolar ranges, repeat zero and gain adjustments as they are interactive.

7.5 Start Convert and Status. To start a conversion, a positive pulse with a minimum pulse width of 50nsec must be applied to the Start Convert terminal, pin 21. The trailing edge (falling edge) resets the converter, starts the internal clock and initiates a conversion. The start convert input must remain logic 0 during conversion, as the internal clock is stopped by logic 1 and the output will be erroneous. Another start convert pulse during a conversion does not reset and restart a conversion; it may momentarily stop the internal clock and produce an erroneous output.

Status output, pin 20, is logic 1 during conversion. When a conversion is complete, Status drops to logic 0 and the internal clock is turned off. Refer to the timing diagram, Figure 4.

7.6 Continuous Conversion. The ADC87 will continuously convert, commencing a new conversion immediately after the last conversion, when wired to accept an external clock. See paragraph 7.8 and Timing Considerations, paragraph 3.3.4. Alternately, the internal clock may be used with a new start convert common every 8.7μsec or slower.

7.7 Internal Clock and Clock Rate. The ADC87 is specified and tested using the internal clock. The internal clock is factory adjusted to 1.6MHz with Clock Rate, pin 17, connected to 0VDC (Digital Common). Under these conditions, the ADC87 will meet all the conversion speed and accuracy specifications.

The internal clock frequency may be increased or decreased by applying a positive or negative voltage to Clock Rate, pin 17 (see Figure 7). The circuits shown in Figure 8 may be used. Increasing the clock frequency decreases the conversion time; however, linearity errors increase as shown in Figures 9 and 10. Decreasing the clock frequency is accomplished by using a negative voltage or using an external clock (see paragraph 7.8).

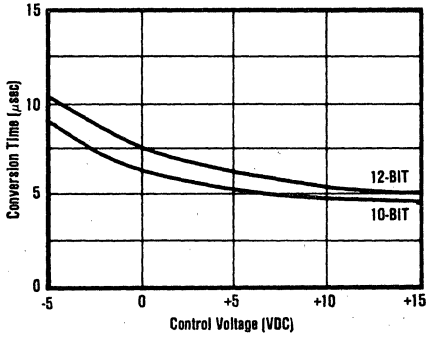
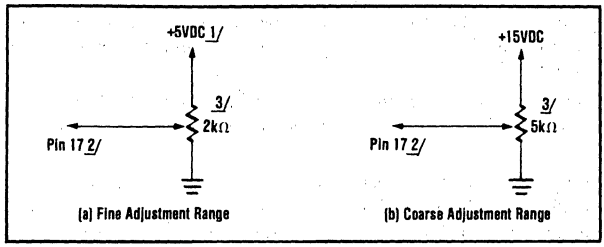


FIGURE 7. Clock Rate Control Voltage.



Notes:
1/ Use negative supply to decrease the clock frequency.
2/ Pin 17 is not connected to 0VDC when using clock rate adjustment potentiometer.
3/ Multiturn potentiometer with 100ppm/°C TCR or less.

FIGURE 8. Clock Rate Adjustment, Optional.

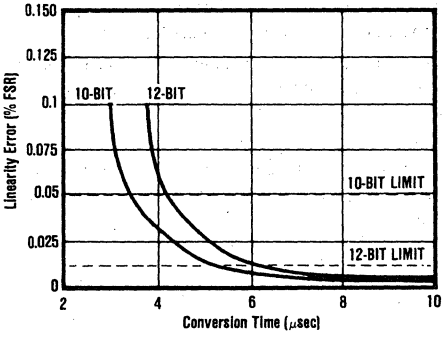


FIGURE 9. Linearity vs Conversion Time.

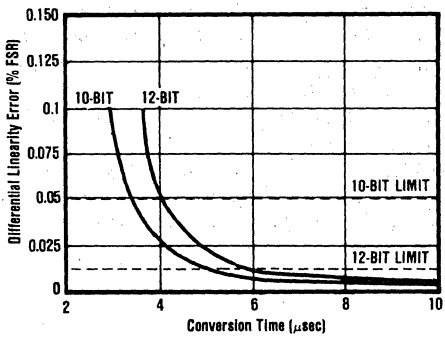


FIGURE 10. Differential Linearity vs Conversion Time.

7.8 External Clock. An external clock may be used with the ADC87 for synchronization or special timing applications. The external clock frequency must be lower than the internal clock frequency. However, the internal clock frequency may be increased; see paragraph 7.7.

The external clock is connected to the Start Convert terminal, pin 21. The normal, start convert positive pulse signal is not required. The external clock must be a negative-going pulse, 100nsec to 200nsec wide, at a frequency lower than the internal clock. The falling edge (leading edge) of the external clock starts the internal clock. The internal clock completes one cycle, then ceases as the Start Convert terminal, pin 21, is logic 1 at that time. The next external clock falling edge turns on the internal clock again, for one cycle. The Clock Output signal, pin 19, displays the internal clock synchronized to the lower, external clock frequency. A conversion is complete and Status output drops to logic 0 after 13 clock pulses.

The converter will provide continuous conversions as long as the external clock signal is present. A conversion is complete when Status output drops to logic 0. Status remains logic 0 for one external clock period. The next conversion starts on the next falling edge of the external clock following conversion completion. Conversions cease when Start Convert input is logic 1.

A circuit to generate an external clock signal from a clock with an arbitrary duty cycle is shown in Figure 11. A circuit to generate an external clock signal from a convert command is shown in Figure 12.

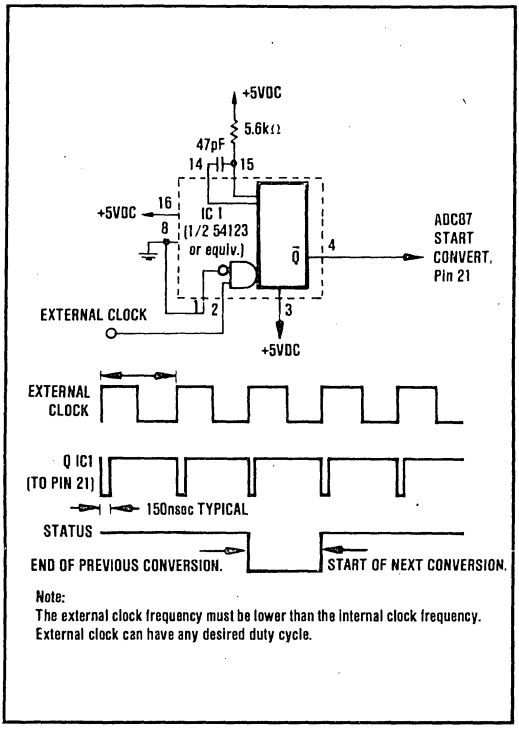


FIGURE 11. Continuous Conversion Using External Clock with Arbitrary Duty Cycle.

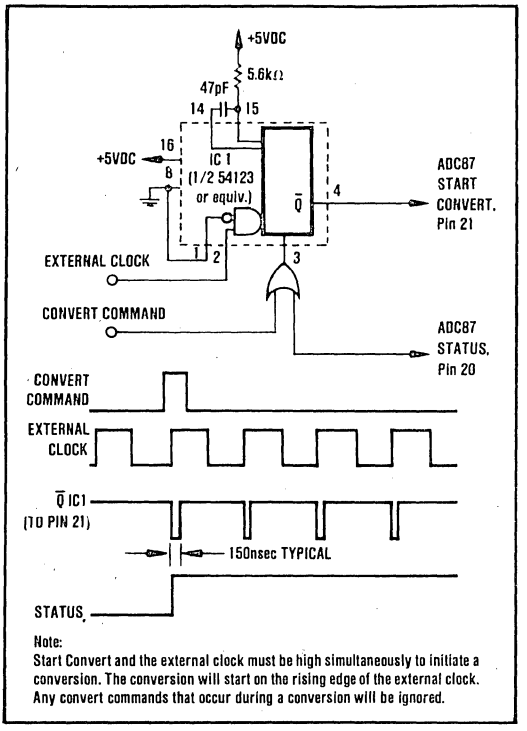


FIGURE 12. Conversion Initiated by Convert Command Using Continuous External Clock.

7.9 Short Cycle. The ADC87 conversion cycle may be stopped prior to converting all 12 bits. This provides faster conversions to less resolution. For conversions to n bits, connect the n + 1 bit output to Short Cycle, pin 14. The remaining bits are truncated.

Table VI shows a complete cycle and a short cycle to 10 bits. For 10 bits the internal clock frequency has been increased to provide the minimum conversion time. See Clock Rate, paragraph 7.7.

TABLE VI. Short Cycle Connections.

Resolution (bits)	12	10
Short Cycle connect pin 14 to pin	15	16
Short Cycle connect pin 14 to pin	16	2
Conversion Speed μsec, max	10	5

BURR-BROWN®

DAC87/883B SERIES

MODEL NUMBERS:
DAC87-CBI-V/B **DAC87U-CBI-V/B**
DAC87-CBI-V **DAC87U-CBI-V**

REVISION E
FEBRUARY, 1986

12-Bit -55°C to +125°C Military DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **HI-REL MANUFACTURE**
- **COMPLETELY SPECIFIED, -55°C to +125°C**
- **ACCURATE**
  - **±1/2LSB max Linearity, over temperature**
  - **±20ppm/°C max Gain Drift**
  - **±0.2% Total Error, over temperature**
  - **Monotonic, over temperature**
- **MIL-STD-883 SCREENING**
- **DAC85 PIN-COMPATIBLE**
- **COMPLETE - INTERNAL REFERENCE AND OUTPUT AMPLIFIER**

DESCRIPTION

The DAC87/883B Series is a high performance, 12-bit TTL-compatible, −55°C to +125°C digital-to-analog converter in a metal, welded, hermetically sealed package, and it is manufactured on a separate hi-rel production line. It is pin-compatible with DAC85 converters and has five user-selected output ranges. Each DAC is a complete device with an internal output amplifier and an ultra-stable reference.

The DAC87/883B Series is designed for high accuracy, wide temperature applications. The total accuracy without external trim adjustments is ±0.1% of FSR, decreasing to only ±0.3% of FSR over -55°C to +125°C. With external offset and gain trim adjustments at +25°C, the total accuracy is less than ±0.2% of FSR over -55°C to +125°C. Gain drift is less than 20ppm/°C. Linearity error, contributed mostly by the internal current switches and resistive ladder, is reduced by laser trimming to less than ±1/2LSB over temperature. Differential linearity is less than ±1LSB over temperature thereby guaranteeing monotonicity from -55°C to +125°C.

There are two electrical performance grades and three product assurance levels allowing a wide application/budget choice. The DAC87-CBI-V model/grade features excellent performance from -55°C to +125°C and finds wide military, aerospace, and industrial applications. The DAC87U-CBI-V model/grade features excellent performance from -25°C to +85°C, and guarantees specifications from -55°C to +125°C. Applications include test equipment, shipboard, ground support, and shirt-sleeve environments where operation is between -25°C and +85°C but full temperature operation must be assured.

Two product assurance levels are available: standard; and /B (100% screened, plus PDA = 10%, plus Groups A and B testing on each inspection lot, plus Groups C and D performed initially, periodically, and when specified on the customer's purchase order). See paragraph 1.2.2 for more details. Each device is manufactured in a hi-rel environment with clean room conditions which assures "built-in" quality.

1/ Current output models are also available. See DAC87-CBI-I Series Data Sheet.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
DIGITAL-TO-ANALOG CONVERTER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a 12-bit, TTL-compatible, integrated circuit, digital-to-analog converter.

1.2 Part Number. The complete part number is as shown below.

DAC87		—	CBI	—	V	/B
Basic model number	Grade (see 1.2.1)		Input coding (Complementary Binary)		Voltage output 1/	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, 12-bit, digital-to-analog converter. The input coding is complementary binary. The device may be externally pin-connected for either Complementary Straight Binary (CSB) or Complementary Offset Binary (COB) coding (see Tables V and VI).

There are two electrical performance grades. The premium grade has no grade designation in the part number and features specifications and tests from -55°C to +125°C. The U grade has a U grade designation in the part number and features specifications and tests from -25°C to +85°C, and specifications from -55°C to +125°C.

Electrical specifications are shown in Table I; electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:

Hi-Rel Product Designator	Requirements
/B	Standard model, plus 100% MIL-STD-883 Class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed initially and as required by MIL-STD-883.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is as defined in Figure 1. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage, V_{CC}	±18VDC
Supply voltage, V_{DD}	0VDC to +18VDC
Data input voltage	-1VDC to +7VDC
Output short circuit duration	Unlimited 2/
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60sec)	+300°C
Junction temperature	T_J = 175°C

1/ Current output models are also available. See DAC87-CBI-1 Series Data Sheet.
2/ Short circuit may be to ground only. Rating applies to 115°C case temperature or 65°C ambient temperature.

1.2.5 Recommended operating conditions.

Supply voltage range	V_{CC}: ±14.5VDC to ±15.5VDC V_{DD}: +4.75VDC to +5.25VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
24-lead can	Figure 1	1350mW at T_A = 125°C	7°C/W 1/	37°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microcircuits.

3. REQUIREMENTS

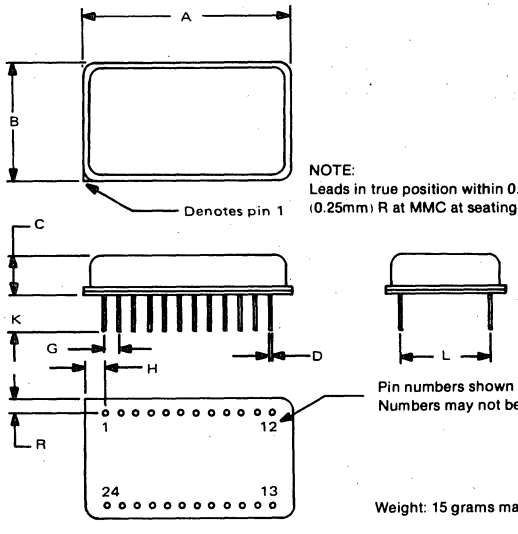
3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1. Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510 except organic and polymeric materials may be used for substrate and die attach. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

FIGURE 1. Case Outline (Double-Wide DIP Configuration).

1/ Rating applies to normal device operation. For the output short circuit condition, the maximum θJ-C of the output die of 100°C/W must be applied to the output short circuit current.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. All dice utilized are glassivated.

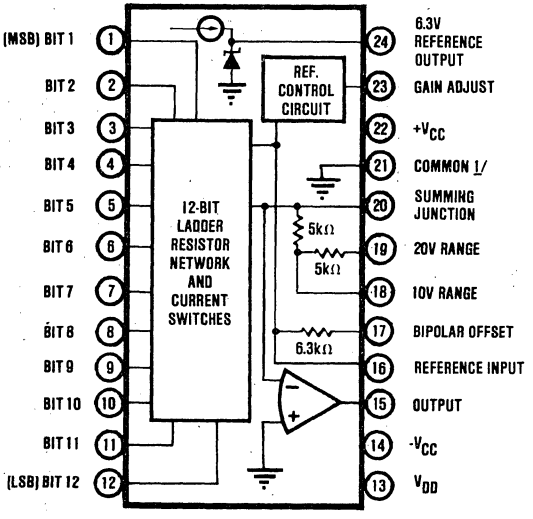
3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

3.3.1 Offset and gain error adjustment. The DAC is capable of being externally adjusted to zero offset error and to zero gain error using the circuits in Figure 3. See applications information, paragraph 7.3.

3.3.2 Input coding. The input coding is complementary binary. The digital input code to yield the corresponding output voltage for the output ranges is specified in Table V.

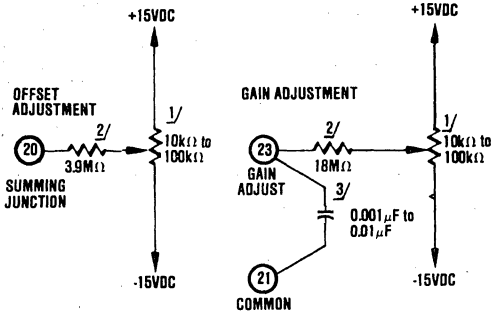
3.3.3 Output range. The output range is specified in Table VI when externally connected as shown therein.

3.4 Electrical test requirements. Electrical test requirements are specified in Table II. The subgroups of Table III and limits of Table IV which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, are specified in Table II.



1/ Pin 21 is connected to the case.

FIGURE 2. Terminal Connections.



1/ ≤100ppm/°C.
2/ ±20% carbon composition or better. Locate close to the DAC87 to prevent noise pickup.
3/ Ceramic.

FIGURE 3. Offset and Gain Error Adjustment Circuits.

TABLE I. Electrical Performance Characteristics.

CHARACTERISTICS	CONDITIONS 1/	LIMITS DAC87-CBI-V/B DAC87-CBI-V MIN	TYP	MAX	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MIN	TYP	MAX	UNITS 2/
RESOLUTION		12			12			Bits
DIGITAL INPUTS								
Input voltage								
Logic "1"	T_A = +25°C	2.0		5.5	*		*	V
	-55°C ≤ T_A ≤ +125°C	2.4		5.5	*		*	V
Logic "0"	T_A = +25°C	0		0.8	*		*	V
	-55°C ≤ T_A ≤ +125°C	0		0.4	*		*	V
Input Current								
Logic "1"	V_{IN} = 2.4V			+40			*	µA
Logic "0"	V_{IN} = 0.4V	-1.6		0	*		*	mA
ACCURACY								
Total error, untrimmed 3/	T_A = +25°C			±0.10			*	% of FSR
Unipolar	-25°C ≤ T_A ≤ +85°C						±0.25	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.30				% of FSR
Bipolar	T_A = +25°C			±0.10			*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.25	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.30				% of FSR
Total error, trimmed 3/ 4/								
Unipolar	T_A = +25°C		±0.006	±0.0122		*	*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.15	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.20				% of FSR
Bipolar	T_A = +25°C		±0.006	±0.0122		*	*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.15	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.20				% of FSR
Linearity error	T_A = +25°C		±0.25	±0.50		*	*	LSB
	-25°C ≤ T_A ≤ +85°C						±0.50	LSB
	-55°C ≤ T_A ≤ +125°C			±0.50			±3	LSB
Differential linearity error 5/	T_A = +25°C		±0.50	±0.75		*	*	LSB
	-25°C ≤ T_A ≤ +85°C						±1.0	LSB
	-55°C ≤ T_A ≤ +125°C			±1.0			±3	LSB
Monotonicity temperature range 5/		-55		+125	-25		+85	°C
Offset error 6/								
Unipolar 7/	T_A = +25°C		±0.02	±0.05		*	*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.068	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.08				% of FSR
Bipolar 7/	T_A = +25°C		±0.02	±0.05		*	*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.10	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.10				% of FSR
Offset temperature sensitivity 7/								
Unipolar	-25°C to +85°C					±1	±3	ppm of FSR/°C
	-55°C to +125°C		±1	±3				ppm of FSR/°C
Bipolar	-25°C to +85°C						±10	ppm of FSR/°C
	-55°C to +125°C		±5	±10			±30	ppm of FSR/°C
Offset adjustment range		±0.15	±0.2		*	*		% of FSR
Gain error 6/ 8/								
Unipolar 7/	T_A = +25°C		±0.05	±0.10		*	*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.20	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.25				% of FSR
Bipolar 7/	T_A = +25°C		±0.05	±0.10		*	*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.20	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.25				% of FSR
Gain temperature sensitivity 7/								
Unipolar	-25°C to +85°C					±10	±20	ppm/°C
	-55°C to +125°C		±10	±20				ppm/°C
Bipolar	-25°C to +85°C					±10	±20	ppm/°C
	-55°C to +125°C		±10	±20			±60	ppm/°C
Gain adjustment range		±0.2	±0.3		*	*		% of FSR
DYNAMIC CHARACTERISTICS								
Slew rate		10	20		*	*		V/µsec
Settling time	ΔV_O = 20V to ±1/2LSB		5	7		*	*	µsec
	ΔV_O = 10V to ±1/2LSB		3	6		*	*	µsec
	ΔV_O = 1LSB to ±1/2LSB		1.5	3		*	*	µsec
ANALOG OUTPUT								
Output voltage range 9/				±10			*	V
Output current 10/		±5			*			mA
Output resistance, DC			0.05	0.2		*	*	Ω
Output short circuit current	T_A = +25°C	±5		±40	*		*	mA

TABLE I. Electrical Performance Characteristics (cont).

CHARACTERISTICS	CONDITIONS 1/	LIMITS DAC87-CBI-V/B DAC87-CBI-V MIN	TYP	MAX	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MIN	TYP	MAX	UNITS 2/
INTERNAL REFERENCE								
Internal reference voltage (V_R)		±6.0	±6.3	±6.6	*	*	*	V
Internal reference temperature sensitivity	-25°C to +85°C					±5	±10	ppm of V_R/°C
	-55°C to +125°C		±5	±10			±30	ppm of V_R/°C
Output current from internal reference	for specified V_R			200			*	µA
POWER SUPPLY								
Power supply range								
+V_{CC}		+14.0	+15	+16.0	*	*	*	V
-V_{CC}		-14.0	-15	-16.0	*	*	*	V
V_{DD}		+4.75	+5	+15.5	*	*	*	V
Power supply sensitivity								
±V_{CC}	±V_{CC} = 15V ±0.5V		±0.002	±0.004		*	*	% of FSR/%V_{CC}
V_{DD}	V_{DD} = 5V ±0.25V		±0.001	±0.002		*	*	% of FSR/%V_{DD}
Power supply current (quiescent)								
±V_{CC}	T_A = +25°C		±20	±30		*	*	mA
	-55°C ≤ T_A ≤ +125°C			±30			*	mA
V_{DD}	T_A = +25°C		20	25		*	*	mA
	-55°C ≤ T_A ≤ +125°C			25			*	mA
TEMPERATURE RANGE								
Operating		-55		+125	*		*	°C
Storage		-65		+150	*		*	°C

*Specification same as DAC87-CBI-V

NOTES:

1/ ±V_{CC} = 15V, V_{DD} = 5V, -55°C ≤ T_A ≤ +125°C, unless otherwise specified.

2/ FSR = Full Scale Range (Example: The FSR is 20V for ±10V range, 10V for ±5V range, and 10V for 0 to +10V range.) LSB = Least Significant Bit.

3/ Total error includes all errors at any fixed power supply voltage within the recommended supply voltage range, including the internal reference, linearity error, offset error, and gain error.

4/ Offset and gain externally trimmed to zero error at T_A = +25°C.

5/ Monotonicity is assured by testing differential linearity to ±1LSB maximum.

6/ Externally adjustable to zero.

7/ The reference error is included.

8/ The offset error is specified separately and is not included herein.

9/ The output voltage range is determined by external conditions (see Table VI).

10/ Limit is assured by testing output resistance where R_{LOAD} = 2kΩ.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MIL-STD-883 test requirements (hybrid class) / MODELS	DAC87-CBI-V/B	DAC87-CBI-V	DAC87U-CBI-V/B	DAC87U-CBI-V
	Subgroups (see Table III)			
Interim electrical parameters (preburn-in)(method 5008)	1	1	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4	1, 2, 3	1, 2U, 3U	1, 2U, 3U
Group A test requirements (method 5008)	1, 2, 3, 4	—	1, 2U, 3U	1, 2U, 3U
Group C end point electrical parameters (method 5008)	Table IV	—	Table IV	—
Additional electrical subgroups performed prior to Group C inspections	2C, 3C, 5, 6	—	—	—

* PDA applies to subgroup 1 (see 4.3.d).

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Index point
b. Part number (see paragraph 1.2)
c. Inspection lot identification code 1/
d. Manufacturer's identification (BURR-BROWN®)
e. Manufactuer's designating symbol (CEBS)
f. Country of origin

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and trainings, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding, for the /B Hi-Rel product designation are in accordance with MIL-M-38510.

1/ A 4-digit date code, indicating year and week of seal, and a 4- or 5-digit lot identifier is marked on each unit.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening; for the /B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5008, Class B, except as modified in paragraph 4.3 herein.

Screening for the standard model, (none) Hi-Rel product designation, includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), temperature cycle, constant acceleration (condition D), and external visual inspection per MIL-STD—883, method 2009.

For the /B Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /B Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS DAC87-CBI-V/B DAC87-CBI-V MIN	LIMITS DAC87-CBI-V/B DAC87-CBI-V MAX	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MIN	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MAX	UNITS
1	Offset error, bipolar	4	±10V range (ideal value = -10.000V)		±10		±10	mV
T_A = +25°C	Gain error, bipolar	4	±10V range (ideal value = +9.995117V) 2/		±20		±20	mV
	Linearity error, bipolar	4	±10V range 3/ 4/					
			For + bit errors		+2.44		+2.44	mV
			For - bit errors		-2.44		-2.44	mV
	Differential linearity error, bipolar	4	±10V range 4/ 5/		±3.66		±3.66	mV
	Total error, untrimmed, bipolar	4			±20		±20	mV
	Total error, trimmed, bipolar	6/			--		--	
	Internal reference voltage	4		+6.0	+6.6	+6.0	+6.6	V
	Input voltage	—	Logic "1", all inputs, V_{in} = 5.0VDC to 2.0VDC, measure ΔV_o		±4		±4.8	mV
		—	Logic "0", all inputs, V_{in} = 0VDC to 0.8VDC, measure ΔV_o		±4		±4.8	mV
	Input current	—	Logic "1", each input, V_{in} = +2.4VDC		+40		+40	µA
		—	Logic "0", each input, V_{in} = +0.4VDC	-1.6	0	-1.6	0	mA
	Power supply current	4	No load $+V_{CC}$		30		30	mA
		4	No load $-V_{CC}$		30		30	mA
		4	No load V_{DD}		25		25	mA
	Output resistance	4	$R_O = \frac{(V_o \text{ no load}) - (V_o 2k\Omega \text{ load})}{5mA}$ *		0.2		0.2	Ω
	Output short circuit current	—	R_{load} = 11, V_o = +FS and -FS	±5	±40	±5	±40	mA
	Power supply sensitivity	4	±10V range, V_o = +FS, ΔV_{CC} = +0.5V and -0.5V		±2.6		±2.6	mV
			±10V range, V_o = +FS, ΔV_{DD} = +0.25V and -0.25V		±2.0		±2.0	mV
	Offset adjustment range	3	±10V range	±30		±30		mV
	Gain adjustment range	3	±10V range	±40		±40		mV
	Offset error, unipolar	4	0 to +10V range (ideal value = 0.00V)		±5		±5	mV
	Gain error, unipolar	4	0 to +10V range (ideal value = +9.997559V) 2/		±10		±10	mV
	Total error, untrimmed, unipolar	4	0 to +10V range		±10		±10	mV
2	Offset error, bipolar (V_{OE})	4	±10V range (ideal value = -10.000V)		±20			mV
T_A = +125°C	Gain error, bipolar (G_E)	4	±10V range (ideal value = +9.995117V) 2/		±50			mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE125} - V_{OE25}}{100°C}$		±0.20			mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E125} - G_{E25}}{100°C}$		±0.40			mV/°C
	Linearity error, bipolar	4	±10V range, 3/ 4/					
			For + bit errors		+2.44			mV
			For - bit errors		±2.44			mV
	Differential linearity error, bipolar	4	±10V range 4/ 5/		±4.88			mV
	Total error, untrimmed, bipolar	4	±10V range		±60			mV

*V_o = +full scale

TABLE III. Group A Inspection (cont).

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS DAC87-CBI-V/B DAC87-CBI-V MIN	LIMITS DAC87-CBI-V/B DAC87-CBI-V MAX	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MIN	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MAX	UNITS
	Total error, trimmed, bipolar	4	±10V range 7/		±40			mV
	Internal reference voltage	4		+6.0	+6.6			V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R125} - V_{R25}}{100°C}$		±63			µV/°C
2C T_A = +125°C	Power supply current	4	No load $+V_{CC}$		30			mA
		4	No load $-V_{CC}$		30			mA
		4	No load V_{DD}		25			mA
2U T_A = +85°C	Offset error, bipolar (V_{OE})	4	±10V range (ideal value = -10.000V)				±20	mV
	Gain error, bipolar (G_E)	4	±10V range (ideal value = +9.995117V) 2/				±40	mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE85} - V_{OE25}}{60°C}$				±0.20	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{GE}}{\Delta T} = \frac{G_{E85} - G_{E25}}{60°C}$				±0.40	mV/°C
	Linearity error, bipolar	4	±10V range, 3/ 4/					
			For + bit errors				+2.44	mV
			For - bit errors				-2.44	mV
	Differential linearity error, bipolar	4	±10V range 4/ 5/				±4.88	mV
	Total error, untrimmed, bipolar	4	±10V range				±50	mV
	Total error, trimmed, bipolar	4	±10V range 7/				±30	mV
	Internal reference voltage	4				+6.0	+6.6	V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R85} - V_{R25}}{60°C}$				±63	µV/°C
3 T_A = -55°C	Offset error, bipolar	4	±10V range (ideal value = -10.000V)		±20			mV
	Gain error, bipolar	4	±10V range (ideal value = +9.995117V) 2/		±50			mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-55}}{80°C}$		±0.20			mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-55}}{80°C}$		±0.40			mV/°C
	Linearity error, bipolar	4	±10V range 3/ 4/					
			For + bit errors		+2.44			mV
			For - bit errors		-2.44			mV
	Differential linearity error, bipolar	4	±10V range 4/ 5/		±4.88			mV
	Total error, untrimmed bipolar	4	±10V range		±60			mV
	Total error, trimmed bipolar	4	±10V range 7/		±40			mV
	Internal reference voltage	4		+6.0	+6.6			V
	Internal reference temperature sensitivity		$\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R-55}}{80°C}$		±63			µV/°C
3C T_A = -55°C	Power supply current	4	No load $+V_{CC}$		30			mA
		4	No load $-V_{CC}$		30			mA
		4	No load V_{DD}		25			mA
3U T_A = -25°C	Offset error, bipolar	4	±10V range (ideal value = -10.000V)				±20	mV
	Gain error, bipolar	4	±10V range (ideal value = +9.995117V) 2/				±40	mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-25}}{50°C}$				±0.20	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-25}}{50°C}$				±0.40	mV/°C
	Linearity error, bipolar	4	±10V range 3/ 4/					
			For + bit errors				+2.44	mV
			For - bit errors				-2.44	mV
	Differential linearity error, bipolar	4	±10V range 4/ 5/				±4.88	mV
	Total error, untrimmed bipolar	4	±10V range				±50	mV
	Total error, trimmed bipolar	4	±10V range 7/				±30	mV
	Internal reference voltage	4				+6.0	+6.6	V
	Internal reference temperature sensitivity		$\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R-25}}{50°C}$				±63	µV/°C

TABLE III. Group A Inspection (cont).

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS DAC87-CBI-V/B DAC87-CBI-V MIN	MAX	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MIN	MAX	UNITS
4 T_A = +25°C	Settling time Slew rate	5 5	To ±1/2LSB, ΔV_O = 20V ΔV_O = 20V, 10% to 90%	 10	7			µsec V/µsec
5 T_A = +125°C	Settling time Slew rate	5 5	To ±1/2LSB, ΔV_O = 20V ΔV_O = 20V, 10% to 90%	 10	7			µsec V/µsec
6 T_A = -55°C	Settling time Slew rate	5 5	To ±1/2LSB, ΔV_O = 20V V_O = 20V, 10% to 90%	 10	7			µsec V/µsec

NOTES:
1/ $\pm V_{CC}$ = 15VDC, V_{DD} = 5VDC, Logic 1 = 4V, Logic 0 = 0.2V, no load, unless otherwise specified.
2/ Offset error corrected to zero.
3/ The individual bit errors that are positive are switched on and compared to 1/2LSB. The individual bit errors that are negative are switched on and compared to 1/2LSB. This guarantees ±1/2LSB maximum linearity error.
4/ Offset error and gain error correction factors for the Device Under Test (DUT), if any, are applied to the DUT output voltage before comparing the DUT output voltage to the ideal output voltage. This is the basis for linearity error and differential linearity error relative to a straight line through the end points of the transfer function.
5/ Differential linearity error is tested at all combinations of the four most significant bits.
6/ Total error, trimmed, (bipolar) is the same as linearity error, bipolar.
7/ Offset and gain errors adjusted to zero at T_A = +25°C.

TABLE IV. Group C, End Point Electrical Parameters.
(T_A = +25°C, $\pm V_{CC}$ = 15VDC, V_{DD} = +5VDC)

Test	Limit	Delta
Total error, untrimmed, bipolar	±0.15% of FSR	±0.12% of FSR
Linearity error, bipolar	±1.0LSB	±0.75LSB
Differential linearity error, bipolar	+1.2LSB, -1.0LSB	±0.6LSB
Monotonicity	Yes	--
Offset error, bipolar	±0.125% of FSR	±0.10% of FSR
Gain error, bipolar	±0.25% of FSR	±0.25% of FSR

TABLE V. Ideal Output Voltage vs Digital Input Code.

Output Range	Digital Input Code (Complementary 12-Bit Binary) 1111 1111 1111	0111 1111 1111	0000 0000 0000
-2.5V to +2.5V	-2.500V	0	+2.498779V
-5V to +5V	-5.000V	0	+4.997559V
-10V to +10V	-10.000V	0	+9.995117V
0 to +5V	0	+2.500V	+4.998779V
0 to +10V	0	+5.000V	+9.997559V

NOTES:
1. One LSB = 1.2207mV for a 5-volt full scale range. One LSB = 2.4414mV for a 10-volt full scale range. One LSB = 4.8828mV for a 20-volt full scale range.
2. Digital input codes are shown with the MSB listed first.

TABLE VI. Output Range Selection.

Output Range	Required External Pin Connections			
-2.5V to +2.5V	15 to 18	17 to 20	19 to 20	16 to 24
-5V to +5V	15 to 18	17 to 20	19 NC	16 to 24
-10V to +10V	15 to 19	17 to 20	19 to 15	16 to 24
0 to +5V	15 to 18	17 to 21	19 to 20	16 to 24
0 to +10V	15 to 18	17 to 21	19 NC	16 to 24

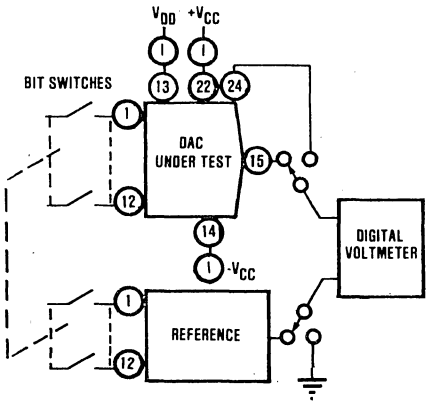


FIGURE 4. Test Circuit—Simplified.

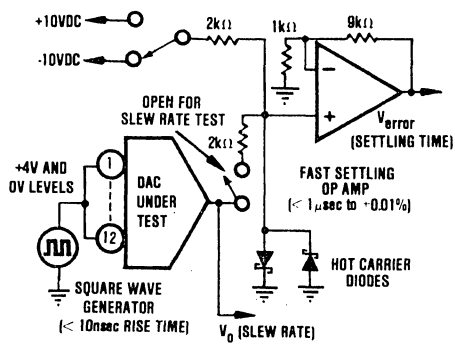


FIGURE 5. Slew Rate and Settling Time Test Circuit.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for the / B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5008, Class B, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition B, Y_1 axis only.
b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 6 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

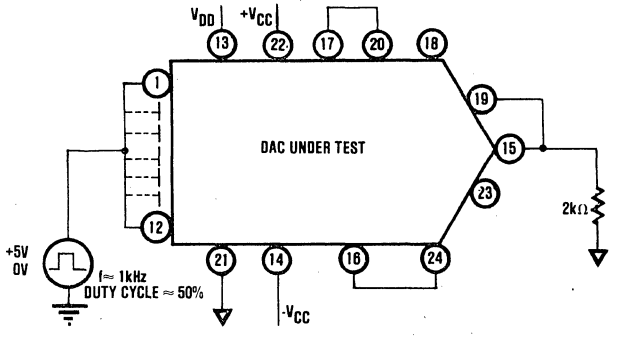


FIGURE 6. Test Circuit—Burn-in and Operating Life Test.

d. Percent defective allowable (PDA). The PDA, for / B Hi-Rel product designations only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test after

cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, are performed as required by MIL-STD-883.

A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 6 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

6.4 Definitions.

Offset error. Offset error is the difference between the ideal analog output voltage and the actual output voltage, when all the input bits are off (digital input code 1111 1111 1111).

Gain error. Gain error is the difference between the ideal analog output voltage span and the actual output voltage span, between when all the input bits are off (digital input code 1111 1111 1111) and when all the input bits are on (digital input code 0000 0000 0000).

Linearity error. Linearity error is the difference between the ideal analog output voltage and the actual output voltage, when the offset error and the gain error equal zero.

Differential linearity. Differential linearity is the difference between the ideal (1LSB) analog output voltage change, for 1-bit change in digital input code, and the actual output voltage change. A differential linearity of ±1LSB means that the output can change anywhere from 0LSB to 2LSB when the input changes from one adjacent input code to the next. Differential linearity of ±1LSB or less guarantees monotonicity.

Monotonicity. Monotonicity is the condition where the analog output increases or remains the same for an increase in input codes.

Unipolar output. Unipolar is an output characteristic that displays zero volts output at one input extreme and full scale volts output at the other input extreme.

Bipolar output. Bipolar is an output characteristic that displays full scale output voltage at one input extreme and the opposite full scale output voltage at the other input extreme.

6.5 Microcircuit group assignment. These microcircuits are in Technology Group F as defined in MIL-M-38510, Appendix I.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. APPLICATIONS INFORMATION

7.1 Power Supply Decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1μF tantalum capacitor from each power supply pin to the ground plane.

7.2 Power supply sensitivity. Power supply sensitivity is specified in Table I. Power supply sensitivity versus ripple frequency is shown in Figure 7.

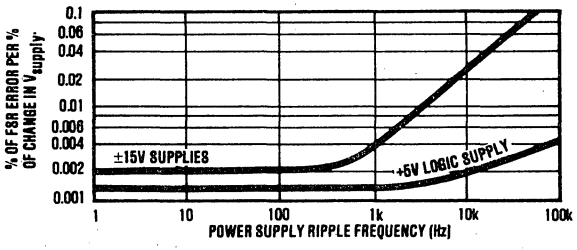


FIGURE 7. Typical Power Supply Sensitivity vs Power Supply Ripple.

7.3 External offset and gain error adjustment. The untrimmed accuracy of the DAC87/MIL Series is very good and is adequate for many applications. However, when the initial offset and gain errors are greater than what can be allowed in the application, the circuits shown in Figure 3 may be connected and the offset and gain errors adjusted to zero.

7.3.1 Offset adjustment. Apply the digital input code, 1111 1111 1111, which should produce zero volts output for the unipolar ranges, or minus full scale for the bipolar ranges. Adjust the offset potentiometer until the output, for the output range being used, is exactly as depicted in Table V.

7.3.2 Gain adjustment. Apply the digital input code, 0000 0000 0000, which should produce positive full scale. Adjust the gain potentiometer until the output, for the output range being used, is exactly as depicted in Table V.

BURR-BROWN®

DAC87-CBI-I SERIES

MODEL NUMBERS:

DAC87-CBI-I/B **DAC87U-CBI-I/B**
DAC87-CBI-I **DAC87U-CBI-I**

REVISION A
MAY, 1986

12-Bit −55°C to +125°C Military DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **HI-REL MANUFACTURE**
- **COMPLETELY SPECIFIED, −55°C to +125°C**
- **ACCURATE**
  - **±1/2LSB max Linearity, over temperature**
  - **±20ppm/°C max Gain Drift**
  - **±0.2% Total Error, over temperature**
  - **Monotonic, over temperature**
- **OPTIONAL MIL-STD-883 SCREENING**
- **DAC85 PIN-COMPATIBLE**
- **COMPLETE—INTERNAL REFERENCE**

DESCRIPTION

The DAC87-CBI-I Series is a high performance, 12-bit, TTL-compatible, current output, −55°C to +125°C digital-to-analog converter in a metal, welded, hermetically sealed package, and it is manufactured on a separate hi-rel production line. It is pin-compatible with DAC85 converters and has five user-selected output ranges. Each DAC is a complete device with an internal output amplifier and an ultra-stable reference.

The DAC87-I Series is designed for high accuracy, wide temperature applications. The total accuracy without external trim adjustments is ±0.1% of FSR, decreasing to only ±0.3% of FSR over −55°C to +125°C. With external offset and gain trim adjustments at +25°C, the total accuracy is less than ±0.2% of FSR over −55°C to +125°C. Gain drift is less than 20ppm/°C. Linearity error, contributed mostly by the internal current switches and resistive ladder, is reduced by laser trimming to less than ±1/2LSB over temperature. Differential linearity is less than ±1LSB over temperature thereby guaranteeing monotonicity from −55°C to +125°C.

There are two electrical performance grades and three product assurance levels allowing a wide application/budget choice. The DAC87-CBI-I model/grade features excellent performance from −55°C to +125°C and finds wide military, aerospace, and industrial applications. The DAC87U-CBI-I model/grade features excellent performance from −25°C to +85°C, and guarantees specifications from −55°C to +125°C. Applications include test equipment, shipboard, ground support, and shirt-sleeve environments where operation is between −25°C and +85°C but full temperature operation must be assured.

The two product assurance levels available are standard, and /B (100% screened per MIL-STD-883 method 5008, hybrid class, class B). See paragraph 1.2.2 for more details. Each device is manufactured in a hi-rel environment with clean room conditions which assures "built-in" quality.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION MICROCIRCUITS, LINEAR DIGITAL-TO-ANALOG CONVERTER HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a 12-bit, TTL-compatible, integrated circuit, current output, digital-to-analog converter.

1.2 Part Number. The complete part number is as shown below.

DAC87		CBI	I	B
Basic model number	Grade (see 1.2.1)	Input coding (Complementary Binary)	Current output	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, 12-bit, digital-to-analog converter. The input coding is complementary binary. The device may be externally pin-connected for either Complementary Straight Binary (CSB) or Complementary Offset Binary (COB) coding (see Tables IV and V).

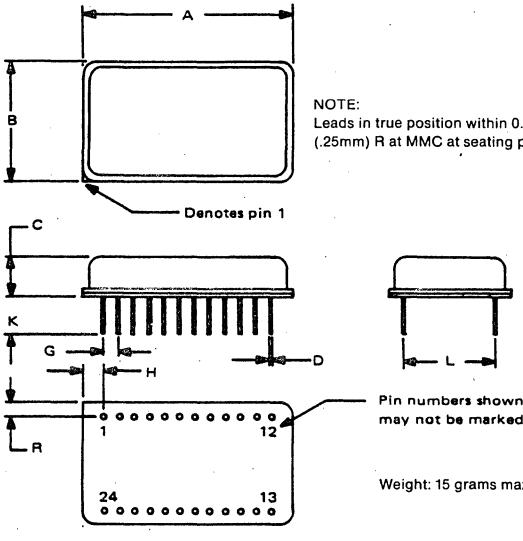
There are two electrical performance grades. The premium grade has no grade designation in the part number and features specifications and tests from −55°C to +125°C. The U grade has a U grade designation in the part number and features specifications and tests from −25°C to +85°C, and specifications from −55°C to +125°C.

Electrical specifications are shown in Table I; electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator position of the part number distinguishes the product assurance levels as follows:

Hi-Rel Product Designator	Requirements
/B	Standard model, plus 100% MIL-STD-883, method 5008, class B screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is as defined in Figure 1. The case is metal and is conductive.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

FIGURE 1. Case Outline (Double-Wide DIP Configuration).

1.2.4 Absolute maximum ratings.

Supply voltage, V_{CC}	±18VDC
Supply voltage, V_{DD}	0VDC to +18VDC
Data input voltage	−1VDC to +7VDC
Output short circuit duration	Unlimited 1/
Storage temperature range	−65°C to +150°C
Lead temperature (soldering, 60sec)	+300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	V_{CC}: ±14.5VDC to ±15.5VDC V_{DD}: +4.75VDC to +5.25VDC
Ambient temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
24-lead can	Figure 1	1350mW at T_A = 125°C	7°C/W 2/	37°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510 - Microcircuits, General Specification for.

STANDARD
MILITARY
MIL-STD-883 - Test Methods and Procedures for Microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510 except organic and polymeric materials may be used for substrate and die attach. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. All dice utilized are glassivated.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C, unless otherwise specified.

1/ Short circuit may be to ground only.

2/ Rating applies to normal device operation. For the output short circuit condition, the maximum θJ-C of the output die of 100°C/W must be applied to the output short circuit.

3.3.1 Offset and gain error adjustment. The DAC is capable of being externally adjusted to zero offset error and to zero gain error using the circuits in Figure 3. See applications information, paragraph 7.3.

3.3.2 Input coding. The input coding is complementary binary. The digital input code to yield the corresponding output current for the output ranges is specified in Table IV.

3.3.3 Output range. The output range is specified in Table V and Figures 4 and 5 when externally connected as shown therein.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

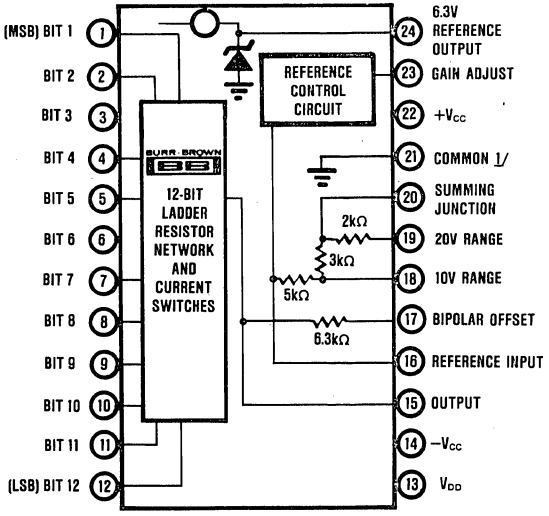
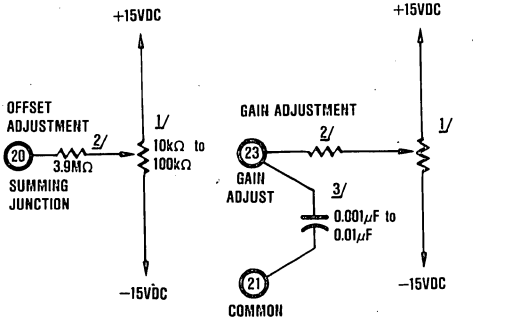


FIGURE 2. Terminal Connections.

1/ Pin 21 is connected to the case.



1/ ≤100ppm/°C.
2/ ±20% carbon composition or better. Locate close to the DAC87 to prevent noise pickup.
3/ Ceramic.

FIGURE 3. Offset and Gain Error Adjustment Circuits.

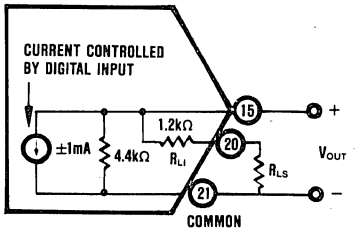


FIGURE 4. Alternate 1 Output Range Selection (Output Voltage with Resistive Load.)

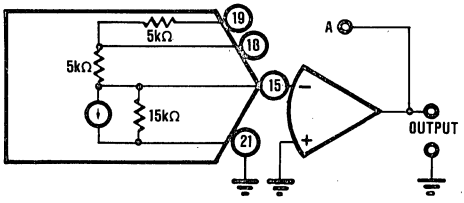


FIGURE 5. Alternate 2 Output Range Selection.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Index point
b. Part number (see paragrpah 1.2)
c. Inspection lot identification code 1/
d. Manufacturer's identification (BURR BROWN ®)
e. Manufacturer's designating symbol (CEBS)
f. Country of origin

1/ A 4-digit date code, indicating year and week of seal, and a 4- or 5-digit lot identifier is marked on each unit.

TABLE I. Electrical Performance Characteristics.

CHARACTERISTICS	CONDITIONS 1/	LIMITS						UNITS 2/
		DAC87-CBI-I/B DAC87-CBI-I			DAC87U-CBI-I/B DAC87U-CBI-I			
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION		12			12			Bits
DIGITAL INPUTS								
Input voltage								
Logic "1"	$T_A = +25°C$	2.0		5.5	•		•	V
	$-55°C \le T_A \le +125°C$	2.4		5.5	•		•	V
Logic "0"	$T_A = +25°C$	0		0.8	•		•	V
	$-55°C \le T_A \le +125°C$	0		0.4	•		•	V
Input Current								
Logic "1"	$V_{IN} = 2.4V$			+40			•	μA
Logic "0"	$V_{IN} = 0.4V$	−1.6		0	•		•	mA
ACCURACY								
Total error, untrimmed 3/	$T_A = +25°C$			±0.10			•	% of FSR
Unipolar	$-25°C \le T_A \le +85°C$						±0.25	% of FSR
	$-55°C \le T_A \le +125°C$			±0.30				% of FSR
Bipolar	$T_A = +25°C$			±0.10			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.25	% of FSR
	$-55°C \le T_A \le +125°C$			±0.30				% of FSR
Total error, trimmed 3/ 4/								
Unipolar	$T_A = +25°C$		±0.006	±0.0122		•	•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.20				% of FSR
Bipolar	$T_A = +25°C$		±0.006	±0.0122		•	•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.20				% of FSR
Linearity error	$T_A = +25°C$		±0.25	±0.50		•	•	LSB
	$-25°C \le T_A \le +85°C$						±0.50	LSB
	$-55°C \le T_A \le +125°C$			±0.50			±3	LSB
Differential linearity error 5/	$T_A = +25°C$		±0.50	±0.75		•	•	LSB
	$-25°C \le T_A \le +85°C$						±1.0	LSB
	$-55°C \le T_A \le +125°C$			±1.0			±3	LSB
Monotonicity temperature range 5/		−55		+125	−25		+85	°C
Offset error 6/								
Unipolar 7/	$T_A = +25°C$		±0.02	±0.05		•	•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.068	% of FSR
	$-55°C \le T_A \le +125°C$			±0.08				% of FSR
Bipolar 7/	$T_A = +25°C$		±0.02	±0.05		•	•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.10	% of FSR
	$-55°C \le T_A \le +125°C$			±0.10				% of FSR
Offset temperature sensitivity 7/								
Unipolar	−25°C to +85°C					±1	±3	ppm of FSR/°C
	−55°C to +125°C		±1	±3				ppm of FSR/°C
Bipolar	−25°C to +85°C						±10	ppm of FSR/°C
	−55°C to +125°C		±5	±10			±30	ppm of FSR/°C
Offset adjustment range		±0.15	±0.2		•	•		% of FSR
Gain error 6/ 8/								
Unipolar 7/	$T_A = +25°C$		±0.05	±0.10		•	•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.20	% of FSR
	$-55°C \le T_A \le +125°C$			±0.25				% of FSR
Bipolar 7/	$T_A = +25°C$		±0.05	±0.10		•	•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.20	% of FSR
	$-55°C \le T_A \le +125°C$			±0.25				% of FSR
Gain temperature sensitivity 7/								
Unipolar	−25°C to +85°C					±10	±20	ppm/°C
	−55°C to +125°C		±10	±20				ppm/°C
Bipolar	−25°C to +85°C					±10	±20	ppm/°C
	−55°C to +125°C		±10	±20			±60	ppm/°C
Gain adjustment range		±0.2	±0.3		•	•		% of FSR
DYNAMIC CHARACTERISTICS								
Settling time	ΔI_o = 2mA to ±1/2LSB, R_L = 250Ω		200	400		•	•	nsec

TABLE I. Electrical Performance Characteristics (cont).

CHARACTERISTICS	CONDITIONS 1/	LIMITS DAC87-CBI-I/B DAC87-CBI-I MIN	TYP	MAX	LIMITS DAC87U-CBI-I/B DAC87U-CBI-I MIN	TYP	MAX	UNITS 2/
ANALOG OUTPUT								
Output current range	9/	−2.1		−1.9	*		*	mA
Output compliance		±2.5			*			V
Output impedance								
Unipolar				15			*	kΩ
Bipolar				4.4			*	kΩ
INTERNAL REFERENCE								
Internal reference voltage V_R		±6.0	±6.3	±6.6	*	*	*	V
Internal reference temperature sensitivity	−25°C to +85°C					±5	±10	ppm of V_R/°C
	−55°C to −125°C		±5	±10			±30	ppm of V_R/°C
Output current from internal reference	for specified V_R			200			*	μA
POWER SUPPLY								
Power supply range								
$+V_{CC}$		+14.0	+15	+16.0	*	*	*	V
$-V_{CC}$		−14.0	−15	−16.0	*	*	*	V
V_{DD}		+4.75	+5	+15.5	*	*	*	V
Power supply sensitivity								
$\pm V_{CC}$	$\pm V_{CC}$ = 15V ±0.5V		±0.002	±0.004		*	*	mA
V_{DD}	V_{DD}= 5V ±0.25V		±0.001	±0.002		*	*	% of FSR/%V_{DD}
Power supply current (quiescent)								
$\pm V_{CC}$	T_A = +25°C		±20	±30		*	*	mA
	−55°C ≤ T_A ≤ +125°C			±30			*	mA
	T_A = −25°C		20	25		*	*	mA
V_{DD}	−55°C ≤ T_A ≤ +125°C			25			*	mA
TEMPERATURE RANGE								
Operating		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C

*Specification same as DAC87-CBI-I

NOTES:

1/ $\pm V_{CC}$ = 15V, V_{DD} = −55°C ≤ T_A ≤ −125°C, unless otherwise specified.

2/ FSR = Full Scale Range (Example: the FSR is 20V for ±10V range, 10V for ±5V range, and 10V for 0 to +10V range). LSB = Least Significant Bit.

3/ Total error includes all errors at any fixed power supply voltage within the recommended supply voltage range, including the internal reference, linearity error, offset error, and gain error.

4/ Offset and gain externally trimmed to zero error at T_A = +25°C.

5/ Monotonicity is assured by testing differential linearity to ±1LSB maximum.

6/ Externally adjustable to zero.

7/ The reference error is included.

8/ The offset error is specified separately and is not included herein.

9/ The output voltage range is determined by external conditions (see Table VI).

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III).

Models	DAC87-CBI-I/B DAC87-CBI-I	DAC87U-CBI-I/B DAC87U-CBI-I
MIL-STD-883 test requirements (hybrid class)	Subgroups (see Table III)	
Interim electrical parameters (preburn-in)(method 5008)	1	1
Final electrical test parameters (method 5008)	1*, 2, 3	1, 2, 2U, 3, 3U
Group A test requirements (method 5008) 1/	1, 2, 3	1, 2, 2U, 3, 3U
Group C end point electrical parameters (method 5008) 1/	1	1

*PDA applies to subgroup 1 (see 4.3.d)

1/ For /B designator only.

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS DAC87-CBI-I/B DAC87-CBI-I MIN	LIMITS DAC87-CBI-I/B DAC87-CBI-I MAX	LIMITS DAC87U-CBI-I/B DAC87U-CBI-I MIN	LIMITS DAC87U-CBI-I/B DAC87U-CBI-I MAX	UNITS
1	Offset error, bipolar	6	±10V range (ideal value = −10.000V)		±10		*	mV
T_A = +25°C	Gain error, bipolar	6	±10V range (ideal value = +9.995117V) 2/		±20		*	mV
	Linearity error, bipolar	6	±10V range 3/ 4/ For + bit errors		+2.44		*	mV
			For − bit errors		−2.44		*	mV
	Differential linearity error, bipolar	6	±10V range 4/ 5/		±3.66		*	mV
	Total error, untrimmed, bipolar	6			±20		*	mV
	Total error, trimmed, bipolar 6/				—		—	
	Internal reference voltage	6		+6.0	+6.6	*	*	V
	Input voltage	—	Logic "1", all inputs, V_{in} = 5.0VDC to 2.0VDC, measure ΔV_o		±4		±4.8	mV
		—	Logic "0", all inputs, V_{in} = 0VDC to 0.8VDC, measure ΔV_o		±4		±4.8	mV
	Input current	—	Logic "1", each input, V_{in} = +2.4VDC		+40		*	μA
		—	Logic "0", each input, V_{in} = +0.4VDC	−1.6	0	*	*	mA
	Power supply current	6	No load $+V_{CC}$		30		*	mA
		6	No load $-V_{CC}$		30		*	mA
		6	No load V_{DD}		25		*	mA
	Power supply sensitivity	6	±10V range, V_o = +FS, ΔV_{CC} = +0.5V and −0.5V		±2.6		*	mV
			±10V range, V_o = +FS, ΔV_{DD} = +0.25V and −0.25V		±2.0		*	mV
	Offset adjustment range	3	±10V range	±30		*		mV
	Gain adjustment range	3	±10V range	±40		*		mV
	Offset error, unipolar	6	0 to +10V range (ideal value = 0.00V)		±5		*	mV
	Gain error, unipolar	6	0 to +10V range (ideal value = +9.997559V) 2/		±10		*	mV
	Total error, untrimmed, unipolar	6	0 to +10V range		±10		*	mV
2	Offset error, bipolar (V_{OE})	6	±10V range (ideal value = −10.000V)		±20			mV
T_A = +125°C	Gain error, bipolar (G_E)	6	±10V range (ideal value = +9.995117V) 2/		±50			mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE125} - V_{OE25}}{100°C}$		±0.20		±0.60	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E125} - G_{E25}}{100°C}$		±0.40		±1.20	mV/°C
	Linearity error, bipolar	6	±10V range 3/ 4/ For + bit errors		+2.44		±14.64	mV
			For − bit errors		±2.44		±14.64	mV
	Differential linearity error, bipolar	6	±10V range 4/ 5/		±4.88		±14.64	mV
	Total error, untrimmed, bipolar	6	±10V range		±60			mV
	Total error, trimmed, bipolar	6	±10V range 7/		±40			mV
	Internal reference voltage	6		+6.0	+6.6	*	*	V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R125} - V_{R25}}{100°C}$		±63		±189	μV/°C
2U	Offset error, bipolar (V_{OE})	6	±10V range (ideal value = −10.000V)				±20	mV
T_A = +85°C	Gain error, bipolar (G_E)	6	±10V range (ideal value = +9.995117V) 2/				±40	mV
	Offset temperature sensitivity, bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE85} - V_{OE25}}{60°C}$				±0.20	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{GE}}{\Delta T} = \frac{G_{E85} - G_{E25}}{60°C}$				±0.40	mV/°C
	Linearity error, bipolar	6	±10V range 3/ 4/ For + bit errors				+2.44	mV
			For − bit errors				+2.44	mV
	Differential linearity error, bipolar	6	±10V range 4/ 5/				±4.88	mV
	Total error, untrimmed, bipolar	6	±10V range				±50	mV
	Total error, trimmed, bipolar	6	±10V range 7/				+30	mV
	Internal reference voltage	6				+6.0	+6.6	V
	Internal reference temperature sensitivity	—	±10V range, $\frac{\Delta V_R}{\Delta T} = \frac{V_{R85} - V_{R25}}{60°C}$				±63	μV/°C

TABLE III. Group A Inspection (cont).

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS DAC87-CBI-I/B DAC87-CBI-I MIN	LIMITS DAC87-CBI-I/B DAC87-CBI-I MAX	LIMITS DAC87U-CBI-I/B DAC87U-CBI-I MIN	LIMITS DAC87U-CBI-I/B DAC87U-CBI-I MAX	UNITS
3 $T_A = -55°C$	Offset error, bipolar	6	±10V range (ideal value = −10.000V)		±20			mV
	Gain error, bipolar	6	±10V range (ideal value = +9.995117V) 2/		±50			mV
	Offset temperature sensitivity, bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-55}}{80°C}$		±0.20		±0.60	mV/°C
	Gain temperature sensitivity, bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-55}}{80°C}$		±0.40		±1.20	mV/°C
	Linearity error, bipolar	6	±10V range 3/ 4/ For + bit errors For − bit errors		+2.44 −2.44		±14.64 ±14.64	mV mV
	Differential Linearity Error	6	±10V range4/5/		±4.88		±14.64	mV
	Total error, untrimmed bipolar	6	±10V range		±60			mV
	Total error, trimmed bipolar	6	±10V range 7/		±40			mV
	Internal reference voltage	6		+6.0	+6.6			V
	Internal reference temperature sensitivity	—	$\frac{V_R}{\Delta T} = \frac{V_{R25} - V_{R55}}{80°C}$		±63		±189	µV/°C
3U $T_A = -25°C$	Offset error, bipolar	6	±10V range (ideal value = −10.000V)		±20			mV
	Gain error, bipolar (G_E)	6	±10V range (ideal value = +9.995117V) 2/				±40	mV
	Offset temperature sensitivity, bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-25}}{50°C}$				±0.20	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-25}}{50°C}$				±0.40	mV/°C
	Linearity error, bipolar	6	±10V range 3/ 4/ For + bit errors For − bit errors				+2.44 −2.44	mV mV
	Differential linearity error, bipolar	6	±10V range 4/ 5/				±4.88	mV
	Total error, untrimmed, bipolar	6	±10V range				±50	mV
	Total error, trimmed, bipolar	6	±10V range 7/				+30	mV
	Internal reference voltage	6				+6.0	+6.6	V
	Internal reference temperature sensitivity	— —	±10V range, $\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R-25}}{50°C}$				±63	µV/°C

*Specification same as DAC87-CBI-I.

NOTES:

1/ $\pm V_{CC}$ = 15VDC, V_{DD} = 5VDC, Logic 1 = 4V, Logic 0 = 0.2V, no load, unless otherwise specified.

2/ Offset error corrected to zero.

3/ The individual bit errors that are positive are switched on and compared to 1/2LSB. The individual bit errors that are negative are switched on and compared to 1/2LSB. This guarantees ±1/2LSB maximum linearity error.

4/ Offset error and gain error correction factors for the Device Under Test (DUT), if any, are applied to the DUT output voltage before comparing the DUT output voltage to the ideal output voltage. This is the basis for linearity error and differential linearity error relative to a straight line through the end points of the transfer function.

5/ Differential linearity error is tested at all combinations of the four most significant bits.

6/ Total error, trimmed, (bipolar) is the same as linearity error, bipolar.

7/ Offset and gain errors adjusted to zero at T_A = +25°C.

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and trainings, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /B Hi-Rel product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

TABLE IV. Ideal Output Current vs Digital Input Code.

Output Range	Digital Input Code (Complementary 12-Bit Binary)		
	1111 1111 1111	0111 1111 1111	0000 0000 0000
0 to −2mA	0.0000mA	−1.0000mA	−1.9995mA
±1mA	+1.0000mA	0.0000mA	−0.9995mA

NOTES:
1/ One LSB = 0.488μA.
2/ Digital input codes are shown with the MSB listed first.

TABLE V. Output Range Selection.

Output Range	Required External Pin Connections				
0 to −2mA 1/	16 to 24	17 to 21	18 NC	19 NC	20 NC
+1mA to −1mA 1/	16 to 24	17 to 15	18 NC	19 NC	20 NC
Alternate 1 Output Range Selection 2/					
0 to −2V	16 to 24	17 to 21	105Ω 1/ between 18 and 21	19 to 18	20 to 15
+1V to −1V	16 to 24	17 to 15	18 to 15	19 to 18	90.9Ω 1/ between 20 and 21
Alternate 2 Output Range Selection 3/ 4/					
−2.5 V to +2.5V	16 to 24	17 to 15	18 to A	19 to 15	20 NC
−5V to +5V	16 to 24	17 to 15	18 to A	19 NC	20 NC
−10V to +10V	16 to 24	17 to 15	18 NC	19 to A	20 NC
0 to +5V	16 to 24	17 to 21	18 to A	19 to 15	20 NC
0 to +10V	16 to 24	17 to 21	18 to A	19 NC	20 NC

NOTES:
1/ ±5%.
2/ External 1% metal film resistor required.
3/ External operational amplifiers (Burr-Brown 3510VM/MIL or equivalent) required (see Figure 5).
4/ Burr-Brown DAC87-CBI-V/MIL provides these output range selections and contains an integral operational amplifier.

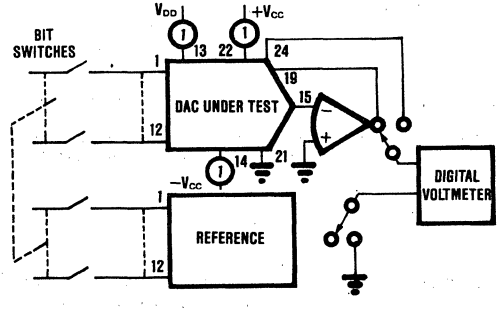


FIGURE 6. Test Circuit—Simplified.

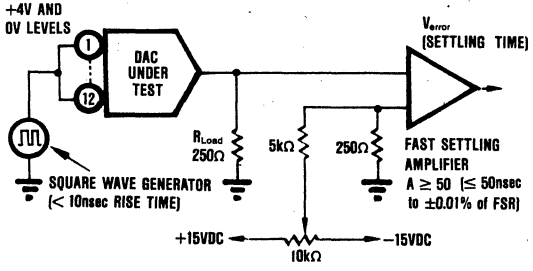


FIGURE 7. Settling Time Test Circuit.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening, for /B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model, (none) Hi-Rel product designation, includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), temperature cycle, constant acceleration (condition D), and external visual inspection per MIL-STD-883, method 2009.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

4.3 Screening. Screening for the /B Hi-Rel product designation is in accordance with MIL-STD-883, method 5008, class B, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883), method 2001) is test condition B, Y_1 axis only.
b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 8 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum
d. External visual inspection need not include measurement of case and lead dimensions.

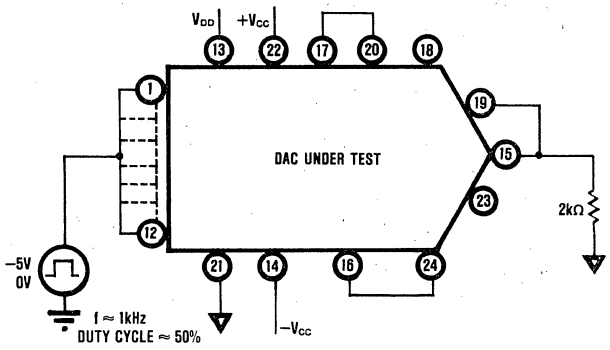


FIGURE 8. Test Circuit—Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, are performed per MIL-STD-883.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 8 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:
   a. Complete part number (see paragraph 1.2)
   b. Requirement for certificate of compliance, if desired.

6.4 Definitions.

Offset error. Offset error is the difference between the ideal analog output voltage and the actual output voltage, when all the input bits are off (digital input code 1111 1111 1111).

Gain error. Gain error is the difference between the ideal analog output voltage span and the actual output voltage span, between when all the input bits are off (digital input code 1111 1111 1111) and when all the input bits are on (digital input code 0000 0000 0000).

Linearity error. Linearity error is the difference between the ideal analog output voltage and the actual output voltage, when the offset error and the gain error equal zero.

Differential linearity. Differential linearity is the difference between the ideal (1LSB) analog output voltage change, for 1-bit change in digital input code, and the actual output voltage change. A differential linearity of ±1LSB means that the output can change anywhere from 0LSB to 2LSB when the input changes from one adjacent input code to the next. Differential linearity of ±1LSB or less guarantees monotonicity.

Monotonicity. Monotonicity is the condition where the analog output increases or remains the same for an increase in input codes.

Compliance. Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy.

Unipolar output. Unipolar is an output characteristics that displays zero current output at one input extreme and full scale current output at the other input extreme.

Bipolar output. Bipolar is an output characteristic that displays full scale output current at one input extreme and the opposite full scale output current at the other input extreme.

6.5 Microcircuit group assignment. These microcircuits are in Technology Group I as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. APPLICATIONS INFORMATION

7.1 Power Supply Decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1μF tantalum capacitor from each power supply pin to the ground plane.

7.2 Power supply sensitivity. Power supply sensitivity is specified in Table I. Power supply sensitivity versus ripple frequency is shown in Figure 9.

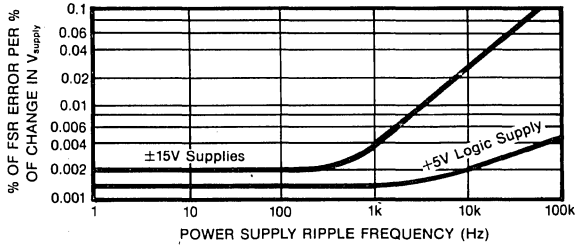


FIGURE 9. Typical Power Supply Sensitivity vs Power Supply Ripple.

7.3 External offset and gain error adjustment. The untrimmed accuracy of the DAC87 Series is very good and is adequate for many applications. However, when the initial offset and gain errors are greater than what can be allowed in the application, the circuits shown in Figure 3 may be connected and the offset and gain errors may be adjusted to zero.

7.3.1 Offset adjustment. Apply the digital input code, 1111 1111 1111, which should produce zero volts output for the unipolar ranges, or minus full scale for the bipolar ranges. Adjust the offset potentiometer until the output, for the output range being used, is exactly as depicted in Table IV.

7.3.2 Gain adjustment. Apply the digital input code, 0000 0000 0000, which should produce positive full scale. Adjust the gain potentiometer until the output, for the output range being used, is exactly as depicted in Table IV.

BURR-BROWN®

DAC870/883B SERIES

MODEL NUMBERS:

DAC870V/883B	DAC870U/883B
DAC870VL/883B	DAC870UL/883B
DAC870V	DAC870U
DAC870VL	DAC870UL

REVISION A
MAY, 1986

12-Bit −55°C to +125°C Military DIGITAL-TO-ANALOG CONVERTER

FEATURES

- HI-REL MANUFACTURE
- COMPLETELY SPECIFIED, −55°C to +125°C
- ACCURATE
  - ±1/2LSB max Linearity, over temperature
  - ±25ppm/°C max Gain Drift
  - ±0.3% Total Error, over temperature
  - Monotonic, over temperature
- MIL-STD-883 SCREENING
- DAC87 PIN-COMPATIBLE
- COMPLETE—INTERNAL REFERENCE AND OUTPUT AMPLIFIER

DESCRIPTION

The DAC870 Series is a high performance, 12-bit, TTL-compatible, −55°C to +125°C digital-to-analog converter in either a 24-pin ceramic side-brazed package or a 28-terminal leadless chip carrier, and it is manufactured on a separate Hi-Rel production line. It is pin-compatible with DAC87 converters and has five user-selected output ranges. Each DAC is a complete device with an internal output amplifier and an ultra-stable reference.

The DAC870 Series is designed for high accuracy, wide temperature applications. The total accuracy without external trim adjustments is ±0.25% of FSR, decreasing to only ±0.4% of FSR over −55°C to +125°C. With external offset and gain trim adjustments at +25°C, the total accuracy is less than ±0.3% of FSR over −55°C to +125°C. Gain drift is less than 25ppm/°C. Linearity error, contributed mostly by the internal current switches and resistive ladder, is reduced by laser trimming to less than ±1/2LSB over temperature. Differential linearity is less than ±1LSB over temperature, thereby guaranteeing monotonicity from −55°C to +125°C.

There are two electrical performance grades and two product assurance levels, allowing a wide application/budget choice. The DAC870V model/grade features excellent performance from −55°C to +125°C and finds wide military, aerospace, and industrial applications. The DAC870U model/grade features excellent performance from −25°C to +85°C, and guarantees specifications from −55°C to +125°C. Applications include test equipment, shipboard, ground support, and shirt-sleeve environments where operation is between −25°C and +85°C but full temperature operation must be assured.

The two product assurance levels available are: standard; and /883B (100% screened, plus PDA = 10%, plus Groups A and B testing on each inspection lot, plus Groups C and D performed as required by MIL-STD-883. See paragraph 1.2.2 for more details. Each device is manufactured in a Hi-Rel environment with clean room conditions which assures "built-in" quality.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
DIGITAL-TO-ANALOG CONVERTER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a 12-bit voltage output digital-to-analog converter hybrid microcircuit.

1.2 Part Number. The complete part number is as shown below.

DAC870	V	L	/883B
Basic model number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, 12-bit, voltage output digital-to-analog converter. The input coding is complementary binary. The device may be externally pin-connected for either Complementary Straight Binary (CSB) or Complementary Offset Binary (COB) coding (see Tables IV and V).

There are two electrical performance grades. The V grade designation is the premium grade and features specifications and tests from −55°C to +125°C. The U grade designation features specifications and tests from −25°C to +85°C and operation from −55°C to +125°C.

Electrical specifications are shown in Table I; electrical tests are shown in Tables II and III.

1.2.2 Device class. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels available as follows:

Hi-Rel product designator	Requirements
/883B	Standard model plus 100% MIL-STD-883 class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
(NONE)	Standard model including 100% electrical testing.

1.2.3 Case outline. Two case outlines are available.

1.2.3.1 24-pin ceramic side-brazed (DIP). No package identifier is utilized to specify the 24-pin ceramic side-brazed package, which is MIL-M-38510, Appendix C, designator D-3, configuration 3. Figure 1 depicts the case outline for this package type.

1.2.3.2 28-terminal leadless chip carrier (LCC). The "L" package identifier is utilized to specify the 28-terminal square leadless chip carrier package, which is MIL-M-38510, Appendix C, designator C-4. Figure 1 depicts the case outline for this configuration.

1.2.4 Absolute maximum ratings.

Supply voltage, V_{CC}	±20VDC
Supply voltage, V_{DD}	0VDC to +18VDC
Data input voltage	−1VDC to +7VDC
Output short circuit duration	Continuous to ground
Storage temperature range	−65°C to +165°C
Lead temperature (soldering, 10sec)	+300°C
Junction temperature	T_J = +165°C

1.2.5 Recommended operating conditions.

Supply voltage range	V_{CC}: ±14.5VDC to ±15.5VDC V_{DD}: ±4.75VDC to +5.25VDC
Ambient temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C
24-lead DIP	Figure 1	850mW	48°C/W
28-terminal LCC	Figure 1	950mW	42°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510 - Microcircuits, General Specification for.

STANDARD
MILITARY
MIL-STD-883 - Test Methods and Procedures for Microcircuits.

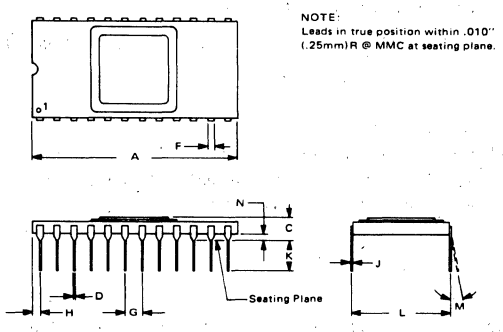
3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

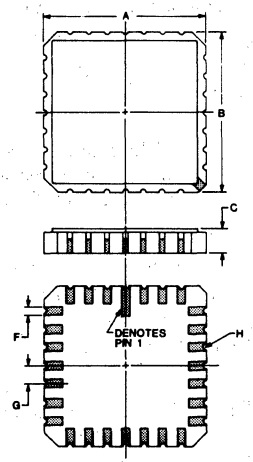
3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	— —	10°	— —	10°
N	.025	.060	0.64	1.52

(a) 24-pin side braze; package ID: (none)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.442	.458	11.23	11.63
B	.442	.458	11.23	11.63
C	.064	.100	1.63	2.54
F	.022	.028	0.56	0.71
G	.050 BASIC		1.27 BASIC	
H	.008R TYP.		0.20R TYP.	

(b) 28-terminal LCC; package ID: "L"

FIGURE 1. Case Outlines.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections for the ceramic side-brazed package are shown in Figure 2 and the circuit diagram and terminal connections for the leadless chip carrier package are shown in Figure 3.

3.2.8 Glassivation. The microcircuit dice are glassivated.

3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

3.3.1 Offset and gain error adjustment. The DAC is capable of being externally adjusted to zero offset error and to zero gain error using the circuits in Figure 4. See applications information paragraph 7.3.

3.3.2 Input coding. The input coding is complementary binary. The digital input code to yield the corresponding output voltage for the various output ranges is specified in Table IV.

3.3.3 Output range. The output range is specified in Table VI when externally connected as shown therein.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

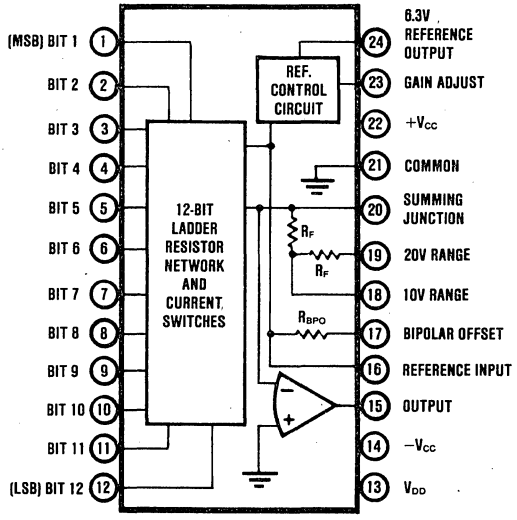


FIGURE 2. Terminal Connections (24-pin Ceramic Side Braze).

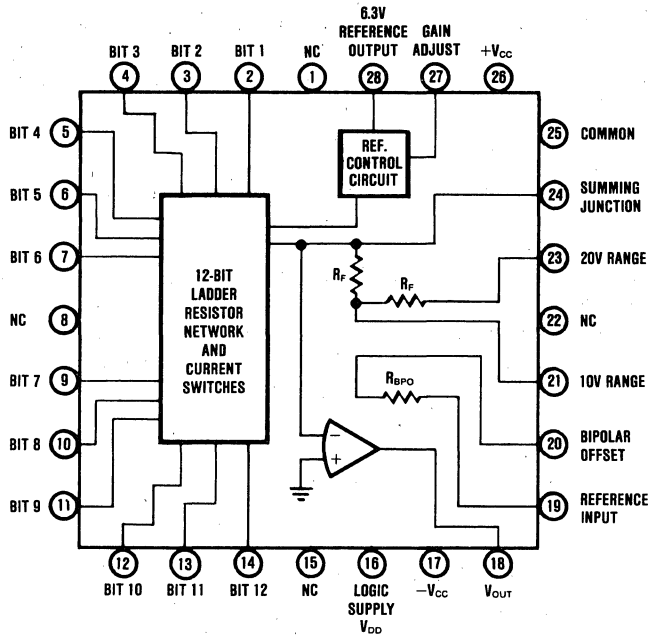
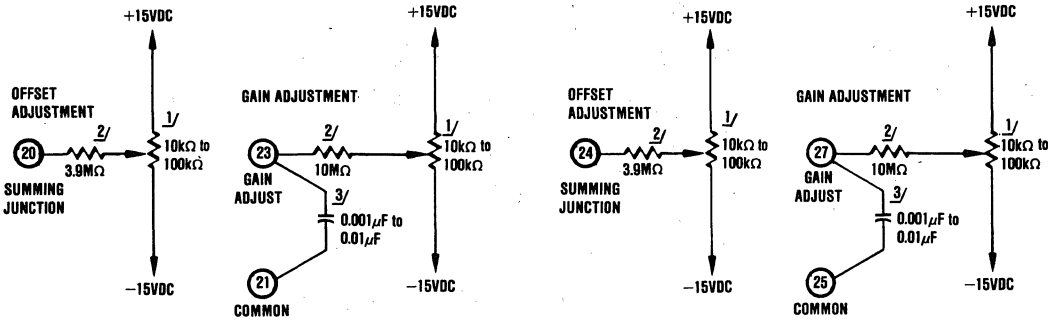


FIGURE 3. Terminal Connections (28-terminal LCC).



(a) 24-PIN CERAMIC SIDE-BRAZED PACKAGE

(b) 28-TERMINAL LCC

1/ ≤100ppm/°C.
2/ ±20% carbon composition or better. Locate close to the DAC870 to prevent noise pickup.
3/ Ceramic.

FIGURE 4. Offset and Gain Error Adjustment Circuits.

TABLE I. Electrical Performance Characteristics.

CHARACTERISTICS	CONDITIONS [1]	LIMITS DAC870V/883B DAC870V MIN	DAC870VL/883B DAC870VL TYP	DAC870VL/883B DAC870VL MAX	DAC870U/883B DAC870U MIN	DAC870UL/883B DAC870UL TYP	DAC870UL/883B DAC870UL MAX	UNITS [2]
RESOLUTION		12			12			Bits
DIGITAL INPUTS								
Input voltage: Logic "1"	$T_A = +25°C$	2.0		5.5	•		•	V
	$-55°C \le T_A \le +125°C$	2.4		5.5	•		•	V
Logic "0"	$T_A = +25°C$	0		0.8	•		•	V
	$-55°C \le T_A \le +125°C$	0		0.4	•		•	V
Input Current: Logic "1"	$V_{IN} = 2.4V$			+40			•	μA
Logic "0"	$V_{IN} = 0.4V$	−1.6		0	•		•	mA
ACCURACY								
Total error, untrimmed [3]: Unipolar	$T_A = +25°C$			±0.25			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.25	% of FSR
	$-55°C \le T_A \le +125°C$			±0.40				% of FSR
Bipolar	$T_A = +25°C$			±0.25			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.25	% of FSR
	$-55°C \le T_A \le +125°C$			±0.40				% of FSR
Total error, trimmed [3,4]: Unipolar	$T_A = +25°C$		±0.006	±0.0122		•	•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.30				% of FSR
Bipolar	$T_A = +25°C$		±0.006	±0.0122		•	•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.30				% of FSR
Linearity error	$T_A = +25°C$		±0.25	±0.50		•	•	LSB
	$-25°C \le T_A \le +85°C$						±0.50	LSB
	$-55°C \le T_A \le +125°C$			±0.50			±3	LSB
Differential linearity error [5]	$T_A = +25°C$		±0.50	±0.75		•	•	LSB
	$-25°C \le T_A \le +85°C$						±1.0	LSB
	$-55°C \le T_A \le +125°C$			±1.0			±3	LSB
Monotonicity temperature range [5]		−55		+125	−25		+85	°C
Offset error [6]: Unipolar [7]	$T_A = +25°C$			±0.10			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.118	% of FSR
	$-55°C \le T_A \le +125°C$			±0.15				% of FSR
Bipolar [7]	$T_A = +25°C$			±0.10			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.15				% of FSR
Offset temperature sensitivity [7]: Unipolar	−25°C to +85°C						±3	ppm of FSR/°C
	−55°C to +125°C			±3				ppm of FSR/°C
Bipolar	−25°C to +85°C						±15	ppm of FSR/°C
	−55°C to +125°C			±15			±45	ppm of FSR/°C
Gain error [6,8]: Unipolar [7]	$T_A = +25°C$			±0.15			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.20	% of FSR
	$-55°C \le T_A \le +125°C$			±0.25				% of FSR
Bipolar [7]	$T_A = +25°C$			±0.15			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.20	% of FSR
	$-55°C \le T_A \le +125°C$			±0.25				% of FSR
Gain temperature sensitivity [7]: Unipolar	−25°C to +85°C						±20	ppm/°C
	−55°C to +125°C			±25				ppm/°C
Bipolar	−25°C to +85°C						±20	ppm/°C
	−55°C to +125°C			±25			±75	ppm/°C
Gain adjustment range		0.15			•			% of FSR
DYNAMIC CHARACTERISTICS								
Slew rate		10			•			V/μsec
Settling time	ΔV_O = 20V to ±1/2LSB		5	7		•	•	μsec
	ΔV_O = 10V to ±1/2LSB		3	6		•	•	μsec
	ΔV_O = 1LSB to ±1/2LSB		1.5	3		•	•	μsec
ANALOG OUTPUT								
Output voltage range [9]				±10			•	V
Output current [10]		±5			•			mA
Output resistance, DC			0.05	0.2		•	•	Ω
Output short circuit current	$T_A = +25°C$	±5		±40	•		•	mA

TABLE I. Electrical Performance Characteristics (cont).

CHARACTERISTICS	CONDITIONS 1/	LIMITS						UNITS 2/
		DAC870V/883B DAC870V	DAC870VL/883B DAC870VL		DAC870U/883B DAC870U	DAC870UL/883B DAC870UL		
		MIN	TYP	MAX	MIN	TYP	MAX	
INTERNAL REFERENCE								
Internal reference voltage (V_R)		±6.23	±6.3	±6.37	*	*	*	V
Internal reference temperature sensitivity	−25°C to +85°C						±20	ppm of V_R/°C
	−55°C to +125°C			±25				ppm of V_R/°C
Output current from internal reference	for specified V_R	1.5			*			mA
POWER SUPPLY								
Power supply range: $+V_{CC}$		+13.5	+15	+16.5	*	*	*	V
$-V_{CC}$		−13.5	−15	−16.5	*	*	*	V
V_{DD}		+4.5	+5	+16.5	*	*	*	V
Power supply sensitivity: $\pm V_{CC}$	$\pm V_{CC}$ = 15V ±0.5V		±0.002	±0.004		*	*	% of FSR/%V_{CC}
V_{DD}	V_{DD} = 5V ±0.25V		±0.001	±0.002		*	*	% of FSR/%V_{DD}
Power supply current (quiescent): $+V_{CC}$	−55°C ≤ T_A ≤ +125°C			+12			*	mA
$-V_{CC}$				−25			*	mA
V_{DD} 11/				+10			*	mA
TEMPERATURE RANGE								
Operating		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C

* Specification same as DAC870V.

NOTES:

1/ $\pm V_{CC}$ = 15V, V_{DD} = 5V, −55°C ≤ T_A ≤ +125°C, unless otherwise specified.

2/ FSR = Full Scale Range (Example: The FSR is 20V for ±10V range, 10V for ±5V range, and 10V for 0 to +10V range.) LSB = Least Significant Bit.

3/ Total error includes all errors at any fixed power supply voltage within the recommended supply voltage range, including the internal reference, linearity error, offset error, and gain error.

4/ Offset and gain externally trimmed to zero error at T_A = +25°C.

5/ Monotonicity is assured by testing differential linearity to ±1LSB maximum.

6/ Externally adjustable to zero.

7/ The reference error is included.

8/ The offset error is specified separately and is not included herein.

9/ The output voltage range is determined by external conditions (see Table VI).

10/ Limit is assured by testing output resistance where R_{LOAD} = 2kΩ.

11/ Power dissipation is an additional 100mW, when V_{DD} is operated at +15V.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

Models / MIL-STD-883 test requirements [hybrid class]	DAC870V/883B DAC870VL/883B DAC870V DAC870VL	DAC870U/883B DAC870UL/883B DAC870U DAC870UL
	Subgroups (see Table III)	
Interim electrical parameters (preburn-in) (method 5008)	1	1
Final electrical test parameters (method 5008)	1*, 2, 3,	1, 2, 2U, 3, 3U
Group A test requirements (method 5008) 1/	1, 2, 3, 4	1, 2, 2U, 3, 3U
Group C end point electrical parameters (method 5008) 1/	—	1
Additional electrical subgroups performed prior to Group C inspections	—	—

*PDA applies to subgroup 1 (see 4.3.d)

1/Applies to /883B models only.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum:

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /883B Hi-Rel product designation, are in accordance with MIL-M-38510.

1/ A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

3.7 Traceability. Traceability for the /883B product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for the /883B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), constant acceleration (condition E), temperature cycle (condition C), and external visual per MIL-STD-883, method 2009.

For the /883B Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection for the /883B Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS [1]	LIMITS DAC870 "V" Grade MIN	LIMITS DAC870 "V" Grade MAX	LIMITS DAC870 "U" Grade MIN	LIMITS DAC870 "U" Grade MAX	UNITS
1	Offset error, bipolar	5	±10V range (ideal value = −10.000V)		±20		*	mV
T_A = +25°C	Gain error, bipolar	5	±10V range (ideal value = +9.995117V) [2]		±30		*	mV
	Linearity error, bipolar	5	±10V range [3] [5]					
			For + bit errors		+2.44		*	mV
			For − bit errors		−2.44		*	mV
	Differential linearity error, bipolar	5	±10V range [4] [5]		±3.66		*	mV
	Total error, untrimmed, bipolar	5			±50		*	mV
	Total error, trimmed, bipolar				—		—	
	Internal reference voltage	5		+6.23	+6.37	*	*	V
	Input voltage [6]	—	Logic "1", all inputs, V_{in} = 5.0VDC to 2.0VDC, measure ΔV_O		±4.0		±4.0	mV
		—	Logic "0", all inputs, V_{in} = 0VDC to 0.8VDC, measure ΔV_O		±4.0		±4.0	mV
	Input current	—	Logic "1", each input, V_{in} = +2.4VDC		+40		*	µA
		—	Logic "0", each input, V_{in} = +0.4VDC	−1.6	0	*	*	mA
	Power supply current	5	No load $+V_{CC}$		12		*	mA
		5	No load $-V_{CC}$		25		*	mA
		5	No load V_{DD}		10		*	mA
	Output resistance	5	$R_o = \frac{(V_O \text{ no load}) - (V_O \text{ 2k}\Omega \text{ load})}{5\text{mA}}$		0.2		*	Ω
	Output short circuit current	—	R_{load} = 1Ω, V_O = +FS and −FS	±5	±40	*	*	mA
	Power supply sensitivity	5	±10V range, V_O = +FS, ΔV_{CC} = +0.5V and −0.5V		±2.6		*	mV
			±10V range, V_O = +FS, ΔV_{DD} = +0.25V and −0.25V		±2.0		*	mV
	Gain adjustment range	4	±10V range	±30		*		mV
	Offset error, unipolar	5	0 to +10V range (ideal value = 0.00V)		±10		*	mV
	Gain error, unipolar	5	0 to +10V range (ideal value = +9.997559V) [2]		±15		*	mV
	Total error, untrimmed, unipolar	5	0 to +10V range		±25		*	mV
2	Offset error, bipolar (V_{OE})	5	±10V range (ideal value =−10.000V)		±30			mV
T_A = +125°C	Gain error, bipolar (G_E)	5	±10V range (ideal value = +9.995117V) [2]		±50			mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE125} - V_{OE25}}{100°C}$		±0.30		±9.0	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E125} - G_{E25}}{100°C}$		±0.50		±1.50	mV/°C
	Linearity error, bipolar	5	±10V range, [3] [4]					
			For + bit errors		+2.44		+14.64	mV
			For − bit errors		−2.44		−14.64	mV
	Differential linearity error, bipolar	5	±10V range [4] [5]		±4.88		±14.64	mV
	Total error, untrimmed, bipolar	5	±10V range		±80			mV
	Total error, trimmed, bipolar	5	±10V range [7]		±60			mV
	Internal reference voltage	5		+6.23	+6.37			V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R125} - V_{R25}}{100°C}$		±157			µV/°C

TABLE III. Group A Inspection (cont).

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS [1]	LIMITS DAC870 "V" Grade MIN	LIMITS DAC870 "V" Grade MAX	LIMITS DAC870 "U" Grade MIN	LIMITS DAC870 "U" Grade MAX	UNITS
2U	Offset error, bipolar (V_{OE})	5	±10V range (ideal value = −10.000V)				±30	mV
T_A = +85°C	Gain error, bipolar (G_E)	5	±10V range (ideal value = +9.995117V) [2]				±40	mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE85} - V_{OE25}}{60°C}$				±0.15	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta VG_E}{\Delta T} = \frac{G_{E85} - G_{E25}}{60°C}$				±0.40	mV/°C
	Linearity error, bipolar	5	±10V range, [3] [4]					
			For + bit errors				+2.44	mV
			For − bit errors				−2.44	mV
	Differential linearity error, bipolar	5	±10V range [4] [5]				±4.88	mV
	Total error, untrimmed, bipolar	5	±10V range				±50	mV
	Total error, trimmed, bipolar	5	±10V range [7]				±30	mV
	Internal reference voltage	5				+6.23	+6.37	V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R85} - V_{R25}}{60°C}$				±126	µV/°C
3	Offset error, bipolar	5	±10V range (ideal value = −10.000V)		±30			mV
T_A = −55°C	Gain error, bipolar	5	±10V range (ideal value = +9.995117V) [2]		±50			mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-55}}{80°C}$		±0.30		±.90	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-55}}{80°C}$		±0.50		±1.50	mV/°C
	Linearity error, bipolar	5	±10V range, [3] [4]					
			For + bit errors		+2.44		+14.64	mV
			For − bit errors		−2.44		−14.64	mV
	Differential linearity error, bipolar	5	±10V range [4] [5]		±4.88		±14.64	mV
	Total error, untrimmed, bipolar	5	±10V range		±80			mV
	Total error, trimmed, bipolar	5	±10V range [7]		±60			mV
	Internal reference voltage	5		+6.23	+6.37			V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R-55}}{80°C}$		±157			µV/°C
3U	Offset error, bipolar	5	±10V range (ideal value = −10.000V)				±30	mV
T_A = −55°C	Gain error, bipolar	5	±10V range (ideal value = +9.995117V) [2]				±40	mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-25}}{50°C}$				±0.30	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-25}}{50°C}$				±0.40	mV/°C
	Linearity error, bipolar	5	±10V range, [3] [4]					
			For + bit errors				+2.44	mV
			For − bit errors				−2.44	mV
	Differential linearity error, bipolar	5	±10V range [4] [5]				±4.88	mV
	Total error, untrimmed, bipolar	5	±10V range				±50	mV
	Total error, trimmed, bipolar	5	±10V range [7]				±30	mV
	Internal reference voltage	5				+6.23	+6.37	V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R-25}}{50°C}$				±126	µV/°C
4	Settling Time	6	T_O ±1/2LSB, ΔV_O = 20V		7			µsec
T_A = +25°C	Slew Rate	6	ΔV_O = 20V, 10% to 90%	10		*		V/µsec

NOTES:
1/ $\pm V_{CC}$ = 15VDC, V_{DD} = 5VDC, Logic 1 = 4V, Logic 0 = 0.2V, no load, unless otherwise specified.
2/ Offset error corrected to zero.
3/ The individual bit errors that are positive are switched on and compared to 1/2LSB. The individual bit errors that are negative are switched on and compared to 1/2LSB. This guarantees ±1/2LSB maximum linearity error.
4/ Offset error and gain error correction factors for the Device Under Test (DUT), if any, are applied to the DUT output voltage before comparing the DUT output voltage to the ideal output voltage. This is the basis for linearity error and differential linearity error relative to a straight line through the end points of the transfer function.
5/ Differential linearity error is tested at all combinations of the four most significant bits.
6/ Total error, trimmed, (bipolar) is the same as linearity error, bipolar.
7/ Offset and gain errors adjusted to zero at T_A = +25°C.

TABLE IV. Ideal Output Voltage vs Digital Input Code.

	Digital Input Code [Complementary 12-Bit Binary]		
Output Range	1111 1111 1111	0111 1111 1111	0000 0000 0000
−2.5V to +2.5V	−2.500V	0	+2.498779V
−5V to +5V	−5.000V	0	+4.997559V
−10V to +10V	−10.000V	0	+9.995117V
0 to +5V	0	+2.500V	+4.998779V
0 to +10V	0	+5.000V	+9.997559V

NOTES:
1. One LSB = 1.2207mV for a 5-volt full scale range. One LSB = 2.4414mV for a 10-volt full scale range. One LSB = 4.8828mV for a 20-volt full scale range.
2. Digital input codes are shown with the MSB listed first.

TABLE V. OutpUt Range Selection.

24-pin Side Braze Package				
Output Range	Required External Pin Connections			
−2.5V to +2.5V	15 to 18	17 to 20	19 to 20	16 to 24
−5V to +5V	15 to 18	17 to 20	19 NC	16 to 24
−10V to +10V	15 to 19	17 to 20	19 to 15	16 to 24
0 to +5V	15 to 18	17 to 21	19 to 20	16 to 24
0 to +10V	15 to 18	17 to 21	19 NC	16 to 24
28-Terminal LCC Package				
Output Range	Required External Pin Connections			
−2.5V to +2.5V	18 to 21	20 to 24	23 to 24	19 to 28
−5V to +5V	18 to 21	20 to 24	23 NC	19 to 28
−10V to +10V	18 to 23	20 to 24	23 to 18	19 to 28
0 to +5V	18 to 21	20 to 25	23 to 24	19 to 28
0 to +10V	18 to 21	20 to 25	23 NC	19 to 28

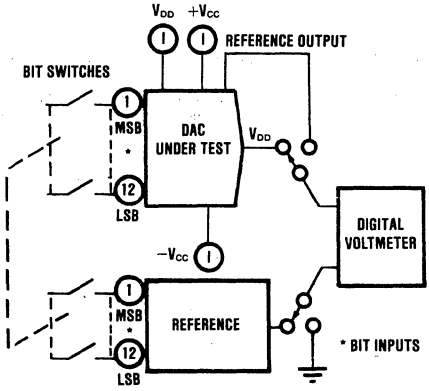


FIGURE 5. Test Circuit—Simplified.

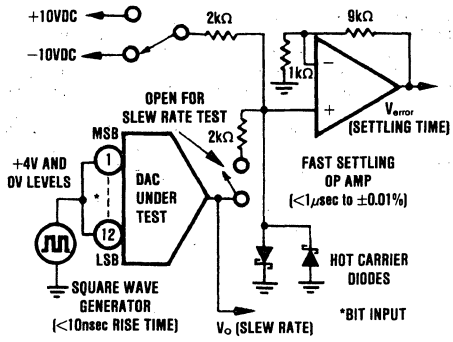


FIGURE 6. Slew Rate and Settling Time Test Circuit.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening, the /883B Hi-Rel product designation, is in accordance with MIL-STD-883B, method 5008, class B, and is conducted on all devices. The following additional criteria apply:

a. Interim and final test parameters are specified in Table II.

b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 7 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

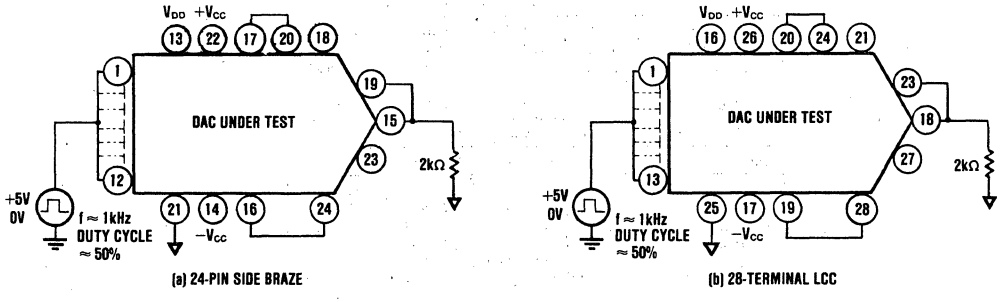


FIGURE 7. Test Circuit-Burn-in and Operating Life Test.

c. Percent defective allowable (PDA). The PDA, for /883B Hi-Rel product designation only, is 10 percent and parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in are used to determine the percent defective for each manufacturing lot, and the lot is accepted or rejected based on the PDA.

d. External visual inspection need not include measurement of case and lead dimensions.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, are performed as required by MIL-STD-883. unless specified by contract or purchase order.

A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 and as follows:

a. End point electrical parameters are specified in Table II herein.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is required or desirable.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

6.4 Definitions.

Offset error. Offset error is the difference between the ideal analog output voltage and the actual output voltage, when all the input bits are off (digital input code: 1111 1111 1111).

Gain error. Gain error is the difference between the ideal analog output voltage span and the output voltage span, between when all the input bits are off (digital input code: 1111 1111 1111) and when all the input bits are on (digital input code: 0000 0000 0000).

Linearity error. Linearity error is the difference between the ideal analog output voltage and the actual output voltage, when the offset error and the gain error are equal to zero.

Differential linearity. Differential linearity is the difference between the ideal (1LSB) analog output voltage change, for a 1-bit change in digital input code and the actual output voltage change. A differential linearity of ±1LSB means that the output can change anywhere from 0LSB to 2LSB when the input changes from one adjacent input code to the next. Differential linearity of ±1LSB or less guarantees monotonicity.

Monotonicity. Monotonicity is the condition where the analog output increases or remains the same for a 1LSB increase in input codes.

Unipolar output. Unipolar is an output characteristic that displays zero volts output at one input extreme and full scale volts output at the other extreme.

Bipolar output. Bipolar is an output characteristic that displays full scale output voltage at one input extreme and the opposite full scale output voltage at the other input extreme.

6.5 Microcircuit group assignment. These microcircuits are assigned to Technology Group I as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. CAUTION—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

7. APPLICATION INFORMATION

7.1 Power Supply Decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1μF tantalum or electrolytic capacitor from each power supply pin to the ground plane. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

7.2 Power Supply Sensitivity. Power supply sensitivity is specified in Table I. Power supply sensitivity versus ripple frequency is shown in Figure 8.

7.3 External offset and gain error adjustment. The untrimmed accuracy of the DAC870 series is very good and is adequate for many applications. However, when the initial offset and gain errors are greater than what can be allowed in the application, the circuits shown in Figure 4 can be utilized to adjust the offset and gain errors to zero.

7.3.1 Offset adjustment. Apply the digital input code, 1111 1111 1111, which should produce zero volts output for the unipolar ranges, or minus full scale for the bipolar ranges. Adjust the offset potentiometer until the output, for the output range employed, is exactly the value indicated in Table IV.

7.3.2 Gain adjustment. Apply the digital input code, 0000 0000 0000, which should produce positive full scale. Adjust the gain potentiometer until the output is exactly as depicted in Table IV for the output range being utilized.

7.4 Reference supply. All models of the DAC870 are supplied with an internal 6.3V reference voltage supply. This voltage has a tolerance of ±1% and must be connected to the Reference Input for specified operation. This reference may be used externally also. The external current drain is limited to sourcing 2.5mA up to +85°C and 1mA up to +125°C exclusive of the current required by the bipolar offset circuit. An external buffer amplifier is recommended if this reference will be used to drive other system components, because variations in a load driven from the reference will result in bipolar offset variations of the DAC870 converter. Gain and bipolar offset adjustments should be made under constant load conditions. It should be noted that because of the design of the DAC870 an external reference voltage cannot be used with the DAC870.

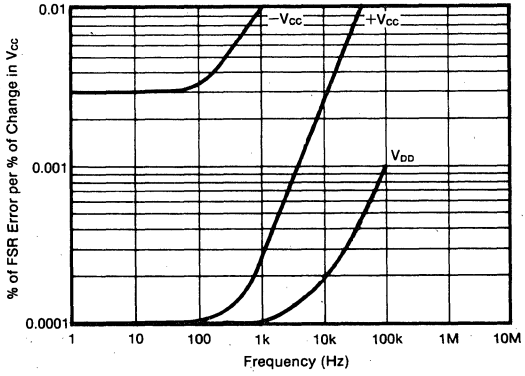


FIGURE 8. Power Supply Sensitivity vs Power Supply Ripple.

BURR-BROWN®

INA258/883B SERIES

MODEL NUMBERS:

INA258WG/883B	INA258VG/883B	INA258UG/883B
INA258WL/883B	INA258VL/883B	INA258UL/883B
INA258WG	INA258VG	INA258UG
INA258WL	INA258VL	INA258UL

REVISION A
MAY, 1986

Very-High Accuracy Military INSTRUMENTATION AMPLIFIER

FEATURES

- VERSATILE FOUR-OP AMP DESIGN
- ULTRA-LOW VOLTAGE DRIFT, 0.5μV/°C
- LOW OFFSET VOLTAGE, 50μV
- LOW NONLINEARITY, 0.005%
- LOW NOISE, 13nV/$\sqrt{\text{Hz}}$ at f_o = 1kHz
- HIGH CMR, 106dB at 60Hz
- HIGH INPUT IMPEDANCE, $10^{10}\Omega$

APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gauges
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS

DESCRIPTION

The INA258 is a high accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very high performance is desired.

A multiamplifier, monolithic design, which uses Burr-Brown's ultra-low drift, low noise technology, provides the highest performance with maximum versatility at the lowest cost. This makes the INA258 ideal for even high volume applications.

Burr-Brown's compatible thin film resistors and state-of-the-art wafer level laser trimming techniques are used for minimizing offset voltage and temperature drift. This advanced technique also maximizes common mode rejection and gain accuracy.

The INA258 also contains a fourth operational amplifier, specified separately, which can conveniently be used for some important applications, such as single-capacitor active low-pass filtering and easy output level shifting.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
INSTRUMENTATION AMPLIFIER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a very high accuracy instrumentation amplifier. For description of operation see paragraph 8.

1.2 Part number. The complete part number is as shown below.

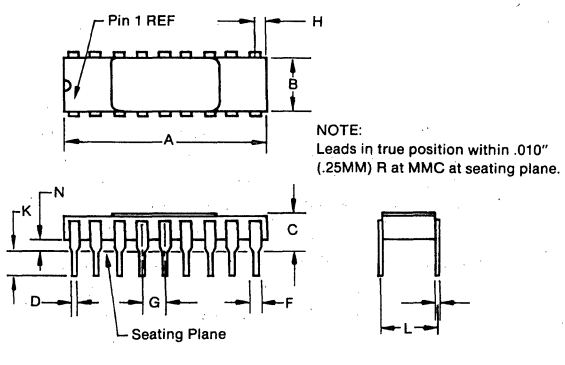
INA258	W	G	/883B
Basic model number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single instrumentation amplifier. Three electrical performance grades (W, V, and U) are provided. The electrical performance characteristics are shown in Table I.

1.2.2 Device class. The device class is similar to the class B product assurance level as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels available as follows:

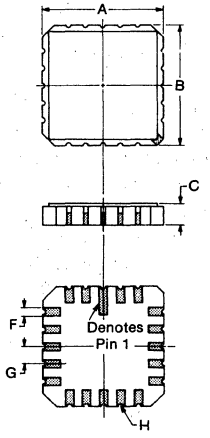
Hi-Rel Product Designator	Requirements
/883B	Standard model plus 100% MIL-STD-883 class B screening, with 5% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. Two case outlines are available. The case outline for the "G" package is D-6, configuration 3 (18-lead ceramic side braze), and the outline for the "L" package is C-2 (20-terminal square leadless chip carrier) as defined in MIL-M-38510 Appendix C. Figure 1 depicts the case outlines for both package types.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	.960	—	24.38
B	.220	.310	5.59	7.87
C	—	.200	—	5.08
D	.014	.023	.36	.58
F	.030	.070	.76	1.78
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.015	.20	.38
K	.125	.200	3.18	5.08
L	.290	.320	7.37	8.13
N	.015	.060	.38	1.52

(a) 18-pin side braze; package ID: "G"



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.342	.358	8.69	9.09
B	.342	.358	8.69	9.09
C	.064	.100	1.63	2.54
F	.022	.028	0.56	0.71
G	.050 BASIC		1.27 BASIC	
A	.008R TYP.		0.20 TYP.	

(b) 20-terminal leadless chip carrier ID: "L"

FIGURE 1. Case Outlines.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	$\pm V_{CC}$
Internal power dissipation	600mW
Storage temperature range	−65°C to +165°C
Output short circuit duration	Continuous to ground
Lead temperature (soldering, 10 sec.)	+300°C

1.2.5 Recommended operating conditions.

Supply voltage range	±5VDC to ±20VDC
Ambient temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case Outline	Maximum allowable power dissipation	Maximum θ_{JC}
18-lead DIP	Figure 1	600mW	41°C/W
20-terminal LCC	Figure 1	600mW	40°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510—Microcircuits, General Specification for.

STANDARD
MILITARY
MIL-STD-883—Test Methods and Procedures for Microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections for the "G" package are shown in Figure 2 and the circuit diagram and terminal connections for the "L" package are shown in Figure 3.

3.2.8 Glassivation. The microcircuit die is glassivated.

3.2.9 Schematic circuits. Simplified schematic circuits for "G" and "L" packages are shown in Figures 2 and 3 respectively.

3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Additional electrical performance curves are shown in paragraph 7.

3.3.2 Offset null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 4. If nulling is unnecessary, delete the potentiometer and make no connections.

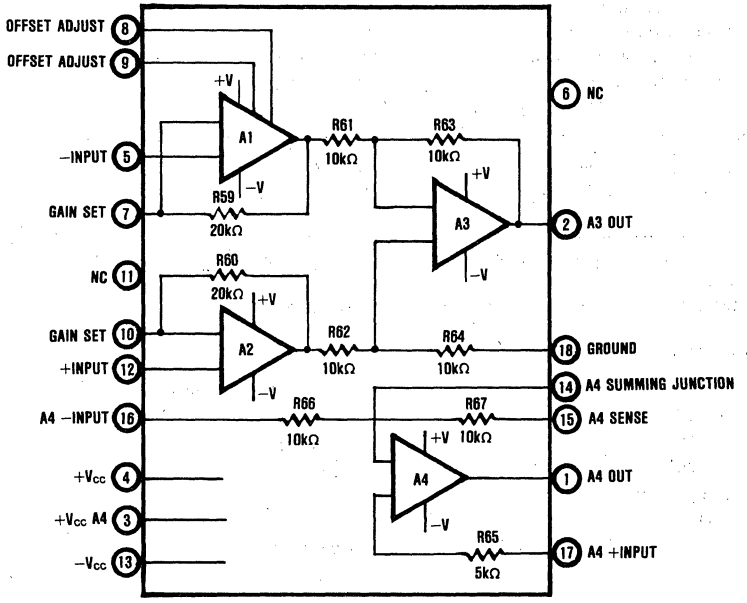


FIGURE 2. INA258 "G" Circuit Diagram and Terminal Connections.

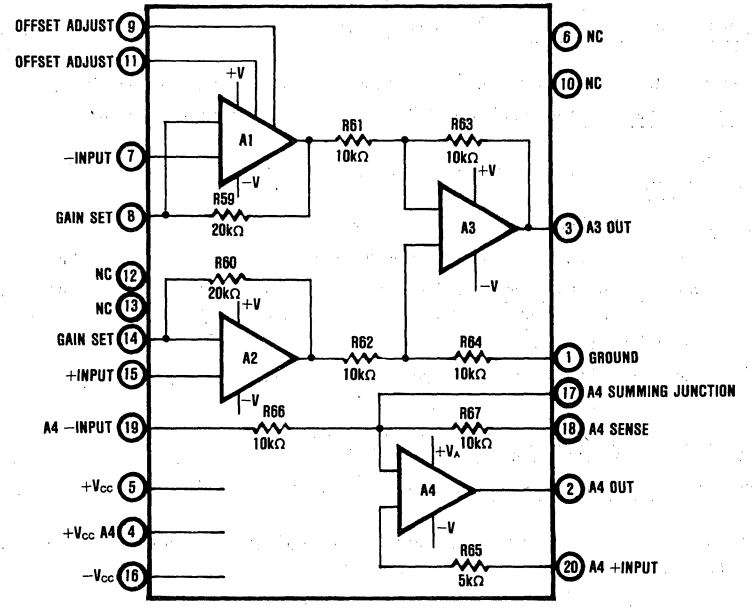


FIGURE 3. INA258 "L" Package Circuit Diagram and Terminal Connections.

TABLE I. Electrical Performance Characteristics.

All characteristics at $-55°C \leq T_A \leq +125°C$, $\pm V_{CC} = 15VDC$, unless otherwise specified.

CHARACTERISTICS	SYMBOL	CONDITIONS	INA258WG/883B INA258WL/883B INA258WG INA258WL			INA258VG/883B INA258VL/883B INA258VG INA258VL			INA258UG/883B INA258UL/883B INA258UG INA258UL			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN												
Range of Gain	A_V	$A_V = 1 + (40k/R_G)$ 1/	1		1000	*		*	*		*	V/V
Gain Equation Error	E_{AV}	$A_V = 1$, $T_A = +25°C$			.05							% FS
		$A_V = 10$, $T_A = +25°C$			.10							% FS
		$A_V = 100$, $T_A = +25°C$			.10							% FS
		$A_V = 1000$, $T_A = +25°C$			.40							% FS
Gain Tempco 2/	$\Delta A_V/\Delta T$	$A_V = 1$		2			*			*		ppm/°C
		$A_V = 10$		20			*			*		ppm/°C
		$A_V = 100$		22			*			*		ppm/°C
		$A_V = 1000$		22			*			*		ppm/°C
DC Nonlinearity	NL	$A_V = 1$, $T_A = +25°C$			0.005							%
		$A_V = 10$, $T_A = +25°C$			0.005							%
		$A_V = 100$, $T_A = +25°C$			0.007							%
		$A_V = 1000$, $T_A = +25°C$			0.025							%
RATED OUTPUT												
Voltage	V_{OP}	$R_L = 2k\Omega$, $T_A = +25°C$	±10			*			*			V
Current	I_O		±5			*			*			mA
Impedance	Z_O			2			*			*		Ω
INPUT OFFSET VOLTAGE												
Initial 3/	V_{io}	$A_V = 1$, $T_A = +25°C$			±250			*			*	μV
	V_{io}	$A_V = 1000$, $T_A = +25°C$			±50			*			*	μV
vs Temperature	$\Delta V_{io}/\Delta T$	$A_V = 1$, $-55°C \leq T_A \leq +125°C$			10			15			45	μV/°C
		$A_V = 1000$, $-55°C \leq T_A \leq +125°C$			0.5			1.0			3.0	μV/°C
		$A_V = 1$, $-25°C \leq T_A \leq +85°C$									20	μV/°C
		$A_V = 1000$, $-25°C \leq T_A \leq +85°C$									1.8	μV/°C
vs Supply	PSRR	$A_V = 1$, $\Delta V_{CC} = \pm 5VDC$, $T_A = +25°C$			20			*			*	μV/V
		$A_V = 1000$, $\Delta V_{CC} = \pm 5VDC$, $T_A = +25°C$			1			*			*	μV/V
INPUT BIAS CURRENT												
Initial	I_{ib}	$T_A = +25°C$			±20			*			*	nA
Tempco	$\Delta I_{ib}/\Delta T$			±.2			*			*		nA/°C
INPUT OFFSET CURRENT												
Initial	I_{io}	$T_A = +25°C$			±20			*			*	nA
Tempco	$\Delta I_{io}/\Delta T$			±.5			*			*		nA/°C
INPUT IMPEDANCE												
Differential	Z_{ID}	$T_A = +25°C$	$10^{10}\|\|3$		*			*		Ω||pF		
Common Mode	Z_{ICM}	$T_A = +25°C$	$10^{10}\|\|3$		*			*		Ω||pF		
INPUT VOLTAGE												
Linear Response Range	V_{IN}		±10			*			*			V
Common Mode Rejection	CMR	DC-60Hz, $A_V = 1k\Omega$ Source Imbalance, $T_A = +25°C$	80			*			*			dB
		DC-60Hz, $A_V = 10$, $1k\Omega$ Source Imbalance $T_A = +25°C$	96			*			*			dB
		DC-60Hz, $A_V = 100$-1000, $1k\Omega$ Source Imbalance, $T_A = +25°C$	106			*			*			dB
INPUT NOISE												
Input Voltage Noise	E_{NPP}	$f_B = 0.01$ to 10Hz, $T_A = +25°C$		.8			*			*		μV, p-p
	E_N	$A_V = 1000$, $f_O = 10Hz$, $T_A = +25°C$		18			*			*		$nV/\sqrt{Hz}$
		$A_V = 1000$, $f_O = 100Hz$, $T_A = +25°C$		15			*			*		$nV/\sqrt{Hz}$
		$A_V = 1000$, $f_O = 1kHz$, $T_A = +25°C$		13			*			*		$nV/\sqrt{Hz}$
Input Current Noise	I_{NPP}	$f_B = 0.01Hz$ to 10Hz, $T_A = +25°C$		50			*			*		pA, p-p
	I_N	$f_O = 10Hz$, $T_A = +25°C$		.8			*			*		$pA/\sqrt{Hz}$
		$f_O = 100Hz$, $T_A = +25°C$		.46			*			*		$pA/\sqrt{Hz}$
		$f_O = 1kHz$, $T_A = +25°C$		.35			*			*		$pA/\sqrt{Hz}$
DYNAMIC RESPONSE												
Slew Rate	SR	$A_V = 1$ to 100, $R_L = 2k\Omega$, $T_A = +25°C$	0.2									V/μsec
Bandwidth	BW	3dB small signal, $A_V = 1$, $T_A = +25°C$		300			*			*		kHz
		$A_V = 10$, $T_A = +25°C$		140			*			*		kHz
		$A_V = 100$, $T_A = +25°C$		25			*			*		kHz
		$A_V = 1000$, $T_A = +25°C$		2.5			*			*		kHz
	BW	Full power $A_V = 1$ to 1000, $T_A = +25°C$		6.4								kHz
Settling Time	T_S	.01%, $A_V = 1$, $T_A = +25°C$		30			*			*		μsec
		$A_V = 100$, $T_A = +25°C$		50			*			*		μsec
		$A_V = 1000$, $T_A = +25°C$		500			*			*		μsec

TABLE I. Electrical Performance Characteristics (cont).

CHARACTERISTICS	SYMBOL	CONDITIONS	INA258WG/883B INA258WL/883B INA258WG INA258WL			INA258VG/883B INA258VL/883B INA258VG INA258VL			INA258UG/883B INA258UL/883B INA258UG INA258UL			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY												
Rated Voltage	$\pm V_{CC}$		±5	±15	±20	*	*	*	*	*	*	V
Quiescent Current	I_Q	$T_A = +25°C$			±8			*			*	mA
FOURTH OP AMP												
Input Offset Drift	V_{IO}	$T_A = +25°C$			5000			*			*	µV
Tempco	$\Delta V_{IO}/\Delta T$	$-55 \leq T_A \leq +125°C$		±5			*	*		*		µV/°C
Input Bias Current	I_{IB}	$T_A = +25°C$			50			*			*	nA
Input Offset Current	I_{IO}	$T_A = +25°C$			50			*			*	nA
Quiescent Current	I_Q	$T_A = +25°C$		2	4			*			*	mA

*Same as INA258W grade.

NOTES: 1/ Typically the tolerance of R_G will be the major source of gain error.
2/ Not including TCR of R_G.
3/ Adjustable to zero at any one gain.

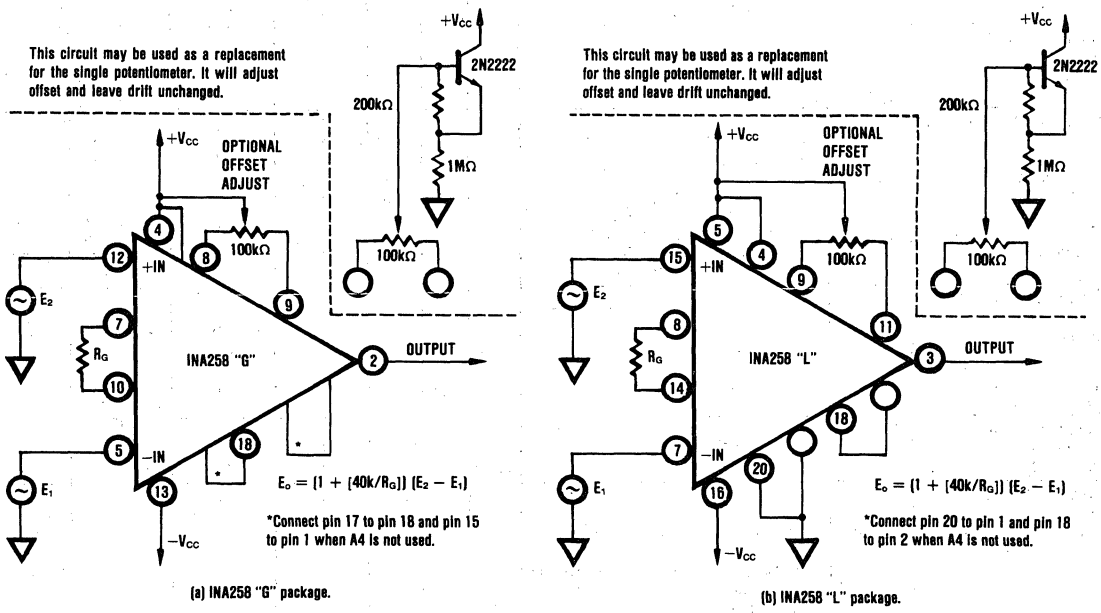


FIGURE 4. Basic Circuit Connection for the INA258 Including Optional Input Offset Null Potentiometer.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

1/ A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

3.6.1 Rework provisions. Rework provisions for the /883B Hi-Rel product designation, including rebonding, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the /883B product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for the /883B Hi-Rel product designation is in accordance with MIL-STD-883, method 5004, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), constant acceleration (condition E), temperature cycle (condition C), and external visual per MIL-STD-883, method 2009.

For the /883B Hi-Rel product designator, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III).

MIL-STD-883 REQUIREMENTS (Class B)	INA258WG/883B INA258WG INA258WL/883B INA258WL	INA258VG/883B INA258VG INA258VL/883B INA258VL	INA258UG/883B INA258UG INA258UL/883B INA258UL
Interim electrical parameters (preburn-in) (method 5004)	1	1	1
Final electrical test parameters (method 5004)	1*, 2, 3, 4	1*, 2, 3, 4	1*, 2, 2U, 3, 3U, 4
Group A test requirements (method 5005)	1, 2, 3, 4	1, 2, 3, 4	1, 2, 2U, 3, 3U, 4
Group C end point electrical parameters (method 5005)	1	1	—

*PDS applies to subgroup 1 (see 4.3.c)

1/Applies to /883B models only.

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD or equivalent	CONDITIONS ($\pm V_{CC}$ = 15VDC unless otherwise specified)	LIMITS						UNITS
				INA258WG/883B INA258WL/883B INA258WG INA258WL		INA258VG/883B INA258VL/883B INA258VG INA258VL		INA258UG/883B INA258UL/883B INA258UG INA258UL		
				MIN	MAX	MIN	MAX	MIN	MAX	
1 T_A = 25°C	V_{io}	4001	A_V = 1		±250		±250		±250	µV
			A_V = 1000		±50		±50		±50	µV
	I_{ib}	4001			±20		±20		±20	nA
	I_{io}	4001			±20		±20		±20	nA
	I_Q	4005	Each Supply		±8		±8		±8	mA
	PSRR	4003	A_V = 1, ΔV_{CC} = ±5VDC		20		20		20	µV/V
			A_V = 1000, ΔV_{CC} = ±5VDC		1		1		1	µV/V
	CMR	4003	DC, A_V = 1, 1kΩ Source Imbalance	80		80		80		dB
			DC, A_V = 10, 1kΩ Source Imbalance	96		96		96		dB
			DC, A_V = 100-1000, 1kΩ Source Imbal.		106	106		106		dB
	V_{io} 1/	4001			5000		5000		5000	µV
	I_{ib} 1/	4001			50		50		50	nA
	I_{io} 1/	4001			50		50		50	nA
	I_Q 1/	4005			4		4		4	mA
2 T_A = 125°C	V_{io}	4001	A_V = 1		1250		1750		5250	µV
			A_V = 1000		100		150		450	µV
	$\Delta V_{io}/\Delta T$	4001	A_V = 1 [V_{io} (125°C) − V_{io} (25°C)] ÷ 100		10		15		45	µV/°C
			A_V = 1000 [V_{io} (125°C) − V_{io} (25°C)] ÷ 100		0.5		1.0		3.0	µV/°C
2U T_A = 85°C	V_{io}	4001	A_V = 1						1575	µV
			A_V = 1000						150	µV
	$\Delta V_{io}/\Delta T$	4001	A_V = 1 [V_{io} (85°C) − V_{io} (25°C)] ÷ 60						20	µV/°C
			A_V = 1000 [V_{io} (85°C) − V_{io} (25°C)] ÷ 60						1.8	µV/°C

TABLE III. Group A Inspection (cont).

SUBGROUP	SYMBOL	MIL-STD-883 METHOD or equivalent	CONDITIONS ($\pm V_{CC}$ = 15VDC unless otherwise specified)	LIMITS						UNITS
				INA258WG/883B INA258WL/883B INA258WG INA258WL		INA258VG/883B INA258VL/883B INA258VG INA258VL		INA258UG/883B INA258UL/883B INA258UG INA258UL		
				MIN	MAX	MIN	MAX	MIN	MAX	
3 $T_A = -55°C$	V_{io}	4001	$A_V = 1$		1050		1450		5250	μV
			$A_V = 1000$		90		150		450	μV
	$\Delta V_{io}/\Delta T$	4001	$A_V = 1$ $[V_{io}\ (25°C) - V_{io}\ (-55°C)] \div 80$		10		15		45	$\mu V/°C$
			$A_V = 1000$ $[V_{io}\ (25°C) - V_{io}\ (-55°C)] \div 80$		1.5		1.0		3.0	$\mu V/°C$
3U $T_A = -25°C$	V_{io}	4001	$A_V = 1$						1380	μV
			$A_V = 1000$						135	μV
	$\Delta V_{io}/\Delta T$	4001	$A_V = 1$ $[V_{io}\ (25°C) - V_{io}\ (-25°C)] \div 50$						20	$\mu V/°C$
			$A_V = 1000$ $[V_{io}\ (25°C) - V_{io}\ (-25°C)] \div 5$						1.8	$\mu V/°C$
4 $T_A = 25°C$	E_{AV}		Gain Equation Error $A_V = 1$		0.05		0.05		0.05	% FS
			$A_V = 10$		0.10		0.10		0.10	% FS
			$A_V = 100$		0.10		0.10		0.10	% FS
			$A_V = 1000$		0.40		0.40		0.40	% FS
	V_{OP}	4004	$R_L = 2k\Omega$	±10		±10		±10		V
	SR		$R_L = 2k\Omega$	0.2		0.2		0.2		V/μsec
	NL 2/	Figure 4	$A_V = 1$		0.005		0.005		0.005	%
			$A_V = 10$		0.005		0.005		0.005	%
			$A_V = 100$		0.007		0.007		0.007	%
			$A_V = 1000$		0.025		0.025		0.025	%

NOTES: 1/ Fourth op amp.

2/ E_1 = 0V and E_2 is varied to enable nonlinearity error to be measured by sampling 21 points between $-10V \leq E_{OUT} \leq +10V$ and determining worst case deviation from straight line connecting these end points at each gain setting.

3.11 Quality conformance inspection. Quality conformance inspection, for the /883B Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5005, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening for the /883 Hi-Rel product designation is in accordance with MIL-STD-883, method 5004, class B, and is conducted on all devices. The following criteria apply:

a. Interim and final test parameters are specified in Table II.

b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

c. Percent defective allowable (PDA). The PDA, for /883B product designation only, is 5 percent and includes both both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5004, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from

preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in are used to determine the percent defective for each manufacturing lot, and the lot is accepted or rejected based on the PDA.

d. External visual inspection need not include measurement of case and lead dimensions.

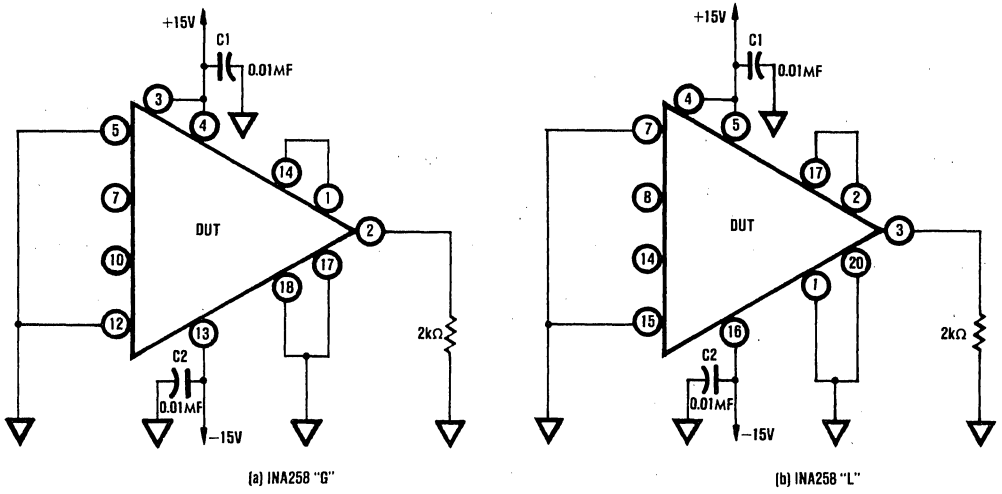


FIGURE 5. Test Circuit, Burn-In and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5005, are performed as required by MIL-STD-883.

A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, class B, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum

b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005 and as follows:

a. End point electrical parameters are specified in Table II herein.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming are intended for use in applications where the use of screened parts is required or desirable.

6.3 Order data. The contract or purchase order should specify the following:

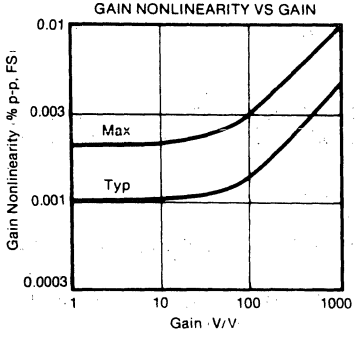
a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

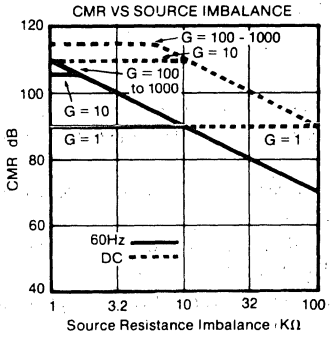
6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group D as defined in MIL-M-38510, Appendix E.

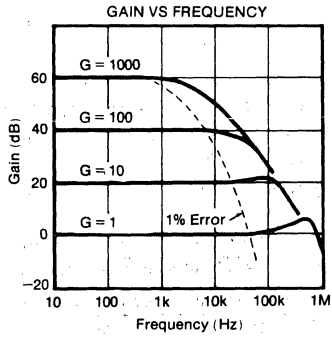
6.5 Electrostatic sensitivity. CAUTION—These microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

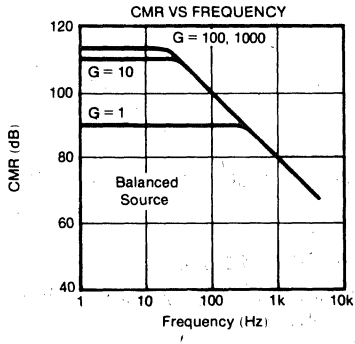
7. ELECTRICAL PERFORMANCE GRADES

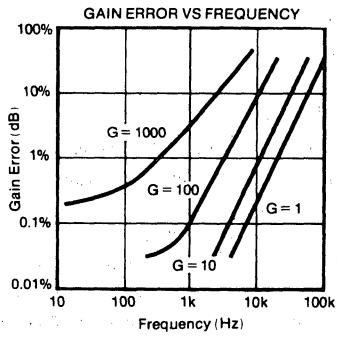
(Typical at +25°C and $\pm V_{CC}$ = 15VDC unless otherwise specified.)

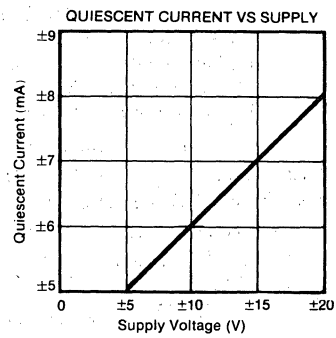


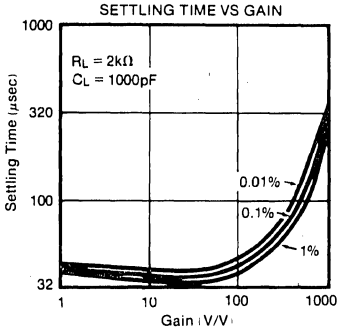


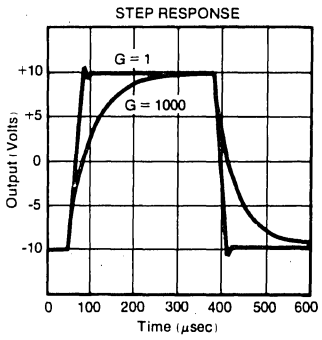


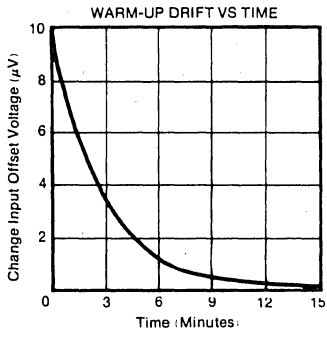


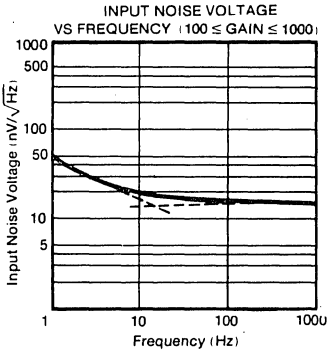


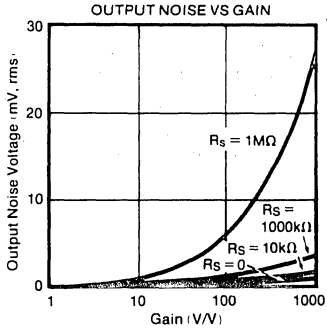












8. APPLICATION INFORMATION

8.1 Description. The INA258 is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found in integrated circuit instrumentation amplifiers. See simplified schematics in Figures 2 and 3.

The input section (A1 and A2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature are low due to the monolithic design, and are improved even further by state-of-the-art laser-trimming techniques.

The output section (A3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the internal resistors are compatible thin-film nichrome formed with the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability of trimmed resistors and simultaneous achievement of excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA258 is operated over wide temperature ranges.

The fourth op-amp (A4) of the INA258 adds a great deal of versatility and convenience to the amplifier. Its use allows easy implementation of active low-pass filtering, output offsetting, and additional gain generation. The pin connections make the use of this stage optional and the specifications appear separately in the table of Electrical Specifications.

8.2 Using the INA258. Figure 4 shows the simplest configuration of the INA258. The gain is set by the external resistor, R_G, with a gain equation of $G = 1 + (40K/R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

For gains greater than unity, resistor R_G is connected externally. At high gains, where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

8.3 Basic circuit connection. The basic circuit connection for the INA258 is shown in Figure 4. The output voltage is a function of the differential input voltage times the gain.

Figure 4 does not include additional internal op amp A4. Power supply bypassing with a 1μF tantalum capacitor or equivalent is always recommended.

In applications which do not use the fourth internal amplifier, insure the A4 $+V_{CC}$ is not connected to V_{CC}, the A4 + input is connected to common and A4 sense is connected to A4 output.

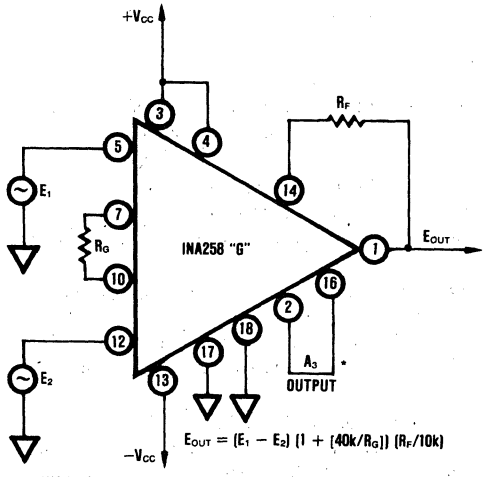
8.4 Typical applications. Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gauges, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA258 accomplishes all of these with high precision.

Figures 6, 7, and 8 show some typical applications circuits.

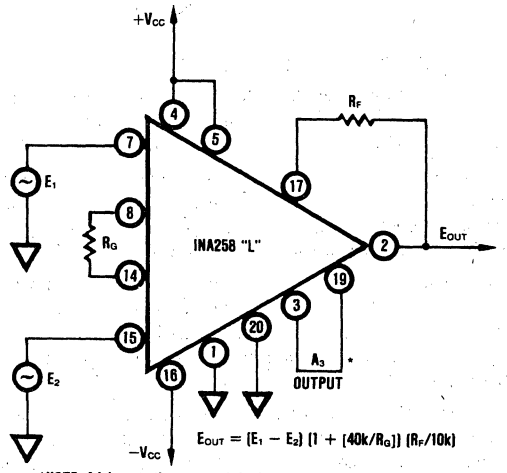
Figure 6 shows how the output stage may be used to provide additional gain. If gains greater than 1000V/V (10,000 up to 100,000 and greater) are desired, it is better to place some gain in the output amplifier rather than the input stage, due to the low values of R_G required ($R_G < 40\Omega$ for $[1 + 40k/R_G] > 1000$). Note, however, that accuracy can degrade due to very high amplification of offset, drift, and noise errors.

Output offsetting ("zero suppression" or "zero elevation") may be more easily accomplished with the INA258 than with most other IC instrumentation amplifiers, as shown in Figure 7. The use of the extra internal op amp, A4, means that CMR of the instrument amp is not disturbed, and that a convenient value of variable resistor can be used.

Amplifier A4 also allows active low-pass filtering to be implemented conveniently with a single capacitor. Filtering can be used for noise reduction or band-limiting of the output signal as shown in Figure 8.

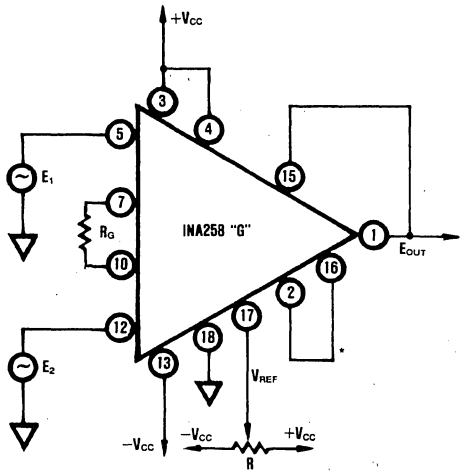


(a) INA258 "G".



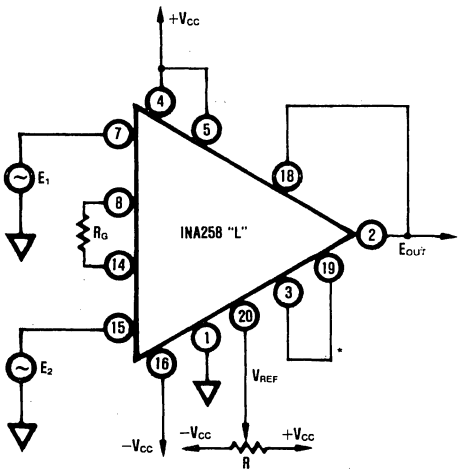
(b) INA258 "L".

FIGURE 6. Additional Gain From Output Stage.



R = a convenient value (<100kΩ typically)
$E_{OUT} = (E_1 - E_2)\ (1 + [40k/R_G]) + 2V_{REF}$
*NOTE: A4 Inverts, see Figure 6.

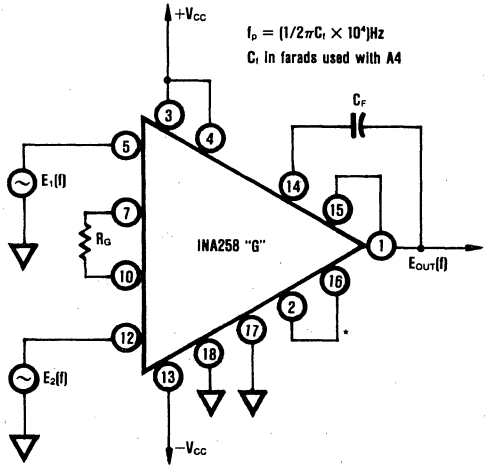
(a) INA258 "G".



R = a convenient value (<100kΩ typically)
$E_{OUT} = (E_1 - E_2)\ (1 + [40k/R_G]) + 2V_{REF}$
*NOTE: A4 Inverts, see Figure 6.

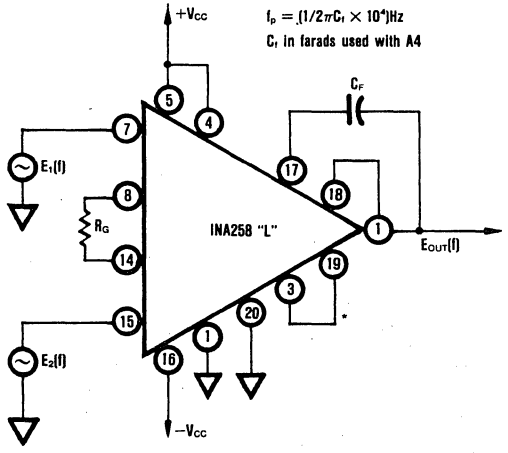
(b) INA258 "L."

FIGURE 7. Output Offsetting.



$E_{OUT} = (E_1 - E_2)\ (1 + [40k/R_G])\ (1/[1 + 2\pi f \times 10^4 \times C_F])$
*NOTE: A4 Inverts, see Figure 6.

(a) INA258 "G"



$E_{OUT} = (E_1 - E_2)\ (1 + [40k/R_G])\ (1/[1 + 2\pi f \times 10^4 \times C_F])$
*NOTE: A4 Inverts, see Figure 6.

(b) INA258 "L".

FIGURE 8. Active Low-Pass Filtering.

BURR-BROWN®

OPA105/883B SERIES

MODEL NUMBERS:

OPA105VM/883B
OPA105VM
OPA105UM/883B
OPA105UM
OPA105WM/883B
OPA105WM

REVISION B
MAY, 1986

FET Input Military OPERATIONAL AMPLIFIER

FEATURES

- LOW BIAS CURRENT, 1pA, max
- HIGH INPUT IMPEDANCE, $10^{13}\Omega$
- ULTRA-LOW DRIFT, $2\mu V/°C$, max
- LOW OFFSET VOLTAGE $250\mu V$, max
- LOW QUIESCENT CURRENT, 1.5mA, max
- HERMETICALLY SEALED TO-99 PACKAGE

APPLICATIONS

- CURRENT-TO-VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS

DESCRIPTION

The OPA105/MIL Series is a low bias current operational amplifier. Guaranteed low initial offset voltage ($250\mu V$, max) and associated drift versus temperature ($2\mu V/°C$, max) is achieved by laser-adjusting the amplifier during manufacturing. This feature, and guaranteed low bias current (1pA, max), allow greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristics of the OPA105/883B Series include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidentally shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA105/883B Series allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a FET input, low bias current, low drift, integrated circuit operational amplifier.

1.2 Part Number. The complete part number is as shown below.

OPA105	V	M	/883B
Basic model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single operational amplifier. Three electrical performance grades are provided. The W grade features $\pm 2\mu V/^{\circ}C$ drift (-55°C to +125°C). The V grade features $\pm 5\mu V/^{\circ}C$ drift (-55°C to +125°C). The U grade features excellent performance ($\pm 15\mu V/^{\circ}C$) from -25°C to +85°C and guarantees performance from -55°C to +125°C.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the class B product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:

Hi-Rel product designator	Requirements
/883B	Standard model, plus 100% MIL-STD-883 class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is A-1 (8-lead can, TO-99) as defined in MIL-M-38510, Appendix C. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	±20VDC [1]
Differential input voltage range	±40VDC [1]
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited [2]
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	±5VDC to ±20VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-A
8-lead can	Figure 1	225mW at T_A =125°C	220°C/W

1 The absolute maximum input voltage is equal to the supply voltage.
2 Short circuit may be to ground only. Rating applies to +135°C case temperature or +50°C ambient temperature at ±15VDC supply voltage.

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

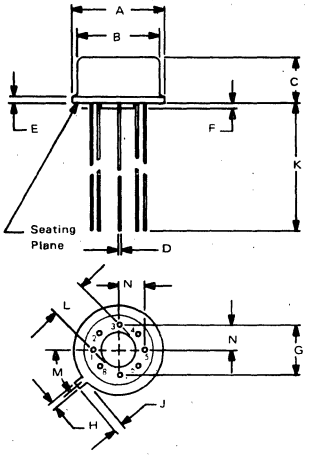
3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510. See Figure 1 for the case outline.



Note:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
Pin numbers shown for reference only.
Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	–	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 1. Case Outline (TO-99) Package Configuration.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. All dice are glassivated.

3.2.9 Schematic Circuit. A simplified schematic circuit is shown in Figure 3.

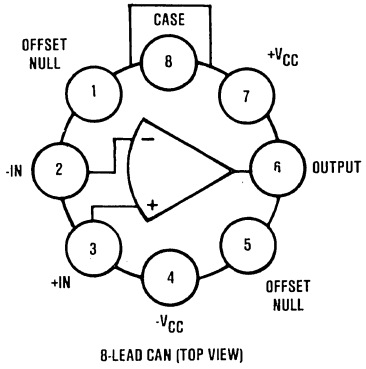
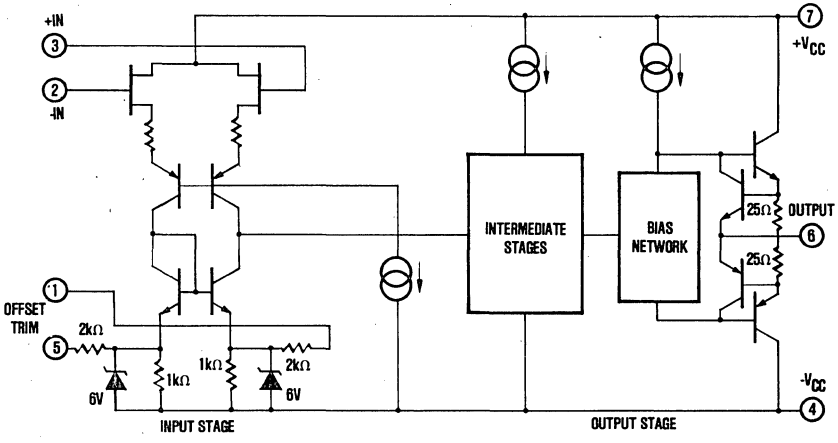


FIGURE 2. Circuit Diagram and Terminal Connections.



3.3 Electrical Performance Characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C unless otherwise specified.

3.3.1 Additional Electrical Performance Characteristics. Electrical performance curves are shown in paragraph 7.

3.3.2 Offset null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 4. If nulling is unnecessary for the application, delete the three components and make no connections.

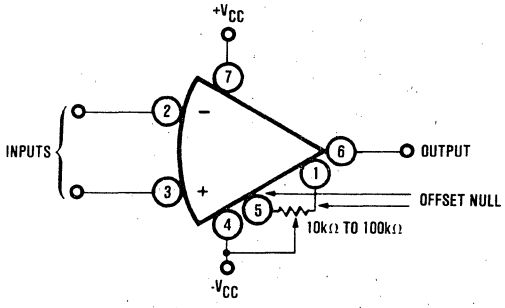


FIGURE 4. Offset Null Circuit.

3.3.3 Frequency compensation. No frequency compensation is required. The amplifier is free of oscillation when operated at any gain and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /883B Hi-Rel product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for /883B Hi-Rel product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

1/ A 4-digit date code, indicating year and week of seal and a 4- or 5-digit lot identifier are marked on each unit.

TABLE I. Electrical Performance Characteristics.

All characteristics at -55°C ≤ T_A ≤ +125°C, ±V_{CC} = 15VDC, unless otherwise specified.

CHARACTERISTIC	SYM-BOL	CONDITIONS	OPA105WM/883B OPA105WM			OPA105VM/883B OPA105VM			OPA105UM/883B OPA105UM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN												
Open-Loop Voltage Gain	Avs	R_L = 2kΩ, V_O = ±10V, F = 0Hz; T_A = +25°C	106	112		*	*		*	*		dB
		-55°C ≤ T_A ≤ +125°C	95	102		*	*		*	*		dB
RATED OUTPUT												
Voltage	Vo	R_L = 1kΩ	±10			*	*		*	*		V
Current	Io		±10			*	*		*	*		mA
Impedance	Zo	T_A = +25°C		3			*			*		kΩ
Load Capacitance	C_L	T_A = +25°C	500	1000		*	*		*	*		pF
Short Circuit Current	Ios	To Ground	10	25		*	*		*	*		mA
DYNAMIC RESPONSE												
Bandwidth	BW	Unity Gain-Small Signal T_A = +25°C		1			*			*		MHz
Bandwidth	BW	Full Power T_A = +25°C	14	20		*	*		*	*		kHz
Slew Rate	SR	R_L = 2kΩ, T_A = +25°C	0.9	1.3		*	*		*	*		V/μsec
Settling Time (0.1%)	Ts	T_A = +25°C		9			*			*		μsec
Settling Time (0.01%)	Ts	T_A = +25°C		20			*			*		μsec
Overload Recovery 1/	Tr	T_A = +25°C		4	15		*	*		*	*	μsec
INPUT OFFSET VOLTAGE												
Initial Offset	V_{IO}	T_A = +25°C			±250			*			*	μV
Temperature Sensitivity	DV_{IO}	$\frac{V_{IO}(T_A) - V_{IO}(+25°C)}{\Delta T}$										
		-55 ≤ T_A ≤ +125°C			±2			±5			±25	μV/°C
		-25 ≤ T_A ≤ +85°C									±15	μV/°C
vs Power Supply	PSRR	V_{CC} = ±5, V_{CC} = ±20VDC			±74			*			*	dB
INPUT BIAS CURRENT												
Initial Bias 2/	I_{IB}	T_A = +25°C			1			*			*	pA
vs Supply Voltage		T_A = +25°C		0.005			*			*		pA/V
INPUT OFFSET CURRENT												
Initial Offset	I_{IO}	T_A = +25°C		±0.2			*			*		pA
INPUT IMPEDANCE												
Differential	Z_{Id}	T_A = +25°C		10^{13} || 1.6			*			*		Ω || pF
Common-Mode	Z_{ICM}	T_A = +25°C		10^{15} || 1.8			*			*		Ω || pF
INPUT NOISE												
Voltage	e_n	f_o = 10Hz T_A = +25°C		55			*			*		$nV/\sqrt{Hz}$
		f_o = 100Hz T_A = +25°C		35			*			*		$nV/\sqrt{Hz}$
		f_o = 1kHz T_A = +25°C		30			*			*		$nV/\sqrt{Hz}$
		f_o = 10kHz T_A = +25°C		25			*			*		$nV/\sqrt{Hz}$
		f_B = 0.1Hz to 10Hz T_A = +25°C		3			*			*		μV/, p-p
Current	i_n	f_B = 0.1Hz to 10Hz T_A = +25°C		0.01			*			*		pA, p-p
		f_B = 10Hz to 10kHz T_A = +25°C		0.03			*			*		pA, rms
		f_o = 1kHz T_A = +25°C		0.6			*			*		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE												
Differential	V_{DI}	T_A = +25°C	±20			*			*			V
Common-Mode		T_A = +25°C	±10	±12		*	*		*	*		V
Common-Mode Rejection	CMRR	V_{IN} = ±10V T_A = +25°C	76	86		*	*		*	*		dB
POWER SUPPLY												
Rated Voltage	V_{DI}			±15			*			*		VDC
Voltage Range			±5		±20	*		*	*		*	VDC
Quiescent Current	I_Q			1.0	1.5		*	*		*	*	mA
TEMPERATURE RANGE (ambient)												
Operating			-55		+125	*		*	*		*	°C
Storage			-65		+150	*		*	*		*	°C

*Same as OPA105W grade

NOTES:

1/ Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.

2/ Bias current is tested and guaranteed at T_A = +25°C. For higher temperature the bias current doubles every +10°C.

3.9 Screening. Screening for /883B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), temperature cycle, constant acceleration (condition B), and external visual inspection per MIL-STD-883, method 2009.

For the /883B Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection for the /883B Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MIL-STD-883B REQUIREMENTS (hybrid class) / MODELS	OPA105WM/883B OPA105WM	OPA105VM/883B OPA105VM	OPA105UM/883B OPA105UM
Interim electrical parameters (pre burn-in) (method 5008)	1, 4	1, 4	1, 4
Final electrical test parameters (method 5008)	1*, 2, 3, 4	1*, 2, 3, 4	1*, 2, 2U, 3, 3U, 4
Group A test requirements (method 5008) 2/	1, 2, 3, 4,	1, 2, 3, 4	1, 2, 2U, 3, 3U, 4
Group C end point electrical parameters (method 5008) 2/	1	1	1
Additional electrical subgroups for Group C inspections 2/	5, 6	5, 6	---

*PDA applies to subgroups 1, 4 see 4.3d)

1/LTPD for these additional tests is 15%.

2/Applies for /883B models only.

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS $\pm V_{CC}$ = 15VDC unless otherwise specified	LIMITS						UNITS
				OPA105WM/883B OPA105WM		OPA105VM/883B OPA105VM		OPA105UM/883B OPA105UM		
				MIN	MAX	MIN	MAX	MIN	MAX	
	V_{IO}	4001			±250		±250		250	µV
	I_{IB}	4001			±1		±1		±1	pA
	V_O		R_L = 2kΩ	±10		±10		±10		V
1	I_Q				1.5		1.5		1.5	mA
T_A = +25°C	CMRR	4003	V_{CM} ±10V	76		76		76		dB
	PSRR		V_{CC} = ±5V, V_{CC} = ±20V	74		74		74		dB
2 T_A = +125	DV_{IO}	4001	$\frac{V_{IO}(+125) - V_{IO}(+25)}{100}$		2		5			µV/°C
2U T_A = +85°C	DV_{IO}	4001	$\frac{V_{IO}(+85) - V_{IO}(+25)}{60°C}$						15	µV/°C
3 T_A = -55°C	DV_{IO}	4001	$\frac{V_{IO}(+25) - V_{IO}(-55)}{80}$		2		5			µV/°C
3U T_A = -25°C	DV_{IO}	4001	$\frac{V_{IO}(+25) - V_{IO}(-25)}{50}$						15	µV/°C
4	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	106		106		106		dB
T_A = +25°C	SR	4002	R_L = 2kΩ, V_O = ±10V	0.9		0.9		0.9		V/µsec
5 T_A = +125°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	95		95				dB
6 T_A = -55°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	95		95				dB

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening, the /883B Hi-Rel product designation, is in accordance with MIL-STD-883B, method 5008, class B, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition B, Y_1 axis only.
b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum
d. Percent defective allowable (PDA). The PDA, for /883B Hi-Rel product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.
e. External visual inspection need not include measurement of case and lead dimensions.

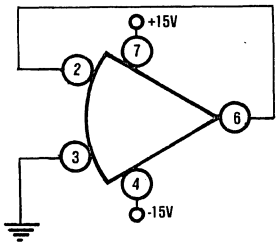


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, are performed as required by MIL-STD-883.

A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

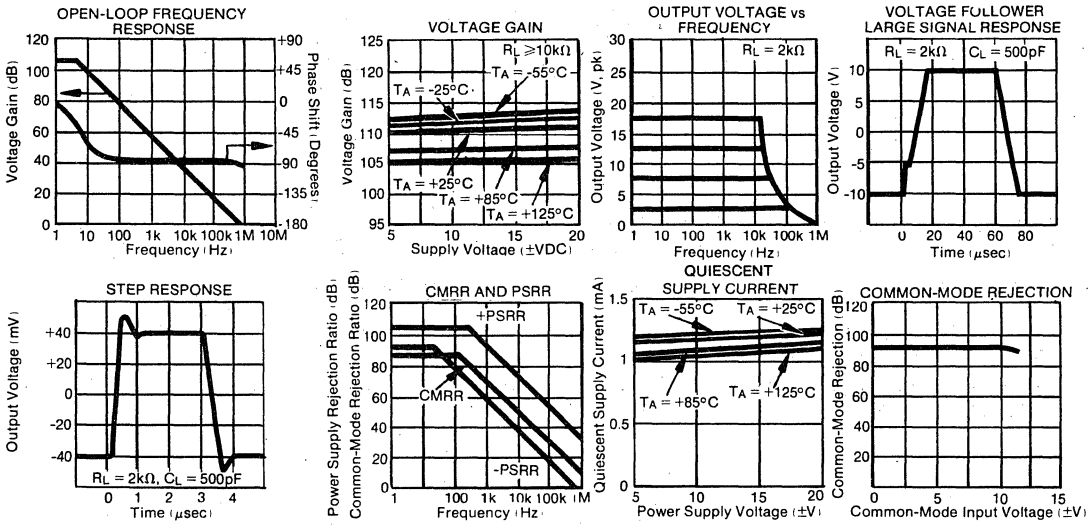
a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group I as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. ELECTRICAL PERFORMANCE CURVES.

(Typical at $T_A = +25°C$ and $\pm V_{CC} = 15VDC$ unless otherwise specified).



8. APPLICATION INFORMATION

8.1 Offset voltage adjustment. Although the OPA105/883B Series has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. Figure 4 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C for every 100μV of offset adjustment.

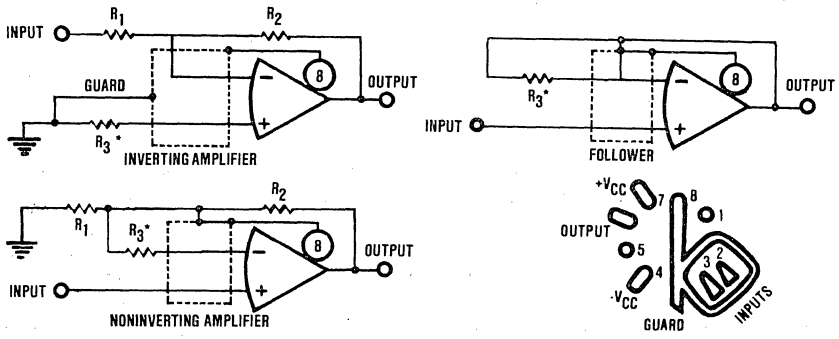
8.2 Guarding and shielding. The ultra-low bias current and high input impedance of the OPA105/883B Series are well-suited to a number of stringent applications, however, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA105/883B Series.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the amplifier's bias current of the OPA105/883B Series. To avoid leakage problems, it is recommended that the signal input lead of the OPA105/883B Series be wired to a Teflon standoff. If the OPA105/883B Series is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low input impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 6 illustrates the use of the guard. The resistor R_3 shown in Figure 6 is optional. It may be used to compensate effects of very large source resistances. However, note that its use would also increase the noise due to the thermal noise of R_3.

8.3 Thermal response time. Thermal response time is an important parameter in low drift operational amplifiers like the OPA105/MIL Series. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA105/883B Series is 20 seconds.



*R_3 may be used to compensate for very large source resistances.

$R_1 R_2/(R_1+R_2)$ must be low impedance.

Board layout for input guarding with TO-99 Package.

FIGURE 6. Connection of Input Guard.

BURR-BROWN®

OPA106/883B SERIES

MODEL NUMBERS:

OPA106WM/883B
OPA106WM
OPA106UM/883B
OPA106UM
OPA106VM/883B
OPA106VM

REVISION B
MAY, 1986

FET Input Military OPERATIONAL AMPLIFIER

FEATURES

- LOW BIAS CURRENT, 100fA, max
- HIGH INPUT IMPEDANCE, $10^{13}\Omega$
- LOW DRIFT, $5\mu V/°C$, max
- LOW OFFSET VOLTAGE $250\mu V$, max
- LOW QUIESCENT CURRENT, 1.5mA, max
- HERMETICALLY SEALED TO-99 PACKAGE

APPLICATIONS

- CURRENT-TO-VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS

DESCRIPTION

The OPA106/883B Series is a low bias current 100fA, max) operational amplifier. Guaranteed low initial offset voltage ($250\mu V$, max) and associated drift versus temperature ($5\mu V/°CC$, max) is achieved by laser-adjusting the amplifier during manufacturing. This feature, and guaranteed low bias current allow greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristic of the OPA106/883B Series include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidentally shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA106/883B Series allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a FET input, low bias current, low drift, integrated circuit operational amplifier.

1.2 Part Number. The complete part number is as shown below.

OPA106	V	M	/883B
Basic model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single operational amplifier. Three electrical performance grades are provided. The W grade features $\pm 5\mu V/°C$ drift (-55°C to +125°C). The V grade features $\pm 10\mu V/°C$ drift (-55°C to +125°C). The U grade features $\pm 20\mu V/°C$ drift from -25°C to +85°C and guarantees performance from -55°C to +125°C.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the class B product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:

Hi-Rel product designator	Requirements
/883B	Standard model, plus 100% MIL-STD-883 class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is A-1 (8-lead can, TO-99) as defined in MIL-M-38510, Appendix C. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	±20VDC 1/
Differential input voltage range	±40VDC 1/
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited 2/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = +175°C

1.2.5 Recommended operating conditions.

Supply voltage range	±5VDC to ±20VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C
8-lead can	Figure 1	225mW at T_A = +125°C	220°C/W

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ Short circuit may be to ground only. Rating applies to +135°C case temperature or +50°C ambient temperature at ±15VDC supply voltage.

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

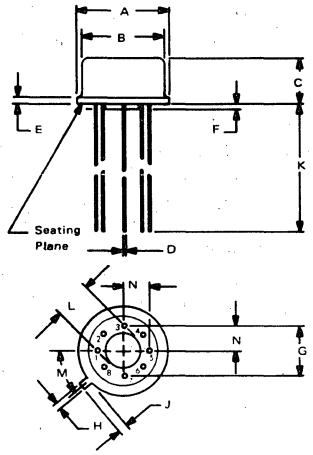
3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510. See Figure 1 for the case outline.



Note:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
Pin numbers shown for reference only.
Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	–	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 1. Case Outline (TO-99) Package Configuration.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. All dice utilized are glassivated.

3.2.9 Schematic Circuit. The schematic circuit is shown in Figure 3.

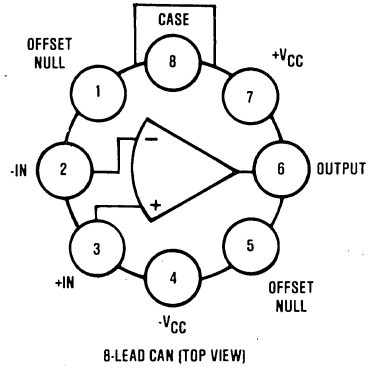


FIGURE 2. Circuit Diagram and Terminal Connections.

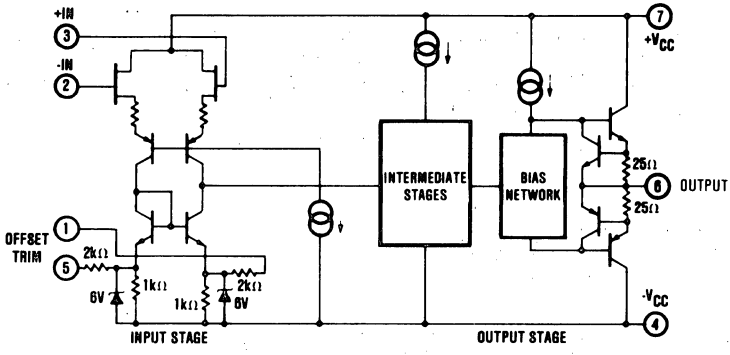


FIGURE 3. Simplified Schematic Circuit.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Electrical performance curves are shown in paragraph 7.

3.3.2 Offset null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 4. If nulling is unnecessary for the application, delete the potentiometer and make no connections.

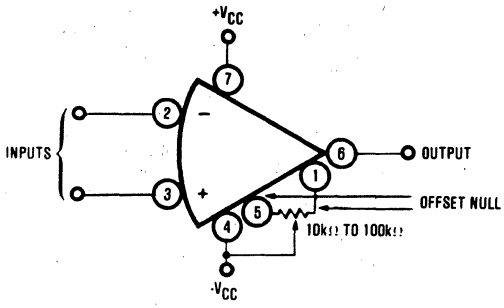


FIGURE 4. Offset Null Circuit.

3.3.3 Frequency compensation. No frequency compensation is required. The amplifier is free of oscillation when operated at any gain and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
d. Manufacturer's identification (BURR-BROWN®)
e. Manufacturer's designating symbol (CEBS)
f. Country of origin

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /883B Hi-Rel product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for /883B product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

1/ A 4-digit date code, indicating year and week of seal and a 4- or 5-digit lot identifier are marked on each unit.

TABLE I. Electrical Performance Characteristics.

All characteristics at -55°C ≤ T_A ≤ +125°C, ±V_{CC} = 15VDC, unless otherwise specified.

CHARACTERISTIC	SYMBOL	CONDITIONS		OPA106WM/883B OPA106WM			OPA106VM/883B OPA106VM			OPA106UM/883B OPA106UM			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN													
Open-Loop		R_L = 2kΩ	T_A = +25°C	103	109		•	•		•	•		dB
Voltage Gain	A_{VS}	V_O = ±10V, F = 0Hz	-55°C ≤ T_A ≤ +125°C	93	101		•	•		•	•		dB
RATED OUTPUT													
Voltage	V_O	R_L = 1kΩ		±10			•			•			V
Current	I_O			±10			•			•			mA
Impedance	Z_O		T_A = +25°C		3			•			•		kΩ
Load Capacitance	C_L		T_A = +25°C	500	1000		•	•		•	•		pF
Short Circuit Current	I_{OS}	To Ground		10	25		•	•		[illegible]	[illegible]		mA
DYNAMIC RESPONSE													
Bandwidth	BW	Unity Gain-Small, Signal	T_A = +25°C		1			•			•		MHz
Bandwidth	BW	Full Power	T_A = +25°C	19	28		•	•		•	•		kHz
Slew Rate	SR	R_L = 2kΩ,	T_A = +25°C	1.2	1.8		•	•		•	•		V/µsec
Settling Time (0.1%)	T_S		T_A = +25°C		6			•			•		µsec
Settling Time (0.01%)	T_S		T_A = +25°C		18			•			•		µsec
Overload Recovery 1/	T_R		T_A = +25°C		4	15		•	•		•	•	µsec
INPUT OFFSET VOLTAGE													
Initial Offset	V_{IO}		T_A = +25°C			±250			•			•	µV
Temperature Sensitivity	DV_{IO}	$\frac{V_{IO}(T_A) - V_{IO}(+25°C)}{\Delta T}$											
			-55°C ≤ T_A ≤ +125°C			±5			±10			50	µV/°C
			-25°C ≤ T_A ≤ +85°C									±20	µV/°C
vs Power Supply	PSRR	V_{CC} = ±5, V_{CC} = ±20VDC				±80			•			•	dB
INPUT BIAS CURRENT													
Initial Bias	I_{ib}		T_A = +25°C			-100			-150			-300	fA
vs Supply Voltage			T_A = +25°C		1			•			•		fA/V
INPUT OFFSET CURRENT 2/													
Initial Offset	I_{IO}		T_A = +25°C		±40			±80			±80		fA
INPUT IMPEDANCE													
Differential	Z_{ID}	T_A = +°C			10^{13} || 0.8			•			•		Ω || pF
Common-Mode	Z_{ICM}				10^{15} || 1.6			•			•		Ω || pF
INPUT NOISE													
Voltage	e_n	f_O = 10Hz	T_A = +25°C		75			•			•		nV/√Hz
		f_O = 100Hz	T_A = +25°C		55			•			•		nV/√Hz
		f_O = 1kHz	T_A = +25°C		35			•			•		nV/√Hz
		f_O = 10kHz	T_A = +25°C		35			•			•		nV/√Hz
		f_B = 0.1Hz to 10Hz	T_A = +25°C		6			•			•		µV/, p-p
Current	i_n	f_B = 0.1Hz to 10Hz	T_A = +25°C		3			•			•		fA, p-p
		f_B = 10Hz to 10kHz	T_A = +25°C		10			•			•		fA, rms
		f_O = 1kHz	T_A = +25°C		0.25			•			•		fA/√Hz
INPUT VOLTAGE RANGE													
Differential	V_{dl}		T_A = +25°C	±20			•			•			V
Common-Mode			T_A = +25°C	±10	±12		•	•		•	•		V
Common-Mode Rejection	CMRR	V_{IN} = ±10V	T_A = +25°C	76	86		•	•		•	•		dB
POWER SUPPLY													
Rated Voltage	±V_{CC}				±15			•			•		VDC
Voltage Range				±5		±20	•		•	•		•	VDC
Quiescent Current	I_Q				1.0	1.5		•	•		•	•	mA
TEMPERATURE RANGE (ambient)													
Operating				-55		+125	•		•	•		•	°C
Storage				-65		+150	•		•	•		•	°C

*Same as OPA106W Grade

NOTES:
1/ Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.
2/ Bias current is tested and guaranteed at T_A = +25°C. For higher temperature the bias current doubles every +10°C.

3.9 Screening. Screening for the /883B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), temperature cycle (condition C), constant acceleration (condition B), and external visual inspection per MIL-STD-883, method 2009.

For the /883B Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection for the /883B Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MIL-STD-883 REQUIREMENTS (Hybrid Class) / MODELS	OPA106WM/883B OPA106WM	OPA106VM/883B OPA106VM	OPA106UM/883B OPA106UM
Interim electrical parameters (pre burn-in) (method 5008)	1, 4	1, 4	1, 4
Final electrical test parameters (method 5008)	1, 2, 3, 4	1, 2, 3, 4	1, 2, 2U, 3, 3U, 4
Group A test requirements (method 5008) 2/	1*, 2, 3, 4	1*, 2, 3, 4	1*, 2, 2U, 3, 3U, 4
Group C end point electrical parameters (method 5008) 2/	1, 4	1, 4	1, 4
Additional electrical subgroups for Group C inspections 2/	5, 6 1/	5, 6 1/	—

*PDA applies to subgroups 1-4 (see 4.3.d)
1/ LTPD for these additional tests is 15%.1
2/ Applies for "/883B" models only.

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS $\pm V_{CC}$ = 15VDC unless otherwise specified	LIMITS						UNITS
				OPA106WM/883B OPA106WM		OPA106VM/883B OPA106WM		OPA106UM/883B OPA106UM		
				MIN	MAX	MIN	MAX	MIN	MAX	
	V_{IO}	4001			±250		±250		±250	µV
	I_{IB}	4001			±100		±150		±300	fA
	V_O		R_L = 2kΩ	±10		±10		±10		V
1	I_Q				1.5		1.5		1.5	mA
T_A = +25°C	CMRR	4003	V_{CM} ±10V	76		76		76		dB
	PSRR		V_{CC} = ±5V, V_{CC} = ±20V	80		80		80		dB
2 T_A = +125°C	DV_{IO}	4001	$\frac{V_{IO}\ (125) - V_{IO}\ (25)}{100}$		5		10			µV/°C
2U T_A = +85°C	DV_{IO}	4001	$\frac{V_{IO}\ (85) - V_{IO}\ (25)}{60}$						20	µV/°C
3 T_A = -55°C	DV_{IO}	4001	$\frac{V_{IO}\ (25) - V_{IO}\ (-55)}{80}$		5		10			µV/°C
3U T_A = -25°C	DV_{IO}	4001	$\frac{V_{IO}\ (25) - V_{IO}\ (-25)}{50}$						20	µV/°C
4	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	103		103		103		dB
T_A = +25°C	SR	4002	R_L = 2kΩ V_O = ±10V	1.2		1.2		1.2		V/µsec
5 T_A = +125°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	93		93				dB
6 T_A = -55°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	93		93				dB

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening, for the /883B Hi-Rel product designation, is in accordance with MIL-STD-883B, method 5008, class B, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition B, Y_1 axis only.
b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum
d. Percent defective allowable (PDA). The PDA, for/883B product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.
e. External visual inspection need not include measurement of case and lead dimensions.

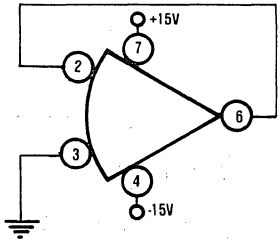


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, are performed as required by MIL-STD-883.

A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum.
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

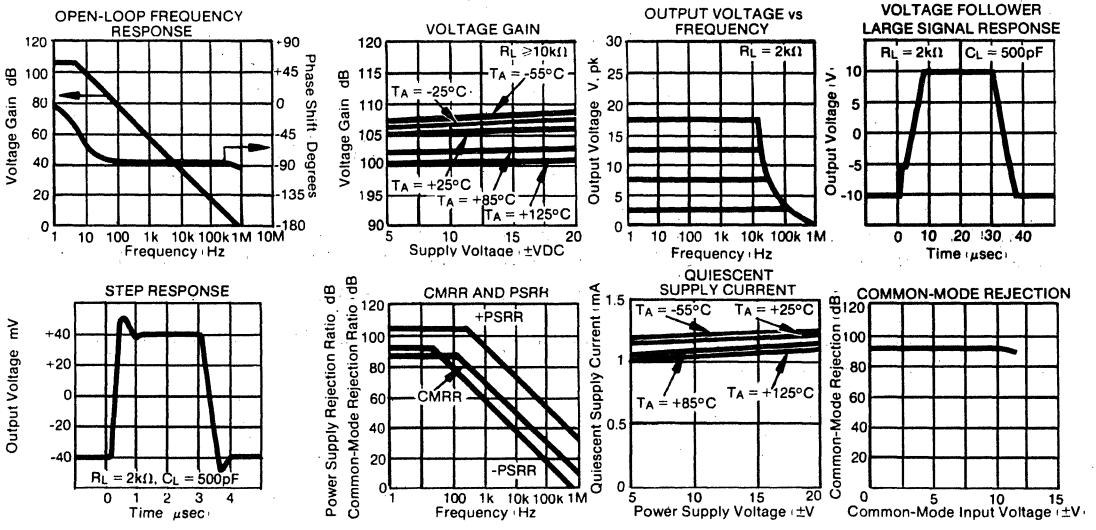
a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group I as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. ELECTRICAL PERFORMANCE CURVES.

(Typical at $T_A = +25°C$ and $\pm V_{CC} = 15VDC$ unless otherwise specified).



8. APPLICATION INFORMATION

8.1 Offset voltage adjustment. Although the OPA106/883B Series has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. Figure 4 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C for every 100μV of offset adjustment.

8.2 Guarding and shielding. The ultra-low bias current and high impedance of the OPA106/883B Series are well-suited to a number of stringent applications, however, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA106/883B Series.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA106/883B Series. To avoid leakage problems, it is recommended that the signal input lead of the OPA106/883B Series be wired to a Teflon standoff. If the OPA106/883B Series is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low input impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 6 illustrates the use of the guard. The resistor R_3 shown in Figure 6 is optional. It may be used to compensate effects of very large source resistances. However, note that its use would also increase the noise due to the thermal noise of R_3.

8.3 Thermal response time. Thermal response time is an important parameter in low drift operational amplifiers like the OPA106/883B Series. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA106/883B Series is approximately 20 seconds.

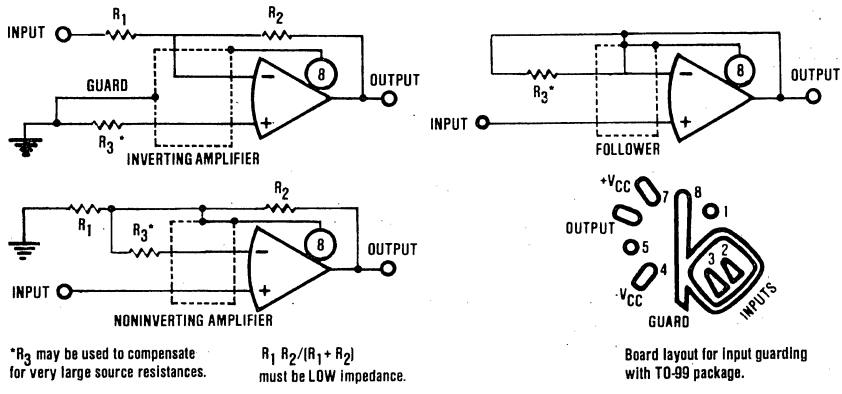


FIGURE 6. Connection of Input Guard.

BURR-BROWN®

OPA600/883B SERIES

MODEL NUMBERS:

OPA600VM/883B **OPA600UM/883B**

OPA600VM **OPA600UM**

REVISION D
MAY, 1986

Fast Settling - Wideband OPERATIONAL AMPLIFIER

FEATURES

- **FAST SETTLING**
  80nsec to ±0.1%
  115nsec to ±0.01%
- **FULL DIFFERENTIAL FET INPUT**
- **-55°C TO +125°C OPERATION**
- **LARGE OUTPUT**
  ±10V, ±200mA (50Ω)
- **GAIN-BANDWIDTH PRODUCT - 5GHz**

APPLICATIONS

- **VOLTAGE CONTROLLED OSCILLATOR DRIVER**
- **LARGE SIGNAL, WIDEBAND DRIVERS**
- **HIGH SPEED DAC OUTPUT AMPLIFIER**
- **VIDEO PULSE AMPLIFIER**

DESCRIPTION

The OPA600 is a wideband operational amplifier specifically designed for fast settling to ±0.01% accuracy. It is stable, easy to use, has good phase margin with minimum overshoot, and it has excellent DC performance. It utilizes a FET input stage to give low input bias current in contrast to the higher currents usually associated with very-fast amplifiers. Its DC stability with temperature is outstanding. Its -3dB bandwidth of 100MHz is available at a closed loop gain of 10. The slew rate exceeds 400V/μsec. All of this combines to form an outstanding amplifier for large and small signals.

Settling time is the best measure of this amplifier's total dynamic capability. High accuracy with fast settling is achieved by the large open-loop gain, which provides the accuracy at the upper frequencies. The thermally balanced design maintains this accuracy without droop or thermal tail. External compensation allows the user to optimize the settling time in his application.

The OPA600 is built to be reliable and is designed to operate from T_A = -55°C to +125°C. It is a hybrid microcircuit in a welded, hermetic, metal package and is available with MIL-STD-883 screening. The circuit is built on an alumina substrate which has a metallic attach to the package for good thermal transfer and reliable high temperature operation. The metal package provides electrostatic shielding. The circuit uses thin-film resistors and all glassivated, high speed silicon die. The gold or aluminum wire-bonds utilized produce a monometallic system wherever possible, eliminating metal migration, a time-temperature reliability problem. The amplifier is actively laser-trimmed and is thoroughly tested. Reliability is emphasized during each phase of manufacture.

The OPA600 is useful in a broad range of video, high speed, and ECM applications. It is particularly well suited to operate as a voltage controlled oscillator (VCO) driver. It makes an excellent digital-to-analog converter output amplifier. It is a workhorse in test equipment where fast pulses, large signals, and 50Ω drive are important. It is a good choice for sample/holds, integrators, fast waveform generators, and multiplexers.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a hybrid, fast settling, integrated circuit operational amplifier.

1.2 Part Number. The complete part number is as shown below.

OPA600	V	M	/883B
Basic model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, operational amplifier. Two electrical performance grades are provided, the U grade and the V grade. The V grade offers the higher performance. Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:

Hi-Rel product designator	Requirements
/883B	Standard model, plus 100% MIL-STD-883, method 5008, class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline (16-lead can) is as defined in Figure 6. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±17VDC
Input voltage range	±17VDC 1/
Differential input voltage range	±25VDC 1/
Storage temperature range	-65°C to +150°C
Output short-circuit duration	A few seconds 2/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	±9VDC to ±16VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ C-A
16-lead can	Figure 4	2.6W at T_{CASE} = +125°C	See Applications Information	35°C/W

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ Duration is limited by device heat sinking (thermal resistance). Short circuit may be to ground only.

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510, except that organic and polymeric materials (epoxy) are used for attach of some of the die. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

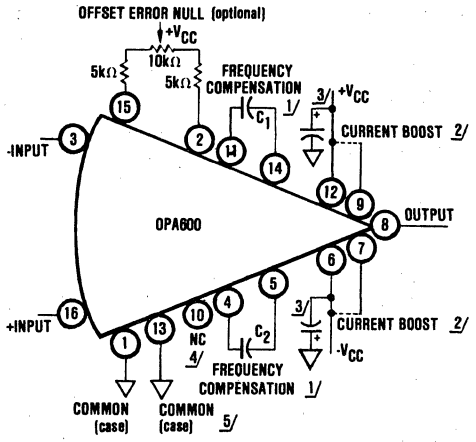
3.2.4 Lead material and finish. The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

3.2.8 Glassivation. Glassivation is in accordance with MIL-M-38510.



1/ Refer to Figure 4 for recommended frequency compensation.
2/ Connect pin 9 to pin 12 and connect pin 7 to pin 6 for maximum output current. See Application Information for further information.
3/ Bypass each power supply lead as close as possible to the amplifier pins. A 1 μF CS13 tantalum capacitor is recommended.
4/ There is no internal connection. An external connection may be made.
5/ It is recommended that the amplifier be mounted with the case in contact with a ground plane for good thermal transfer and optimum AC performance.

FIGURE 1. Circuit Diagram and Terminal Connections.

3.2.9 Schematic Circuit. The schematic circuit is shown in Figure 2.

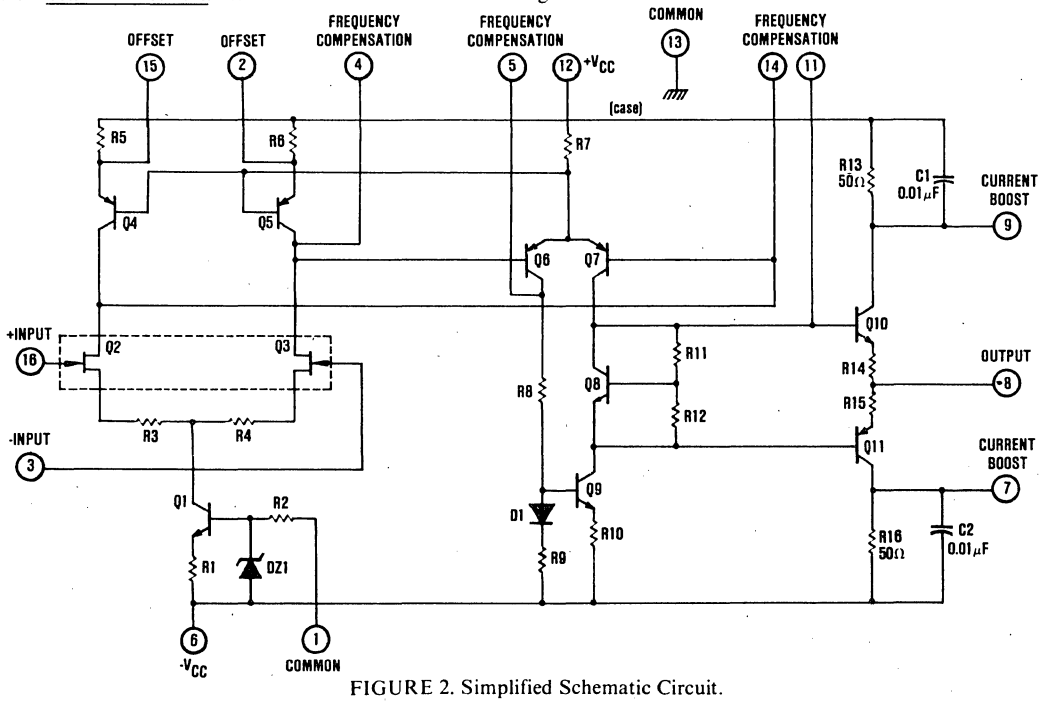


FIGURE 2. Simplified Schematic Circuit.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Electrical performance characteristic curves are shown in paragraph 7.

3.3.2 Offset error null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 3. If nulling is unnecessary for the application, delete the three components and make no connections.

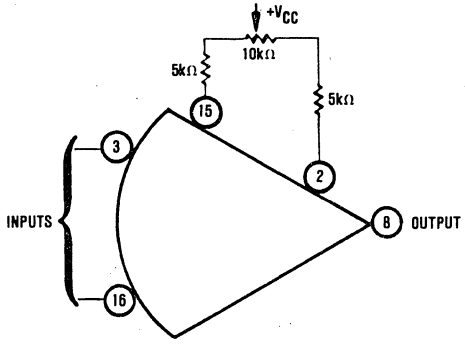


FIGURE 3. Offset Null Circuit.

3.3.3 Frequency compensation. The amplifier must be externally frequency compensated. See Figure 4.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Index point
b. Part number (see paragraph 1.2)
c. Inspection lot identification code 1/
d. Manufacturer's identification (BURR-BROWN®)
e. Manufacturer's designating symbol (CEBS)
f. Country of origin

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /883B Hi-Rel product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for /883B Hi-Rel product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

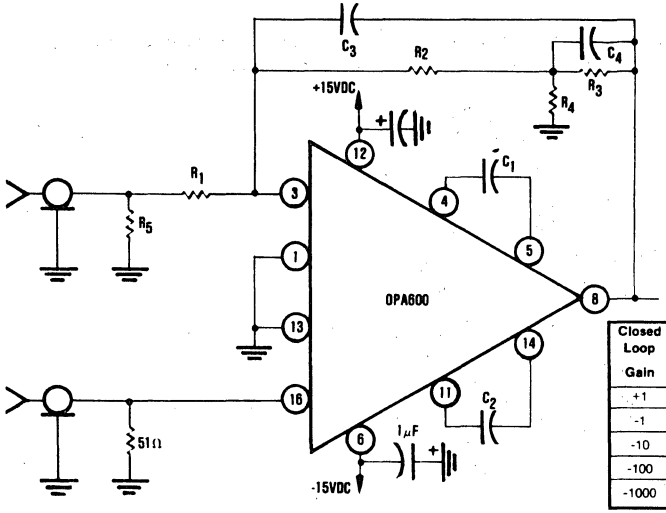
3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for /883B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.
Screening for the standard model, includes Burr-Brown QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), temperature cycle, constant acceleration (condition B), and external visual inspection per MIL-STD-883, method 2009.

For the /883B Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection for the /883B Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.



Closed Loop Gain	R_1	R_2	R_3	R_4	C_1, C_2	C_3	C_4	R_5
+1	open	100	short	open	6.8	0	0	--
-1	620	620	short	open	3.3	4.7	0	56
-10	100	1k	short	open	1	2.2	0	100
-100	100	3.3k	3.3k	3.2k	0	1	0	100
-1000	100	3.3k	3.3k	116	0	0	4.7	100

Note: Resistance is in ohms, capacitance is in pF, gain is volts/volt.

FIGURE 4. Recommended Amplifier Circuits and Frequency Compensation.

1/ A 4-digit date code, indicating year and week of seal, and a 4- or 5-digit lot indentifier is marked on each unit.

TABLE I. Electrical Performance Characteristics

All characters from -55°C ≤ T_A ≤ +125°C, ±V_{CC} = 15VDC, unless otherwise noted.

			OPA600VM/883B OPA600VM			OPA600UM/883B OPA600UM			
CHARACTERISTICS	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OUTPUT									
Voltage (V_O)	R_L = 2kΩ		±10	±11		•	•		V
	R_L = 50Ω 1/		±9	±10		•	•		V
Current (I_O)	R_L = 50Ω 1/		±180	±200		•	•		mA
Current, pulse (I_{OP})	R_L = 50Ω 2/		±180	±200		•	•		mA
Resistance (R_O)	Open-loop, DC			75	150		•	•	Ω
Short Circuit Current (I_{OS})	To ground only, t_{MAX} = 1sec 3/			250	300		•	•	mA
DYNAMIC RESPONSE									
Settling Time, ±0.01% 4/ (t_S)	ΔV_O = 10V	T_A = 25°C		115	125		125	150	nsec
		T_A = -25°C to +85°C					135	165	nsec
		T_A = -55°C to +125°C		125	140			175	nsec
±0.1%	ΔV_O = 20V	T_A = +25°C		105	130		•	•	nsec
	ΔV_O = 10V	T_A = +25°C		80	105		•	•	nsec
±1%	ΔV_O = 20V	T_A = +25°C		80	105		•	•	nsec
	ΔV_O = 5V	T_A = +25°C		55	75		•	•	nsec
Post Settling Time Stability (t_S+) 5/	±0.01%	t = 1μsec to 500msec		0.5	1		•	•	mV
Gain-Bandwidth Product (open-loop) (GBP)	C_C = 0pF, G = 1 V/V	T_A = +25°C		150			•		MHz
	C_C = 0pF, G = 10V/V	T_A = +25°C		500			•		MHz
	C_C = 0pF, G = 100V/V	T_A = +25°C		1.5			•		GHz
	C_C = 0pF, G = 1000V/V	T_A = +25°C		5			•		GHz
	C_C = 0pF, G = 10,000V/V	T_A = +25°C		10			•		GHz
Bandwidth (BW) -3dB, small signal 6/	G = +1V/V	T_A = +25°C	100	125		•	•		MHz
	G = -1V/V	T_A = +25°C	75	90		•	•		MHz
	G = -1V/V	T_A = -55°C to +125°C	70	90	135	•	•		MHz
	G = -10V/V	T_A = +25°C	80	95		•	•		MHz
	G = -10V/V	T_A = -55°C to +125°C	70	95	135	•	•		MHz
	G = -100V/V	T_A = +25°C	15	20		•	•		MHz
	G = -1000V/V	T_A = +25°C	5	6		•	•		MHz
Full Power Bandwidth (BW_{FP})	V_O = ±5V, G = -1V/V, C_C = 3.3pF, R_L = 100Ω	T_A = +25°C	13	16		•	•		MHz
Slew Rate (SR)	V_O = ±5V, G = 1000V/V, C_C = 0pF, R_L = 100Ω	T_A = +25°C, ΔV_o = 10V		500			•		V/μsec
	V_O = ±5V, G = -1V/V	T_A = +25°C, ΔV_o = 10V	400	440		•	•		V/μsec
	4/	T_A = -55°C to +125°C	350			•			V/μsec
Phase Margin	G = -1V/V, C_C = 3.3pF	T_A = +25°C		40			•		Degrees
GAIN									
Open-Loop Voltage Gain (A_{VS})	f = D.C., R_L = 2kΩ	T_A = +25°C	86	94		•	•		dB
		T_A = -55°C to +125°C	74			•			dB
INPUT									
Offset Voltage (V_{IO}) 7/		T_A = +25°C		1	4		2	5	mV
		T_A = -25°C to +85°C						10	mV
		T_A = -55°C to +125°C			6			15	mV
Offset Voltage vs Temperature (DV_{IO})		T_A = -25°C to +25°C					50	80	μV/°C
		T_A +25°C to +85°C					25	80	μV/°C
		T_A = -55°C to +25°C		10	20			100	μV/°C
		T_A = +25°C to +125°C		10	20			100	μV/°C
Bias Current (I_{IB})		T_A = +25°C	0	-20	-100	•	•	•	pA
		T_A = +25°C to +125°C	0	-20	-100	•	•	•	nA
Offset Current (I_{IO})		T_A = +25°C		20	50		•	•	pA
		T_A = -55°C to +125°C		20	50		•	•	nA

TABLE I. Electrical Performance Characteristics (cont)

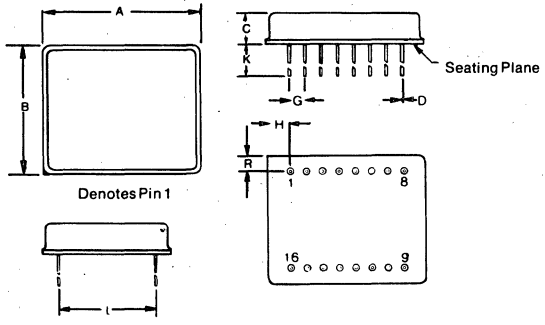
All characteristics from -55°C ≤ T_A ≤ +125°C, ±V_{CC} = 15VDC, unless otherwise noted.

		OPA600VM/883B OPA600VM			OPA600UM/883B OPA600UM			
CHARACTERISTICS	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply Rejection Ratio (PSRR)	V_{CC} = ±15V, ±1V T_A = +25°C		200	500		•	•	µV/V
Common-Mode Voltage Range (CMV)	T_A = +25°C	-10		+7	•		•	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = -5V to +5V T_A = +25°C	60	80		•	•		dB
Impedance (Z_{IN})	Differential T_A = +25°C		10^{11} ‖ 2			•		Ω ‖ pF
	Common-mode T_A = +25°C		10^{11} ‖ 2			•		Ω ‖ pF
Voltage Noise (e_n)	f = 10kHz T_A = +25°C		20			•		$nV/\sqrt{Hz}$
POWER SUPPLY								
Rated (V_{CC})			±15			•		VDC
Operating Range (V_{CC})		±9		±16	•		•	VDC
Quiescent Current (I_Q)			±30	±38		•	•	mA
TEMPERATURE RANGE (ambient)								
Operating		-55		+125	-55		+125	°C
Storage		-65		+150	-65		+150	°C
θ_{JC} (junction to case)	See applications information							
θ_{CA} (case to ambient)			35			•		°C/W

*Specifications the same as V grade.

NOTES:

1/ Pin 9 connected to +V_{CC}, pin 7 connected to -V_{CC}. Observe power dissipation ratings.
2/ Pin 9 and pin 7 open. Single pulse t = 100nsec. Observe power dissipation ratings.
3/ Pin 9 and pin 7 open. See paragraph 8.8.
4/ G = −1V/V. Optimum settling time and slew rate achieved by individually compensating each device. Refer to paragraph 8.3.
5/ Post settling time stability is a measure of the pulse droop, or thermal tail, after the output has settled.
6/ Compensation per paragraph 8.3.
7/ Adjustable to zero.



NOTES:
1. Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
2. Pin numbers shown for reference only.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.963	.980	24.46	24.89
B	.760	.805	19.30	20.45
C	.175	.190	4.45	4.83
D	.014	.022	0.36	0.56
G	.100 BASIC		2.54 BASIC	
H	.135	.155	3.43	3.94
K	.230	.270	5.84	6.86
L	.600 BASIC		15.24 BASIC	
R	.095	.115	2.41	2.92

FIGURE 5. Case Outline.

TABLE II. Electrical Test Requirements.
(The individual tests within the subgroups appear in Table III)

MODELS	OPA600VM/883B OPA600VM	OPA600UM/883B OPA600UM
MIL-STD-883 TEST REQUIREMENT	Subgroups (see Table III)	
Interim electrical parameters (pre burn-in)(method 5008)	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4, 7, 9	1*, 2, 2U, 3, 3U, 4, 7, 9
Group A test requirements (method 5008)	1, 2, 3, 4, 7, 9	1, 2, 2U, 3, 3U, 4, 7, 9
Group C end point electrical parameters (method 5008)	1	1
Additional electrical subgroups performed prior to Group C inspections	10, 11	10, 11

*PDA applies to subgroup 1 (see 4.3.d)

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS $\pm V_{CC}$ = 15V, unless otherwise specified	LIMITS OPA600VM/883B OPA600VM MIN	LIMITS OPA600VM/883B OPA600VM MAX	LIMITS OPA600UM/883B OPA600UM MIN	LIMITS OPA600UM/883B OPA600UM MAX	UNITS
1	V_{IO}	4001	V_{CM} = 0	-4	+4	-5	+5	mV
T_A = +25°C	I_{IB}	4001	V_{CM} = 0	0	-100	0	-100	pA
	+PSRR	4003	+V_{CC} = 15V, ±1V, -V_{CC} = 15V	-500	+500	-500	+500	µV/V
	-PSRR	4003	+V_{CC} = 15V, -V_{CC} = 15V, ±1V	-500	+500	-500	+500	µV/V
	CMR	4003	V_{CM} = -5V to +5V	60		60		dB
	I_Q	4005			38		38	mA
2	V_{IO}	4001		-6	+6	-15	+15V	mV
T_A = +125°C	DV_{IO}	4001	$\frac{V_{IO}\ (+25°C) - V_{IO}\ (+125°C)}{100°C}$	-20	+20	-100	+100	µV/°C
2U	V_{IO}	4001				-10	+10	mV
T_A = +85°C	DV_{IO}	4001	$\frac{V_{IO}\ (+25°C) - V_{IO}\ (+85°C)}{60°C}$			-80	+80	µV/°C
3	V_{IO}	4001		-6	+6	-13	+13	mV
T_A = -55°C	DV_{IO}	4001	$\frac{V_{IO}\ (+25°C) - V_{IO}\ (-55°C)}{80°C}$	-20	+20	-100	+100	µV/°C
3U	DV_{IO}	4001	$\frac{V_{IO}\ (+25°C) - V_{IO}\ (-25°C)}{50°C}$			-9	+9	mV
T_A = -25°C						-80	+80	µV/°C
4	V_O	4004	R_L = 2kΩ	±10		±10		V
T_A = +25°C	I_O	4004	R_L = 50Ω, pin 9 to +V_{CC}, pin 7 to -V_{CC}	±180		±180		mA
	Avs	4004	R_L = 2kΩ, f = 0Hz, V_O = ±10V	86		86		dB
7	V_O	4004	R_L = 2kΩ, ±V_{CC} = 16VDC	±11		±11		V
T_A = +25°C	V_O	4004	R_L = 2kΩ, ±V_{CC} = 12VDC	±7		±7		V
9	ts 1/	4002	To ±0.01%, Figure 10 final value at t = 1µsec		125		150	nsec
T_A = +25°C	SR 1/	4002	G = -1, V_O = ±5V, Figure 10 10% to 90%	400		400		V/µsec
10	ts 1/	4002	To ±0.01%, Figure 10 G = -1, V_o = ±5V		140			nsec
T_A = +125°C								
11	ts 1/	4002	To ±0.01%, Figure 10 G = -1, V_o = ±5V		140			nsec
T_A = -55°C								

NOTE:

1/ G = −1V/V. Optimum settling time and slew rate achieved by individually compensating each device. Refer to paragraph 8.3

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specified by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, the /883B Hi-Rel product designation, is in accordance with MIL-STD-883B, method 5008, class B, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition B, Y_1 axis only.

b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Burn-in test (MIL-STD-883, method 1015) conditions:

(1) Test condition B

(2) Test circuit is Figure 6 herein

(3) T_A = +125°C minimum

(4) Test duration is 160 hours minimum

d. Percent defective allowable (PDA). The PDA, for /883B Hi-Rel product designation only, is 10 percent and includes both parametric and catastropic failures. It is based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

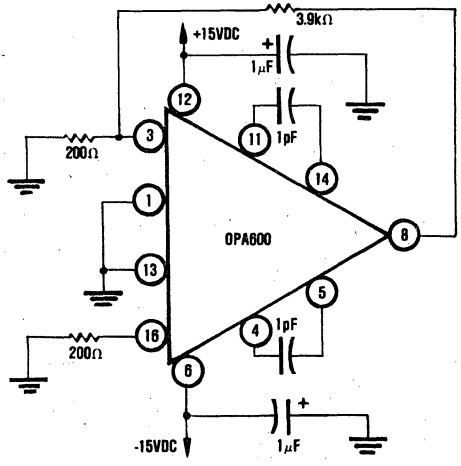


FIGURE 6. Test Circuit Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, are performed as required by MIL-STD-883.

A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 6 herein
   (3) T_A = 125°C minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of packaging. Inspection of packaging shall be as specified in MIL-M-38510.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:
a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

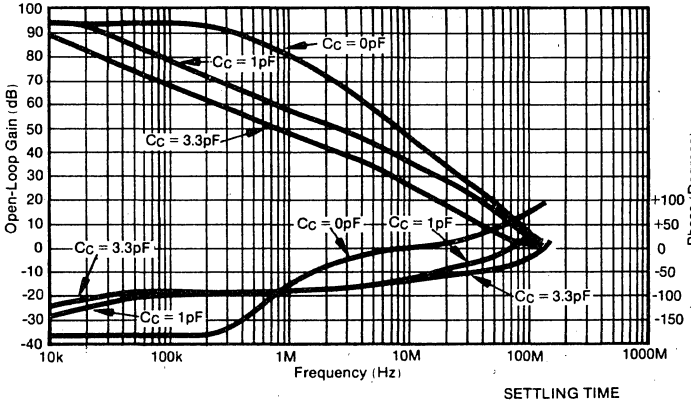
6.4 Microcircuit group assignment. These mircocircuits are assigned to Technology Group I as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

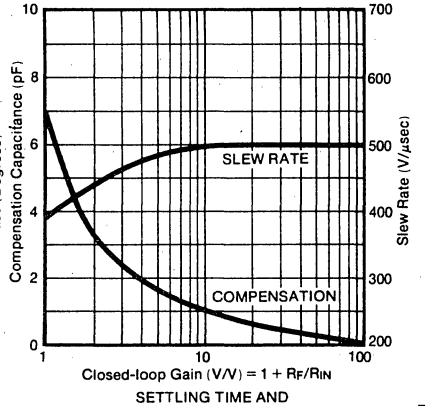
7. ELECTRICAL PERFORMANCE CURVES

(Typical at T_A = +25°C and ±V_{CC} = 15VDC, unless otherwise specified).

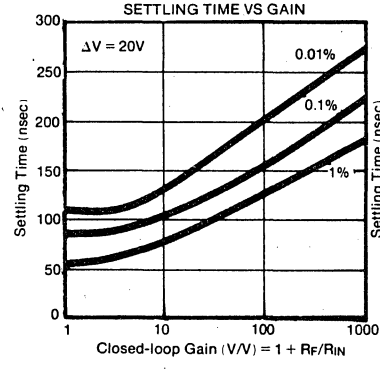
BODE PLOT



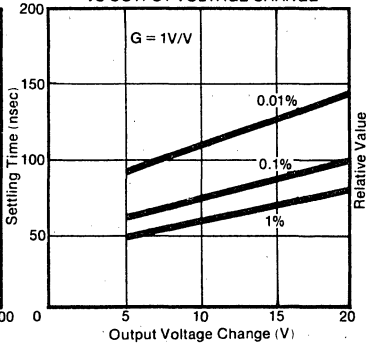
COMPENSATION AND SLEW RATE VS GAIN



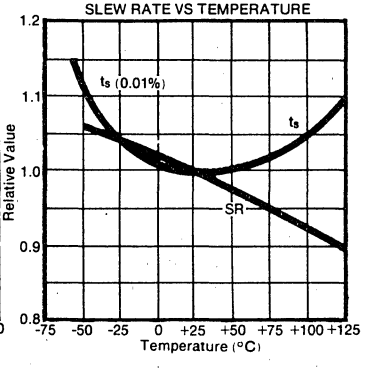
SETTLING TIME VS GAIN

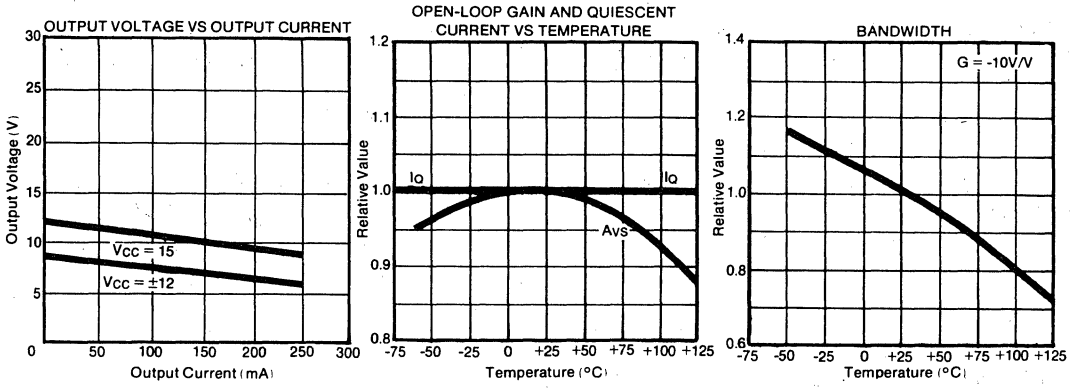


SETTLING TIME VS OUTPUT VOLTAGE CHANGE



SETTLING TIME AND SLEW RATE VS TEMPERATURE





8. APPLICATIONS INFORMATION

8.1 Wiring precautions. The OPA600 is a wideband, high frequency operational amplifier with a gain-bandwidth product exceeding 5GHz. This capability can be realized by observing a few wiring precautions and using high frequency layout techniques. Of all the wiring precautions, grounding is the most important and is described in detail in the next section.

In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths and should be as short as possible. The entire physical circuit should be as small as is practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the input terminals of the amplifier and compensation pins. Stray signal coupling from the output to the input should be minimized. All circuit element leads should be as short as possible and low values of resistance should be used. This will give the best circuit performance as it will minimize the time constants formed with the circuit capacitances and will eliminate stray, unwanted tuned circuits.

8.2 Grounding. Grounding is the most important applications consideration for the OPA600, as it is with all high frequency circuits. Ultra-high frequency transistors are used in the design of the OPA600 and oscillations at frequencies of 500MHz and above can be stimulated if good grounding techniques are not used. A ground plane is highly recommended. It should connect all areas of the pattern side of the printed circuit that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pickup. It eliminates parasitic circuits from what would otherwise be long, component leads.

Point-to-point wiring is not recommended. However, if point-to-point wiring is used, a single-point ground should be used. The input signal return, the load signal return and the power supply common should all be connected at the same physical point. This eliminates common current paths or ground loops which can cause unwanted feedback.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A 1μF CS13 tantalum capacitor is recommended. A parallel 0.01μF ceramic may be added if desired. This is especially important when driving high current loads. Properly bypassed and modulation free power supply lines allow full amplifier output and optimum settling time performance.

OPA600 circuit common is connected to pins 1 and 13; these pins should be connected to the ground plane. The input signal return, load return, and power supply common should also be connected to the ground plane.

The case of the OPA600 is internally connected to circuit common, and as indicated above, pins 1 and 13 should be connected to the ground plane. Ideally, the case should be mechanically connected to the ground plane for good thermal transfer but because this is difficult in practice, the OPA600 should be fully inserted into the printed circuit board with the case very close to the ground plane to make the best possible thermal connection. If the case and ground plane are physically connected or are in close thermal proximity, the ground plane will provide heat sinking which will reduce the case temperature rise. The minimum OPA600 pin length will minimize lead inductance, thereby maximizing performance.

To repeat, proper grounding is the single most important aspect of high frequency circuitry.

8.3 Compensation. The OPA600 uses external frequency compensation so that the user may optimize the bandwidth or settling time for his particular application. Several performance curves aid in the selection of the correct compensations capacitance value. The Bode plot shows amplitude and phase versus frequency for several values of compensation. A

related curve shows the recommended compensation capacitance versus closed-loop gain.

Figure 4 shows a recommended circuit schematic. Component values and compensation for amplifiers with several different closed-loop gains are shown. This circuit will yield the specified settling time. Because each device is unique and slightly different, as is each user's circuit, optimum settling time will be achieved by individually compensating each device in its own circuit, if desired. A 10% to 20% improvement in settling time has been experienced from the values indicated in Table I.

The primary compensation capacitors are C_1 and C_2 (see Figure 4). They are connected between pins 4 and 5 and between pins 11 and 14. Both C_1 and C_2 should be the same value. As Figure 4 and the performance curves show, larger closed-loop configurations require less capacitance and improved gain-bandwidth product can be realized. Note that no compensation capacitor is required for closed-loop gains equal to or above 100V/V. If upon initial application the user's circuit is unstable, and remains so after checking for proper bypassing, grounding, etc., it may be necessary to increase the compensation slightly to eliminate oscillations. Do not over compensate. It should not be necessary to increase C_1 and C_2 beyond 10pF to 15pF. It may also be necessary to individually optimize C_1 and C_2 for improved performance.

The flat high frequency response of the OPA600 is preserved and high frequency peaking is minimized by connecting a small capacitor in parallel with the feedback resistor (see Figure 4). This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. It will typically be 2pF for a clean layout using low resistances (1kΩ) and up to 10pF for circuits using larger resistances. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator is recommended to avoid using a large value resistor with its long time constant.

For heavy capacitive loads, greater than 50pF, refer to the section on capacitive loads, paragraph 8.6. For particularly difficult applications where the wiring layout may not be the best or where there may be 1000pF loads, parasitics, strays, long lead lengths, changing capacitive loads, etc., doublet compensation is recommended. This is discussed in paragraph 8.12 and is shown in Figure 9. This circuit offers increased stability at the expense of increasing the settling time by approximately 50%. Also, this circuit is especially useful for functional testing at low frequency and incoming inspection.

8.4 Settling time. Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition.

Settling time is a complete dynamic measure of the OPA600's total performance. It includes the slew rate time, a large signal dynamic parameter, and the time to accurately reach the final value, a small signal parameter that is a function of bandwidth and open-loop gain. Performance curves show the OPA600 settling time to ±1%, ±0.1%, and ±0.01%. The best settling time is achieved in low closed-loop gain circuits.

Settling time is dependent upon compensation. Under-compensation will result in small phase margin, overshoot or instability. Over-compensation will result in poor settling time. Refer to paragraph 8.3.

Figure 4 shows the recommended compensation to yield the specified settling tine. Improved or optimum settling time may be achieved by individually compensating each device in the user's circuit since individual devices vary slightly from one to another as do user's circuits.

8.5 Slew rate. Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed-loop gain or the small signal bandwidth. Slew rate is dependent upon compensation and decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve.

8.6 Capacitive loads. The OPA600 will drive large capacitive loads (up to 100pF) when properly compensated and settling times of under 150nsec are achievable. The effect of a capacitive load is to decrease the phase margin of the amplifier which may cause high frequency peaking or oscillations. A solution is to increase the compensation capacitance, somewhat slowing the amplifier's ability to respond. The recommended compensation capacitance value as a function of load capacitance is shown in Figure 7. (Use two capacitors, each with the value indicated.) Alternately, without increasing the OPA600's compensation capacitance, the capacitive load may be buffered by connecting a small resistance, usually 5Ω to 50Ω, in series with the Output, pin 8.

For very-large capacitive loads, greater than 100pF, it will be necessary to use doublet compensation. Refer to Figure 9 and paragraph 8.12. This places the dominant pole at the input stage. Settling time will be approximately 50% slower; slew rate should increase. Load capacitance should be minimized for optimum high frequency performance.

Because of its large output capability, the OPA600 is particularly well suited for driving loads via coaxial cables. Note that the capacitance of coaxial cable (29pF/foot of length for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

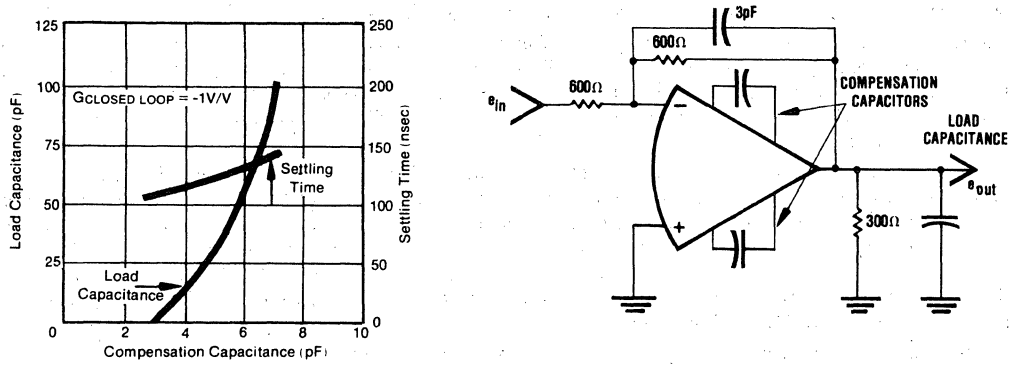


FIGURE 7. Capacitive Load Compensation and Response.

8.7 Offset voltage adjustment. The offset voltage of the OPA600 may be adjusted to zero by connecting a 5kΩ resistor in series with a 10kΩ linear potentiometer in series with another 5kΩ resistor between pins 2 and 15, as shown in Figure 3. It is important that one end of each of the two resistors be located very close to pins 2 and 15 to isolate and avoid loading these sensitive terminals. The potentiometer should be a small, noninductive type with the wiper connected to the positive supply. The leads connecting these components should be short, no longer than 0.5-inch, to avoid stray capacitance and stray signal pick-up. If the potentiometer must be located away from the immediate vicinity of the OPA600, extreme care must be observed with the sensitive leads. Locate the two 5kΩ resistors very close to pins 2 and 15.

Never connect $+V_{CC}$ directly to pin 2 or 15. Do not attempt to eliminate the 5kΩ resistors because at extreme rotation, the potentiometer will directly connect $+V_{CC}$ to pin 2 or pin 15 and permanent damage will result.

Offset voltage adjustment is optional. The potentiometer and two resistors are omitted when the offset voltage is considered sufficiently low for the particular application. For each microvolt of offset voltage adjusted, the offset voltage temperature sensitivity will change by $\pm 0.004 \mu V/°C$.

8.8 Current boost. External ability to bypass the internal current limiting resistors has been provided in the OPA600. This is referred to as current boost. Current boost enables the OPA600 to deliver large currents into heavy loads (±200mA at ±10V). To bypass the resistors and activate the current boost, connect pin 7 to $-V_{CC}$ at pin 6 with a short lead to minimize lead inductance and connect pin 9 to $+V_{CC}$ at pin 12 with a short lead.

CAUTION - Activating current boost by bypassing the internal current limiting resistors can permanently damage the OPA600 under fault conditions. See paragraph 8.9.

Not activating current boost is especially useful for initial breadboarding. The 50Ω (±5%) current limiting resistor in the collector circuit of each of the output transistors causes the output transistors to saturate; this limits the power dissipation in the output stage in case of a fault. Operating with the current boost not activated may also be desirable with small-signal outputs (i.e.±1V) or when the load current is small.

Each resistor is internally capacitively-bypassed ($0.01 \mu F$, ±20%) to allow the amplifier to deliver large pulses of current, such as to charge diode junctions or circuit capacitances and still respond quickly. The length of time that the OPA600 can deliver these current pulses is limited by the RC time constant.

The internal voltage drops, output voltage available, power dissipation, and maximum output current can be determined for the user's application by knowing the load resistance and computing:

$$V_{OUT} = 14 \left(\frac{R_{LOAD}}{50 + R_{LOAD}} \right)$$

This applies for R_{LOAD} less than 100Ω and the current boost not activated. When R_{LOAD} is large, the peak output voltage is typically ±11V, which is determined by other factors within the OPA600.

8.9 Short circuit protection. The OPA600 is a short-circuit-protected for momentary short to common (<5sec), typical of those encountered when probing a circuit during experimental breadboarding or troubleshooting. This is true only if pins 7 and 9 are open (current boost not activated). An internal 50Ω resistor is in series with the collector of each of the output transistors which under fault conditions will cause the output transistors to saturate and limit the power dissipation in the output stage. Extended application of an output short can damage the amplifier due to excessive power dissipation.

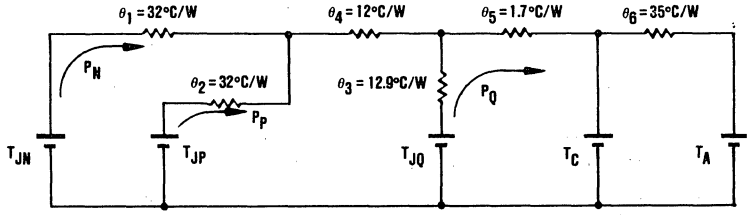
The OPA600 is not short-circuit-protected when the current boost is activated. The large output current capability of the OPA600 will cause excessive power dissipation and permanent damage will result even for momentary shorts to ground.

Output shorts to either supply will generally destroy the OPA600 whether the current boost is activated or not.

8.10 Heat sinking and power dissipation. The OPA600 is intended as a printed circuit board mounted device and as such, does not require a heat sink. It is specified for ambient temperature operation from -55°C to +125°C. However, the power dissipation must be kept within safe limits. At extreme temperature and under full load conditions, some form of heat sinking will be necessary. The use of a heat sink, or other heat dissipating means such as proximity to the ground plane, will result in cooler operating temperatures, better temperature performance, and improved reliability.

The thermal model used to describe the OPA600 is more complete than is usual for operational amplifiers. The thermal resistances for the output stages have been separated from the thermal resistrance for the balance of the OPA600. For most monolithic op amps and hybrids, thermal properties are usually represented by one thermal resistance, θJC; and in general, that is fairly accurate because the total power dissipation is low and the heat that is generated is in one area. For packaged power transistors, thermal properties are also accurately represented by one thermal resistance, θJC; all the power is dissipated in one point source. The OPA600 op amp however, has a large power handling capability and large power dissipations occur in different locations within the amplifier under differing load conditions.

The total power dissipation within the OPA600 is the sum of all the individual sources of dissipation. By making some simplifying assumptions and neglecting second order effects, the dissipations are grouped into three sources - quiescent power, NPN output transistor power, and PNP output transistor power. Using the thermal model shown in Figure 8 and the absolute maximum junction temperature rating (derate the maximum, if desired) and solving the Thevenin equivalent simultaneous equations that result, the user can determine junction, internal substrate, and case temperatures. It will be apparent that the output stages contribute significantly to the thermal rise. Under light loading, the requirements to dissipate the generated heat are much less than the requirements to dissipate heat under full load conditions at a maximum temperature. Using this expanded thermal information allows the user to safely apply the OPA600.



T_{JN} = Junction temperature of NPN output transistor.
T_{JP} = Junction temperature of PNP output transistor.
T_{JQ} = Worst case temperature of any device in the balance of the amplifier.
T_C = Case temperature.
T_A = Ambient temperature.
θ_1, θ_2 = Thermal resistance, output transistors.
θ_3, θ_4 = Thermal resistance, substrate.
θ_5 = Thermal resistance, substrate attach and package.
θ_6 = Thermal resistance, case to ambient.
P_N = Worst case power dissipation in the NPN output transistor.
P_P = Worst case power dissipation in the PNP output transistor.
P_Q = Quiescent power dissipation.

FIGURE 8. OPA600 Thermal Model.

Below are two examples of using the thermal model.

1. Find the worst case internal junction temperature rise above ambient.

Conditions: $P_Q = 1$ W
$P_N = P_P = 0.1$ W
no heatsink

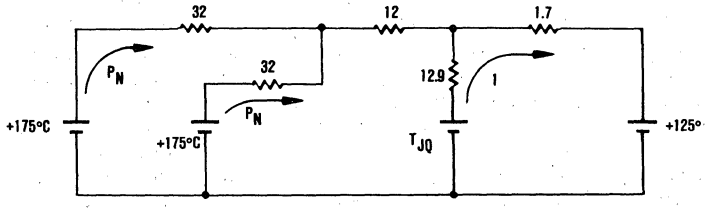
Solution: $T_{JN} = 80.7P_N + 48.7P_P + 36.7P_Q + T_A$
$T_{JN} - T_A = 49.6°C$
as $P_N = P_P$ $T_{JP} - T_A = 49.6°C$
$T_{JQ} = 49.6P_Q + 36.7P_N + 36.7P_P + T_A$
$T_{JQ} - T_A = 57°C$

Answer: 57°C

2. Find the maximum output stage power dissipation allowed with a maximum case temperature of +125°C and not exceeding the maximum junction temperature of +175°C.

Conditions: $P_Q = 1$ Watt
$P_N = P_P$

Solution:



$T_{JN} = P_N\ 32 + (P_N + P_P)12 + (P_N + P_P)\ 1.7 + P_Q\ 1.7 + T_C$
$175 = 59.4\ P_N + 1.7 + 125$
$P_N = 0.813W$

Checking T_{JQ}: $T_{JQ} = (1)\ 12.9 + (2x\ 0.813 + 1)\ 1.7 + 125$
$T_{JQ} = 142°C$ (i.e. $< 175°C$)

Answer: 0.813W may be dissipated in each output transistor.

It may be necessary to physically connect the OPA600 to the printed circuit board ground plane, attach fins, tabs, etc., to dissipate the generated heat. Because of the wide variety of possibilities, this task is left to the user. For all applications it is recommended that the OPA600 be fully inserted into the printed circuit board and that the pin length be short. Heat will be dissipated through the ground plane and the AC performance will be its best. See paragraphs 8.1 and 8.2

8.11 Testing. For static and low frequency dynamic measurements, the OPA600 may be tested in conventional operational amplifier test circuits, provided proper grounding techniques are observed, excessive lead lengths are avoided, and care is maintained to avoid parasitic oscillations. See the above sections, especially paragraphs 8.1 and 8.2. The circuit in Figure 9 is recommended for low frequency functional testing, incoming inspection, etc. This circuit is less susceptible to stray capacitance, excessive lead length, parasitic tuned circuits, changing capacitive loads, etc. It does not yield optimum settling time. We recommend placing a resistor (approximately 300Ω) in series with each piece of test equipment, such as a DVM, to isolate loading effects on the OPA600.

To realize the full performance capabilities of the OPA600, high frequency techniques must be employed and the test fixture must not limit the amplifier. Settling time is the most critical dynamic test and Figure 10 shows a recommended OPA600 settling time test circuit schematic. Good grounding, truly square drive signals, minimum stray coupling, and small physical size are important.

The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. A circuit that generates a ±5V flat topped pulse is shown in Figure 11.

Every OPA600 is thoroughly tested prior to shipment assuring the user that all parameters equal or exceed their specifications.

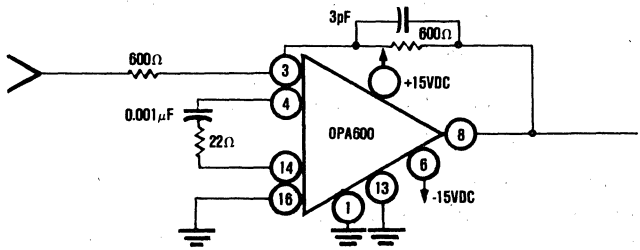


FIGURE 9. Amplifier Circuit for Increased Stability.

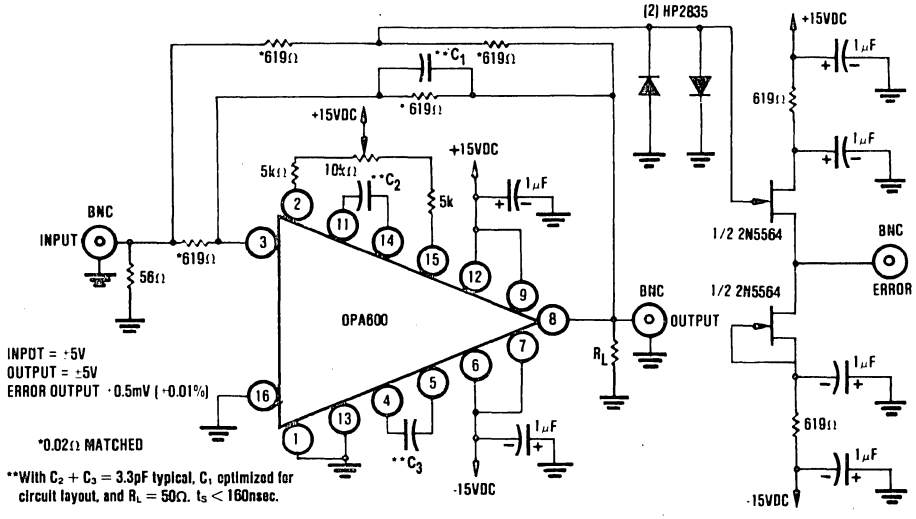


FIGURE 10. Settling Time and Slew Rate Test Circuit.

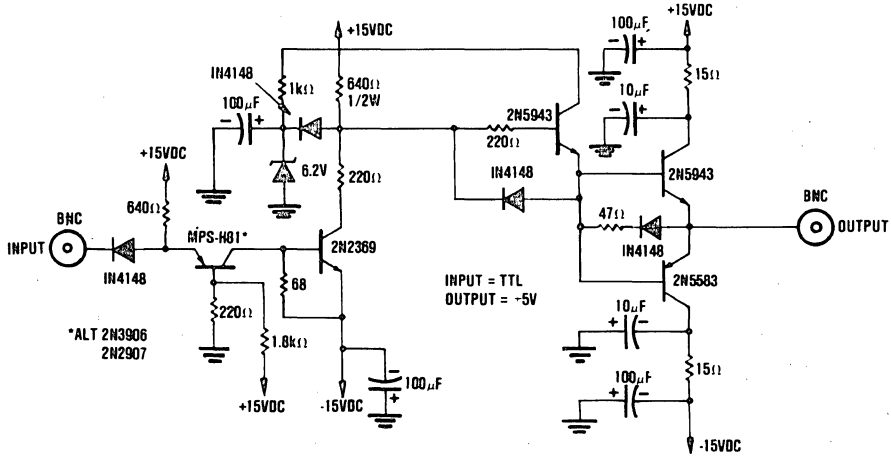


FIGURE 11. Flat Top Pulse Generator.

8.12 Increased Slew Rate. The OPA600 slew rate may be increased by using an alternate compensation shown in Figure 9. The slew rate will increase between 700 and 800V/μsec typical with 0.01% settling time increasing to between 175 and 190nsec typical and 0.1% settling time increasing to between 110 and 120nsec typical.

For alternate doublet compensation refer to Figure 9. For a closed-loop gain equal -1, delete C1 and C2 and add a series RC circuit (R = 22Ω, C = 0.001μF) between pins 14 and 4. Make no connections to pins 11 and 5. Absolutely minimize the capacitance to these pins. If a connector is used for the OPA600, it is recommended that sockets for pins 11 and 5 be removed. For a PC board mount, it is recommended that the PC board holes be overdrilled for pins 11 and 5 and adjacent ground plane copper be removed. Effectively this compensation places the dominant pole at the input stage, allowing the output stage to have no compensation and to slew as fast as possible. Bandwidth and settling time are impaired only slightly. For closed-loop gains other than -1, different values of R and C may be required.

BURR-BROWN®

OPA8780/883B SERIES

MODEL NUMBERS:

OPA8780VM/883B
OPA8780VM
OPA8780UM/883B
OPA8780UM

REVISION A
MAY, 1986

High Voltage OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT SWING, ±30V
- LARGE LOAD CURRENT, ±60mA
- DIFFICULT TO DAMAGE, automatic thermal shutoff
- REDUCES SOURCE LOADING, 100GΩ input impedance
- PRESERVES SYSTEM ACCURACY, 106db CMR, 20pA bias current
- FAST SLEWING, 15V/μsec

APPLICATIONS

- LARGE SIGNAL DRIVERS
- HIGH POWER AUDIO AMPLIFIER

DESCRIPTION

The OPA8780 is the first military version integrated circuit operational amplifier that provides high output swings up to ±30V. The monolithic FET input stage has low bias current (20pA) which minimizes the offset voltage caused by the bias current and the large resistance normally associated with high voltage circuits.

The OPA8780 is packaged in a TO-3 package which will dissipate over 3W of power without a heat sink and 4.5W with a suitable heat sink.

The input stage is protected against overvoltage and the output stage is protected against short-circuits to ground. A special thermal sensing circuit prevents damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a very-high accuracy, operational amplifier.

1.2 Part number. The complete part number is as shown below.

OPA8780	V	M	/883B
Basic model number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single operational amplifier. Two electrical performance grades are provided: the V grade (−55°C to +125°C) and U grade (−25°C to +85°C). The electrical performance characteristics are shown in Table I.

1.2.2 Device class. The device class is similar to the class B product assurance level as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels available as follows:

Hi-Rel Product Designator	Requirements
/883B	Standard model plus 100% MIL-STD-883 class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed as required by MIL-STD-883. fter.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is an 8-pin TO-3 package. Figure 1 depicts the case outline for the package.

1.2.4 Absolute maximum ratings.

Supply voltage range	±35VDC
Input voltage range	[±(V_{CC})−5]
Internal power dissipation	4.5W with heat sink
Case storage temperature range	−55°C to +150°C
Lead temperature (soldering, 60 sec.)	300°C

1.2.5 Recommended operating conditions.

Supply voltage range	±15VDC to ±35VDC
Case temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θJ−C
8-lead CAN	Figure 1	4.5W with heat sink at T_C +25°C	10°C/W with heat sink

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510—Microcircuits, general specification for.

STANDARD
MILITARY
MIL-STD-883—Test methods and procedures for microcircuits.

3. REQUIREMENTS

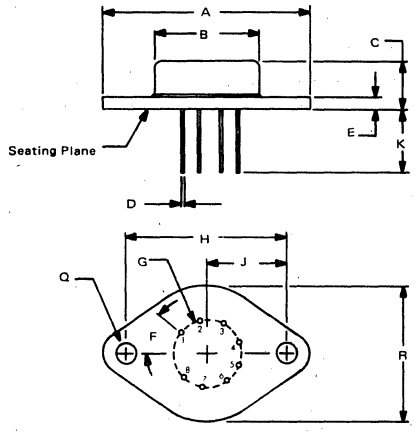
3.1. General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.340	6.60	8.64
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

FIGURE 1. Case Outline (TO-3) Package Configuration.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragrpah 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections for the TO-3 package are shown in Figure 2.

3.2.8 Glassivation. The microcircuit die are glassivated.

3.2.9 Schematics circuit. A simplified schematic circuit is shown in Figure 3.

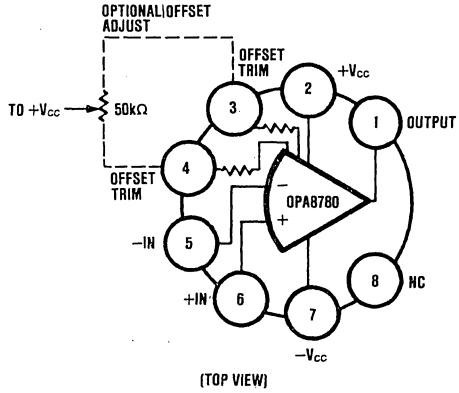


FIGURE 2. Connection Diagram.

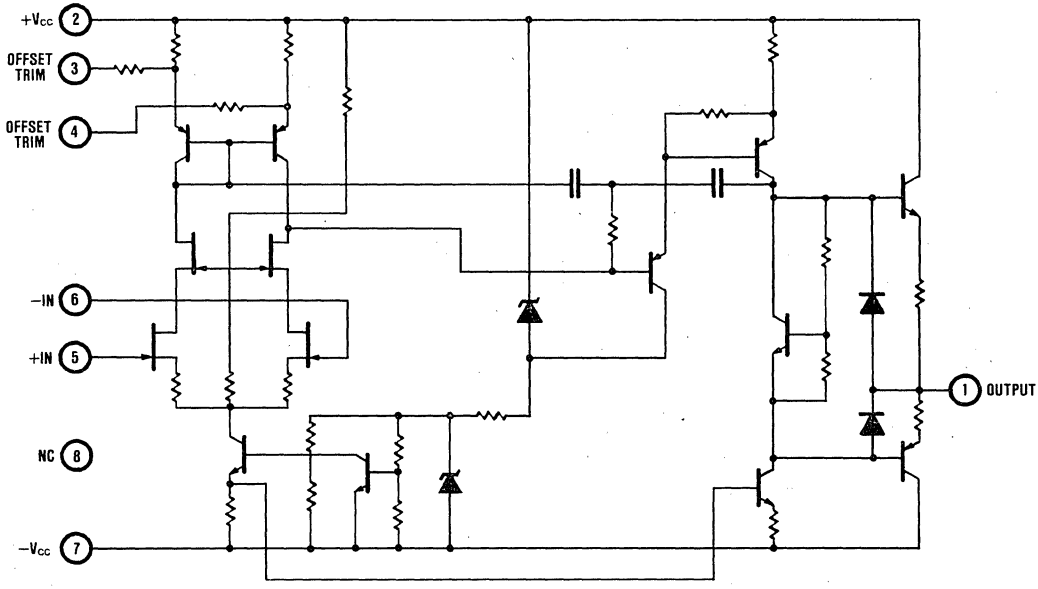


FIGURE 3. Simplified Schematic.

3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Additional electrical performance curves are shown in paragraph 7.

3.3.2 Offset null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 2. If nulling is unnecessary delete the potentiometer and make no connections.

TABLE I. Electrical Performance Characteristics.

All characteristics from −55°C ≤ T_C ≤ +125°C, ±V_{CC} = 35VDC unless otherwise noted.

CHARACTERISTICS	CONDITIONS	OPA8780VM/883B OPA8780VM			OPA8780UM/883B OPA8780UM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Voltage ±V_{CC}		±15		±35	*		*	V
Quiescent Current	T_C = +25°C			±10			*	mA
RATED OUTPUT								
Voltage (V_O)	T_C = +25°C	±10		±30	*		*	V
Current	T_C = +25°C	±60			*			mA
Current, Short Circuit		±70		±200	*		*	mA
Load Capacitance				10			*	nF
OPEN LOOP GAIN								
No Load, DC			106			*		dB
Rated Load, DC	T_C = +25°C	90			*			dB
FREQUENCY RESPONSE								
Unity Gain Bandwidth	Small Signal	5			*			MHz
Full Power Bandwidth			100			*		kHz
Slew Rate	T_C = +25°C	15	20		*	*		V/μsec
	T_C = −25°C	10	12		*	*		V/μsec
	T_C = −55°C	9	12					V/μsec
	T_C = +85°C	10	12		*	*		V/μsec
	T_C = +125°C	4	6					V/μsec
Settling Time	0.1%		12			*		μsec
INPUT OFFSET VOLTAGE								
Initial	T_C = +25°C		±1	±10			*	mV
	T_C = −55°C to +125°C			±15				mV
	T_C = −25°C to +85°C			±15			*	mV
Drift vs Temperature				30			50	μV/°C
Drift vs Supply Voltage			100			*		μV/V
Drift vs Time			100			*		μV/mo
INPUT BIAS CURRENT								
Initial	T_C = +25°C		±20	±50			*	pA
Drift vs Temperature			Doubles every 10°C			*		
Drift vs Supply Voltage			0.5			*		pA/V
INPUT OFFSET CURRENT	*							
Initial	T_C = +25°C		±20			*		pA
Drift vs Temperature			Doubles every 10°C			*		
Drift vs Supply Voltage			0.5			*		pA/V
INPUT IMPEDANCE								
Differential			100			*		GΩ
Common Mode			100			*		GΩ
INPUT NOISE								
Voltage	0.01Hz to 10Hz p-p		5			*		μV
	10Hz to 1000Hz rms		1			*		μV
Current	0.1Hz to 10Hz p-p		1			*		pA
INPUT VOLTAGE RANGE								
Max Safe Differential Voltage			$+V_{CC} + \lvert -V_{CC} \rvert$			*		V
Max Safe Common-Mode Voltage			$+V_{CC}$ to $-V_{CC}$			*		V
Common-Mode Voltage, Linear Operation			$\pm(\lvert V_{CC} \rvert - 8)$			*		V
Common-Mode Rejection			86			*		dB
TEMPERATURE RANGE [CASE]								
Operating		−55		+125	*		*	°C
Storage		−55		+150	*		*	°C
Specification		−55		+125	−25		+85	°C

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III).

MIL-STD-883 TEST REQUIREMENTS (Hybrid Class)	OPA8780VM/883B OPA8780VM	OPA8780UM/883B OPA8780UM
Interim electrical parameters (preburn-in) (method 5008)	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4, 5, 6	1, 2, 2U, 3, 3U, 4, 5, 5U, 6, 6U
Group A test requirements (method 5008)	1, 2, 3, 4, 5, 6	1, 2, 2U, 3, 3U, 4, 5, 5U, 6, 6U
Group C end point electrical parameters (method 5008)	1	1

*PDA applies to subgroup 1 (see 4.3.c)

TABLE III. Group A Inspection.

			LIMITS				
			OPA8780VM/883B OPA8780VM		OPA8780UM/883B OPA8780UM		
SUBGROUP	PARAMETERS	CONDITIONS	MIN	MAX	MIN	MAX	UNITS
1	Initial Input Offset Voltage	$T_C = +25°C$		±10		*	mV
	Quiescent Current	$T_C = +25°C$		±10		*	mA
	Initial Bias Current	$T_C = +25°C$		±50		*	pA
	Open-Loop Gain	$T_C = +25°C$, $R_L = 500\Omega$	90		*		dB
	Short-Circuit Current	$T_C = +25°C$, $R_{SC} = 10\Omega$	±70	±200	*	*	mA
2	Input Offset Voltage	$T_C = +125°C$		±15			mV
2U	Input Offset Voltage	$T_C = +85°C$		±15		*	mV
3	Input Offset Voltage	$T_C = -55°C$		±15			mV
3U	Input Offset Voltage	$T_C = -25°C$		±15		*	mV
4	Slew Rate	$T_C = +25°C$, $R_L = 500\Omega$	15		*		V/μsec
5	Slew Rate	$T_C = +125°C$, $R_L = 500\Omega$	4				V/μsec
5U	Slew Rate	$T_C = +85°C$, $R_L = 500\Omega$	10		*		V/μsec
6	Slew Rate	$T_C = -55°C$, $R_L = 500\Omega$	9				V/μsec
6U	Slew Rate	$T_C = -25°CC$, $R_L = 500\Omega$	10		*		V/μsec

*Specification is the same as for the V grade.

3.3.3 Frequency compensation. No frequency compensation is required. The amplifier is free of oscillation when operated in any gain and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

1/ A 4-digit date code, indicating year and week of seal, and a 4- or 5-digit lot identifier is marked on each unit.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /883B product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the /MIL product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for /883B Hi-Rel product designation is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), constant acceleration (condition A), temperature cycle (condition C), and external visual per MIL-STD-883, method 2009.

For the /883B product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /883B product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening for the /883B Hi-Rel product designation is in accordance with MIL-STD-883B, method 5008, class B, and is conducted on all devices. The following criteria apply:

a. Interim and final test parameters are specified in Table II.

b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 4 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

c. Percent defective allowable (PDA). The PDA, for /883B product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in are used to determine the percent defective for each manufacturing lot, and the lot is accepted or rejected based on the PDA.

d. External visual inspection need not include measurement of case and lead dimensions.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, are performed as required by MIL-STD-883.

A report of the most recent groups C and D inspections is available from Burr-Brown.
recent groups C and D inspections is available form Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B.

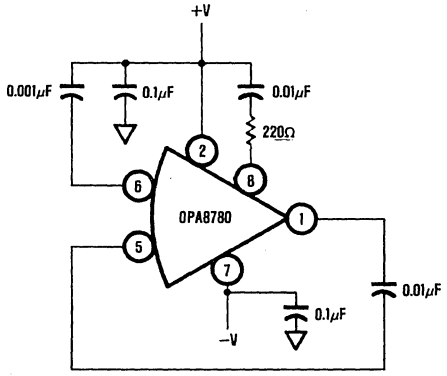


FIGURE 4. Burn-In Circuit.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 4 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage), are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is required or desirable.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

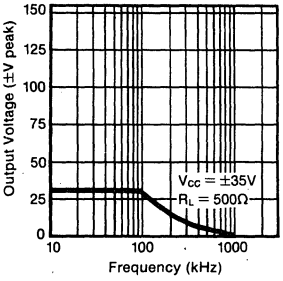
6.4. Microcircuits group assignment. These microcircuits are assigned to Technology Group I as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. CAUTION—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

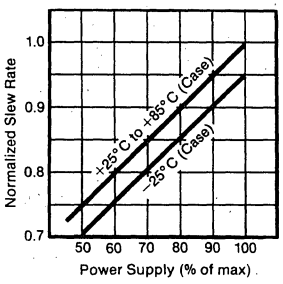
7. ELECTRICAL PERFORMANCE CURVES

T_{CASE} = +25°C and $\pm V_{CC}$ max unless otherwise noted.

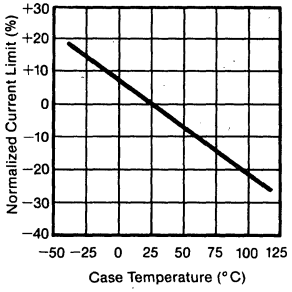
OUTPUT VOLTAGE VS FREQUENCY



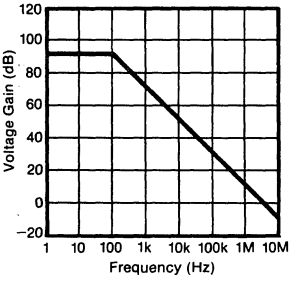
SLEW RATE VS SUPPLY VOLTAGE AT FULL LOAD



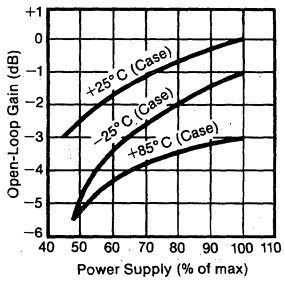
CURRENT LIMIT VS TEMPERATURE



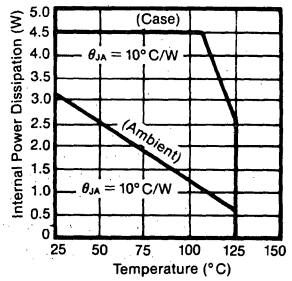
OPEN-LOOP FREQUENCY RESPONSE—FULL LOAD



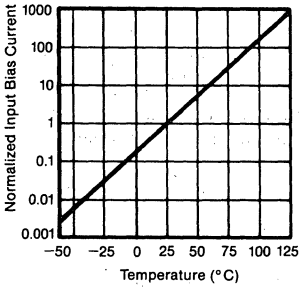
OPEN-LOOP GAIN VS SUPPLY VOLTAGE AT MAX LOAD



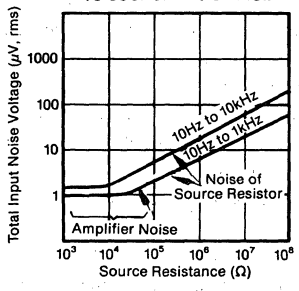
MAXIMUM POWER DISSIPATION



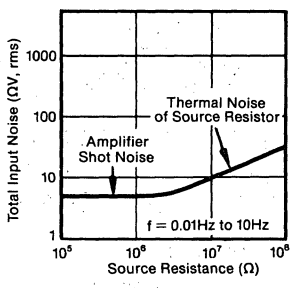
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



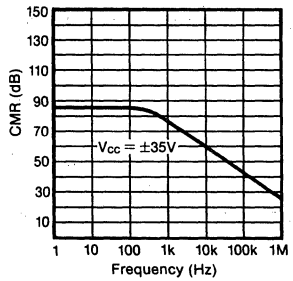
TOTAL INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



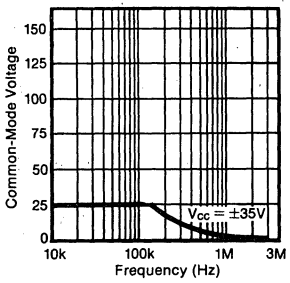
TOTAL LOW FREQUENCY INPUT NOISE VS SOURCE RESISTANCE



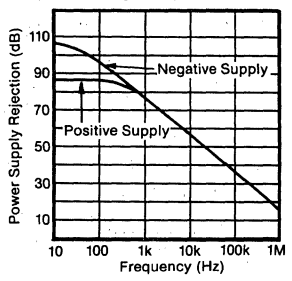
COMMON-MODE REJECTION VS FREQUENCY



MAXIMUM COMMON-MODE VOLTAGE VS FREQUENCY



POWER SUPPLY REJECTION VS FREQUENCY



8. APPLICATION INFORMATION

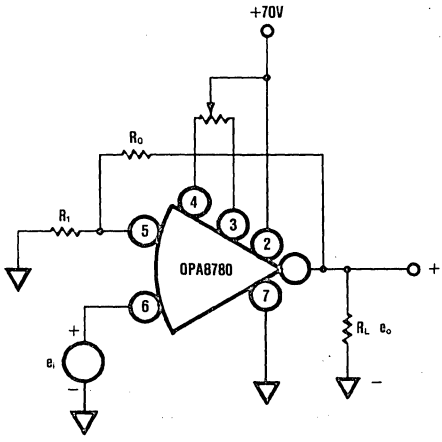
8.1 Offset voltage adjustment. If offset adjustment is necessary this may be done as indicated in Figure 2, by adding a 100kΩ potentiometer between pins 3 and 4 with the center tap connected to $+V_{CC}$.

8.2 Case connection. The case is electrically isolated. It is recommended that the case be grounded during use.

8.3 Single supply operation. It may be desirable in some applications to operate the amplifiers from a single supply. The circuit in Figure 5 illustrates a typical application.

Note that there are restrictions on the input and output voltages (e_i and e_o) which are necessary in order to keep the amplifier circuits operating in a linear manner.

It should also be noted that the OPA8780 is short-circuit limited, thermally protected, and protected from short circuits to ground.



$$e_o = e_i \left(\frac{R_O + R_I}{R_I} \right)$$

$+10V \leq e_i \leq +70V$
$+5V \leq e_o \leq +70V$

FIGURE 5. Operation From a Single Supply.

BURR-BROWN®

OPA8785/883B SERIES

OPA8785VM/883B **OPA8785UM/883B**
OPA8785VM **OPA8785UM**

ADVANCE INFORMATION
Subject to Change
Revision B, May 1986

High Current, High Power Military OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE, ±10V to ±40V
- HIGH OUTPUT CURRENT, ±10A Peak
- HIGH OUTPUT POWER, 260W Peak
- LOW DC THERMAL IMPEDANCE: 2.2°C/W
- MIL-STD-883 SCREENING

DESCRIPTION

The OPA8785 is a high power operational amplifier. Its high current output stage delivers ±10A, yet the amplifier is unity-gain stable and it can be used in any operational amplifier configuration. The 260W peak output capability allows the OPA8785 to drive loads (such as motors) with a greater safety margin.

Safe operating area is fully specified and output current limiting is provided to protect both the amplifier and the load from excessive current.

This hybrid IC is housed in an 8-pin hermetic TO-3 package. The electrically-isolated package allows direct mounting to chassis or heat sink without an insulating washer or spacer which would increase thermal resistance.

Two electrical performance grades are available. The premium grade operates from −55°C to +125°C and is designed for military, aerospace, and demanding industrial applications. The U grade has specifications for operation from −25°C to +85°C and from −55°C to +125°C. Applications include test equipment, shipboard, and ground support equipment where operation is normally between −25°C and +85°C and full temperature range operation must be assured.

The OPA8785/883B Series is manufactured on a Hi-Rel manufacturing line with clean room conditions which meet the requirements of MIL-STD-883.

Two product assurance levels are available: Standard and /883B. The Standard product assurance level offers Hi-Rel manufacturing where many MIL-STD-883 screens are performed routinely. The /883B product assurance level, /883B suffix, offers Hi-Rel manufacturing, 100% screening per MIL-STD-883 method 5008 and 10% PDA. Quality assurance further processes /883B devices, by performing group A and B inspections on each inspection log and groups C and D inspections as required by MIL-STD-883. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

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DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
HIGH CURRENT-HIGH POWER OPERATIONAL AMPLIFIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a high current-high power operational amplifier.

1.2 Part Number. The complete part number is as shown below.

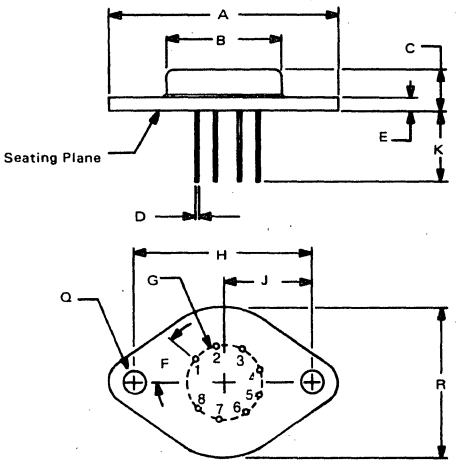
OPA8785	V	M	/883B
Basic model number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel product designator (see 1.2.1)

1.2.1 Device type. The device is a single operational amplifier. Two electrical performance grades are provided. The V grade offers performance specifications over the MIL temperature range (−55°C to +125°C) and the U grade which is specified over the industrial temperature range (−25°C to +85°C). Electrical specifications are shown in Table I and electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the class B product assurance level as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels available as follows:

Hi-Rel Product Designator	Requirements
/883B	Standard model plus 100% MIL-STD-883 class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
(none)	Standard model including 100% electrical testing.

1.2.3 Case Outline. The case outline is an 8-pin TO-3 package and is depicted in Figure 1.



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.340	6.60	8.64
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

FIGURE 1. Case Outline (TO-3) Package Configuration.

1.2.4 Absolute maximum ratings.

Supply voltage V_{CC}	±40VDC
Differential input voltage	$\pm V_{CC} - 3$
DC internal power dissipation	80W 1/
AC Internal power dissipation (10kHz, 50% duty cycle)	160W 1/
Output short circuit duration	Continuous to ground
Storage temperature range	−65°C to +165°C
Lead temperature (soldering, 60sec)	300°C
Junction temperature	$T_j = 200°C$
Common-mode input voltage	$\pm V_{CC}$

1.2.5 Recommended operating conditions.

Supply voltage range	±34VDC (see Table I)
Ambient temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θJ-C
8-lead TO-3	Figure 1	80W with heat sink	2.2°C/W with heat sink

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510—Microcircuits, general specification for.

STANDARD
MILITARY
MIL-STD-883—Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. The microcircuit dice are glassivated.

3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

1/ $T_A \leq +25°C$

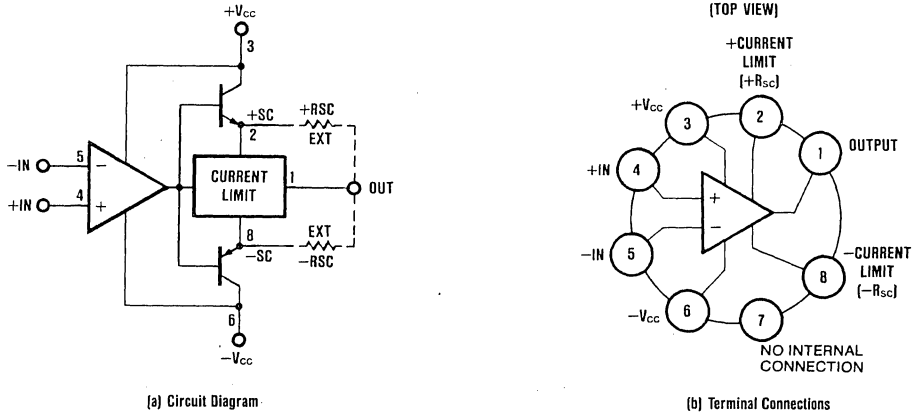


FIGURE 2. Circuit Diagram and Terminal Connections.

TABLE I. Electrical Performance Characteristics.

All characteristics at $-55°C \le T_A \le +125°C$, $\pm V_{CC} = \pm 34VDC$ unless otherwise specified.

CHARACTERISTICS	SYMBOL	CONDITIONS	OPA8785VM/883B OPA8785VM			OPA8785UM/883B OPA8785UM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
RATED OUTPUT 1/ 2/									
Output Current, Continuous 3/	I_O	$R_L = 2.6\Omega$	±10			±10			A
Output Voltage 3/	V_O	$I_O = 10A$ peak	±30			±30			V
DYNAMIC RESPONSE									
Bandwidth	BW	Unity Gain—Small Signal $T_A = +25°C$		1			*		MHz
		Full Power $V_O = 40V$ p-p, $R_L = 8\Omega$, $T_A = +25°C$	10			*			kHz
Slew Rate	SR	$R_L = 6.5\Omega$	1.5			*			V/μsec
INPUT OFFSET VOLTAGE									
Initial Offset	V_{IO}	$T_A = +25°C$			±5			±10	mV
Tempco	DV_{IO}	$[V_{IO}(T_A) - V_{IO}(+25°C)] \div \Delta T$							
		$-55 \le T_A \le +125°C$	−40		+40	−65		+65	μV/°C
		$-25 \le T_A \le +85°C$				−65		+65	μV/°C
Vs Supply Voltage	PSRR	$V_{CC} = \pm 10$, $V_{CC} = \pm 40$	−100		+100	*		*	μV/V
INPUT BIAS CURRENT									
Initial	I_{IB}	$T_A = +25°C$			+20			+40	nA
Tempco	I_{IB}	$-55 \le T_A \le +125°C$	−35		+35	−60		+60	nA
		$-25 \le T_A \le +85°C$				−50		+50	nA
Vs Supply				±0.02			±0.02		nA/V
INPUT DIFFERENCE CURRENT									
Initial	I_{IO}	$T_A = +25°C$			±3			±10	nA
Tempco	I_{IO}	$-55 \le T_A \le +125°C$			±7			±20	nA
		$-25 \le T_A \le +85°C$						±15	nA
OPEN LOOP GAIN, DC	A_{VS}	$R_L = 10k\Omega$	98			94			dB
INPUT IMPEDANCE	Z_{ID}			10			*		MΩ
	Z_{ICM}			250			*		MΩ

TABLE I. Electrical Performance Characteristics (continued).

CHARACTERISTICS	SYMBOL	CONDITIONS	OPA8785VM/883B OPA8785VM			OPA8785UM/883B OPA8785UM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE									
Voltage Noise	e_n	f_n = 0.3Hz to 10Hz		3			*		μV, p-p
		f_n = 10Hz to 10kHz		5			*		μV, rms
Current Noise	i_n	f_n = 0.3Hz to 10Hz		20			*		pA, p-p
		f_n = 10Hz to 10kHz		4.5			*		pA, rms
INPUT VOLTAGE RANGE									
Common-Mode	V_{ICM}	Linear Operation	±(|V_{CC}|−6)			*			V
Common-Mode Rejection	CMRR	F = DC, V_{ICM} = ±22V	76			70			dB
		F = DC, V_{ICM} = 22V, T_A = 25°C	80			70			dB
POWER SUPPLY									
Rated Voltage	V_{CC}			±34			*		V
Operating Voltage Range			±10		±40	*		*	V
Current, Quiescent	I_Q				±10			*	mA
TEMPERATURE RANGE									
Specification			−55		+125	−25		+85	°C
Storage			−65		+150	*		*	°C

*Specification same as OPA8785 "V" grade.

NOTES:

1/ Package must be derated based on a junction-to-case thermal resistance of 2.2°C/W or a junction-to-ambient thermal resistance of 30°C/W.

2/ Safe Operating Area and Power Derating Curves must be observed.

3/ With $\pm R_{SC} = 0$. Peak output current is typically greater than 10A if duty cycle and pulse width limitations are observed. Output current greater than 10A is not guaranteed.

3.4 Electrical test requirements. Electrical test requirements are shown in Table II. The subgroups of Table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, are specified in Table II.

TABLE II. Electrical Test Requirements.

MIL-STD-883 REQUIREMENTS (Hybrid Class)	MODELS			
	OPA8785VM/883B	OPA8785VM	OPA8785UM/883B	OPA8785UM
Interim electrical parameters (preburn-in) (method 5008)	1	1	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4, 5, 6, 7	1, 2, 3, 4, 5, 6, 7	1, 2, 3, 4, 5, 6, 7	1, 2, 3, 4, 5, 6, 7
Group A test requirements (method 5008)	1, 2, 3, 4, 5, 6, 7	—	1, 2, 3, 4, 5, 6, 7	—
Group C end point electrical parameters (method 5008)	1	—	1	—

*PDA applies to subgroup 1 for /883B Hi-Rel designator (see 4.3c).

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS ±V_{CC} = ±34VDC unless otherwise specified	LIMITS				UNITS
				OPA8785VM/883B OPA8785VM		OPA8785UM/883B OPA8785UM		
				MIN	MAX	MIN	MAX	
1	V_{IO}	4001		−5	+5	−10	+10	mV
T_A = +25°C	I_{IB+}	4001		−20	+20	−40	+40	nA
	I_{IB-}	4001		−20	+20	−40	+40	nA
	I_{IO}	4001		−3	+3	−10	+10	nA
	+PSRR	4003	$-V_{CC}$ = −34, $+V_{CC}$ = +10 to +40VDC	−100	+100	−100	+100	μV/V
	−PSRR	4003	$+V_{CC}$ = +34VDC, $-V_{CC}$ = −10 to −40VDC	−100	+100	−100	+100	μV/V
	CMRR	4003	V_{CM} = ±22V, F = DC	80		70		dB
	I_{CC+}	4005	V_{CM} = 0, no load condition		+10		+10	mA
	I_{CC-}	4005	V_{CM} = 0, no load condition	−10		−10		mA

TABLE III. Group A Inspection (continued).

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS $\pm V_{CC} = \pm 34VDC$ unless otherwise specified	LIMITS				UNITS
				OPA8785VM/883B OPA8785VM		OPA8785UM/883B OPA8785UM		
				MIN	MAX	MIN	MAX	
2	DV_{IO}	4001	$[V_{IO}\ (+125°C) - V_{IO}\ (+25°C)] \div 100$	−40	+40	−65	+65	µV/°C
$T_A = +125°C$	I_{IB+}	4001		−35	+35	−60	+60	nA
	I_{IB-}	4001		−35	+35	−60	+60	nA
	I_{IO}	4001		−7	+7	−20	+20	nA
	+PSRR	4003	$-V_{CC} = -34VDC, +V_{CC} = 10$ to 40VDC	−100	+100	−100	+100	µV/V
	−PSRR	4003	$+V_{CC} = +34VDC, -V_{CC} = -10$ to −40VDC	−100	+100	−100	+100	µV/V
	CMRR	4003	$V_{CM} = \pm 22V$, F = DC	76		70		dB
	I_{CC+}	4005	$V_{CM} = 0$, no load condition		+10		+10	mA
	I_{CC-}	4005	$V_{CM} = 0$, no load condition	−10		−10		mA
3	DV_{IO}	4001	$[V_{IO}\ (+25°C) - V_{IO}\ (-55°C)] \div 80$	−40	+40	−65	+65	µV/°C
$T_A = -55°C$	I_{IB+}	4001		−35	+35	−60	+60	nA
	I_{IB-}	4001		−35	+35	−60	+60	nA
	I_{IO}	4001		−7	+7	−20	+20	nA
	+PSRR	4003	$-V_{CC} = -34VDC, +V_{CC} = -10$ to +40VDC	−100	+100	−100	+100	µV/V
	−PSRR	4003	$+V_{CC} = +34VDC, -V_{CC} = -10$ to −40VDC	−100	+100	−100	+100	µV/V
	CMRR	4003	$V_{CM} = \pm 22V$, F = DC	76		70		dB
	I_{CC+}	4005	$V_{CM} = 0$, no load condition		+10		+10	mA
	I_{CC-}	4005	$V_{CM} = 0$, no load condition	−10		−10		mA
4	V_{OP}	4004	$I_O = 10A$ peak, 10kHz sine wave, 1sec duration	−30	+30	−30	+30	V
$T_A = +25°C$	I_{OP}	4004	$R_L = 2.6\Omega$, 10kHz sine wave, 1sec duration	−10	+10	−10	+10	A
	A_{VS}	4004	$R_L = 10k\Omega$	98		94		dB
5	V_{OP}	4004	$R_L = 10k\Omega$	−30	+30	−30	+30	V
$T_A = +125°C$	A_{VS}	4004	$R_L = 10k\Omega$	98		94		dB
6	V_{OP}	4004	$R_L = 10k\Omega$	−30	+30	−30	+30	V
$T_A = -55°C$	A_{VS}	4004	$R_L = 10k\Omega$	98		94		dB
7	SR	4002	$R_L = 6.5\Omega$	1.5		1.5		V/µsec
$T_A = +25°C$								

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum:

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin
f. Electrostatic sensitivity identifier (Δ)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /883B product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the /883B product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for /883B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, constant acceleration (condition A), temperature cycle (condition C), and external visual per MIL-STD-883, method 2009.

For the /883B product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /883B product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening for the /883B Hi-Rel product designation is in accordance with MIL-STD-883, method 5008, class B, and is conducted on all devices. The following criteria apply:

a. Interim and final test parameters are specified in Table II.
b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B or D
   (2) Test circuit is Figure 3 herein for condition B
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum
c. Percent defective allowable (PDA). The PDA, for /883B product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no

1/ A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in are used to determine the percent defective for each manufacturing lot, and the lot is accepted or rejected based on the PDA.

d. External visual inspection need not include measurement of case and lead dimensions.

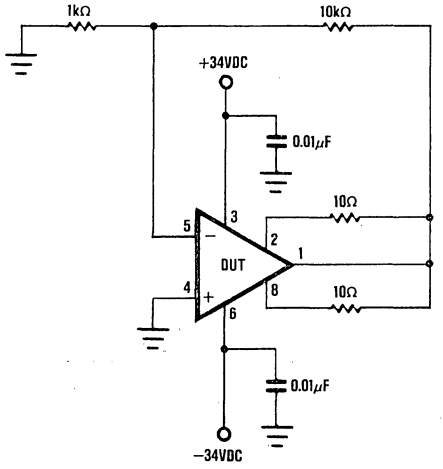


FIGURE 3. Test Circuit—Burn-in and Operating Life Test (Condition B).

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, class B, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, class B are performed as required by MIL-STD-883.

A report of the most recent group C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B or D.
   (2) Test circuit is Figure 3 herein for condition B.
   (3) $T_A = +125°C$ minimum
   (4) Test condition is 1000 hours minimum

b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 and as follows:

a. End point electrical parameters are specified in Table II herein.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is required or desirable.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

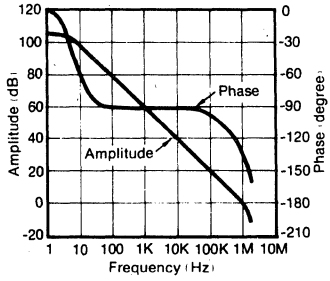
6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group I as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. CAUTION—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

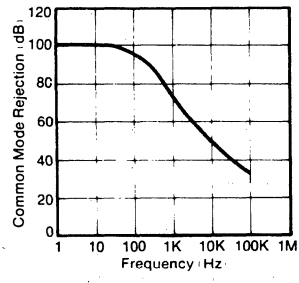
7. ELECTRICAL PERFORMANCE CURVES

(Typical at +25° case and ±V_{CC} = 28VDC unless otherwise noted.)

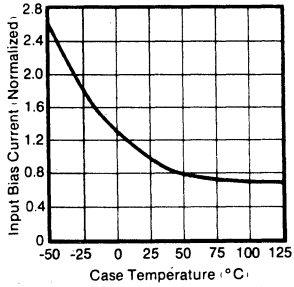
OPEN-LOOP FREQUENCY RESPONSE



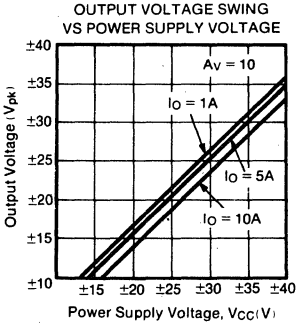
COMMON MODE REJECTION VS FREQUENCY



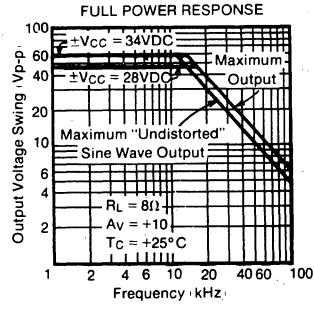
INPUT BIAS CURRENT VS TEMPERATURE



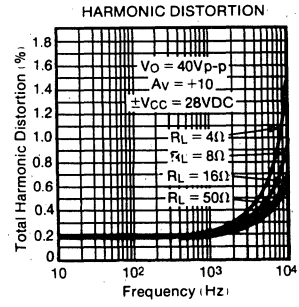
OUTPUT VOLTAGE SWING VS POWER SUPPLY VOLTAGE

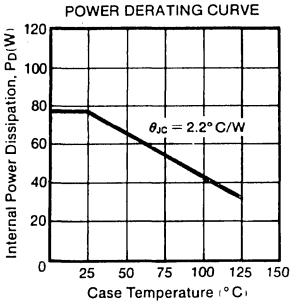


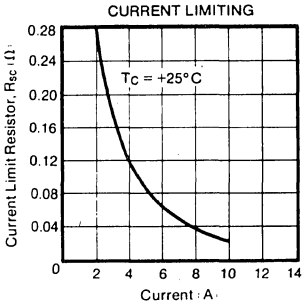
FULL POWER RESPONSE

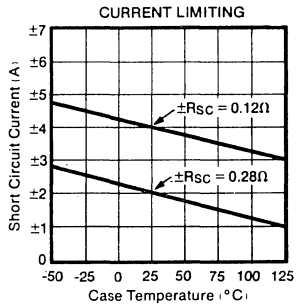


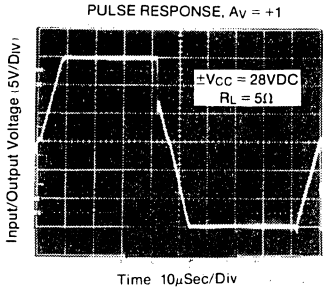
HARMONIC DISTORTION

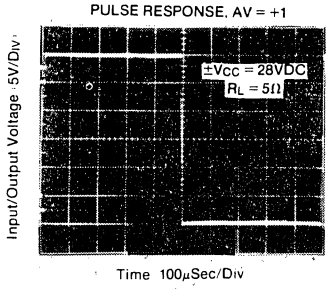












8. APPLICATION INFORMATION

8.1 Grounding. Because of the high output current capability of the OPA8785 Series, the user is cautioned to observe proper grounding techniques. Figure 4 illustrates a recommended technique.

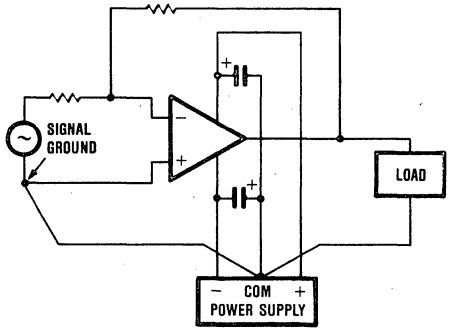


FIGURE 4. Proper Power Supply Connections.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

8.2 Supply bypassing. The OPA8785 power supplies should be bypassed with 50μF tantalum capacitors connected as close as possible to pins 3 and 6. These bypass capacitors should be connected to the load ground rather than the signal ground.

8.3 Current limits. The OPA8785 amplifier is designed so that both positive and negative load current limits can be set independently with external resistors $+R_{SC}$ and $-R_{SC}$ respectively. The approximate value of these resistors is given by the equation:

$$R_{SC} = [(0.65 \div I_{LIMIT}) - 0.0437] \text{ ohms}$$

I_{LIMIT} is the desired maximum current in amperes. The power dissipation of the current limit resistor is:

$$P_{max} = R_{SC} (I_{LIMIT})^2 \text{ watts}$$

R_{SC} is in ohms and I_{LIMIT} is in amperes.

Current limit resistors carry the full amplifier output current so lead lengths should be minimized. Highly inductive resistors can cause loop instability. Variation in limit with case temperature is shown in the Typical Performance Curves, paragraph 7.

The amplifier should be used with as low a current limit as possible for its particular application. This will minimize the change of damaging the amplifier under abnormal load conditions and will increase reliability by limiting internal power dissipation.

The current limits may be used to generate other functions such as constant current supplies and torque or stall current limits for servomotor applications.

8.4 Heat sinking. The OPA8785 requires a heat sink to limit output transistor junction temperature (T_J) to an absolute maximum of +200°C. The steady-state thermal circuit is illustrated in Figure 5.

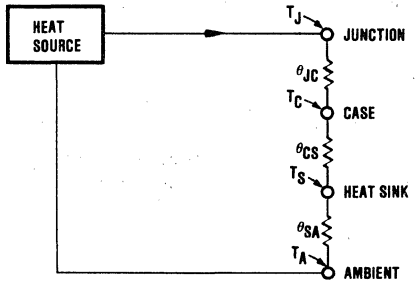


FIGURE 5. Simplified Steady-State Heat Flow Model.

Junction temperature (T_J) is found from the equation:

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$

where P_D = average amplifier power dissipation (W)
θ_{JC} = junction to case thermal resistance (°C/W)
θ_{CS} = case to sink thermal resistance (°C/W)
θ_{SA} = sink to ambient thermal resistance (°C/W)
T_A = ambient temperature (°C)

For most heat sink calculations the quiescent power dissipation is very low (<1 watt) and can be disregarded with only a small error.

The maximum size heat sink can be found as follows:

Example: Find the maximum thermal resistance (smallest heat sink) that can be used for an OPA8785 with $\pm V_{CC}$ = 28VDC. Output voltage is +10VDC across a 10Ω resistor and ambient temperature is +50°C:

$$\theta_{SA} = [(T_J - T_A) \div PD] - \theta_{CS} - \theta_{JC}$$

As large a heat sink as possible should be used. θ_{CS} depends on the flatness of the heat sink, the thermal compound used, and the roughness of the mating surfaces. Typical values are between 0.1°C/W and 0.3°C/W for a TO-3 package properly mounted on a heat sink.

The OPA8785 mounting flange is electrically-isolated and can be mounted directly to a heat sink without insulating washers or spacers.

The output transistor thermal resistance (θ_{JC}) is a function of the output current pulse width, pulse shape, and duty cycle. Long duration pulses allow the junction temperature to approach its steady state value while shorter pulses cause a lower peak junction temperature due to the junction's thermal time constant. Heat is conducted away from the junction rapidly so that as the duty cycle decreases, junction temperature decreases.

Steady state θ_{JC} is rated at 2.2°C/W maximum. In applications where the amplifier's output current alternates between output transistors—for example, an AC amplifier—the transistor θ_{JC} will depend on frequency as shown in Figure 6.

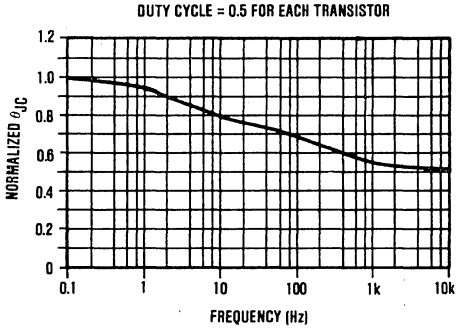


FIGURE 6. Effective θ_{JC} for Applications Where Output Current Alternates Between Output Transistors.

8.5 Safe operating area (SOA). In addition to the limits imposed by power dissipation, the amplifier's output transistors are also limited by a second breakdown region. This occurs because of increased emitter current density due to current crowding at higher operating voltages. Both the dissipation and second breakdown limits depends on time and temperature. Figure 7 shows each output transistor's SOA at a case temperature of +25°C.

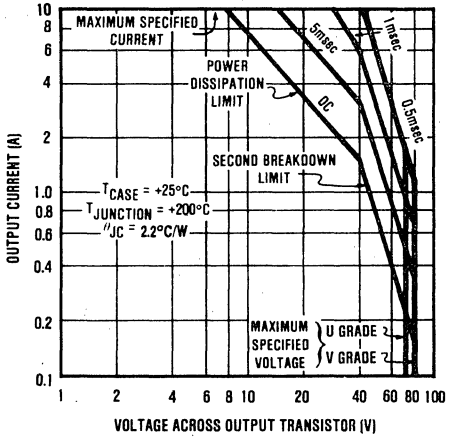


FIGURE 7. Transistor Safe Operating Area at +25°C Case Temperature.

Limits for short pulse widths are substantially greater than for steady state (DC). At a case temperature of +125°C the SOA limits are reduced (see Figure 8). The SOA shown in these curves is based on a conservative linear derating of both the power dissipation and the second breakdown region.

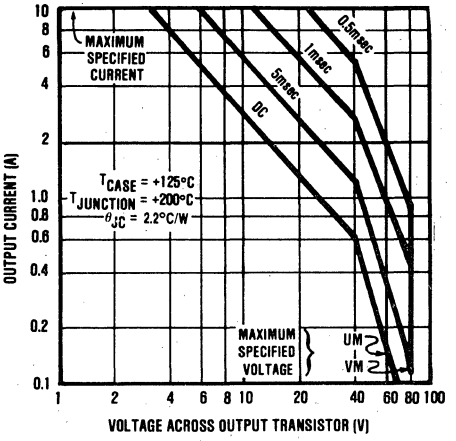


FIGURE 8. Transistor Safe Operating Area at +125°C Case Temperature.

Resistive loads are easy to analyze by simply plotting load lines on the SOA curve. If the curve representing the load line stays within the OPA8785 output transistor's SOA curve and all other parameters are observed, such as case temperature, etc., the amplifier will be safe. The load line can swing through the larger SOA limits if their time duration constraints are strictly observed.

Reactive loads present a more complex problem since the output voltage and current are not in phase. This results in the reactive load line becoming elliptical (when plotted on linear axes) which requires a larger SOA for safe operation.

Although detailed analysis is beyond the scope of this data sheet, the load line can be viewed on an oscilloscope as shown in Figure 9. The X-Y display is driven by the voltage across the load and by the current into the load. This setup can also display voltage and current stress across the OPA8785 output transistors as shown in Figure 10. This data can then be compared to the SOA limits.

The amplifier is designed to operate with electromotive force generating loads such as servomotors, relays, and actuators. Careful attention must be paid to both the load characteristics and the amplifier's SOA to ensure safe operation.

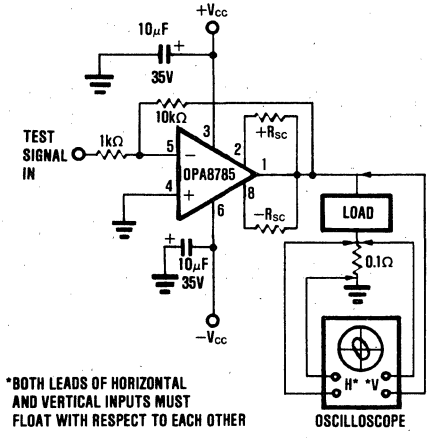


FIGURE 9. Loadline Display.

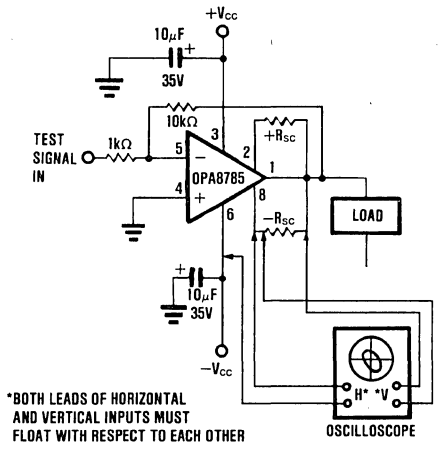


FIGURE 10. Output Transistor Safe Operating Area Stress Display.

Figure 11 shows the OPA8785 configured as a DC permanent magnet motor driver. The armature current (1A) and motor voltage (V_m) are monitored by an oscilloscope in the X-Y mode. Slewing the motor with a 4Hz sine wave results in the motor power ellipse of Figure 12. The input level has been adjusted to give ±20V, peak across the motor. An examination of the power ellipse indicates that the instantaneous power delivered to the motor exceeds the amplifier's output transistors safe operating area at a case temperature of +25°C. The point at which the motor shows 0V at −6.9A is a problem. The voltage across the output is 28V − 0V = 28V. Checking the SOA curve shows that the amplifier can safely withstand this condition for slightly under 5msec. At 4Hz this transient swing outside the DC SOA region is exceeded for much longer than 5msec. Continued operation under these conditions will result in device failure. Peak junction temperatures should not exceed +200°C. Perhaps a motor with a higher impedance winding should be considered for this application. Current limiting and lower supply voltage can also reduce dissipation.

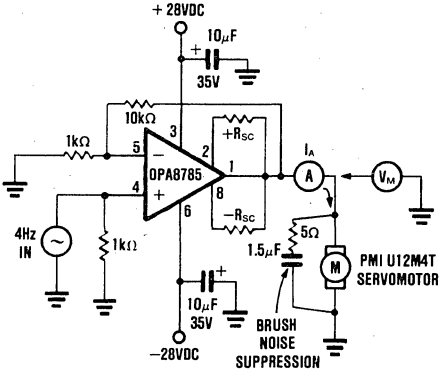


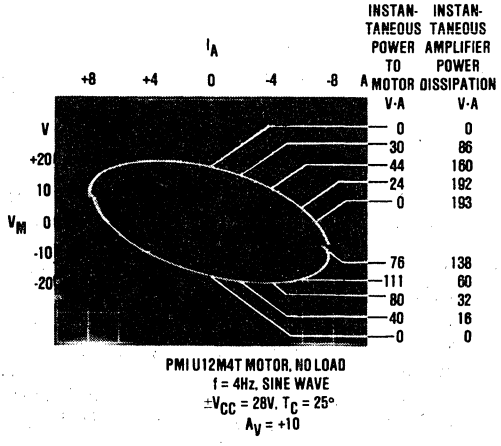
FIGURE 11. Servomotor Amplifier.

Motors used in servo applications often require a surprisingly large current to accelerate quickly. Worst-case conditions occur when the motor is operating at full speed and is suddenly slammed into reverse ("plugging"). This condition is illustrated in Figure 13 when a DC servomotor is driven by a bipolar square wave. As the motor reverses direction a large surge current flows, causing very-high peak power dissipation in the amplifier. After several time constants (determined by the inertia moment) the current drops to a lower steady-state value. Loading the motor increases the motor average power and amplifier dissipation. SOA curves should be checked for safe operation under these surge conditions.

The OPA8785 current limits may be set to clip the high surge currents to a safe level. This is shown in Figure 14. Note that the current limit does limit the servomotor peak acceleration.

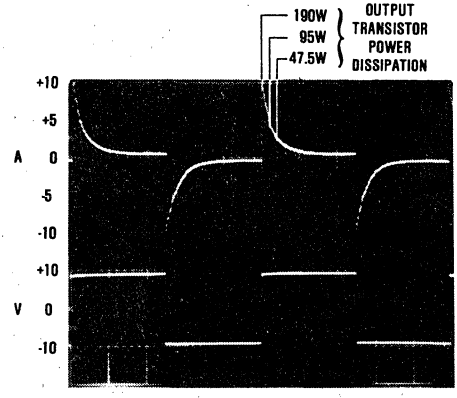
Inductive loads should be investigated for high peak transients generated by a collapsing magnetic field. Resistive damping can reduce this problem and although the amplifier has a substrate as part of the Darlington output transistor structure, external diodes are recommended for heavy clamping.

Fast diodes such as those normally used as rectifiers in switching power supplies are suitable.



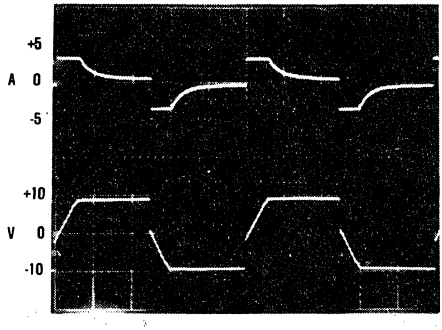
PMI U12M4T MOTOR, NO LOAD
f = 4Hz, SINE WAVE
$\pm V_{CC}$ = 28V, T_C = 25°
A_V = +10

FIGURE 12. DC Servomotor Load Line.



PMI U12M4T MOTOR, NO LOAD
f = 4Hz, SQUARE WAVE
$\pm V_{CC}$ = 28V, T_C = 25°
A_V = +10

FIGURE 13. Servomotor Drive—"Plugging"



PMI U12M4T MOTOR, NO LOAD
f = 4Hz, SQUARE WAVE
$\pm V_{CC}$ = 28VDC, $\pm R_{SC}$ = 0.15Ω
T_C = 25°, A_V = +10

FIGURE 14. Servomotor Drive With Current Limit.

BURR-BROWN®

VFC32/883B SERIES

MODEL NUMBERS:

VFC32WM/883B
VFC32WM
VFC32UM/883B
VFC32UM
VFC32VM/883B
VFC32VM

REVISION D
MAY, 1986

VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- **HIGH LINEARITY**
  - **±0.006% max (13 bits) and ±0.01% max (12 bits) at 10kHz FS**
  - **±0.05% max at 100kHz FS**
  - **±0.1% max at 200kHz FS**
- **HI-REL MANUFACTURE**
- **6-DECADE DYNAMIC RANGE**
- **OUTPUT DTL/TTL/CMOS COMPATIBLE**
- **V/F OR F/V CONVERSION**

DESCRIPTION

The VFC32 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple, low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with DTL, TTL, and CMOS logic families.

The converter requires two external resistors and two external capacitors to operate. One external resistor and one external capacitor set up the full scale frequency, with a guaranteed nonlinearity of ±0.1% maximum at 200kHz. The other capacitor is the one-shot capacitor; for best performance it should have a low temperature coefficient. The other resistor is a noncritical open collector pull-up resistor.

The VFC32/883B Series converter is available in three electrical performance grades. The V grade has 200kHz specifications and tests. The W grade has premium linearity, ±0.006% of FSR, and premium full scale accuracy temperature coefficient of 100ppm/°C.

The U grade is specified from −25°C to +85°C and from −55°C to +125°C. It is primarily for high performance test equipment, shipboard, ground support and industrial applications, where operation is normally between −25°C and +85°C and full temperature operation must be assured. All are packaged in welded, hermetically-sealed, TO-100 cans.

All devices are manufactured on a Hi-Rel manufacturing line with impeccable clean room conditions to assure "built-in" quality.

Two product assurance levels are available: standard, and /883B. The standard models have many MIL-STD-883 screens performed routinely. Each /883B suffixed device is Hi-Rel manufactured, 100% screened per MIL-STD-883 method 5004 class B, and had 5% PDA.

Quality assurance further processes /883B devices, performing group A and B inspections on each inspection lot and group C and D inspections as required by MIL-STD-883. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

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DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
VOLTAGE-TO-FREQUENCY CONVERTER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a very linear, voltage-to-frequency converter. For the description of operation see paragraph 3.3.3.

1.2 Part Number. The complete part number is as shown below.

VFC32	V	M	/883B
Basic model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, voltage-to-frequency converter; it will also function as a single, frequency-to-voltage converter. Three electrical performance grades are provided. The V grade features specifications and tests at 200kHz. The W grade features premium linearity (13 bits) and premium full scale accuracy. The U grade features specified and tested performance from -25°C to +85°C and maintains -55°C to +125°C operation.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the product assurance level class B, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance level as follows:

Hi-Rel Product Designator	Requirements
/883B	Standard Model, plus 100% MIL-STD-883 class B screening, with 5% PDA, plus quality conformance inspections (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
(none)	Standard model including 100% electrical testing.

1.2.3. Case outline. The case outline is A-2 (10-lead can, TO-100) as defined in MIL-M-38510, Appendix C. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±22VDC
Input voltage range, +input, pin 1	±22VDC 1/
Input voltage range, -input, pin 2	±22VDC 1/
Output pull-up supply voltage (V_{PU})	±22VDC 1/ 2/
Output sink current, pin 6	16mA
Comparator input voltage	±22VDC 1/
Output current pin 10	±20mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ V_{PU} is the supply voltage connected to pin 6 via R_2; see Figure 2.

1.2.5 Recommended operating conditions.

Supply voltage range	±11VDC to ±20VDC
Output pull-up supply (V_{PU})	+4.5VDC to +20VDC
Input voltage range, (V_{IN})	0VDC to +[0.00025 x (R_1 + R_3)]VDC 1/ 2/
	-10VDC to 0VDC 3/
Input current range, pin 2	0mA to +0.25mA
	0mA to +0.50mA 2/
Full scale frequency	100kHz 4/
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ C-A	Maximum θ J-A
10-lead can (TO-100)	A-2	225mW at T_A = 125°C	70°C/ W	150°C W	220°C W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1. Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4. Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. The microcircuit die is glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

3.2.9 Schematic circuit. The functional schematic circuit is shown in Figure 1.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Electrical performance curves are shown within paragraph 7.

3.3.2 Connection diagram. The connection diagrams for voltage-to-frequency operation are shown in Figures 2 and 3. The connection diagram for frequency-to-voltage operation is shown in Figure 4.

1/ For positive input voltages (see Figure 2).
2/ For frequencies 100kHz to 200kHz 50% duty cycle is recommended (see paragraph 3.3.3.1).
3/ For negative input voltages (see Figure 3).
4/ For best line linearity.

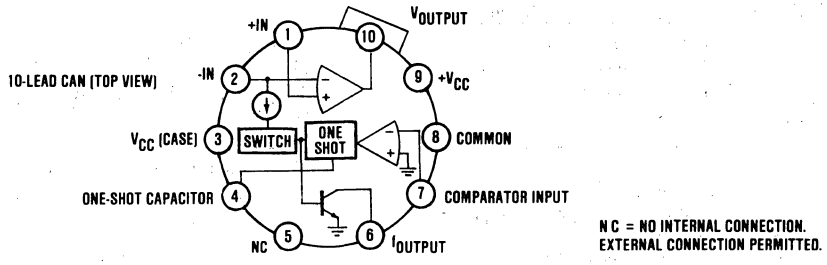


FIGURE 1. Terminal Connections and Functional Schematic Circuit.

3.3.3. Description of Operation. The input amplifier of the VFC is connected as an integrator (see Figure 2). When a positive input voltage is applied at V_{IN}, a constant current, $V_{IN}/(R_1 + R_3)$, will flow through the input resistor, $(R_1 + R_3)$, charging capacitor C_2. At this time the current sink is disabled as the switch is open and the VFC output, pin 6, is logic "0". The voltage at the amplifier output (comparator input) will ramp down from a positive voltage toward zero, according to $dv/dt = V_{IN}/[(R_1 + R_3)C_2]$. When the ramp reaches a voltage close to zero ($\approx$ -0.6V), the comparator changes state, and fires the one shot. Note, this period of time is a function of the input voltage, V_{IN}.

As the one-shot fires, the VFC output, pin 6, changes from logic "0" to logic "1", and the switch closes enabling the 1mA current sink. The length of time the one shot fires is determined by a reference (7.5V) within the one shot and the external one shot capacitor C_1. Note, this period of time is not a function of the input voltage. For good over temperature performance C_1 must have a low temperature coefficient. When the current sink is enabled, the current in the integrating capacitor, C_2, reverses direction and flows toward the summing junction. This occurs because the constant input current, $V_{IN}/(R_1 + R_3)$, is set up to always be less than the 1mA current sink. The voltage at the amplifier output ramps up according to $dv/dt = [(V_{IN}/(R_1 + R_3)) - (1mA)]/C_2$. Before the ramp voltage saturates the amplifier, the one shot resets. When the one shot resets, the switch opens, the current sink is disabled, the VFC output changes back to logic "0" and the cycle repeats.

The total VFC period is determined by the following equations:

$$f_o = \frac{1}{t}$$

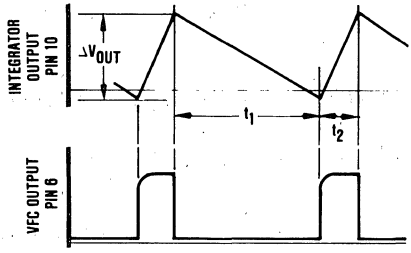
$$t = t_1 + t_2$$

$$t = \Delta V_{OUT}\, t \frac{C_2}{V_{IN}/(R_1 + R_3)} + \Delta V_{OUT}\, t_2 \frac{C_2}{V_{IN}/(R_1 + R_3) - 1mA}$$

and:

$$-\Delta V_{OUT}\, t_1 = +\Delta V_{OUT}\, t_2$$

$$t_2 = C_1 \frac{7.5V}{1mA}$$



The equations reduce to:

$$f_o = \frac{V_{IN}}{7.5\,(R_1 + R_3)\,C_1}$$

Note, the output frequency is not dependent upon C_2, and the temperature coefficients of R_1, R_3, and C_1 are critical to the VFC's over-temperature performance. These temperature coefficient effects must be added to the drift specifications of the integrated circuit itself.

3.3.3.1 Duty cycle. The duty cycle (D) of the VFC is the percent the one-shot period (t_2) is of the total VFC period ($t_1 + t_2$). It is measured at the full scale input voltage, which is the full scale frequency.

$$D = \frac{t_2}{t_1 + t_2}$$

Duty cycle is related to the maximum input current and the 1mA (nominal) current sink. By reducing the equations for t_2 and f_o:

$$D = \frac{V_{IN}\,max/(R_1 + |R_3)}{1mA} = \frac{I_{IN}\,max}{1mA}$$

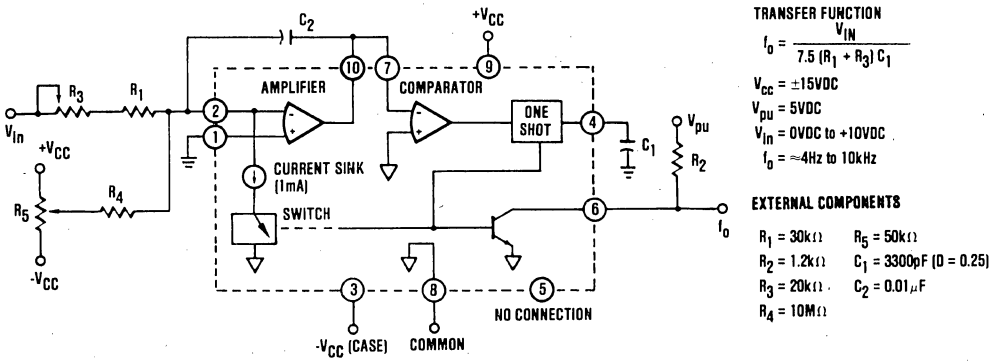


FIGURE 2. Connection Diagram, Voltage-to-Frequency Operation, Positive Input.

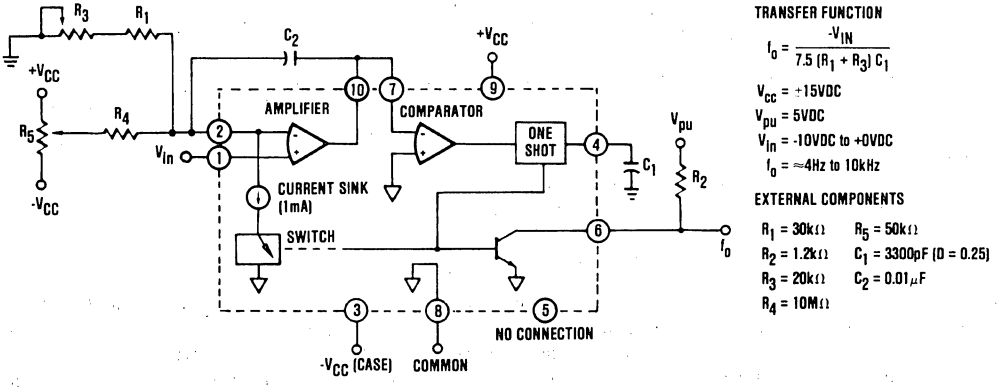


FIGURE 3. Connection Diagram, Voltage-to-Frequency Operation, Negative Input.

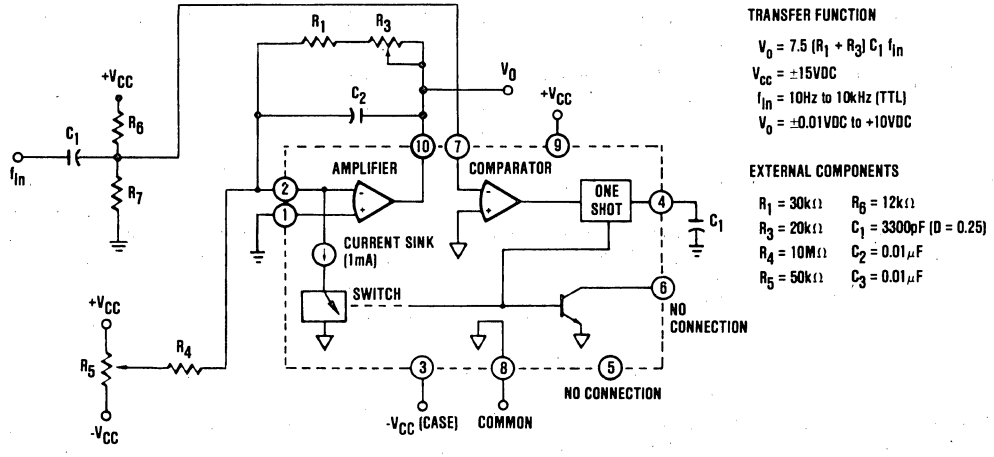


FIGURE 4. Connection Diagram, Frequency-to-Voltage Operation.

External component selection is typical. See paragraph 3.3.3.

The duty cycle (D) may be selected by the user to any value $\leq 70\%$ ($D \leq 0.70$). The 70% limit is due to component tolerances, offset, temperature effects, etc., and allowing 0.70mA as the minimum value for the 1mA (nominal) current sink, the worst case, maximum input current, $V_{IN}/(R_1 + R_3)$, is 0.50mA.

The normal, recommended duty cycle is 25% ($D = 0.25$) because this yields the best linearity. This is a maximum input current, V_{IN} ($R_1 + R_3$), of 0.25mA. The value of the external capacitor C_1 is the primary determinant of duty cycle and it is selected first; it determines the period t_2. Then the maximum input current, V_{IN} ($R_1 + R_3$), is computed to satisfy the VFC transfer function, which determines the total VFC period, $t_1 + t_2$.

For frequencies above 100kHz, the recommended duty cycle is 50% ($D = 0.50$); that is, 0.50mA maximum input current. This provides additional time for t_2 and compensates for the inherent delay time within the integrated circuit. This additional time allows the output transistor to turn off, providing a logic "1" output pulse, especially at elevated temperature.

3.3.4. External component selection. Refer to Figures 2, 3, and 4 for examples of external components' selection. One-shot capacitor C_1. This capacitor determines the duration of the logic "1" output pulse. For a 25% duty cycle ($D = 0.25$), 0.25mA maximum input current, use the first equation and select the closest standard value. For any duty cycle, D, use the second equation.

$$C_1\,(pF) = \frac{33 \times 10^6}{f_{MAX}} - 30 \quad \text{or} \quad C_1\,(pF) = \frac{D \times 133 \times 10^6}{f_{MAX}} - 30 \qquad (150pF\ min)$$

The initial tolerance of this capacitor is not critical because R_3 can be adjusted to remove the initial gain error. The temperature coefficient is critical because it adds directly as a transfer function error. An NPO ceramic type capacitor is recommended. Every effort should be made to minimize parasitic capacitance and C_1 should be mounted as close as possible to the VFC.

Input resistor $R_1 + R_3$. $R_1 + R_3$ determines the magnitude of the input current which charges the integrating capacitor C_2. The total resistance is calculated according to

$$R_1 + R_3 = \frac{V_{IN}\ max}{I_{IN}}$$

Normally, I_{IN} is 0.25mA; refer to paragraph 3.3.3.1. R_1, as a percentage of the R_1 and R_3 total resistance, should be 90% minus the percent initial tolerance of C_1. R_3 is the initial gain error adjustment, and as a percentage of the $R_1 + R_3$ total resistance, R_3 should be 20% plus twice the percent initial tolerance of C_1. The initial tolerance of R_1 and R_3 are not critical, but the temperature coefficients are critical because they add directly as transfer function errors. If the input signal is current rather than a voltage, R_1 and R_3 are replaced with a short circuit, and the removal of a gain error then requires adjustment of C_1.

Trimming components R_4 and R_5. R_5 nulls the offset voltage of the input amplifier (VFC offset error). It should have a resistance between 10kΩ and 100kΩ and a temperature coefficient less than or equal to 100ppm °C. R_4 should be 10MΩ and may be a 20% carbon composition resistor.

Output pull-up resistor R_2. Select a 10% carbon composition resistor according to

$$R_{2\ min} = \frac{V\ pull\text{-}up}{5mA - I_{from\text{-}the\text{-}load}}$$

For high frequency operation, $f \geq 100kHz$, it is necessary to minimize the capacitive loading of the output terminal, pin 6, to allow the open collector output voltage to rise rapidly to logic "1". One way to shorten the time constant formed by the pull-up resistance and the capacitance at this node is to lower the pull-up resistance. A constant current supply of 5mA to the output terminal with a diode clamp works well. The best way to shorten the time constant is to minimize the capacitive loading. The use of a TTL buffer is effective.

Integrating capacitor C_2. C_2 is a function of the full scale frequency and is selected according to

$$C_2\,(\mu F) = \frac{10^2}{f_{max}} \qquad (0.001\mu F\ min)$$

Select the closest standard value to the calculated value. The initial tolerance and temperature coefficient are not critical since C_2 does not appear in the transfer function. The leakage current of C_2 is critical as it introduces a gain error. Select a capacitor type with small leakage compared to the full scale input current (0.25mA); a mylar type is recommended.

Frequency-to-voltage operation R_6, R_7, C_3.
To interface with TTL logic, the input should be coupled through a capacitor (C_3), and the minus input to the comparator, pin 7, biased near +2.5V (see Figure 4). The converter will detect the falling edge of the input pulse train as the voltage at

pin 7 crosses -0.6V. The converter will reset as the voltage at pin 7 goes positive and crosses +1.0V. Choose C_3 for an appropriate R_6, R_7, C_3 time constant such that the time, t, from -0.6V to +1.0V, meets the specified pulse width range requirements (Table I). For input signals with amplitudes less than 5V, it will be necessary to bias pin 7 closer to zero to insure that the input signal at pin 7 crosses the -0.6V threshold. Errors may be nulled (see paragraph 3.3.5) using 0.001 of full scale frequency to null the offset, and full scale frequency to null the gain error.

Power supply bypass capacitors. Each power supply should be bypassed to ground as close as possible to the converter with 0.01μF capacitors.

3.3.5. Offset and gain error null. The VFC is capable of being nulled to zero offset and zero gain error using the circuits shown in Figures 2, 3, and 4. R_5 effects zero offset error; R_3 effects zero gain error.

The offset and gain error null adjustment procedure is:

a. Apply an input voltage that should produce an output frequency of 0.001 of full scale.
b. Adjust R_5 for 0.001 of full scale frequency.
c. Apply full scale input voltage. 1/
d. Adjust R_3 for full scale frequency.
e. Repeat steps a through e.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

3.4 Electrical Tests. Electrical test requirements are as specified in Table II. The subgroups of Table III which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2).
b. Inspection lot identification code. 2/
c. Manufacturer's identification (BURR-BROWN®).
d. Manufacturer's designating symbol (CEBS).
e. Country of origin.

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions for the /883B Hi-Rel product designation, including rebonding, are in accordance with Mll-M-38510.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening, for the /883B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5004, class B, except as modified in paragraph 4.3.

For the standard model, Hi-Rel product designation (none), routine manufacturing processing includes Burr-Brown internal visual inspection, stabilization bake, fine leak, gross leak, constant acceleration, and external visual inspection per MIL-STD0883, method 2009.

For the /883B Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /883B Hi-Rel product designation, is in accordance with MIL-STD-883, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

1/ For optimum linearity it is recommended that gain error nulling be performed at 90% of full scale frequency rather than at 100% of full scale frequency.
2/ A 4-digit data code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

TABLE I. Electrical Performance Characteristics

All characteristics T_A = -55°C to +125°C, $\pm V_{CC}$ = 15VDC, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	VFC32 V GRADE MIN	VFC32 V GRADE TYP	VFC32 V GRADE MAX	VFC32 W GRADE MIN	VFC32 W GRADE TYP	VFC32 W GRADE MAX	VFC32 U GRADE MIN	VFC32 U GRADE TYP	VFC32 U GRADE MAX	UNITS
INPUT (V/F CONVERTER)											
Bias current	T_A = +25°C										
Inverting input			10	40		•	•		•	•	nA
Noninverting input			50	100		•	•		•	•	nA
Offset voltage 1/	T_A = +25°C		1	4		•	•		•	•	mV
Differential impedance	T_A = +25°C	330 ‖ 10	650 ‖ 10		•	•		•	•		kΩ ‖ pF
Common-mode impedance	T_A = +25°C	300 ‖ 3	500 ‖ 3		•	•		•	•		MΩ ‖ pF
INPUT (F/V CONVERTER)											
Impedance	T_A = +25°C	50 ‖ 10	150 ‖ 10		•	•		•	•		kΩ ‖ pF
Logic "1"		+1.0		+V_{CC}	•		•	•		•	V
Logic "0"		-V_{CC}		-0.6	•		•	•		•	V
Pulse-width range		0.1		150k/F_{MAX}	•		•	•		•	µsec
ACCURACY											
Linearity error 2/	T_A = +25°C, 0.01Hz ≤ oper freq ≤ 10kHz		±0.005	±0.010 3/		±0.003	±0.006		±0.005	±0.010	% of FSR 4/
	T_A = +25°C, 10kHz ≤ oper freq ≤ 100kHz		±0.025	±0.050		•	•		•	•	% of FSR
	T_A = +25°C, 100kHz ≤ oper freq ≤ 200kHz		±0.050	±0.100		•	•		•	•	% of FSR
Offset error (input offset voltage) 1/	T_A = +25°C			±4			•			•	mV
Offset drift 5/	-25°C to +85°C			±3			±3			±3	ppm of FSR/°C
	-55°C to +125°C									±9	ppm of FSR/°C
Gain error 1/	T_A = +25°C		5	10		•	•		•	•	% of FSR
Gain drift 5/	f = 10kHz -25°C to +85°C						±100			±150	ppm/°C
	f = 10kHz -55°C to +125°C			±200			±100			±300	ppm/°C
Full scale drift (offset drift & gain drift) 5/6/	f = 10kHz -25°C to +25°C				-100	-50	0	-150		+50	ppm of FSR/°C
	+25°C to +85°C				0	+25	+100	-50		+150	ppm of FSR/°C
	f = 10kHz -55°C to +25°C	-200	-50	+100	-100	-50	0	-300		+100	ppm of FSR/°C
	+25°C to +125°C	-100	+50	+200	0	+50	+100	-100		+300	ppm of FSR/°C
	f = 200kHz -55°C to +25°C	-400	-200	0							ppm of FSR/°C
	+25°C to +125°C		0	±150							ppm of FSR/°C
Power supply sensitivity	f = DC, $\pm V_{CC}$ = 12VDC to 18VDC		±0.030	±0.040		•	•		•	•	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, logic "0"	I_{SINK} = 8mA	0	0.2	0.4	•	•	•	•	•	•	V
Leakage current, logic "1"	V_O = 15V T_A = +25°C		0.01	1.0		•	•		•	•	µA
Voltage, logic "1"	External pull-up resistor required (see Figure 2)			V_{PU}			•			•	V
Pulse width			0.25/F_{MAX}			•			•		sec
Fall time	I_{OUT} = 5mA, C_{LOAD} = 500pF			400			•			•	nsec
OUTPUT (F/V CONVERTER)											
Voltage	I_o = 7mA, T_A = +25°C	0 to +10			•			•			V
Current	V_O = 7VDC	+10			•			•			mA
Impedance	Closed loop			0.1			•			•	Ω
Capacitive load	Without oscillation			100			•			•	pF
DYNAMIC RESPONSE											
Full scale frequency		200			•			•			kHz
Dynamic range		6			•			•			decades
Settling time	(V/F) to specified linearity ΔVIN = 10V					•			•		
Overload recovery	<50% overload		7/			•			•		
			7/								
POWER SUPPLY											
Quiescent current	T_A = +25°C		±4.5	±6.0		•	•		•	•	mA
TEMPERATURE RANGE (ambient)											
Operating		-55		+125	•		•	•		•	°C
Storage		-65		+150	•		•	•		•	°C

*Specification the same as V grade.

NOTES:

1/ Adjustable to zero. See paragraph 3.3.5.

2/ Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0.1% of full scale frequency. See paragraph 7.

3/ ±0.015% of FSR for negative inputs.

4/ FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage).

5/ Exclusive of external components' drift.

6/ Positive drift is defined to be increasing frequency with increasing temperature.

7/ One pulse of new frequency plus 1µsec.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III.)

MODELS	VFC32VM VFC32VM/883B	VFC32WM VFC32WM/883B	VFC32UM VFC32UM/883B
MIL-STD-883 test requirement (class B)	SUBGROUPS (SEE TABLE III)		
Interim electrical parameters (preburn-in, method 5004)	1	1	1
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6	1*, 2, 3, 4, 5, 5U, 6, 6U	1*, 2, 3, 4, 5, 5U, 6, 6U
Group A test requirements (method 5005) 1/	1, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 5U, 6, 6U	1, 2, 3, 4, 5, 5U, 6, 6U
Groups C and D end point electrical parameters (method 5005) 1/	1	1	1

* PDA applies to subgroup 1 (see 4.3.c)
1/ Applies to "/883B" product only.

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	CONDITIONS $+V_{CC}$ = 15V, unless otherwise specified	LIMITS VFC32 V GRADE MIN	 MAX	VFC32 W GRADE MIN	 MAX	VFC32 U GRADE MIN	 MAX	UNITS
1 T_A = +25°C	Input offset voltage			4		*		*	mV
	Input bias current (inverting input)			40		*		*	nA
	Input bias current (noninverting input)			100		*		*	nA
	Output logic "0"	Pin 6 I_{SINK} = 8mA		0.4		*		*	V
	Output leakage current (logic 1)	Pin 6 V_{OUT} = 15V		1.0		*		*	μA
	Quiescent current	$+V_{CC}$ and $-V_{CC}$		±6.0		*		*	mA
	Power supply sensitivity	f = DC $\pm V_{CC}$ = 12VDC to 18VDC		±0.04		*		*	% of FSR/%
2 T_A = +125°C	Output logic "0"	Pin 6 I_{SINK} = 5mA		0.4		*			V
3 T_A = −55°C	Output logic "0"	Pin 6 I_{SINK} = 5mA		0.4		*			V
4 T_A = +25°C	Gain error, unadjusted	f = $f_{FULL\ SCALE}$ = 200kHz		±20					kHz
	Linearity error	f = 200kHz		±200					Hz
	$f_{FULL\ SCALE}$ = 200kHz 1/	f = 150kHz		±200					Hz
		f = 100kHz		±100					Hz
		f = 50kHz		±100					Hz
		f = 10kHz		±20					Hz
		f = 5kHz		±20					Hz
		f = 1kHz		±20					Hz
	Gain error, unadjusted	f = $f_{FULL\ SCALE}$ = 10kHz				±1		±1	kHz
	Linearity error	f = 10kHz				±0.6		±1	Hz
	$f_{FULL\ SCALE}$ = 10kHz 1/	f = 7kHz				±0.6		±1	Hz
		f = 5kHz				±0.6		±1	Hz
		f = 1kHz				±0.6		±1	Hz
		f = 0.5kHz				±0.6		±1	Hz
		f = 0.1kHz				±0.6		±1	Hz
5 T_A = +125°C	Full scale drift	f = 200kHz 2/ +25°C to +125°C	−3.0	+3.0					kHz
	Full scale drift	f = 10kHz 2/ +25°C to +125°C			0	+100			Hz
5U T_A = +85°C	Full scale drift	f = 10kHz 2/ +25°C to +85°C			0	+60	−30	+90	Hz
6 T_A = −55°C	Full scale drift	f = 200kHz 2/ −55°C to +25°C	−6.4	0					kHz
	Full scale drift	f = 10kHz 2/ −55°C to +25°C			−80	0			Hz
6U T_A = −25°C	Full scale drift	f = 10kHz 2/ −25°C to +25°C			−50	0	−75	+25	Hz

* Limits the same as V grade.
NOTES: 1/ Linearity error is adjusted or normalized to zero at 90% of full scale frequency and at 0.1% of full scale frequency.
2/ Subtract the frequency at the colder temperature from the frequency at the hotter temperature.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5005 except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for the /883B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5004, class B, and is conducted on all devices. The following additional criteria apply:

a. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) T_A = +125°C minimum
   (4) Test duration is 160 hours minimum
c. Percent defective allowable (PDA). The PDA, for MIL Hi-Rel Product designations only, is 5 percent based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5004, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter test prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.
d. External visual inspection need not include measurement of case and lead dimensions.

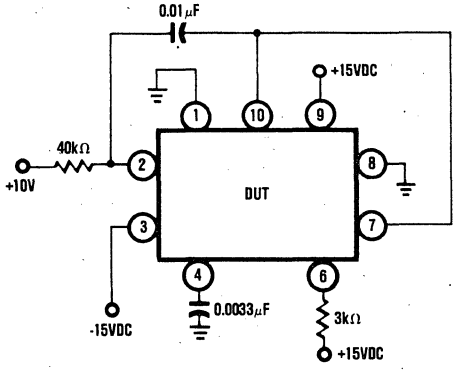


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5005, are performed as required by MIL-STD-883.

A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table I and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, and as follows:

a. End point electical parameters are specified in Table II herein.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:
a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group D as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. Caution - these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

7. DISCUSSION OF SPECIFICATIONS.

7.1 Linearity. Linearity is the maximum deviation of the actual transfer function from the straight line intersecting 90% of the full scale frequency (90% of full scale input) and 0.1% of the full scale frequency (≈ zero input). Linearity is the true measure of a VFC's performance. Linearity error is a function of the full scale frequency as shown in Figure 6. For a given full scale frequency the linearity error decreases with decreasing operating frequency as shown in Figure 7. To allow the user to benefit with improved linearity at lower frequencies, linearity error is specified in bands of operating frequency (see Table I).

7.2 Frequency stability versus temperature. The full scale frequency drift of the VFC32 versus temperature is shown in Figure 8. The temperature coefficient effects of the external components (especially R_1 and C_1) must be added to the drift of the converter.

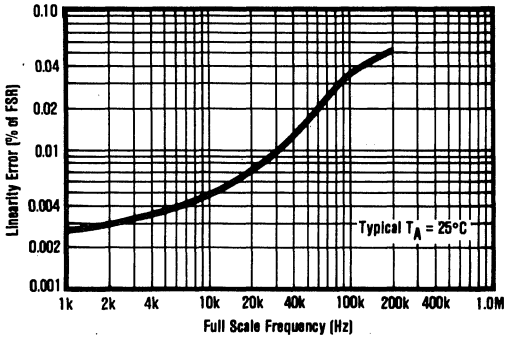


FIGURE 6. Linearity Error vs Full Scale Frequency.

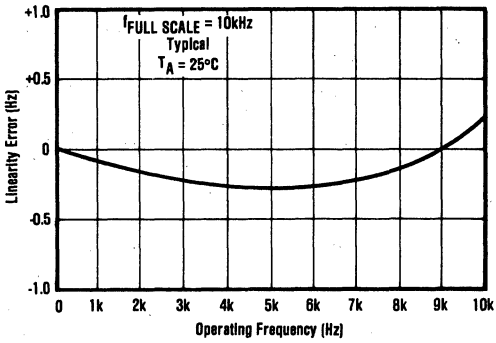


FIGURE 7. Linearity Error vs Operating Frequency.

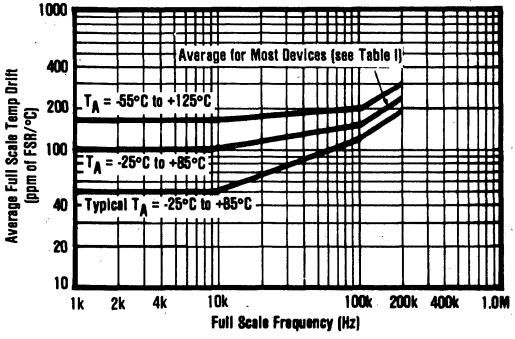


FIGURE 8. Full Scale Drift vs Full Scale Frequency.

BURR-BROWN®

3500/883B SERIES

MODEL NUMBERS:
3500R/MIL
3500R/883B
3500U/883B

REVISION B
MAY, 1986

General Purpose - Military OPERATIONAL AMPLIFIER

FEATURES

- LOW BIAS CURRENT, ±30nA, MAX
- LOW DRIFT, ±20μV/°C, MAX
- LOW NOISE, 1.4μV, rms
- WIDE SUPPLY RANGE, ±3VDC to ±20VDC
- INTERNAL COMPENSATION
- HI-REL MANUFACTURE

APPLICATIONS

- GENERAL PURPOSE AMPLIFIER
- ANALOG COMPUTATION
- PRECISION BUFFER
- LOW DRIFT INTEGRATOR
- BRIDGE AMPLIFIER
- STABLE REFERENCE CIRCUITS

DESCRIPTION

The 3500 IC op amps are designed for low input current while maintaining slew rate and bandwidth adequate for most applications. The low input bias current is achieved by a unique bias current cancelling circuit. This method insures that the bias current remains low over the full temperature and common-mode voltage ranges. The same circuitry gives the amplifier high impedance, both differential and common-mode.

The 3500 is also a low noise IC op amp. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually prevent the use of IC op amps for low-level signal processing.

The 3500 is internally compensated for unconditional stability for all feedback configurations, even with capacitive loads. The slew rate is independent of supply voltage level. The input stage of the 3500 series exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high with differential inputs as high as ±30 volts, thus the amplifier can be used as a sensitive comparator. The output stage is internally current-limited to provide protection against continuous short circuits. The 3500 is interchangeable with 741 type amplifiers but gives greatly improved performance.

These devices are manufactured in a hi-rel environment with clean room conditions which assures "built-in" quality. Each device is 100% internally visually inspected per MIL-STD-883 method 2010 and after the cap is welded on, the balance of the MIL-STD-883 method 5004 class B screening is completed.

They are then processed further by Quality Assurance, performing groups A and B inspections on each inspection lot and groups C and D inspections as required by MIL-STD-883. A report containing the most recent groups A, B, C, and D tests is available for a nominal charge.

The R grade devices offer the best performance over the ambient temperature range of -55°C to +125°C. However, if the operating ambient temperature range will not exceed -25°C to +85°C, such as with test equipment, the U grade device provides full performance at lower cost.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic, integrated circuit operational amplifier.

1.2 Part Number. The complete part number is as shown below.

3500	R	/883B
Basic model number	Grade (see 1.2.1)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, operational amplifier. Two electrical performance grades are provided, the R grade and the U grade, with the R grade offering the higher electrical performance.

1.2.2 Device class. The device class is similar to the product assurance level class B, as defined in MIL-M-38510.

The Hi-Rel product designator portion of the part number distinquishes the product assurance level as follows.

Hi-Rel product designator	Requirements
/883B	Basic model, plus 100% MIL-STD-883 class B screening with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
/883B	Basic model, plus 100% MIL-STD-883 class B screening.

1.2.3 Case outline. The case outline (8-lead can) is as defined in Figure 4. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	±20VDC 1/
Differential input voltage range	±40VDC 1/
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited 2/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	±3VDC to ±20VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ C-A
8-lead can	Figure 4	225mW at T_A = 125°C	70°C/W	220°C/W

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ Short circuit may be to ground only. Rating applies to +135°C case temperature or +50°C ambient temperature at ±15VDC supply voltage.

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead finish is gold plate. The lead material and finish is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. The microcircuit die is glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

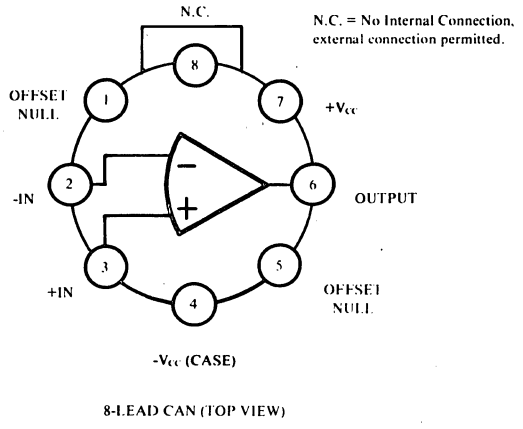


FIGURE 1. Terminal Connections.

FIGURE 2. Schematic Circuit.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Electrical performance curves are shown in paragraph 7.

3.3.2 Offset and gain error null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 2. If nulling is unnecessary for the application, delete the potentiometer and make no connections.

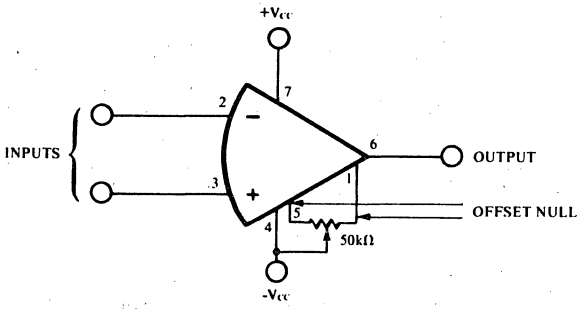


FIGURE 2. Offset Null Circuit.

3.3.3 Frequency compensation. No frequency compensation is required. The amplifier is free of oscillation when operated at any gain and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table III. The subgroups of Table III which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microciruit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions for the /883B Hi-Rel product designation, including rebonding, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening is in accordance with MIL-STD-883, method 5004, class B, except as modified in paragraph 4.3 herein.

For the /883B Hi-Rel product designator, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection for the /883B Hi-Rel product designation is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

1/ A 4-digit data code, indicating year and week of seal, and a 4- or 4-digit lot identifier are marked on each unit.

TABLE I. Electrical Performance Characteristics.

All characteristics at -55°C ≤ T_A ≤ +125°C, $\pm V_{CC}$ = 15VDC, unless otherwise specified.

Characteristics	Symbol	Conditions		3500R/MIL 3500R/883B Min	Typ	Max	3500U/883B Min	Typ	Max	Units
OUTPUT										
Voltage	V_O	R_L = 1kΩ		±10	±12		•	•		V
Current	I_O	R_L = 1kΩ		±10			•			mA
Resistance	R_O				2			•		kΩ
Current, short circuit	I_{OS}	To ground	T_A = 25°C	±10	±22		•	•		mA
OPEN-LOOP VOLTAGE GAIN	A_{VS}	f = 0Hz, No load		93	106		•	•		dB
DYNAMIC RESPONSE										
Bandwidth	BW	Unity gain	T_A = 25°C	1	1.5	2	•	•	•	MHz
			-55°C ≤ T_A ≤ +125°C	0.75	1.2		•	•		MHz
Bandwidth, full power	BW_{FP}		T_A = 25°C	10	25		•	•		kHz
Slew rate	SR		T_A = 25°C	0.6	1.2		•	•		V/μsec
			-55°C ≤ T_A ≤ +125°C	0.4			•			V/μsec
INPUT										
Offset voltage	V_{IO}	V_{CM} = 0	T_A = 25°C		±2	±5		•	•	mV
Offset voltage temperature sensitivity	$\Delta V_{IO}/\Delta T$		-25°C ≤ T_A ≤ +85°C						±20	μV/°C
			-55°C ≤ T_A ≤ +125°C			±20			±60	μV/°C
Bias current	I_B	V_{CM} = 0	T_A = 25°C		±10	±30		•	•	nA
Bias current temperature sensitivity	$\Delta I_B/\Delta T$		-25°C ≤ T_A ≤ +85°C						±1.0	nA/°C
			-55°C ≤ T_A ≤ +125°C			±1.5			±3.0	nA/°C
Offset current	I_{IO}	V_{CM} = 0	T_A = 25°C		±10	±30		•	•	nA
Offset current temperature sensitivity	$\Delta I_{IO}/\Delta T$		-25°C ≤ T_A ≤ +85°C					±0.5	±1.0	nA/°C
			-55°C ≤ T_A ≤ +125°C		±0.7	±1.5			±3.0	nA/°C
Power supply rejection	PSRR		T_A = 25°C		±40			•		μV/V
Common-mode voltage range	CMV	Linear operation	T_A = 25°C	±11	±12		•	•		V
Common-mode rejection	CMR	V_{CM} = ±10V	T_A = 25°C	90	100		•	•		dB
			-55°C ≤ T_A ≤ +125°C	80			•			dB
Impedance	Z_{IS}	T_A = 25°C	Differential		10^7 ‖ 3			•		Ω ‖ pF
			Common mode		10^9 ‖ 3			•		Ω‖ pF
Noise voltage	e_n	0.3Hz to 10Hz	T_A = 25°C		2	3		•	•	μV, p-p
		10Hz to 10kHz	T_A = 25°C		1.4	2		•	•	μV, rms
Noise, current	i_n	0.3Hz to 10Hz	T_A = 25°C		200	300		•	•	pA, p-p
		10Hz to 10kHz	T_A = 25°C		35	100		•	•	pA, rms
POWER SUPPLY										
Quiescent current	I_Q		T_A = 25°C		±2.5	±3.5		•	•	mA
TEMPERATURE RANGE (ambient)										
Operating				-55		+125	-55		+125	°C
Storage				-65		+150	-65		+150	°C

*Specifications the same as 3500R/883B.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III.)

MODELS / MIL-STD-883 Test Requirement (class B)	3500R/ 3500U/883B	3500U/883B
	SUBGROUPS (see Table III)	
Interim electrical parameters (pre burn-in)(method 5004)	1	1
Final electrical test parameters (method 5004)	1*, 2, 4, 5, 6	1*, 2, 2U, 4, 5, 6
Group A test requirements (method 5005)	1, 2, 4, 5, 6	1
Groups C and D end point electrical parameters (method 5005)	1	1
Additional electrical subgroups for group C inspections	7	7

*PDA applies to subgroup 1 (see 4.3d)

TABLE III. Group A Inspection

Subgroup	Symbol	MIL-STD-883 method or equivalent	Conditions $\pm V_{CC}$ = 15V unless otherwise specified	Limits				Units
				3500R/MIL. 3500R/883B		3500U/883B		
				Min	Max	Min	Max	
1	V_{IO}	4001			±5		±5	mV
T_A = 25°C	I_B	4001			±30		±30	nA
	I_{IO}	4001			±30		±30	nA
	I_Q	4005			±3.5		±3.5	mA
	CMR	4003	V_{CM} = ±10V	90		90		dB
2	$\Delta V_{IO}/\Delta T$	4001			±20			µV/°C
T_A = +125°C	$\Delta I_B/\Delta T$	4001			±1.5			nA/°C
to T_A = -55°C	$\Delta I_{IO}/\Delta T$	4001			±1.5			nA/°C
2A	$\Delta V_{IO}/\Delta T$	4001					±20	µV/°C
T_A = +85°C	$\Delta I_{IB}/\Delta T$	4001					±1.0	nA/°C
to T_A = -25°C	$\Delta I_O/\Delta T$	4001					±1.0	nA/°C
4	A_{VS}	4004	f = 0Hz, no load	93		93		dB
T_A = 25°C	SR	4002		0.6		0.6		V/µsec
5	A_{VS}	4004	f = 0Hz, no load	93		93		dB
T_A = +125°C	SR	4002	G = +1, ΔV_{in} = 10V, R_L = 1kΩ	0.4		0.4		V/µsec
6	A_{VS}	4004	f = 0Hz, no load	93		93		dB
T_A = -55°C	SR	4002	G = +1, ΔV_{in} = 10V, R_L = 1kΩ	0.4		0.4		V/µsec
7	e_n		0.3Hz to 10Hz		3			µV, p-p
T_A = 25°C			10Hz to 10kHz		2			µV, rms
	i_n		0.3Hz to 10Hz		300			pA, p-p
			10Hz to 10kHz		100			pA, rms

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5005, class B, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

Burr-Brown has performed and successfully completed qualification inspection as described below. The qualification report is available from Burr-Brown.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

4.3 Screening. Screening is in accordance with MIL-STD-883, method 5004, class B, and is conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition D, Y_1 axis only.

b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 3 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

d. Percent defective allowable (PDA). The PDA, for the /MIL Hi-Rel product designation only, is 5 percent based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5004, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter test prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

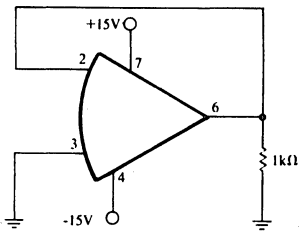


FIGURE 3 Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, are performed as required by MIL-STD-883. or purchase order.

A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, and as follows:

a. Tests are specified in Table II herein.

b. Tests previously performed as part of final electrical test need not be repeated.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 3 herein
   (3) $T_A = 125°C$ minimum
   (4) Test duration is 1000 hours minimum

b. End point electrical parameters are specified in Table II herein.

c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, and as follows:
a. end point electrical parameters are specified in Table II herein.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

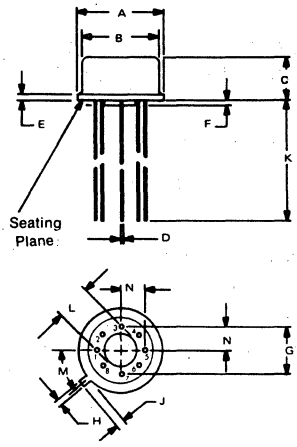
6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:
a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

6.4 Substitutability. Mircocircuits furnished under this specification are similar to Burr-Brown model 3500.

6.5 Microcircuit group assignment. These mircocircuits are assigned to Technology Group D as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.



NOTE:
Leads in true position within 0.10" (25mm) R at MMC at seating place.
Pin numbers shown for reference only.
Numbers may not be marked on package.
Weight: 3 grams max.

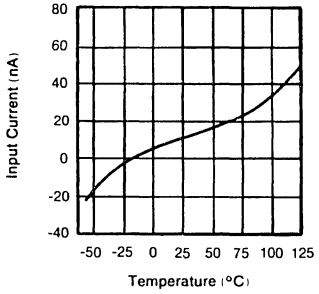
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 4. Case Outline (TO-99 Package Configuration).

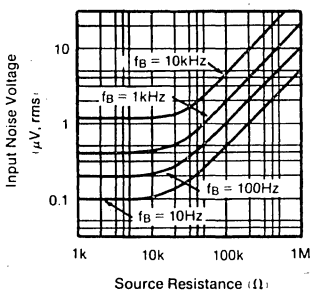
7. ELECTRICAL PERFORMANCE CURVES.

(Typical at $T_A = +25°C$ and $\pm V_{CC} = 15VDC$ unless otherwise specified).

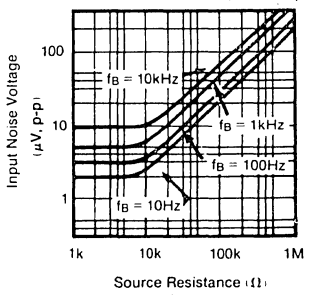
INPUT BIAS CURRENT vs. TEMPERATURE



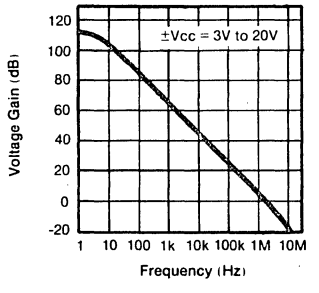
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



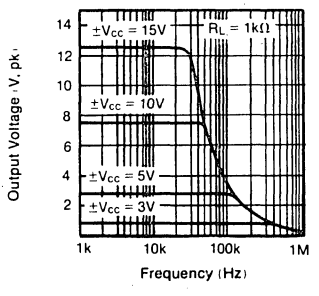
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



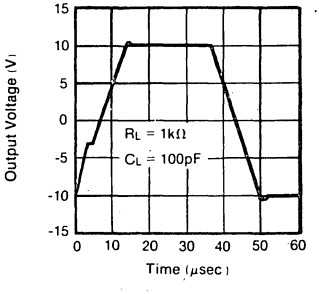
OPEN-LOOP FREQUENCY RESPONSE



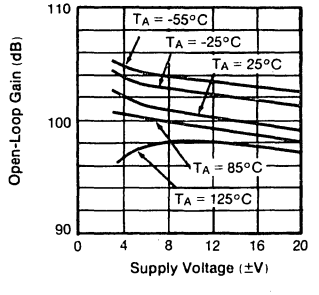
OUTPUT VOLTAGE vs. FREQUENCY



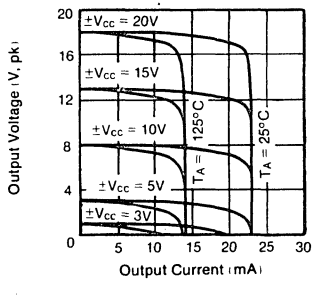
VOLTAGE FOLLOWER STEP RESPONSE



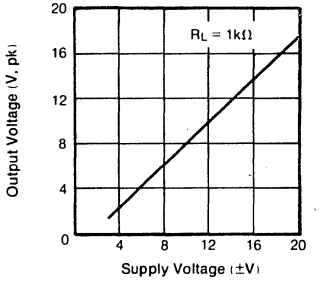
VOLTAGE GAIN vs. SUPPLY VOLTAGE



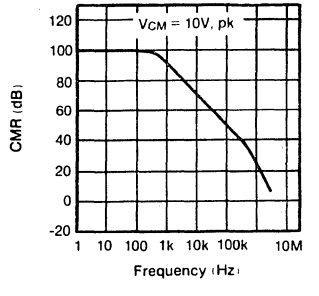
OUTPUT VOLTAGE vs. OUTPUT CURRENT



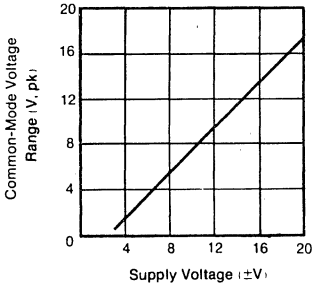
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



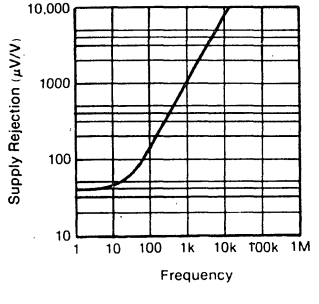
COMMON-MODE REJECTION vs. FREQUENCY



COMMON-MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



8. APPLICATIONS INFORMATION

8.1 Offset Adjustment. The input offset voltage of the Model 3500 may be adjusted to zero by connecting a 50kΩ potentiometer between pins 1 and 5 with the wiper arm connected to negative supply (Figure 5a). This provides an adjustment range of approximately ±10mV. This offset control is optional and may be omitted if the specified offset is considered sufficiently low.

Adjustment of the input offset voltage of the 3500 will affect the voltage drift to some extent. A rough "rule-of-thumb" is ±3μV/°C change of drift for each 1.0mV of offset adjustment. This is true of other IC op amps, such as the 741, 101, etc., but is usually masked by the greater drift of these units. However, in low drift amplifiers, this effect must be considered. By use of a transistor as in Figure 5b the effect of the offset adjustment on drift can be substantially reduced (by approximately a factor of six).

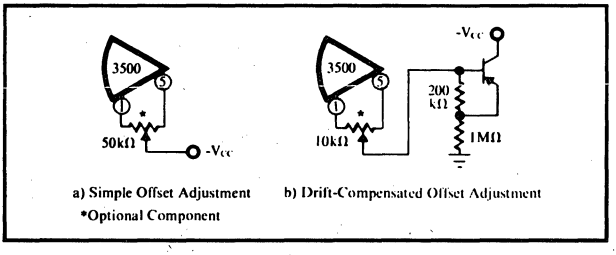


FIGURE 5. Offset Adjustment Techniques.

8.2 Bias Current Effects. Input bias current of the amplifier creates additional offset voltages by flowing in the impedances of the signal source and the feedback network. Although the bias currents of the 3500 are quite small, their effects may be appreciable when these impedances are large. The bias currents at the two inputs tend to be equal and the difference current smaller than either. Thus equalizing the resistance from each input to common, as in Figure 6, is an effective means of reducing DC offset due to bias current.

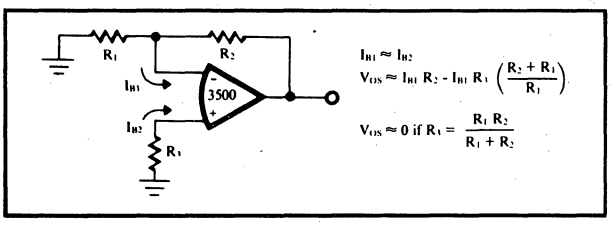


FIGURE 6. Minimization of Bias Current Effects.

8.3 Operation on a Single Supply. Although virtually any op amp can be operated on a single supply if input and output voltage limitations are observed, the Model 3500 is particularly suitable for such use. Its wide supply range of ±3VDC to ±20VDC translates to a single supply operating range of 6VDC to 40VDC, plus or minus. Two possible modes of operation on a single supply are shown in Figure 7. The following conditions must be observed to keep the amplifier within its linear region of operation.

1) $+2 < V_O < (V_{CC} - 2)$
2) $+3 < V_{IN} < (V_{CC} - 3)$. Figure 7b.

When operating on a single supply ($+V_{CC}$), shorting the output to common is equivalent to a short to supply and the internal power dissipation is approximately twice that which occurs for a short to common with balanced supplies of $\pm(V_{CC}/2)$. This dissipation may exceed safe limits for single supply voltages greater than 20V and must be prevented by use of a series limiting resistor or other device, if short circuit protection is desired.

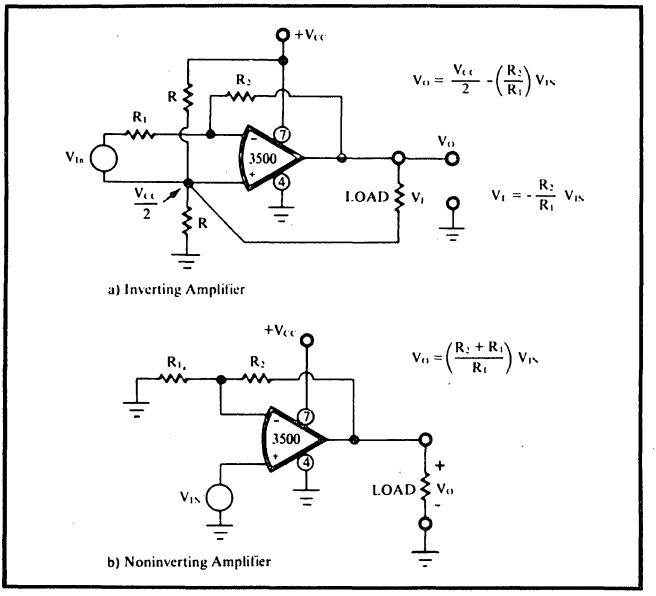
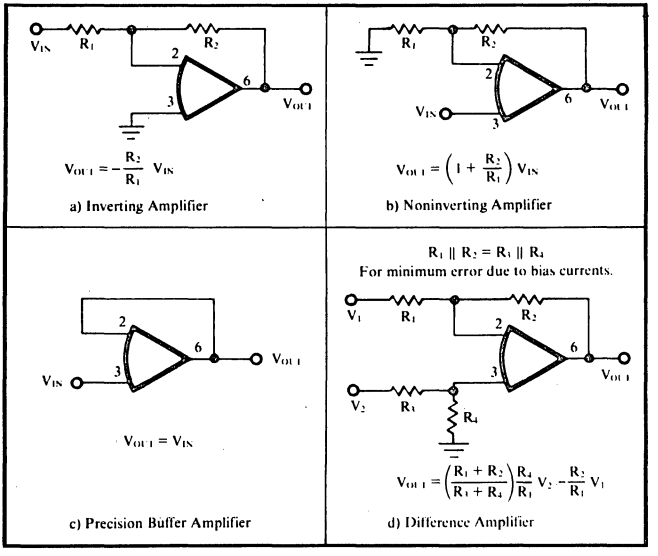


FIGURE 7. Operation on a Single Supply.

8.4 Wiring Precautions. In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 0.001μF ceramic capacitor from pins 7 and 4 to the power supply common.

8.5 Typical Applications.



BURR-BROWN®

3510/883B SERIES

MODEL NUMBER: 3510VM/883B

REVISION C
MAY, 1986

Very Low Drift Military OPERATIONAL AMPLIFIER

FEATURES

- **VERY LOW DRIFT, ±2μV/°C max**
- **VERY LOW OFFSET, ±120μV max**
- **LOW BIAS CURRENT, ±25nA max**
- **HIGH OPEN-LOOP GAIN, 120dB min**
- **HIGH CMR, 110dB min**

DESCRIPTION

High overall accuracy is offered by Burr-Brown's 3510 Operational Amplifier. It's designed expressly for use in high gain analog circuits where very-low drift and high accuracy are essential requirements.

This precision instrumentation grade op amp provides an economical method to maintain high circuit accuracy and reliability over temperature ranges from −55°C to +125°C.

Additional performance features of the 3510 include high open-loop gain, extremely low initial offset voltage, high CMR, very low thermal feedback, low input bias current and very low voltage drift vs temperature.

Burr-Brown's rigid control of monolithic processing and its rigid quality control standards result in very low voltage and current noise in the 3510. It's specifically designed for use in low level analog signal processing. Performance specifications are met exactly by precision trimming at the wafer level with complete testing before shipment.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic, low offset voltage drift, integrated circuit operational amplifier.

1.2 Part number. The complete part number is as shown below.

3510	V	M	/883B
Basic model number	Grade	Metal Package	Hi-Rel product designator

1.2.1 Device type. The device is a single, operational amplifier.

1.2.2 Device class. The device class is similar to the class B product assurance level as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance level as follows:

Hi-Rel Product Designator	Requirements
/883B	Standard model plus 100% MIL-STD-883 class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.

1.2.3 Case outline. The case outline (8-lead can) is as defined in Figure 5. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	±20VDC[1]/
Differential input voltage range	±40VDC[1]/
Storage temperature range	−65°C to +150°C
Output short-circuit duration	Unlimited[2]/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	±3VDC to ±20VDC
Ambient temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θJ−C	Maximum θJ−A
8-lead can	Figure 5	225mW at T_A = 125°C	70°C/W	220°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510 – Microcircuits, general specification for.

STANDARD
MILITARY
MIL-STD-883 – Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

1/ The absolute maximum input voltage is equal to the supply voltage.

2/ Short circuit may be to ground only. Rating applies to +135°C case temperature or +50°C ambient temperature at ±15VDC supply voltage.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. The microcircuit die is glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.7 Physical dimensions. The physical dimensions are in accordance with paragrpah 1.2.3 herein.

3.2.8 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

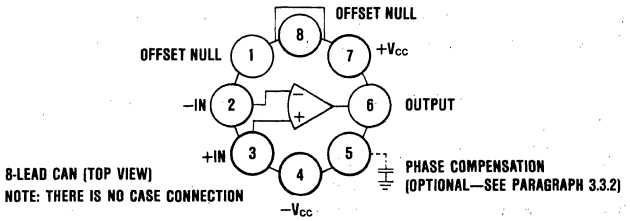


FIGURE 1. Terminal Connections.

3.2.9 Schematic circuit. A simplified schematic circuit is shown in Figure 2.

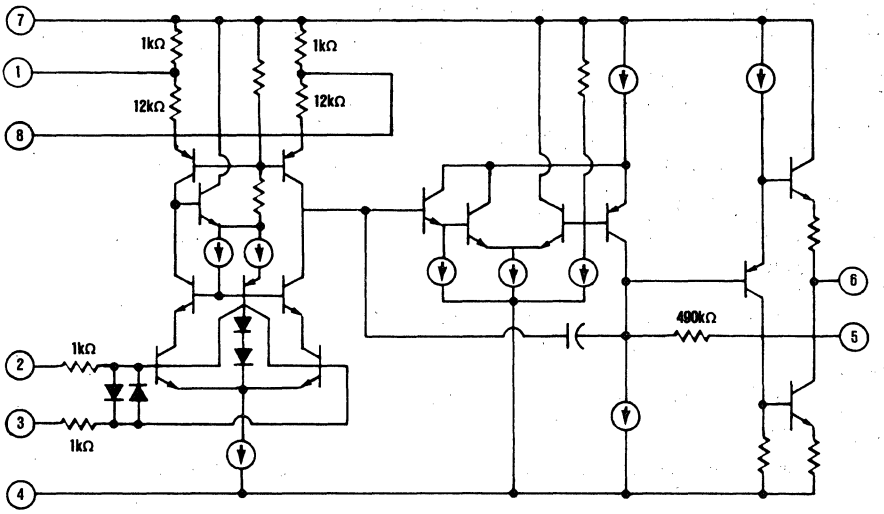


FIGURE 2. Schematic Circuit.

3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C, unless otherwise specified.

TABLE I. Electrical Performance Characteristics.

Characteristics	Symbol	Conditions (±V_{CC} = 15V, unless otherwise specified)		3510VM/883B Limits Min	Max	Units
Input offset voltage	V_{IO}		T_A = 25°C		±120	µV
			-55°C ≤ T_A ≤ +125°C		±350	µV
Input offset voltage temperature sensitivity (unnulled V_{IO})	$\frac{\Delta V_{IO}}{\Delta T}$	Δ T_A from -55°C to +25°C			±2	µV/°C
		Δ T_A from +25°C to +125°C			±2	µV/°C
Input offset current	I_{IO}		T_A = 25°C		±15	nA
			-55°C ≤ T_A ≤ +125°C		±55	nA
Input offset current temperature sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	Δ T_A from -55°C to +25°C			±0.4	nA/°C
		Δ T_A from +25°C to +125°C			±0.4	nA/°C
Input bias current	I_{IB}		T_A = 25°C		±25	nA
			-55°C ≤ T_A ≤ +125°C		±85	nA
Input bias current temperature sensitivity	$\frac{\Delta I_{IB}}{\Delta T}$	Δ T_A from -55°C to +25°C			±0.6	nA/°C
		Δ T_A from +25°C to +125°C			±0.6	nA/°C
Power supply rejection ratio	+PSRR	+V_{CC} = 10V -V_{CC} = -15V	T_A = 25°C		3	µV/V
Power supply rejection ratio	-PSRR	+V_{CC} = 15V -V_{CC} = -10V	T_A = 25°C		3	µV/V
Input voltage common-mode rejection	CMR	V_{CM} = -10V to +10V	T_A = 25°C	110		dB
Adjustment for input offset voltage	V_{IO} ADJ (±)			±1.5		mV
Output short circuit current (for positive output)	I_{OS} (+)		+25°C ≤ T_A ≤ +125°C	10	30	mA
			-55°C ≤ T_A ≤ +25°C	10	40	mA
Output short circuit current (for negative output)	I_{OS} (-)		+25°C ≤ T_A ≤ +125°C	10	30	mA
			-55°C ≤ T_A ≤ +25°C	10	40	mA
DC power dissipation (quiescent)	P_D	±V_{CC} = 20V	T_A = -55°C		170	mW
			T_A = +25°C		150	mW
			T_A = +125°C		130	mW
Single-ended input impedance (noninverting input)	Z_{IS1}		T_A = 25°C	1.5		MΩ
			-55°C ≤ T_A ≤ +125°C	1.0		MΩ
Single-ended input impedance (inverting input)	Z_{IS2}		T_A = 25°C	1.5		MΩ
			-55°C ≤ T_A ≤ +125°C	1.0		MΩ
Output voltage swing (maximum)	V_{OM}		R_L = 10kΩ	±11		V
			R_L = 1kΩ	±10		V
Open-loop voltage gain (single-ended) 1/	A_{VS} (±)	R_L = 2kΩ f = 0Hz	T_A = 25°C	120		dB
			-55°C ≤ T_A ≤ +125°C	114		dB
Open-loop voltage gain (single-ended) 1/	A_{VS} (±)	R_L = 2kΩ f = 0Hz	±V_{CC} = 3V T_A = 25°C	95		dB
Bandwidth, unity gain, small signal	BW		T_A = 25°C	0.25		MHz
Slew rate	SR (±)	V_{OUT} = ±10V, R_L = 1kΩ, A = +10, T_A = 25°C		0.5		V/µsec
Bandwidth, full power	BW_{FP}	V_{OUT} = ±10V, R_L = 1kΩ, A = +10, T_A = 25°C 2/		7		kHz
Input noise voltage	e_n	T_A = 25°C	0.1Hz to 10Hz		4.0	µV, pk-pk
			f_o = 1kHz		25	nV/√Hz
Input noise current	I_n	T_A = 25°C	0.1Hz to 10Hz		250	pA, pk-pk
			f_o = 1kHz		0.7	pA/√Hz

1/ Note that gain is not specified at $V_{IO\ ADJ}$ extremes. Some gain reduction is usually seen at $V_{IO\ ADJ}$ extremes.
2/ This parameter is untested. It is guaranteed by the slew rate test.

3.3.1 Offset and gain error null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 3.

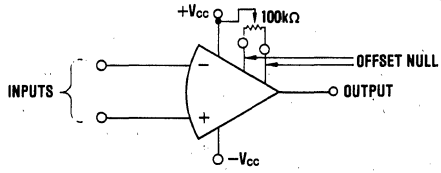


FIGURE 3. Offset Null Circuit.

3.3.2 Frequency compensation. The amplifier is free of oscillation when operated at a gain of 10 or greater with no external compensation and a source resistance of ≤10kΩ and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin

3.6 Workmanship These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared by Burr-Brown in fullfillment of the product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /883B product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the /883B product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing processes which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening is in accordance with method 5004 of MIL-STD-883, class B, except as modified in paragraph 4.3 herein. All microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /883B product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III).

MIL-STD-883 requirements (class B)	3510VM/883B
Interim electrical parameters (pre burn-in)(method 5004)	1A
Final electrical test parameters (method 5004)	1A*, 2A, 3A, 4A
Group A test requirements (method 5005)	1A, 2A, 3A, 4A, 7
Groups C and D end point electrical parameters (method 5005)	1
Additional electrical subgroups for Group C inspections	1C, 2C, 3C, 4C, 5, 6

*PDA applies to subgroup 1 (see 4.3.c)

1/ A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

TABLE III. Group A Inspection.

Subgroup	Symbol	MIL-STD-883 method or equivalent	Conditions $\pm V_{CC}$ = 15V, unless otherwise specified	3510VM/883B Limits Min	Max	Units
1A T_A = 25°C	V_{IO}	4001			±120	µV
	I_{IO}	4001			±15	nA
	I_{IB}	4001			±25	nA
	+PSRR	4003	+V_{CC} = 10V, -V_{CC} = -15V		3	µV/V
	-PSRR	4003	+V_{CC} = 15V, -V_{CC} = -10V		3	µV/V
	CMR	4003	V_{CM} = -10V to +10V	110		dB
	I_{OS}(+) 1/	3011	5sec. min 2/	10	30	mA
	I_{OS}(-) 1/	3011	5sec. min 2/	10	30	mA
	P_D	4005			105	mW
	$V_{IO\ ADJ}$			±1.5		mV
1C T_A = 25°C	$Z_{IS}1$			1.5		MΩ
	$Z_{IS}2$			1.5		MΩ
2A T_A = 125°C	V_{IO}	4001			±350	µV
	$\Delta V_{IO}/\Delta T$		$\frac{\Delta V_{IO}}{\Delta T} = \frac{V_{IO}\text{ (test 13)} - V_{IO}\text{ (test 1)}}{100°C}$		±2	µV/°C
	I_{IB}	4001			±50	nA
	$\Delta I_{IB}/\Delta T$		$\frac{\Delta I_{IB}}{\Delta T} = \frac{I_{IB}\text{ (test 15)} - I_{IB}\text{ (test 3)}}{100°C}$		±0.6	nA/°C
	I_{IO}	4001			±20	nA
	$\Delta I_{IO}/\Delta T$		$\frac{\Delta I_{IO}}{\Delta T} = \frac{I_{IO}\text{ (test 17)} - I_{IO}\text{ (test 2)}}{100°C}$		±0.4	nA/°C
2C T_A = 125°C	$V_{IO\ ADJ}$			±1.5		mV
	$Z_{IS}1$			1.0		MΩ
	$Z_{IS}2$			1.0		MΩ
3A T_A = -55°C	V_{IO}	4001			±310	µV
	$\Delta V_{IO}/\Delta T$		$\frac{\Delta V_{IO}}{\Delta T} = \frac{V_{IO}\text{ (test 22)} - V_{IO}\text{ (test 1)}}{80°C}$		±2	µV/°C
	I_{IB}	4001			±85	nA
	$\Delta I_{IB}/\Delta T$		$\frac{\Delta I_{IB}}{\Delta T} = \frac{I_{IB}\text{ (test 24)} - I_{IB}\text{ (test 3)}}{80°C}$		±0.6	nA/°C
	I_{IO}	4001			±55	nA
	$\Delta I_{IO}/\Delta T$		$\frac{\Delta I_{IO}}{\Delta T} = \frac{I_{IO}\text{ (test 26)} - I_{IO}\text{ (test 2)}}{80°C}$		±0.4	nA/°C
3C T_A = -55°C	$V_{IO\ ADJ}$			±1.5		mV
	$Z_{IS}1$			1.0		MΩ
	$Z_{IS}2$			1.0		MΩ
4A T_A = 25°C	V_{OM}	4004	R_L = 10kΩ, $\pm V_{CC}$ = 20V	±16		V
	V_{OM}	4004	R_L = 1kΩ	±10		V
	A_{VS}	4004	R_L = 2kΩ, V_{OUT} = ±10V, f = 0Hz	120		dB
	SR(±)	4002	V_{OUT} = ±10V, R_L = 1kΩ, A = +10	0.5		V/µsec
4C T_A = 25°C	A_{VS}		$\pm V_{CC}$ = 3V, R_L = 1kΩ	95		dB
5 T_A = 125°C	A_{VS}		R_L = 1kΩ, V_{OUT} = ±10V	114		dB
6 T_A = -55°C	A_{VS}		R_L = 1kΩ, V_{OUT} = ±10V	114		dB
7 T_A = 25°C	e_n		f_B = 0.1Hz to 10Hz		4.0	µV, pk-pk
	i_n		f_n = 0.1Hz to 10Hz		250	pA, pk-pk

NOTES:

1/ Due to significant power dissipation and associated device heating, these tests shall always be the last tests performed in any given sequence, followed by operational verification.

2/ The five second minimum test duration for I_{OS} test shall apply only for group A sampling inspections. For screening final electrical test, test duration for I_{OS} may be reduced to be consistent with automated test procedures.

3/ This parameter is untested. It is guaranteed by the conditions of the slew rate test.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening is in accordance with method 5004 of MIL-STD-883, class B, and is conducted on all devices. The following additional criteria apply:

a. Interim and final electrical parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

b. Burn-in test (method 1015 of MIL-STD-883) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 4 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

c. Percent defective allowable (PDA). The PDA for the / MIL product designation only, is 5 percent based on failures from group A, subgroup 1A test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures are included in the PDA. The verified failures of group A, subgroup 1A after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

d. External visual inspection need not include measurement of case and lead dimensions.

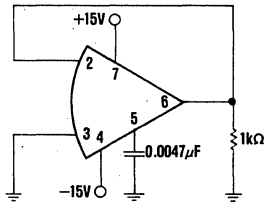


FIGURE 4. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of method 5005, MIL-STD-883, are conducted on each inspection lot. Groups C and D inspections of method 5005, MIL-STD-883, are performed as required by MIL-STD-883.

A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in Table I of method 5005 of MIL-STD-883 and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, class B, and as follows:

a. Steady state life test (method 1005 of MIL-STD-883) conditions::
   (1) Test condition B
   (2) Test circuit is Figure 4 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum

b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005 and as follows:

a. End point electrical parameters are specified in Table II herein.

4.4.5 Inspection of packaging. Inspection of packaging is in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage), are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

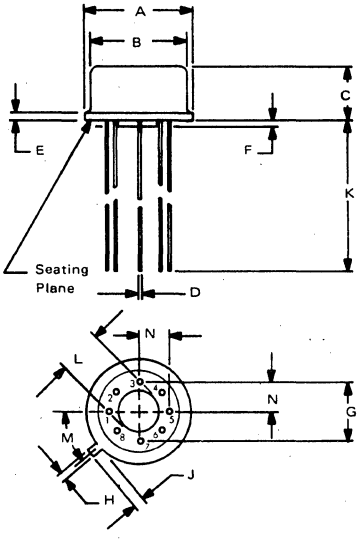
6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group D as defined in MIL-M-38510-, Appendix E.

6.5 Electrostatic sensitivity. CAUTION—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.



NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

Weight: 3 grams max.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 5. Case Outline (TO-99 Package Configuration).

BURR-BROWN®

4213/883B SERIES

MODEL NUMBERS:
4213WM/883B
4213WM
4213UM/883B
4213UM
4213VM/MIL
4213VM/883B
4213VM

REVISION C
MAY, 1986

Military
MULTIPLIER - DIVIDER

FEATURES

- **HI REL MANUFACTURE**
- **ACCURATE**
  - **±1/2% TOTAL ERROR (W grade)**
  - **±1% TOTAL ERROR (V and U grades)**
- **4-QUADRANT MULTIPLICATION**
  2-QUADRANT DIVISION
- **NO EXTERNAL COMPONENTS NECESSARY**
- **DIFFERENTIAL INPUT**
- **MIL-STD-883B SCREENING**
- **-55°C TO +125°C SPECIFICATIONS**

DESCRIPTION

The 4213/883B Series is a high performance, precision multiplier/divider with a total full scale error of ±1/2% or ±1%. It is intended for transducer and analog computation applications; it will also square, square root, and perform trigonometric computations. It has differential inputs and is ideal for instrumentation applications. The operating range is −55°C to +125°C. The 4213/883B is a hybrid microcircuit consisting of a monolithic bipolar IC and a precision laser-trimmed thin-film network. It is assembled into a hermetic TO-100 (10-lead can).

These devices are manufactured on a separate Hi-Rel manufacturing line with impeccable clean room conditions which assures "built-in" quality and provides for a long product life.

The 4213/883B Series is available in three electrical performance grades. The W grade features premium accuracy (±1/2% total error, ±50mV feedthrough, and ±25mV offset error). The V grade features ±1% total error, ±100mV feedthrough, and ±30mV offset error. The U grade has excellent performance from -25°C to +85°C and is also specified from -55°C to +125°C. U grade applications include test equipment, shipboard, ground support, and industrial applications where operation is normally between -25°C and +85°C and full temperature operation must be assured.

Two product assurance levels are available: standard, and /883B. The standard models have many MIL-STD0883 screens performed routinely. The /883B suffixed devices feature Hi-Rel manufacture, 100% screening per MIL-STD-883 method 5008 class B, and a 10% PDA. Quality assurance further processes /883B devices, performing group A and B inspections on each inspection lot and group C and D inspections as required by MIL-STD-883. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
MULTIPLIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a precision, integrated circuit multiplier.

1.2 Part Number. The complete part number is as shown below.

4213	V	M	/883B
Basic, model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, four-quadrant, analog multiplier; it will also function as a single, two-quadrant, analog divider, a squarer, a square rooter, etc. (see paragraph 8.3). Three electrical performance grades are provided. The W grade features premium accuracy of ±1/2% total error, ±50mV feedthrough and ±25mV offset error. The V grade features ±1% total error, ±100mV feedthrough and ±30mV offset error. The U grade features excellent performance from -25°C to +85°C and guarantees performance from -55°C to +125°C.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device Class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance level as follows:

Hi-Rel product designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883 hybrid class screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
(none)	Standard model, including 100% electrical testing

1.2.3 Case outline. The case outline is A-2 (10-lead can, TO-100) as defined in MIL-M-38510, Appendix C. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range (X, Y, and Z inputs)	±20VDC 1/
Differential input voltage (X, Y, and Z inputs)	±40VDC 1/
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited 2/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ Short circuit may be to ground only. Rating applies to +125°C case temperature or +75°C ambient temperature at ±15VDC supply voltage.

1.2.5 Recommended operating conditions.

Supply voltage range	±8.5VDC to ±20VDC
Ambient temperature range	-55°C to +125°C
Input voltage range ($\pm V_{CC}$ = 15VDC)	±10VDC

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
10-lead can (TO-100)	A-2	225mW at T_A = 125°C	70°C/W	220°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510, except that organic and polymeric materials are used for die attach. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. The dice utilized are glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

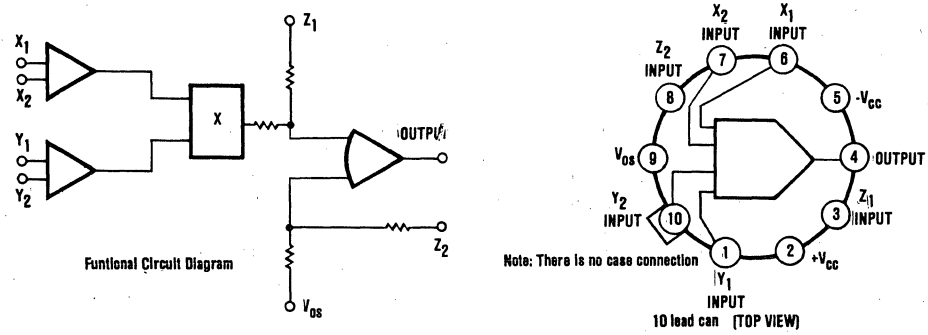


FIGURE 1. Functional Circuit Diagram and Terminal Connections.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

TABLE I. Electrical Performance Characteristics.

All characteristics T_A = -55°C to +125°C, $\pm V_{CC}$ = 15VDC, unless otherwise noted.

CHARACTERISTICS	SYMBOL	CONDITIONS		LIMITS 4212WM/883B 4213WM MIN	TYP	MAX	4213VM/883B 4213VM MIN	TYP	MAX	4213UM/883B 4213UM MIN	TYP	MAX	UNITS
ACCURACY													
Total Error	E_T	Each quadrant	T_A = +25°C			1/2			1			1	±% of FSR
			-25°C to +85°C									2	±% of FSR
			T_A = -55°C			3			3			4	±% of FSR
			T_A = +125°C			4			4			8	±% of FSR
Feedthrough													
X Input	FT_X	V_X = 20V, p-p	T_A = +25°C		30	50		30	100			100	±mV, p-p
		V_Y = 0, f = 50Hz	-55°C to +125°C			100			200			200	±mV, p-p
Y Input	FT_Y	V_X = 0, f = 50Hz	T_A = +25°C		25	40		25	80			80	±mV, p-p
		V_Y = 20V, p-p	-55°C to +125°C			80			180			180	±mV, p-p
Nonlinearity													
X Input	LIN_X	V_X = 20V, p-p, V_Y = ±10V	T_A = +25°C		0.08			•			•		±% of FSR
Y Input	LIN_Y	V_Y = 20V, p-p, V_X = ±10V	T_A = +25°C		0.01			•			•		±% of FSR
INPUT													
Input Resistance	R_{IN}	X, Y, Z inputs, pin 9 open		3.5	10		•	•		•	•		MΩ
Input Bias Current	I_{IB}	X, Y, Z inputs	T_A = +25°C		1.4	2.5		•	•		•	•	µA
			-55°C to +125°C			6			•			•	µA
Input Voltage Range	V_{IN}	Rated Operation		±10			•			•			V
Common-mode Rejection	CMR	+10V, -6V		60			•			•			dB
DYNAMIC CHARACTERISTICS													
Small Signal Bandwidth ±3dB Bandwidth	BW_{3dB}	X and Y inputs	T_A = +25°C	450	550		•	•		•	•		kHz
±1 flatness	$BW_{1\%}$	X and Y inputs	T_A = +25°C	70			•			•			kHz
Full Power Bandwidth	BW_{FP}		T_A = +25°C	130			•			•			kHz
Slew Rate	SR	X and Y inputs	T_A = +25°C	20			•			•			V/µsec
OUTPUT													
Output Voltage	V_{OM}	R_L = 2kΩ, C_L = 1000pF		10			•			•			±V
Output Resistance	R_O	Closed loop			1.5	10		•	•		•	•	Ω
Output Noise	N	T_A = +25°C	1Hz to 10kHz			200			•			•	µV, rms
			1Hz to 10MHz			1000			•			•	µV, rms
Output Offset Error 1/	V_{OO}		T_A = +25°C			25			30			50	±mV
			-25°C to +85°C									100	±mV
			-55°C to +125°C			100			100			200	±mV
Output Offset Error Temperature Sensitivity	$\frac{\Delta V_{OO}}{\Delta T}$		-25°C to +85°C									1.7	±mV/°C
			-55°C to +125°C			1.0			1.0			2.0	±mV/°C
Short Circuit Current	I_{OS}		T_A = +25°C	5		20	•		•	•		•	mA
			-55°C to +125°C	5		30	•		•	•		•	mA
POWER SUPPLY													
Power Supply Range				8.5	15	20	•	•	•	•	•	•	±V
Power Dissipation, Quiescent			T_A = +25°C		150	180		•	•		•	•	mW
			-55°C to +125°C			225			•			•	mW
TEMPERATURE RANGE (AMBIENT)													
Operating				-55		+125	•		•	•		•	°C
Storage				-65		+150	•		•	•		•	°C

*Specifications same as 4213WM

NOTE:

1/ Externally adjustable to zero.

3.3.1 Additional electrical performance characteristics. Electrical performance curves are shown in paragraph 7.

3.3.2 Transfer functions. The transfer functions for multiplier and divider connections are shown in Figure 2.

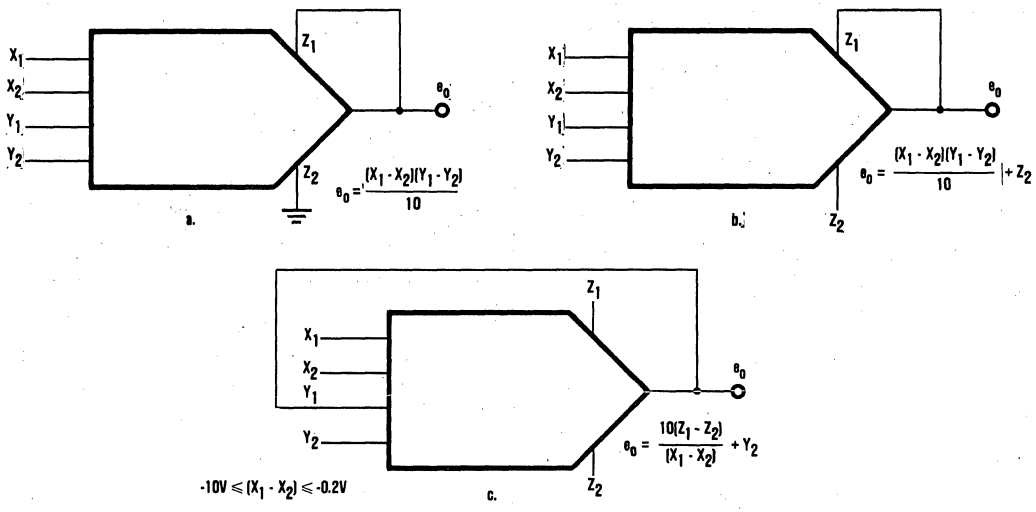


FIGURE 2. Transfer Functions.

3.3.3 Output offset error null. The multiplier is capable of being nulled to zero offset error using the circuit in Figure 3.

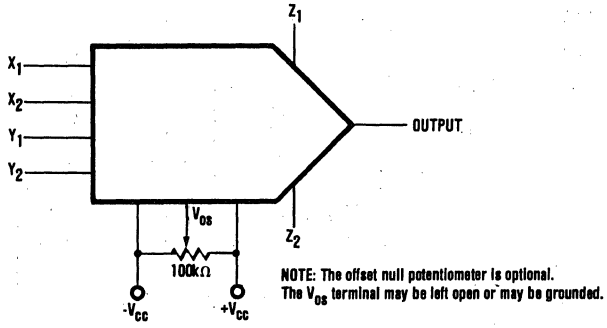


FIGURE 3. Offset Null Circuit.

3.4 Electrical tests. Electrical tests requirements are specified in Table II, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MODELS / MIL-STD-883 TEST REQUIREMENTS (HYBRID CLASS)	4213WM/883B 4213WM	4213VM/883B 4213VM	4213UM/883B 4213UM
		Subgroups (see Table III)	
Interim electrical parameters (Pre burn-in) (method 5008)	1	1	1
Final electrical test parameters (method 5008)	1, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 6	1, 2, 2U, 3, 3U, 4, 4U, 5, 5U, 6, 6U
Group A test requirements (method 5008)	1, 2, 3, 4, 4A, 5, 6	1, 2, 3, 4, 5, 6	1, 2, 2U, 3, 3U, 4, 4U, 5, 5U, 6, 6U
Group C end point electrical parameters (method 5008)	1	1	1
Additional electrical subgroups performed prior to Group C inspections	1C, 2C, 3C, 5C, 6C, 7C	1C, 2C, 3C, 5C, 6C, 7C	1C, 2C, 3C, 5C, 6C, 7C

*PDA applies to subgroup 1 (see 4.3.d)

TABLE III. Group A Inspection.

SUBGROUP	PARAMETER SYMBOL	CONDITIONS $\pm V_{CC}$ = 15VDC, pin 9 open unless otherwise specified	LIMITS 4213 V GRADE MIN	4213 V GRADE MAX	4213 W GRADE MIN	4213 W GRADE MAX	4213 U GRADE MIN	4213 U GRADE MAX	UNITS
1 T_A = +25°C	V_{OO} I_{IB} P_D	X_1 Input		±30 2.5 180		±25 2.5 180		±50 2.5 180	mV µA mW
1C T_A = +25°C	CMR R_{IN} R_o I_o	X = Y = +10V to -6V	60 3.5 5	 10 20					dB MΩ Ω mA
2 T_A = +125°C	V_{OO}			±100		±100			mV
2U T_A = +85°C	V_{OO}							±100	mV
2C T_A = +125°C	I_{IB} $\frac{\Delta V_{OO}}{\Delta T}$ P_D CMR	X_1 Input $\frac{\Delta V_{OO}}{\Delta T} = \frac{V_{OO}\ (+125°C) - V_{OO}\ (+25°C)}{100°C}$ X = Y = +10V to -6V	 60	6 ±1 225					µA mV/°C mW dB
3 T_A = -55°C	V_{OO}			±100		±100			mV
3U T_A = -25°C	V_{OO}							±100	mV
3C T_A = -55°C	I_{IB} $\frac{\Delta V_{OO}}{\Delta T}$ P_D CMR	X_1 Input $\frac{\Delta V_{OO}}{\Delta T} = \frac{V_{OO}\ (-55°C) - V_{OO}\ (+25°C)}{80°C}$ X = Y = +10V to -6V	 60	6 ±1 225					µA mV/°C mW dB
4 T_A = +25°C	E_T FT_X FT_Y	Each quadrant X = 20V, p-p; Y = 0; f = 50Hz X = 0; Y = 20V, p-p; f = 50Hz		±1 100 80		±1/2 50 40		±1 100 80	% mV, p-p mV, p-p
4A T_A = +25°C	V_{OM}	R_L = 2kΩ, C_L = 1000pF		±10					V
5 T_A = +125°C	E_T	Each quadrant		±4		±4			%
5U T_A = +85°C	E_T	Each quadrant						±2	%
5C T_A = +125°C	V_{OM} FT_X FT_Y	R_L = 2kΩ, C_L = 1000pF X = 20V, p-p; Y = 0; f = 50Hz X = 0; Y = 20V, p-p; f = 50Hz		±10 200 180					V mV, p-p mV, p-p
6 T_A = -55°C	E_T	Each quadrant		±3		±3			%
6U T_A = -25°C	E_T	Each quadrant						±2	%
6C T_A = -55°C	V_{OM} FT_X FT_Y	R_L = 2kΩ, C_L = 1000pF X = 20V, p-p; Y = 0; f = 50Hz X = 0; Y = 20V, p-p; f = 50Hz		±10 200 180					V mV, p-p mV, p-p
7C T_A = +25°C	$BW_{1\%}$ $BW_{1\%}$ SR SR BW_{3dB} BW_{3dB} BW_{FP} N N	X = 20V, p-p; Y = 10V X = 10V; Y = 20V, p-p X = +20V-step; Y = 10V; R_L = 2kΩ X = 10V; Y = +20V-step; R_L = 2kΩ X = 1V, rms; Y = 10V X = 10V; Y = 1V, rms R_L = 20kΩ, V_o = ±10V f_B = 1Hz to 10kHz f_B = 1Hz to 10MHz	70 70 20 20 450 450 130	 200 1000					kHz kHz V/µsec V/µsec kHz kHz kHz µV, rms µV, rms

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BB)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, for the /883B Hi-Rel product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for the /883B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

For the standard model, Hi-Rel product designation (none), routine manufacturing processing includes Burr-Brown internal visual inspection, and stabilization bake, fine leak, gross leak, burn-in (72 hours, performed preseal), constant acceleration (condition D) and external visual inspection per MIL-STD-883, method 2009.

For the /883B Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /883B Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

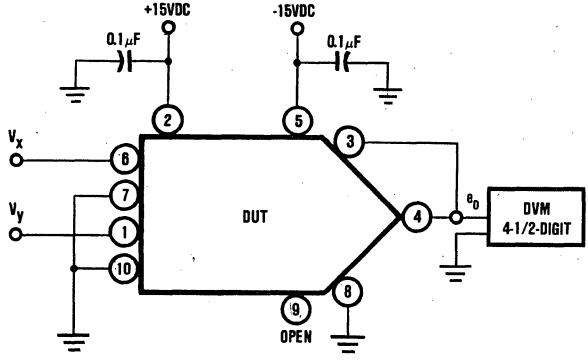


FIGURE 4. Test Circuit for Total Error.

1/ A 4-digit date code, indicating year and week of seal and a 4- or 5-digit lot identifier are marked on each unit.

PROCEDURE:

1. Set $V_x = V_y = +10.000VDC \pm 1mV$, measure $E_o = E_{o1}$.
2. Set $V_x = V_y = -10.000VDC \pm 1mV$, measure $E_o = E_{o2}$.
3. Set $V_x = +10.000VDC \pm 1mV$ and $V_y = -10.000VDC \pm 1mV$, measure $E_o = E_{o3}$.
4. Set $V_x = -10.000VDC \pm 1mV$ and $V_y = +10.000VDC \pm 1mV$, measure $E_o = E_{o4}$.
5. Calculate $V_{o1} = |E_{o1} - 10|$, $V_{o2} = |E_{o2} - 10|$, $V_{o3} = |E_{o3} + 10|$ and $V_{o4} = |E_{o4} + 10|$.
6. V_{ox} is the largest of V_{o1}, V_{o2}, V_{o3} or V_{o4}.

$$E_T(\%) = \frac{V_{ox}}{10} \times 100$$

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008 except as modified herein.

4.2 Qualification. Qualification is not required unless specified by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for the /883B Hi-Rel product designation, is in accordance with MIL-STD-883B, method 5008, class B, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition D, Y_1 axis only.

b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

d. Percent defective allowable (PDA). The PDA, for the /883B Hi-Rel product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

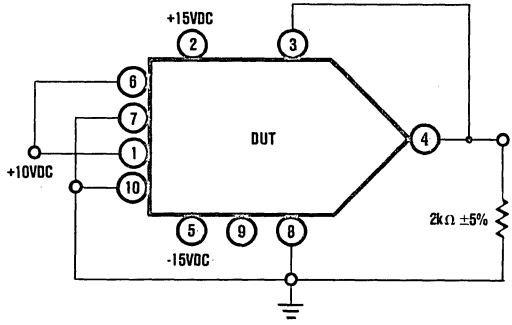


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, are performed as required by MIL-STD-883.

A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = 125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

6.4 Definitions.

Total error. Total error (E_T) is the difference between the actual output voltage and the ideal output voltage expressed as a percentage of the maximum output voltage, 10 volts. It is the sum of the individual errors and includes feedthrough and output offset voltage.

Feedthrough. Feedthrough (FT_X or FT_Y) is the output voltage when the ideal output voltage is zero (i.e., $X = 0$, $Y = \pm V$ or $X = \pm V$, $Y = 0$).

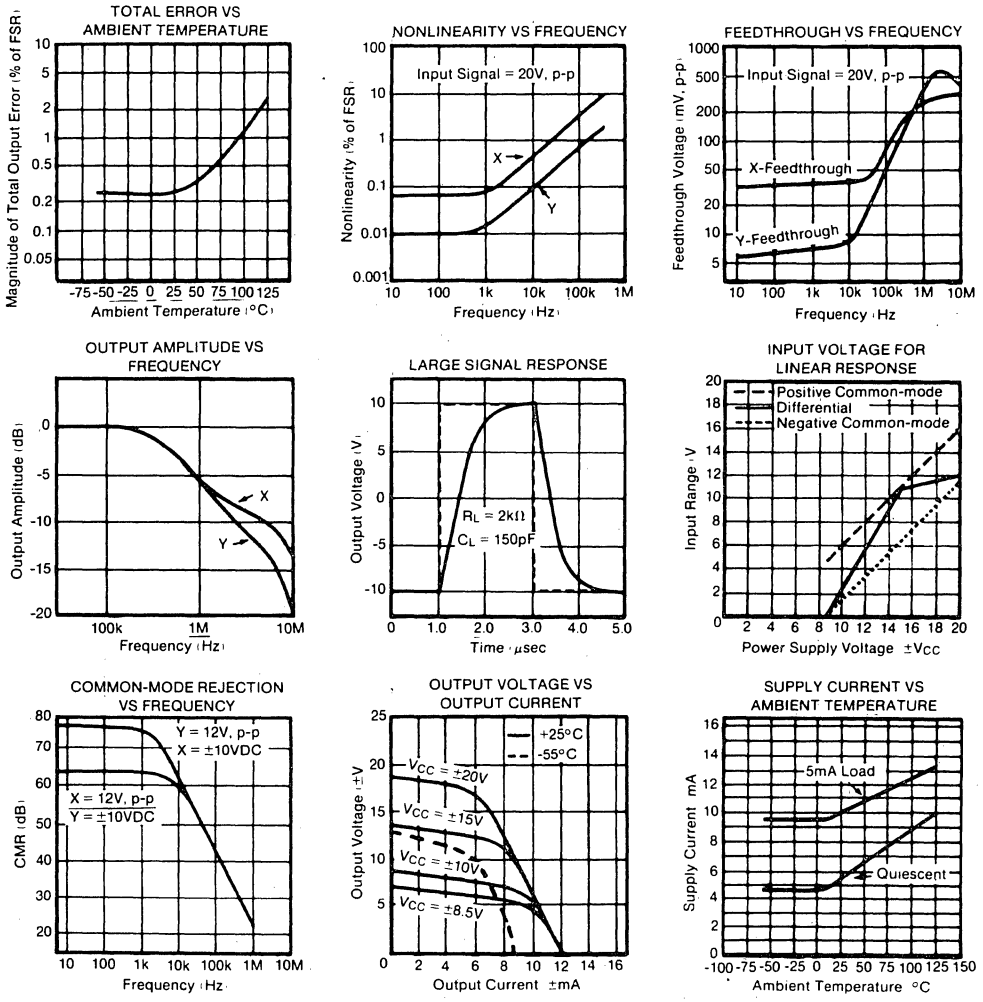
6.5 Microcircuit group assignment. These microcircuits are assigned to Technology Group I as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

6.7 Power Supply Sequencing. Apply, and remove, both supplies together. Alternatively, apply the positive supply first. Permanent damage may occur if the minus supply is applied with an input greater than +6VDC.

7. ELECTRICAL PERFORMANCE CURVES.

(Typical at T_A = +25°C and ± V_{CC} = 15VDC unless otherwise specified.)



8. APPLICATIONS INFORMATION

8.1 Power supply decoupling. For optimum performance and to prevent frequency instability due to power supply lead inductance, each power supply should be decoupled by connecting a 1μF tantalum capacitor from each power supply pin to ground (power supply common).

8.2 Capacitive loads. Stable operation is maintained with capacitive loads up to 1000pF, except for the square root mode which is limited to 50pF. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the output for isolation.

8.3 Typical Applications.

8.3.1 Multiplication. The basic connection for four-quadrant multiplication is shown in Figures 2a and 2b. Optional offset nullling is shown in Figure 3. Feedthrough may be minimized by applying an external nulling voltage to the X and/or Y input, as appropriate. Usually, the nulling voltage is applied to X_2 or Y_2. If Z_2 input is not used, it should be grounded.

Figure 6 shows how to achieve a scale factor larger than 0.1 (i.e., a denominator less than 10). A larger scale factor is electrically advantageous in some applications, but this has the disadvantage of proportionately increasing the output offset voltage. Note, the offset may be nulled as shown in Figure 3. Also, the small signal bandwidth is reduced to about 50kHz.

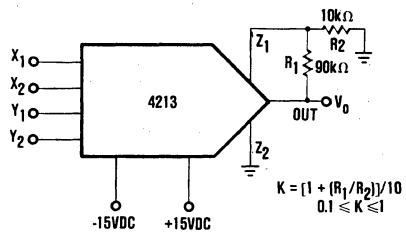


FIGURE 6. Connection for Unity Scale Factor.

8.3.2 Division. The basic connection for two-quadrant division is shown in Figure 2c.
Divider error is approximately

$$\epsilon_{divider} = \frac{10\epsilon_{multiplier}}{X_1 - X_2}$$

Note, the divider error will become very large for small values of $(X_1 - X_2)$. A 10 to 1 denominator range is a practical limit.

8.3.3 Squaring. The basic connection is shown in Figure 7.

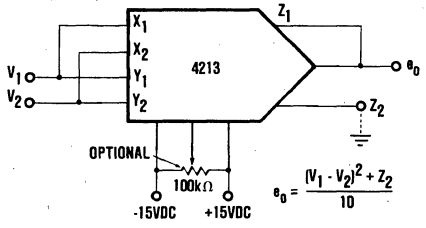


FIGURE 7. Squaring Connection.

8.3.4 Square Root. Figure 8 shows the connection for taking the square root of the voltage $V_{Z1} - V_{Z2}$. The diode prevents a latching condition which could occur if the input momentarily changed polarity. The load resistance R_L must be in the range of $10k\Omega \leq R_L \leq 1M\Omega$ to provide the current necessary to operate the diode. The output offset should be nulled for optimum performance; allow the input to be its smallest expected value and adjust R_1 for the proper output voltage. The square root mode accuracy is then approximately that of the multiply mode.

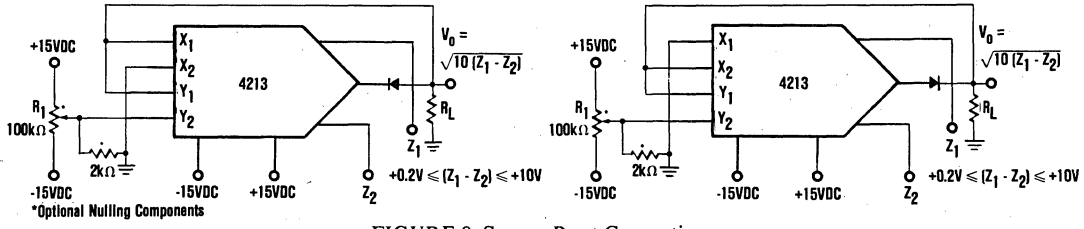


FIGURE 8. Square Root Connection.

8.3.5 Percent. The circuit of Figure 9 has a sensitivity of 1V/% and is capable of measuring 10% deviations. Wider deviation can be measured by decreasing the ratio of R_2/R_1.

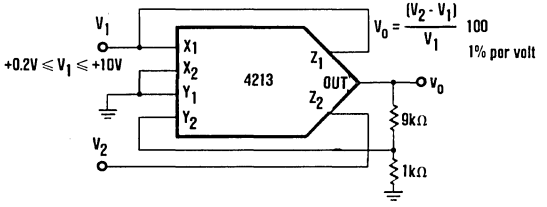


FIGURE 9. Percentage Computation.

8.3.6 Sine Function Generator. The circuit in Figure 10 uses implicit feedback to implement the following sine function approximation: $V_O = (1.5715V_I - 0.004317V_I^3)/(1 + 0.001398V_I^2) = 10 \text{ sine } (9V_I)$.

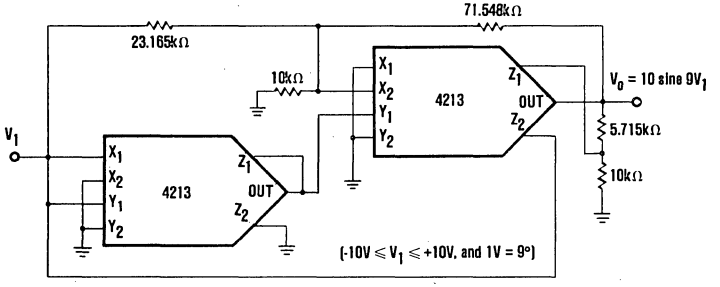


FIGURE 10. Sine Function Generator.

8.3.7 Single-phase Power Measurement. Figure 11 shows a circuit for measurement of single-phase instantaneous and real power.

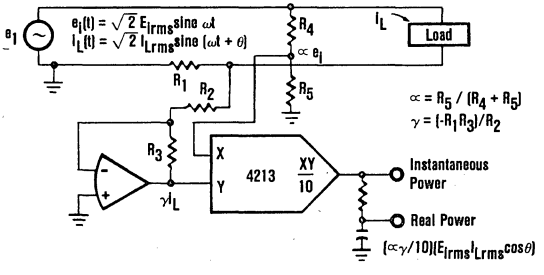
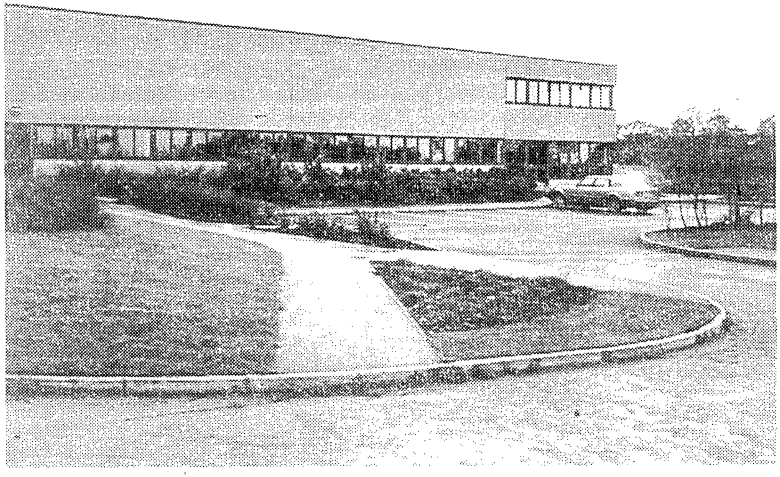


FIGURE 11. Single-Phase Instantaneous and Real Power Measurement.

BS9000 PRODUCTS



In the early 1980s Burr-Brown Corporation made the strategic decision to extend its international operations and invest in a manufacturing and design facility in Europe.

In 1982 the Corporation staffed and equipped a 30,000-square-foot facility at Kirkton Campus Science Park in Livingston, Scotland. The facility incorporates 10,000 square feet of class 10,000 clean area and the most modern test, laser, assembly and reliability equipment then available.

The facility was designed from conception as a location where high-quality, high-reliability components would be designed and manufactured. The vehicle chosen to demonstrate and promote this concept of high-quality, high-reliability components was BS9000/CECC.

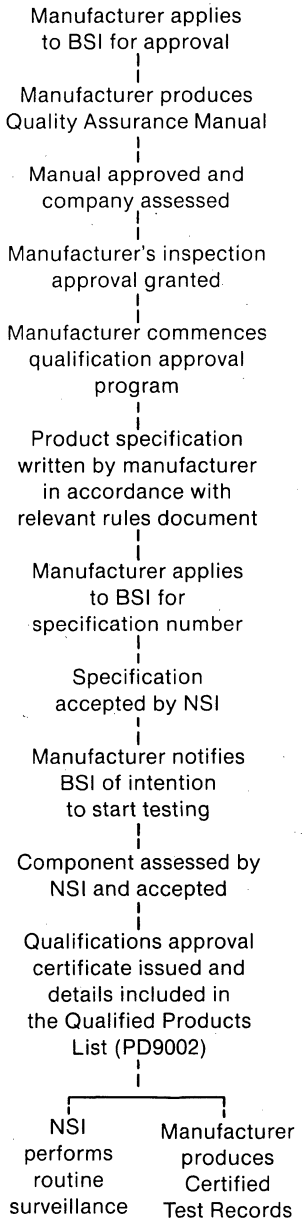
In December 1983 Burr-Brown Limited gained systems approval, via Route 2 to BS90000 and CECC90,000.

BSI registration number is	1247/M
CECC registration number is	M/123/CECC/UK
Factory Code is	BBM

Burr-Brown supplies precision components in total compliance with the stringent "harmonized assessed quality systems" BS9000 and CECC. The award of a "Route 2 Systems" approval by the British Standards Institution to the UK-based European manufacturing facility makes Burr-Brown the first manufacturer to offer traditional and specialized circuit functions to meet these internationally recognized assessed quality systems.

The user has a choice of all electrical performance grades across the 0/+70°C, −25/+85°C and −55/+125°C temperature ranges. Each temperature range and grade combination is offered in conjunction with four application categories from benign to aerospace environmental requirements.

PROCEDURE FOR QUALIFICATION APPROVAL



BS9000, CECC, IECQ

BS9000 is the United Kingdom national specification system for the quality assurance of electronic components. The CECC system is operated in the UK and Europe and the IECQ system is operated in the UK and internationally. However, within the UK, increasing emphasis is being placed on the CECC system to facilitate interchangeability of components throughout western Europe.

BS9000, CECC, IECQ are the quality assurance systems for the specification approval and release of electronic components. Requirements which must be met by participants in the systems are defined so that component purchasers can be sure of getting exactly what they have specified. In other words, electronic components are supplied by quality-assured sources.

In the UK, all three systems are operated by the British Standards Institution (BSI). In the case of CECC and IECQ, BSI acts on behalf of the relevant governing bodies—CECC for Europe and IECQ internationally.

An independent inspection authority—the National Standards Inspectorate (NSI)—is responsible for the assessment of manufacturers within the UK for all three systems.

The NSI undertakes all assessment and surveillance duties required by the three systems on behalf of all users. These include organizations involved in the manufacture of military, industrial and commercial systems as well as government bodies—for instance, the Ministry of Defense.

Their recommendations are submitted to BSI, which grants final approval.

COMPONENT QUALIFICATION

Three production lots using dice from three different wafer fabrication runs of each product type to be qualified are assembled and tested. Results are recorded. The products are then subjected to Groups A, B and C testing with results being recorded at various pre-determined points. From the results a "Qualification Test Report" is created and submitted, along with a full component specification, to NSI for approval. NSI audits the Report and Specification and, if satisfactory, issues component approval. **The component specification is now 'frozen' and may not be revised without NSI approval.**

MAINTENANCE OF QUALIFICATION

All BS/CECC components must be manufactured using assessed and qualified dice (see Figure 1). Samples are removed from all production lots and retained for extended life testing. Certified Test Records (CTRs) are created and maintained continuously and submitted to NSI annually. NSI also monitors the manufacturer's control system on a random basis using the approved Quality Manual as the control document. If the random audits and CTRs are acceptable to the published quality standards, qualification is maintained.

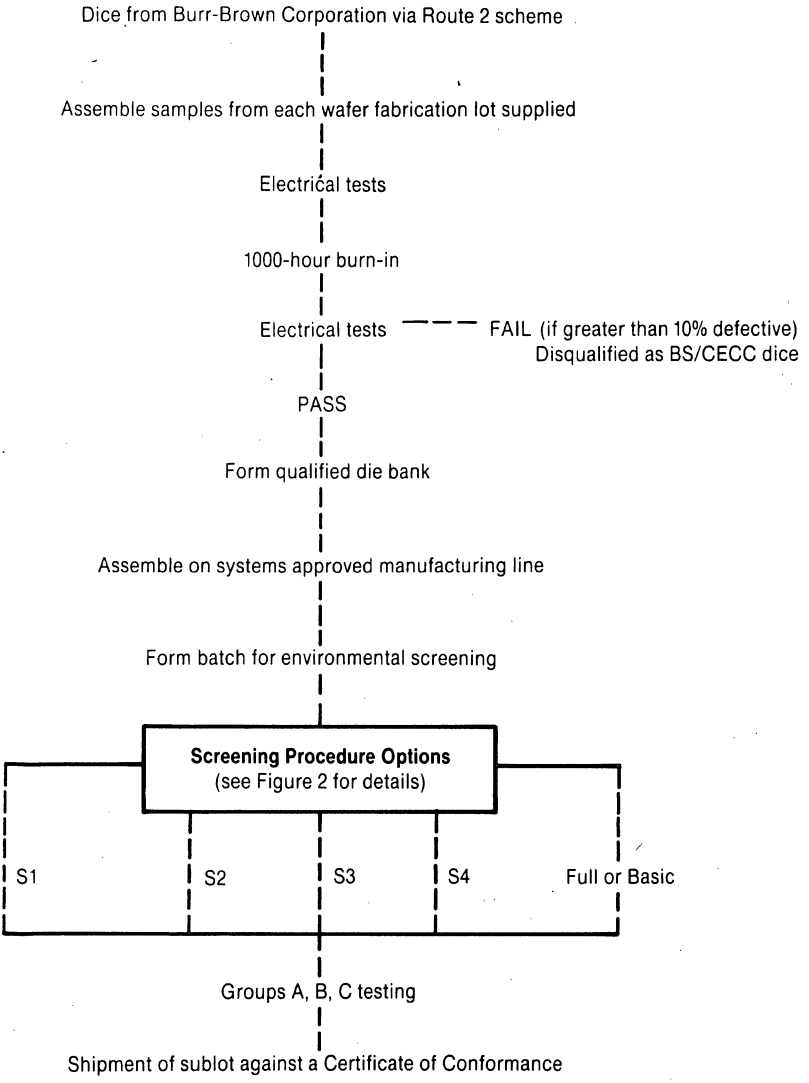


FIGURE 1. Manufacturers' Flow for Assessed Products.

RELATED DOCUMENTS

BS 2011. Basic environmental test procedures.

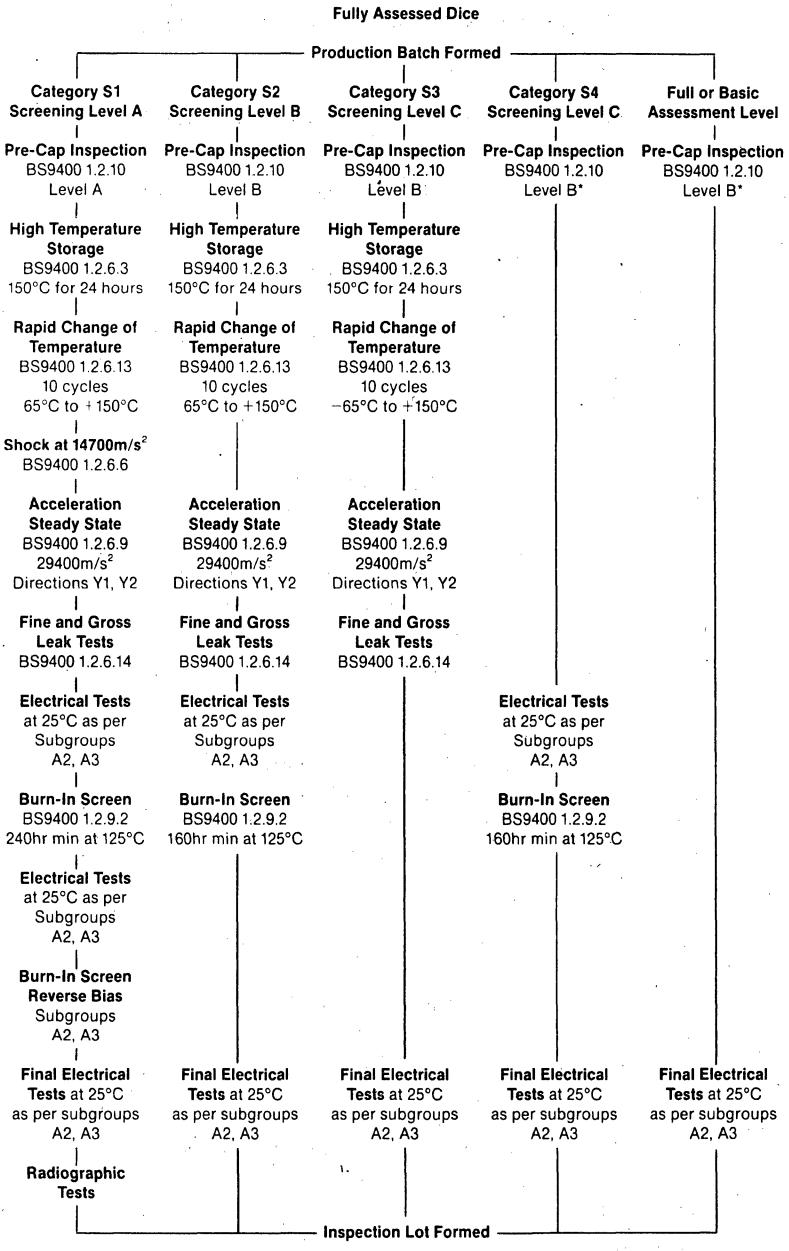
BS 3934 Dimensions of semiconductor devices.

BS 6001 Sampling procedures and table for inspection by attributes.

BS 9000 General requirements for electronic components of assessed quality.

BS 9400 Integrated electronic circuits of assessed quality: generic data and methods of test.

PD 9002 Qualified Products List for electronic components of assessed quality.



NOTE: The procedures specify the minimum screening requirements for each category.
Additional screens may be added according to customer requirements; e.g., PIND testing, shock, etc.

*Not required by B.S. but carried out 100% by Burr-Brown.

FIGURE 2. Screening Procedure Options.

Operation	BS9000, S2	MIL-STD-883, Revision B, Class B	MIL-STD-883, Revision C, Class B
Pre-Cap Inspection	BS9400 1-2-10 Level B	Method 2010 Condition B	Method 2010 Condition B
Stabilization Bake	BS9400 1-2-6-3 (150°C for 24hrs)	Method 1008 Condition C (150°C for 24hrs)	Method 1008 Condition C
Temperature Cycle	BS9400 1-2-6-13 (10 cycles −65°C to +150°C	Method 1010 Condition C (10 cycles −65, 25, 150, 25)	Method 1010 Condition C
Constant Acceleration	BS9400 1-2-6-9	Method 2001 Condition E (30,000g)	Method 2001 Condition E
Pre-Burn-In Electrical Test	Subgroups A2 & A3	(Optional)	(Optional)
Burn In	BS9400 1-2-9-2 (160hrs at 125°C)	Method 1015 (160hrs at 125°C)	Method 1015 (160hrs at 125°C)
Post-Burn-In Electrical Test	Subgroups A2 & A3	As Per Specification	As Per Specification
Leak Tests Fine/Gross	BS9400 1-2-6-14	Method 1014	Method 1014
PIND			Method 2020, Condition A

Comparisons of Ruled Documents and Classifications.

	BS/CECC	MIL-STD-883 Revision B	MIL-STD-883 Revision C
Qualification Procedures	BS9400 Section 2	Method 5005-7	Method 5005-8
Screening Procedures	BS9400 Section 2	Method 5004-5	Method 5004-6
Classification Similarity Matrix	S1 S2 S3 S4 Full Basic	S B — C — —	S B — — — —

Screening Procedure References and Methods.

EXPLANATION OF ADDITIONAL APPLICATION CATEGORIES

A complete explanation can be found in BS9400 Section 2.4 and 2.5. The following brief outline may be used as a guide:

Assessment Level S1 — For circuits where reliability is imperative, maintenance is impossible or very difficult, or downtime must be minimal. Examples are: equipment in space, critical military applications, high-revenue-earning equipment used in an adverse environment.

Assessment Level S2 — For circuits where reliability is important, maintenance is difficult or downtime must be low. Examples are: aircraft equipment, military applications, mobile communications equipment.

Assessment Level S3 — For circuits having similar environmental requirements to those for assessment level S2, but where electrical assurance can be relaxed.

Assessment Level S4 — For circuits having similar requirements to those for assessment level S2, but whose environmental performance is not assessed.

Full Assessment Level — For circuit applications where traceability in conjunction with a consistent quality assurance level is required.

Basic Assessment Level — The lowest level of assessment recognized in the BS9000 system—similar attributes to the full assessment level, but with relaxed inspection and acceptable quality levels.

PRODUCTS CURRENTLY UNDERGOING QUALIFICATION TO BS 9000—TARGET RELEASE IN 1986

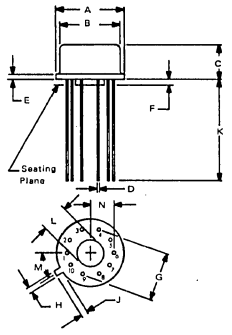
Model	Function	Package(s)
OPA2111	Dual low noise precision operational amplifier	TO-99, 20-pin LCC
OPA606	Wide-bandwidth operational amplifier	TO-99, 20-pin LCC
OPA156A	Wide-bandwidth operational amplifier	TO-99, 20-pin LCC
OPA356A	Wide-bandwidth operational amplifier	TO-99, 20-pin LCC
INA102	Low-power, high-accuracy instrumentation amplifier	14-pin DIL, 20-pin LCC
INA105	Precision unity-gain differential amplifier	TO-99, 20-pin LCC
INA110	High-speed FET-input instrumentation amplifier	TO-100, 20-pin LCC
MPY534	Precision analog multiplier	TO-100, 20-pin LCC
XTR101	Precision, low-drift, 4-20mA, 2-wire transmitter	14-pin DIL, 20-pin LCC
XTR110	Precision voltage-to-current converter/transmitter	14-pin DIL, 20-pin LCC
VFC100	Synchronized voltage-to-frequency converter	14-pin DIL, 20-pin LCC
DAC811	Microprocessor-compatible, 12-bit D/A converter	28-pin DIL, 28-pin LCC

In addition to the above, all of the following are undergoing qualification in the 20-pin 0.35" square LCC: OPA27, OPA37, OPA111, OPA121, INA101, VFC32, VFC62, VFC320, MPY100, MPY100, 4213.

Also being qualified in the 28-pin 0.45" square LCC are DAC702 and DAC703.

All LCC pinouts are as per "Jedec Standard No. 1 for Leadless Chip Carrier Pinouts Standardized for Linears".

TO-100

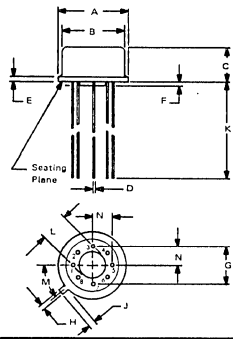


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.70	—
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

TO-99

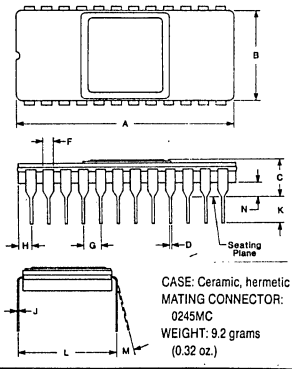


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

24-Pin Side-Brazed DIP



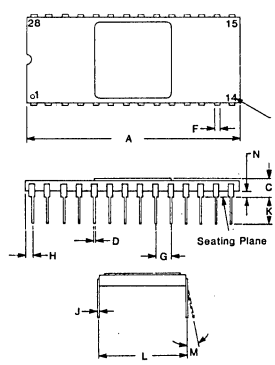
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.237	1.263	31.42	32.08
B	.514	.526	13.06	13.36
C	.120	.200	3.06	6.08
D	.016	.020	0.41	0.51
F	.050	.070	1.27	1.78
G	.100 BASIC		2.54 BASIC	
H	.065	.085	1.65	2.16
J	.008	.012	0.20	0.30
K	.100	.200	2.54	5.08
L	.600 BASIC		15.42 BASIC	
M	—	15°	—	15°
N	.035	.055	0.89	1.40

CASE: Ceramic, hermetic
MATING CONNECTOR: 0245MC
WEIGHT: 9.2 grams (0.32 oz.)

28-Pin Side-Brazed DIP

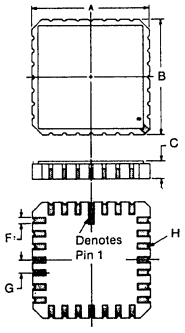


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

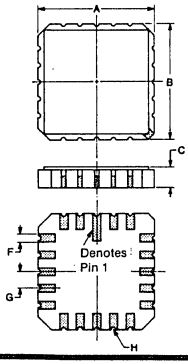
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.386	1.414	35.20	35.92
C	.108	.166	2.74	4.22
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

28-Pin LCC



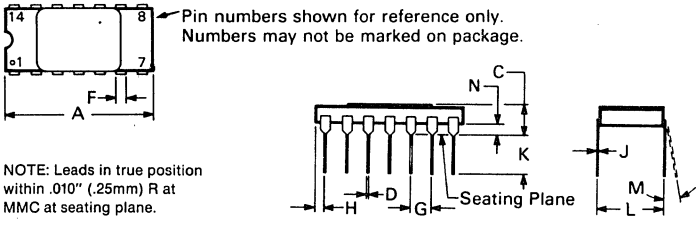
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.442	.458	11.23	11.63
B	.442	.458	11.23	11.63
C	.064	.100	1.63	2.54
F	.022	.028	0.56	0.71
G	.050 BASIC		1.27 BASIC	
H	.008R TYP.		0.20R TYP.	

20-Pin LCC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.342	.358	8.69	9.09
B	.342	.358	8.69	9.09
C	.064	.100	1.63	2.54
F	.022	.028	0.56	0.71
G	.050 BASIC		1.27 BASIC	
H	.008R TYP.		0.20R TYP.	

14-Pin Side-Brazed DIP



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

ORDERING INFORMATION

Product Type	Grade	Package	Category
INA101	S	M	S2

For specific grade and package options, refer to BS Product Data Sheet.

For category options, refer to the Category Options Table on page 6.

DIRECTORY OF ORGANIZATIONS

British Standards Institution
Head Office
2 Park Street
London, W1A 2BS, England

Telephone: 01-629-9000
TWX: 266933 (BSILONG)

CECC General Secretariat
VDE, Stresemannallee 15
D-6000 Frankfurt/Main 70
Federal Republic of Germany

Telephone: 69-630-8283/8207
TWX: 412871 (VDETZD)

IEC Quality Assessment System for Electronic Components

Bureau Central de la Commission Electrotechnique Internationale
1-3 Rue de Varembé
Geneva, Switzerland

Telephone: 022-340150
TWX: 28872 (CEJECCH)

BURR-BROWN®

DAC702

BS Number: BS9493-F0045

MONOLITHIC 16-BIT DIGITAL-TO-ANALOG CONVERTER—VOLTAGE OUTPUT

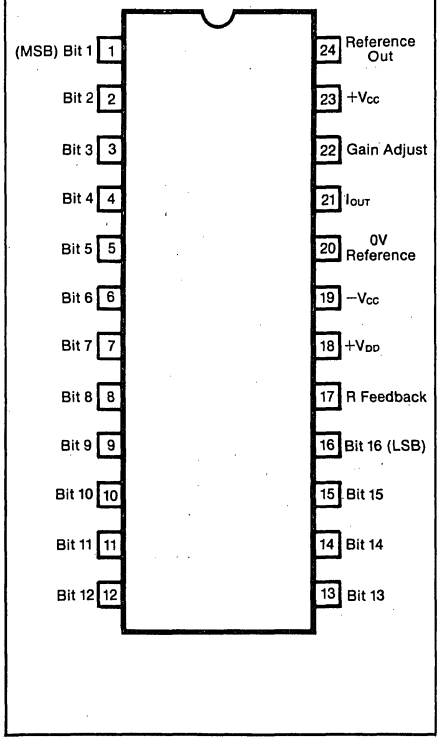
For applications information, see the standard product data sheet.

With the following exceptions, all Electrical Specifications are as per the specifications table included in the standard product data sheet (page 6-98).

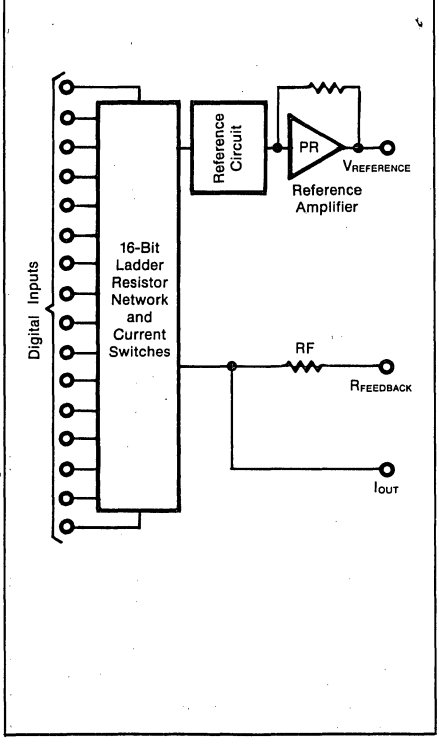
T_{AMB} = 25°C, V_{CC} = ±15V and V_{DD} = +5V.

ELECTRICAL SPECIFICATION		MIN	MAX	UNITS
Analog Output Current (I_O):	Code 0000 Hexadecimal	−0.7	−1.3	mA
	Code FFFF Hexadecimal	0.7	1.3	mA

PIN CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



PACKAGE OUTLINE—28-pin DIP (see page 13-7)

BURR-BROWN®

DAC703

BS Number: BS9493-F0046

MONOLITHIC 16-BIT DIGITAL-TO-ANALOG CONVERTER—VOLTAGE OUTPUT

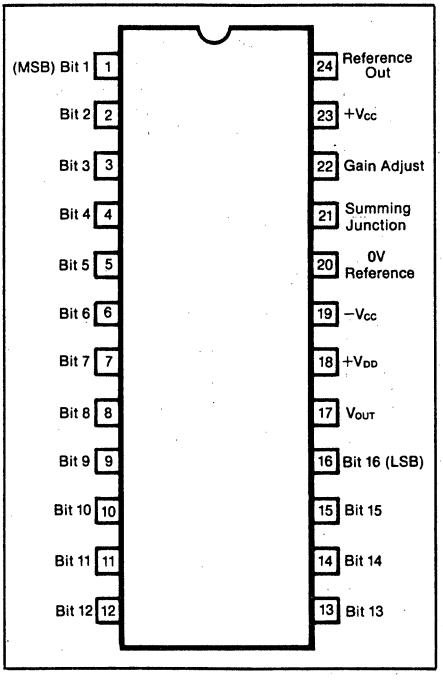
For applications information, see the standard product data sheet.

With the following exceptions, all Electrical Specifications are as per the specifications table included in the standard product data sheet (page 6-98).

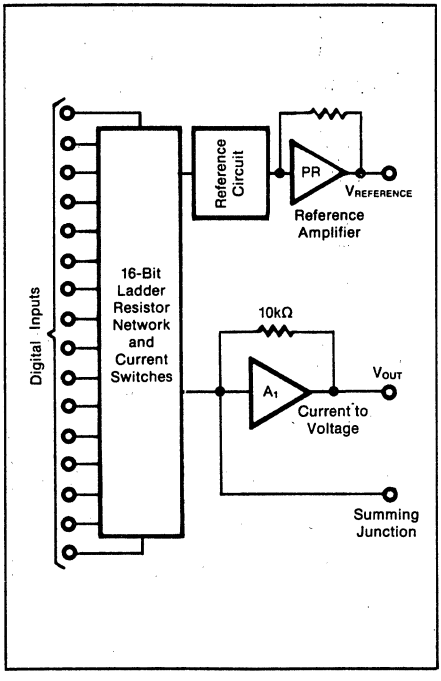
T_{AMB} = 25°C, V_{CC} = ±15V and V_{DD} = +5V.

ELECTRICAL SPECIFICATION	MODEL	MIN	MAX	UNITS
ANALOG OUTPUT				
Analog Output Voltage (V_O): Code 0000 Hexadecimal	DAC703BH	9.9992	10.000	V
	DAC703KH	9.9991	10.0001	V
Code FFFF Hexadecimal	DAC703BH	−9.9996	−10.0004	V
	DAC703KH	−9.9995	−10.0005	V
Analog Output Current (I_O)		5.0	—	mA
CONVERSION SPEED				
Settling Time to 0.003% of FSR, R = 2kΩ (t_{SETT}):				
For FSR Change		—	8.0	µs
For 1LSB Change (Major Carry)		—	4.0	µs

PIN CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



PACKAGE OUTLINE—28-pin DIP (see page 13-7)

BURR-BROWN®

INA101

BS Number: BS9400-G0077

VERY-HIGH ACCURACY INSTRUMENTATION AMPLIFIER

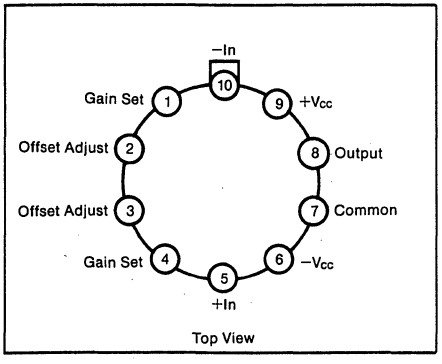
For applications information, see the standard product data sheet.

With the following exceptions, all Electrical Specifications are as per the specifications table included in the standard product data sheet (page 2-7).

Full temperature range V_{CC} = ±15V unless otherwise stated.

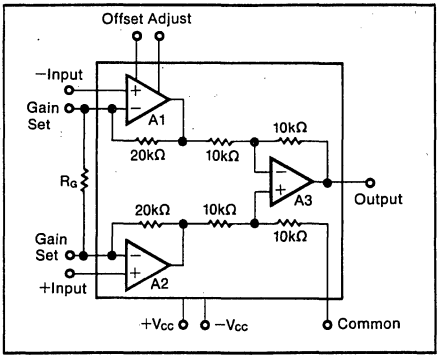
ELECTRICAL SPECIFICATION	MODEL	MIN	MAX	UNITS
Input Offset Voltage (V_{IO}), T_{AMB} = 25°C	INA101AM	—	±50 ±400/G	µV
	INA101BM/CM/SM	—	±25 ±200/G	µV
ΔV_{IO}	INA101AM	—	±2 ±20/G	µV/°C
	INA101BM/SM	—	±0.75 ±10/G	µV/°C
	INA101CM	—	±0.25 ±10/G	µV/°C
Input Offset Current (I_{IO}), T_{AMB} = 25°C	INA101AM/BM/SM	—	±30	nA
	INA101CM	—	±20	nA
ΔI_{IO}	INA101AM/BM/CM	—	±0.5	nA/°C
Input Bias Current (I_{IB}), T_{AMB} = 25°C	INA101AM/BM/SM	—	±30	nA
	INA101CM	—	±20	nA
Variation with V_{CC} (ΔI_{IB})	INA101AM/BM/SM	—	±0.2	nA/°C
	INA101AM/BM/SM	—	±0.1	nA/V
Voltage Gain (A_V), G = 1 + [(40K/RG)]	INA101AM/BM/SM	1.0	1000	V/V
Gain Temperature Coefficient ($A_{V\Delta T}$): Gain = 1	INA101AM/BM/CM/SM	—	5.0	ppm/°C
Gain = 10	INA101AM/BM/CM/SM	—	100	ppm/°C
Gain = 100	INA101AM/BM/CM/SM	—	110	ppm/°C
Gain = 1000	INA101AM	—	110	ppm/°C
Nonlinearity, DC	INA101AM	—	±(0.005 + 2 X 10^{-5}G)	% of p-p FS
	INA101BM/CM/SM	—	±(0.002 + 10^{-5}G)	% of p-p FS
Slew Rate ($\Delta V_O/\Delta T$), G = 1 to 100	INA101AM/BM/CM/SM	0.2	—	V/µs
Settling Time (t_{SETT}), to 0.1%: G = 1	INA101AM/BM/CM/SM	—	40	µs
G = 100	INA101AM/BM/CM/SM	—	55	µs
G = 1000	INA101AM/BM/CM/SM	—	470	µs
to 0.01%: G = 1	INA101AM/BM/CM/SM	—	45	µs
to 0.01%: G = 100	INA101AM/BM/CM/SM	—	70	µs
to 0.01%: G = 1000	INA101AM/BM/CM/SM	—	650	µs

PIN CONNECTION DIAGRAM



Top View

FUNCTIONAL DIAGRAM



PACKAGE OUTLINE—TO-100 (see page 13-7)

BURR-BROWN®

MPY100

BS Number: BS9400-G0083

MULTIPLIER-DIVIDER

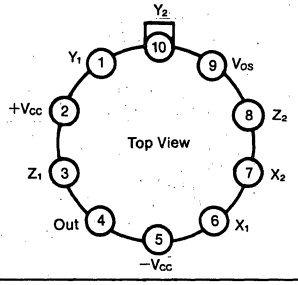
For applications information, see the standard product data sheet.

With the following exceptions, all Electrical Specifications are as per the specifications table included in the standard product data sheet (page 4-23).

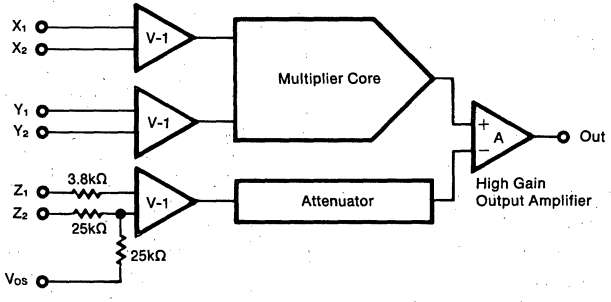
Full temperature range and V_{CC} = ±15V unless otherwise stated.

ELECTRICAL SPECIFICATION	MODEL	MIN	MAX	UNITS
Total Error (−10V < X, Y < 10V; FSR = ±10V): T_{AMB} = +25°C	MPY100AM	—	±2.0	%FSR
	MPY100BM	—	±1.0	%FSR
	MPY100SM/CM	—	±0.5	%FSR
vs Temperature: T_{AMB} = −25°C to +85°C	MPY100AM	—	±0.05	%FSR/°C
	MPY100BM/CM	—	±0.02	%FSR/°C
T_{AMB} = −55°C to +125°C	MPY100SM	—	±0.05	%FSR/°C
Output Offset: T_{AMB} = +25°C	MPY100AM	—	±100	mV
	MPY100BM/SM	—	±50	mV
	MPY100CM	—	±25	mV
vs Temperature: T_{AMB} = −25°C to +85°C	MPY100AM/BM	—	±2.0	mV/°C
	MPY100CM	—	±0.7	mV/°C
T_{AMB} = −55°C to +125°C	MPY100SM	—	±0.7	mV/°C
Power Supply Current (I_{CC}): T_{AMB} = +25°C		—	±9.5	mA

PIN CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



PACKAGE OUTLINE—TO-100 (see page 13-7)

BURR-BROWN®

OPA27

BS Number: BS9460-F0649

ULTRA-LOW NOISE PRECISION OPERATIONAL AMPLIFIER

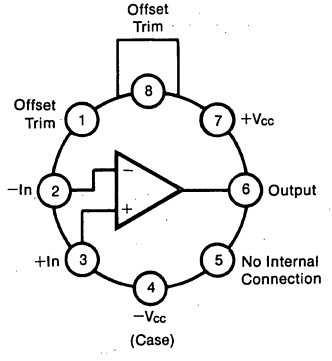
For applications information, see the standard product data sheet.

With the following exceptions, all Electrical Specifications are as per the specifications table included in the standard product data sheet (page 1-17).

T_{AMB} = 25°C unless otherwise stated, V_{CC} = ±15V unless otherwise stated.

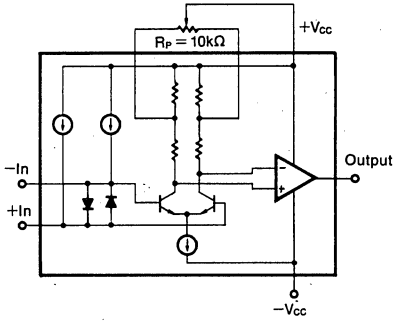
ELECTRICAL SPECIFICATION	MODEL	MIN	MAX	UNITS
Large Signal Voltage Gain (A_{VOL}): Full temp, range, $R_L \geq 2k\Omega$, $V_O = \pm 10V$	OPA27A	115	—	dB
	OPA27B	113	—	dB
	OPA27C	109	—	dB
	OPA27E	117	—	dB
	OPA27F	116	—	dB
	OPA27G	113	—	dB
Output Impedance (Z_O)		—	250	Ω
Slew Rate ($\Delta V_O/\Delta T$)	OPA27A/B/C/E/F/G	1.5	—	V/μs
Large Signal Voltage Gain (A_{VOL}): $R_L \geq 2k\Omega$, $V_O = \pm 10V$	OPA27A/B/E/F	120	—	dB
	OPA27C/G	116	—	dB
Gain Bandwidth Product (stable for $A_V \geq 1$)	OPA27A/B/C/E/F/G	5.0	—	MHz

PIN CONNECTION DIAGRAM



Top View

FUNCTIONAL DIAGRAM



NOTE: Offset null circuit is optional.

PACKAGE OUTLINE—TO-99 (see page 13-7)

BURR-BROWN®

OPA37

BS Number: BS9460-F0650

ULTRA-LOW NOISE PRECISION OPERATIONAL AMPLIFIER

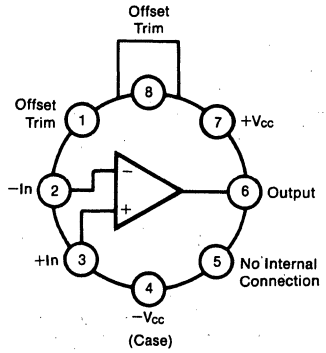
For applications information, see the standard product data sheet.

With the following exceptions, all Electrical Specifications are as per the specifications table included in the standard product data sheet (page 1-17).

T_{AMB} = 25°C unless otherwise stated, V_{CC} = ±15V unless otherwise stated.

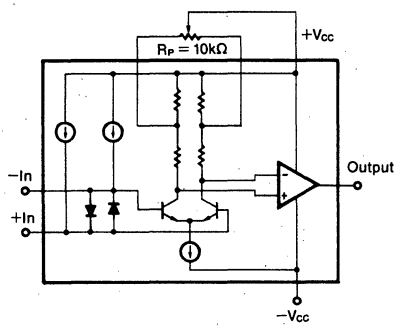
ELECTRICAL SPECIFICATION	MODEL	MIN	MAX	UNITS
Large Signal Voltage Gain (A_{VOL}): $R_L \geq 2k\Omega$, $V_O = \pm 10V$	OPA37A	115	—	dB
	OPA37B	113	—	dB
	OPA37C	109	—	dB
	OPA37E	117	—	dB
	OPA37F	116	—	dB
	OPA37G	113	—	dB
Output Impedance (Z_O)		—	250	Ω
Large Signal Voltage Gain (A_{VOL}): $R_L \geq 2k\Omega$, $V_O = \pm 10V$	OPA37A/B/E/F	120	—	dB
	OPA37C/G	116	—	dB
Gain Bandwidth Product (stable for $A_V > 5$)		45	—	MHz

PIN CONNECTION DIAGRAM



Top View

FUNCTIONAL DIAGRAM



NOTE: Offset null circuit is optional.

PACKAGE OUTLINE—TO-99 (see page 13-7)

BURR-BROWN®

OPA111

BS Number: BS9460-F0647

LOW NOISE PRECISION *Difet*® OPERATIONAL AMPLIFIER

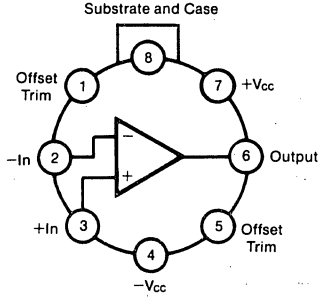
For applications information, see the standard product data sheet.

With the following exceptions, all Electrical Specifications are as per the specifications table included in the standard product data sheet (page 1-53).

$T_{AMB} = 25°C$, $V_{CC} = \pm 15V$.

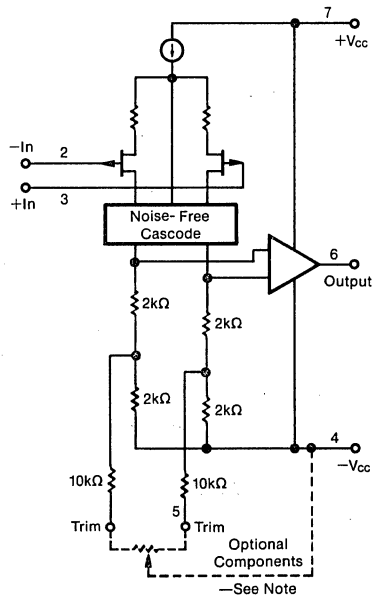
ELECTRICAL SPECIFICATION	MIN	MAX	UNITS
Output Impedance (Z_O)	—	250	Ω
Full Power Response: 20V p-p, $R_L = 2k\Omega$	16	—	kHz
Acquisition Time (t_{AQU})	—	30	μs

PIN CONNECTION DIAGRAM



Top View

FUNCTIONAL DIAGRAM



Case and substrate pin 8 connected to ground.

NOTE: The addition of the offset trim pot will degrade the $\Delta V_{IOS}/\Delta_t$ performance.

PACKAGE OUTLINE—TO-99 (see page 13-7)

BURR-BROWN®

OPA121

BS Number: BS9460-F0648

LOW COST PRECISION *Difet*® OPERATIONAL AMPLIFIER

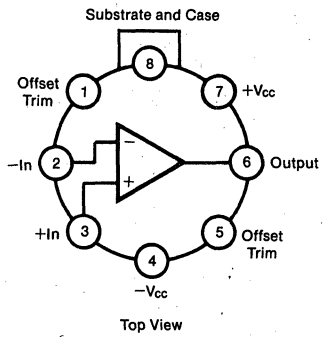
For applications information, see the standard product data sheet.

With the following exceptions, all Electrical Specifications are as per the specifications table included in the standard product data sheet (page 1-67).

T_{AMB} = +25°C, V_{CC} = ±15V.

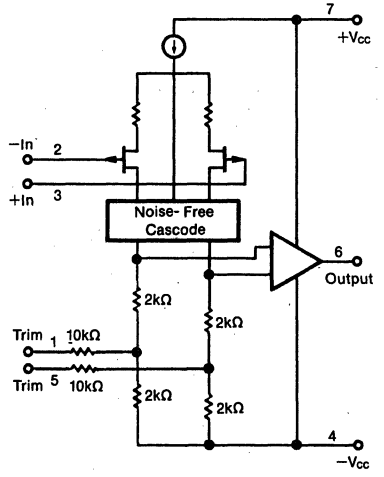
ELECTRICAL SPECIFICATION	MIN	MAX	UNITS
Output Impedance (Z_O)	—	300	Ω
Input Impedance (Z_{IN})	10^8	—	Ω
Acquisition Time (t_{AQU})	—	35	µs

PIN CONNECTION DIAGRAM



Top View

FUNCTIONAL DIAGRAM



Case and substrate pin 8 connected to ground.

PACKAGE OUTLINE—TO-99 (see page 13-7)

BURR-BROWN®

VFC32

BS Number: BS9400-G0100

VOLTAGE-TO-FREQUENCY CONVERTER AND FREQUENCY-TO-VOLTAGE CONVERTER

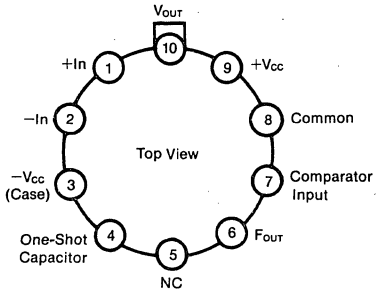
For applications information, see the standard product data sheet.

With the following exceptions, all Electrical Specifications are as per the specifications table included in the standard product data sheet (page 10-3).

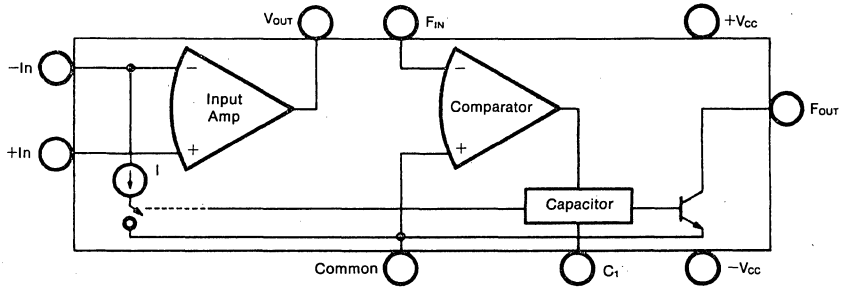
T_{AMB} = 25°C, V_{CC} = ±15V.

ELECTRICAL SPECIFICATION	MIN	MAX	UNITS
Pulse Width Range (t_{PW}), F to V configuration	0.1	150kΩ/F_{MAX}	µs
Gain Error	—	±10	%FSR

PIN CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



PACKAGE OUTLINE—TO-100 (see page 13-7)

BURR-BROWN®

VFC62

BS Number: BS9400-G0104

VOLTAGE-TO-FREQUENCY CONVERTER AND FREQUENCY-TO-VOLTAGE CONVERTER

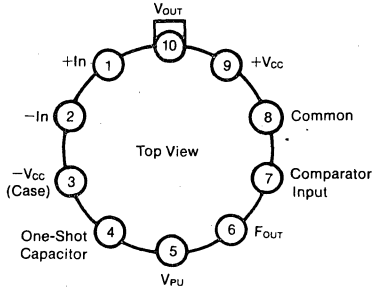
For applications information, see the standard product data sheet.

With the following exceptions, all Electrical Specifications are as per the specifications table included in the standard product data sheet (page 10-17).

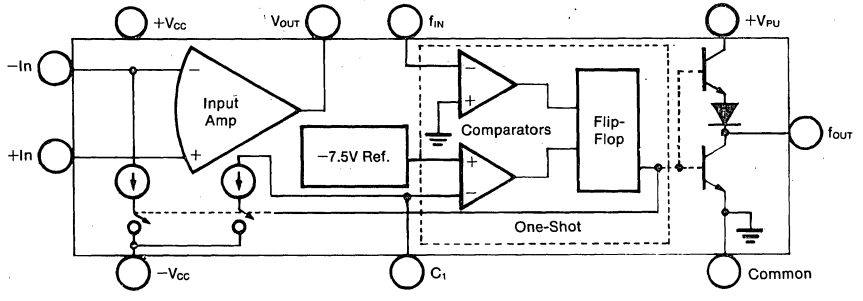
T_{AMB} = 25°C, V_{CC} = ±15V.

ELECTRICAL SPECIFICATION	MIN	MAX	UNITS
Supply Current, each supply (I_{CC}) Source Current Logic "1" (I_{OH}): V_{PU} = 5.0V, V_{OH} = 2.4V	— −9.0	±7.5 —	mA mA
Voltage Logic "1"(V_{OH}): 3.5V < V_{PU} < 15V, I_{OH} = 0mA	V_{PU} − 2.6V	V_{PU}	V
Fall Time (t_{THL}): I_{OUT} = 5.0mA, C_{LOAD} = 500pF	—	400	ns
Output Voltage (V_{OH}): F to V configuration, I_O = 7.0mA	—	+10	V
Output Driver Supply Operating Voltage (V_{PU})	+3.5	V_{CC}	V

PIN CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



PACKAGE OUTLINE—TO-100 (see page 13-7)

BURR-BROWN®

VFC320

BS Number: BS9400-G0101

VOLTAGE-TO-FREQUENCY CONVERTER AND FREQUENCY-TO-VOLTAGE CONVERTER

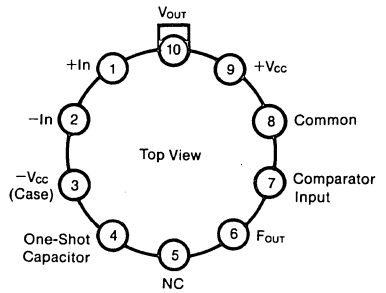
For applications information, see the standard product data sheet.

With the following exceptions, all Electrical Specifications are as per the specifications table included in the standard product data sheet (page 10-40).

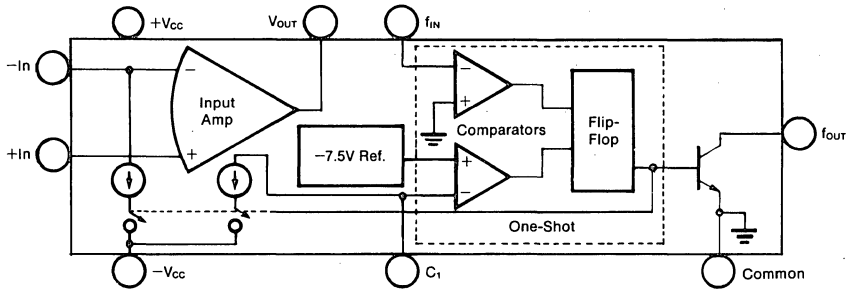
T_{AMB} = 25°C, V_{CC} = ±15V.

ELECTRICAL SPECIFICATION	MIN	MAX	UNITS
Fall Time (t_{THL}): I_{OUT} = 5.0mA, C_{LOAD} = 500pF	—	400	ns
Output Voltage (V_{OH}): F to V configuration, I_O = 7.0mA	—	+10	V
Supply Current (I_{CC}), each supply	—	±7.5	mA

PIN CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



PACKAGE OUTLINE—TO-100 (see page 13-7)

BURR-BROWN®

4213

BS Number: BS9400-G0082

MULTIPLIER-DIVIDER

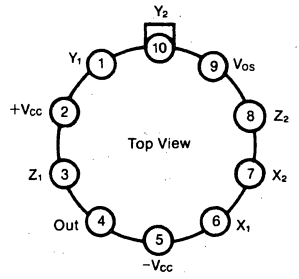
For applications information, see the standard product data sheet.

With the following exceptions, all Electrical Specifications are as per the specifications table included in the standard product data sheet (page 4-105).

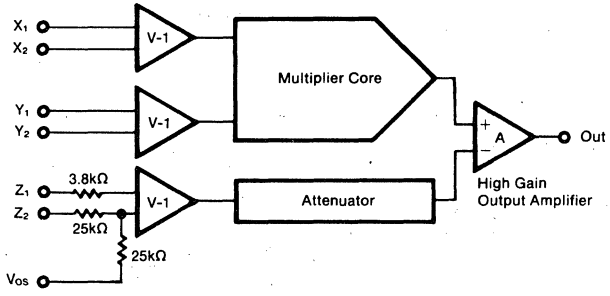
T_{AMB} = 25°C, V_{CC} = ±15V.

ELECTRICAL SPECIFICATION	MIN	MAX	UNITS
Power Supply Current (I_{CC}): T_{AMB} = 25°C	—	±9.5	mA

PIN CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



PACKAGE OUTLINE—TO-100 (see page 13-7)

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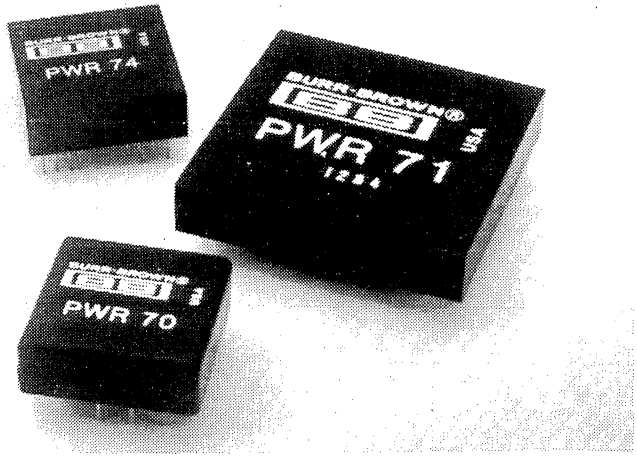
MODULAR POWER SUPPLIES



A broad line of compact, easily mounted encapsulated power supplies, AC/DC and DC/DC converters, are available from Burr-Brown. They are designed to power analog interface circuitry involving operational, instrumentation and isolation amplifiers, A/D and D/A converters and analog circuit functions in digital and analog systems. DC/DC converters offer high input-output isolation for those computer interface applications where analog circuitry must be floated independent of digital ground.

We provide a wide range of output voltages and current. International input voltage ratings are also available.

Burr-Brown offers one of the largest, most complete selections of high performance DC/DC converters in the industry. The new Power/Plus Series includes over 400 feature-packed, low cost converters to meet demanding power conversion requirements in such applications as process control, telecommunications, portable equipment, automatic test systems and medical, airborne and shipboard electronics systems.

Surface-Mounted Device (SMD) technology is used exclusively in the production of Power/Plus converters, providing higher levels of DC/DC circuit performance in compact, rugged packages—all at no additional cost. Standard features of the Power/Plus Series—normally costly options in other conventional designs—include: input and output filtering; six-sided shielding; input overvoltage and output short-circuit protection; nonconductive packages; and, full UL544, VDE750 and CSA C22.2 dielectric withstand test compliance.

Power Plus converters also offer the best isolation voltage performance available—1000V peak minimum isolation voltage and 25pF isolation capacitance—and every unit is tested at 240VAC for barrier capacitance and leakage current.

SELECTION GUIDE

AC/DC CONVERTERS								
Description	Model	Rated Output	Rated Input	Regulation No Load to Full Load	Regulation Overrated Line Voltage	Output[1] Ripple/ Noise	Package	Page
Dual ±15VDC Supply P.C.B. Mount	550	±15V, ±25mA	105VAC to 125VAC, 50Hz to 400Hz [2] [3] [4]	±0.1%	±0.05%	2mV	Module	14-3
	551	±15V, ±50mA		±0.05%	±0.05%	0.5mV	Module	14-3
	552	±15V, ±100mA		±0.05%	±0.05%	0.5mV	Module	14-3
	553	±15V, ±200mA		±0.05%	±0.05%	0.5mV	Module	14-3
	554	±15V, ±350mA		±0.02%	±0.02%	0.5mV	Module	14-3
Dual ±15VDC Supply Chassis Mount	556	±15V, ±200mA	105VAC to 125VAC, 50Hz to 400Hz [2] [3] [4]	±0.05%	±0.05%	1mV	Module	14-3
	558	±15V, ±500mA		±0.05%	±0.05%	1mV	Module	14-3
5VDC Supply P.C.B. Mount	560	5V[5], ±250mA	105VAC to 125VAC, 50Hz to 400Hz [2] [3] [4]	±0.1%	±0.05%	1mV	Module	14-3
	561	5V[5], ±500mA		±0.1%	±0.05%	1mV	Module	14-3
	562	5V[5], ±1000mA		±0.1%	±0.05%	1mV	Module	14-3

DC/DC CONVERTERS							
Description	Model	Input	Output	Isolation	Leakage Current	Package	Page
Regulated	546	4.5VDC to 5.5VDC 400mA	Single-Bipolar ±15V, 120mA	300V	Not Specified	Module	14-3
Unregulated	PWR1xx	5VDC to 48VDC	450mW	1000VDC	5µA, max	Module	14-9
Unregulated	PWR2xx	5VDC to 48VDC	1.5W	1000VDC	5µA, max	Module	14-11
Unregulated	PWR3xx	5VDC to 48VDC	2W, dual channel	1000VDC	5µA, max	Module	14-13
Unregulated	PWR4xx	5VDC to 48VDC	3W	1000VDC	5µA, max	Module	14-15
Unregulated	PWR5xx	5VDC to 48VDC	4W	1000VDC	15µA, max	Module	14-17
Regulated	PWR6xx	5VDC to 48VDC	2W	1000VDC	20µA, rms	Module	14-19
Regulated	PWR7xx	5VDC to 48VDC	5W	1000VDC	25µA, rms	Module	14-23
Unregulated	PWR8xx	5VDC to 48VDC	5W, triple output	1000VDC	5µA, max	Module	14-25
Isolated	PWR70	10VDC to 18VDC	±15VDC, ±15mA	2000Vp	2µA, max	Module	14-27
	PWR71	10VDC to 18VDC	±15VDC, ±25mA	1000VDC	3µA, max	Module	14-29
	PWR72	5VDC to 22VDC	±15VDC, ±100mA	1000VDC	3µA, max	Module	14-31
	PWR74	10VDC to 20 VDC	±15VDC, ±25mA	1500V_{pk}	2µA, max	Module	14-33
	700	10VDC to 18VDC 89mA	±10VDC to ±18VDC (±1V tolerance) at 60mA total	1500Vp	1µA, max	Module	14-35
	700U[5]	10VDC to 18VDC 89mA	±10VDC to ±18VDC (±1V tolerance) at 60mA total	2000Vp	1µA, max	Module	14-35
	710[6]	10VDC to 18VDC 100mA	Four sets of outputs each set: ±10VDC to ±18VDC (±1V tolerance) at 76mA total all outputs	1000Vp	1µA, max	Module	14-37
	722 722BG	5VDC to 16VDC 120mA	Two-Bipolar ±15V, 64mA	3500V[5] 8000V[6]	1µA at 240V, 60Hz	DIP	14-41
	724	5VDC to 16VDC 125mA	Four-Bipolar ±8V	1000V[5] 3000V[6]	1µA at 240V, 60Hz	DIP	14-45

NOTES: (1) At full load, rms (max). (2) 205VAC, 50Hz to 400Hz option available. (3) 90VAC to 110VAC, 50Hz to 400Hz option available. (4) 220VAC to 260VAC, 50Hz to 400Hz option available. (5) Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields. Model 700M and 700UM are similar to Models 700/700U but, in addition, they are 100% screened to patient-connected circuit requirements for the leakage current (par. 27.5) and withstand voltage (par. 31.11) of UL544. Additional per unit charge for 700M or 700UM. (6) Model 710 provides 4 channels (sets) of isolated outputs.

BURR-BROWN®

MODULAR AC/DC AND DC/DC POWER SUPPLIES

FEATURES

- PC BOARD-COMPATIBLE
- CHASSIS MOUNTABLE
- HIGH RELIABILITY, FULLY TESTED
- LOW INSTALLED COST
- COMPLETELY SELF-CONTAINED

DESCRIPTION

Burr-Brown standard series power supplies and DC/DC converters provide maximum flexibility in systems design. They are particularly useful for powering analog interface circuitry in digital and analog systems and have a wide range of output voltage and current ratings. They are completely self-contained, ready to use encapsulated units. For most OEM users they eliminate engineering start-up/documentation costs and manufacturing delays at prices generally far below internal manufacturing costs.

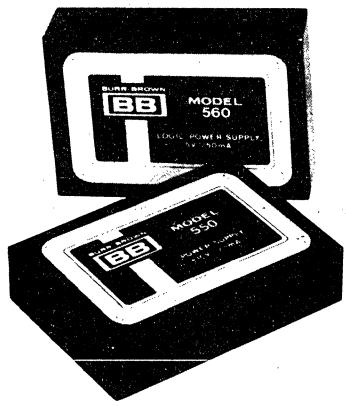
The AC/DC power supplies have a current limiting circuit in the output stage, designed to withstand output short-circuit-to-common or substantial overload conditions for long periods of time, without causing damage to the power supply.

In applications where isolation between input and output is an essential requirement (such as powering isolation amplifier input and output stages) the Burr-Brown isolated DC/DC converters provide up to 1500VDC of isolation protection.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

MODULAR AC/DC POWER SUPPLIES

- PC BOARD/CHASSIS MOUNT TYPE
- ±15VDC DUAL OUTPUTS, +5VDC SINGLE OUTPUT
- 25mA TO 1000mA CURRENT CAPABILITY
- CURRENT-LIMITED OUTPUTS FOR SHORT CIRCUIT PROTECTION
- INTERNATIONAL AC INPUT VOLTAGE OPTIONS AVAILABLE



SPECIFICATIONS COMMON TO ALL AC/DC POWER SUPPLIES

Input Voltage: 105VAC to 125VAC, 50Hz to 400Hz. For international AC input voltages see options E, F, and H.

Input Isolation: 50MΩ

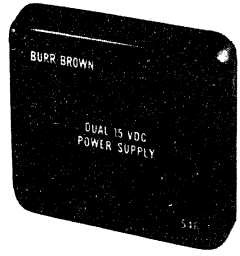
Breakdown Voltage: 500V, min.

Output Voltage: Error, ±1%; temperature coefficient, ±0.02%/°C

Output Protection: Current limiting protection for output to withstand overloads and direct short circuits to ground to prevent excessive temperature within the unit.

Rated Operating Temperature: -25°C to +71°C. May be operated at higher temperatures with proper derating.

Storage Temperature: -25°C to +85°C.



DC/DC CONVERTERS, ±15VDC OUTPUT

- REGULATED ±15VDC FROM UNREGULATED DC INPUT
- DIFFERENT DC INPUT VOLTAGE RANGES AVAILABLE
- HIGH CURRENT CAPABILITY WITH CURRENT LIMIT PROTECTION
- ISOLATED DC/DC CONVERTERS, 75% EFFICIENCY AT FULL LOAD
- LOW COUPLING CAPACITANCE (8pF)
- HIGH ISOLATION VOLTAGE (1500VDC)
- LOW EMI, SHIELDED AND UNSHIELDED UNITS
- UP TO FOUR FULLY ISOLATED OUTPUT CHANNELS (Model 710)
- SMALL SIZE

AC/DC CONVERTERS

	Dual ±15VDC Supplies							5VDC Logic Supplies		
	PC Board Mount					Chassis Mount		PC Board Mount		
Model	550	551	552	553	554	556	558	560	561	562
RATED OUTPUT										
Voltage (nom)	±15V	±15V	±15V	±15V	±15V	±15V	±15V	5V[1]	5V[1][2]	5V[1][2]
Current (max)	±25mA	±50mA	±100mA	±200mA	±350mA	±200mA	±500mA	250mA	500mA	1000mA
RATED INPUT										
Voltage	105 - 125VAC, 50 - 400Hz					105 - 125VAC 50 - 400Hz		105 - 125VAC, 50 - 400Hz		
Options[3]	E, F, H					E,F,H		E, F, H		
REGULATION										
No load to full load (max)	±0.1%	±0.05%	±0.05%	±0.05%	±0.02%	±0.05%	±0.05%	±0.1%	±0.1%	±0.1%
Over rated line voltage (max)	±0.05%	±0.05%	±0.05%	±0.05%	±0.02%	±0.05%	±0.05%	±0.05%	±0.05%	±0.05%
OUTPUT RIPPLE AND NOISE										
At full load, rms (max)	2mV	0.5mV	0.5mV	0.5mV	0.5mV	1mV	1mV	1mV	1mV	1mV

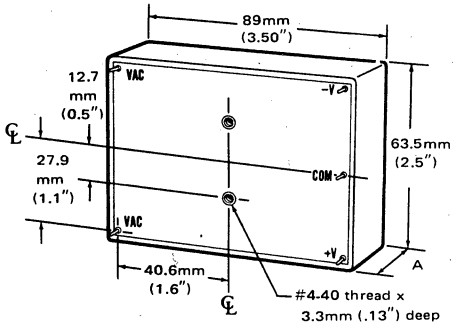
DC/DC CONVERTERS ±15VDC Output

	Low Profile	Isolated[6]	
MODEL	546	700/700U[4]	710[5]
RATED INPUT			
Voltage	4.5VDC to 5.5VDC	10VDC to 18VDC	10VDC to 18VDC
Current, Quiescent	400mA, max	20mA at ±3mA load	40mA at total output of 24mA
Current, full load	1.8A, max	±100mA max at ±30mA load	110mA at total output of 76mA
RATED OUTPUT			
Voltage (no load)	15V	$\pm V_{IN}$ w/ 1V tolerance	4 sets of $\pm V_{IN}$ w/1V tolerance
Current	120mA, max	total 60mA, max	total 76mA max; any single output -60mA, max
Short circuit current	250mA, max	120mA, max	120mA, max
REGULATION			
Line at full load	0.1%, max	—	—
Load, zero to full load	0.02% typ, 0.1% max	35mV/mA	75mV/mA
OUTPUT VOLTAGE TEMP. COEFFICIENT	±3mV °C	—	—
OUTPUT RIPPLE	10mV peak, typ; 20mV peak, max; 0.8mV, rms max	±15mV peak at ±3mA load; ±80mV peak, max, at ±30mA load	±25mV peak at ±3mA load; ±80mV peak; max, at ±9.5mA load
INPUT-OUTPUT ISOLATION			
Test voltage, 5sec at 60Hz		4200Vp/5000Vp	2200V, rms
Voltage, continuous, derated	300VDC	1500Vp/2000Vp	600V, rms, 1000Vp
Impedance	$10^{10}\Omega \parallel 50pF$	$10^{10}\Omega \parallel 5pF / 10^{10}\Omega \parallel 3pF$	$10^{10}\Omega \parallel 8pF$
Leakage current at 240V 60Hz, tested		1μA, max	1μA, max
TEMPERATURE RANGE			
Operating	0°C to 71°C	-25°C to +85°C	-25°C to +85°C
Storage	-55°C to +100°C	-55°C to +125°C	-55°C to +110°C

1. The output may be connected as +5V or -5V.
2. These 5V supplies have over-voltage protection which limits the output voltage to 7V (max) in a fault condition.
3. International input voltage rating available. Specify: E option - 205VAC to 240VAC, 50Hz to 400Hz.
   F option - 90VAC to 110VAC, 50Hz to 400Hz.
   H option - 220VAC to 260VAC, 50Hz to 400Hz.
4. Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields. Model 700M and 700UM are similar to Models 700 700U but, in addition, they are 100% screened to patient connected circuit requirements for the leakage current (par. 27.5) and dielectric withstand voltage (par. 31.11) of UL544. See Product Data Sheet for complete specifications.
5. Model 710 provides 4 channels (sets) of isolated outputs. See Product Data Sheet for complete specifications.
6. For newer designs, the models 722 and 724 (hybrid isolated DC/DC converters) which are smaller in size and better in performance are recommended. Please refer to models 722 and 724 product data sheets.

PACKAGE DRAWINGS

DRAWING NO. 1



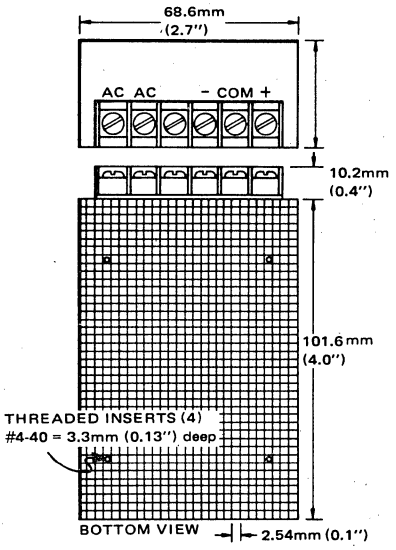
Pin Diameter 1.02mm (0.04")
* No Connection for Models 560, 561, 562.

For Models 550, 551, 560 – A = 22.2mm (0.875")
Weight: 340 grams (12 oz)

For Models 552, 553, 561, 562 – A = 32mm (1.25")
Weight: 425 grams (15 oz)

For Model 554 – A = 4.1cm (1.62")
Weight: 750 grams (26 oz)

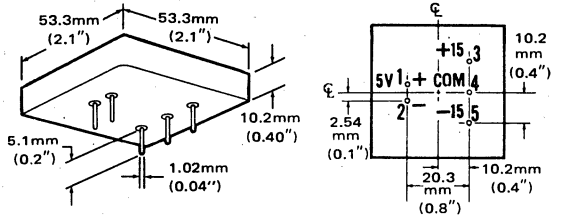
DRAWING NO. 2



For Model 556 – A = 36.6mm (1.44")

For Model 558 – A = 50.8mm (2.00")

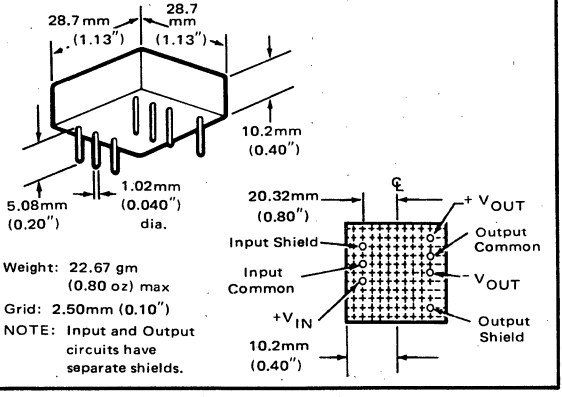
DRAWING NO. 3 Model 546



BOTTOM VIEW

WEIGHT - 50 grams (1.7 oz)

DRAWING NO. 4 Model 700

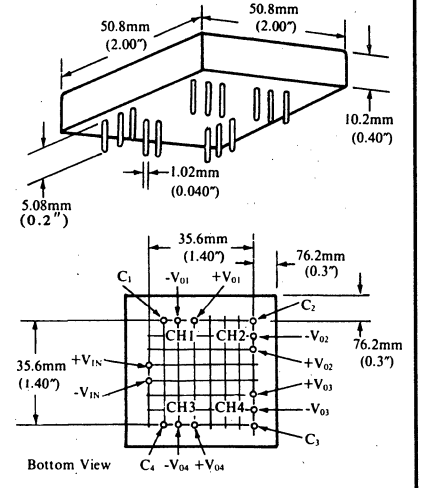


Weight: 22.67 gm
(0.80 oz) max

Grid: 2.50mm (0.10")

NOTE: Input and Output circuits have separate shields.

DRAWING NO. 5 Model 710



Weight: 25 grams (0.9 oz.)
Grid: 5.08mm (.20")

BURR-BROWN®

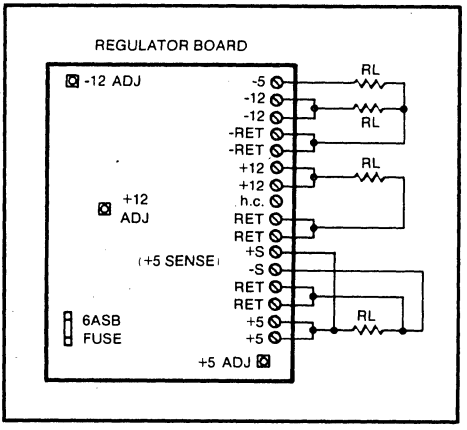
PSB100

REGULATED DC POWER SUPPLY WITH BATTERY BACK-UP

DESCRIPTION

Customers building critical control systems can now purchase a power supply with a self-contained battery back-up, eliminating the need for separate, expensive UPS systems.

PSB100 supplies all common voltages used in microcomputer systems, such as the Multibus™ system. The supply unit includes an internal 24V battery pack and charger, three TTL outputs and LED indicators that indicate power system status. Signals are provided for line power loss, low battery, and very low battery. Internal batteries provide a minimum of 30 minutes back-up at full load. An external 24VDC battery pack can be added to extend back-up time.



INPUT

Line Voltage	(1) 100-130VAC/200-260 VAC
Battery (Internal)	(2) 18-24 VAC 2.5AHR
Line Fuse	1.5ASB-115VAC/.75ASB-230VAC

(1) Operation above 130/260VAC may damage unit. 115/230VAC operation is switch selectable.

(2) An external 24VDC lead acid battery may be connected. No fuse protection is provided for the external battery.

OUTPUTS

		RIPPLE (MAX)	CURRENT	CURRENT LIMIT
+5VDC	±5%	150mV P-P	11.2A	12.0A ±5%
+12VDC	±5%	360mV P-P	1.2A	1.5A ±5%
-12VDC	±5%	360mV P-P	1.2A	1.5A ±5%
-5VDC	±1%	40mV	100mA	NONE

Multibus™ - Intel Corp.

OPERATION

1. Insure proper line and load connection to unit.
2. Insure proper line voltage selection, 115/230VAC.
3. Place AC switch in ON position; the AC indicator should light. The unit is now operating.
4. Place BATTERY switch in ON position. Battery back-up of supply is now operational. Note that the supply is not battery-startable.
5. To turn unit off once started, both the AC switch and the BATTERY switch must be in the OFF position.

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BATTERY BACK-UP

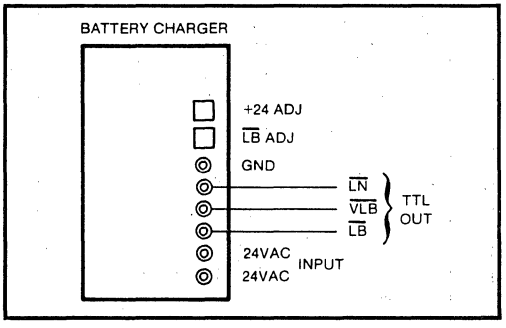
PSB100 contains a 24VDC 2.5 AHR lead acid battery pack. The battery is charged and maintained by an internal battery charger. Upon loss of AC power, the battery will maintain operation of a full load for 30 minutes minimum if fully charged. An external 24VDC rechargeable battery may be connected if desired. If an external battery is installed, the internal battery should be disconnected (remove battery fuse). The internal charger will supply 24VDC at 500mA to charge or maintain external batteries.

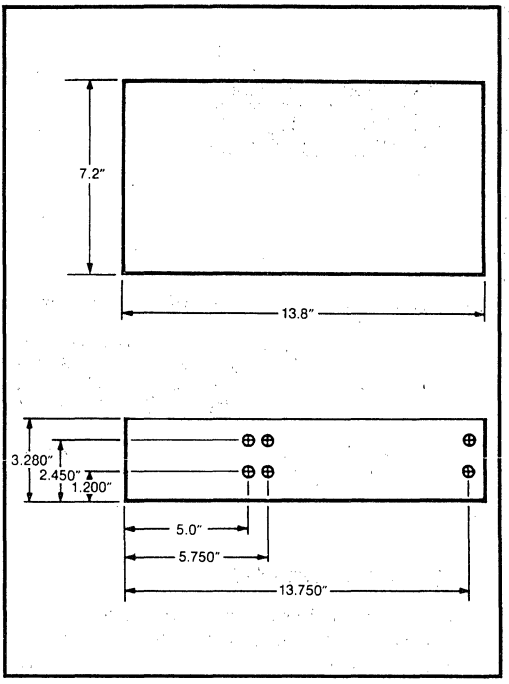
BATTERY CHARGER

24VDC at 500mA
Low battery (LB) indication 21VDC
Very low battery (VLB) indication 19.5VDC

LB and VLB indication are operational only during battery discharge cycle.

Three TTL compatible outputs are provided on the charger circuit board for low battery (LB), very low battery (VLB) and line loss (LN). All three outputs are active low.





BURR-BROWN®

PWR1XX Series

450mW Rated Output Power UNREGULATED DC/DC CONVERTER SERIES

FEATURES

- Isolation Voltage Tested per UL544, VDE750, and CSAC22.2 Dielectric Withstand Requirement
- Barrier Leakage Current 100% Tested at 240VAC
- Single Channel
- Single or Dual Unregulated Outputs
- Wide Operating Temperature Range: −40°C to +100°C
- Input and Output Filtering
- Six-Sided Shielding

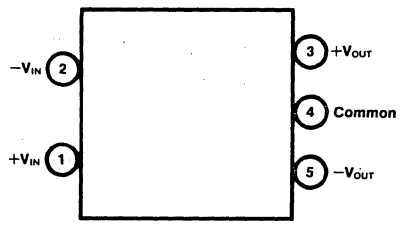
DESCRIPTION

The PWR1XX Series offers a large selection of unregulated 450mW DC/DC converters for use in such diverse applications as process control, telecommunications, portable equipment, medical systems, airborne and shipboard electronic circuits, and automatic test equipment.

Thirty-six models allow the user to select input voltages ranging from +5VDC to +48VDC and output voltages of +5, +12, +15, ±5, ±12, or ±15V.

Surface-mounted devices and manufacturing processes are used in the PWR1XX Series to give the user a device which is more environmentally rugged than most DC/DC converters. The use of surface-mount technologies also gives the PWR1XX Series superior isolation voltage. Each PWR1XX Series unit is tested in compliance with the dielectric withstand voltage requirements of UL544, VDE750, and CSAC22.2.

CONNECTION DIAGRAM



ORDERING INFORMATION

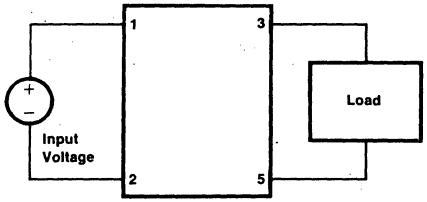
PWR 1XX /G

Device Family
PWR indicates DC/DC converter

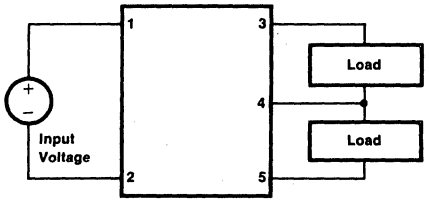
Model Number
Selected from table of Electrical Characteristics

Reliability Screening
No designator indicates standard manufacturing processing
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

TYPICAL APPLICATIONS



(Single Output Models)



(Dual Output Models)

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1]

Model	Nominal Input Voltage (VDC)	Rated Output Voltage (VDC)	Rated Output Current (mA)	Maximum Input Current (mA)
PWR100	5	5	90	180
PWR101		12	38	180
PWR102		15	30	180
PWR103		±5	±45	180
PWR104		±12	±19	180
PWR105		±15	±15	180
PWR106	12	5	90	75
PWR107		12	38	75
PWR108		15	30	75
PWR109		±5	±45	75
PWR110		±12	±19	75
PWR111		±15	±15	75
PWR112	15	5	90	60
PWR113		12	38	60
PWR114		15	30	60
PWR115		±5	±45	60
PWR116		±12	±19	60
PWR117		±15	±15	60
PWR118	24	5	90	40
PWR119		12	38	40
PWR120		15	30	40
PWR121		±5	±45	40
PWR122		±12	±19	40
PWR123		±15	±15	40
PWR124	28	5	90	35
PWR125		12	38	35
PWR126		15	30	35
PWR127		±5	±45	35
PWR128		±12	±19	35
PWR129		±15	±15	35
PWR130	48	5	90	20
PWR131		12	38	20
PWR132		15	30	20
PWR133		±5	±45	20
PWR134		±12	±19	20
PWR135		±15	±15	20

COMMON SPECIFICATIONS[1]

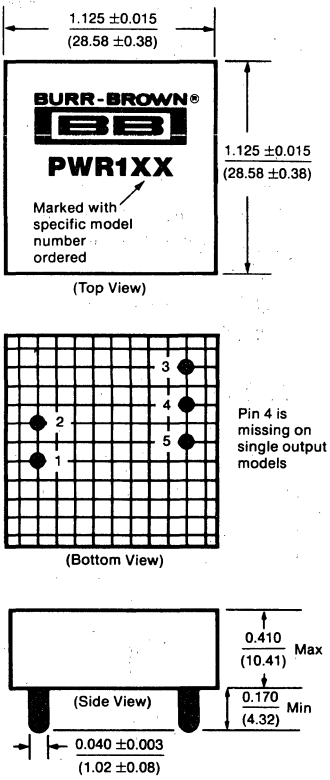
Parameter	Conditions	Min	Typ	Max	Units
INPUT					
Voltage Range			±20% of Rated Input		
Input Ripple Current	I_{LOAD} = Rated Load		30		mA, p-p
ISOLATION					
Rated Voltage		1000			VDC
Test Voltage	60Hz, 60 seconds	3000			V_{PK}
Resistance			10		GΩ
Capacitance			25		pF
Leakage Current	V_{ISO} = 240VAC			5	μA
OUTPUT					
Voltage Accuracy	I_{LOAD} = Rated Load			±5	%
Voltage (No Load)	V_{OUT} = 5 Models			7	VDC
	V_{OUT} = 12 Models			15	VDC
	V_{OUT} = 15 Models			18	VDC
Ripple Voltage	I_{LOAD} = Rated Load		50		mV, p-p
Line Regulation			1		%/%
TEMPERATURE					
Specification		−25		+85	°C
Operation		−40		+100	°C
Storage		−55		+125	°C

NOTE: (1) Specifications typical at T_A = +25°C, nominal input voltage, and rated output current unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	120% × Rated voltage
Output Short-Circuit Duration	Continuous to output common
Internal Power Dissipation	1W
Junction Temperature	+175°C
Package Thermal Resistance	90°C/W
Lead Temperature (soldering, 10 seconds)	+300°C

MECHANICAL



NOTES:

All dimensions are in inches (millimeters)

GRID: 0.100 inches (2.54 millimeters)

MATERIAL: Low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range and good electrical properties under high humidity environments. Lead material is brass with a hot-solder-dipped surface to allow ease of solderability.

BURR-BROWN®

PWR2XX Series

1.5 Watts Rated Output Power UNREGULATED DC/DC CONVERTER SERIES

FEATURES

- Isolation Voltage Tested per UL544, VDE750, and CSAC22.2 Dielectric Withstand Requirement
- Barrier Leakage Current 100% Tested at 240VAC
- Single Channel
- Single or Dual Unregulated Outputs
- Wide Operating Temperature Range: −40°C to +100°C
- Input and Output Filtering
- Six-Sided Shielding

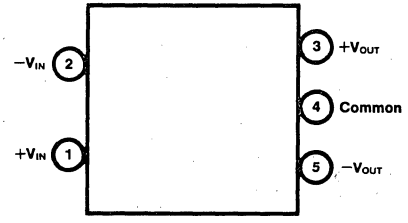
DESCRIPTION

The PWR2XX Series offers a large selection of unregulated 1.5W DC/DC converters for use in such diverse applications as process control, telecommunications, portable equipment, medical systems, airborne and shipboard electronic circuits, and automatic test equipment.

Thirty-six models allow the user to select input voltages ranging from +5VDC to +48VDC and output voltages of +5, +12, +15, ±5, ±12, or ±15VDC.

Surface-mounted devices and manufacturing processes are used in the PWR2XX Series to give the user a device which is more environmentally rugged than most DC/DC converters. The use of surface-mount technologies also gives the PWR2XX Series superior isolation voltage. Each PWR2XX Series unit is tested in compliance with the dielectric withstand voltage requirements of UL544, VDE750, and CSAC22.2.

CONNECTION DIAGRAM



ORDERING INFORMATION

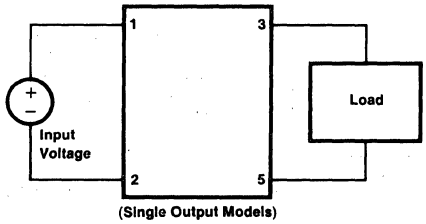
PWR 2XX /G

Device Family
PWR indicates DC/DC converter

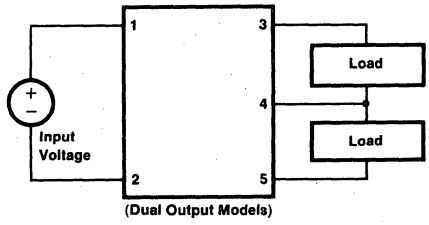
Model Number
Selected from table of Electrical Characteristics

Reliability Screening
No designator indicates standard manufacturing processing
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

TYPICAL APPLICATIONS



(Single Output Models)



(Dual Output Models)

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1]

Model	Nominal Input Voltage (VDC)	Rated Output Voltage (VDC)	Rated Output Current (mA)	Maximum Input Current (mA)
PWR200	5	5	300	545
PWR201		12	125	545
PWR202		15	100	545
PWR203		±5	±150	545
PWR204		±12	±63	545
PWR205		±15	±50	545
PWR206	12	5	300	208
PWR207		12	125	208
PWR208		15	100	208
PWR209		±5	±150	208
PWR210		±12	±63	208
PWR211		±15	±50	208
PWR212	15	5	300	167
PWR213		12	125	167
PWR214		15	100	167
PWR215		±5	±150	167
PWR216		±12	±63	167
PWR217		±15	±50	167
PWR218	24	5	300	104
PWR219		12	125	104
PWR220		15	100	104
PWR221		±5	±150	104
PWR222		±12	±63	104
PWR223		±15	±50	104
PWR224	28	5	300	92
PWR225		12	125	92
PWR226		15	100	92
PWR227		±5	±150	92
PWR228		±12	±63	92
PWR229		±15	±50	92
PWR230	48	5	300	63
PWR231		12	125	63
PWR232		15	100	63
PWR233		±5	±150	63
PWR234		±12	±63	63
PWR235		±15	±50	63

COMMON SPECIFICATIONS[1]

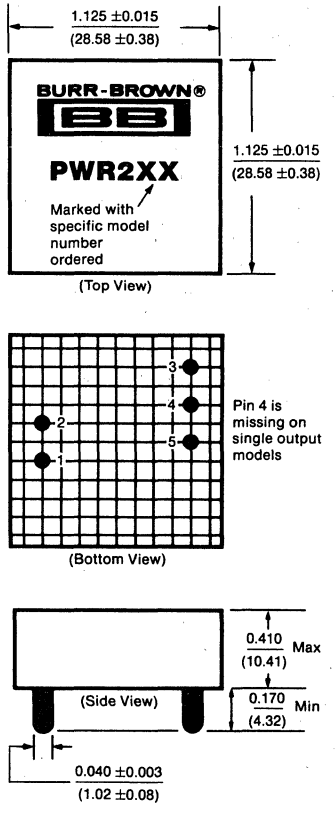
Parameter	Conditions	Min	Typ	Max	Units
INPUT					
Voltage Range			±20% of Rated Input		
Input Ripple Current	I_{LOAD} = Rated Load		50		mA, p-p
ISOLATION					
Rated Voltage		1000			VDC
Test Voltage	60Hz, 60 seconds	3000			V_{PK}
Resistance			10		GΩ
Capacitance			25		pF
Leakage Current	V_{ISO} = 240VAC			5	μA
OUTPUT					
Voltage Accuracy	I_{LOAD} = Rated Load			±5	%
Voltage (No Load)	V_{OUT} = 5V Models			7	VDC
	V_{OUT} = 12V Models			15	VDC
	V_{OUT} = 15V Models			18	VDC
Ripple Voltage	I_{LOAD} = Rated Load		75		mV, p-p
Line Regulation			1		%/%
TEMPERATURE					
Specification		−25		+85	°C
Operation		−40		+100	°C
Storage		−55		+125	°C

NOTE: (1) Specifications typical at T_A = +25°C, nominal input voltage, and rated output current unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS

Input Voltage..... 120% × rated voltage
Output Short-Circuit Duration..... Continuous to output common
Internal Power Dissipation 2W
Junction Temperature ..... +175°C
Package Thermal Resistance ..... 60°C/W
Lead Temperature
(soldering, 10 seconds) ..... +300°C

MECHANICAL



NOTES:

All dimensions are in inches (millimeters)

GRID: 0.100 inches (2.54 millimeters)

MATERIAL: Low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range and good electrical properties under high humidity environments. Lead material is brass with a hot-solder-dipped surface to allow ease of solderability.

BURR-BROWN®

PWR3XX Series

Dual-Channel, 2 Watts Rated Output Power UNREGULATED DC/DC CONVERTER SERIES

FEATURES

- **Isolation Voltage Tested per UL544, VDE750, and CSAC22.2 Dielectric Withstand Requirement**
- **Barrier Leakage Current 100% Tested at 240VAC**
- **Single Channel**
- **Single or Dual Unregulated Outputs**
- **Wide Operating Temperature Range: −40°C to +100°C**
- **Input and Output Filtering**
- **Six-Sided Shielding**

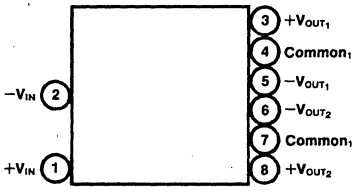
DESCRIPTION

The PWR3XX Series offers a large selection of unregulated 2W DC/DC converters for use in such diverse applications as process control, telecommunications, portable equipment, medical systems, airborne and shipboard electronic circuits, and automatic test equipment.

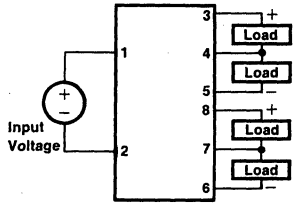
Thirty-six models allow the user to select input voltages ranging from +5VDC to +48VDC and output voltages of +5, +12, +15, ±5, ±12, or ±15VDC.

Surface-mounted devices and manufacturing processes are used in the PWR3XX Series to give the user a device which is more environmentally rugged than most DC/DC converters. The use of surface-mount technologies also gives the PWR3XX Series superior isolation voltage. Each PWR3XX Series unit is tested in compliance with the dielectric withstand voltage requirements of UL544, VDE750, and CSAC22.2.

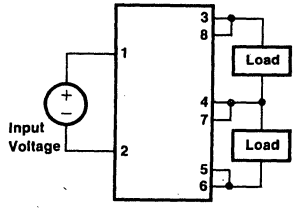
CONNECTION DIAGRAM



TYPICAL APPLICATIONS



(Dual-Channel, Dual Output)



(Single-Channel, High-Current Dual Output)

ORDERING INFORMATION

PWR 3XX /G

Device Family
PWR indicates DC/DC converter

Model Number
Selected from table of Electrical Characteristics

Reliability Screening
No designator indicates standard manufacturing processing
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1]

Model	Nominal Input Voltage (VDC)	Rated Output Voltage (VDC)	Rated Output Current (mA)	Maximum Input Current (mA)
PWR300	5	5	200	690
PWR301		12	84	690
PWR302		15	67	690
PWR303		±5	±100	690
PWR304		±12	±42	690
PWR305		±15	±34	690
PWR306	12	5	200	265
PWR307		12	84	265
PWR308		15	67	265
PWR309		±5	±100	265
PWR310		±12	±42	265
PWR311		±15	±34	265
PWR312	15	5	200	205
PWR313		12	84	205
PWR314		15	67	205
PWR315		±5	±100	205
PWR316		±12	±42	205
PWR317		±15	±34	205
PWR318	24	5	200	130
PWR319		12	84	130
PWR320		15	67	130
PWR321		±5	±100	130
PWR322		±12	±42	130
PWR323		±15	±34	130
PWR324	28	5	200	115
PWR325		12	84	115
PWR326		15	67	115
PWR327		±5	±100	115
PWR328		±12	±42	115
PWR329		±15	±34	115
PWR330	48	5	200	70
PWR331		12	84	70
PWR332		15	67	70
PWR333		±5	±100	70
PWR334		±12	±42	70
PWR335		±15	±34	70

COMMON SPECIFICATIONS[1]

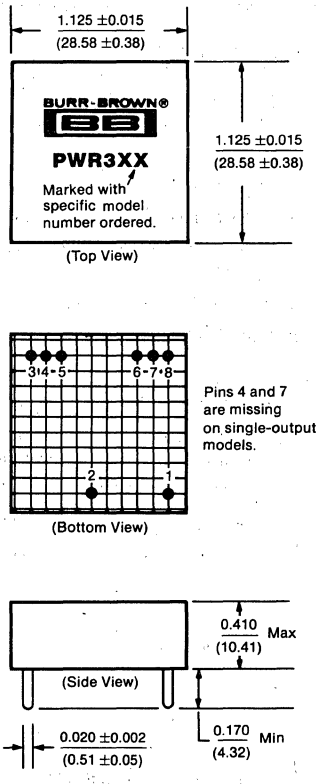
Parameter	Conditions	Min	Typ	Max	Units
INPUT					
Voltage Range			±20% of Rated Input		
Input Ripple Current	I_{LOAD} = Rated Load		30		mA, p-p
ISOLATION					
Rated Voltage		1000			VDC
Test Voltage	60Hz, 60 seconds	3000			V_{PEAK}
Resistance			10		GΩ
Capacitance			25		pF
Leakage Current	V_{ISO} = 240VAC			5	μA
OUTPUT					
Voltage Accuracy	I_{LOAD} = Rated Load			±5	%
Voltage (No Load)	V_{OUT} = 5V Models			7	VDC
	V_{OUT} = 12V Models			15	VDC
	V_{OUT} = 15V Models			18	VDC
Ripple Voltage	I_{LOAD} = Rated Load		50		mV, p-p
Line Regulation			1		%/%
TEMPERATURE					
Specification		−25		+85	°C
Operation		−40		+100	°C
Storage		−55		+125	°C

NOTE: (1) Specifications typical at T_A = +25°C, nominal input voltage, and rated output current unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS

Input Voltage..... 120% × rated voltage
Output Short-Circuit Duration..... Continuous to Output Common
Internal Power Dissipation..... 2W
Junction Temperature..... +175°C
Package Thermal Resistance..... 90°C/W
Lead Temperature
(soldering, 10 seconds)..... +300°C

MECHANICAL



NOTES:
All dimensions are in inches (millimeters)
GRID: 0.100 inches (2.54 millimeters)
MATERIAL: Low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range and good electrical properties under high humidity environments. Lead material is brass with a hot-solder-dipped surface to allow ease of solderability.

BURR-BROWN®

PWR4XX Series

3 Watts Rated Output Power UNREGULATED DC/DC CONVERTER SERIES

FEATURES

- Isolation Voltage Tested per UL544, VDE750, and CSAC22.2 Dielectric Withstand Requirement
- Barrier Leakage Current 100% Tested at 240VAC
- Single Channel
- Single or Dual Unregulated Outputs
- Wide Operating Temperature Range: −40°C to +100°C
- Input and Output Filtering
- Six-Sided Shielding

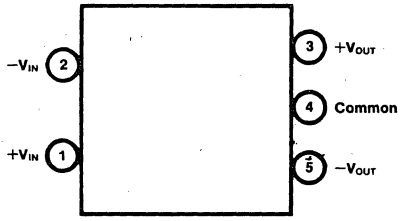
DESCRIPTION

The PWR4XX Series offers a large selection of unregulated 3W DC/DC converters for use in such diverse applications as process control, telecommunications, portable equipment, medical systems, airborne and shipboard electronic circuits, and automatic test equipment.

Thirty-six models allow the user to select input voltages ranging from +5VDC to +48VDC and output voltages of +5, +12, +15, ±5, ±12, or ±15V.

Surface-mounted devices and manufacturing processes are used in the PWR4XX Series to give the user a device which is more environmentally rugged than most DC/DC converters. The use of surface-mount technologies also gives the PWR4XX Series superior isolation voltage. Each PWR4XX Series unit is tested in compliance with the dielectric withstand voltage requirements of UL544, VDC750, and CSAC22.2.

CONNECTION DIAGRAM



ORDERING INFORMATION

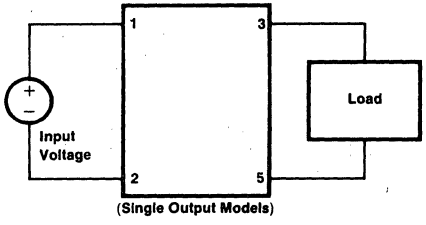
PWR 4XX /G

Device Family
PWR indicates DC/DC converter

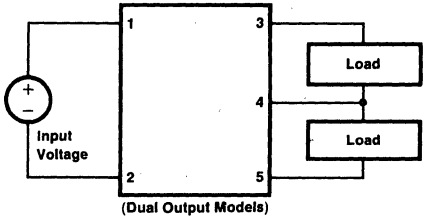
Model Number
Selected from table of Electrical Characteristics

Reliability Screening
No designator indicates standard manufacturing processing
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

TYPICAL APPLICATIONS



(Single Output Models)



(Dual Output Models)

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1]

Model	Nominal Input Voltage (VDC)	Rated Output Voltage (VDC)	Rated Output Current (mA)	Maximum Input Current (mA)
PWR400	5	5	600	1034
PWR401		12	250	1034
PWR402		15	200	1034
PWR403		±5	±300	1034
PWR404		±12	±125	1034
PWR405		±15	±100	1034
PWR406	12	5	600	380
PWR407		12	250	380
PWR408		15	200	380
PWR409		±5	±300	380
PWR410		±12	±125	380
PWR411		±15	±100	380
PWR412	15	5	600	286
PWR413		12	250	286
PWR414		15	200	286
PWR415		±5	±300	286
PWR416		±12	±125	286
PWR417		±15	±100	286
PWR418	24	5	600	184
PWR419		12	250	184
PWR420		15	200	184
PWR421		±5	±300	184
PWR422		±12	±125	184
PWR423		±15	±100	184
PWR424	28	5	600	162
PWR425		12	250	162
PWR426		15	200	162
PWR427		±5	±300	162
PWR428		±12	±125	162
PWR429		±15	±100	162
PWR430	48	5	600	105
PWR431		12	250	105
PWR432		15	200	105
PWR433		±5	±300	105
PWR434		±12	±125	105
PWR435		±15	±100	105

COMMON SPECIFICATIONS[1]

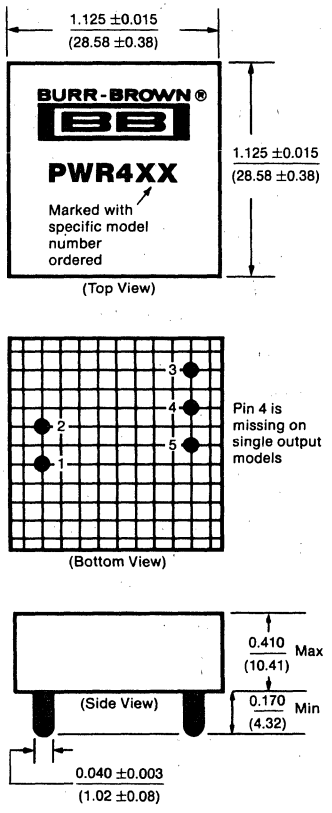
Parameter	Conditions	Min	Typ	Max	Units
INPUT					
Voltage Range			±20% of Rated Input		
Input Ripple Current	I_{LOAD} = Rated Load		70		mA, p-p
ISOLATION					
Rated Voltage		1000			VDC
Test Voltage	60Hz, 60 seconds	3000			V_{PEAK}
Resistance			10		GΩ
Capacitance			50		pF
Leakage Current	V_{ISO} = 240VAC			10	μA
OUTPUT					
Voltage Accuracy	I_{LOAD} = Rated Load			±5	%
Voltage (No Load)	V_{OUT} = 5V Models			7	VDC
	V_{OUT} = 12V Models			15	VDC
	V_{OUT} = 15V Models			18	VDC
Ripple Voltage	I_{LOAD} = Rated Load		100		mV, p-p
Line Regulation			1		%/%
TEMPERATURE					
Specification		−25		+85	°C
Operation		−40		+100	°C
Storage		−55		+125	°C

NOTE: (1) Specifications typical at T_A = +25°C, nominal input voltage, and rated output current unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS

Input Voltage..... 120% × rated voltage
Output Short-Circuit Duration..... Momentary
Internal Power Dissipation..... 2.5W
Junction Temperature..... +125°C
Package Thermal Resistance..... 16°C/W
Lead Temperature
(soldering, 10 seconds)..... +300°C

MECHANICAL



NOTES:

All dimensions are in inches (millimeters)

GRID: 0.100 inches (2.54 millimeters)

MATERIAL: Low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range and good electrical properties under high humidity environments. Lead material is brass with a hot-solder-dipped surface to allow ease of solderability.

BURR-BROWN®

PWR5XX Series

4W Rated Output Power
UNREGULATED DC/DC CONVERTER SERIES

FEATURES

- Isolation Voltage Tested per UL544, VDE750, and CSAC22.2 Dielectric Withstand Requirement
- Barrier Leakage Current 100% Tested at 240VAC
- Quad Channel
- Single or Dual Unregulated Outputs
- Wide Operating Temperature Range: −40°C to +100°C
- Input and Output Filtering
- Six-Sided Shielding

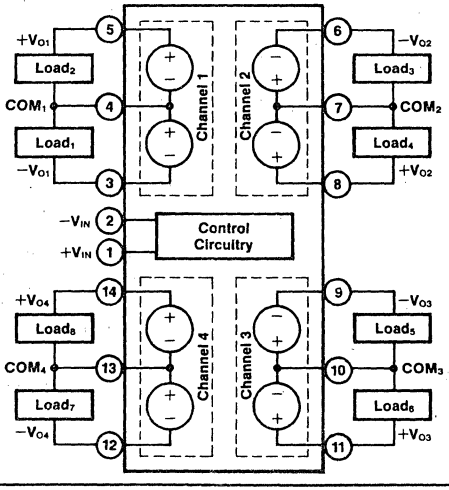
DESCRIPTION

The PWR5XX Series offers a large selection of unregulated four-watt DC/DC converters for use in diverse applications as process control, telecommunications, portable equipment, medical systems, airborne and shipboard electronic circuits, and automatic test equipment.

Thirty-six models allow the user to select input voltages ranging from +5VDC to +48VDC and output voltages of +5, +12, +15, ±5, ±12, or ±15V.

Surface-mounted devices and manufacturing processes are used in the PWR5XX Series to give the user a device which is more environmentally rugged than most DC/DC converters. The use of surface-mount technologies also gives the PWR5XX Series superior isolation voltage. Each PWR5XX Series unit is tested in compliance with the dielectric withstand voltage requirements of UL544, VDE750, and CSAC22.2.

CONNECTION DIAGRAM



ORDERING INFORMATION

PWR 5XX /G

Device Family
PWR indicates DC/DC converter

Model Number
Selected from table of Electrical Characteristics

Reliability Screening
No designator indicates standard manufacturing processing
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1]

Model	Nominal Input Voltage (VDC)	Rated[2] Output Voltage (VDC)	Rated[2] Output Current (mA)	Maximum Input Current (mA)
PWR500	5	5	200	1300
PWR501		12	84	1290
PWR502		15	67	1230
PWR503		±5	±100	1300
PWR504		±12	±42	1290
PWR505		±15	±34	1230
PWR506	12	5	200	490
PWR507		12	84	444
PWR508		15	67	444
PWR509		±5	±100	490
PWR510		±12	±42	444
PWR511		±15	±34	444
PWR512	15	5	200	390
PWR513		12	84	355
PWR514		15	67	355
PWR515		±5	±100	390
PWR516		±12	±42	355
PWR517		±15	±34	355
PWR518	24	5	200	245
PWR519		12	84	222
PWR520		15	67	222
PWR521		±5	±100	245
PWR522		±12	±42	222
PWR523		±15	±34	222
PWR524	28	5	200	210
PWR525		12	84	190
PWR526		15	67	190
PWR527		±5	±100	210
PWR528		±12	±42	190
PWR529		±15	±34	190
PWR530	48	5	200	123
PWR531		12	84	111
PWR532		15	67	111
PWR533		±5	±100	123
PWR534		±12	±42	111
PWR535		±15	±34	111

COMMON SPECIFICATIONS[1]

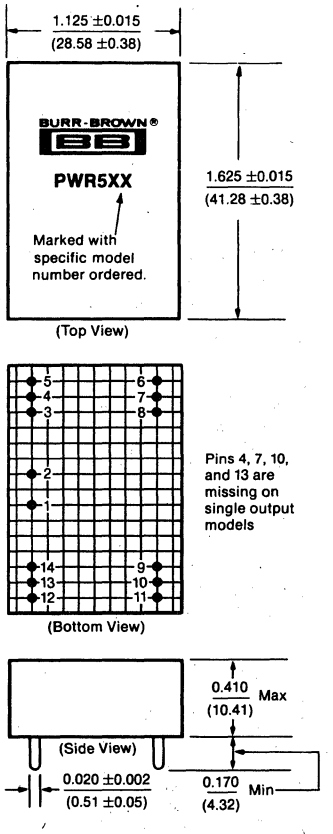
Parameter	Conditions	Min	Typ	Max	Units
INPUT					
Voltage Range			±20% of Rated Input		
Input Ripple Current	I_{LOAD} = Rated Load		70		mA, p-p
ISOLATION					
Rated Voltage		1000			VDC
Test Voltage	60Hz, 60 seconds	3000			V_{PK}
Resistance			10		GΩ
Capacitance			55		pF
Leakage Current	V_{ISO} = 240VAC			15	μA
OUTPUT					
Voltage Accuracy	I_{LOAD} = Rated Load			±5	%
Voltage (No Load)	V_{OUT} = 5 Models			7	VDC
	V_{OUT} = 12 Models			15	VDC
	V_{OUT} = 15 Models			18	VDC
Ripple Voltage	I_{LOAD} = Rated Load		1		% of V_{OUT}, p-p
Line Regulation			1		%/%
TEMPERATURE					
Specification		−25		+85	°C
Operation		−40		+100	°C
Storage		−55		+125	°C

NOTE: (1) Specifications typical at T_A = +25°C, nominal input voltage, and rated output current unless otherwise noted. (2) Specifications apply to each output.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	120% × Rated voltage
Output Short-Circuit Duration	Momentary
Internal Power Dissipation	2.5W
Junction Temperature	+150°C
Package Thermal Resistance	38°C/W
Lead Temperature (soldering, 10 seconds)	+300°C

MECHANICAL



NOTES:

All dimensions are in inches (millimeters)

GRID: 0.100 inches (2.54 millimeters)

MATERIAL: Low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range and good electrical properties under high humidity environments. Lead material is brass with a hot-solder-dipped surface to allow ease of solderability.

BURR-BROWN®

PWR6XX Series

2W Rated Output Power
REGULATED DC/DC CONVERTER SERIES

FEATURES

- Isolation Voltage Tested per UL544, VDE750, and CSAC22.2 Dielectric Withstand Requirement
- Barrier Leakage Current 100% Tested at 240VAC
- Single Channel
- Single or Dual Regulated Outputs
- Linear Output Regulation
- Wide Operating Temperature Range: −40°C to +95°C
- Input and Output Filtering
- Six-Sided Shielding

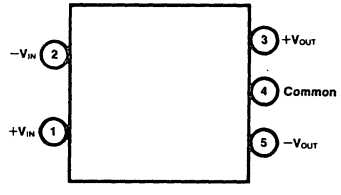
DESCRIPTION

The PWR6XX Series offers a large selection of regulated two-watt DC/DC converters for use in such diverse applications as process control, telecommunications, portable equipment, medical systems, airborne and shipboard electronic circuits, and automatic test equipment.

Thirty-six models allow the user to select input voltages ranging from +5VDC to +48VDC and output voltages of +5, +12, +15, ±5, ±12, or ±15V.

Surface-mounted devices and manufacturing processes are used in the PWR6XX Series to give the user a device which is more environmentally rugged than most DC/DC converters. The use of surface-mount technologies also gives the PWR6XX Series superior isolation voltage. Each PWR6XX Series unit is tested in compliance with the dielectric withstand voltage requirements of UL544, VDE750, and CSAC22.2.

CONNECTION DIAGRAM



ORDERING INFORMATION

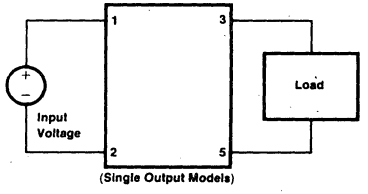
PWR 6XX /G

Device Family
PWR indicates DC/DC converter

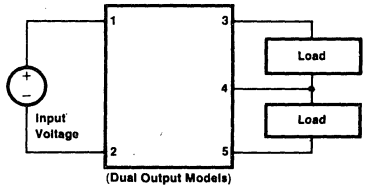
Model Number
Selected from table of Electrical Characteristics

Reliability Screening
No designator indicates standard manufacturing processing
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

TYPICAL APPLICATIONS



(Single Output Models)



(Dual Output Models)

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS[1]

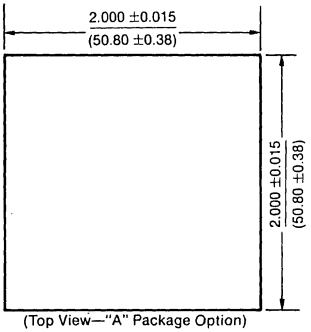
Model	Nominal Input Voltage (VDC)	Rated Output Voltage (VDC)	Rated Output Current (mA)	Input Current		Reflected Ripple Current, typ (mA)	Regulation		Efficiency, min (%)
				No Load, typ (mA)	Rated Load, typ (mA)		Line, typ (%)	Load, typ (%)	
PWR600	5	5	400	45	645	25	0.02	0.04	59
PWR601		12	167	45	597	25	0.02	0.04	63
PWR602		15	134	45	580	25	0.02	0.04	64
PWR603		±5	±200	45	645	25	0.02	0.04	60
PWR604		±12	±84	45	600	25	0.02	0.04	63
PWR605		±15	±67	45	580	25	0.02	0.04	64
PWR606	12	5	400	22	268	20	0.02	0.04	59
PWR607		12	167	22	248	20	0.02	0.04	63
PWR608		15	134	22	241	20	0.02	0.04	64
PWR609		±5	±200	22	269	20	0.02	0.04	60
PWR610		±12	±84	22	249	20	0.02	0.04	63
PWR611		±15	±67	22	243	20	0.02	0.04	64
PWR612	15	5	400	15	214	20	0.02	0.04	59
PWR613		12	167	15	199	20	0.02	0.04	63
PWR614		15	134	15	193	20	0.02	0.04	64
PWR615		±5	±200	15	215	20	0.02	0.04	60
PWR616		±12	±84	15	200	20	0.02	0.04	63
PWR617		±15	±67	15	195	20	0.02	0.04	64
PWR618	24	5	400	10	134	15	0.02	0.04	59
PWR619		12	167	10	124	15	0.02	0.04	63
PWR620		15	134	10	120	15	0.02	0.04	64
PWR621		±5	±200	10	135	15	0.02	0.04	60
PWR622		±12	±84	10	126	15	0.02	0.04	63
PWR623		±15	±67	10	122	15	0.02	0.04	64
PWR624	28	5	400	10	114	15	0.02	0.04	59
PWR625		12	167	10	107	15	0.02	0.04	63
PWR626		15	134	10	104	15	0.02	0.04	64
PWR627		±5	±200	10	114	15	0.02	0.04	60
PWR628		±12	±84	10	108	15	0.02	0.04	63
PWR629		±15	±67	10	105	15	0.02	0.04	64
PWR630	48	5	400	10	67	10	0.02	0.04	59
PWR631		12	167	10	63	10	0.02	0.04	63
PWR632		15	134	10	63	10	0.02	0.04	64
PWR633		±5	±200	10	67	10	0.02	0.04	60
PWR634		±12	±84	10	63	10	0.02	0.04	63
PWR635		±15	±67	10	63	10	0.02	0.04	64

COMMON SPECIFICATIONS[1]

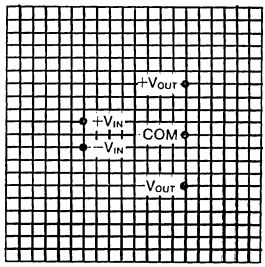
Parameter	Conditions	Min	Typ	Max	Units
INPUT					
Voltage Range	V_{IN} = 5V Models	4.5		5.5	VDC
	V_{IN} = 12V Models	10.8		13.5	VDC
	V_{IN} = 15V Models	13.8		16.5	VDC
	V_{IN} = 24V Models	21.6		26.5	VDC
	V_{IN} = 28V Models	25.2		31.0	VDC
	V_{IN} = 48V Models	43.2		53.0	VDC
ISOLATION					
Rated Voltage		1000			VDC
Test Voltage	60 Seconds, 60Hz	3000			V_{PK}
Resistance			10		GΩ
Capacitance			140		pF
Leakage Current	240V, 60Hz			20	μA, rms
OUTPUT					
Voltage Accuracy			±0.5	±1	%
Voltage Balance	Dual Output Units Only		±0.3		%
Temperature Coefficient	$-25°C \leq T_A \leq -85°C$		±0.01		%/°C
Ripple and Noise	BW = DC to 10MHz		30		mV, p-p
TEMPERATURE					
Specification		−25		+85	°C
Operation		−40		+95	°C
Storage		−55		+125	°C

NOTE: (1) Specifications typical at T_A = +25°C, nominal input voltage, and rated output current unless otherwise noted.

MECHANICAL



(Top View—"A" Package Option)



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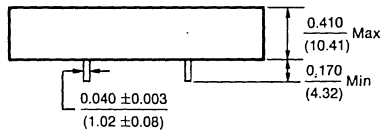

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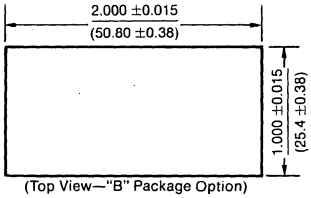

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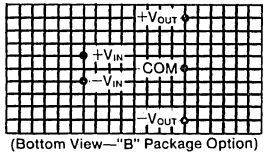

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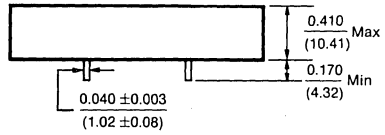

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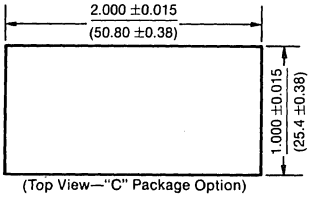

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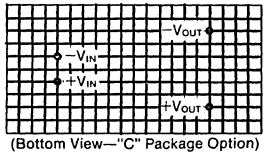

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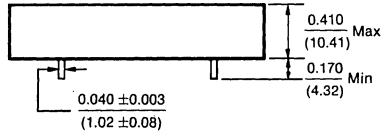

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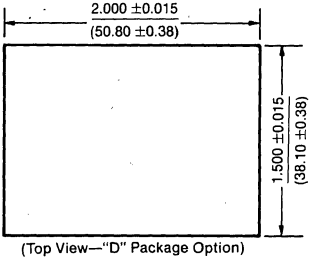

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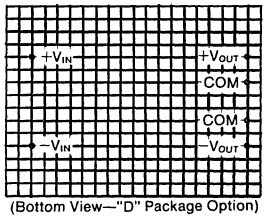
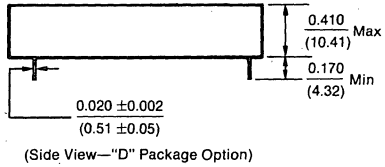


(Bottom View—"D" Package Option)



(Side View—"D" Package Option)

NOTES:

All dimensions are in inches (millimeters)

GRID: 0.100 inches (2.54 millimeters)

MATERIAL: Units are encapsulated in a low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range, and good electrical properties under high humidity environments. Lead material is brass with a hot-solder-dipped surface to allow ease of solderability.

Common pins are missing on single output models.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	120% of nominal
Output Short-Circuit Duration	5 seconds
Internal Power Dissipation	1.5W
Lead Temperature (soldering, 10 seconds)	+300°C
Junction Temperature	+150°C
Package Thermal Resistance (Junction-to-Ambient, θ_{JA})	45°C/W

APPLICATION NOTES

TESTING ISOLATION BARRIER CHARACTERISTICS

The insulation and spacings of the PWR6XX Series are 100% tested to meet the dielectric withstand requirements of UL544, paragraph 31. A 60Hz essentially sinusoidal potential is applied between the primary and secondary for a period of one minute. The potential used for this test is twice the maximum rated voltage plus 1000V. For the PWR6XX Series the test voltage is 3000V peak.

Dielectric withstand testing is intended to be done at the manufacturer's site only. This test should not be repeated. Exposing the dielectric material of the isolation barrier to repeated testing causes microscopic carbonizing of the dielectric, resulting in a weakened barrier. A low resistance path will eventually be created across the barrier.

PRESERVING ISOLATION CHARACTERISTICS

If intrinsic safety is required, care should be taken in the layout and assembly of the printed wiring board (PWB) to avoid degrading the isolation barrier of the PWR6XX. Precautionary measures include cleaning the PWB prior to installing the PWR6XX to prevent trapping contaminates under the unit. Use nonconductive spacers to keep the PWR6XX off the PWB. Use epoxy solder mask to isolate PWB conductive traces which must run under or close to the PWR6XX. In the layout of the PWB, avoid placing PWB traces under the unit. Do not use conductive inks on the PWB under the unit; e.g., inks used in inspection stamps or component identification marking.

OUTPUT POWER DISTRIBUTION

Figure 1 shows the recommended method of connecting multiple loads to the PWR6XX. Single-point power distribution prevents ground loops and interaction between parallel load circuits.

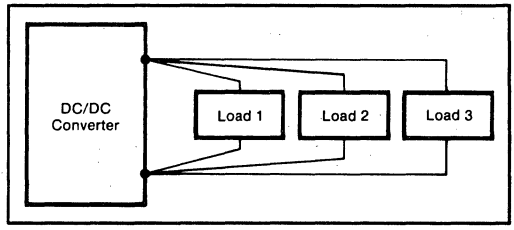


FIGURE 1. Recommended Power Distribution.

MEASURING NOISE

Measuring the input and output noise performance of a DC/DC converter is a very difficult task that should be attempted only in a controlled laboratory test environment due to extraneous noise sources.

Figure 2 illustrates two recommended methods for testing output voltage ripple and noise. Reflected input current ripple and noise should be measured with a high performance current probe. Measuring input current and noise into a "known" impedance with a voltage probe should be avoided.

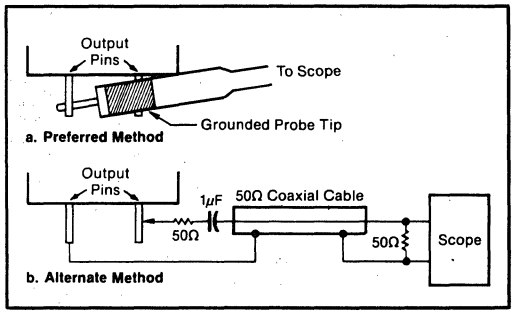


FIGURE 2. Recommended Noise Measurement Methods.

BURR-BROWN®

PWR7XX Series

5W Rated Output Power
REGULATED DC/DC CONVERTER SERIES

FEATURES

- Isolation Voltage Tested per UL544, VDE750, and CSAC22.2 Dielectric Withstand Requirement
- Barrier Leakage Current 100% Tested at 240VAC
- Single Channel
- Single or Dual Regulated Outputs
- Linear Output Regulation
- Wide Operating Temperature Range: −40°C to +100°C
- Input and Output Filtering
- Six-Sided Shielding

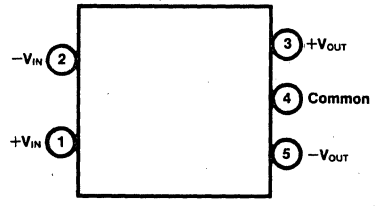
DESCRIPTION

The PWR7XX Series offers a large selection of regulated 5W DC/DC converters for use in such diverse applications as process control, telecommunications, portable equipment, medical systems, airborne and shipboard electronic circuits, and automatic test equipment.

Thirty-six models allow the user to select input voltages ranging from +5VDC to +48VDC and output voltages of +5, +12, +15, ±5, ±12, or ±15V.

Surface-mounted devices and manufacturing processes are used in the PWR7XX Series to give the user a device which is more environmentally rugged than most DC/DC converters. The use of surface-mount technologies also gives the PWR7XX Series superior isolation voltage. Each PWR7XX Series unit is tested in compliance with the dielectric withstand voltage requirements of UL544, VDC750, and CSAC22.2.

CONNECTION DIAGRAM



ORDERING INFORMATION

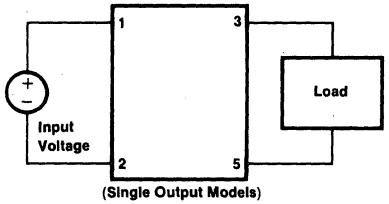
PWR 7XX / G

Device Family
PWR indicates DC/DC converter

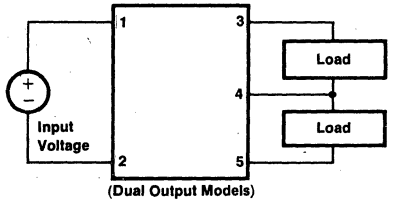
Model Number
Selected from table of Electrical Characteristics

Reliability Screening
No designator indicates standard manufacturing processing
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

TYPICAL APPLICATIONS



(Single Output Models)



(Dual Output Models)

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS[1]

Model	Nominal Input Voltage (VDC)	Rated Output Voltage (VDC)	Rated Output Current (mA)	Input Current		Reflected Ripple Current, typ (mA) p-p	Regulation		Efficiency, min (%)
				No Load, typ (mA)	Rated Load, typ (mA)		Line, typ (%)	Load, typ (%)	
PWR700	5	5	1000	168	1600	30	.02	.04	61
PWR701		12	417	168	1535	30	.02	.04	63
PWR702		15	334	168	1490	30	.02	.04	65
PWR703		±5	±500	168	1560	30	.02	.04	62
PWR704		±12	±209	168	1490	30	.02	.04	65
PWR705		±15	±167	168	1450	30	.02	.04	67
PWR706	12	5	1000	38	620	10	.02	.04	61
PWR707		12	417	38	550	10	.02	.04	63
PWR708		15	334	38	535	10	.02	.04	65
PWR709		±5	±500	38	640	10	.02	.04	62
PWR710		±12	±209	38	550	10	.02	.04	65
PWR711		±15	±167	38	535	10	.02	.04	67
PWR712	15	5	1000	35	510	10	.02	.04	61
PWR713		12	417	35	490	10	.02	.04	63
PWR714		15	334	35	470	10	.02	.04	65
PWR715		±5	±500	35	520	10	.02	.04	62
PWR716		±12	±209	35	480	10	.02	.04	65
PWR717		±15	±167	35	455	10	.02	.04	67
PWR718	24	5	1000	33	320	20	.02	.04	61
PWR719		12	417	33	305	20	.02	.04	63
PWR720		15	334	33	300	20	.02	.04	65
PWR721		±5	±500	33	330	20	.02	.04	62
PWR722		±12	±209	33	310	20	.02	.04	65
PWR723		±15	±167	33	305	20	.02	.04	67
PWR724	28	5	1000	33	280	20	.02	.04	61
PWR725		12	417	33	270	20	.02	.04	63
PWR726		15	334	33	260	20	.02	.04	65
PWR727		±5	±500	33	280	20	.02	.04	62
PWR728		±12	±209	33	270	20	.02	.04	65
PWR729		±15	±167	33	260	20	.02	.04	67
PWR730	48	5	1000	31	165	10	.02	.04	61
PWR731		12	417	31	160	10	.02	.04	63
PWR732		15	334	31	155	10	.02	.04	65
PWR733		±5	±500	31	165	10	.02	.04	62
PWR734		±12	±209	31	155	10	.02	.04	65
PWR735		±15	±167	31	155	10	.02	.04	67

COMMON SPECIFICATIONS[1]

Parameter	Conditions	Min	Typ	Max	Units
INPUT					
Voltage Range	V_{IN} = 5V Models	4.65		6	VDC
	V_{IN} = 12V Models	11.00		15	VDC
	V_{IN} = 15V Models	13.70		17	VDC
	V_{IN} = 24V Models	21.00		27	VDC
	V_{IN} = 28V Models	25.00		31	VDC
	V_{IN} = 48V Models	44.50		53	VDC
ISOLATION					
Rated Voltage		1000			VDC
Test Voltage	60 Seconds, 60Hz	3000			V_{PK}
Resistance			10		GΩ
Capacitance			170		pF
Leakage Current	240V rms, 60Hz			25	μA, rms
OUTPUT					
Voltage Accuracy			±0.5	±1	%
Voltage Balance	Dual Output Units Only		±0.3		%
Temperature Coefficient	−25°C ≤ T_A ≤ +85°C		±0.01		%/°C
Ripple and Noise	BW = DC to 10MHz		30		mV, p-p
TEMPERATURE					
Specification		−25		+85	°C
Operation		−40		+100	°C
Storage		−55		+125	°C

NOTE: (1) Specifications typical at T_A = +25°C, nominal input voltage, and rated output current unless otherwise noted.

BURR-BROWN®

PWR8XX Series

5 Watts—Triple-Output UNREGULATED DC/DC CONVERTER SERIES

FEATURES

- Isolation Voltage Tested per UL544, VDE750, and CSAC22.2 Dielectric Withstand Requirement
- Barrier Leakage Current 100% Tested at 240VAC
- Single Channel
- Single or Dual Unregulated Outputs
- Wide Operating Temperature Range: −40°C to +100°C
- Input and Output Filtering
- Six-Sided Shielding

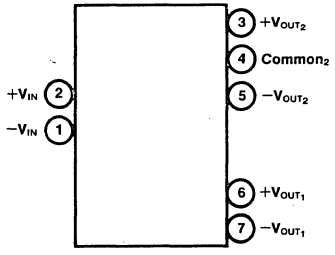
DESCRIPTION

The PWR8XX Series offers a large selection of unregulated 5W DC/DC converters for use in such diverse applications as process control, telecommunications, portable equipment, medical systems, airborne and shipboard electronic circuits, and automatic test equipment.

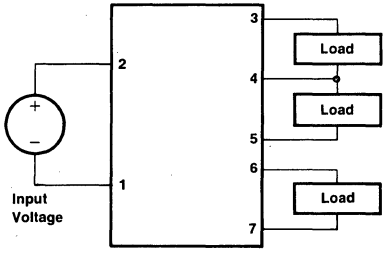
Twelve models allow the user to select input voltages ranging from +5VDC to +48VDC and output voltages of +5 and ±12VDC or ±15VDC.

Surface-mounted devices and manufacturing processes are used in the PWR8XX Series to give the user a device which is more environmentally rugged than most DC/DC converters. The use of surface-mount technologies also gives the PWR8XX Series superior isolation voltage. Each PWR8XX Series unit is tested in compliance with the dielectric withstand voltage requirements of UL544, VDC750, and CSAC22.2.

CONNECTION DIAGRAM



TYPICAL APPLICATION



ORDERING INFORMATION

PWR 8XX /G

Device Family
PWR indicates DC/DC converter

Model Number
Selected from table of Electrical Characteristics

Reliability Screening
No designator indicates standard manufacturing processing
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1]

Model	Nominal Input Voltage (VDC)	Channel 1 Rated Output		Channel 2 Rated Output		Maximum Input Current (mA)
		Voltage (VDC)	Current (mA)	Voltage (VDC)	Current (mA)	
PWR800	5	5	250	±12	±156	1665
PWR801		5	250	±15	±125	1665
PWR802	12	5	250	±12	±156	695
PWR803		5	250	±15	±125	695
PWR804	15	5	250	±12	±156	555
PWR805		5	250	±15	±125	555
PWR806	24	5	250	±12	±156	345
PWR807		5	250	±15	±125	345
PWR808	28	5	250	±12	±156	295
PWR809		5	250	±15	±125	295
PWR810	48	5	250	±12	±156	170
PWR811		5	250	±15	±125	170

COMMON SPECIFICATIONS[1]

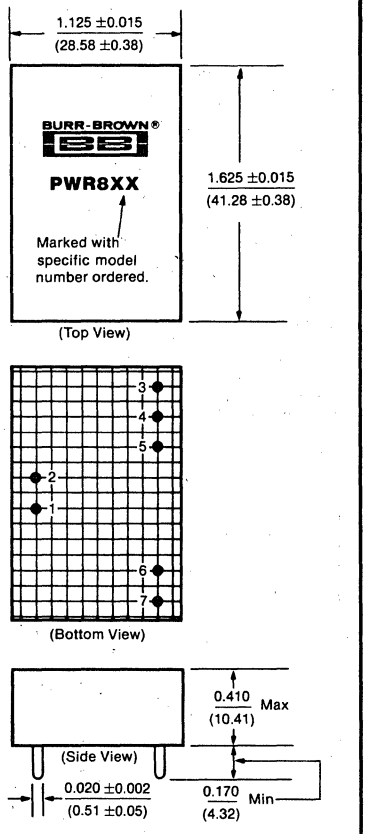
Parameter	Conditions	Min	Typ	Max	Units
INPUT					
Voltage Range			±20% of Rated Input		
Input Ripple Current	I_{LOAD} = Rated Load		50		mA, p-p
ISOLATION					
Rated Voltage		1000			VDC
Test Voltage	60Hz, 60 seconds	3000			V_{PEAK}
Resistance			10		GΩ
Capacitance			80		pF
Leakage Current	V_{ISO} = 240VAC			10	μA
OUTPUT					
Voltage Accuracy	I_{LOAD} = Rated Load			±5	%
Voltage (No Load)	V_{OUT} = 5V Models			7	VDC
	V_{OUT} = 12V Models			15	VDC
	V_{OUT} = 15V Models			18	VDC
Ripple Voltage	I_{LOAD} = Rated Load		100		mV, p-p
Line Regulation			1		%/%
TEMPERATURE					
Specification		−25		+85	°C
Operation		−40		+100	°C
Storage		−55		+125	°C

NOTE: (1) Specifications typical at T_A = +25°C, nominal input voltage, and rated output current unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	120% × rated voltage
Output Short-Circuit Duration	Momentary
Internal Power Dissipation	4W
Junction Temperature	+175°C
Package Thermal Resistance	27°C/W
Lead Temperature (soldering, 10 seconds)	+300°C

MECHANICAL



NOTES:

All dimensions are in inches (millimeters)

GRID: 0.100 inches (2.54 millimeters)

MATERIAL: Low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range and good electrical properties under high humidity environments. Lead material is brass with a hot-solder-dipped surface to allow ease of solderability.

BURR-BROWN®

PWR70

ISOLATED DC/DC CONVERTER
Low Cost—Unregulated Outputs
OUTPUT POWER TO 3 WATTS

FEATURES

- TESTED IN COMPLIANCE WITH UL544
- OUTPUT POWER TO 3 WATTS
- HIGH ISOLATION VOLTAGE 2000V_{PEAK}
- SIX-SIDED SHIELDING
- INPUT AND OUTPUT FILTERING
- LOW PROFILE PACKAGE 0.4" HIGH

APPLICATIONS

- SPOT REGULATOR
- POWER FOR DATA ACQUISITION, OP AMPS, ETC.
- PROCESS CONTROL
- PORTABLE EQUIPMENT
- TEST EQUIPMENT

DESCRIPTION

The PWR70 is a single-channel, dual-output DC/DC converter designed for general purpose power conversion applications where high efficiency is more important than load regulation.

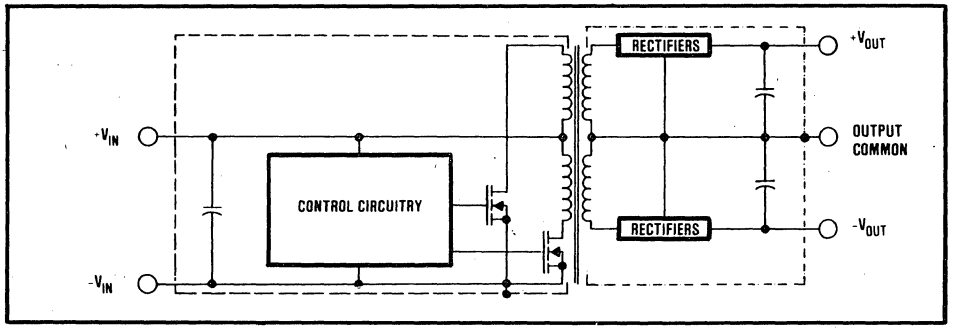
The PWR70 provides a plus and minus output voltage approximately equal to the input voltage magnitude. It operates over an input voltage range of 10VDC to 18VDC. Isolation voltage is a minimum of 2000 V_{PK}.

Six-sided shielding suppresses electromagnetic radiation which could disturb sensitive analog measurements or interfere with system timing signals. Input filtering minimizes reflected ripple current. Output ripple voltage and switching transients are reduced by filtering the PWR70 outputs.

Connecting an output pin to the output common will not damage the PWR70. Continuous short-circuit protection is accomplished by using power MOSFETs in the PWR70's input circuitry.

The PWR70 is tested in compliance with UL544 dielectric withstand voltage requirements for primary circuits.

SIMPLIFIED CIRCUIT DIAGRAM



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{IN}$ = 15VDC, and I_{OUT} = ±15mA unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Rated Voltage			15		VDC
Voltage Range		10		18	VDC
Input Current	I_{OUT} = ± 3mA		25		mA
	I_{OUT} = ±33mA			150	mA
Ripple Current	I_{OUT} = ± 3mA		±10		mA, pk
	I_{OUT} = ±33mA		±10		mA, pk
ISOLATION					
Rated Voltage	60sec, 60Hz, 5000V pk	2000			VDC
Resistance			10G		Ω
Capacitance			12		pF
Leakage Current	V_{ISO} = 240VAC, 60Hz			2	μA
OUTPUT					
Rated Voltage			±15		VDC
Voltage Accuracy				5	%
Rated Current			±15		mA
Current Range		0		±100	mA
Line Regulation	10VDC ≥ V_{IN} ≥ 18VDC		1.08		V/V
Load Regulation	±3mA ≥ I_{OUT} ≥ ±33mA		35		mV/mA
Ripple Voltage	I_{OUT} = ±3mA		±10		mV, pk
	I_{OUT} = ±33mA			±80	mV, pk
TEMPERATURE					
Specification		-25		+85	°C
Operating		-55		+125	°C
Storage		-65		+150	°C

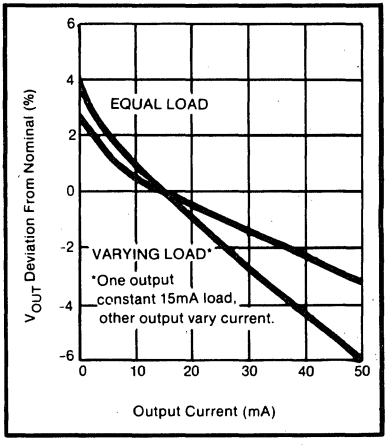


FIGURE 1. Load Regulation.

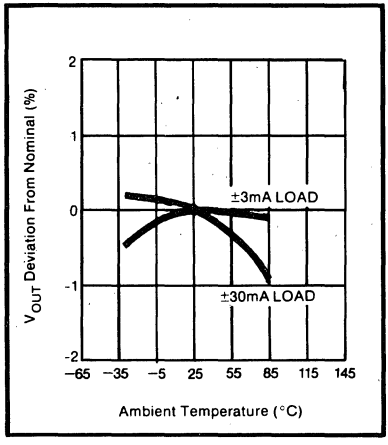
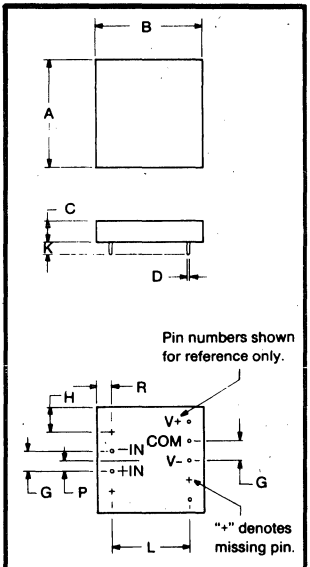


FIGURE 2. Temperature Drift.

ABSOLUTE MAXIMUM RATINGS

Input Voltage 18VDC
Output Current ..... ±150mA
Output Short-Circuit Duration ..... Continuous

MECHANICAL

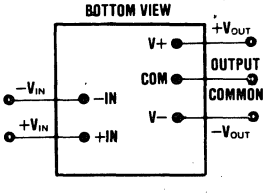


NOTE: Input and Output circuits have separate shields.

DIM.	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.075	1.175	27.31	29.85
B	1.075	1.175	27.31	29.85
C	.350	.420	8.89	10.67
D	.038	.042	0.97	1.07
G	.200 BASIC		5.08 BASIC	
H	.212	.312	5.38	7.92
K	.170	.350	4.32	8.89
L	.800 BASIC		20.32 BASIC	
P	.100 BASIC		2.54 BASIC	
R	.112	.212	2.84	5.38

Material: Black Epoxy
Weight: 15 gm. (0.53 oz.)
Grid: 2.50mm (0.10")

CONNECTION DIAGRAM



NOTE: Input and output circuits have separate shields. Input shield is connected to $-V_{IN}$. Output shield is connected to output common.

BURR-BROWN®

PWR71

ISOLATED DC/DC CONVERTER
Four Isolated Channels – Dual, Unregulated Outputs
3 WATTS RATED OUTPUT POWER

FEATURES

- TESTED IN COMPLIANCE WITH UL544
- OUTPUT POWER TO 3 WATTS
- HIGH ISOLATION VOLTAGE 1000V_{PEAK}
- SIX-SIDED SHIELDING
- INPUT AND OUTPUT FILTERING
- LOW PROFILE PACKAGE 0.4" HIGH

APPLICATIONS

- SPOT REGULATOR
- POWER FOR DATA ACQUISITION, OP AMPS, ETC.
- PROCESS CONTROL
- PORTABLE EQUIPMENT
- TEST EQUIPMENT

DESCRIPTION

The PWR71 is a four-channel, dual-output, unregulated DC/DC converter designed for general purpose power conversion applications where high efficiency is more important than load regulation.

The PWR71 has four isolated plus and minus output voltages approximately equal to the magnitude of the input voltage. It operates over an input voltage range of 10VDC to 18VDC. Rated output current for the PWR71 is 25mA per output or a total of 200mA for all outputs.

Isolation voltage between the input and any of the four output circuits is 1000V_{PK} continuous. This same isolation specification applies between any of the four dual outputs.

A continuous connection between an output and its common will not damage the PWR71. Short circuit protection is accomplished by using power MOSFETs in the PWR71 input circuitry.

Six-sided shielding suppresses electromagnetic radiation which could disturb sensitive analog measurements or interfere with system timing signals. Filtering the PWR71 input and outputs minimizes the effects of electrical noise on the source and loads of the converter.

Each PWR71 is tested in compliance with UL544, VDE750, and CSA C22.2 dielectric withstand specifications. In addition, barrier leakage current is 100% tested.

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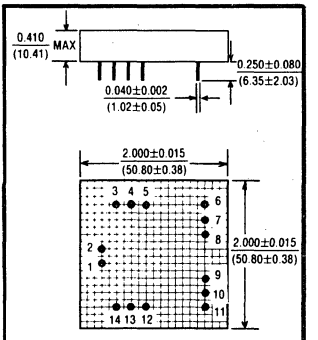
SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{IN}$ = 15VDC, and I_{OUT} = ±25mA unless otherwise noted.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
INPUT					
Rated Voltage			15		VDC
Voltage Range		10		18	VDC
Input Current	I_{LOAD} = 0		50		mA
	I_{LOAD} = Rated Load		280	375	mA
Ripple Current	I_{LOAD} = 0		30		mA, pk
	I_{LOAD} = Rated Load		80		mA, p-p
ISOLATION	Ratings apply input-to-output and channel-to-channel				
Rated Voltage	60 sec, 60 Hz, 3000 V_{PK}	1000			VDC
Resistance			10G		Ω
Capacitance			10		pF
Leakage Current	V_{ISO} = 240VAC, 60Hz			3	μA
OUTPUT					
Rated Voltage			±15		VDC
Voltage Range	I_{OUT} = No Load	±15		±18	VDC
	I_{OUT} = Rated Load	±14.25		±15.75	VDC
Rated Power		3			Watts
Rated Current	Each output	±25			mA
	Total of all outputs	200			mA
Current Range	Each output	0		±40	mA
	Total of all outputs	0		500	mA
Line Regulation	10VDC ≥ V_{IN} ≥ 18VDC		1.08		V/V
Load Regulation	0mA ≥ I_{LOAD} ≥ 25mA		35		mV/mA
Ripple Voltage	I_{LOAD} = 0		±10		mV, pk
	I_{LOAD} = Rated Load			±100	mV, pk
TEMPERATURE					
Specification		-25		+85	°C
Operating		-40		+100	°C
Storage		-55		+125	°C

MECHANICAL



NOTES:

All dimensions are in inches (millimeters).

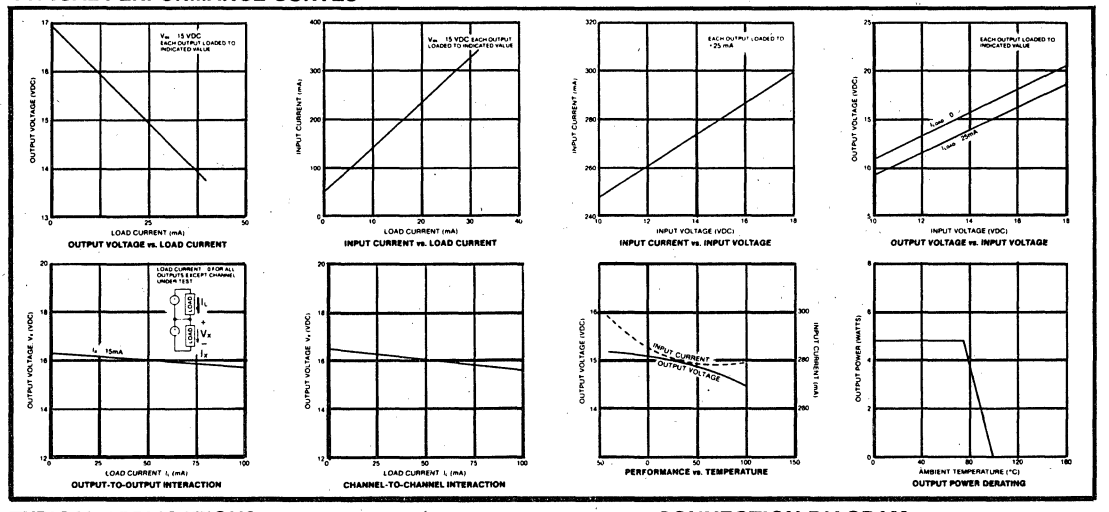
GRID: 0.100 inches (2.54 millimeters)

MATERIAL: Low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range and good electrical properties under high humidity environments. Lead material is brass with a hot solder dipped surface to allow ease of solderability.

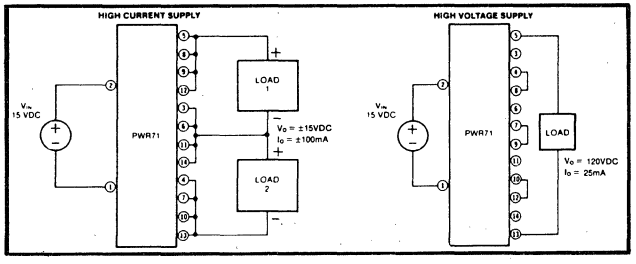
ABSOLUTE MAXIMUM RATINGS

Input Voltage	18VDC
Output Current	500 mA
Output Short-Circuit Duration	Continuous

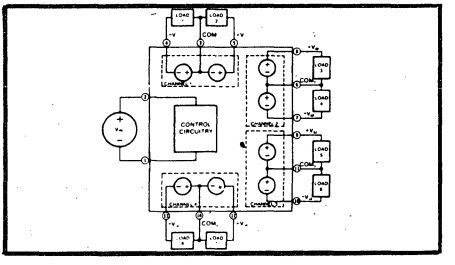
TYPICAL PERFORMANCE CURVES



TYPICAL APPLICATIONS



CONNECTION DIAGRAM



BURR-BROWN®

PWR72

Wide Input Voltage Range—5VDC to 22VDC UNREGULATED DC/DC CONVERTER

FEATURES

- Low Price
- High Power Output: 3W, minimum
- Wide Input Voltage Range: 5VDC to 22VDC
- Isolation Barrier 100% Tested per UL544, VDE750, and CSA C22.2 Dielectric Withstand
- Isolation Barrier Leakage Current 100% Tested at 240VAC: 3μA, maximum
- Low Isolation Barrier Capacitance: 10pF
- Single-Channel, Dual Output

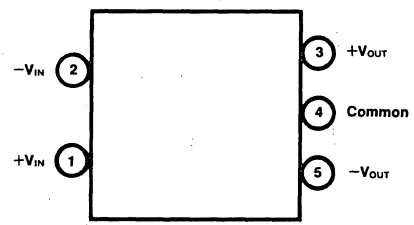
DESCRIPTION

The PWR72 is a 3W, single-channel, dual-output DC/DC converter designed for low cost spot power conversion and ground elimination applications.

It provides a plus and minus output voltage approximately equal to the input voltage magnitude. The PWR72 operates over a wide range of input voltages from 5VDC to 22VDC. Its unregulated outputs give the PWR72 high efficiency power conversion.

Surface-mounted devices and manufacturing processes are used in the PWR72 to give the user a device which is more environmentally rugged than most DC/DC converters. The use of surface-mounted technologies also gives the PWR72 superior isolation voltage. A third advantage of using surface-mounted technologies is low manufacturing cost.

CONNECTION DIAGRAM



[Bottom View]

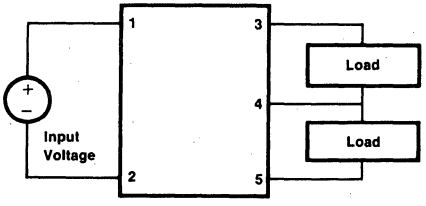
ORDERING INFORMATION

PWR 72 /G

Device Family
PWR indicates DC/DC converter
Model Number

Reliability Screening
No designator indicates standard manufacturing processing
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

TYPICAL APPLICATION



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SPECIFICATIONS

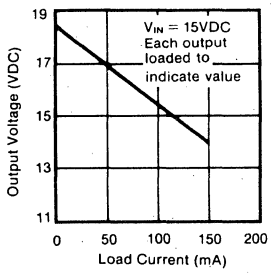
ELECTRICAL

At T_A = +25°C, $+V_{IN}$ = 15VDC, and I_{OUT} = ±100mA unless otherwise noted.

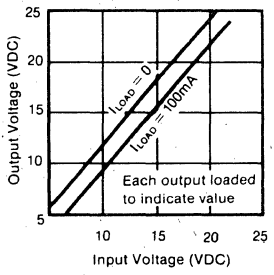
Parameter	Conditions	Min	Typ	Max	Units
INPUT					
Rated Voltage			15		VDC
Voltage Range		5		22	VDC
Input Current	I_{LOAD} = 0		40		mA
	I_{LOAD} = Rated Load		280	330	mA
Ripple Current	I_{LOAD} = 0		15		mA, pk
	I_{LOAD} = Rated Load		150		mA, p-p
ISOLATION					
Rated Voltage		1000			VDC
Test Voltage	60sec, 60Hz	3000			V_{PK}
Resistance			10		GΩ
Capacitance			10		pF
Leakage Current	V_{ISO} = 240VAC, 60Hz			3	μA
OUTPUT					
Rated Voltage			±15		VDC
Voltage Range	I_{OUT} = No Load	±15		±20	VDC
	I_{OUT} = Rated Load	±14.25		±15.75	VDC
Rated Power		3			W
Rated Current		100			mA
	Total of all outputs	200			mA
Current Range	Each output	0		±150	mA
	Total of all outputs	0		300	mA
Line Regulation	10VDC ≥ V_{IN} ≥ 18VDC		1.15		V/V
Load Regulation	0mA ≥ I_{LOAD} ≥ 100mA		15		mV/mA
Ripple Voltage	I_{LOAD} = 0		30		mV, pk
	I_{LOAD} = Rated Load			150	mV, pk
TEMPERATURE					
Specification		−25		+85	°C
Operation		−40		+100	°C
Storage		−55		+125	°C

TYPICAL PERFORMANCE CURVES

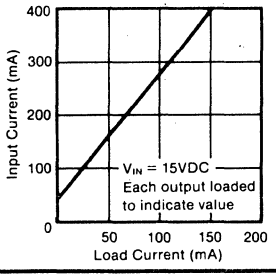
OUTPUT VOLTAGE VS LOAD CURRENT



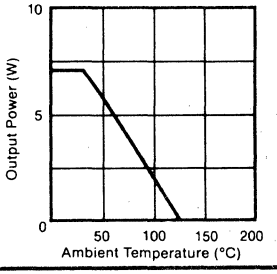
OUTPUT VOLTAGE VS INPUT VOLTAGE



INPUT CURRENT VS LOAD CURRENT



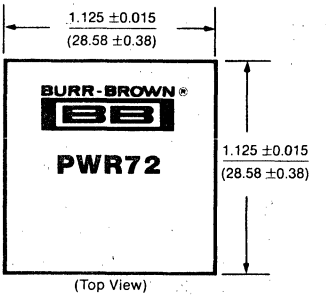
POWER DERATING

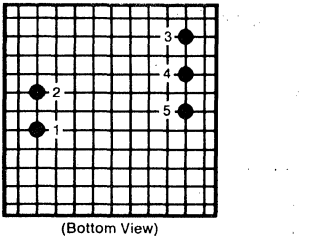


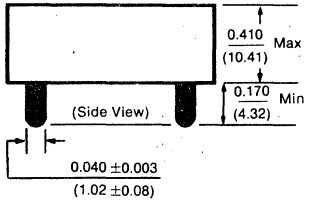
ABSOLUTE MAXIMUM RATINGS

Input Voltage	22VDC
Output Short-Circuit Duration	Momentary
Internal Power Dissipation	3W
Junction Temperature	+175°C
Package Thermal Resistance	13°C/W
Lead Temperature (soldering, 10 seconds)	+300°C

MECHANICAL







NOTES:

All dimensions are in inches (millimeters)

GRID: 0.100 inches (2.54 millimeters)

MATERIAL: Low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range and good electrical properties under high humidity environments. Lead material is brass with a hot-solder-dipped surface to allow ease of solderability.

BURR-BROWN®

PWR74

ISOLATED DC/DC CONVERTER
Two Isolated Channels - Dual, Unregulated Outputs
OUTPUT POWER TO 3 WATTS

FEATURES

- TESTED IN COMPLIANCE WITH UL544
- OUTPUT POWER TO 3 WATTS
- HIGH ISOLATION VOLTAGE 1500V_{PEAK}
- SIX-SIDED SHIELDING
- INPUT AND OUTPUT FILTERING
- LOW PROFILE PACKAGE 0.4" HIGH

APPLICATIONS

- SPOT REGULATOR
- POWER FOR DATA ACQUISITION, OP AMPS, ETC.
- PROCESS CONTROL
- PORTABLE EQUIPMENT
- TEST EQUIPMENT

DESCRIPTION

The PWR74 is a two-channel, dual-output DC/DC converter designed for general purpose power conversion applications where high efficiency is more important than load regulation.

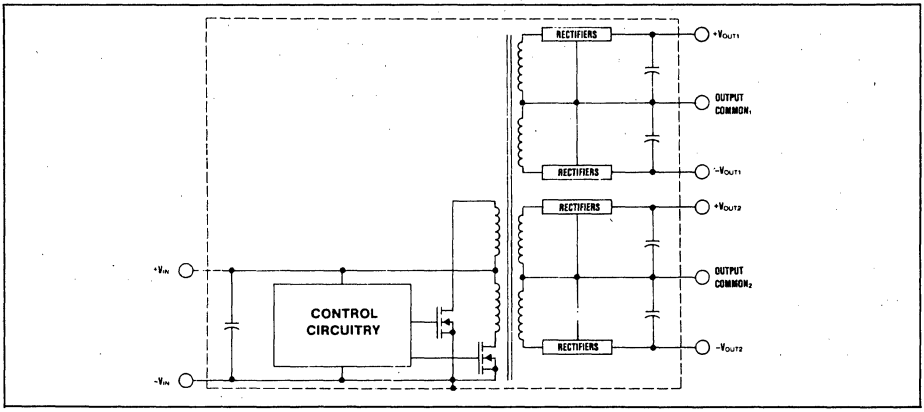
The PWR74 provides two isolated plus and minus output voltages approximately equal to the input voltage magnitude. It operates over an input voltage range of 10VDC to 20VDC. Isolation voltage is a minimum of 1500 V_{PK}.

Six-sided shielding suppresses electromagnetic radiation which could disturb sensitive analog measurements or interfere with system timing signals. Input filtering minimizes reflected ripple current. Output ripple voltage and switching transients are reduced by filtering the PWR74 outputs.

Momentarily connecting an output pin to its output common will not damage the PWR74. Short-circuit protection is accomplished by using power MOSFETs in the PWR74's input circuitry.

The PWR74 is tested in compliance with UL544 dielectric withstand voltage requirements for primary circuits.

SIMPLIFIED CIRCUIT DIAGRAM



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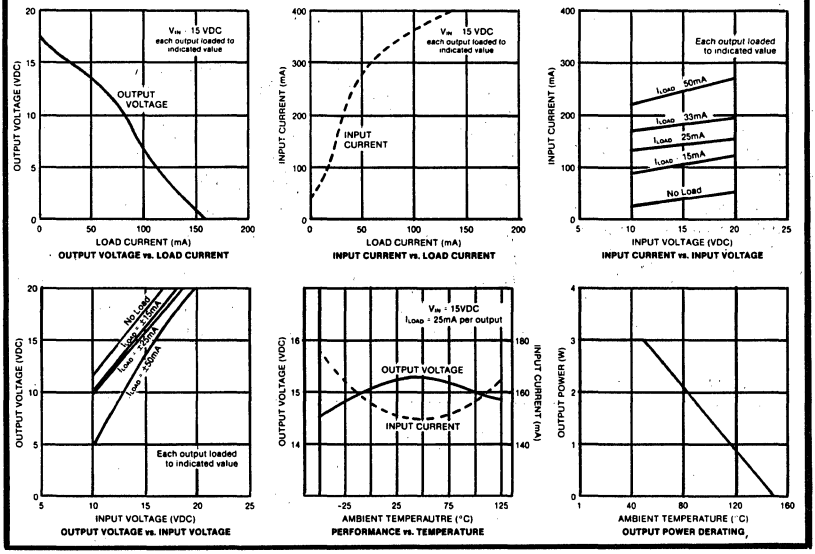
SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{IN}$ = 15VDC, and I_{OUT} = ±25mA unless otherwise noted.

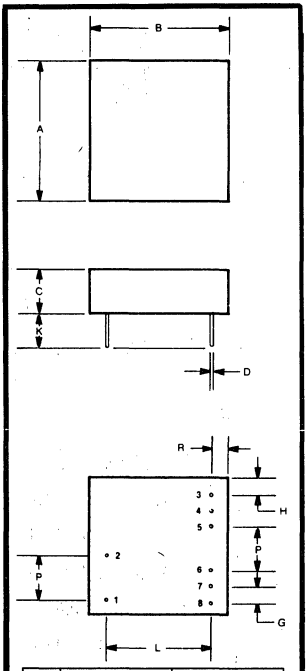
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Rated Voltage			15		VDC
Voltage Range		10		20	VDC
Input Current	I_{OUT} = No Load		55	75	mA
	I_{OUT} = Rated Load		155	175	mA
Ripple Current	I_{OUT} = No Load		80		mA, p.p
	I_{OUT} = Rated Load		100		mA, p.p
ISOLATION	Ratings apply input-to-output and channel-to-channel				
Rated Voltage	60 sec, 60 Hz, 4000 V_{PK}	1500			V_{PK}
Resistance			10G		Ω
Capacitance			12		pF
Leakage Current	V_{ISO} = 240VAC, 60Hz			2	μA
OUTPUT					
Rated Voltage	-25°C ≤ T_A ≤ +85°C		±15		VDC
Voltage Accuracy				5	%
Rated Current	-25°C ≤ T_A ≤ +85°C		±25		mA
Current Range		0		±50	mA
Line Regulation	10VDC ≥ V_{IN} ≥ 20VDC		1.15		V/V
Load Regulation	±5mA ≥ I_{OUT} ≥ ±25mA		18		mV/mA
Ripple Voltage	I_{OUT} = ≥ No Load		20		mV, p.p
	I_{OUT} = ≥ Rated Load		40	100	mV, p.p
TEMPERATURE					
Specification		-25		+85	°C
Operating		-55		+125	°C
Storage		-65		+150	°C



ABSOLUTE MAXIMUM RATINGS

Input Voltage 20VDC
Output Current ..... ±100mA
Output Short-Circuit Duration ..... 45 Seconds

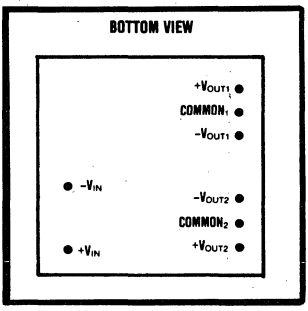
MECHANICAL



DIM.	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.075	1.175	27.31	29.85
B	1.075	1.175	27.31	29.85
C	.350	.420	8.89	10.67
D	.018	.022	0.46	0.56
G	.100 BASIC		2.54 BASIC	
H	.085	.175	2.16	4.45
K	.150	.350	3.81	8.89
L	.900 BASIC		22.86 BASIC	
P	.500 BASIC		12.7 BASIC	
R	.085	.175	2.16	4.45

Material: Black Epoxy
Weight: 15 gm. (0.53 oz.)
Grid: 2.50mm (0.10")

CONNECTION DIAGRAM



BURR-BROWN®

700/700U

ISOLATED DC-TO-DC CONVERTER

FEATURES

- HIGH BREAKDOWN VOLTAGE 5000V PEAK
- LOW LEAKAGE CAPACITANCE ≈ 3pF
- SHIELDED AND UNSHIELDED UNITS
- COMPLETELY SPECIFIED

APPLICATIONS

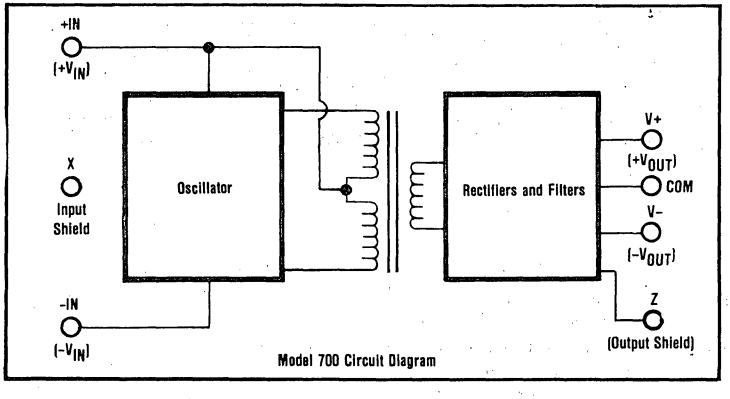
- INDUSTRIAL PROCESS CONTROL
- MEDICAL INSTRUMENTATION
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS

BENEFITS

- HIGH VOLTAGE RATING PROTECTS EXPENSIVE INSTRUMENTATION
- LOW LEAKAGE CURRENT PROTECTS HUMAN LIFE
- EXCELLENT ISOLATION CMR IMPROVES SYSTEM PERFORMANCE
- SHIELDING PREVENTS ELECTROSTACTIC AND EMI PROBLEMS

DESCRIPTION

The Model 700 converts a 10VDC to 18VDC input to a dual output of the same value as the input voltage. The internal hybrid integrated circuit reduces size and cost. A self-contained frequency stable 130kHz oscillator drives switching circuitry which is designed to minimize the common problem of spiking due to transformer saturation. Regulation and short circuit protection, if desired, can easily be added (see Figure 3). Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields.



Model 700 Circuit Diagram

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SPECIFICATIONS

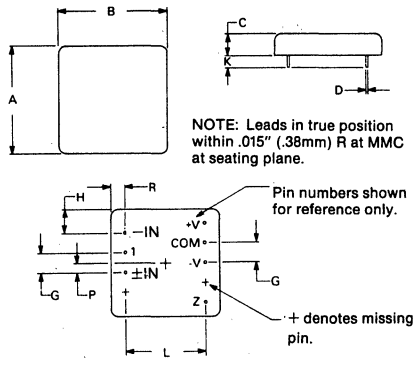
ELECTRICAL

Typical at 25°C with 15VDC supply unless otherwise noted.

MODEL	700/700M	700U/700UM
INPUT		
Voltage Range(1)	10V to 18V	
Current at ±3mA Load	20mA	
Current at ±30mA Load	±100mA, max	
Ripple Current at ±3mA Load	±3mA, peak	
Ripple Current at ±30mA Load	±100mA, peak	
ISOLATION(2)		
Voltage, Test, 5sec at 60Hz	4200V, p	5000V, p
Voltage, Continuous, derated	1500V, p	2000V, p
Impedance	10GΩ ‖ 5pF	10GΩ ‖ 3pF
Leakage Current at 240V/60Hz	1μA, max	1μA, max
OUTPUT		
V_{OUT} at ±3mA to ±30mA Load	$\pm V_{IN}$ with ±1V tolerance	
Operating Current total of both outputs	60mA, max	
Safe Nondestructive Current at 25°C	120mA, max	
Sensitivity to Input Voltage	1.08V/V	
Load Regulation	35mV/mA	
Ripple Voltage at ±3mA Load	±15mV, peak	
Ripple Voltage at ±30mA Load	±80mV, peak max	
Balance of +V and -V at +I = -I	±20mV	
TEMPERATURE RANGE		
Operating	-25°C to +85°C	
Storage	-55°C to +125°C	

NOTES:
1. Derate to 16V max between $+V_{IN}$ and $-V_{IN}$ above 70°C.
2. A medical grade unit is available which is 100% screened to Patient Connected Circuit requirements for the leakage current (par. 27.5) and dielectric withstand voltage (par. 31.11) of UL544. Specify 700M or 700UM.

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.075	1.135	27.31	28.83
B	1.075	1.135	27.31	28.83
C	.350	.410	8.89	10.41
D	.038	.042	0.97	1.07
G	.200 BASIC		5.08 BASIC	
H	.212	.312	5.38	7.92
K	.170	.350	4.32	8.89
L	.800 BASIC		20.32 BASIC	
P	.100 BASIC		2.54 BASIC	
R	.112	.212	2.84	5.38

Material: Black epoxy
Weight: 22.67gm (0.80oz)
Grid: 2.50mm (0.10")

NOTE: Input and Output circuits have separate shields.

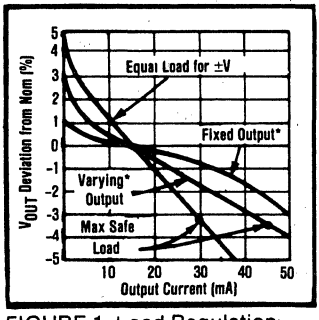


FIGURE 1. Load Regulation.

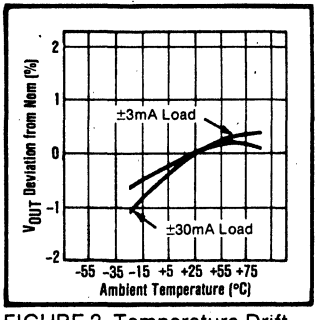


FIGURE 2. Temperature Drift.

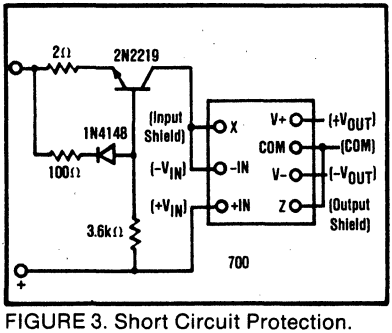


FIGURE 3. Short Circuit Protection.

*For one output with constant 15mA load and varying current on other output.
(A minimum load of 3mA is recommended for each output).

USE WITH ISOLATION AMPLIFIERS:

When the Model 700/700U is used with isolation amplifiers such as the Burr-Brown 3650 and 3652 special attention should be given to current ratings to avoid over designing. Since the isolation amplifiers do not draw maximum current simultaneously from the V+ and V− Model 700/700U terminals, it is possible to drive more isolation amplifiers per Model 700/700U than one might initially expect. The Model 700/700U is capable of providing a total output current of 60mA balanced or unbalanced between the two outputs. A minimum load of 3mA is recommended for each output.

BURR-BROWN®

710

QUAD-ISOLATED DC-TO-DC CONVERTER

FEATURES

- FOUR ISOLATED ±10VDC to ±18VDC OUTPUTS
- DRIVES FOUR 3650/3652 ISOLATION AMPS
- HIGH BREAKDOWN VOLTAGE, 2200VDC TEST
- LOW LEAKAGE CAPACITANCE, 8pF
- LOW LEAKAGE CURRENT, 1μA @ 240V/60Hz
- LOW COST PER ISOLATED CHANNEL

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The Model 710 converts a single 10VDC to 18VDC input into four dual-isolated outputs of the same value as the input voltage. The converter is capable of providing a total of 76mA at rated output voltage accuracy and can provide isolated power to four independently isolated 3650/3652 optically-coupled isolation amplifiers with the entire assembly mounted on one 5" x 7" card.

Extensive use is made of hybrid integrated circuits to reduce size and cost. A self-contained frequency stable 130kHz oscillator drives switching circuitry which is designed to minimize the common problem of spiking due to transformer saturation.

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DESCRIPTION

OUTPUT CURRENT RATINGS

The Model 710 is capable of providing a total of 76mA of output current divided among its eight outputs. The maximum current available from any one output is shown in Figure 9. A minimum average current of 3mA is recommended for each output in order to maintain output voltage accuracy. Thus, the current may be balanced (such as +9.5mA and -9.5mA) or unbalanced (such as +16mA and -3mA). The best output voltage accuracy will be obtained under balanced conditions.

Channels may be connected in series or parallel for higher voltage or current. For parallel operation connection of channel 1 to 2 or channel 3 to 4 will result in lowest ripple.

In some cases the 710 may drive larger loads than would be apparent from a cursory examination of the specifications. For example, see Figures 1 and 2. The most total current drawn from the pair of $+V_o$ and $-V_o$ output is $I_{max} + I_Q$ (not 2 x I_{max}). For the 3650 this is a maximum of 12mA +1.2mA = 13.2mA (instead of 24mA).

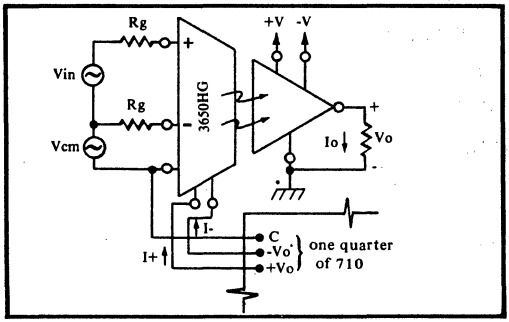


FIGURE 1. Typical Connection

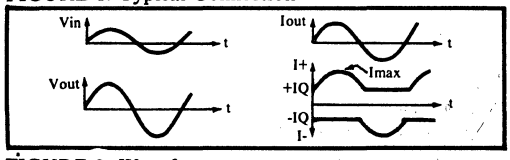


FIGURE 2. Waveforms

ISOLATION VOLTAGE RATINGS

It is important that the user understand the significance of the continuous derated isolation voltage specification and its relationship to the actual test voltage applied to the unit. Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (i.e., higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated minimum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.* Where the real voltages are well defined or where the isolation voltage is not continuous the user may choose to use a less conservative derating to establish a specification from the test voltage.

* Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS I-109 and ICS I-111.

SHORT CIRCUIT PROTECTION

The circuit in Figure 3 may be added to the input of the 710 in order to protect it from damage in situations where too much current is demanded from the outputs – such as a short circuit from an output to its common. The circuit limits the input current to approximately 100mA for an input voltage of 15VDC (for β of 2N2219 of 50).

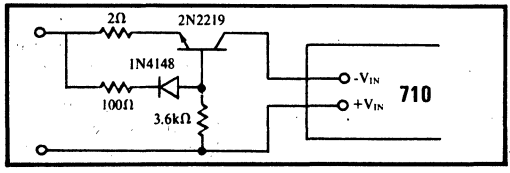


FIGURE 3. Short Circuit Protection

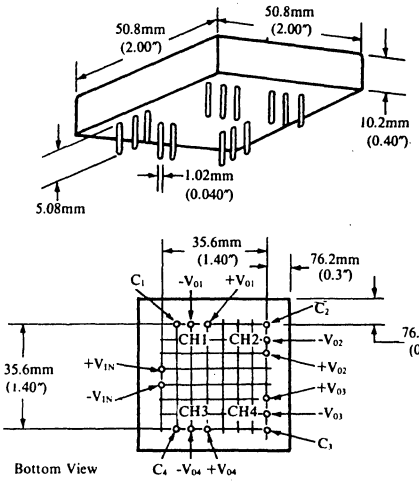
SPECIFICATIONS

Typical at 25°C with 15V supply unless otherwise noted.

ELECTRICAL

MODEL	710
INPUT	
Voltage Range[1][2]	10V to 18V
Current at Total Output Current of 24mA	40mA
Current at Total Output Current of 76mA	100mA, max.
Ripple at Total Output Current of 24mA	15mA, peak
Ripple at Total Output Current of 76mA	40mA, peak
ISOLATION[3]	
Voltage, Test, 5 sec.[4]	2200V, rms at 60Hz
Voltage, Continuous, derated, minimum[4]	600V, rms AC, 1000VDC
Impedance	10GΩ ‖ 8pF
Leakage Current at 240V/60 Hz	1μA, max
OUTPUT	
Voltage Accuracy[5]	See Figure 8
Current for Rated Accuracy: Total of all currents	76mA, max
: Any one output	60mA, max
Total Safe Nondestructive Current at 25°C	1200mA, max
Sensitivity to Input Voltage	1.08V/V
Load Regulation[6]	75mV/mA
Ripple Voltage at ±3mA Load	±25mV, peak
Ripple Voltage at ±9.5mA Load	±80mV, peak max
Balance of +V and -V at +I = -I	±20mV
ΔV_{out} vs Temperature -25°C to +85°C	3.0%
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +110°C

MECHANICAL



Material: Black Epoxy
Weight: 25 grams (0.9 oz.)
Grid: 5.08mm (.20")
Pin: Material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

NOTES:
1. Derate to 16V max between $+V_{IN}$ and $-V_{IN}$ above 70°C.
2. Operation down to 5V is possible with reduced output current and accuracy.
3. Isolation specifications are applicable to input to output isolation as well as channel to channel isolation.
4. See discussion on previous page; 2200V, rms = 3000V peak.
5. A minimum output current of ±3mA per channel is recommended to maintain output voltage accuracy.
6. Load regulation for one channel with other channels at ±9.5mA load.

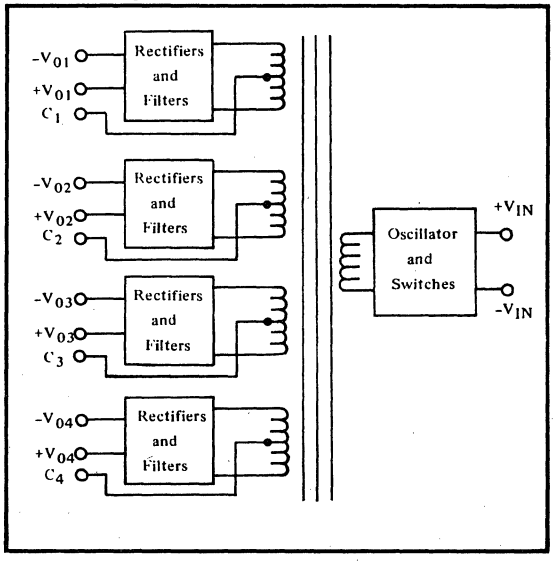


FIGURE 4. Functional Diagram

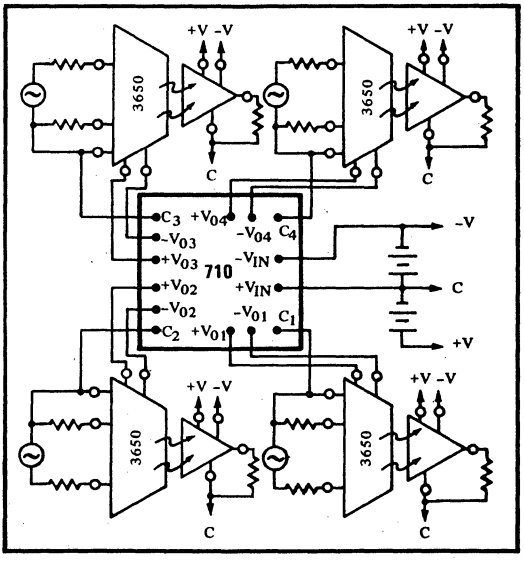


FIGURE 5. Typical Connection with Four 3650 Isolation Amplifiers.

TYPICAL PERFORMANCE CURVES

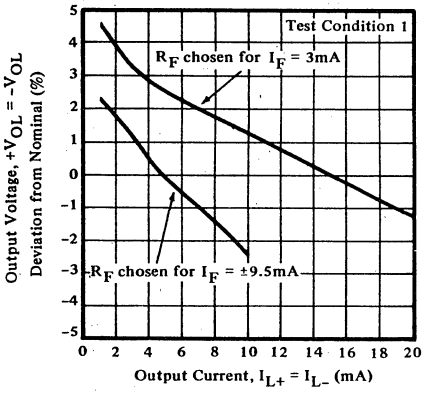


FIGURE 6. LOAD REGULATION - Balanced Load

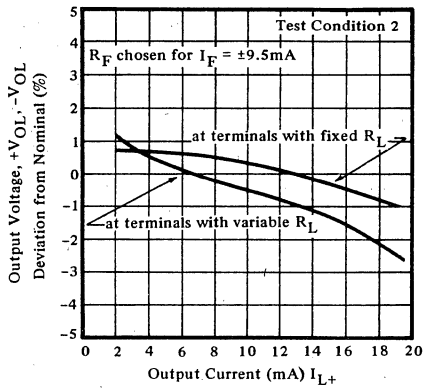


FIGURE 7. LOAD REGULATION - Unbalanced Load

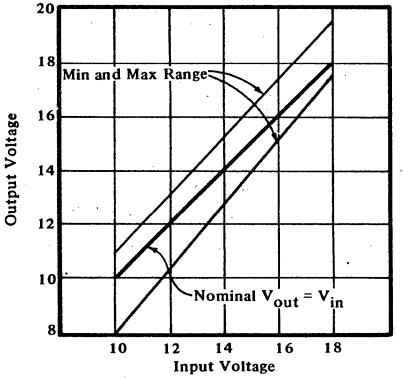


FIGURE 8. OUTPUT VOLTAGE ACCURACY VS INPUT VOLTAGE

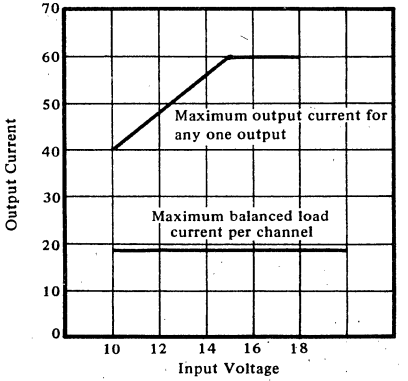


FIGURE 9. OUTPUT CURRENT RATINGS TO MAINTAIN OUTPUT VOLTAGE TOLERANCE

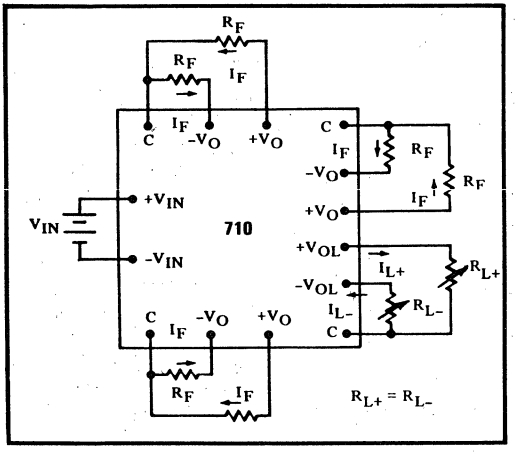


FIGURE 10. Test Condition 1: Balanced Load

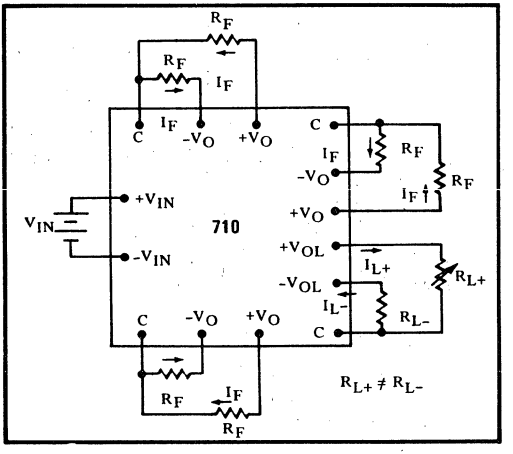


FIGURE 11. Test Condition 2: Unbalanced Load

BURR-BROWN®

722

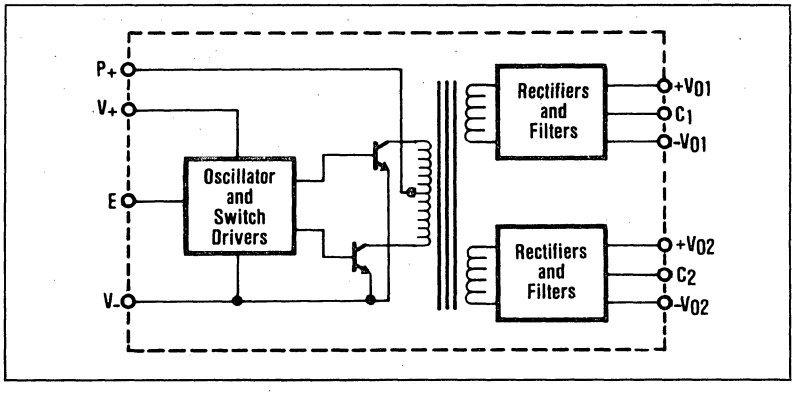
DUAL ISOLATED DC/DC CONVERTER

FEATURES

- DUAL ISOLATED ±5V TO ±16V OUTPUTS
- HIGH BREAKDOWN VOLTAGE, 8000V TEST
- LOW LEAKAGE CURRENT, <1μA AT 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE, 27.9mm x 27.9mm x 7.6mm (1.1" x 1.1" x 0.3")

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION



DESCRIPTION

The 722 converts a single 5VDC to 16VDC input into a pair of bipolar output voltages of the same value as the input voltage. The converter is capable of providing a total output current of 64mA at rated voltage accuracy and up to 250mA without damage.

The two output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage or in parallel for higher output current, as a single channel isolated DC/DC converter.

Integrated circuit construction of the 722 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 900kHz oscillator drives switching circuitry which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.

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DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 722 is capable of providing 64mA divided among its four outputs[1]. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Output channels[2] may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

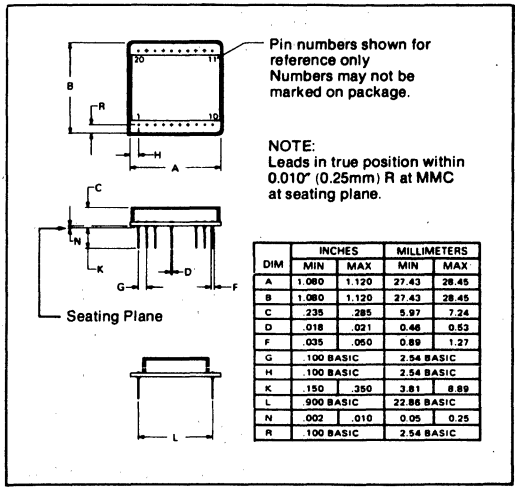
The fact that the two outputs of the 722 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows Burr-Brown's 3650 Optically Coupled Isolation Amplifier connected in three-port configuration. One of the 722 channels provides power to the 3650's input. The other channel supplies power to the 3650's output. The amplifier's input and output are isolated from each other and the system's power supply common. In this configuration the 722's channel-to-channel isolation specification applies to the amplifier input-to-output voltage.

Figure 3 illustrates how the 722 may provide isolated input power to the input stage of two 3650's connected in the two-port configuration. Power for the output stage is provided by the system +15V and -15V supplies. Input stages are isolated from each other and from the system supply. In this situation the 722's input-to-output isolation specification applies to the amplifiers' input-to-output voltages while the channel-to-channel 722 specification applies to the voltage existing between "I/P Com # 1" and "I/P Com # 2."

(1) "output" denotes a single output terminal (+V or -V) and its associated common
(2) "channel" denotes a pair of outputs (+V and -V) and their associated common

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.080	1.120	27.43	28.45
B	1.080	1.120	27.43	28.45
C	.235	.285	5.97	7.24
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.350	3.81	8.89
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.100 BASIC		2.54 BASIC	

SHORT CIRCUIT PROTECTION

The circuit in Figure 2 may be added to the input of the 722 to protect it from damage in situations where too much current is demanded from the outputs - such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for β of 2N2219 of 50).

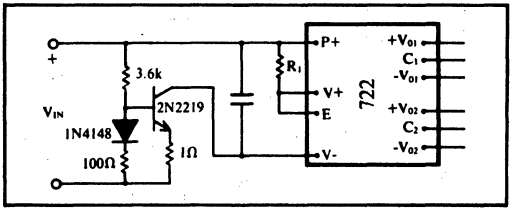


FIGURE 2. Short Circuit Protection

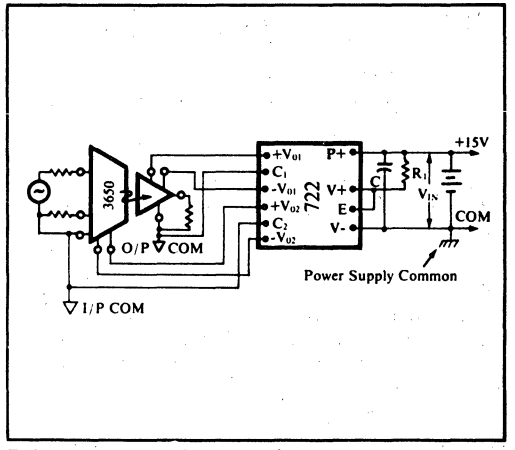


FIGURE 1. Three-Port Isolation

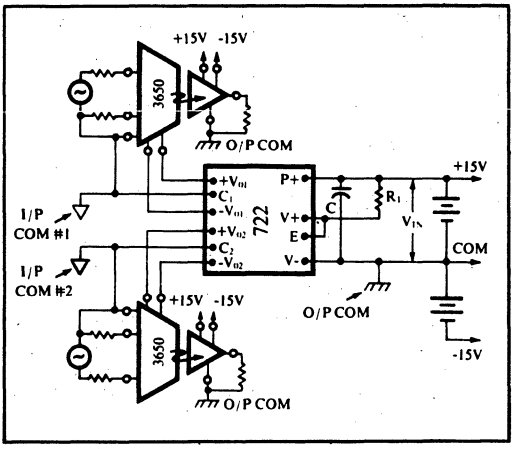


FIGURE 3. Two-Port Isolation with two 3650's.

ELECTRICAL SPECIFICATIONS

Specifications at T_A = +25°C, V_{IN} = 15VDC, C = 0.47μF, R_1 Selected per Typical Performance Curve.

PARAMETER	CONDITIONS	722			722BG			722MG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
Rated Input Voltage						&			•		VDC
Input Voltage Range(1)		5		16	•		•	•		•	VDC
Input Current	Total output current = 12mA		50			•			•		mA
	Total output current = 64mA		105	120		•	•		•	•	mA
	Total output current = 64mA at T_A = +85°C		120			•			•		mA
	Total output current = 160mA		225	275		•	•		•	•	mA
Input Ripple(2)	Total output current = 12mA		3			•			•		mA, pk
	Total output current = 64mA		6			•			•		mA, pk
	Total output current = 160mA		12			•			•		mA, pk
ISOLATION											
Test Voltages(3)	Input-to-output, 5 seconds, min			8000			•			•	V, pk
	Input-to-output, 1 minute, min			--			--			2500	V, rms
	Channel-to-channel, 5 seconds, min			5000			•			•	V, pk
Rated Voltage(3)	Input-to-output, continuous			3500			•			•	V
	Channel-to-channel, continuous			2000			•			•	V
Isolation Impedance	Input-to-output		10||6			•			•		GΩ||pF
Leakage Current(4)	Input-to-output, 240V, 60Hz			1			•			•	μA
OUTPUT											
Rated Output Voltage(5)	I_{Load} = 3mA per output	15.4		16.0	•		•	•		•	VDC
	I_{Load} = 16mA per output	14.3		15.3	•		•	•		•	VDC
	I_{Load} = 40mA per output	--	--	--	13.7	14.2	15.0	--	--	--	VDC
Output Current	Total of all outputs			200			•			•	mA
	Any one output(6)	3		100	•		•	•		•	mA
Load Regulation			Note 5			•			•		
Ripple Voltage	I_{Load} = 3mA per output		15			•			•		mV, pk
	I_{Load} = 16mA per output		35	100		•	•		•	•	mV, pk
	I_{Load} = 40mA per output		50			•			•		mV, pk
Tracking Error Between Dual Outputs	Balanced loads		±100			•			•		mVDC
Sensitivity to Input Voltage Changes			1.13			•			•		V/V
Output Voltage Temperature Coefficient	$T_A = T_{Specification\ Range}$		±0.02			•			•		%/°C
TEMPERATURE											
Specification	$I_{Load} \leq$ 16mA per output	-25		+85	•		•	•		•	°C
	$I_{Load} \leq$ 40mA per output	-25		+60	•		•	•		•	°C
Storage		-55		+125	•		•	•		•	°C
Junction Temperature				+125			•			•	°C

*Specifications same as 722.

NOTES:

1. For ambient temperature above 70°C the input voltage is 12.5V max. The input voltage remains 16V max if case temperature is kept below 85°C
2. External capacitor across "P+" to "V-" pins and 12" of #24 wire to V_{IN}
3. See "Isolation Voltage Ratings" on page 2 of data sheet
4. Reference UL544, paragraph 27.5, Leakage Current
5. See "Typical Performance Curves"
6. A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy

INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 722 are shown in Figures 1 and 3. Primary power (V_{IN}) is applied at the "P+" and "V-" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V-"; the only requirement is that "P+" and "V+" must be positive with respect to "V-."

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor R_1. The value of R_1 as a function of V_{IN} is shown in the TYPICAL PERFORMANCE CURVES section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5V to +7.5V positive with respect to "V-". If a separate source is used, the V+ input must be applied before the "P+" input to avoid possible damage to the unit. P+ and V+ must remain positive with respect to V- at all times (including transients). If necessary, diode clamps should be put across these inputs.

The "E" pin enables the converter when connected to "V+" and disables it when connected to "V-."

An external capacitor, "C", (0.47μF ceramic) is used to reduce input ripple. It should be connected as close to the "P+" and "V-" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 722 is not internally shielded, external shielding may be appropriate in applications where RFI at the 900kHz nominal oscillator frequency is a problem.

Each output is filtered with an internal 0.22μF capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10μF between each output and its common.

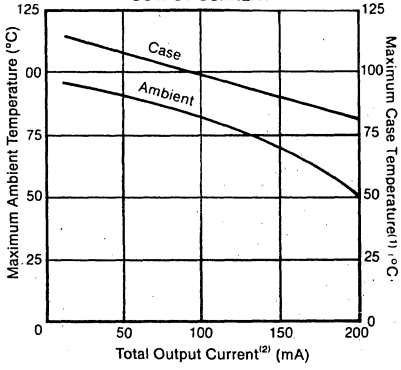
TYPICAL PERFORMANCE CURVES

Specifications at $T_A = +25°C$, $V_{IN} = 15VDC$, $C = 0.47\mu F$, R_1 selected per typical performance curve.

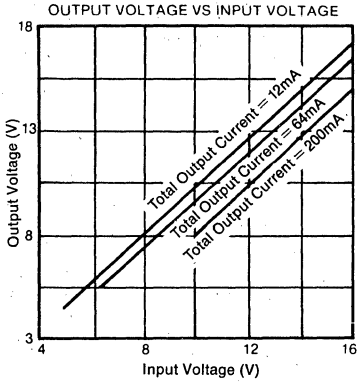
SELECTION OF R_1 OR EXTERNAL VOLTAGE V+ FOR MINIMUM INTERNAL POWER DISSIPATION

		Maximum Output Current From Any Single Output		
		<16mA	16mA to 30mA	30mA
Input Voltage (V)	>13	1.3kΩ	820Ω	510Ω
	11 to 13	820Ω	510Ω	200Ω
	9 to 11	510Ω	200Ω	0Ω
	8 to 9	200Ω	0Ω	-
	<8	0Ω	-	-
→ V+EXT		6.5V	7.5V	9.0V

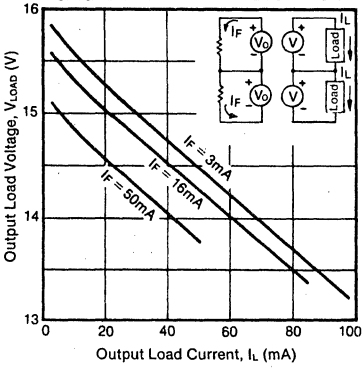
MAXIMUM SAFE OPERATING TEMPERATURE VS TOTAL OUTPUT CURRENT



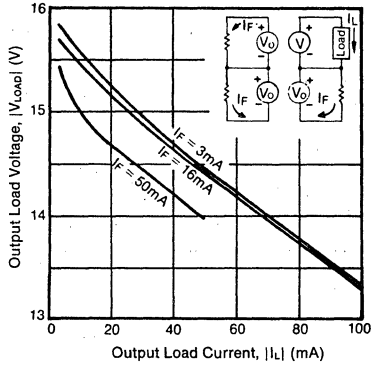
OUTPUT VOLTAGE VS INPUT VOLTAGE



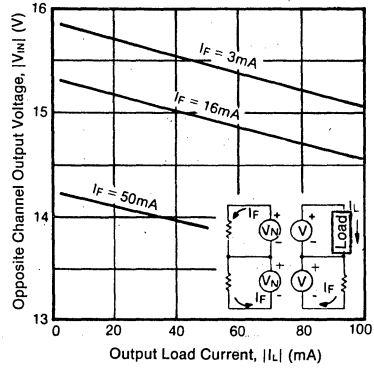
SINGLE-CHANNEL LOAD REGULATION



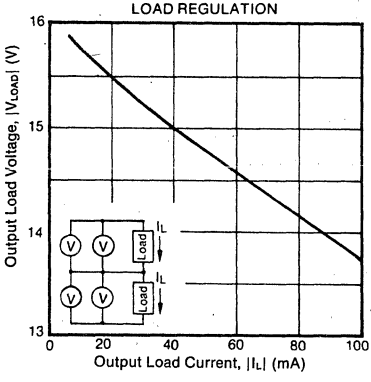
SINGLE OUTPUT LOAD REGULATION



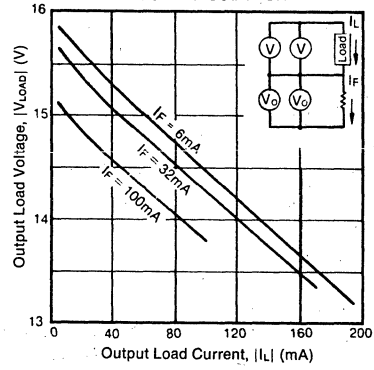
CHANNEL-TO-CHANNEL INTERACTION



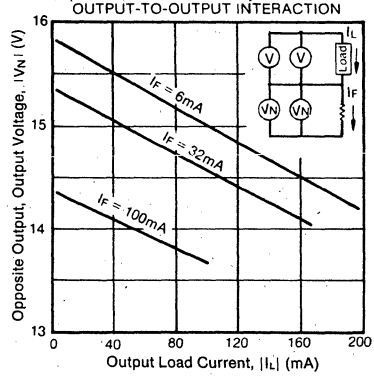
PARALLEL OUTPUT BALANCED LOAD REGULATION



PARALLEL OUTPUT UNBALANCED LOAD REGULATION



OUTPUT-TO-OUTPUT INTERACTION



NOTES: (1) Using a 104mm × 1.6mm aluminum strip mounted to the bottom of the case with heat sink compound.
(2) Total output current is the sum of the currents for each individual output.

BURR-BROWN®

724

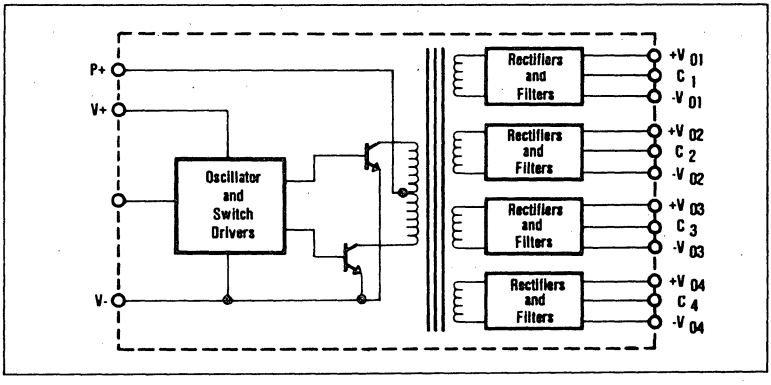
QUAD ISOLATED DC/DC CONVERTER

FEATURES

- QUAD ISOLATED ±8V OUTPUTS
- HIGH BREAKDOWN VOLTAGE, 3000V TEST
- LOW LEAKAGE CURRENT, <1μA AT 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE, 27.9mm x 27.9mm x 6.6mm (1.1" x 1.1" x 0.26")

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION



DESCRIPTION

The 724 converts a single 5VDC to 16VDC input into four pairs of bipolar output voltages of approximately half the input voltage. The converter is capable of providing a total output current of 128mA at rated voltage accuracy and up to 500mA without damage.

The four output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage, or in parallel for higher output current as a single channel isolated DC/DC converter.

Integrated circuit construction of the 724 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 800kHz oscillator drives switching circuitry which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

ELECTRICAL SPECIFICATIONS

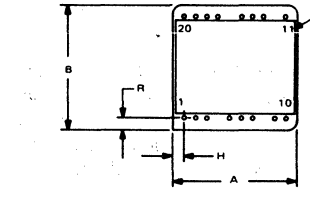
At 25°C with V_{IN} = 15V, R_1 = 1.3kΩ, C = 0.47μF unless noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Input Voltage		5	15	16	VDC
Input Current	Σ I_{OUT} = 24mA		50		mA
	Σ I_{OUT} = 128mA, 25°C		110	125	mA
	Σ I_{OUT} = 128mA, 85°C		120		mA
Input Ripple[1][5]	Σ I_{OUT} = 24mA, C = 0.47μF		10		mA, pk
	Σ I_{OUT} = 128mA, C = 0.47μF			25	mA, pk
ISOLATION					
Test Voltage[2]	Input-to-output, 5sec min			3000	VDC
	Channel-to-channel, 5sec min			3000	VDC
Rated Voltage[2]	Input-to-output, continuous			1000	VDC
	Channel-to-channel, continuous			1000	VDC
Isolation Impedance	Input-to-output		10 ‖ 6		GΩ ‖ pF
Leakage Current	Input-to-output, 240V/60Hz			1.0	μA
OUTPUT					
Voltage[3]	At 15V input I_L = 3mA	8.0	8.5	9.0	V
	I_L = 16mA	7.5	7.9	8.3	V
Current for Rated Voltage	Total of all outputs			128	mA
	Any one output[4]	3			mA
Total Safe Nondestructive Current	Total of all outputs			500	mA
	Any one output			200	mA
Load Regulation[3]			Note 4		
Ripple Voltage[5]	I_L = 3mA		35		mV, pk
	I_L = 16mA			200	mV, pk
Difference of $+V_0$ and $-V_0$	$+I_L$ = $-I_L$		±30		mV
Sensitivity to Input Voltage Change			0.63		V/V
Output Voltage Change Over Temperature	-25°C to +85°C		2		%
TEMPERATURE RANGE					
Operating		-25		+85	°C
Storage		-55		+125	°C

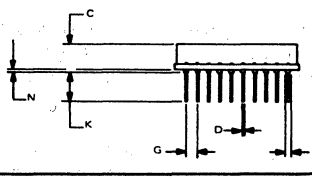
NOTES:
1. 0.47μF external capacitor across "P+" to "V-" pins and 12" of # 24 wire to V_{IN}.
2. See "Isolation Voltage Ratings" on preceding page. The input to output and channel to channel continuous AC rating is 700V, rms.
3. See "Typical Performance Curves."
4. A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy.
5. Test bandwidth 10MHz, max.

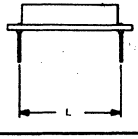
MECHANICAL

Pin numbers shown for reference only.
Numbers may not be marked on package.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.080	1.120	27.43	28.45
B	1.080	1.120	27.43	28.45
C	.235	.285	5.97	7.24
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.350	3.81	8.89
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.100 BASIC		2.54 BASIC	





NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

PIN POSITION	PIN DESIGNATION
1	$+V_{04}$
2	C_4
3	$-V_{04}$
4	No pin present
5	$+V_{03}$
6	C_3
7	$-V_{03}$
8	No pin present
9	$+V_{02}$
10	C_2
11	$-V_{02}$
12	No pin present
13	$+V_{01}$
14	C_1
15	$-V_{01}$
16	No pin present
17	P+
18	V-
19	V+
20	E

DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 724 is capable of providing 128mA divided among its eight outputs[1]. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Output channels[2] may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

The fact that the four outputs of the 724 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows two of Burr-Brown's 3650 Optically Coupled Isolation Amplifiers connected in three-port configuration. Two of the 724 channels provide power to the 3650's inputs. The other channels supply power to both 3650's outputs. Each amplifier's input and output are isolated from each other and the system's power supply common. Isolation specification applies to the amplifier input-to-output voltage isolation specification.

Figure 2 illustrates how the 724 may provide isolated input power to the input stage of four 3650's connected in the two-port configuration. Power for the four output stages is provided by the system +15VDC and -15VDC supplies. Input stages are isolated from each other and from the system supply. In this situation the 724's isolation specification applies to the amplifier's input-to-output voltage and to the voltage existing between any two I/P COM terminals.

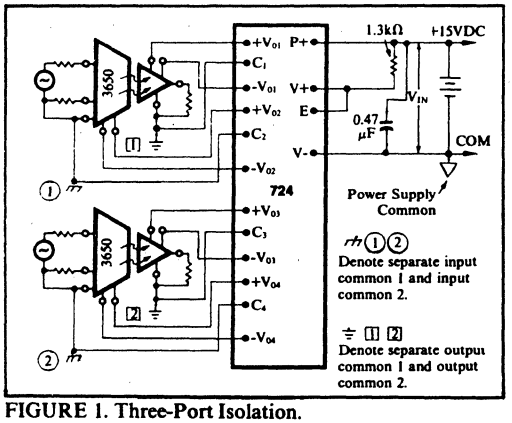


FIGURE 1. Three-Port Isolation.

ISOLATION VOLTAGE RATINGS

Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (i.e., higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated maximum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.[3] Where the real voltages are well defined or where the isolation voltage is not continuous the user may choose to use a less conservative derating to establish a specification from the test voltage.

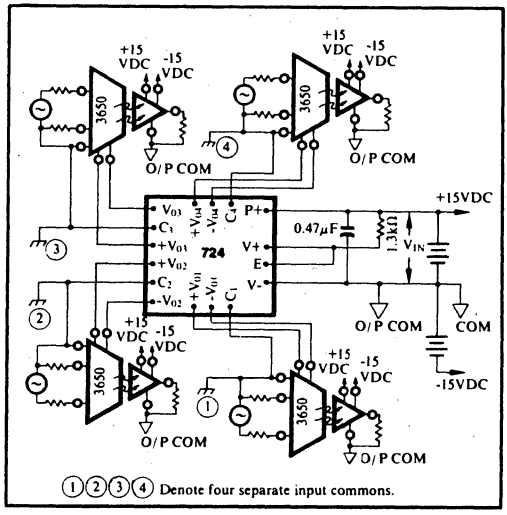


FIGURE 2. Two-Port Isolation with Four 3650's.

SHORT CIRCUIT PROTECTION

The circuit in Figure 3 may be added to the input of the 724 to protect it from damage in situations where too much current is demanded from the outputs - such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for β of 2N2219 of 50).

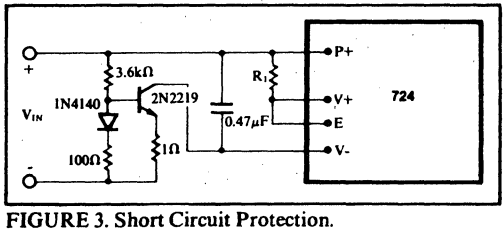


FIGURE 3. Short Circuit Protection.

(1) "output" denotes a single output terminal (+V or -V) and its associated common
(2) "channel" denotes a pair of outputs (+V and -V) and their associated common
(3) Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS 1-109 and ICS 1-111.

INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 724 are shown in Figures 1 and 2. Primary power (V_{IN}) is applied at the "P+" and "V-" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V-"; the only requirement is that "P+" and "V+" must be positive with respect to "V-."

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor R_1. The value of R_1 as a function of V_{IN} is shown in the "Typical Performance Curves" section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5VDC to +7.5VDC positive with respect to "V-." If a separate source is used, the V+ input must be applied before the "P+" input to avoid possible damage to the unit. P+ and V+ must remain positive with respect to V- at all times (including transients). If necessary, diode clamps should be put across these inputs.

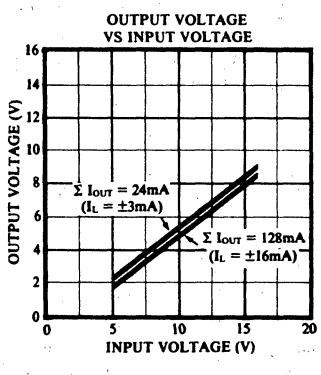
The "E" pin enables the converter when connected to "V+" and disables it when connected to "V-."

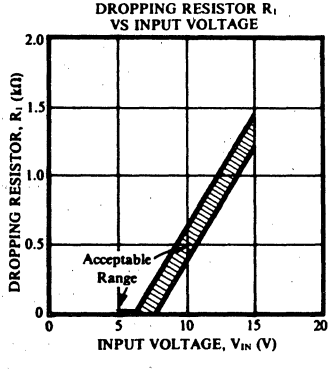
An external capacitor, "C", (0.47μF ceramic) is used to reduce input ripple. It should be connected as close to the "P+" and "V-" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 724 is not internally shielded, external shielding may be appropriate in applications where RFI at the 800kHz nominal oscillator frequency is a problem.

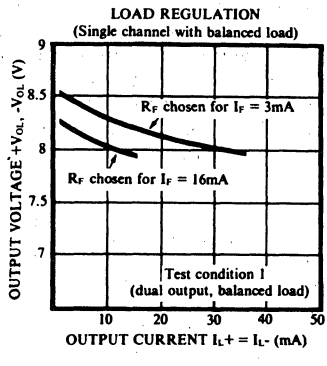
Each output is filtered with an internal 0.047μF capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10μF between each output and its common.

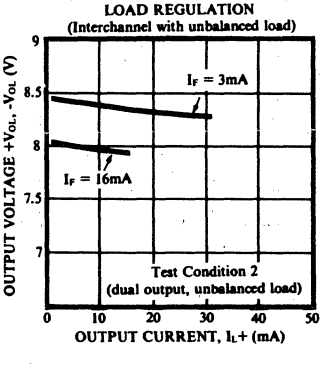
TYPICAL PERFORMANCE CURVES

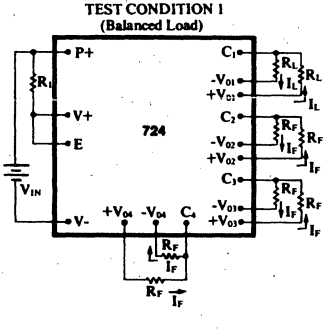
All specifications typical at 25°C unless otherwise noted.

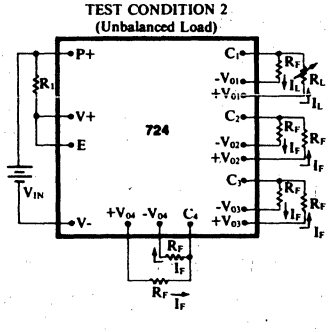










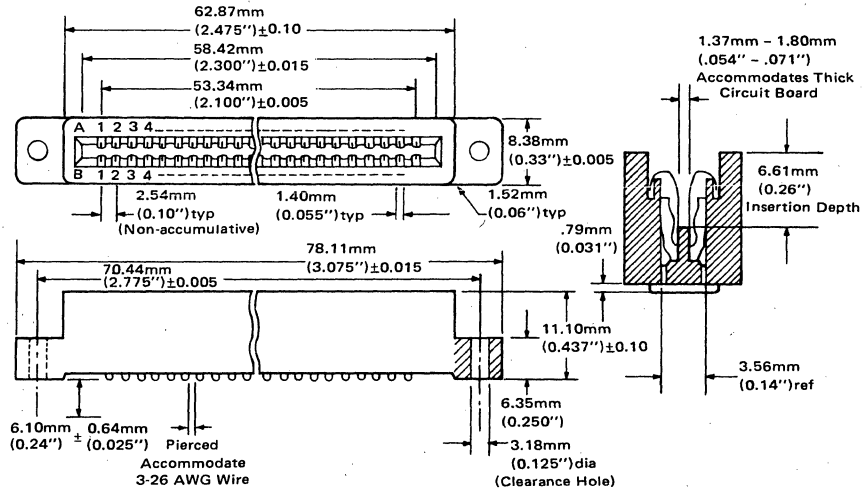


ACCESSORIES

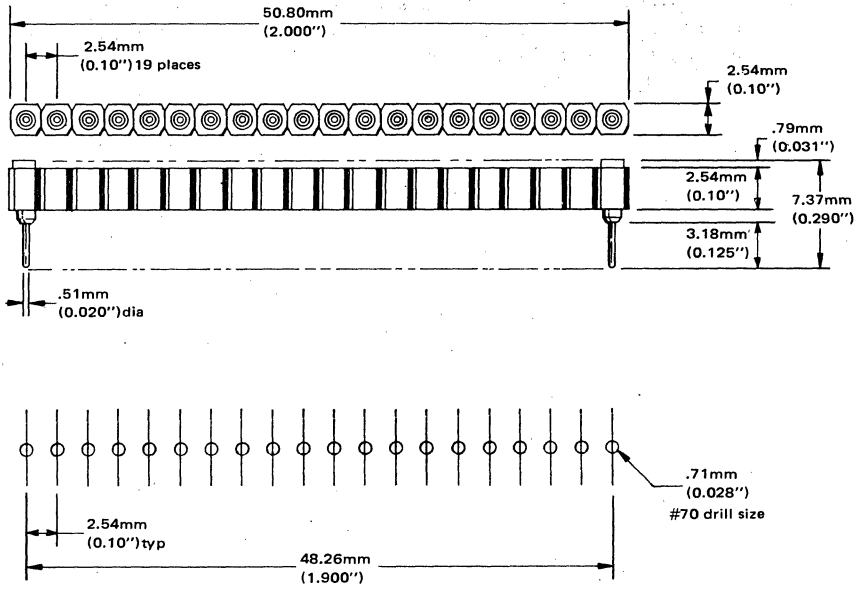
This section contains illustrations and information on the mating connectors and heat sinks available for use with various Burr-Brown products. The type of connector and/or heat sink required by the product is specified within the product data sheet. Prices are available from your nearest Burr-Brown representative.

MATING CONNECTORS

2201MC



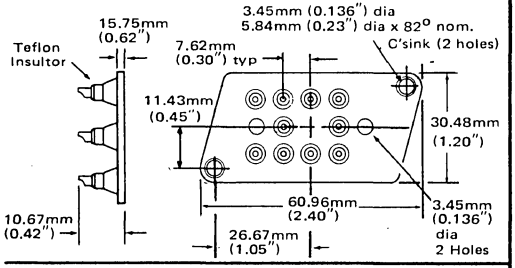
2350MC



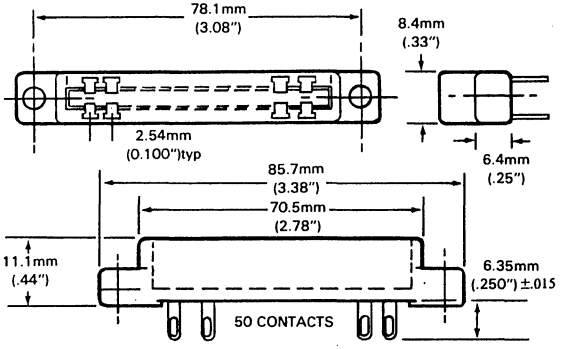
MATING CONNECTORS

1500MC

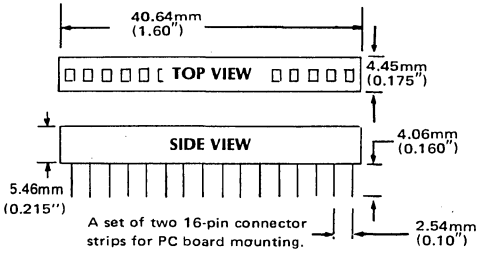
Material: Aluminum
Finish: Hard Black Anodize



2250MC



2302MC

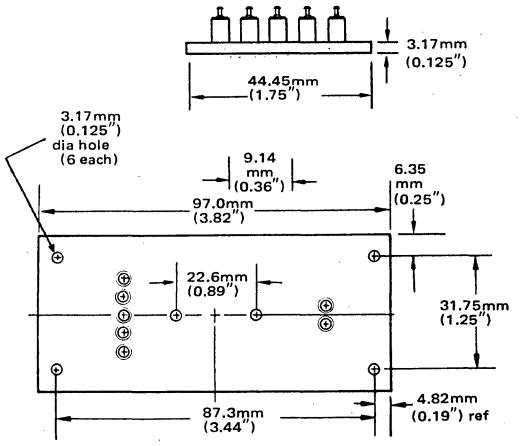


2401MC

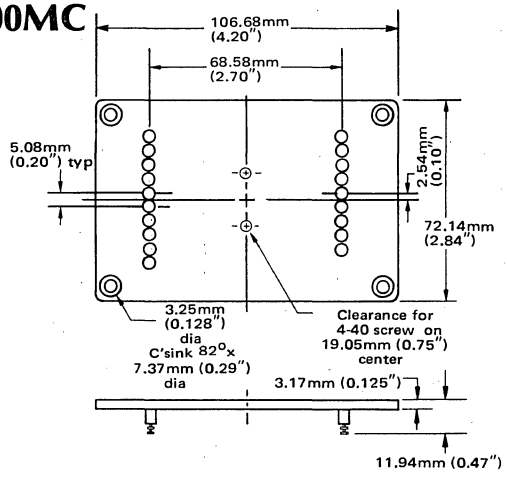
Identical to 2302MC except each connector strip length is 45.72mm (1.80")

A set of four 18-pin connector strips for PC board mounting.

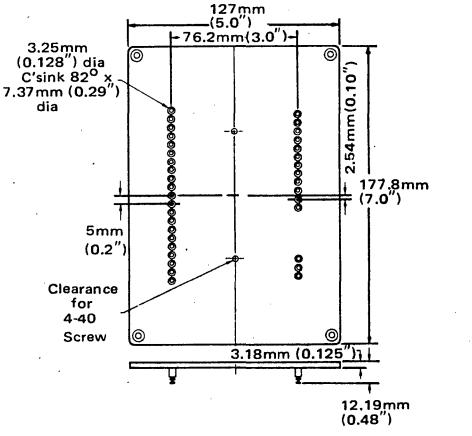
2800MC



4400MC

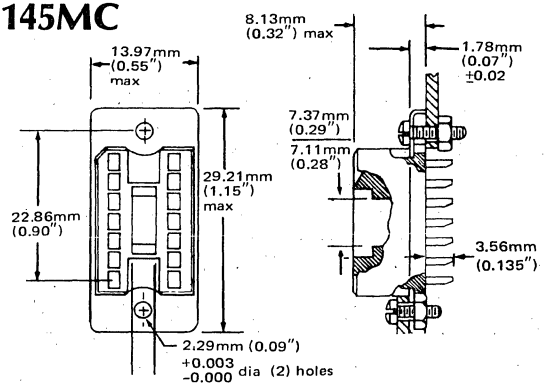


4800MC

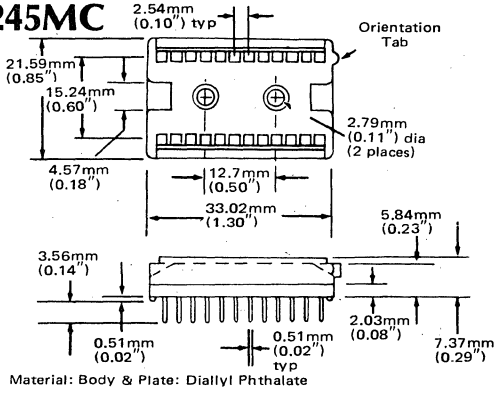


MATING CONNECTORS

145MC

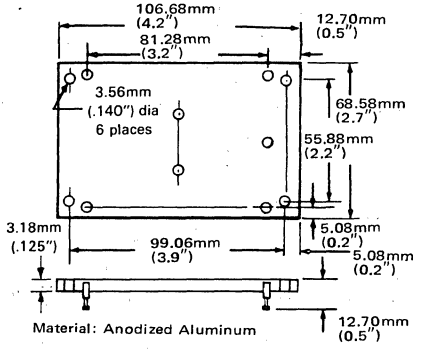


245MC



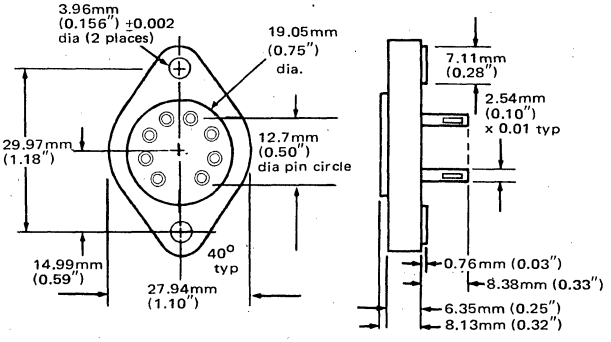
Material: Body & Plate: Diallyl Phthalate

548MC

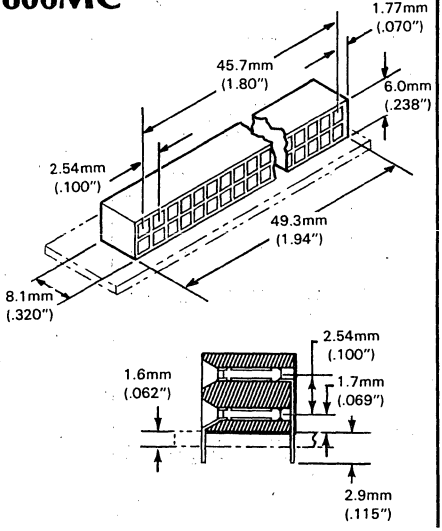


Material: Anodized Aluminum

803MC

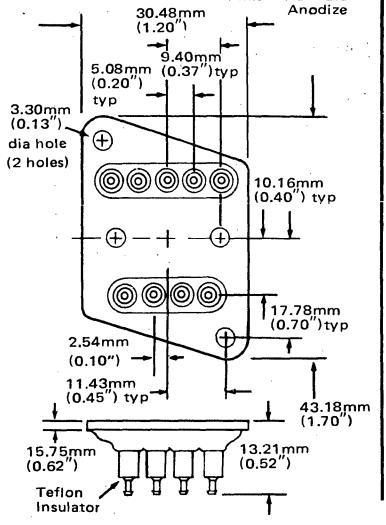


806MC

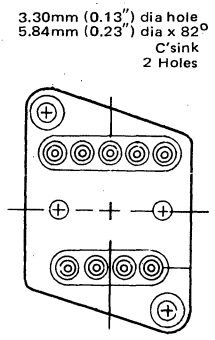


1200MC

Material: Aluminum
Finish: Hard Black Anodize



1400MC*

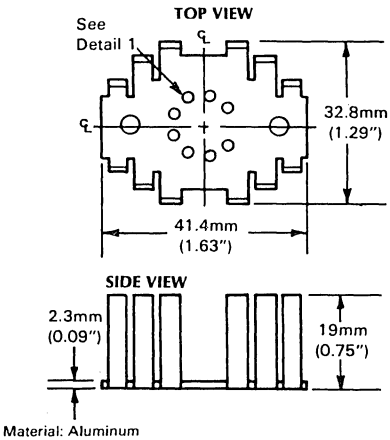


Material: Aluminum
Finish: Hard Black Anodize

* Identical to 1200MC except for mounting holes.

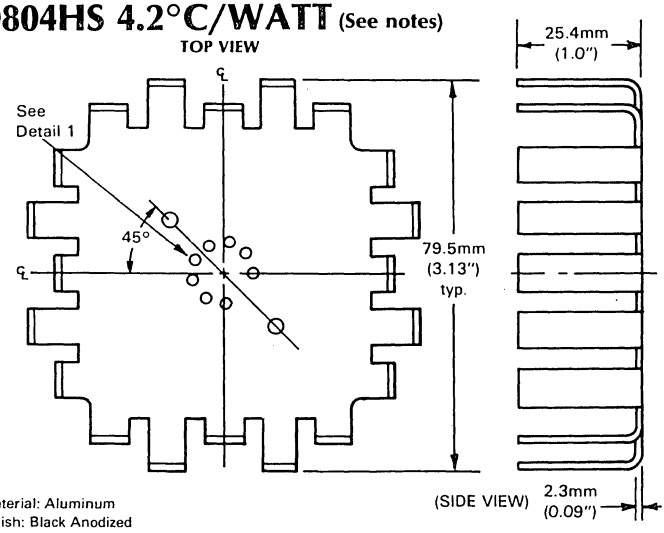
0803HS 12°C/WATT

(See notes)



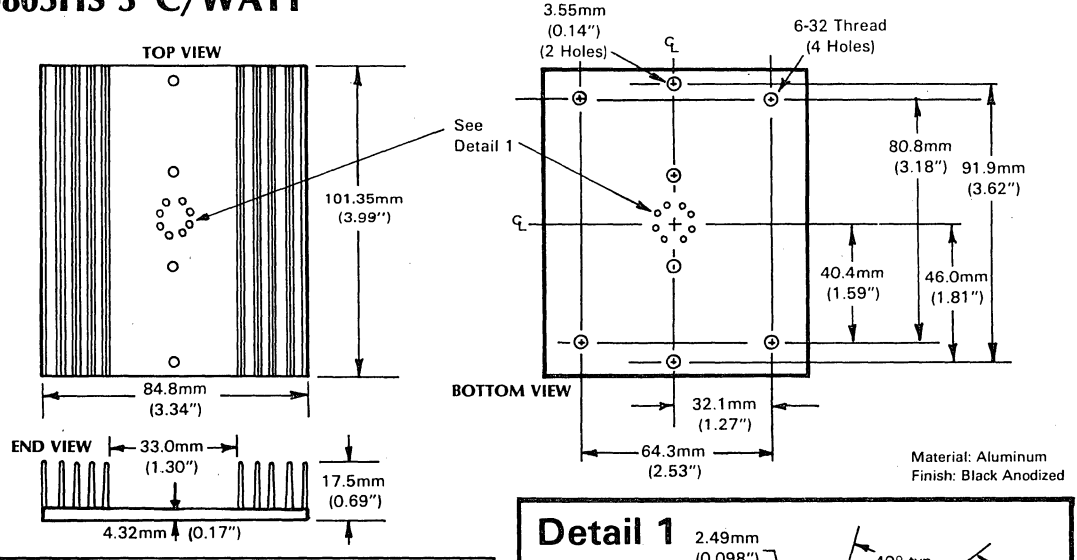
Material: Aluminum
Finish: Black Anodized

0804HS 4.2°C/WATT (See notes)



Material: Aluminum
Finish: Black Anodized

0805HS 3°C/WATT

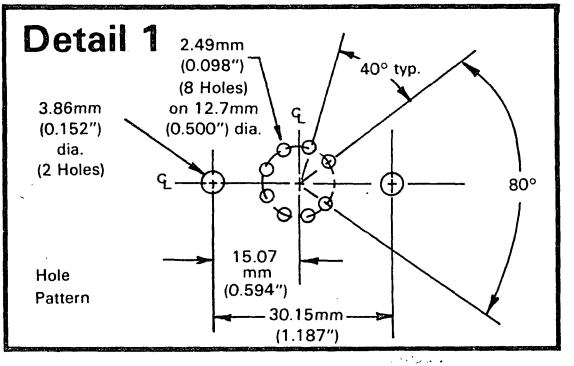


Material: Aluminum
Finish: Black Anodized

*NOTES

1. Thermal resistance specified are for natural connection. Heatsinks 0803HS and 0804HS are mounted on 6" x 6" x 1/16" G-10 PC board.
2. A thin-film of heatsink compound(Dow Corning 340 or equivalent) between the heatsink and the TO-3 device is recommended.

Detail 1



SYSTEM AND SUBSYSTEM PRODUCTS

MICROTERMINALS

Burr-Brown Microterminals are found wherever a cost-effective solution is needed for real-time data collection—inventory control, shop floor control, equipment reporting, time and attendance, or transaction recording. These display terminals insure the accurate collection of data from a variety of input sources including bar codes, magnetic stripe and keyboard input. Their small size and rugged construction make them an excellent choice for any harsh application typically requiring a CRT, printer or other fragile peripheral.

MICROTERMINALS

Model Number	Display Type(1) # of Characters	Display Buffer	Keyboard Type	# of Keys	Function Keys	Communications	Baud Rates	Protocol	Multidrop Capacity	TX Message Length	Nonvolatile Memory	Configuration	Digital I/O	Printer Port	Bar Code Input	Power	Maximum Current
TM25	LED 8 Num	8	Flat w/key domes	21 or 27	7	RS232 & Current Loop	300	Block	8	8	No	None	No	No	No	15VDC	250 mA
TM27	LED 8 Num	8	Flat w/key domes	21	6 prog.	RS232 or RS422	300 to 4800	Block	63	8	No	Jumper	3/5	No	No	8-12 VDC	300 mA
TM70	LED 12 U AN	36	Flat w/key domes	42	8 prog.	RS232 & Current Loop	300 & 1200	Character (echo)	15	36	No	Jumper	0/2	No	No	5VDC	600 mA
TM76	LED 12 U AN	36	Flat w/key domes	29	8 prog.	RS232 & Current Loop	300 & 1200	Character (echo)	15	36	No	Jumper	0/2	No	No	5VDC	600 mA
TM76 K	LED 12 U AN	36	Full travel	29	8 prog.	RS232 & Current Loop	300 & 1200	Character (echo)	15	36	No	Jumper	0/2	No	No	5VDC	600 mA
TM71	LED 16 U AN	80	Flat w/key domes	42	14 prog.	R232 & Cur. Loop or RS422	110 to 19,200	Block	15	80	User EPROM	Jumper or EPROM	0/2	No	No	5VDC	650 mA
TM77	LED 16 U AN	80	Flat w/key domes	30	14 prog.	RS232 & Cur. Loop or RS422	110 to 19,200	Block	15	80	User EPROM	Jumper or EPROM	0/2	No	No	5VDC	650 mA
TM77 K	LED 16 U AN	80	Full travel	30	14 prog.	RS232 & Cur. Loop or RS422	110 to 19,200	Block	15	80	User EPROM	Jumper or EPROM	0/2	No	No	5VDC	650 mA
TM71 -IO	LED 16 U AN	80	Flat w/key domes	42	14 prog.	RS232 & Cur. Loop or RS422	110 to 19,200	Block	15	80	User EPROM	Jumper or EPROM	8/10	No	No	5VDC	850 mA
TM77 -IO	LED 16 U AN	80	Flat w/key domes	30	14 prog.	RS232 & Cur. Loop or RS422	110 to 19,200	Block	15	80	User EPROM	Jumper or EPROM	8/10	No	No	5VDC	850 mA
TM77 K-IO	LED 16 U AN	80	Full travel	30	14 prog.	RS232 & Cur. Loop or RS422	110 to 19,200	Block	15	80	User EPROM	Jumper or EPROM	8/10	No	No	5VDC	850 mA
TM71 Q	LED 16 U AN	80	Flat w/key domes	42	14 prog.	RS232	110 to 9600	Block	15	80	No	Jumper	0/2	No	No	5VDC	2A
TM71 B	LED 16 U AN	80	Flat with key domes	42	16 prog.	RS232 or Current Loop or RS422	110 to 19,200	Block	63	80	No	Jumper	8/10	No	Yes	5VDC, 18-28 VAC/ DC	1.5A
TM77 B	LED 16 U AN	80	Flat with key domes	30	16 prog.	RS232 or Current Loop or RS422	110 to 19,200	Block	63	80	No	Jumper	8/10	No	Yes	5VDC, 18-28 VAC/ DC	1.5A
TM71 MS	LED 16 U AN	80	Flat w/key domes	42	16 prog.	RS232 or Cur. Loop or RS422	110 to 19,200	Block	63	80	No	Jumper	8/10	No	No	5VDC, 18-28 VAC/DC	1.5A
TM77 MS	LED 16 U AN	80	Flat w/key domes	30	16 prog.	RS232 or Cur. Loop or RS422	110 to 19,200	Block	63	80	No	Jumper	8/10	No	No	5VDC, 18-28 VAC/DC	1.5A
TM 200	VF 40 UL AN	80	Full travel	27	16 prog.	RS232 & Cur. Loop & RS422	110 to 19,200	Block	63	80	User EPROM	Jumper or EPROM	0/10	Yes	Yes (scan. opt.)	5VDC	1.5A
TM 8400 (2)	Backlit LCD 2X40 UL AN	1920	Elastomer	51	16 prog.	RS232 or Cur. Loop or RS422 (isol/non)	300 to 19,200	Char., Block, Monitor	32	80	Battery RAM	Interactive	Opt. with mod.	Opt. with mod.	Opt. with mod.	5VDC, 7.5-9 VDC	500 mA

NOTE: (1) Num = Numeric, AN = alpha-numeric, U = upper-case characters, UL = upper and lower case characters. (2) **TM8400 also features user-definable keyboard layout and auxiliary serial port (with optional module).**

MICROCOMPUTER I/O SYSTEMS

This full line of μC compatible I/O boards is available off-the-shelf. Design features let you put your microcomputer-based system together fast, using these analog and digital I/O's that offer: simple software requirements; memory-mapped designs; up to 64 input channels per board; analog inputs and outputs on the same board; 8- or 12-bit resolutions; software programmable gains; relay outputs; isolated digital I/O. Plug compatible with Intel, DEC, National, Motorola, Rockwell, Synertek, and others.

MULTIBUS™ ANALOG I/O								
			Inputs		Analog	Number Channels		
Model	Analog Input	Analog Output	High Level	Low Level	Resolution (Bits)	Input	Output	Features
MP8305		●	●		12		4	Individual D/A converters
MP8316-V		●	●		12		16	Low cost per channel
MP8316-I		●			12		16	0 to 25mA inputs
MP8418	●		●	●	12	15 DIF/31 SE		Resistor programmable gain
MP8418-AO	●	●	●	●	12	15 DIF/31 SE	2	Resistor programmable gain
MP8418-PGA	●		●	●	12	15 DIF/31 SE		Software programmable gain
MP8418-PGA-AO	●	●	●	●	12	15 DIF/31 SE	2	Software programmable gain
MP8418-EXP	(1)		(1)	(1)	(1)	48 DIF/96 SE		Analog input expander
MP8430	●		●	●	12	16 DIF		RTD excitation
MP8450	●		●	●	12	16 DIF		900V transformer isolated
MP8616	●		●	●	8	16 SE		Low cost

NOTES: (1) Must be used with MP8418, MP8418-AO, MP8418-PGA or MP8418-PGA-AO which govern MP8418-EXP performance.

MULTIBUS™ DISCRETE I/O					
Model	Digital Input	Digital Output	Number Channels	Isolated	Features
MP801		●	16	●	Relay output
MP802		●	32	●	Relay output
MP810	●		24	●	Contact closure input
MP810-NS	●		24	●	Voltage input
MP810-LV	●		24	●	Low voltage inputs
MP810-AC	●		24	●	AC sense inputs
MP810-DB	●		24	●	Debounce circuit
MP821-05	●		5	●	Time measurement
MP821-15	●		15	●	Time measurement
MP830-72	●	●	72		Output read back
MP830-72R	●	●	72		Input terminators
MP840	●		24	●	Sequence of events detection

MULTIBUS™ BOARD		
Model	Function	Description
MP85188	CPU	Single-board computer with 80188-3, 16 JEDEC memory sockets, 8k RAM supplied, dual RS-232C ports, 24 parallel TTL I/O, 3 counters, watchdog timer, user-definable features.

Multibus™ Intel Corp.

MOTOROLA MICROMODULES ANALOG I/O								
			Inputs		Analog	Number Channels		
Model	Analog Input	Analog Output	High Level	Low Level	Resolution (Bits)	Input	Output	Features
MP7105		●			12		4	General purpose
MP7209	●		●	●	12	8 DIF		General purpose
MP7217	●		●	●	12	16 SE		General purpose
MP7218	●		●	●	12	16 SE		Low cost
MP7432	●		●	●	8	32 DIF/64 SE		Low cost
MP7432-AO	●	●	●	●	8	32 DIF/64 SE	2	Low cost
MP7504		●			8		4	Isolated-fused outputs
MP7608-I	●		●		12	8 DIF		Fused inputs

MOTOROLA MICROMODULES DIGITAL I/O					
Model	Digital Input	Digital Output	Number Channels	Isolated	Features
MP702		●	32	●	Reed relays
MP710	●		24	●	Dry contact closures
MP710-NS	●		24	●	Wet contact closures

DEC Q-BUS ANALOG I/O								
			Inputs		Analog	Number Channels		
Model	Analog Input	Analog Output	High Level	Low Level	Resolution (Bits)	Input	Output	Features
MP1104		•			12		4	Individual D/A converters
MP1216	•		•	•	12	32 SE/16DIF		Resistor programmable gain
MP1216-PGA	•		•	•	12	32 SE/16DIF		Software programmable gain

VMEbus ANALOG I/O						
		Input Channels			Output Channels	
Model	Analog Resolution (Bits)	Number	Range	Gain	Number	Range
MPV901	12	32SE/16DIF	(1)	1-1000 (R)		
MPV901A	12	32SE/16DIF	(1)	1-1000 (R)	2	(1)
MPV901P	12	32SE/16DIF	(1)	1-1000 (S)	2	(1)
MPV904	12				16	(1)
MPV905	12				8	(3)
MPV950S	12	16SE	(2)			
MPV950D	12	8SE, 8SE/8DIF	(2)	1-10 (R)		
MPV952	12	8SE	(2)			

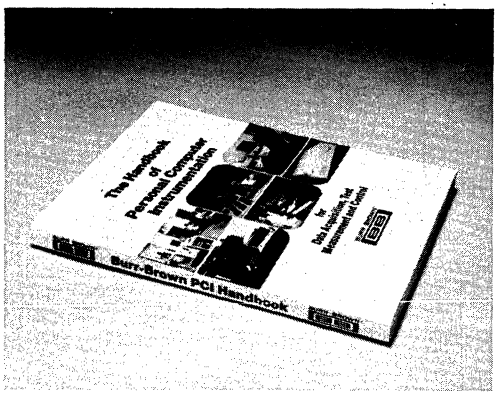
NOTES: (1) 0 to +5V, 0 to +10V, ±2.5V, ±5V, ±10V. (2) 0 to ±10V. ±5V, ±10V. (3) 0 to 20mA, 4 to 20mA, 5 to 25mA. (R) Resistor selectable. (S) Software programmable.

VMEbus DISCRETE I/O					
Model	Digital Input	Digital Output	Number Channels	Isolated	Comments
MPV902		•	32	•	Relay output
MPV910	•		32	•	Contact closure input
MPV910-NS	•		32	•	Voltage input
MPV910-LV	•		32	•	Low voltage input
MPV930-48	•	•	48		TTL, output readback

VMEbus DIGITAL SIGNAL PROCESSING BOARDS		
Model	Function	Description
SPV100	General purpose DSP	DSP board based on TMS320 processor board incorporates two 4k × 16-bit swinging buffer data memories and two program memories (4k × 16-bit PROM and a 4k × 16-bit RAM).
MPV960	DSP with analog input	Four optically isolated high level input channels with simultaneous sampling, 12-bit resolution, fast (12μs) throughput, and flexible triggering modes. On-board high speed TMS320 DSP processor. Two 4K × 16K bit swinging buffer data memories. Includes monitor and signal processing firmware.
ACX960	Software development	Daughter board plugs into the MPV960, providing custom software development environment for TMS320.
VMEbus ACCESSORY BOARD		
MPV990	Anti-aliasing (low-pass) filter	Four independent filter channels with selectable input amplification (0.1-10,000) and cutoff frequencies (2-20kHz). User-configurable output amplification.
DSP SPV100 FIRMWARE		
FIL100	Filtering	Digital filtering (FIR) package.
COR100	Correlation	Cross- and auto-correlation package.
FFT100-1	FFT	64-point fast Fourier transform.
FFT100-3	FFT	256-point fast Fourier transform.
FFT100-4	FFT	512-point fast Fourier transform.
FFT100-5	FFT	1024-point fast Fourier transform.
VMEbus REAL-TIME SOFTWARE DRIVERS[1]		
PSOA	pSOS-68k™	Drivers for MPV901, MPV904, MPV905, MPV950 and MPV952. Includes source code.
PSOB	pSOS-68k™	Drivers for SPV100 and MPV960. Includes source code.
VERA	VERSAdos™	Drivers for MPV901, MPV904, MPV905, MPV950 and MPV952.
VERB	VERSAdos™	Drivers for MPV960 and SPV100.
PDOA	pDOS™	Drivers for MPV901, MPV904, MPV905, MPV950 and MPV952.
PDOB	pDOS™	Drivers for MPV960 and SPV100.

NOTES: (1) All driver packages include demonstration programs.

pSOS-68k™ Software Components Group; VERSAdos™ Motorola, Inc.; pDOS™ Eyring Research Institute, Inc.



The Handbook Of Personal Computer Instrumentation

For Data Acquisition, Test Measurement, And Control

A tutorial section describing, in practical terms, the theory and philosophy of using personal computer instrumentaiton for data acquisition, test, measurement, and control.

An applications section, complete with dozens of diagrams, showing specifically how you can use personal computer instrumentation in more ways than you ever thought possible. Written by leading experts who design and use intelligent instrumentation systems, this section is the (sweet) heart of the handbook. Down-to-earth advice about how to apply PCI.

A software section that describes and references the wide range of packages that are readily available from vendors, and from software houses often overlooked by some firms.

There's more. Much more, including guides on how to configure a system and technical specifications for specific PCI hardware and software. Contact your local Burr-Brown sales office or sales representative for your copy.

PCI-20000 SERIES

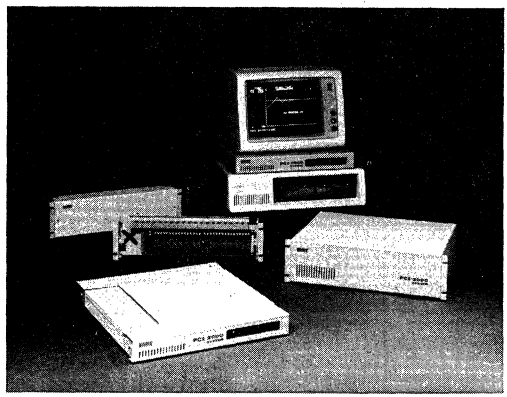
Personal Computer Instrumentation . . .

For Data Acquisition, Test Measurement, And Control

The new PCI-20000 gives you modular I/O you can never outgrow. Component modularity gives you the most cost-effective, expandable PC instrumentation system available today—and tomorrow. The PCI-20000 is an exciting new generation of instrumentation for IBM and bus-compatible personal computers. It lets you start small. Add plug-in channels and functions only as requirements grow. Never pay for more I/O than you need.

The key is component modularity. Carrier cards plug directly into the PC expansion slots and provide power, communications, mounting mechanisms and optional digital I/O capability. Versatile instrument modules plug into the carrier and perform the data acquisition, test, measurement, and control functions your system requires. You can choose from 15 different modules now, with many more planned for the future. Each carrier accepts up to three modules. Different termination panels simplify wiring and bring signals to and from the system.

Hundreds of possible systems can be configured now, even more later. Combine components now to meet exact requirements for



analog and digital I/O, counter, timer, and pulse functions. Change components later to add capacity and functions for future needs. Your system will always be at its optimum price/performance level. Extensive software is available.

PCI-3000

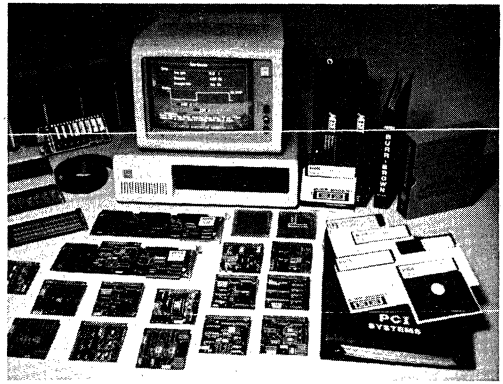
Intelligent Instrumentation for Industry and Laboratory

The PCI-3000 Intelligent Instrumentation Series gives you 1 to 31,744 analog and digital I/O channels, configured to meet your exact industrial computer system requirements.

The PCI-3002/3003 self-contained enclosures communicate with any host via RS-232 or RS-422 interface, with IEEE-488 option. Up to 31 units can be multidropped on RS-422 to make expandable, flexible data acquisition, test, measurement and control networks.

The PCI-3001 series, for large systems up to 31,744 channels, includes an intelligent master enclosure to unburden the host computer. Add expansion enclosures and unique industrial termination panels and enclosures to meet any requirement. Choose from over 25 different analog and digital I/O boards with special functions for signal conditioning, clock inputs, thermocouple inputs, and many more. This series is completely compatible with the PCI-3002/3003 and may be mixed on the same RS-422 communications channel.

The PCI-4901 software support diskettes let users write simple BASIC programs quickly and economically, specifying channel measurement parameters, affecting thermocouple compensation linearization. PCI-20040S-1 software lets users prepare finished



reports, including high-quality graphics, with no direct keyboard entries required.

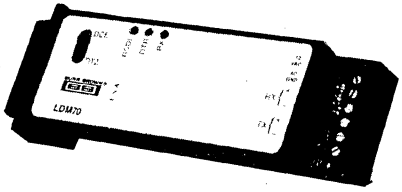
Burr-Brown offers a complete selection of hardware and software to provide all the I/O and special features your industrial system will ever need.

DATA COMMUNICATIONS DEVICES

The LDM line of data communications devices solve the problem of connecting RS-232 and RS-422 computer ports and peripheral devices over extended distances in factories and other institutions. They provide surge suppression and electrical isolation in one low cost unit. No external "lightning sponges" are required. Complete electrical isolation is provided by optical couplers and transformer-coupled DC-to-DC converters to clean up noisy data links by breaking ground loops.

LDM422 provides a low cost bidirectional conversion between RS-232 and RS-422 ports. These units may be used to implement local area networks through multi-drop connection of up to 32 units on a four-wire bus. They may be connected bidirectional two-wire simplex. Request to Send and Clear to Send are carried through and may be used as a second data pair if desired. Surge protection and complete electrical isolation are provided for all lines.

LDM80 is a complete fiber optic RS-232 compatible transmitter-receiver with multi-drop capability and up to 2km between drops at

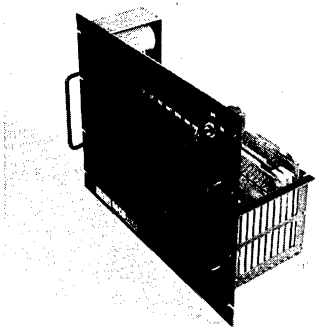


2.5Mbaud, NRZ codes. It is designed for fiber optic local area networks.

The APA120 is a software product, full-functioned RS-232 breakout box, and line adapter that converts a personal computer into a communications protocol analyzer. It provides the function of dedicated instruments costing thousands of dollars.

HIGH SPEED, INDUSTRIAL LIMITED DISTANCE MODEMS							
Series	Surge Protection	Isolation	Distance, max (miles)	Data Rate, max (kbaud)	Connection	Power*	
LDM30	Yes	Receiver	12	57.6	4-wire	DC or AC	
LDM35	Yes	Receiver	7	19.2	4-wire	Signal Power	
LDM70	Yes	Complete	12	57.6	4-wire	DC or AC	
LDM422	Yes	Complete	7	19.2	2, 4, or 8-wire	DC or AC	
FIBER OPTIC TRANSMITTER-RECEIVER							
LDM80	RS-232 or TTL I/O, multi-drop capability, 2km at 2.5Mbaud NRZ, 5Mbaud 50% duty cycle.						
PROTOCOL ANALYZER							
APA120	Software, RS-232 breakout box/adapter, cables and manual.						
APA130	Software and manual only. (Evaluation disk available.)						

*European AC power supplies available.



MCS SERIES

Truly Cost-Effective Analog and Digital I/O

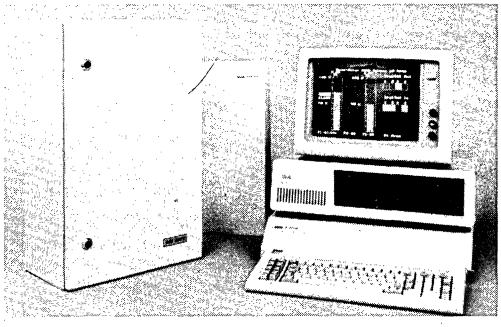
The MCS Series are low-cost, Multibus™-based data acquisition and control systems with 4 or 9 I/O cards. Screw terminations are provided for all I/O, and optional IEEE surge-withstand protection is available. MCS provides direct sensor interface for RTDs and thermocouples, with cold junction compensation and linearization. Voltage, current, and discrete (TTL to 220VAC) I/Os are provided, as well as isolated pulse inputs. Analog data may be scaled 0 to 100%. Other features include: ASCII asynchronous serial interface; dual ports, multidroppable; RS-232, RS-422 and 20mA current loop; −10°C to +60°C in NEMA or rack mount. Process control and display software is available for personal computers and other computer systems.

Multibus™ Intel Corp.

SCADAR SERIES 10

Supervisory Control and Data Acquisition Remote

SCADAR Series 10 is a compact, rugged supervisory control and data acquisition system for local and remote monitoring and control applications. Intelligent and self-contained, Series 10 is a single-board microcomputer system complete with CPU, memory, power supply, and I/O. It is easily interfaced to any host computer through standard communications techniques, and is ideal for remote monitoring and control installations that require low power. The packaging is designed to allow expansion I/O and intelligence for conditioning I/O via plug-in modules. Field I/O connections are made via screwdriver-locked terminations. Two-piece pluggable terminal blocks integral to the base board and I/O modules allow removal of I/O modules and base board electronics without disturbing field connections. SCADAR Series 10 is available in attractive desk-mount or wall-mount general-purpose housings for control-room applications. Series 10 is also available packaged in



NEMA-4 enclosures for use in harsh environments. Process control and display software is available for personal computers and other computer systems.

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Prices in U.S. dollars. F.O.B. Tucson, Arizona Quantity discounts available. **Effective March 31, 1986**

COMPONENT PRODUCTS

Model	1-9	10-24	25-99	100-249
0025MK	1.00	1.00	1.00	
0100MS	11.80	11.80	11.80	9.85
0145MC	4.65	4.65	4.10	3.60
0245MC	5.40	4.90	4.65	4.50
0432MC	8.00	8.00	6.00	5.20
0546	98.50	98.50	94.00	
0548MC	26.00	26.00	26.00	
0549	62.00	62.00	62.00	
0550	67.50	67.50	67.50	
0551	69.50	69.50	69.50	
0552	75.50	75.50	75.50	
0553	97.38	97.38	97.38	
0554	122.25	122.25	122.25	
0556	155.00	155.00	155.00	
0560	68.75	68.75	68.75	
0561	75.10	75.10	75.10	
0562	97.38	97.38	97.38	
0700	48.00	48.00	46.00	
M	50.50	50.50	48.50	
U	38.00	38.00	37.00	
UM	51.50	51.50	50.00	
0710	64.25	64.25	61.00	
0722	49.95	49.95	37.75	34.50
BG	60.35	60.35	49.20	44.85
MG	54.35	54.35	43.55	38.80
0724	66.65	66.65	52.65	48.55
0803HS	3.30	3.30	3.00	2.70
MC	4.95	4.95	4.10	3.85
0804HS	4.85	4.85	4.00	3.75
0805HS	16.50	16.50	16.50	
0806MC	19.00	19.00	19.00	
2014MC	15.00	15.00	15.00	
2020MC	8.00	8.00	8.00	
2026MC	25.00	25.00	25.00	
2201MC	28.00	28.00	28.00	
2220MC	18.00	18.00	18.00	
2240MC	18.00	18.00	18.00	
2250MC	18.00	18.00	18.00	
2302MC	7.75	7.75	7.75	
2350MC	13.00	13.00	13.00	
2360MC	9.00	9.00	9.00	
2525MC	25.50	25.50	25.50	
2803MC	6.30	6.30	5.50	
3291/14	119.00	119.00	113.50	
3292/14	119.00	119.00	113.50	
3293/14	119.00	119.00	113.50	
3329/03	38.60	38.60	33.00	24.00
3354/25	155.00	155.00	149.25	
3355/25	126.50	126.50	122.50	
3356/25	101.00	101.00	99.00	

Model		1-9	10-24	25-99	100-249
3430J		104.00	104.00	101.00	
K		123.00	123.00	117.00	
3450		249.50	249.50	237.50	
3451		217.00	217.00	211.00	
3452		217.00	217.00	211.00	
3455		224.00	224.00	217.00	
3500A		10.30	10.30	8.15	6.40
B		17.60	17.60	14.45	10.85
C		22.45	22.45	18.65	14.20
E		36.25	36.25	28.00	22.25
MP	*	36.25	36.25	28.00	22.25
R		21.25	21.25	16.60	12.50
R/883B	†	20.00	20.00	18.00	17.00
R/MIL	‡†	20.00	20.00	18.00	17.00
RQ		27.50	27.50	22.50	18.00
S		33.00	33.00	25.25	21.20
SQ		44.50	44.50	34.70	29.50
T		53.25	53.25	41.00	33.60
TQ		71.00	71.00	56.50	48.00
U/883B	†	15.00	15.00	13.00	12.00
3501A		6.25	6.25	5.10	4.15
AQ		9.75	9.75	7.65	6.25
B		12.20	12.20	10.10	7.95
BQ		15.75	15.75	13.40	11.10
C		15.95	15.95	13.25	11.20
CQ		20.60	20.60	17.50	14.45
R		17.50	17.50	15.60	11.70
S		25.50	25.50	20.75	16.95
3507J		11.65	11.65	9.65	8.30
JQ		17.35	17.35	13.95	12.35
3508J		10.25	10.25	8.25	7.40
3510AM		9.35	9.35	7.50	5.95
BM		11.85	11.85	9.40	7.45
CM		18.25	18.25	14.25	11.60
SM		18.25	18.25	14.25	11.60
VM/883B	†	35.00	35.00	30.00	25.00
VM/MIL	‡†	35.00	35.00	30.00	25.00
3521H		23.95	23.95	19.45	15.70
J		34.25	34.25	25.90	21.25
JQ		45.15	45.15	34.65	29.40
K		51.40	51.40	38.85	34.25
L		72.40	72.40	55.25	47.00
R		84.25	84.25	68.80	55.70
RQ		110.00	110.00	95.00	82.65
3522J		17.85	17.85	14.35	11.75
K		23.50	23.50	19.40	16.00
L		32.75	32.75	25.25	21.10
S		46.30	46.30	37.30	29.85
SQ		61.65	61.65	51.95	43.65
3523J		33.35	33.35	26.25	21.65
JQ		44.00	44.00	37.00	31.50
K		39.70	39.70	32.95	27.55
L		47.60	47.60	37.80	31.80
LQ		64.00	64.00	54.50	48.95
3527AM		16.25	16.25	12.70	10.95
AMQ		21.80	21.80	17.15	14.85
BM		21.75	21.75	16.50	14.65
BMQ		26.75	26.75	22.05	19.25
CM		33.15	33.15	26.75	23.30

* Prices for the 3500MP are for matched pairs.
Prices subject to change without notice. Minimum order $75.

BURR-BROWN CUSTOMER PRICE LIST

Prices in U.S. dollars. F.O.B. Tucson, Arizona. Quantity discounts available. **Effective March 31, 1986**

Model	1-9	10-24	25-99	100-249
3528AM	20.25	20.25	15.85	12.95
AMQ	27.05	27.05	21.55	17.45
BM	24.85	24.85	19.35	17.55
BMQ	33.00	33.00	25.95	23.60
CM	30.25	30.25	24.15	21.90
CMQ	40.95	40.95	33.65	29.00
3542J	9.75	9.75	8.50	6.50
JQ	15.00	15.00	13.00	11.00
S	15.80	15.80	14.00	12.65
SQ	22.45	22.45	18.75	17.50
3550J	31.20	31.20	25.00	21.45
K	39.75	39.75	31.25	25.50
S	57.80	57.80	46.85	35.70
SQ	78.00	78.00	64.50	51.00
3551J	31.80	31.80	25.25	21.45
S	56.15	56.15	46.25	35.70
SQ	70.00	70.00	60.00	49.00
3553AM	36.00	36.00	28.90	22.45
AMQ	57.00	57.00	50.00	44.00
3554AM	73.20	73.20	57.70	47.70
AMQ	90.00	90.00	74.00	65.00
BM	83.80	83.80	69.30	56.15
BMQ	105.00	105.00	90.00	77.00
SM	97.60	97.60	78.80	66.30
SMQ	130.00	130.00	110.00	94.50
3571AM	72.45	72.45	54.00	48.00
AMQ	98.00	98.00	79.00	69.00
3572AM	83.00	83.00	64.00	54.50
AMQ	112.00	112.00	92.00	78.00
3573AM	36.00	36.00	26.50	25.00
AMQ	49.00	49.00	39.00	35.00
3580J	62.00	62.00	47.50	41.00
JQ	89.00	89.00	69.50	59.00
3581J	93.45	93.45	69.85	61.00
3582J	101.50	101.50	87.40	71.00
JQ	135.00	135.00	119.00	104.00
3583AM	100.00	100.00	85.00	70.00
AMQ	140.00	140.00	118.00	103.00
JM	95.00	95.00	80.00	65.00
3584JM	94.50	94.50	72.50	65.50
JMQ	129.50	129.50	109.00	98.00
3606AG	105.00	105.00	95.00	87.00
BG	137.00	137.00	126.50	113.85
3627AM	12.50	12.50	9.85	9.15
AMQ	25.00	25.00	16.25	13.50
BM	16.75	16.75	12.60	11.25
BMQ	32.50	32.50	20.00	16.75
3630AM	44.00	44.00	34.00	28.00
BM	62.25	62.25	48.70	41.15
CM	95.00	95.00	72.25	64.50
SM	95.00	95.00	72.25	64.50
3650HG	56.25	56.25	42.80	33.75
JG	73.15	73.15	55.15	46.70
KG	88.90	88.90	75.35	65.00
MG	50.40	50.40	36.60	32.00
3652HG	73.15	73.15	57.35	46.70
JG	88.90	88.90	69.70	64.00
MG	57.25	57.25	47.25	42.80
3656AG	86.35	86.35	69.00	57.85
BG	106.75	106.75	85.35	77.85
HG	76.25	76.25	61.00	51.00
JG	81.30	81.30	65.00	54.50
KG	99.95	99.95	79.95	66.95

Model	1-9	10-24	25-99	100-249
4025MC	81.30	81.30	65.00	54.50
4084/25	167.00	167.00	162.00	
4085BM	82. 00	82.00	73.50	59.00
KG	71.00	71.00	60.65	49.50
SM	103.00	103.00	94.50	75.50
4115/04	66.30	66.30	52.50	48.75
4127JG	50.75	50.75	39.40	34.40
KG	58.45	58.45	49.45	43.90
4203J	36.25	36.25	26.00	19.60
K	49.65	49.65	42.75	34.80
S	77.00	77.00	59.00	53.00
SQ	102.50	102.50	82.00	74.00
4204J	68.00	68.00	59.95	51.00
K	88.75	88.75	79.55	64.50
S	101.00	101.00	94.00	82.00
SQ	134.00	134.00	129.00	116.00
4205J	31.95	31.95	26.00	19.95
K	46.50	46.50	37.85	30.25
S	66.45	66.45	52.00	40.00
SQ	88.35	88.35	71.85	56.65
4206J	48.45	48.45	39.95	30.25
K	68.80	68.80	56.65	42.25
4213AM	29.35	29.35	23.45	18.90
AM/S2 (1)	38.16	38.16	30.49	24.57
AM/S3 (1)	33.75	33.75	26.97	21.74
AM/S4 (1)	32.29	32.29	25.80	20.32
AMQ	36.70	36.70	30.60	25.50
BM	42.50	42.50	33.40	28.30
BM/S2 (1)	55.25	55.25	43.42	36.79
BM/S3 (1)	48.88	48.88	38.41	32.55
BM/S4 (1)	46.75	46.75	36.74	30.42
SM	55.00	55.00	46.90	37.75
SM/S2 (1)	71.50	71.50	60.97	49.08
SM/S3 (1)	63.25	63.25	53.94	43.41
SM/S4 (1)	60.50	60.50	51.59	40.58
UM	31.00	31.00	26.00	23.00
UM/883B †	43.00	43.00	37.00	29.00
VM	45.00	45.00	39.00	29.00
VM/883B †	60.00	60.00	49.00	38.00
VM/MIL ‡†	60.00	60.00	49.00	38.00
WM	60.00	60.00	49.00	38.00
WM/883B †	75.00	75.00	62.00	48.00
4214AP	25.25	25.25	21.25	16.80
BP	37.45	37.45	31.20	27.00
RM	30.50	30.50	24.95	23.35
SM	49.40	49.40	42.00	36.75
4302	52.55	52.55	39.70	32.15
4340	90.75	90.75	71.40	64.20
4341	29.20	29.20	24.05	17.95
4423	24.20	24.20	19.50	16.65
AD515JH	17.00	17.00	13.25	9.50
KH	22.75	22.75	18.25	13.85
LH	28.00	28.00	22.50	18.00
ADC10HT	495.00	495.00	455.00	395.00
ADC574AJH	45.00	45.00	36.00	30.00
AKH	59.00	59.00	47.20	39.50
ASH	124.00	124.00	99.00	83.00
ATH	177.00	177.00	141.50	118.50

Model	1-4	5-9	10-24	25-49
ADC600K	1995.00	1895.00	1795.00	1695.00

Model	1-9	10-24	25-99	100-249
ADC674AJH	58.50	58.50	46.75	39.25
AKH	75.00	75.00	60.00	50.25
ASH	158.00	158.00	126.00	106.00
ATH	228.00	228.00	182.00	153.00

(1) BS9400-G0082

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Prices in U.S. dollars. F.O.B. Tucson, Arizona. Quantity discounts available. **Effective March 31, 1986**

Model	1-9	10-24	25-99	100-249
ADC71JG	87.00	87.00	82.00	63.00
KG	109.00	109.00	102.00	78.00
ADC72AM	207.00	207.00	194.00	149.00
BM	258.00	258.00	242.00	186.00
JM	173.00	173.00	162.00	125.00
KM	216.00	216.00	202.00	155.00
ADC731J	440.00	440.00	434.00	
K	465.00	465.00	458.00	
ADC73J	420.00	420.00	414.00	
K	465.00	465.00	457.00	
ADC76AM	255.00	255.00	214.00	184.00
BM	300.00	300.00	252.00	216.00
JG	139.00	139.00	129.00	99.00
JM	175.00	175.00	147.00	126.00
KG	159.00	159.00	146.00	119.00
KM	220.00	220.00	185.00	158.00
ADC803BM	239.00	239.00	199.00	162.00
BMQ	292.00	292.00	244.00	195.00
CM	265.00	265.00	225.00	180.00
CMQ	335.00	335.00	279.00	223.00
SM	364.00	364.00	304.00	243.00
SMQ	456.00	456.00	380.00	304.00
ADC804BH	55.00	55.00	45.00	39.00
BHQ	86.00	86.00	69.00	55.00
SH	104.00	104.00	83.00	66.00
SHQ	130.00	130.00	104.00	83.00
ADC80AG-10	79.50	79.50	63.00	44.00
AG-12	81.00	81.00	64.00	44.50
AGZ-12	83.00	83.00	66.00	46.00
H-AH-12	81.00	81.00	64.00	44.50
H-AH-12Q	105.00	105.00	84.00	58.00
ADC82AG	65.00	65.00	52.00	44.00
AM	94.00	94.00	75.00	63.00
AMQ	127.00	127.00	110.00	100.00
ADC84KG-10	110.00	110.00	87.00	71.00
KG-12	115.00	115.00	90.00	77.00
ADC85-10	151.00	151.00	137.00	99.00
-12	171.00	171.00	138.00	105.00
C-12	132.00	132.00	106.00	86.00
Q-10	172.00	172.00	139.00	115.00
Q-12	206.00	206.00	165.00	138.00
ADC87	220.00	220.00	205.00	195.00
/883B †	270.00	270.00	250.00	230.00
/MIL ‡†	270.00	270.00	250.00	230.00
U	172.00	172.00	160.00	150.00
U/883B †	206.00	206.00	206.00	190.00
V	220.00	220.00	205.00	195.00
V/883B †	270.00	270.00	250.00	230.00
V/MIL ‡†	270.00	270.00	250.00	230.00
BOOK-01	33.50			
Operational Amplifiers—Design and Applications				
BOOK-02	33.50			
Applications of Operational Amplifiers—Third Generation Techniques				
BOOK-03	29.50			
Function Circuits—Theory and Applications				
BOOK-04	29.50			
Designing With Operational Amplifiers—Applications Alternatives				
DAC10HT	295.00	295.00	230.00	170.00
DAC1200KP-V	9.50	9.50	9.50	5.95
DAC1201KP-L-V	11.20	11.20	11.20	6.95
DAC1600JP-V	14.35	14.35	14.35	8.95
KP-V	15.95	15.95	15.95	9.95
DAC60-10	147.00	147.00	141.00	
-12	157.00	157.00	151.00	

Model	1-9	10-24	25-99	100-249
DAC63BG	108.00	108.00	89.00	83.00
BM	126.00	126.00	107.00	97.00
CG	119.00	119.00	99.00	92.00
CM	139.00	139.00	119.00	107.00
SM	209.00	209.00	182.00	166.00
TM	229.00	229.00	203.00	184.00
DAC70BH-COB-I	130.00	130.00	108.00	90.00
BH-CSB-I	130.00	130.00	108.00	90.00
DAC700BH	58.00	58.00	46.00	39.00
BH/QM	67.00	67.00	53.00	45.00
BL	87.00	87.00	69.00	59.00
BL/QM	99.00	99.00	79.00	68.00
KH	46.00	46.00	35.00	29.00
SH	84.00	84.00	67.00	56.00
SH/QM	97.00	97.00	77.00	65.00
SL	147.00	147.00	117.00	99.00
SL/QM	169.00	169.00	134.00	114.00
DAC701BH	58.00	58.00	46.00	39.00
BH/QM	67.00	67.00	53.00	45.00
BL	87.00	87.00	69.00	59.00
BL/QM	99.00	99.00	79.00	68.00
KH	46.00	46.00	35.00	29.00
SH	84.00	84.00	67.00	56.00
SH/QM	97.00	97.00	77.00	65.00
SL	147.00	147.00	117.00	99.00
SL/QM	169.00	169.00	134.00	114.00
DAC702BH	58.00	58.00	46.00	39.00
BH/QM	67.00	67.00	53.00	45.00
BL	87.00	87.00	69.00	59.00
BL/QM	99.00	99.00	79.00	68.00
JP	20.50	20.50	18.65	17.00
KH	46.00	46.00	35.00	29.00
KP	22.95	22.95	20.90	19.00
SH	84.00	84.00	67.00	56.00
SH/QM	97.00	97.00	77.00	65.00
SL	147.00	147.00	117.00	99.00
SL/QM	169.00	169.00	134.00	114.00
DAC703BH	58.00	58.00	46.00	39.00
BH/QM	67.00	67.00	53.00	45.00
BL	87.00	87.00	69.00	59.00
BL/QM	99.00	99.00	79.00	68.00
JP	20.50	20.50	18.65	17.00
KH	46.00	46.00	35.00	29.00
KP	22.95	22.95	20.90	19.00
SH	84.00	84.00	67.00	56.00
SH/QM	97.00	97.00	77.00	65.00
SL	147.00	147.00	117.00	99.00
SL/QM	169.00	169.00	134.00	114.00
DAC705BH	73.00	73.00	69.00	54.00
BH/QM	84.00	84.00	79.00	62.00
KH	63.00	63.00	51.00	44.00
SH	95.00	95.00	89.00	70.00
SH/QM	109.00	109.00	103.00	81.00
DAC706BH	73.00	73.00	69.00	54.00
BH/QM	84.00	84.00	79.00	62.00
KH	63.00	63.00	51.00	44.00
SH	95.00	95.00	89.00	70.00
SH/QM	109.00	109.00	103.00	81.00
DAC707BH	73.00	73.00	69.00	54.00
BH/QM	84.00	84.00	79.00	62.00
KH	63.00	63.00	51.00	44.00
KP	29.00	29.00	24.50	21.00
SH	95.00	95.00	89.00	70.00
SH/QM	109.00	109.00	103.00	81.00
DAC708BH	73.00	73.00	69.00	54.00
BH/QM	84.00	84.00	79.00	62.00
KH	63.00	63.00	51.00	44.00
SH	95.00	95.00	89.00	70.00
SH/QM	109.00	109.00	103.00	81.00

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Model	1-9	10-24	25-99	100-249
DAC709BH	73.00	73.00	69.00	54.00
BH/QM	84.00	84.00	79.00	62.00
KH	63.00	63.00	51.00	44.00
KP	29.00	29.00	24.50	21.00
SH	95.00	95.00	89.00	70.00
SH/QM	109.00	109.00	103.00	81.00
DAC710KH	43.00	43.00	34.00	29.00
DAC71-CCD-I	55.00	55.00	48.00	42.00
-CCD-V	58.00	58.00	52.00	48.00
-COB-I	50.00	50.00	42.00	37.00
-COB-V	53.00	53.00	45.00	39.00
-CSB-I	50.00	50.00	42.00	37.00
-CSB-V	53.00	53.00	45.00	39.00
DAC711KH	43.00	43.00	34.00	29.00
DAC72BH-COB-I	75.00	75.00	63.00	51.00
BH-COB-V	78.00	78.00	66.00	53.00
BH-CSB-I	75.00	75.00	63.00	51.00
BH-CSB-V	78.00	78.00	66.00	53.00
DAC73J	355.00	355.00	349.00	
K	392.00	392.00	386.00	
DAC736J	357.00	357.00	350.00	
K	398.00	398.00	392.00	
DAC7700KD			24.00	17.50
DAC7701KD			24.00	17.50
DAC80-CBI-I	23.00	23.00	18.25	15.25
-CBI-V	24.00	24.00	19.00	16.00
-CCD-I	42.00	42.00	37.50	25.00
-CCD-V	42.50	42.50	38.00	26.00
P-CBI-I	20.00	20.00	16.00	13.25
P-CBI-V	21.00	21.00	16.75	14.00
Z-CBI-I	23.00	23.00	18.25	15.25
Z-CBI-V	24.00	24.00	19.00	16.00
DAC800-CBI-I	23.00	23.00	19.00	15.00
-CBI-V	27.50	27.50	23.00	18.00
P-CBI-I	20.25	20.25	16.20	13.65
P-CBI-V	25.00	25.00	21.00	16.00
DAC811AH	22.50	22.50	17.90	14.90
AH/QM	28.25	28.25	22.50	18.75
AL	29.25	29.25	23.25	19.40
AL/QM	36.75	36.75	29.25	24.25
BH	28.50	28.50	22.50	18.90
BH/QM	35.75	35.75	28.25	23.75
BL	37.00	37.00	29.25	24.60
BL/QM	46.50	46.50	37.00	31.00
JD			15.25	9.60
JP	18.60	18.60	14.90	11.90
KP	24.75	24.75	19.80	15.85
RH	79.00	79.00	63.00	53.00
RH/QM	91.00	91.00	73.00	61.00
RL	103.00	103.00	82.00	69.00
RL/QM	119.00	119.00	95.00	80.00
SH	130.00	130.00	106.00	86.00
SH/QM	150.00	150.00	122.00	99.00
SL	169.00	169.00	138.00	112.00
SL/QM	195.00	195.00	159.00	129.00
DAC812BM	119.00	105.00	95.00	86.00
CM	159.00	141.00	127.00	115.00
DAC82KG	34.00	34.00	27.00	23.00
DAC85H-CBI-I	34.50	34.50	27.50	24.00
H-CBI/QM	42.00	42.00	33.50	29.50
H-CBI-V	36.00	36.00	29.00	25.00
H-CBI-V/QM	44.00	44.00	35.50	30.50
L-V	36.00	36.00	29.00	25.00
L-V/QM	44.00	44.00	35.50	30.50

Model	1-9	10-24	25-99	100-249
DAC850-CBI-I	33.00	33.00	26.00	22.00
-CBI-I/QM	41.00	41.00	32.50	27.50
-CBI-V	35.00	35.00	28.00	23.50
-CBI-V/QM	44.00	44.00	35.00	29.50
BL-I	43.00	43.00	34.00	29.00
BL-I/QM	54.00	54.00	43.00	36.50
BL-V	46.00	46.00	36.00	30.50
BL-V/QM	58.00	58.00	45.00	38.50
DAC851-CBI-I	49.00	49.00	39.00	33.00
-CBI-I/QM	56.50	56.50	45.00	38.00
-CBI-V	53.00	53.00	42.50	35.50
-CBI-V/QM	61.00	61.00	49.00	41.00
SL-I	64.00	64.00	51.00	43.00
SL-I/QM	74.00	74.00	59.00	49.50
SL-V	69.00	69.00	56.00	46.00
SL-V/QM	79.00	79.00	64.00	53.00
DAC87-CBI-I	115.00	115.00	105.00	95.00
-CBI-I/B †	125.00	125.00	115.00	105.00
-CBI-V	120.00	120.00	110.00	100.00
-CBI-V/B †	130.00	130.00	120.00	110.00
-CBI-V/MIL ‡†	130.00	130.00	120.00	110.00
8300201XC	170.00	170.00	163.00	155.00
H-CBI-V	79.00	79.00	63.00	55.00
H-CBI-V/QM	96.00	96.00	77.00	67.00
L-V	79.00	79.00	63.00	55.00
L-V/QM	96.00	96.00	77.00	67.00
U-CBI-I	90.00	80.00	80.00	70.00
U-CBI-I/B †	100.00	100.00	90.00	80.00
U-CBI-V	95.00	95.00	85.00	75.00
U-CBI-V/B †	105.00	105.00	95.00	85.00
DAC870U	45.00	45.00	40.00	35.00
U/883B †	65.00	65.00	60.00	55.00
UL	50.00	50.00	45.00	40.00
UL/883B †	70.00	70.00	65.00	60.00
V	80.00	80.00	75.00	67.00
V/883B †	100.00	100.00	95.00	80.00
V/MIL ‡†	100.00	100.00	95.00	80.00
VL	85.00	85.00	80.00	72.00
VL/883B †	105.00	105.00	100.00	90.00
VL/MIL ‡†	105.00	105.00	100.00	90.00
DAC90BG	19.50	19.50	15.50	13.00
SG	27.00	27.00	22.00	18.00
DIV100HP	30.25	30.25	24.15	18.15
JP	42.25	42.25	36.25	27.75
KP	60.35	60.35	51.95	39.85
DTP-05	195.00	195.00		
E	195.00	195.00		
INA101AD			8.90	4.95
AG	17.95	17.95	13.50	11.00
AM	14.00	14.00	10.50	7.25
AM/S2	10.00	10.00	10.85	9.45
AM/S3	16.10	16.10	12.08	8.34
AM/S4	15.40	15.40	11.55	7.79
BM/S2	22.10	22.10	16.56	11.44
BM/S3	19.55	19.55	14.65	10.12
BM/S4	18.70	18.70	14.01	9.46
CG	23.00	23.00	17.25	16.35
CM	18.40	18.40	13.80	12.85
CM/S2	23.92	23.92	17.94	16.71
CM/S3	21.16	21.16	15.87	14.78
CM/S4	20.24	20.24	15.18	13.81
HP	6.95	6.95	5.45	4.95
SG	24.75	24.75	18.50	17.65
SGQ	35.00	35.00	27.00	25.00
SM	19.50	19.50	14.65	13.95
SM/S2	25.35	25.35	19.05	18.14
SM/S3	22.43	22.43	16.85	16.04
SM/S4	21.45	21.45	16.12	15.00
SMQ	28.00	28.00	21.00	20.00

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Model		1-9	10-24	25-99	100-249
INA102AD				9.35	5.20
AG		13.95	13.95	11.15	7.95
CG		18.40	18.40	15.85	11.35
INA104AM		24.25	24.25	19.25	17.95
BM		29.00	29.00	23.25	21.65
CM		37.45	37.45	29.85	27.85
HP		18.75	18.75	14.95	13.95
JP		22.50	22.50	17.95	16.75
KP		29.00	29.00	23.25	21.65
SM		40.00	40.00	31.75	29.65
INA105AM		9.50	9.50	7.15	5.75
BM		11.85	11.85	8.95	7.20
KP		5.75	5.75	4.35	3.50
INA110AG		16.85	16.85	12.65	8.85
BG		23.60	23.60	17.75	12.35
INA258UG		34.00	34.00	34.00	25.00
UG/883B	†	38.00	38.00	38.00	28.00
UL		37.00	37.00	37.00	27.00
UL/883B	†	41.00	41.00	41.00	31.00
VG		45.00	45.00	41.00	38.00
VG/883B	†	60.00	60.00	55.00	53.00
VG/MIL	‡†	60.00	60.00	55.00	53.00
VL		49.00	49.00	45.00	42.00
VL/883B	†	68.00	68.00	61.00	58.00
VL/MIL	‡†	68.00	68.00	61.00	58.00
WG		58.00	58.00	52.00	49.00
WG/883B	†	78.00	78.00	70.00	66.00
WG/MIL	‡†	78.00	78.00	70.00	66.00
WL		64.00	64.00	57.00	53.00
WL/883B	†	86.00	86.00	77.00	72.00
WL/MIL	‡†	86.00	86.00	77.00	72.00
ISO100AP		32.50	32.50	28.75	25.50
BP		35.40	35.40	31.60	28.65
CP		39.50	39.50	36.30	33.60
LOG100JP		43.00	43.00	35.00	30.00
MP22BG		324.00	285.00	259.00	217.00
MP32BG		324.00	280.00	259.00	217.00
CG		405.00	405.00	324.00	272.00
MPC16S		23.21	23.21	20.06	17.00
MPC4D		12.97	12.97	11.21	9.50
MPC800KG		27.86	27.86	23.06	19.22
SG		55.67	55.67	46.07	38.39
MPC801KG		14.50	14.50	12.00	10.00
SG		30.00	30.00	24.83	20.69
MPC8D		23.21	23.21	20.06	17.00
S		12.97	12.97	11.21	9.50
MPY100AG		13.85	13.85	12.45	10.95
AM		10.50	10.50	9.45	7.50
AM/S2	(2)	13.65	13.65	12.29	9.75
AM/S3	(2)	12.08	12.08	10.87	8.63
AM/S4	(2)	11.55	11.55	10.40	8.06
BG		22.45	22.45	20.45	16.40
BM		17.00	17.00	15.45	11.65
BM/S2	(2)	22.10	22.10	20.09	15.15
BM/S3	(2)	19.55	19.55	17.77	13.40
BM/S4	(2)	18.70	18.70	17.00	12.52
CG		33.70	33.70	31.00	26.25
CM		25.50	25.50	23.45	19.95
CM/S2	(2)	33.15	33.15	30.49	25.94
CM/S3	(2)	29.33	29.33	26.97	22.94
CM/S4	(2)	28.05	28.05	25.80	21.45
SG		50.55	50.55	46.50	32.00
SGQ		69.00	69.00	62.50	46.50
SM		38.25	38.25	35.20	27.25
SM/S2	(2)	49.73	49.73	45.76	35.43
SM/S3	(2)	43.99	43.99	40.48	31.34
SM/S4	(2)	42.08	42.08	38.72	29.29
SMQ		52.00	52.00	47.50	41.00
MPY534JD		27.95	27.95	23.45	16.75
JH		21.50	21.50	17.95	12.85
KD		39.95	39.95	33.85	24.65
KH		32.85	32.85	27.35	19.85
LD		59.70	59.70	49.35	36.85
LH		48.50	48.50	39.95	29.50
SD		75.85	75.85	62.95	47.00
SH		64.75	64.75	53.35	39.85
TD		107.40	107.40	89.50	64.00
TH		91.80	91.80	76.50	54.50
MPY634AM		16.65	16.65	13.85	9.95
BM		24.75	24.75	20.55	15.25
KP		12.85	12.85	10.65	7.95
SM		59.65	59.65	49.85	37.85
OPA101AM		35.00	35.00	29.85	23.25
BM		43.50	43.50	37.50	32.75
OPA102AM		37.00	37.00	31.75	24.25
BM		45.00	45.00	38.65	33.50
OPA103AM		10.50	10.50	8.60	6.80
BM		14.20	14.20	11.45	8.95
CM		18.60	18.60	14.85	11.55
DM		29.85	29.85	23.85	18.50
OPA104AM		17.50	17.50	13.95	10.25
BM		23.65	23.65	18.95	14.50
CM		29.50	29.50	23.50	19.00
OPA105UM		25.00	25.00	23.50	22.00
UM/883B	†	30.00	30.00	28.00	25.00
VM		35.00	35.00	32.00	30.00
VM/883B	†	48.00	48.00	44.00	40.00
VM/MIL	‡†	48.00	48.00	44.00	40.00
WM		47.00	47.00	42.00	40.00
WM/883B	†	66.00	66.00	59.00	52.00
WM/MIL	‡†	66.00	66.00	59.00	52.00
OPA106UM		28.00	28.00	25.00	22.00
UM/883B	†	34.00	34.00	32.00	28.00
VM		38.00	38.00	35.00	32.00
VM/883B	†	53.00	53.00	49.00	44.00
VM/MIL	‡†	53.00	53.00	49.00	44.00
WM		50.00	50.00	45.00	42.00
WM/883B	†	70.00	70.00	63.00	57.00
WM/MIL	‡†	70.00	70.00	63.00	57.00
OPA11HT		49.00	49.00	46.55	39.20
OPA111AD				6.75	3.85
AM		9.75	9.75	7.95	5.45
AM/S2		12.68	12.68	10.34	7.09
AM/S3		11.21	11.21	9.14	6.27
AM/S4		10.73	10.73	8.75	5.86
BM		15.35	15.35	12.25	9.95
BM/S2		19.96	19.96	15.93	12.94
BM/S3		17.65	17.65	14.09	11.44
BM/S4		16.89	16.89	13.48	10.70
HT		52.75	52.75	45.25	37.00
SM		16.85	16.85	13.95	11.95
SM/S2		21.91	21.91	18.14	15.54
SM/S3		19.38	19.38	16.04	13.74
SM/S4		18.54	18.54	15.35	12.85
SMQ		22.75	22.75	19.50	15.95
OPA121KM		6.85	6.85	4.50	3.40
KM/S2		8.91	8.91	5.85	5.85
KM/S3		7.88	7.88	5.18	5.18
KM/S4		7.54	7.54	4.95	4.84
KP		5.65	5.65	3.65	2.75
OPA128JM		17.50	17.50	13.95	10.25
KM		25.00	25.00	20.00	15.50
LM		31.50	31.50	25.00	20.00
SM		54.25	54.25	44.95	38.50
OPA156AM		11.25	11.25	8.95	6.75

(2) BS9400-G0083

Prices subject to change without notice. Minimum order $75.

BURR-BROWN CUSTOMER PRICE LIST

Prices in U.S. dollars. F.O.B. Tucson, Arizona. Quantity discounts available. **Effective March 31, 1986**

Model		1-9	10-24	25-99	100-249
OPA201AG		7.50	7.50	5.25	3.95
BG		11.65	11.65	8.15	6.15
CG		13.95	13.95	9.75	7.45
SG		15.25	15.25	10.75	8.15
OPA2111AD				9.95	6.95
AM		14.50	14.50	11.50	9.95
BM		25.95	25.95	20.85	16.50
SM		26.50	26.50	21.20	16.75
OPA21EZ		8.95	8.95	7.15	5.95
GZ		4.45	4.45	3.60	2.95
OPA27AJ		19.95	19.95	15.65	12.50
AJ/S2	(3)	25.94	25.94	20.35	16.25
AJ/S3	(3)	22.94	22.94	18.00	14.38
AJ/S4	(3)	21.95	21.95	16.82	13.44
AJQ		32.85	32.85	25.00	18.75
AZ		19.95	19.95	15.65	12.50
AZQ		32.85	32.85	25.00	18.75
BJ		12.85	12.85	9.65	7.65
BJ/S2	(3)	16.71	16.71	12.55	9.95
BJ/S3	(3)	14.78	14.78	11.10	8.80
BJ/S4	(3)	14.14	14.14	10.37	8.22
BJQ		21.20	21.20	15.45	11.85
BZ		12.85	12.85	9.65	7.65
BZQ		21.20	21.20	15.45	11.85
CD				6.30	4.20
CJ		9.95	9.95	7.50	5.95
CJ/S2	(3)	12.94	12.94	9.75	7.74
CJ/S3	(3)	11.44	11.44	8.63	6.84
CJ/S4	(3)	10.95	10.95	8.06	6.40
CJQ		16.45	16.45	12.00	9.25
CZ		9.95	9.95	7.50	5.95
CZQ		16.45	16.45	12.00	9.25
EJ		11.00	11.00	8.35	6.65
EJ/S2	(3)	14.30	14.30	10.86	8.65
EJ/S3	(3)	12.65	12.65	9.60	7.65
EJ/S4	(3)	12.10	12.10	8.98	7.15
EZ		11.00	11.00	8.35	6.65
FJ		8.55	8.55	5.95	4.95
FJ/S2	(3)	11.12	11.12	7.74	6.44
FJ/S3	(3)	9.83	9.83	6.84	5.69
FJ/S4	(3)	9.41	9.41	6.40	5.32
FZ		8.55	8.55	5.95	4.95
GD				4.20	2.80
GJ		6.00	6.00	4.95	4.00
GJ/S2	(3)	7.80	7.80	6.44	5.20
GJ/S3	(3)	6.90	6.90	5.69	4.60
GJ/S4	(3)	6.60	6.60	5.32	4.30
GP		5.25	5.25	3.95	2.95
GZ		6.00	6.00	4.95	4.00
HT		59.90	59.90	51.35	42.00
OPA356AM		7.25	7.25	5.95	4.50
OPA37AJ		19.95	19.95	15.65	12.50
AJ/S2	(4)	25.94	25.94	20.35	16.25
AJ/S3	(4)	22.94	22.94	18.00	14.38
AJ/S4	(4)	21.95	21.95	16.82	13.44
AJQ		32.85	32.85	25.00	18.75
AZ		19.95	19.95	15.65	12.50
AZQ		32.85	32.85	25.00	18.75
BJ		12.85	12.85	9.65	7.65
BJ/S2	(4)	16.71	16.71	12.55	9.95
BJ/S3	(4)	14.78	14.78	11.10	8.80
BJ/S4	(4)	14.14	14.14	10.37	8.22
BJQ		21.20	21.20	15.45	11.85
BZ		12.85	12.85	9.65	7.65
BZQ		21.20	21.20	15.45	11.85
CD				6.30	4.20
CJ		9.95	9.95	7.50	5.95
CJ/S2	(4)	12.94	12.94	9.75	7.74
CJ/S3	(4)	11.44	11.44	8.63	6.84
CJ/S4	(4)	10.95	10.95	8.06	6.40
CJQ		16.45	16.45	12.00	9.25
CZ		9.95	9.95	7.50	5.95
CZQ		16.45	16.45	12.00	9.25
EJ		11.00	11.00	8.35	6.65
EJ/S2	(4)	14.30	14.30	10.86	8.65
EJ/S3	(4)	12.65	12.65	9.60	7.65
EJ/S4	(4)	12.10	12.10	8.98	7.15
EZ		11.00	11.00	8.35	6.65
FJ		8.55	8.55	5.95	4.95
FJ/S2	(4)	11.12	11.12	7.74	6.44
FJ/S3	(4)	9.83	9.83	6.84	5.69
FJ/S4	(4)	9.41	9.41	6.40	5.32
FZ		8.55	8.55	5.95	4.95
GD				4.20	2.80
GJ		6.00	6.00	4.95	4.00
GJ/S2	(4)	7.80	7.80	6.44	5.20
GJ/S3	(4)	6.90	6.90	5.69	4.60
GJ/S4	(4)	6.60	6.60	5.32	4.30
GP		5.25	5.25	3.95	2.95
GZ		6.00	6.00	4.95	4.00
HT		59.90	59.90	51.35	42.00
OPA404AG		14.95	14.95	12.50	8.95
BG		19.75	19.75	15.75	12.85
SG		29.25	29.25	23.25	19.95
KP		11.85	11.85	9.25	6.95
OPA501AM		53.40	53.40	40.00	32.50
BM		63.00	63.00	47.85	37.85
RM		68.50	68.50	49.25	42.50
SM		82.00	82.00	59.85	49.95
SMQ		112.00	112.00	87.00	72.00
OPA511AM		45.00	45.00	38.50	34.50
OPA512BM		63.50	63.50	53.95	48.50
SM		76.50	76.50	66.50	61.50
OPA600BM		97.00	97.00	81.00	74.00
CM		119.00	119.00	101.00	97.00
SM		122.00	122.00	101.00	97.00
TM		149.00	149.00	135.00	129.00
UM		143.00	143.00	115.00	102.00
UM/883	†	165.00	165.00	145.00	118.00
VM		175.00	175.00	153.00	143.00
VM/883B	†	195.00	195.00	176.00	163.00
VM/MIL	‡†	195.00	195.00	176.00	163.00
OPA605AM		64.00	64.00	54.50	48.00
CM		89.00	89.00	74.50	66.75
HG		51.50	51.50	45.00	40.50
KG		76.65	76.65	67.00	57.50
OPA606KM		5.70	5.70	4.35	3.50
KP		3.75	3.75	2.85	2.30
LM		13.85	13.85	9.95	8.25
SM		14.25	14.25	10.25	8.50

(3) BS9460-F0648
(4) BS9400-F0649
Prices subject to change without notice. Minimum order $75.

Prices in U.S. dollars. F.O.B. Tucson, Arizona Quantity discounts available. **Effective March 31, 1986**

Model		1-9	10-24	25-99	100-249
OPA8780UM		102.00	102.00	81.00	72.00
UM/883B	†	135.00	135.00	106.00	95.00
VM		125.00	125.00	99.00	88.00
VM/883B	†	215.00	215.00	176.00	152.00
VM/MIL	‡†	215.00	215.00	176.00	152.00
OPA8785UM		73.00	73.00	69.00	66.00
UM/883B	†	86.00	86.00	82.00	77.25
VM		97.00	97.00	86.00	71.50
VM/883B	†	110.00	110.00	99.00	88.00
PCM53JG-I		37.00	37.00	32.50	23.00
JG-V		37.00	37.00	32.50	23.00
JP-I		19.50	19.50	19.50	12.15
JP-V		19.50	19.50	19.50	12.15
KP-I		21.25	21.25	21.25	13.25
KP-V		21.25	21.25	21.25	13.25
PCM54HP		17.50	17.50	17.50	10.90
JP		19.50	19.50	19.50	12.15
KP		21.25	21.25	21.25	13.25
PCM55HP		17.50	17.50	17.50	10.90
JP		19.50	19.50	19.50	12.15
PCM75JG		122.00	122.00	114.00	87.00
KG		139.00	139.00	129.00	99.00
PGA100AG		65.00	65.00	55.00	49.50
BG		72.00	72.00	62.00	54.00
PGA102AG		10.95	10.95	9.00	7.65
BG		19.95	19.95	16.25	13.75
KP		5.95	5.95	4.75	3.95
SG		24.45	24.45	19.95	16.75
PGA200AG		51.50	51.50	39.95	34.75
BG		57.85	57.85	46.75	41.00
PGA201AG		51.50	51.50	39.95	34.75
BG		57.85	57.85	46.75	41.00
PSX-24		35.00	35.00	35.00	
PWR70	§	43.00	40.00	37.00	30.10
71	§	61.00	57.00	52.00	42.70
72	§	49.00	46.00	42.00	34.30
74	§	48.00	45.00	41.00	33.60
76	§	67.00	62.00	57.00	46.90
PWR1xx Series	§	33.00	31.00	29.00	23.00
2xx Series	§	38.00	36.00	33.00	27.00
3xx Series	§	43.00	40.00	37.00	30.00
4xx Series	§	49.00	46.00	42.00	34.00
5xx Series	§	59.00	55.00	51.00	41.00
6xx Series	§	54.00	50.00	46.00	38.00
7xx Series	§	81.00	75.00	69.00	57.00
8xx Series	§	92.00	86.00	79.00	65.00
REF101JM		30.90	30.90	27.80	22.50
KM		38.50	38.50	35.00	28.80
RM		33.75	33.75	30.70	25.20
RMQ		47.50	47.50	43.00	35.00
SM		42.35	42.35	38.95	32.40
SMQ		59.00	59.00	54.00	46.00
REF10JM		17.40	17.40	15.65	13.35
KM		21.85	21.85	19.65	16.75
RM		19.95	19.95	17.95	15.35
RMQ		28.00	28.00	25.00	21.85
SM		29.40	29.40	26.35	22.50
SMQ		41.00	41.00	36.50	31.85
RF-500-108		8.00	8.00	7.50	7.00
SDM853		329.00	329.00	323.00	
SDM854AG		210.00	210.00	168.00	141.00
BG		233.00	233.00	187.00	156.00
SDM856JG		181.00	181.00	145.00	121.00
KG		219.00	219.00	175.00	147.00
SDM857JG		194.00	194.00	155.00	130.00
KG		232.00	232.00	186.00	155.00
SHC298AM		6.95	6.95	5.50	4.50
SHC5320KH		13.40	13.40	11.60	9.80
SH		61.00	61.00	52.75	44.70
SHC600BH		299.00	295.00	276.00	254.00
SHC76BM		85.00	85.00	68.00	57.00
KM		77.00	77.00	62.00	52.00
SHC803BM		162.00	143.00	129.00	117.00
CM		184.00	163.00	146.00	133.00
SHC804BM		145.00	129.00	115.00	105.00
CM		159.00	141.00	126.00	115.00
SHC80KP		51.00	51.00	41.00	34.00
SHC85		85.00	85.00	68.00	57.00
ET		129.00	129.00	110.00	106.00
ETQ		179.00	179.00	162.00	155.00
Q		137.00	137.00	110.00	92.00
SHM60		140.00	140.00	135.00	
UAF11		53.60	53.60	40.70	26.40
UAF21		85.50	85.50	78.65	53.35
UAF41		20.85	20.85	14.10	11.50
VFC100AG		13.25	13.25	9.95	7.95
BG		21.50	21.50	18.35	15.60
SG		18.95	18.95	15.95	13.65
VFC320BG		15.95	15.95	11.75	8.95
BM		15.60	15.60	11.40	8.75
BM/S2	(5)	20.28	20.28	14.82	11.38
BM/S3	(5)	17.94	17.94	13.11	10.06
BM/S4	(5)	17.16	17.16	12.54	9.41
CG		18.50	18.50	13.65	11.50
CM		16.60	16.60	12.45	10.45
CM/S2	(5)	21.58	21.58	16.19	13.59
CM/S3	(5)	19.09	19.09	14.32	12.02
CM/S4	(5)	18.26	18.26	13.70	11.23
SM		20.65	20.65	15.60	13.40
SM/S2	(5)	26.85	26.85	20.28	17.42
SM/S3	(5)	23.75	23.75	17.94	15.41
SM/S4	(5)	22.72	22.72	17.16	14.41
VFC32BD				8.45	5.55
BM		11.95	11.95	9.95	7.95
BM/S2	(6)	15.54	15.54	12.94	10.34
BM/S3	(6)	13.74	13.74	11.44	9.14
BM/S4	(6)	13.15	13.15	10.95	8.55
BMQ		16.85	16.85	13.95	11.95
KP		8.95	8.95	7.45	5.95
SM		17.25	17.25	14.40	11.50
SM/S2	(6)	22.43	22.43	18.72	14.95
SM/S3	(6)	19.84	19.84	16.56	13.23
SM/S4	(6)	18.98	18.98	15.84	12.36
SMQ		23.30	23.30	19.45	15.55
UM		15.00	15.00	11.00	7.50
UM/883B	†	20.00	20.00	16.00	12.50
VM		26.00	26.00	21.00	18.00
VM/883B	†	50.00	50.00	41.00	33.00
VM/MIL	‡†	50.00	50.00	41.00	33.00
WM		40.00	40.00	35.00	30.00
WM/883B	†	45.00	45.00	40.00	35.00
VFC42BM		29.65	29.65	25.15	21.95
BP		21.35	21.35	17.35	15.70
SM		36.00	36.00	30.00	24.65
VFC52BM		29.65	29.65	25.00	21.95
BP		21.35	21.35	17.35	15.70
SM		36.00	36.00	30.00	24.65

§ /B, Level I Screening, add 25% to pricing indicated above;
/S, Level II Screening, add 45% to pricing indicated above.
(5) BS9400-G0101
(6) BS9400-G0100
Prices subject to change without notice. Minimum order $75.

Prices in U.S. dollars. F.O.B. Tucson, Arizona Quantity discounts available. **Effective March 31, 1986**

Model		1-9	10-24	25-99	100-249
VFC62BG		15.95	15.95	11.75	8.95
BM		15.60	15.60	11.40	8.75
BM/S2	(7)	23.26	23.26	16.99	13.04
BM/S3	(7)	20.57	20.57	15.00	11.53
BM/S4	(7)	19.68	19.68	14.38	10.78
CG		18.50	18.50	13.65	11.50
CM		16.60	16.60	12.45	10.40
CM/S2	(7)	24.75	24.75	18.56	15.50
CM/S3	(7)	21.90	21.90	16.42	13.71
CM/S4	(7)	20.95	20.95	15.71	12.81
SM		20.65	20.65	15.60	13.40
SM/S2	(7)	30.78	30.78	23.37	19.98
SM/S3	(7)	27.23	27.23	20.57	17.68
SM/S4	(7)	26.05	26.05	19.68	16.52
XTR100AM		38.00	38.00	35.65	28.95
AP		30.00	30.00	27.80	23.85
BM		46.00	46.00	43.35	35.95
BP		36.00	36.00	33.95	29.25
XTR101AG		11.75	11.75	9.75	8.25
BG		17.35	17.35	14.45	12.25
XTR110AD				7.45	4.95
AG		10.85	10.85	8.75	7.45
BG		16.25	16.25	13.10	11.10
KP		7.45	7.45	5.95	4.95

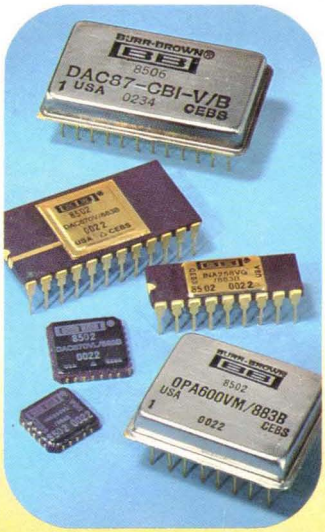
(7) BS9400-G0104

‡ As of March 1, 1985, Military Products will no longer offer the /MIL for new customers/applications. Instead the /883B is to be utilized. MIL-STD-883C now mandates the same processing for /883 products as what we offered with the /MIL. All inquiries for /MIL are to be referred to Military Products Marketing. The /MIL will continue to be offered for applications where the /MIL is already specified on customer drawings.

† Qualification reports $100 each.

Prices subject to change without notice. Minimum order $75.

 MKT-153 Printed in U.S.A. May, 1986


BURR-BROWN®
8506
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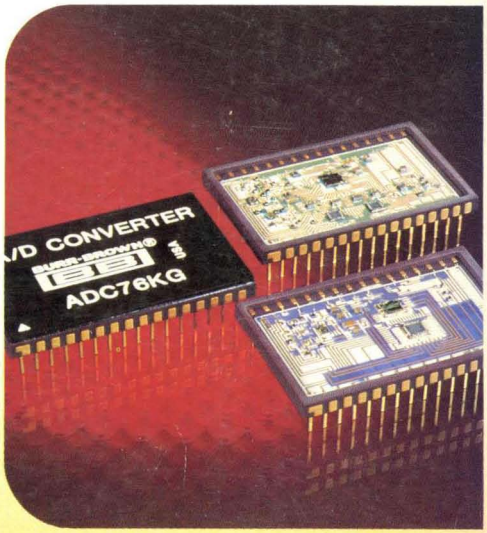
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