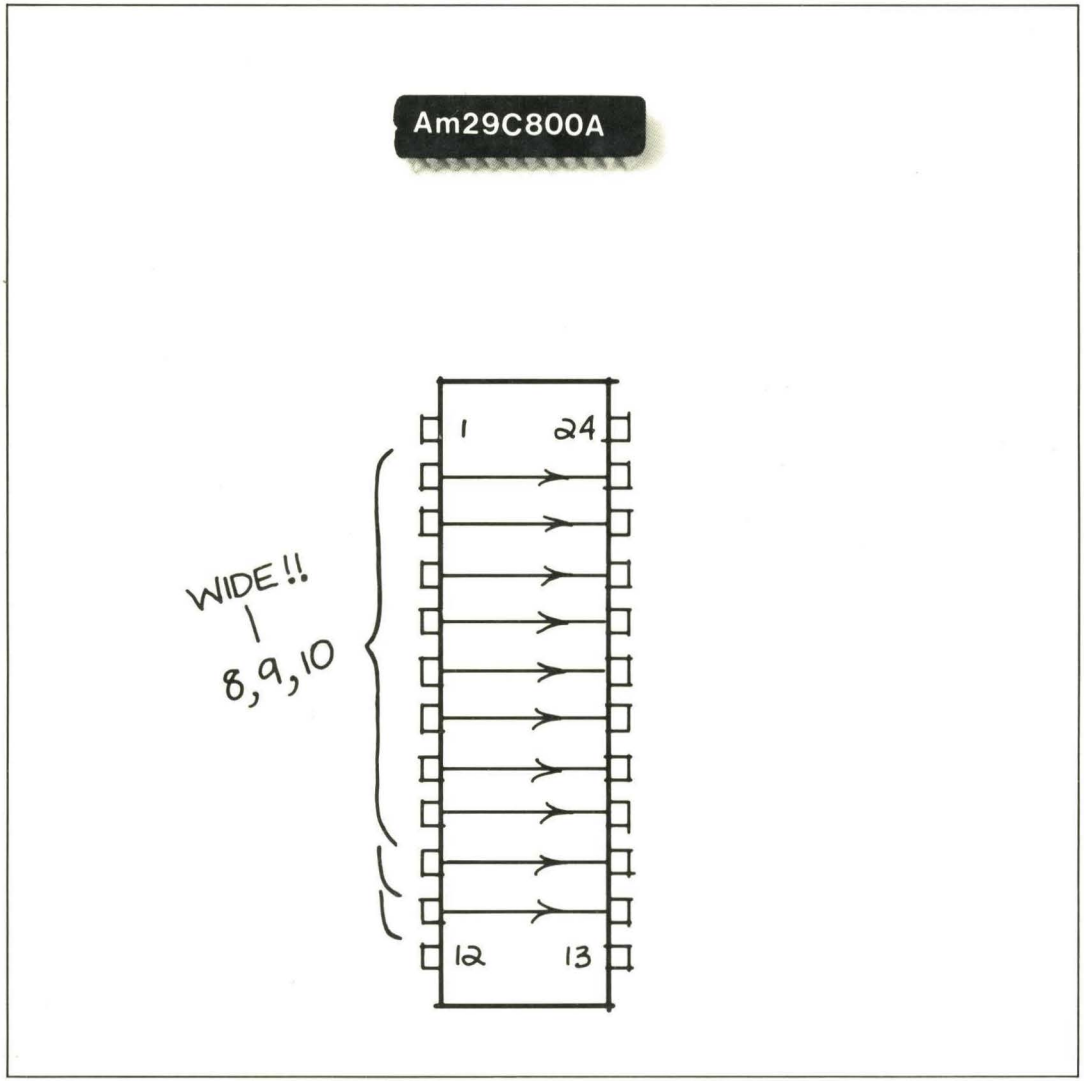
High Performance CMOS Bus Interface Products

1989 Data Book

Advanced Micro Devices



"Increasing integration and performance on the system level now requires corresponding improvements in bus interface. AMD's Am29C800A family meets this challenge, offering the designer innovative solutions to his interface needs. We are confident that you will find these devices suitable for your most demanding applications."

Fred J. Roeder
Vice-President and Managing Director
Logic Products Division

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Numerical Device Index

Introduction

This document contains preliminary product specifications for the Am29C800A High-Performance Bus interface devices. This newest Am29800 Family provides wide data-path solutions in a variety of functions for use in various system applications.

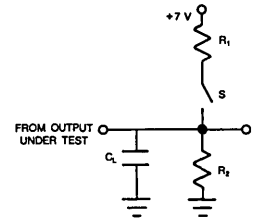
The Am29C800A High-Performance CMOS Bus Interface Family provides bipolar-comparable performance while consuming much less power. Pin-for-pin compatible with the Am29800A/Am29C800 Families, the Am29C800A Family provides the same functionality and features with 48-mA output drive. The Am29C800A devices offer lower propagation delays and consume less power than their predecessors. Built with AMD's advanced CS-11SA 1.0 micron process, you obtain the necessary output drive for driving heavily loaded buses while achieving the fast switching speeds required for high-performance systems.

The family is available in a variety of packages, including 24-Pin Slim (300-mil) Ceramic and Plastic DIPs, a 28-Pin Ceramic Leadless Chip Carrier (LCC), and a 28-Pin Plastic Leaded Chip Carrier (PLCC). Physical Dimensions for these packages, as well as a common Switching Test Circuit, with associated waveforms, are provided on the following pages.

For further information, please contact the nearest AMD Sales Office or Representative listed on the back cover.

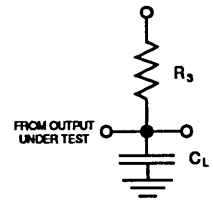
SWITCHING TEST CIRCUITS

THREE-STATE OUTPUTS



TC002682

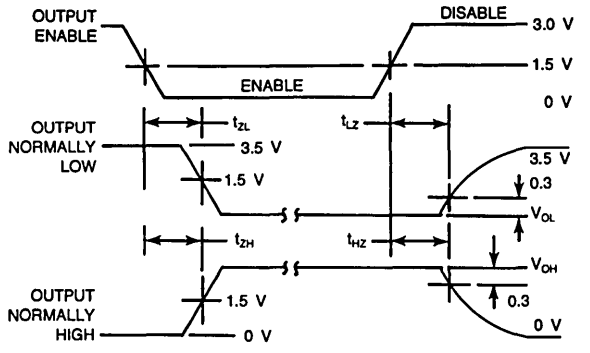
OPEN-DRAIN OUTPUTS



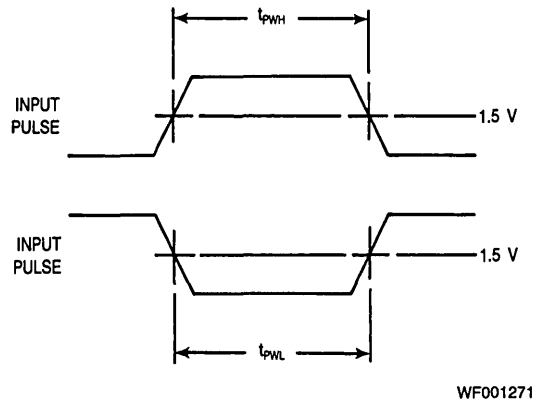
SWITCH POSITIONS FOR PARAMETER TESTING

Parameter	S Position
t_{PLH}	OPEN
t_{PHL}	OPEN
t_{HZ}	OPEN
t_{ZH}	OPEN
t_{LZ}	CLOSED
t_{ZL}	CLOSED

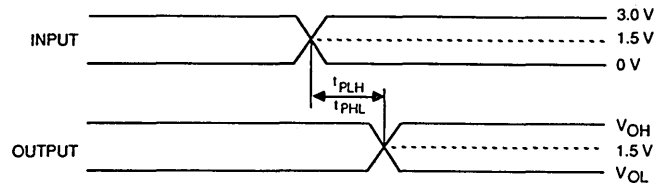
SWITCHING TEST WAVEFORMS



Enable and Disable Times



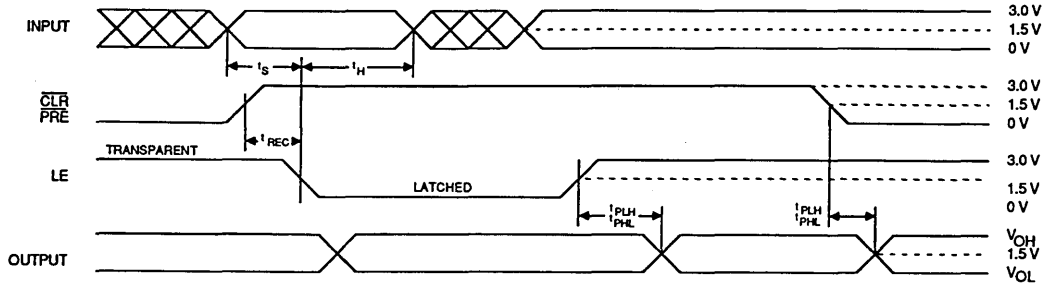
Pulse Width



WF024420

Propagation Delay for Buffers, Transceivers, and Latches in the Transparent Mode

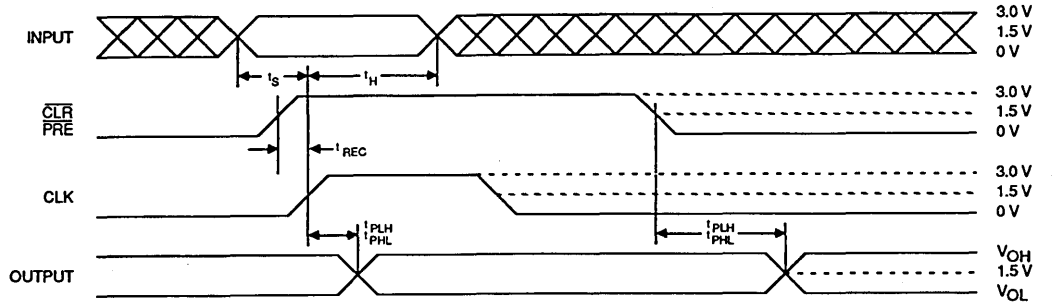
Am29C841A, Am29C843A, Am29C833A, Am29C853A, Am29C855A



WF024440

Switching Parameters for Circuits with Latches

Am29C841A, Am29C843A, Am29C853A, Am29C855A



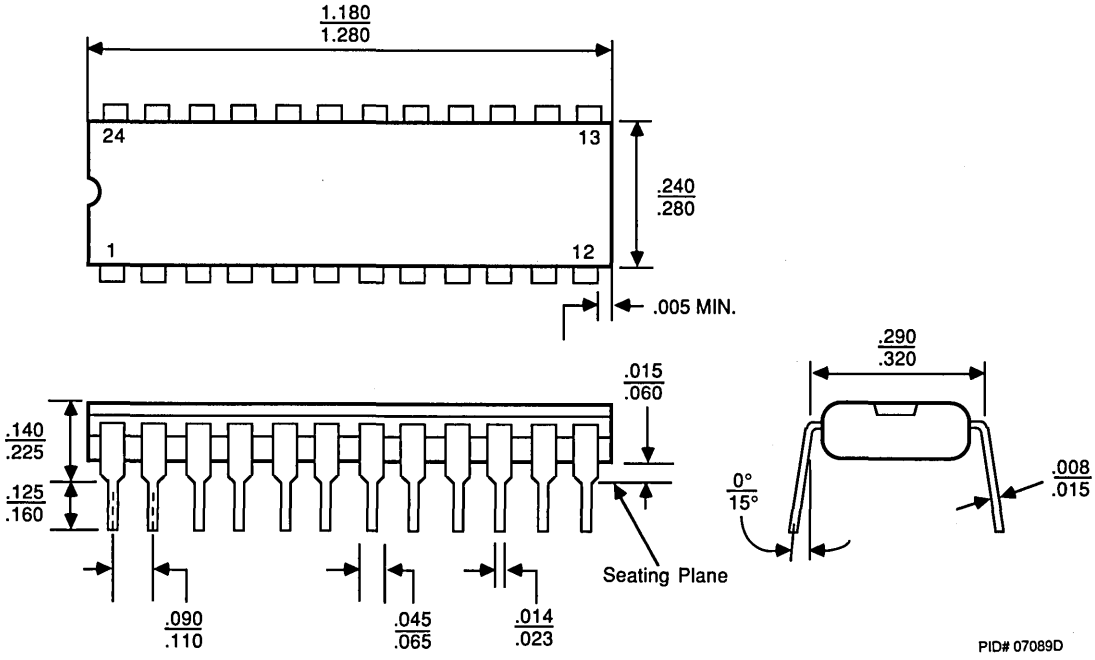
WF024430

Switching Parameters for Circuits with Registers

Am29C821A, Am29C823A, Am29C833A

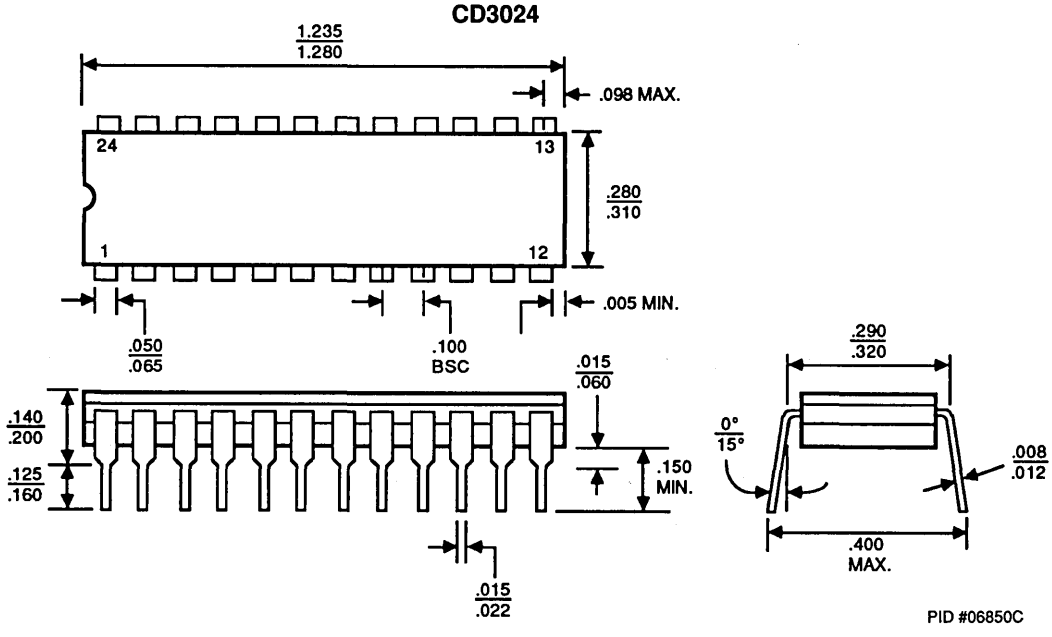
PHYSICAL DIMENSIONS*

PD3024



PID# 07089D

CD3024

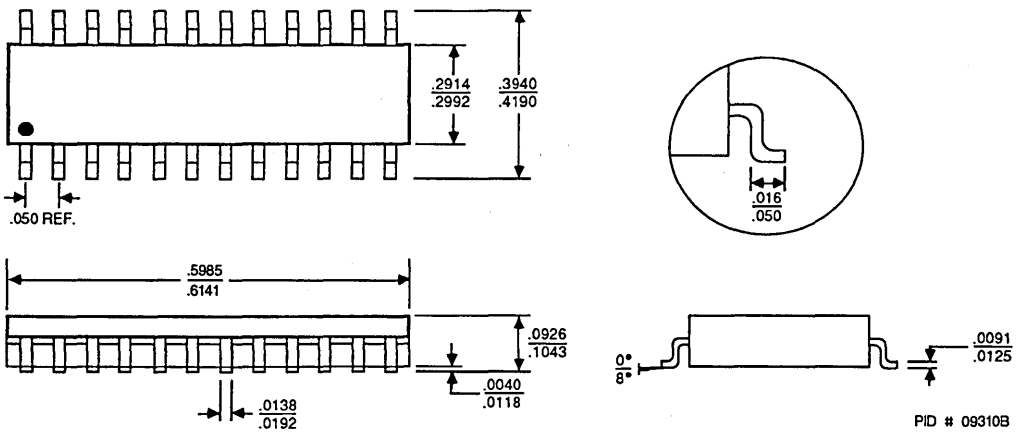


PID #06850C

*For reference only. All dimensions are measured in inches.
BSC is an ANSI standard for Basic Space Centering.

PHYSICAL DIMENSIONS (cont'd)

SO 024



PID # 09310B

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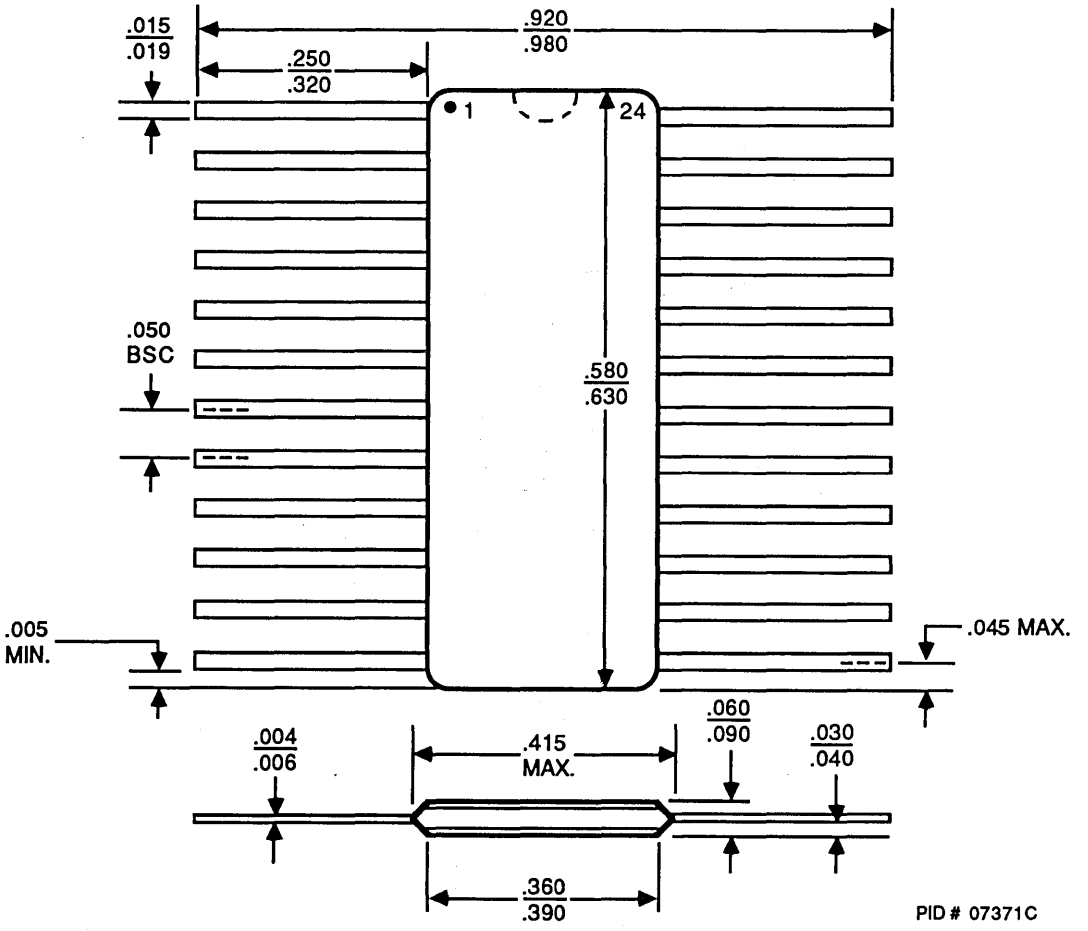
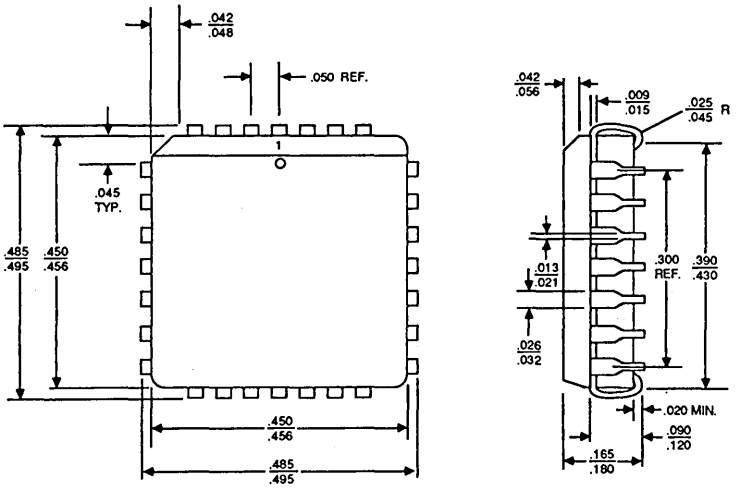


PID # 07371C

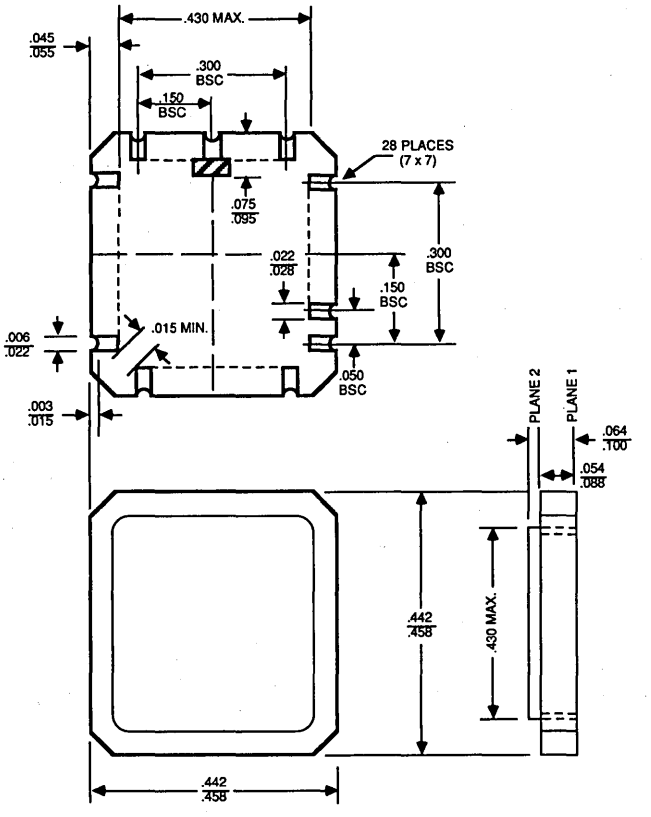
PHYSICAL DIMENSIONS (cont'd)

PL 028



PID # 06751E

CL 028



PID #06595F

Am29C821A/Am29C823A

High-Performance CMOS Bus Interface Registers

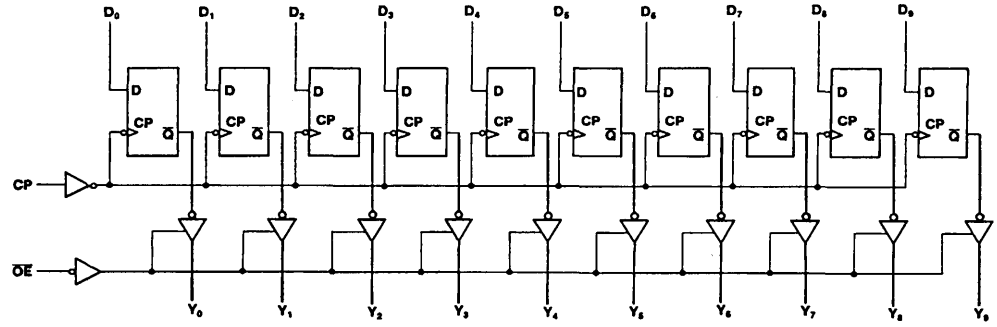
PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High-speed parallel positive edge-triggered registers with D-type flip-flops
  - CP-Y propagation delay = 5 ns typical
- Low standby power
- JEDEC FCT-compatible specs
- Very high output drive
  - I_{OL} = 48 mA Commercial, 32 mA Military
- Extra-wide (9- and 10-bit) data paths
- Proprietary edge-rate controlled outputs
- Power-up/down disable circuit provides for glitch-free power supply sequencing

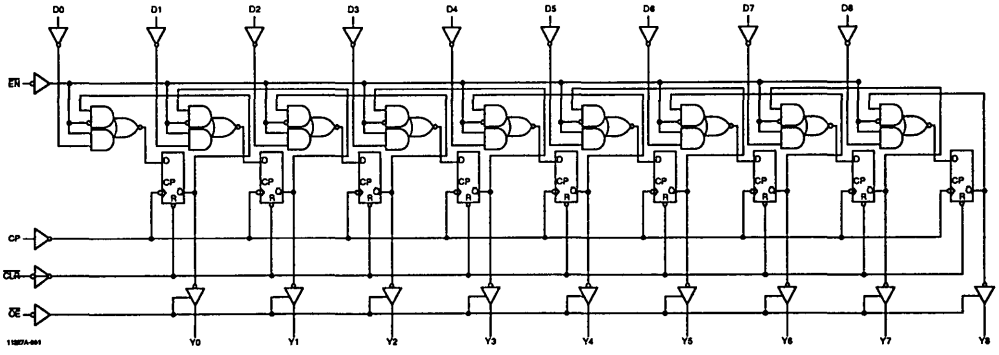
BLOCK DIAGRAMS

Am29C821A



BD005471

Am29C823A



LS003330

Publication # 11227 | Rev. A | Amendment /0
Issue Date: November 1988

GENERAL DESCRIPTION

The Am29C821A and Am29C823A CMOS Bus Interface Registers are designed to eliminate the extra devices required to buffer stand alone registers and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800A registers are produced with AMD's exclusive CS11SA CMOS process, and feature typical propagation delays of 5 ns, as well as an output current drive of 48 mA.

The Am29C821A is a buffered, 10-bit version of the popular '374/'534 function. The Am29C823A is a 9-bit buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems.

The Am29C821A and Am29C823A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce). By controlling the output transient currents, ground bounce and ouput ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry provices for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

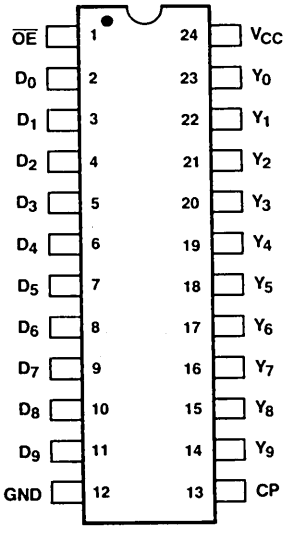
The Am29C821A and Am29C823A are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks.

*For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (PID #10181A).

CONNECTION DIAGRAMS
Top View

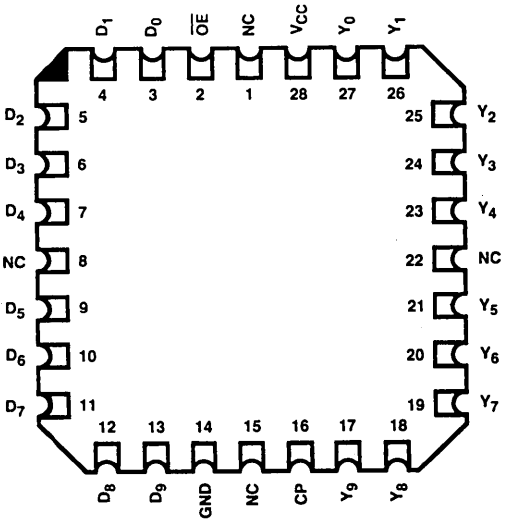
Am29C821A

DIPs*



CD001360

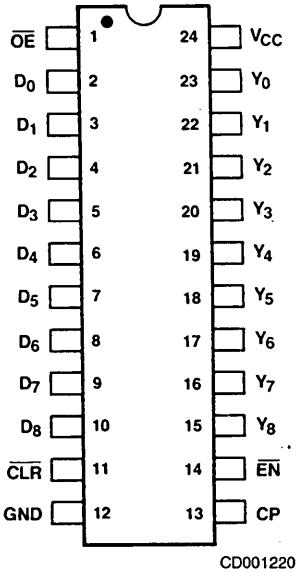
LCC**



CD001370

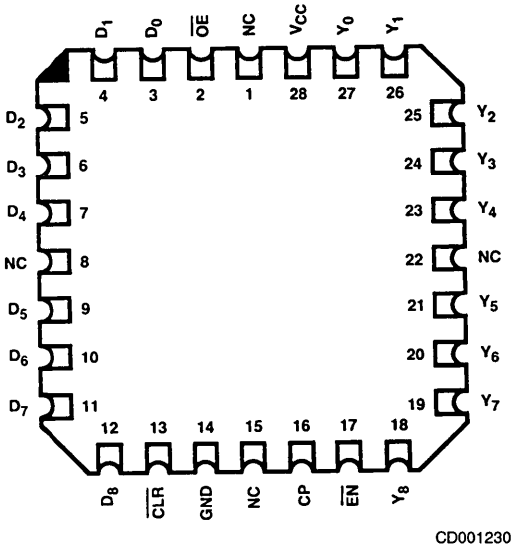
Am29C823A

DIPs*



CD001220

LCC**

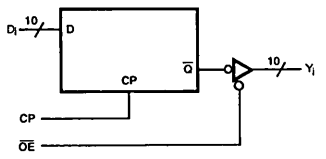


CD001230

* Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

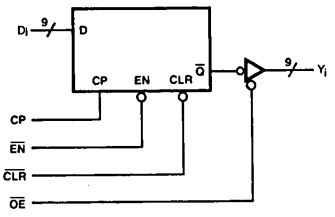
LOGIC SYMBOLS

Am29C821A



LS000452

Am29C823A



LS000432

FUNCTION TABLES

Am29C821A

Inputs			Internal	Outputs	
$\overline{OE}$	D_I	CP	$\overline{Q_I}$	Y_I	Function
H	L	↑	H	Z	Hi-Z
H	H	↑	L	Z	
L	L	↑	H	L	Load
L	H	↑	L	H	

Am29C823A

Inputs					Internal	Outputs	
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	$\overline{Q_I}$	Y_I	Function
H	H	L	L	↑	H	Z	Hi-Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	L	
L	H	L	H	↑	L	H	

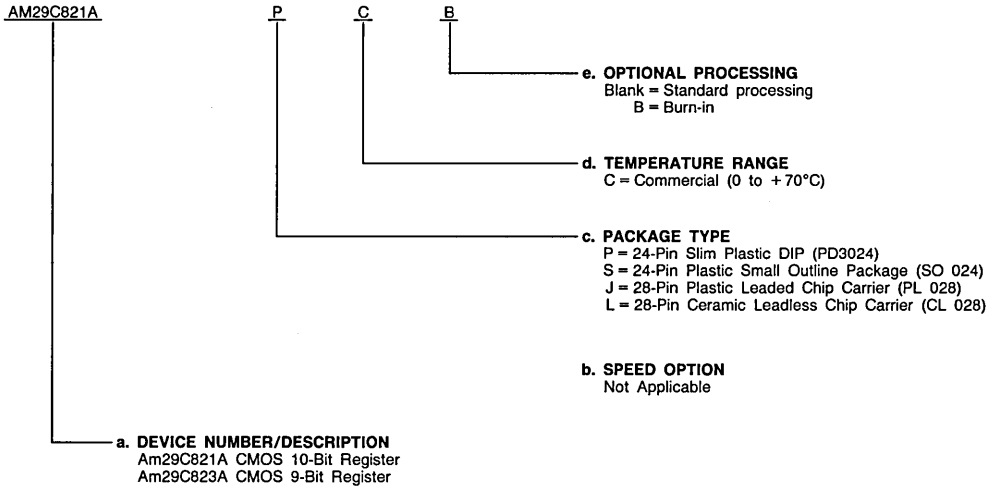
H = HIGH
L = LOW
X = Don't Care

NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C821A	PC, PCB, SC, JC, LC
AM29C823A	

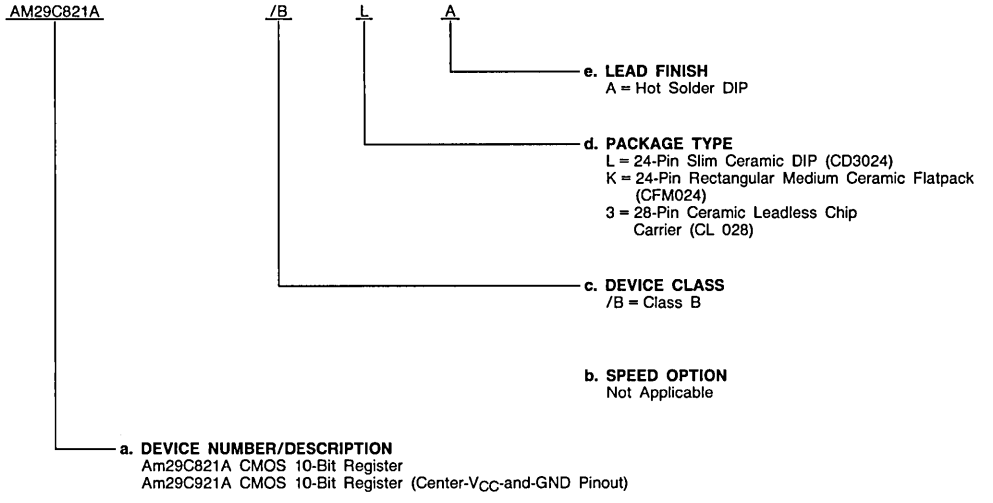
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C821A	/BLA, /BKA, /B3A
AM29C823A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C821A/Am29C823A

D_i Data Input (Input)
D_i are the register data inputs.

CP Clock Pulse (Input, LOW-to-HIGH Transition)
Clock Pulse is the clock input for the registers. Data is entered into the registers on the LOW-to-HIGH transitions.

Y_i Data Outputs (Output)
Y_i are the three-state outputs.

$\overline{OE}$ Output Enable (Input, Active LOW)
When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, the register data is present at the Y_i outputs.

Am29C823A only:

$\overline{EN}$ Clock Enable (Input, Active LOW)
When $\overline{EN}$ is LOW, data on the D_i inputs are transferred to the $\overline{Q}_i$ outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the $\overline{Q}_i$ outputs do not change state, regardless of the data or clock input transitions.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal register is cleared. When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the $\overline{Q}_i$ outputs are HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to −6 V
DC Output Voltage ..... −0.5 V to −6 V
DC Input Voltage ..... −0.5 V to −6 V
DC Output Diode Current: Into Output ..... +50 mA
Out of Output ..... −50 mA
DC Input Diode Current: Into Input ..... +20 mA
Out of Input ..... −20 mA
DC Output Current per Pin: I_{Sink} ..... +70 mA
I_{Source} ..... −30 mA
Total DC Ground Current .$(n \times I_{OL} + m \times I_{CCT})$ mA (Note 1)
Total DC V_{CC} Current .... $(n \times I_{OH} + m \times I_{CCT})$ mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) Devices
Ambient Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, $V_{IN} = V_{IH}$ or V_{IL}	MIL I_{OL} = 32 mA			0.5	Volts
			COM'L I_{OL} = 48 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−10	μA
		V_{CC} = 5.5 V, V_{IN} = 0.4 V				−5	μA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				5	μA
		V_{CC} = 5.5 V, V_{IN} = 5.5 V				10	μA
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V or 2.7 V (Note 3)				+10	μA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V or GND (Note 3)				−10	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 4)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V, Outputs Open	$V_{IN} = V_{CC}$ or GND	MIL		1.5	mA
				COM'L		1.2	mA
I_{CCT}*			V_{IN} = 3.4 V	Data Input		1.5	mA/Bit
				$\overline{OE}$, $\overline{CLR}$, CP, $\overline{EN}$		3.0	mA/Bit
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 5)				275	μA/MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Off-state currents are only tested at worst-case conditions of V_{OUT} = 5.5 V or 0.0 V.
4. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
5. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITHCING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	COMMERCIAL		MILITARY		Units
				Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW) (Note 1)		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		8.5		9.5	ns
t_{PHL}					8.5		9.5	ns
t_S	Data to CP Setup Time			3		3		ns
t_H	Data to CP Hold Time			1.5		1.5		ns
t_S	Enable ($\overline{EN}$ ⎍) to CP Setup Time			3		3		ns
t_S	Enable ($\overline{EN}$ ⎍) to CP Setup Time			3		3		ns
t_H	Enable ($\overline{EN}$) Hold Time			0		0		ns
t_{PHL}	Propagation Delay, Clear to Y_i				10		10.5	ns
t_{REC}	Clear ($\overline{CLR}$ ⎍) to CP Setup Time			6		6		ns
t_{PWH}	Clock Pulse Width	HIGH		6		6		ns
t_{PWL}		LOW		6		6		ns
t_{PWL}	Clear Pulse Width	LOW		6		6		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⎍ to Y_i				8.5		9	ns
t_{ZL}					8.5		9	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⎍ to Y_i				7.5		8	ns
t_{LZ}					7.5		8	ns

*See Test Circuit and Waveforms.

Notes: 1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (PID #10181A).

Am29C827A/Am29C828A

High-Performance CMOS Bus Buffers

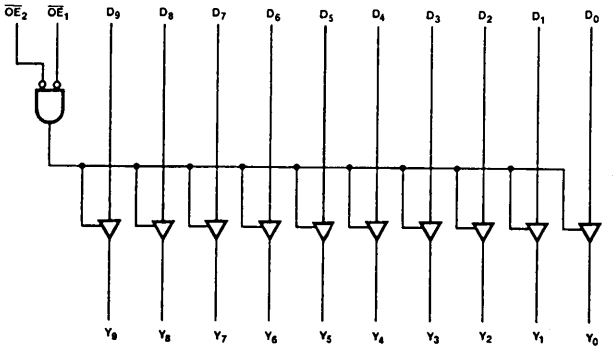
PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High-speed CMOS buffers and inverters
  - D-Y delay = 4 ns typical
- Low standby power
- JEDEC FCT-compatible specs
- Very high output drive
  - I_{OL} = 48 mA Commercial, 32 mA Military
- 200-mV typical hysteresis on data input ports
- Proprietary edge-rate controlled outputs
- Power-up/down disable circuit provides for glitch-free power supply sequencing

BLOCK DIAGRAMS

Am29C827A (Noninverting)



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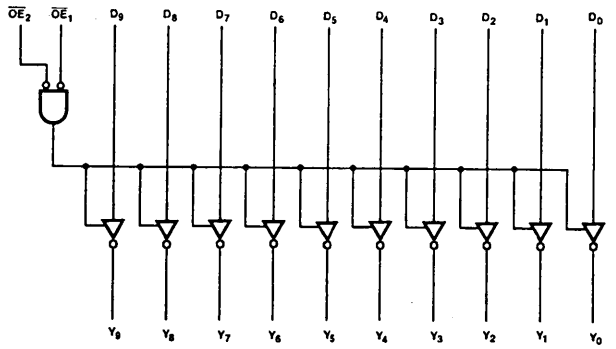
Am29C828A (Inverting)



BD001093

Publication # 11228 | Rev. A | Amendment /0
Issue Date: November 1988

GENERAL DESCRIPTION

The Am29C827A and Am29C828A CMOS Bus Buffers provide high-performance bus interface buffering for wide address/data paths or buses carrying parity. Both devices feature 10-bit wide data paths and NORed output enables for maximum control flexibility. The Am29C827A has non-inverting outputs, while the Am29C828A has inverting outputs. Each device has data inputs with 200-mV typical input hysteresis to provide improved noise immunity. The Am29C827A and Am29C828A are produced with AMD's exclusive CS11SA CMOS process, and feature typical propagation delays of 4 ns, as well as an output current drive of 48 mA.

The Am29C827A and Am29C828A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce). By controlling the output transient currents, ground bounce and ouput ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits or edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry provides for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

The Am29C827A and Am29C828A are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks.

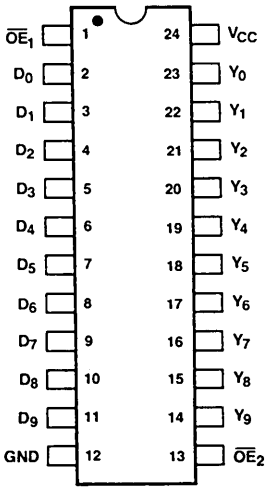
*For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (PID #10181A)

CONNECTION DIAGRAMS

Top View

Am29C827A/Am29C828A

DIPs*



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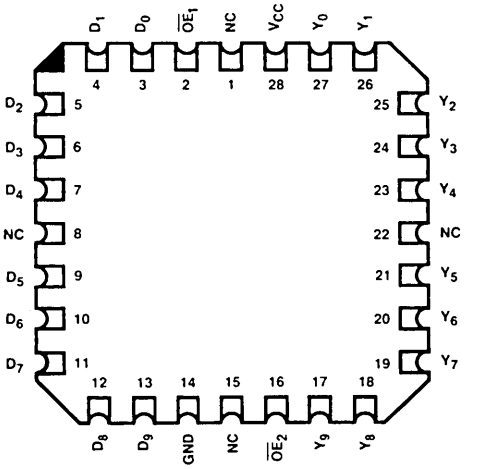
LCC**



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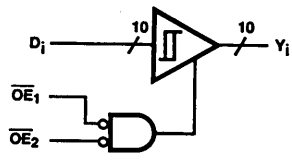
*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

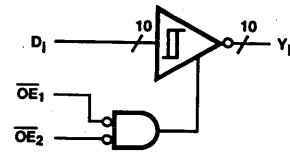
LOGIC SYMBOLS

Am29C827A



LS000391

Am29C828A



LS000393

FUNCTION TABLES

Am29C827A

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	Function
L	L	H	H	Transparent
L	L	L	L	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

Am29C828A

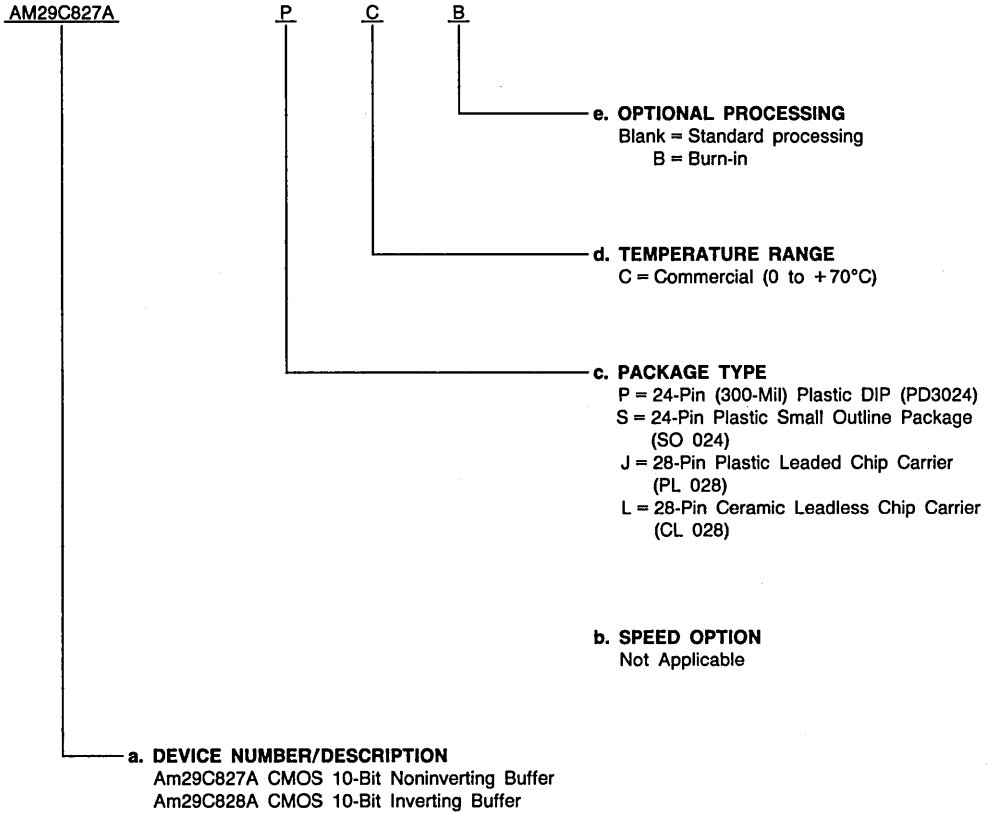
Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	Function
L	L	H	L	Transparent
L	L	L	H	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

H = HIGH
L = LOW
X = Don't Care
Z = Hi-Z

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C827A	PC, PCB, SC, JC, LC
AM29C828A	

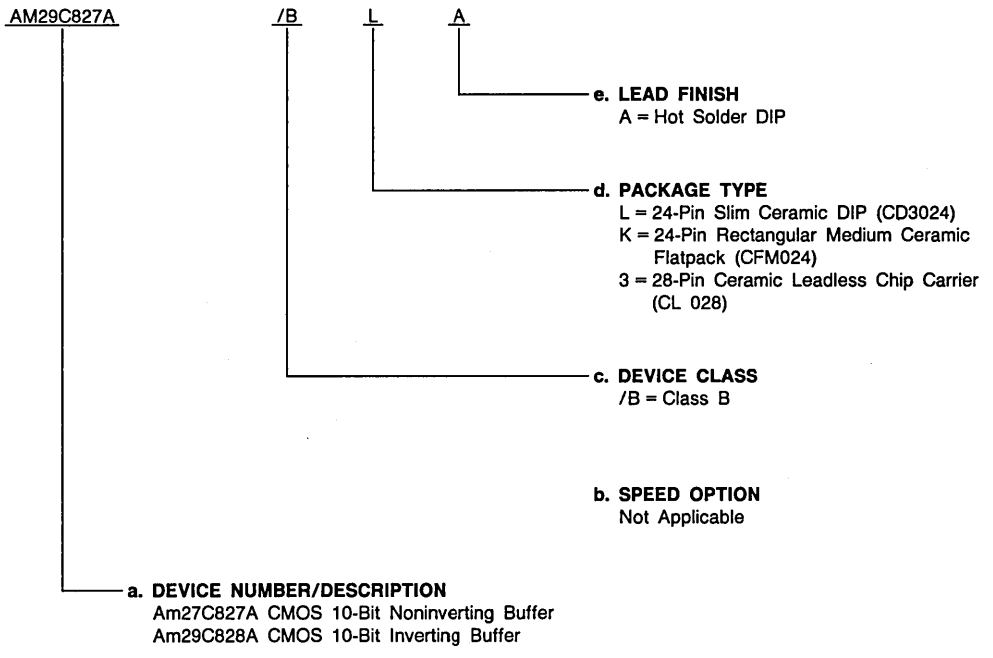
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C827A	/BLA, /BKA, /B3A
AM29C828A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$\overline{OE}_i$ Output Enables (Input, Active LOW)
When $\overline{OE}_1$ and $\overline{OE}_2$ are both LOW, the outputs are enabled. When either one or both are HIGH, the outputs are in the Hi-Z state.

D_i Data Inputs (Input)
D_i are the 10-bit data inputs.

Y_i Data Output (Output)
Y_i are the 10-bit data outputs.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +6.0 V
DC Output Voltage ..... −0.5 V to +6.0 V
DC Input Voltage ..... −0.5 V to +6.0 V
DC Output Diode Current: Into Output ..... +50 mA
Out of Output ..... −50 mA
DC Input Diode Current: Into Input ..... +20 mA
Out of Input ..... −20 mA
DC Output Current per Pin:
I_{SINK} ..... +70 mA
I_{SOURCE} ..... −30 mA
Total DC Ground Current .$(n \times I_{OL} + m \times I_{CCT})$ mA (Note 1)
Total DC V_{CC} Current .... $(n \times I_{OH} + m \times I_{CCT})$ mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) Devices
Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	MIL I_{OL} = 32 mA			0.5	V
			COM'L I_{OL} = 48 mA				
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−10	μA
		V_{CC} = 5.5 V, V_{IN} = 0.4 V				−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				5	μA
		V_{CC} = 5.5 V, V_{IN} = 5.5 V				10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V or 2.7 V (Note 3)				+10	μA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V or GND (Note 3)				−10	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 4)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V, Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	mA
				COM'L		1.2	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/Bit
				$\overline{OE}_1$, $\overline{OE}_2$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 5)				275	μA/MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Off-state currents are only tested at worst-case conditions of V_{OUT} = 5.5 V or 0.0 V.
4. Not more than one output should be shorted at a time. Duration should not exceed 100 milliseconds.
5. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions*	COMMERCIAL		MILITARY		Units
			Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output (Y_i) Am29C827A (Noninverting) (Note 1)	C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		6.5		7.5	ns
t_{PHL}				6.5		7.5	ns
t_{PLH}	Data (D_i) to Output (Y_i) Am29C828A (Inverting) (Note 1)			6.5		7.5	ns
t_{PHL}				6.5		7.5	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i			9		10	ns
t_{ZL}				9		10	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i			8		9	ns
t_{LZ}				8		9	ns

*See Test Circuit and Waveforms.

Notes: 1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (PID #10181A).

Am29C833A/Am29C853A/Am29C855A

High-Performance CMOS Parity Bus Transceivers

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High-speed CMOS bidirectional bus transceivers
  - T-R delay = 5 ns typical
  - R-Parity delay = 8 ns typical
- Error flag with open-drain output
- Generates odd parity for all-zero protection
- Low standby power
- Am29C855A adds new functionality
- 200-mV typical input hysteresis on input data ports
- Very high output drive
  - I_{OL} = 48 mA Commercial, 32 mA Military
- JEDEC FCT-compatible specs
- Proprietary edge-rate controlled outputs
- Power-up/down disable circuit provides for glitch-free power supply sequencing

GENERAL DESCRIPTION

The Am29C833A, Am29C853A, and Am29C855A are high-performance CMOS parity bus transceivers designed for two-way communications. Each device can be used as an 8-bit transceiver, as well as a 9-bit parity checker/generator. In the transmit mode, data is read at the R port and output at the T port with a parity bit. In the receive mode, data and parity are read at the T port, and the data is output at the R port along with the $\overline{ERR}$ flag showing the results of the parity test. Each of these devices is produced with AMD's exclusive CS11SA CMOS process, and features a typical propagation delay of 5 ns, as well as an output current drive of 48 mA.

In the Am29C833A, the error flag is clocked and stored in a register which is read at the open-drain $\overline{ERR}$ output. The $\overline{CLR}$ input is used to clear the error flag register. In the Am29C853A, a latch replaces this register, and the $\overline{EN}$ and $\overline{CLR}$ controls are used to pass, store, sample or clear the error flag output. When both output enables are disabled in the Am29C853A and Am29C833A, parity logic defaults to the transmit mode, so that the $\overline{ERR}$ pin reflects the parity of the R port. The Am29C855A, a variation of the Am29C853A, is designed so that when both output enables are HIGH, the $\overline{ERR}$ pin retains its current state.

The output enables, $\overline{OER}$ and $\overline{OET}$, are used to force the port outputs to the high-impedance state so that other devices can drive bus lines directly. In addition, the user can force a parity error by enabling both $\overline{OER}$ and $\overline{OET}$ simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability.

The Am29C833A, Am29C853A, and Am29C855A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce). By controlling the output transient currents, ground bounce and ouput ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

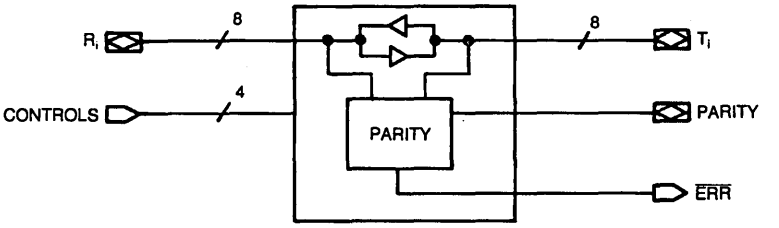
Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry provices for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

The Am29C833A, Am29C853A, and Am29C855A are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks.

*For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (PID #10181A).

SIMPLIFIED BLOCK DIAGRAM

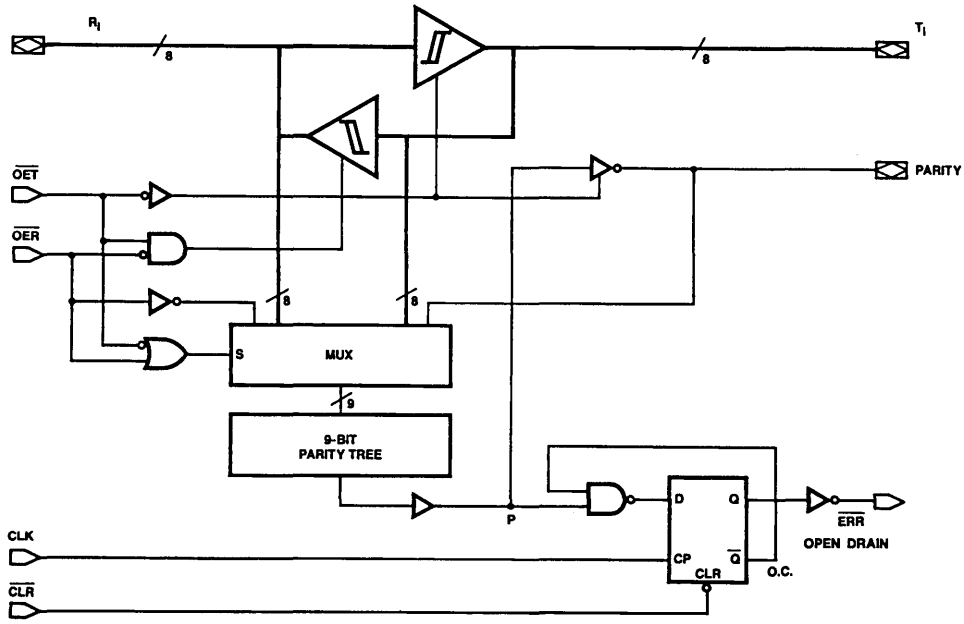


BD005541

Publication # 11229 Rev. A Amendment /0
Issue Date: November 1988

BLOCK DIAGRAMS

Am29C833A



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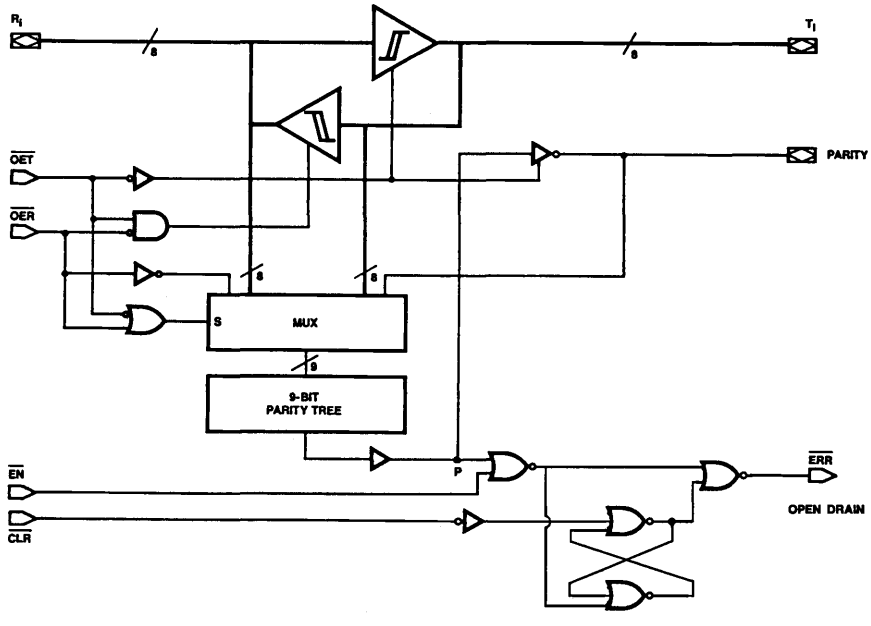
Am29C853A



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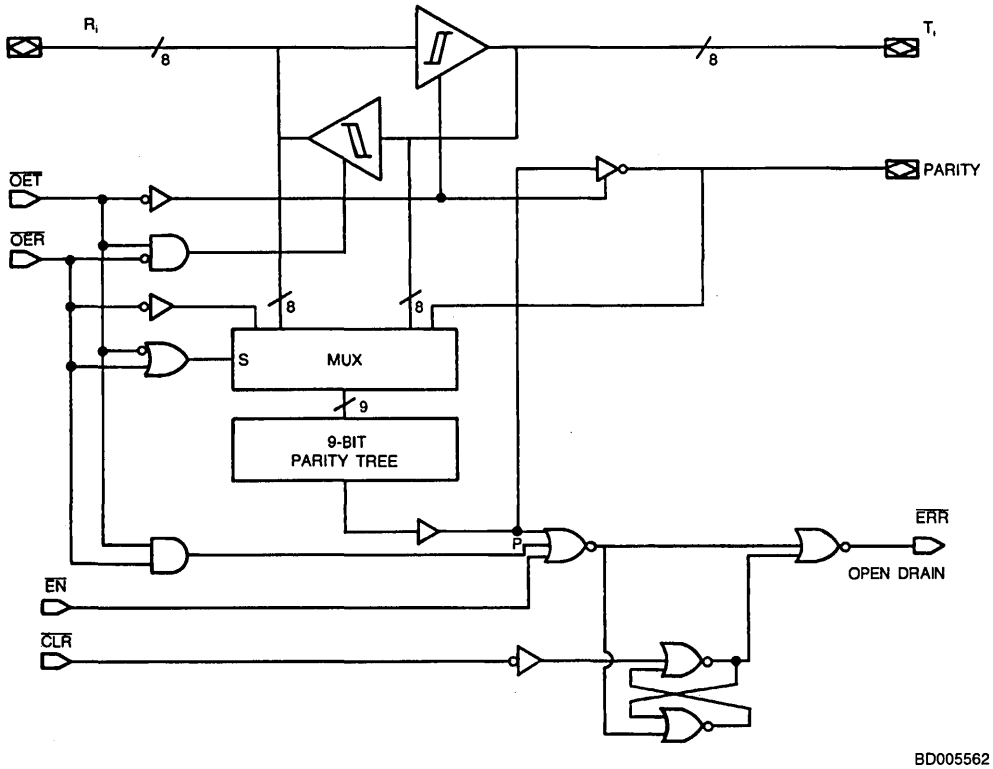
BLOCK DIAGRAMS (Cont'd.)

Am29C855A



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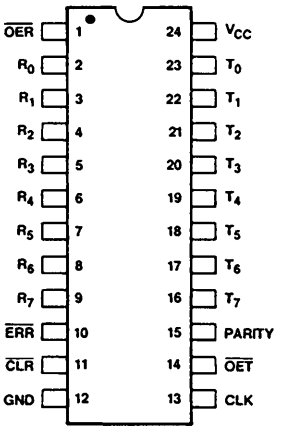
CONNECTION DIAGRAMS
Top View

Am29C833A

DIPs*



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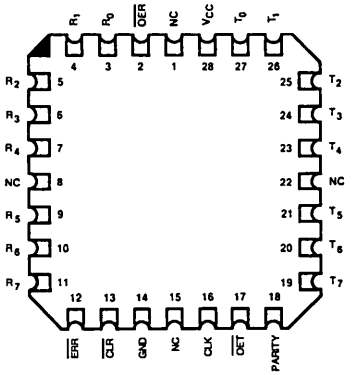
LCC**



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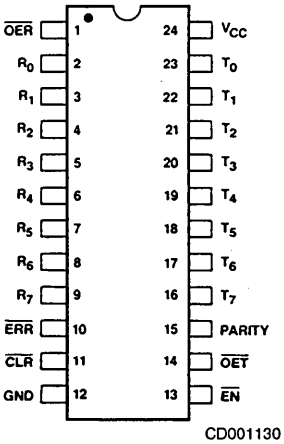
Am29C853A/Am29C855A

DIPs*



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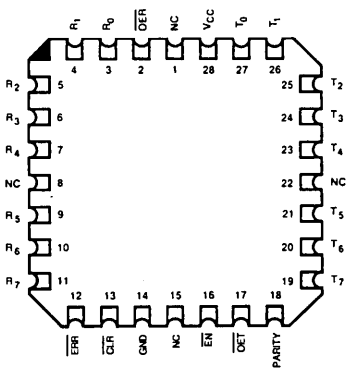

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*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

FUNCTION TABLES

Am29C833A (Register Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	H	↑	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	H	↑	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	↑	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	↑	NA	NA	L	EVEN	L	NA	NA	L	
X	X	L	X	X	X	X	X	X	X	X	H	Clear error flag register.
H	H	H	X	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	X	X	X	X	X	Z	Z	Z	H	
H	H	H	↑	L	ODD	X	X	Z	Z	Z	H	
H	H	H	↑	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition of Clock
X = Don't Care or Irrelevant
Z = High Impedance
NA = Not Applicable
* = Store the State of the Last Receive Cycle
ODD = Odd Number
EVEN = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLE

Error Flag Output

Am29C833A

Inputs		Internal to Device	Outputs Pre-state	Output	
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	Sample (1's Capture)
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

Note: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

FUNCTION TABLES (Cont'd.)

Am29C853A (Latch Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
H	H	X	L	L	ODD	X	X	Z	Z	Z	H	
H	H	X	L	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

Am29C855A (Latch Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of L's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	*	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	*	
L	H	X	X	L	ODD	NA	NA	NA	L	L	*	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	*	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	*	Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	*	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
L	L	X	X	H	ODD	NA	NA	NA	H	H	*	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	*	
L	L	X	X	L	ODD	NA	NA	NA	L	H	*	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	*	

H = HIGH
L = LOW
X = Don't Care or Irrelevant

Z = High Impedance
NA = Not Applicable
* = Store the State of the Last Receive Cycle

ODD = Odd Number
EVEN = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLE
Error Flag Output

Am29C853A/Am29C855A

Inputs		Internal to Device	Outputs Pre-state	Output	
$\overline{EN}$	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
L	L	L	X	L	Pass
L	L	H	X	H	
L	H	L	X	L	Sample
L	H	X	L	L	(1's
L	H	H	H	H	Capture)
H	L	X	X	H	Clear
H	H	X	L	L	Store
H	H	X	H	H	

Note: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29C833A P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 24-Pin (300-Mil) Plastic DIP (PD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C833A CMOS Parity Bus Transceiver — Register Option
Am29C853A CMOS Parity Bus Transceiver — Latch Option
Am29C855A CMOS Parity Bus Transceiver — Latch Option

Valid Combinations	
AM29C833A	PC, PCB, SC, JC, LC
AM29C853A	
AM29C855A	

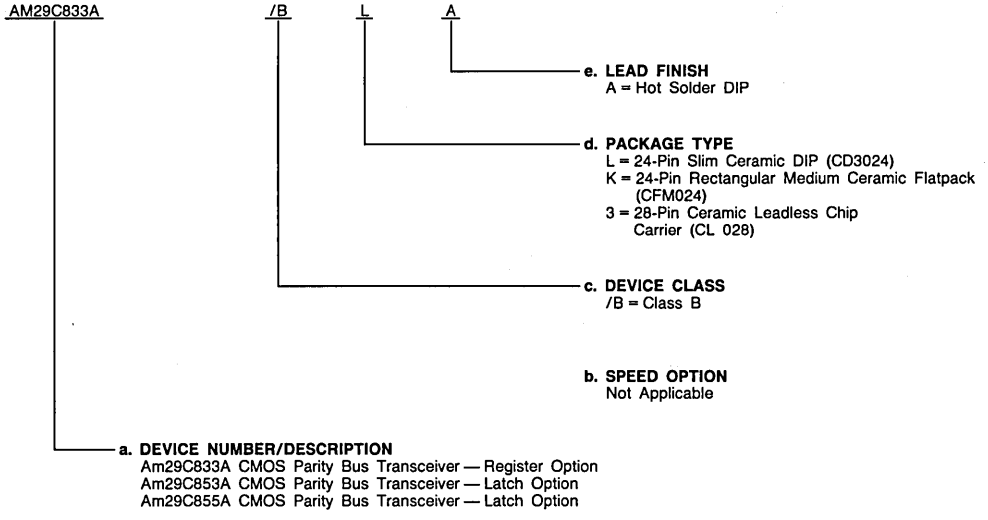
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C833A	/BLA, /BKA, /B3A
AM29C853A	
AM29C855A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C833A/Am29C853A/Am29C855A

$\overline{OER}$ Output Enable-Receive (Input, Active LOW)
When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i and Parity are inputs).

$\overline{OET}$ Output Enable-Transmit (Input, Active LOW)
When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i and Parity are outputs).

R_i Receive Port (Input/Output, Three-State)
R_i are the 8-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i Transmit Port (Input/Output, Three-State)
T_i are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Parity Parity Flag (Input/Output, Three-State)
In the Transmit mode, the Parity signal is an active output used to generate odd parity. In the Receive mode, the T_i and Parity inputs are combined and checked for odd parity. When both output enables are HIGH, the Parity Flag is in the high impedance state. When both output enables are LOW, the Parity bit forces a parity error.

Am29C833A Only

$\overline{ERR}$ Error Flag (Output, Open Drain)
In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{ERR}$ goes LOW when the comparison indicates a parity error. $\overline{ERR}$ stays LOW until the register is cleared.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ goes LOW, the Error Flag Register is cleared ($\overline{ERR}$ goes HIGH).

CLK Clock (Input, Positive Edge-Triggered)
This pin is the clock input for the Error Flag register.

Am29C853A/Am29C855A Only

$\overline{ERR}$ Error Flag (Output, Open Drain)
In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{ERR}$ goes LOW when the comparison indicates a parity error. $\overline{ERR}$ stays LOW until the latch is cleared. In the Am29C855A, the error flag will retain its previous state when $\overline{OET}$ and $\overline{OER}$ are HIGH.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ goes LOW and $\overline{EN}$ is HIGH, the Error Flag latch is cleared ($\overline{ERR}$ goes HIGH).

$\overline{EN}$ Latch Enable (Input, Active LOW)
This pin is the latch enable for the Error Flag latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +6 V
DC Output Voltage ..... −0.5 V +6 V
DC Input Voltage ..... −0.5 V +6 V
DC Output Diode Current: Into Output ..... +50 mA
Out of Output ..... −50 mA
DC Input Diode Current: Into Input ..... +20 mA
Out of Input ..... −20 mA
DC Output Current per Pin: I_{SINK} ..... +70 mA
I_{SOURCE} ..... −30 mA
Total DC Ground Current .$(n \times I_{OL} + m \times I_{CCT})$ mA (Note 1)
Total DC V_{CC} Current .... $(n \times I_{OH} + m \times I_{CCT})$ mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage ..... +4.5 V to +5.5 V

Military (M) Devices
Temperature (T_A) ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	MIL I_{OL} = 32 mA			0.5	Volts
			COM'L I_{OL} = 48 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage (Note 2)	Am29C853A Am29C855A	All Inputs	2		Volts
			Am29C833A				
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V	V_{IN} = 0.0 V			−10	μA
		Input Only	V_{IN} = 0.4 V			−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V	V_{IN} = 2.7 V			5	μA
		Input Only	V_{IN} = 5.5 V			10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V I/O Port	V_{OUT} = 2.7 V			15	μA
			V_{OUT} = 5.5 V			20	
I_{OZL}		V_{CC} = 5.5 V I/O Port	V_{OUT} = 0.4 V			−15	μA
			V_{OUT} = 0.0 V			−20	
I_{OFF}	Off-State Current ($\overline{ERR}$ Only)	V_{CC} = 5.5 V, V_O = 5.5 V				20	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 3)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	mA
				COM'L		1.2	
I_{CCT}			V_{IN} = 3.4 V	R_i, T_i, Parity		1.5	mA/Bit
				$\overline{CLR}$, $\overline{EN}$, $\overline{OET}$, $\overline{OER}$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 4)				275	μA/Bit/MHz

Notes: 1. n = number outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
4. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
t_{PLH}	Propagation Delay R_i to T_i, T_i to R_i (Note 3)		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω R_3 = 360 Ω		10.5		12	ns
t_{PHL}					10.5		12	ns
t_{PLH}	Propagation Delay R_i to Parity				13		12	ns
t_{PHL}					13		14.5	ns
t_{ZH}	Output Enable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i and				10.5		12	ns
t_{ZL}	Parity				10.5		12	ns
t_{HZ}	Output Disable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i and				10.5		12	ns
t_{LZ}	parity				10.5		12	ns
t_S	T_i, Parity to CLK Setup Time (Note 1)			12		14		ns
t_H	T_i, Parity to CLK Hold Time (Note 1)			0		2		ns
t_{REC}	Clear ($\overline{CLR}$ ⎍) to CLK Setup Time (Note 2)			0		2		ns
t_{PWH}	Clock Pulse Width (Note 1)	HIGH		6		9		ns
t_{PWL}		LOW		6		9		ns
t_{PWL}	Clear Pulse Width	LOW		6		9		ns
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$ (Note 1)				10		14	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$				18		21	ns
t_{PLH}	Propagation-Delay T_i, Parity to $\overline{ERR}$ (PASS Mode Only) Am29C853A/855A				19		21	ns
t_{PHL}					19		21	ns
t_{PLH}	Propagation Delay $\overline{OER}$ to Parity				13		15	ns
t_{PHL}					15		17	ns

*See test circuit and waveforms.

Notes: 1. For Am29C853A/Am29C855A, replace CLK with $\overline{EN}$.
2. Applies only to Am29C833A.
3. *For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (PID #10181A).

Am29C841A/Am29C843A

High-Performance CMOS Bus Interface Latches

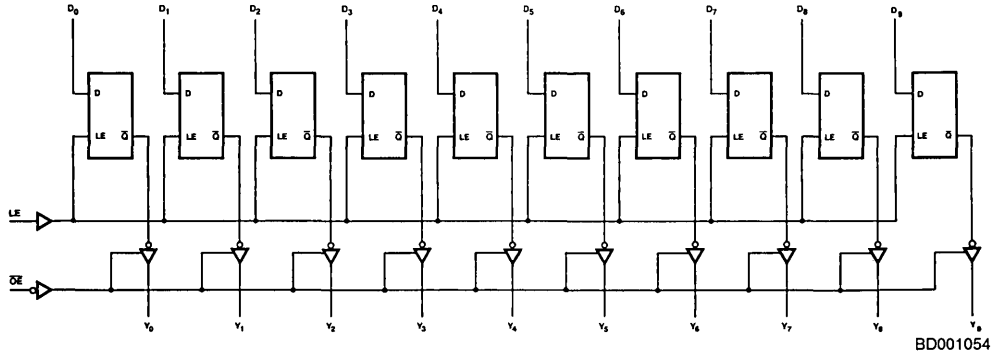
PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High-speed parallel latches
  - D-Y propagation delay = 5 ns typical
- Low standby power
- Very high output drive
  - I_{OL} = 48 mA Commercial, 32 mA Military
- JEDEC FCT-compatible specs
- Extra-wide (9- and 10-bit) data paths
- Proprietary edge-rate controlled outputs
- Power-up/down disable circuit provides for glitch-free power supply sequencing

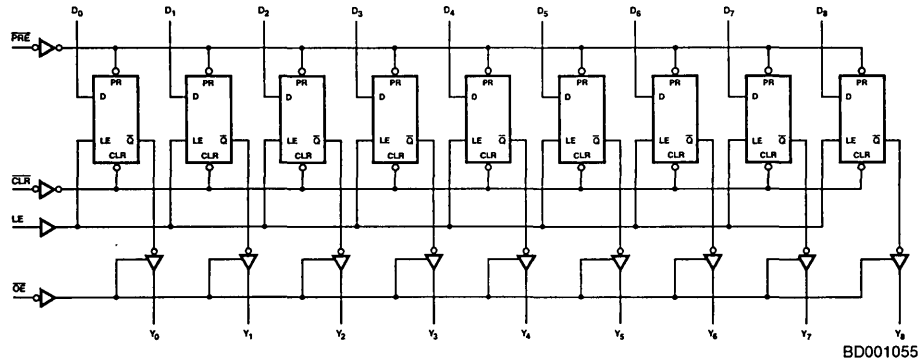
BLOCK DIAGRAMS

Am29C841A



BD001054

Am29C843A



BD001055

Publication # 11230 Rev. A Amendment /0
Issue Date: November 1988

GENERAL DESCRIPTION

The Am29C841A and Am29C843A CMOS Bus Interface Latches are designed to eliminate the extra devices required to buffer stand alone latches and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800A latches are produced with AMD's exclusive CS11SA CMOS process, and feature typical propagation delays of 5 ns, as well as an output current drive of 48 mA.

The Am29C841A is a buffered, 10-bit version of the popular '373 function. The Am29C843A is a 9-bit buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems.

The Am29C841A and Am29C843A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce). By controlling the output transient currents, ground bounce and ouput ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry provices for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

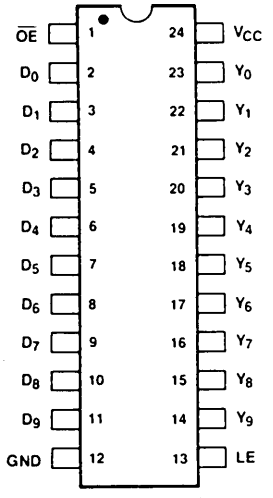
The Am29C841A and Am29C843A are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks.

*For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (PID #10181A).

CONNECTION DIAGRAMS
Top View

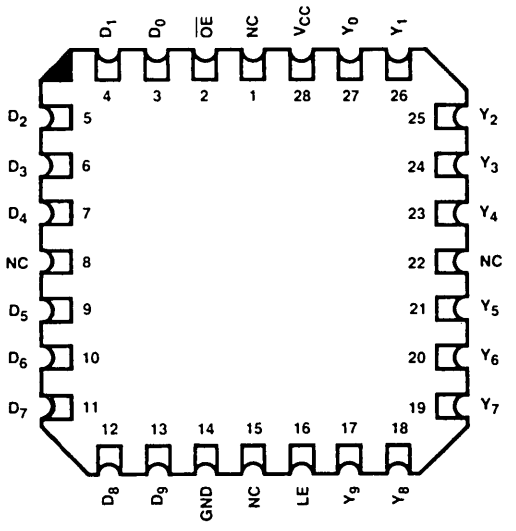
Am29C841A

DIPs*



CD001380

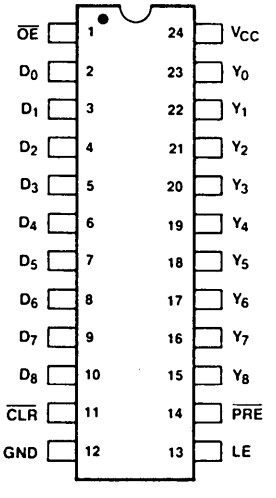
LCC**



CD001390

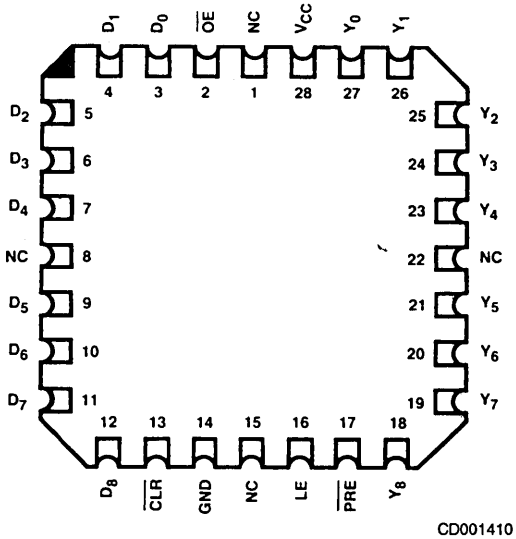
Am29C843A

DIPs*



CD001401

LCC**

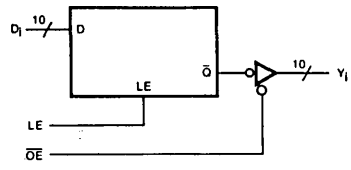


CD001410

* Also available in 24-Pin Flatpack and Small Outline package; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

LOGIC SYMBOLS

Am29C841A



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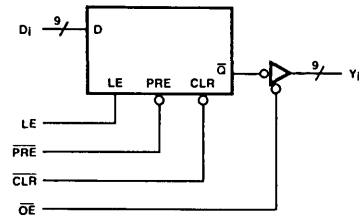
Am29C843A



LS000473

FUNCTION TABLES

Am29C841A

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	X	X	X	Z	Hi-Z
H	H	L	H	Z	Hi-Z
H	H	H	L	Z	Hi-Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

Am29C843A

Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	H	L	H	Transparent
H	H	L	H	L	H	L	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

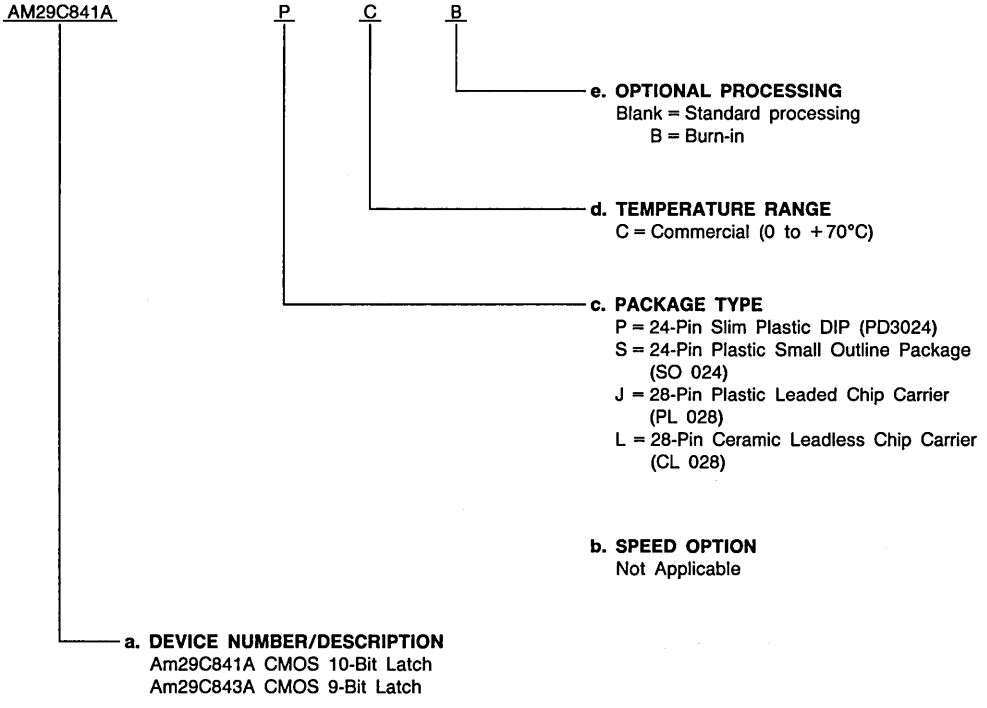
H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C841A	PC, PCB, SC, JC, LC
AM29C843A	

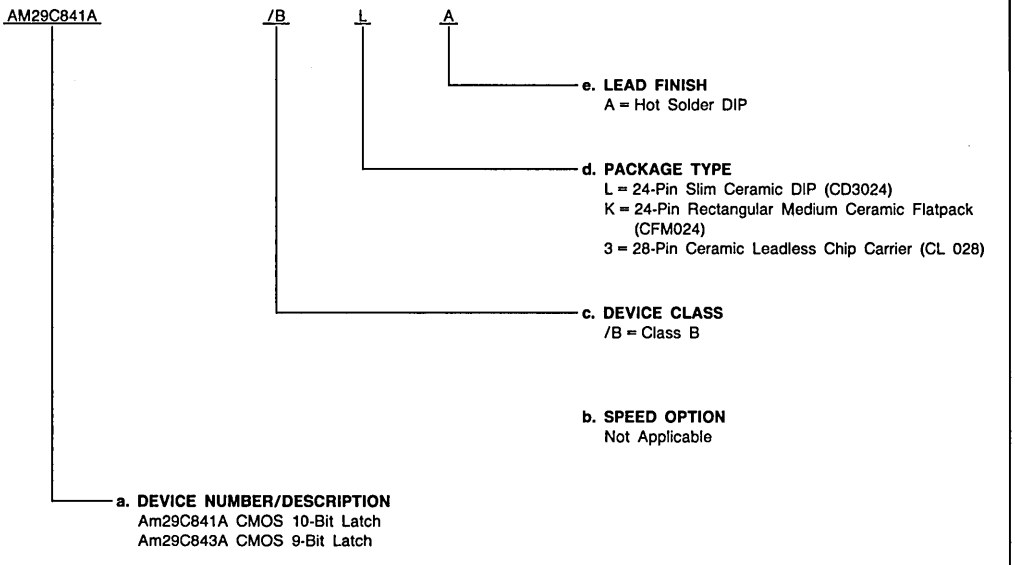
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C841A	/BLA, /BKA, /B3A
AM29C843A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C841A/Am29C843A

D_I Data Inputs (Input)
D_i are the latch data inputs.

Y_I Data Outputs (Output)
Y_i are the three state data outputs.

LE Latch Enable (Input, Active HIGH)
The latches are transparent when LE is HIGH. Input data is latched on a HIGH-to-LOW transition.

$\overline{OE}$ Output Enable (Input, Active LOW)
When $\overline{OE}$ is LOW, the latch data is passed to the Y_i outputs. When $\overline{OE}$ is HIGH, the Y_i outputs are in the high impedance state.

Am29C843A Only

$\overline{PRE}$ Preset (Input, Active LOW)
When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. $\overline{PRE}$ overrides the $\overline{CLR}$ pin. $\overline{PRE}$ will set the latch independent of the state of $\overline{OE}$.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal latch is cleared. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW and $\overline{PRE}$ is HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +6 V
DC Output Voltage ..... −0.5 V to +6 V
DC Input Voltage ..... −0.5 V to +6 V
DC Output Diode Current: Into Output ..... +50 mA
Out of Output ..... −50 mA
DC Input Diode Current: Into Input ..... +20 mA
Out of Input ..... −20 mA
DC Output Current per Pin: I_{SINK} ..... +70 mA
I_{SOURCE} ..... −30 mA
Total DC Ground Current .($n \times I_{OL} + m \times I_{CCT}$) mA (Note 1)
Total DC V_{CC} Current .... ($n \times I_{OH} + m \times I_{CCT}$) mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) Devices
Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	MIL I_{OL} = 32 mA			0.5	Volts
			COM'L I_{OL} = 48 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−10	µA
		V_{CC} = 5.5 V, V_{IN} = 0.4 V				−5	µA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				5	µA
		V_{CC} = 5.5 V, V_{IN} = 5.5 V				10	µA
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V or 2.7 V (Note 3)				+10	µA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V or GND (Note 3)				−10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 4)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V, Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	mA
				COM'L		1.2	mA
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/Bit
				$\overline{OE}$, $\overline{PRE}$, $\overline{CLR}$, LE		3.0	mA/Bit
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 5)				275	µA/MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Off-state currents are only tested at worst-case conditions of V_{OUT} = 5.5 V or 0.0 V.
4. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
5. Measured at a frequency ⩽ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	COMMERCIAL		MILITARY		Units
				Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output Y_i (LE = HIGH) (Note 1)		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		7.5		8.5	ns
t_{PHL}					7.5		8.5	ns
t_S	Data to LE Setup Time			2.5		2.5		ns
t_H	Data to LE Hold Time			2.5		2.5		ns
t_{PLH}	Latch Enable (LE) to Y_i				8		9	ns
t_{PHL}					8		9	ns
t_{PLH}	Propagation Delay, Preset to Y_i				9		11	ns
t_{PHL}					9		11	ns
t_{REC}	Preset ($\overline{PRE}$ ⌐‾) to LE Setup Time			4		4		ns
t_{PLH}	Propagation Delay, Clear to Y_i				11		12	ns
t_{PHL}					11		12	ns
t_{REC}	Clear ($\overline{CLR}$ ⌐‾) to LE Setup Time			3		3		ns
t_{PWH}	LE Pulse Width	HIGH		4		4		ns
t_{PWL}	Preset Pulse Width	LOW		4		4		ns
t_{PWL}	Clear Pulse Width	LOW		4		4		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ‾⌐ to Y_i				9		9.5	ns
t_{ZL}					9		9.5	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⌐‾ to Y_i				8		8.5	ns
t_{LZ}					8		8.5	ns

*See Test Circuit and Waveforms.

Notes: 1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (PID #10181A)

Am29C861A/Am29C863A

High-Performance CMOS Bus Transceivers

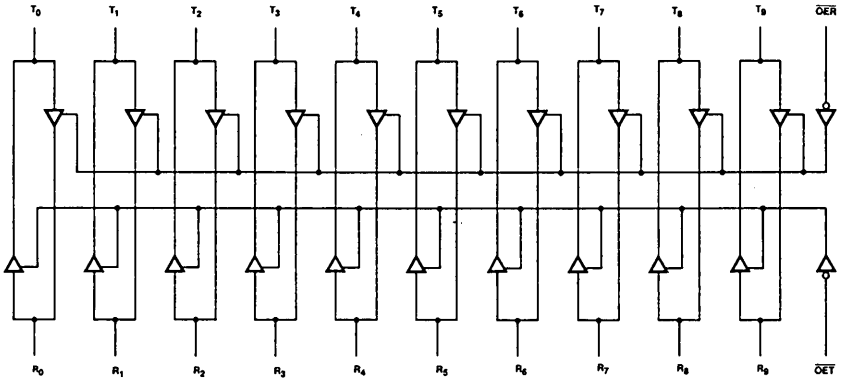
PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High-speed CMOS bidirectional bus transceivers
  - T-R delay = 4 ns typical
- Low standby power
- JEDEC FCT-compatible specs
- Very high output drive
  - I_{OL} = 48 mA Commercial, 32 mA Military
- 200-mV typical hysteresis on data input ports
- Proprietary edge-rate controlled outputs
- Power-up/down disable circuit provides for glitch-free power supply sequencing

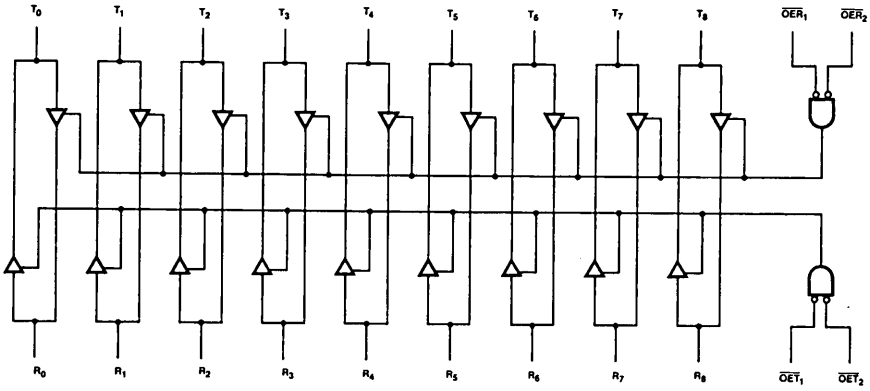
BLOCK DIAGRAMS

Am29C861A



BD001060

Am29C863A



BD001070

Publication # 11231 Rev. A Amendment /0
Issue Date: November 1988

GENERAL DESCRIPTION

The Am29C861A and Am29C863A CMOS Bus Transceivers provide high-performance bus interface buffering for wide address/data paths or buses carrying parity. The Am29C861A is a 10-bit bidirectional transceiver; the Am29C863A is a 9-bit transceiver with NORed output enables for maximum control flexibility. Each device features data inputs with 200-mV typical input hysteresis to provide improved noise immunity. The Am29C861A and Am29C863A are produced with AMD's exclusive CS11SA CMOS process, and features a typical propagation delay of 4 ns, as well as an output current drive of 48 mA.

The Am29C861A and Am29C863A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce). By controlling the output transient currents, ground bounce and ouput ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry provices for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

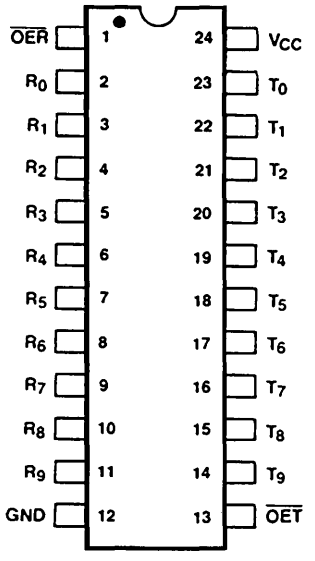
The Am29C861A and Am29C863A are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks.

*For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (PID #10181A).

CONNECTION DIAGRAMS
Top View

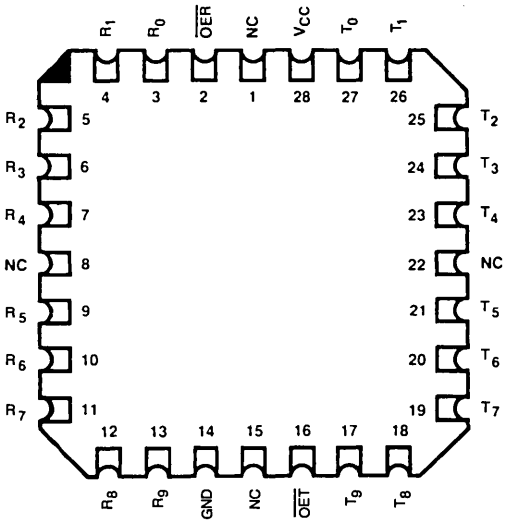
Am29C861A

DIPs*



CD001150

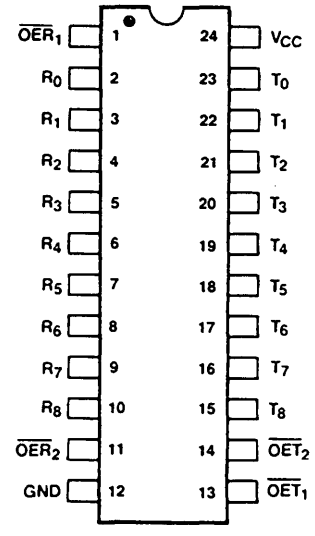
LCC**



CD010810

Am29C863A

DIPs*



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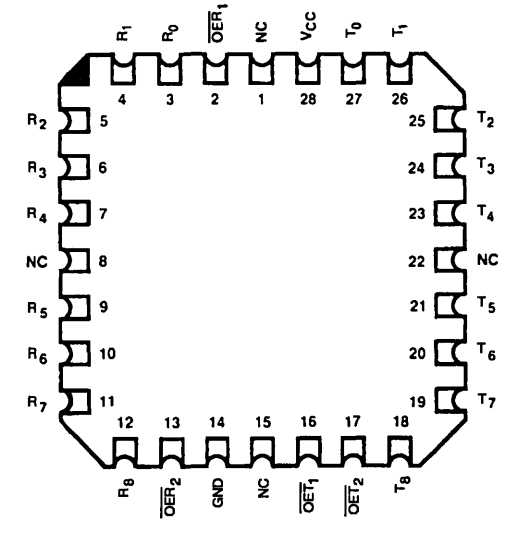
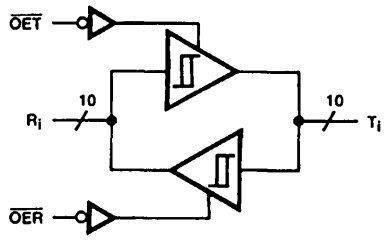


CD001397

* Also available in 24-Pin Flatpack and Small Outline Package; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

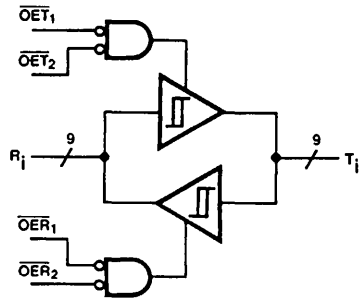
LOGIC SYMBOLS

Am29C861A



LS000372

Am29C863A



LS000382

FUNCTION TABLES

Am29C861A

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	R_I	T_I	R_I	T_I	Function
L	H	L	N/A	N/A	L	Transmit
L	H	H	N/A	N/A	H	Transmit
H	L	N/A	L	L	N/A	Receive
H	L	N/A	H	H	N/A	Receive
H	H	X	X	Z	Z	Hi-Z

Am29C863A

Inputs						Outputs		
$\overline{OET}_1$	$\overline{OET}_2$	$\overline{OER}_1$	$\overline{OER}_2$	R_I	T_I	R_I	T_I	Function
L	L	H	X	L	N/A	N/A	L	Transmit
L	L	X	H	L	N/A	N/A	L	Transmit
H	X	L	L	N/A	L	L	N/A	Receive
X	H	L	L	N/A	L	L	N/A	Receive
L	L	H	X	H	N/A	N/A	H	Transmit
L	L	X	H	H	N/A	N/A	H	Transmit
H	X	L	L	N/A	H	H	N/A	Receive
X	H	L	L	N/A	H	H	N/A	Receive
H	X	H	X	X	X	Z	Z	Hi-Z
X	H	X	H	X	X	Z	Z	Hi-Z

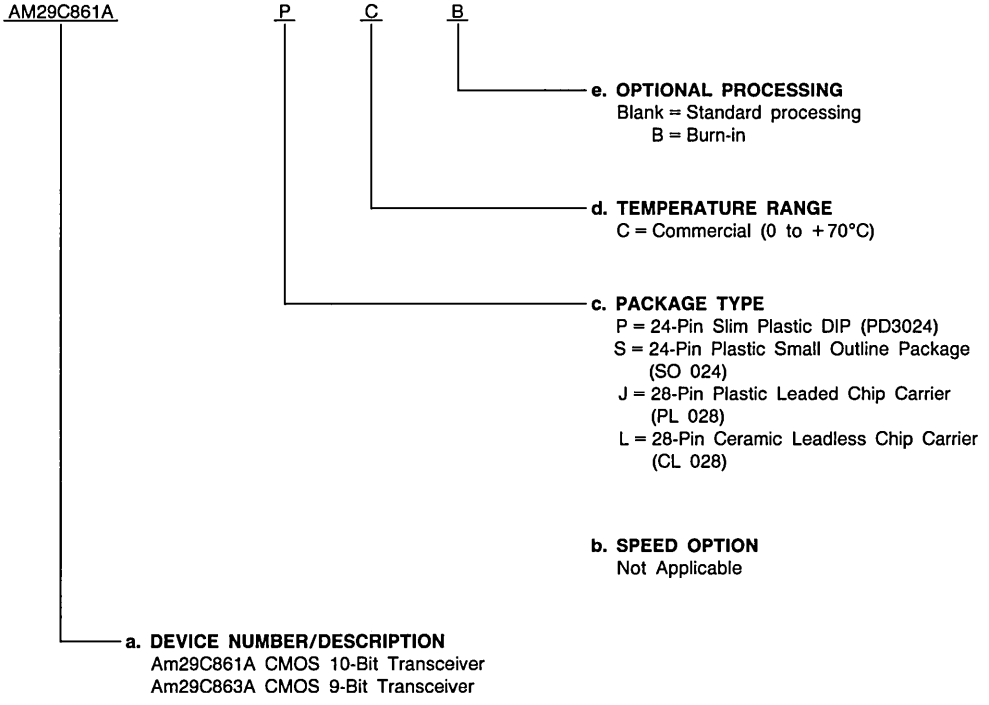
H = HIGH
L = LOW
Z = High Impedance

X = Don't Care
N/A = Not Applicable

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C861A	PC, PCB, SC, JC, LC
AM29C863A	

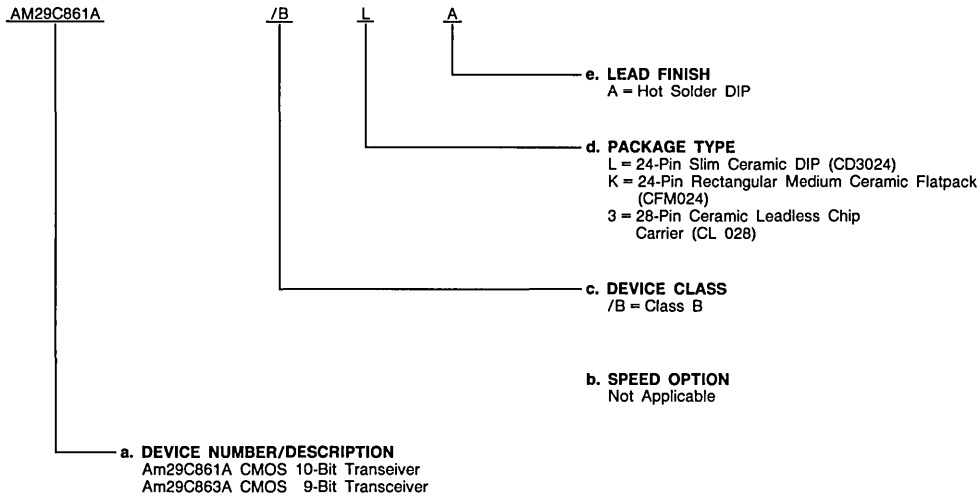
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C861A	/BLA, /BKA, /B3A
AM29C863A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C861A Only

$\overline{OER}$ Output Enable-Receive (Input, Active LOW)
When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET}$ Output Enable-Transmit (Input, Active LOW)
When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i are output).

R_I Receive Port (Input/Output)
R_i are the 10-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_I Transmit Port (Input/Output)
T_i are the 10-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Am29C863A Only

$\overline{OER}_I$ Output Enables-Receive (Input, Active LOW)
When both $\overline{OER}_1$ and $\overline{OER}_2$ are LOW while $\overline{OET}_1$ or $\overline{OET}_2$ (or both) are HIGH, the device is in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET}_I$ Output Enables-Transmit (Input, Active LOW)
When both $\overline{OET}_1$ and $\overline{OET}_2$ are LOW while $\overline{OER}_1$ or $\overline{OER}_2$ (or both) are HIGH, the device is in the Transmit mode (R_i are inputs, T_i are outputs).

R_I Receive Port (Input/Output)
R_i are the 9-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_I Transmit Port (Input/Output)
T_i are the 9-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +6 V
DC Output Voltage..... −0.5 V to +6 V
DC Input Voltage..... −0.5 V to +6 V
DC Output Diode Current: Into Output..... +50 mA
Out of Output ..... −50 mA
DC Input Diode Current: Into Input..... +20 mA
Out of Input ..... −20 mA
DC Output Current per Pin: I_{SINK}..... +70 mA
I_{SOURCE}..... −30 mA
Total DC Ground Current .$(n \times I_{OL} + m \times I_{CCT})$ mA (Note 1)
Total DC V_{CC} Current .... $(n \times I_{OH} + m \times I_{CCT})$ mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A)..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) Devices
Temperature (T_A)..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbols	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	MIL I_{OL} = 32 mA			0.5	Volts
			COM'L I_{OL} = 48 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V Input Only	V_{IN} = 0.0 V			−10	μA
			V_{IN} = 0.4 V			−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V Input Only	V_{IN} = 2.7 V			5	μA
			V_{IN} = 5.5 V			10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V I/O Port	V_{OUT} = 2.7 V			15	μA
			V_{OUT} = 5.5 V			20	
I_{OZL}		V_{CC} = 5.5 V I/O Port	V_{OUT} = 0.4 V			−15	μA
			V_{OUT} = 0.0 V			−20	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 3)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V, Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	mA
				COM'L		1.2	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/Bit
				$\overline{OER_1}$, $\overline{OER_2}$, $\overline{OET_1}$, $\overline{OET_2}$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 4)				275	μA/ MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
4. Measured at a frequency ⩽10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions*	COMMERCIAL		MILITARY		Units
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay from (Note 1) R_i to T_i or T_i to R_i Am29C861A/Am29C863A (Non-inverting)	C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		6.5		7.5	ns
t_{PHL}				6.5		7.5	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i			9		10	ns
t_{ZL}				9		10	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i			8		9	ns
t_{LZ}				8		9	ns

*See Test Circuit and Waveforms.

Notes: 1 *For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (PID #10181A).

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