ADVANCED MEMORY SYSTEMS, INC.

NEW PRODUCT BULLETIN

Fully Functional Memory Devices with Less than 10 nsec Access Time

AMS' initial product emphasis is on building the world's highest performance memory systems. Our competitive advantage in the high-speed area stems from highly sophisticated computer-aided design techniques combined with state of the art semiconductor processing.

The computer simulation allows for the simultaneous design and optimization of the integrated circuits in the full memory system environment. The primary result of this capability is the ability to produce the extremely high-speed memories discussed here with modest integrated circuit processing tolerances. Further, there is a complete commitment to the design approach that includes memory support functions on each integrated circuit memory device. This, in conjunction with the optimization of speed/power performance through our computerized design tools makes possible the achievement of these high speeds with relatively slow signal transition times and low power. This combination of slow transition times and fully functional devices helps solve one of the major problems facing builders of high speed digital system - packaging. The fully functional approach at the integrated circuit level greatly reduces the number of pins required for the first level package. This considerably reduces the cost (standard dual-in-line packages can be used), simplifies the testing, improves the reliability and simplifies second-level packaging (printed circuit cards).

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Also, the slower transition times of the signals minimize the noise generated in the interconnections and reduces the sensitivity of the memory elements to noise. It is possible, therefore, to build very high-speed memory systems with conventional low-cost first and second level packaging approaches.

Enclosed are preliminary product specifications on two of the memory devices AMS has utilized in building ultra high-speed modular memory cards and systems. These devices are now being made available on an individual basis for the first time- offering systems designers in data processing, signal processing, data communications, test equipment and instrumentation the ultimate in both performance and flexibility!

Pricing is as follows:

AMS 0161

1-24	$32.00
25-99	25.60
100-249	21.30
250-499	19.50
500-999	18.40

Delivery: 2 weeks ARO

AMS 0641

1-9	$77.00
10-24	65.10
25-99	61.20
100-249	54.20
250-499	51.60
500-999	47.50

Delivery: 4-8 weeks ARO

Features:

Fully functional	-	decoding and sensing on-chip
Two Chip Selects	-	permits more efficient system utilization of the devices
Wire-OR'able Output	-	for simplified word expansion

Hermetic Dual-In-Line Package
Highest Speed Available on the Market

Order these devices from your local AMS representative (see list attd.) or directly through the Eastern or Western Area Sales offices listed.

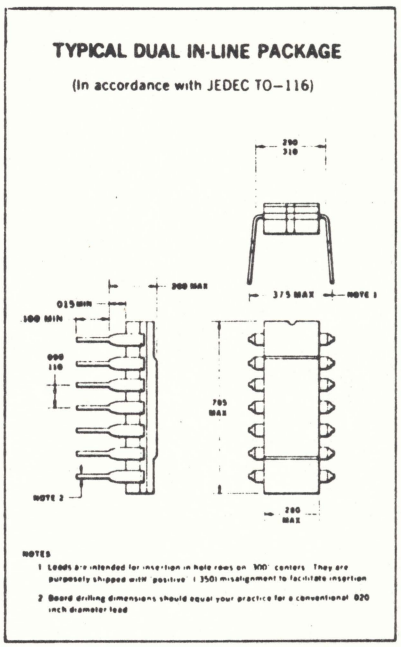
Jerome D. Larkin
Vice President Marketing
May 5, 1970

JDL:pjb

March, 1970
AMS 0641
64 Bit Memory Cell
Preliminary Product Specification*

ADVANCED MEMORY SYSTEMS, INC.

GENERAL DESCRIPTION:



The AMS 0641 is a monolithic 64 bit non-destructive readout memory designed for very high speed CML scratchpad, register, buffer and control memory applications. It is organized as 64 words by one bit with full address decoding and output sense amplification included on-chip. This device features a typical access time of 7 nsec, power dissipation of 5 mw/bit and two Select Inputs which provide an additional level of decoding in memory systems.

A key feature of the design of the AMS 0641 is that it draws virtually constant current over the range of power supply voltages from 3 to 7 volts. The performance of the AMS chip is relatively constant over this range of voltages whereas conventional designs are quite restricted. The ability to operate at 3.5 volts rather than 5.2 volts could represent a 33% savings in power with no loss of speed performance. This insensitivity to voltage variations allows the use of simple power supplies with minimal regulation or filtering. Power distribution is particularly simple, too, since load current is constant. The importance of these points is emphasized when it is considered that power supplies and distribution are estimated to be 20-25% of the hardware costs of computing systems.

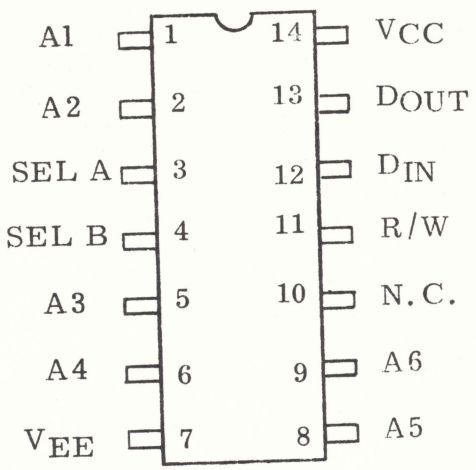
The AMS 0641 now makes it possible, therefore, to build very high-speed memory systems with conventional first and second level packaging and standard cooling techniques.

OPERATION:

ADDRESS: To select a particular bit location apply the appropriate binary code to ADDRESS INPUTS 1-6.

READ: To read the contents of an address, the SELECT inputs must be held LOW and the READ/WRITE input must be HIGH while the bit location is addressed.

WRITE: Writing is accomplished by addressing the desired bit location (both SELECT lines LOW) and momentarily bringing the READ/WRITE line LOW while the DATA IN is valid.



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*Specification is subject to change.

ABSOLUTE MAXIMUM RATINGS:

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{EE}	-7.0	V_{DC}
Input Voltages	V_{IN}	0 to V_{EE}†	V_{DC}
Output Current	I_O	25	mA
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +125	°C

† Assuming power applied to circuit

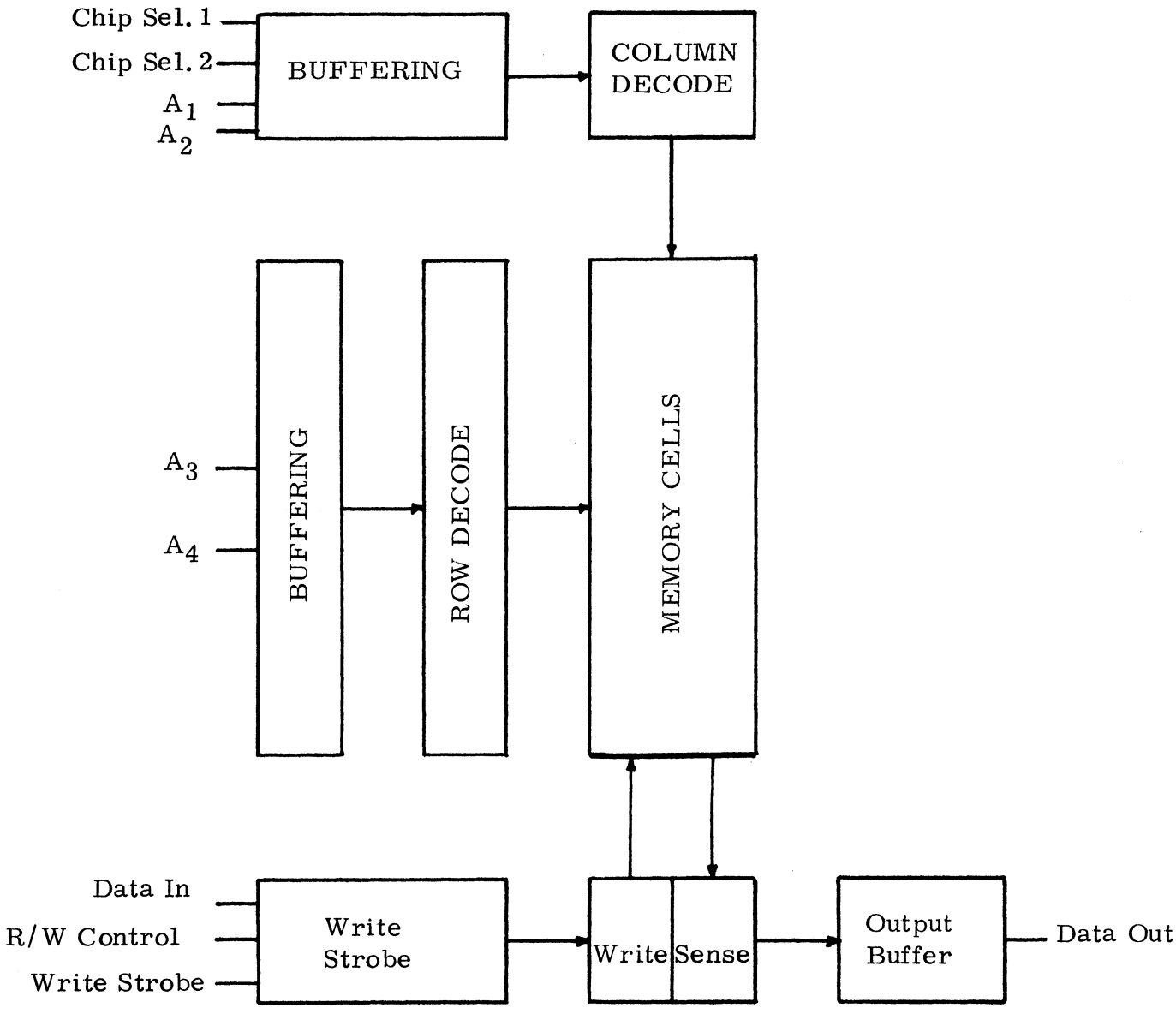
DC CHARACTERISTICS:

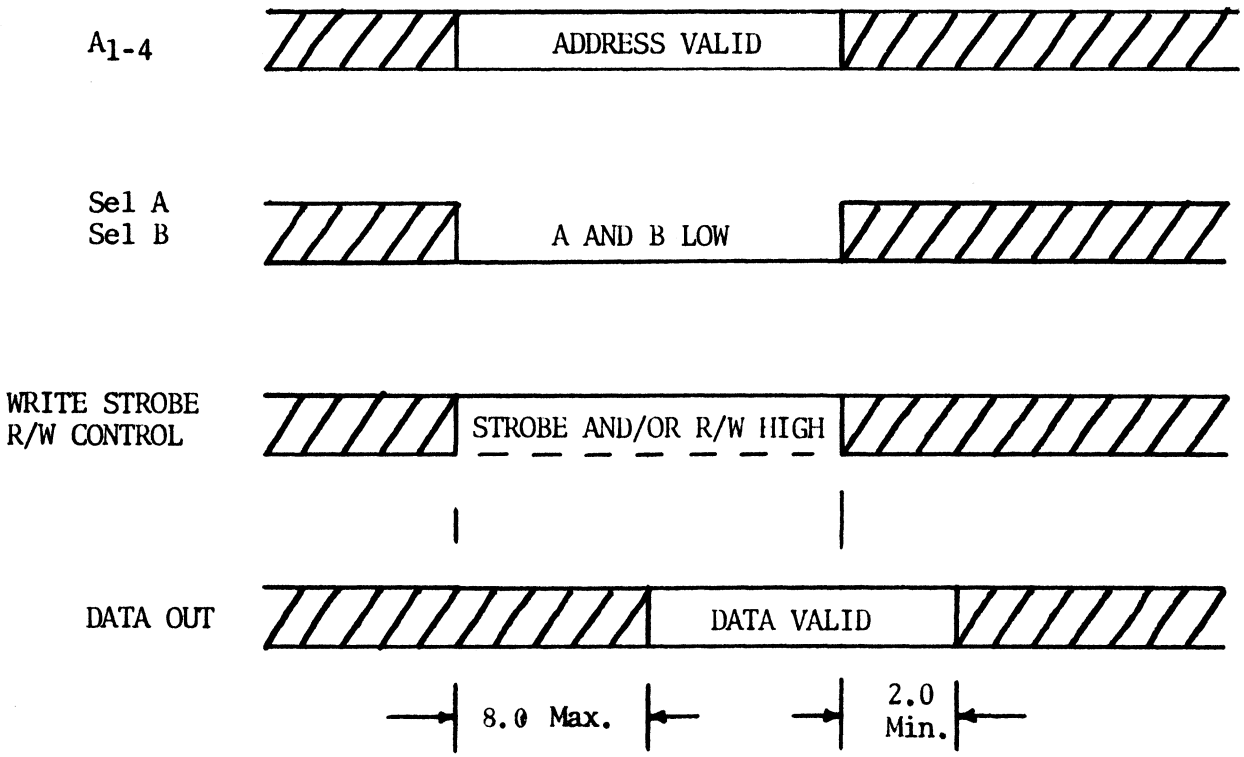
at T_A = 25°C, V_{EE} = -5.2 ± 5% V_{DC}, V_{CC} = Ground

CHARACTERISTIC	SYMBOL	TEST LIMITS MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input "HIGH" Voltage	V_{IH}	-1.00	-0.800	-0.400	V_{DC}	
Input "LOW" Voltage	V_{IL}	V_{EE}	-1.600	-1.350	V_{DC}	
Input Load Current[1]	I_{IN}		25	60	μA	V_I = -0.8 V_{DC}
Input Leakage Current	I_R			10	μA	V_I -1.6 V_{DC}
Output "HIGH" Voltage	V_{OH}	-0.950	-0.870	-0.700	V_{DC}	R_L 90 ohms
Output "LOW" Voltage	V_{OL}	-1.850	-1.630	-1.450	V_{DC}	to -2.0 V_{DC}
Supply Current	I_E		75		mA	

1 Values given are for single unit load inputs, i.e., address and data inputs. Read/Write and Write Strobe are two unit load inputs.

16 x 1 FUNCTIONAL DIAGRAM



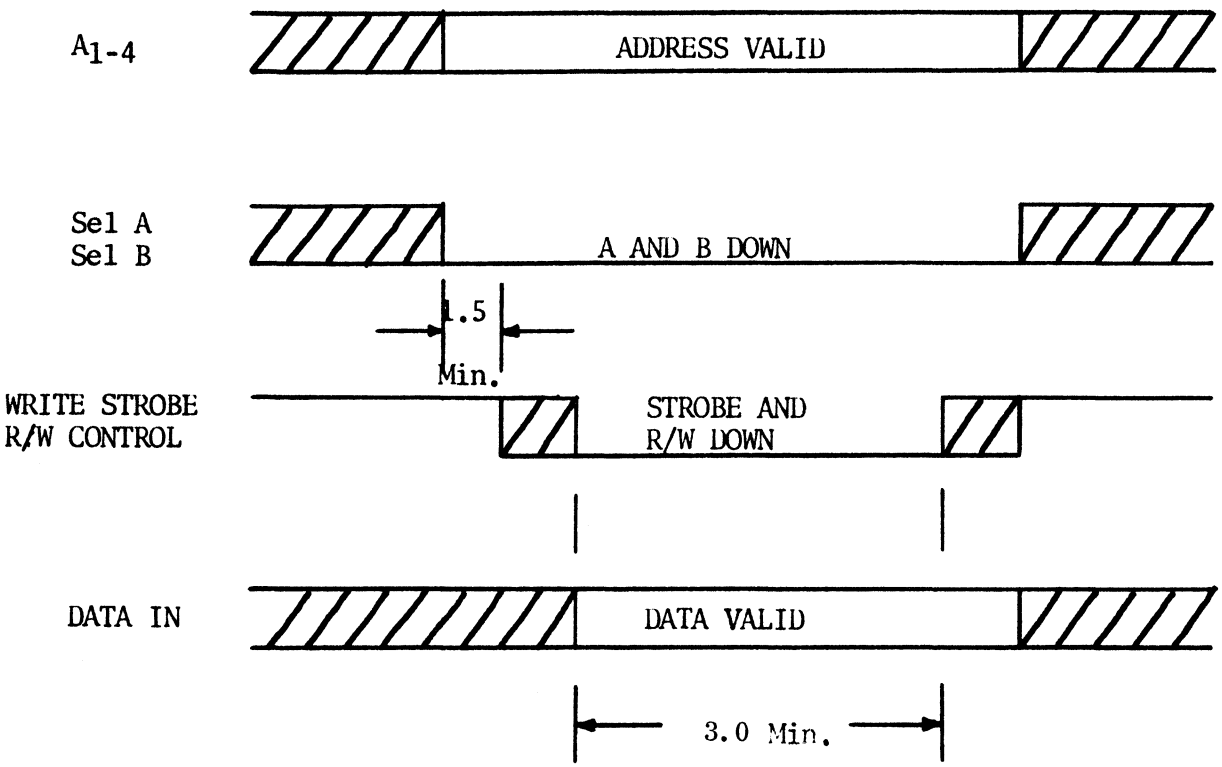


Note:

1. To read, Write Strobe Input and/or R/W Control input must be "High".

2. Data out will go negative, to allow wired-or outputs, a minimum of 2.0 and a maximum of 6.2 nsec after either chip select input goes "High".
Data out will remain negative for a minimum of 2.0ns and may stay negative as long as 6.2 ns after both Sel A and Sel B go "Low".

AMS 0161 TIMING CHART-READ



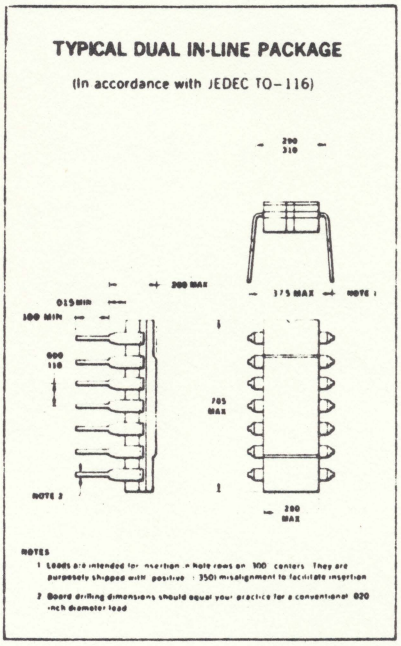
Note: 1. Write Strobe and R/W Control Pulses can occur anytime, when addresses are valid and chip selects A and B have been selected (Low) for 1.5nsec.

2. Data need be valid only during the last 3.0 nsec of Write Strobe and R/W Control pulse coincidence.

AMS 0161 TIMING CHART-WRITE

March, 1970
AMS 0161
16 BIT MEMORY CELL

ADVANCED MEMORY SYSTEMS, INC.



GENERAL DESCRIPTION:

The AMS 0161 is a monolithic 16 bit non-destructive readout memory designed for very high speed CML scratch-pad, register, buffer and control memory applications. It is organized as 16 words by one bit with full address decoding and output sense amplification included on-chip. This device features a typical access time of 5 nsec and two Chip Select inputs which provide an additional level of decoding in memory systems.

OPERATION:

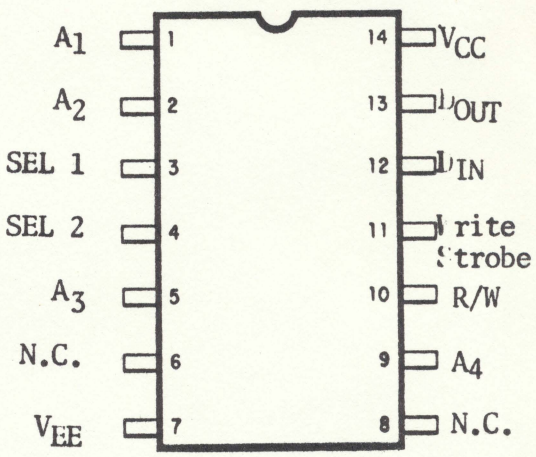
ADDRESS: To select a particular bit location, apply the appropriate binary code to ADDRESS INPUTS 1-4.

READ: To read the contents of an address, the CHIP SELECT inputs must be held LOW, the READ/WRITE CONTROL and/or the WRITE STROBE inputs must be HIGH while the bit location is addressed.

WRITE: Writing is accomplished by selecting the desired bit location; bring the CHIP SELECTS LOW; bringing LOW the WRITE STROBE and READ/WRITE CONTROL while the DATA IN is valid.

CHIP SELECT: Two CHIP SELECT inputs are provided for more efficient system utilization of this device. Either input can be used to select a particular row or column of packages on a P.C. card. The output is forced LOW when either CHIP SELECT is HIGH.

OUTPUT: The output is open-emitter which may be Wire-OR'ed for word length expansion. An external resistor should be provided to pull down the OR'ed outputs and terminate the line. (90 ohms to -2v is recommended)



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SELECT: Two SELECT inputs are provided for more efficient system utilization of this device. Either input can be used to select a particular row or column of packages on a P.C. card. The output is forced LOW when either SELECT is HIGH.

OUTPUT: The output is an unterminated emitter which may be Wire-OR'ed for word length expansion. An external resistor should be provided to pull down the OR'ed outputs and terminate the line. (90 ohms to -2v is recommended)

ABSOLUTE MAXIMUM RATINGS:

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{EE}	-7.0	V_{DC}
Input Voltages	V_{IN}	0 to V_{EE}†	V_{DC}
Output Current	I_O	25	mA
Operating Temp.	T_A	0 to +70	°C
Storage Temp.	T_{STG}	-55 to +125	°C

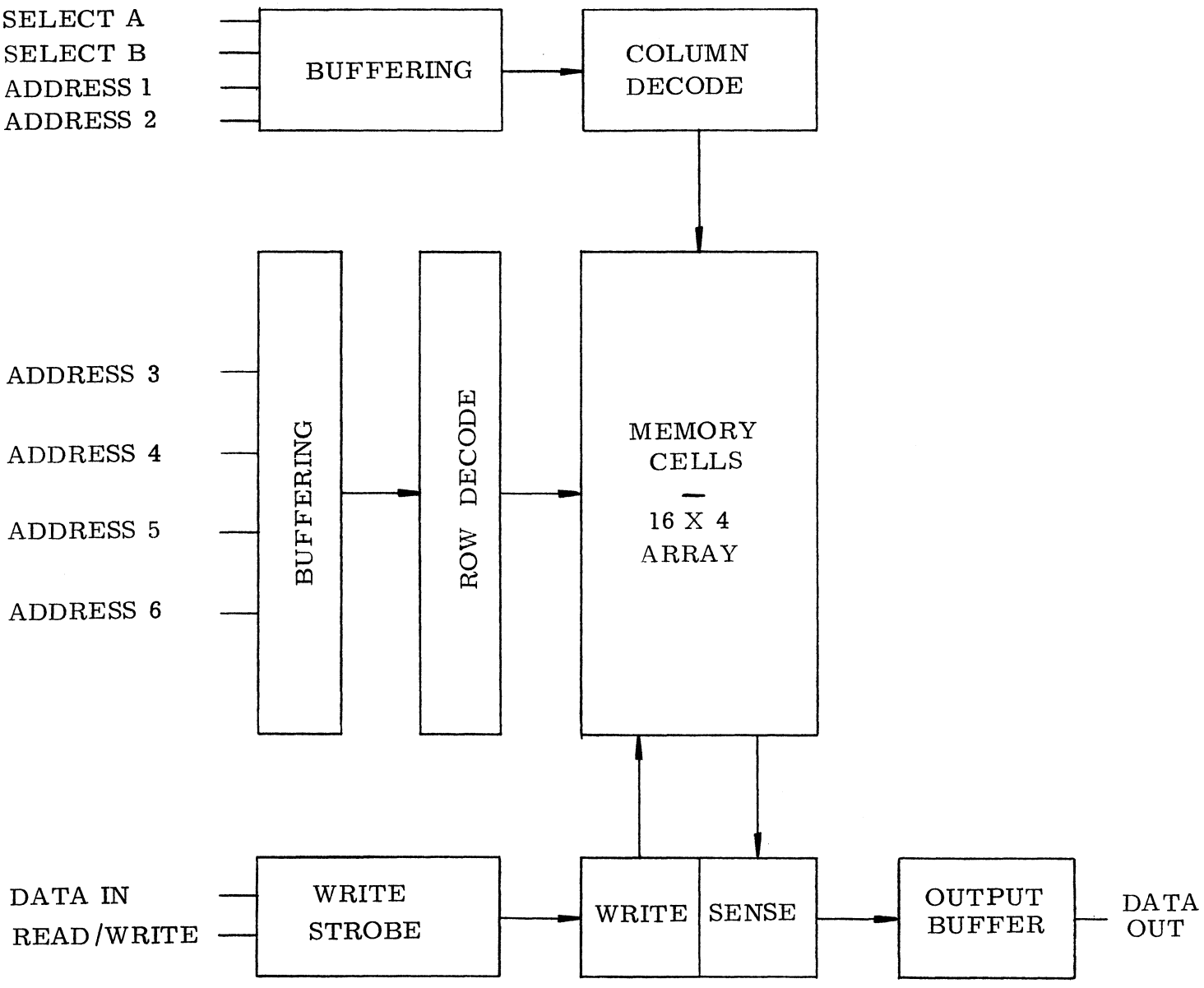
† Assuming power applied to circuit.

DC CHARACTERISTICS:

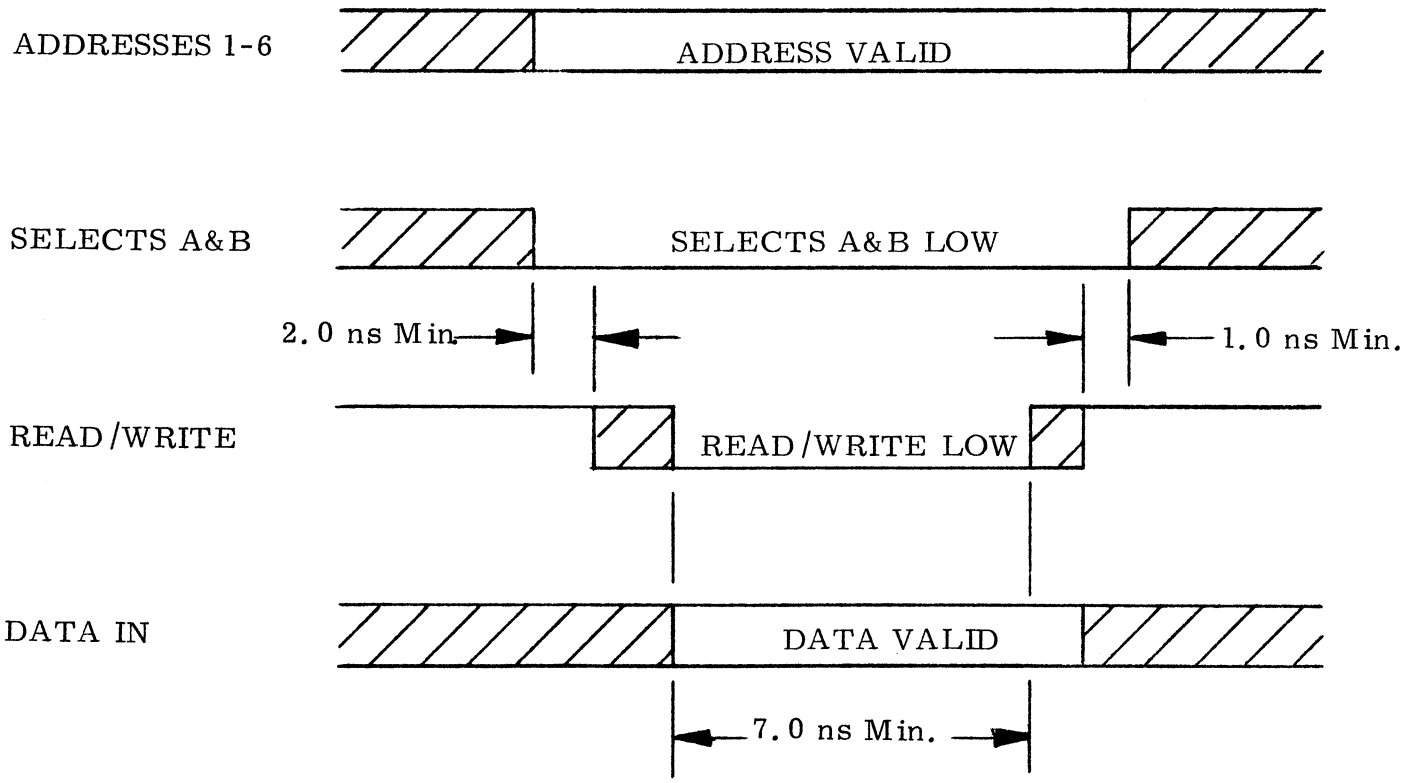
at $T_A = 25°C$, $V_{EE} = -3.5\ V_{DC}$ to $-6.5\ V_{DC}$, V_{CC} = Ground

CHARACTERISTIC	SYMBOL	TEST LIMITS MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input "HIGH" Voltage	V_{IH}		-0.80	-0.40	V_{DC}	
Input "LOW" Voltage	V_{IL}	V_{EE}	-1.60		V_{DC}	
Input Load Current	I_{IN}		≦50		μA	V_I = -0.8 V_{DC}
Input Leakage Current	I_R			10	μA	V_I = -1.6 V_{DC}
Output "HIGH" Voltage	V_{OH}		-0.88		V_{DC}	R_L = 90 ohms
Output "LOW" Voltage	V_{OL}		-1.90		V_{DC}	to -2.0 V_{DC}
Supply Current	I_E		80		mA	

AMS 0641 FUNCTIONAL DIAGRAM



WRITE CYCLE:

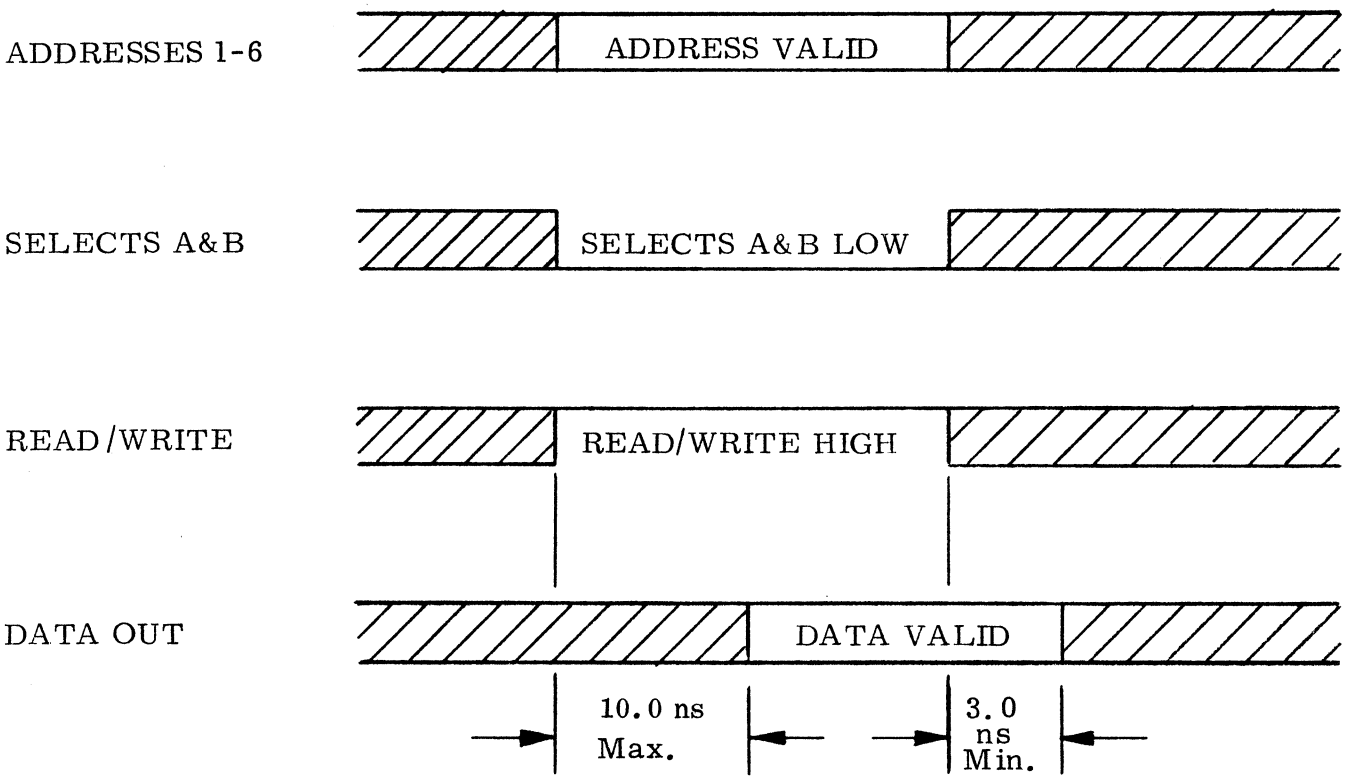


Notes:

1. Transistons may occur only in shaded regions.
2. Negative going READ/WRITE pulse can occur anytime, when ADDRESSES are valid and SELECTS A and B have been LOW for 2.0 ns.
3. DATA IN need be valid only during the last 7.0 ns of the negative going READ/WRITE pulse.

SWITCHING CHARACTERISTICS:
@ T_A = 25 C, V_{EE} = -3.5 V_{DC} to -6.5V_{DC} , V_{CC} = GROUND

READ CYCLE:



Notes:
1. Transitions may occur only in shaded regions.
2. DATA OUT will go LOW to allow wired - OR outputs, a minimum of 3.0 ns and a maximum of 7.0 ns after either SELECT goes HIGH. DATA OUT will remain LOW for a minimum of 3.0 ns and may stay LOW as long as 7.0 ns after both SELECT A and B go LOW.
3. Output load is R_L = 90 ohms to -2.0 Vdc, C_L = 15 pf.