AMS
Advanced Memory Systems

1275 HAMMERWOOD AVENUE, SUNNYVALE, CALIFORNIA 94086

JULY 1976

2650

8-Bit NMOS Monolithic Microprocessor

Features

Ease of Use

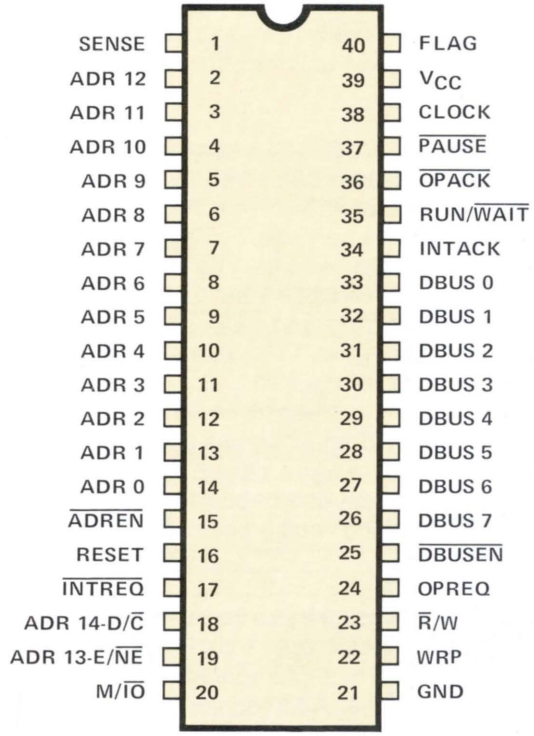
- Static Logic
  - Easy to Debug
  - True Single-Step Operation
- Single-Phase TTL-Level Clock Input
  - Simple Interface
  - Non-Critical Timing
- Single +5 Volt Power Supply
- General Purpose Instruction Set
- Tri-State* Output Busses (except A_{13} and A_{14})
- Machine Cycle Time of 2.4 μs at 1.25 MHz Clock Frequency
- N-Channel Silicon-Gate MOS Technology
- 40-Pin Ceramic Dual-Inline Package
- TTL-Compatible Inputs and Outputs
- 32K Byte Addressing Range
- Separate Address and Data Lines
- Direct Instructions Take 2, 3 or 4 Cycles
- Uses Standard Low-Cost Semiconductor Memories
- Expanding Family of I/O Devices

Ease of Programming

- Fixed Set of 75 Instructions
  - Most Complex Operation Executes in 9.6 μs
  - Fastest Operation Executes in 4.8 μs
- Parallel 8-Bit Binary Operation
- Seven General-Purpose Registers
  - Use as Source or Destination for Arithmetic Operations
  - Use as Index Registers
  - Easy I/O Transfer
- Vector Interrupt Format
  - Easy to Use with Separate I/O Lines
- Return Address Stack, 8 Deep, On Chip
  - Automatic Subroutine Nesting
- Variable-Length Instructions
  - 1, 2, or 3 Byte Lengths
  - Conserves Memory
- Address Capability Up to 32,768 Bytes of Memory
- Flexible Addressing Modes
  - Register
  - Immediate
  - Relative
  - Absolute
  - Indirect
  - Indexed

* *Tri-Share is a registered trademark of National Semiconductor Corp.*

Pin Configuration



TOP VIEW

Description

The 2650 microprocessor is a general-purpose, single-chip, fixed instruction set, 8-bit parallel binary device. A general-purpose processor can perform any data manipulation through a stored set of machine instructions. The processor function has been designed to resemble those of conventional binary computers, but will execute variable-length instructions of one to three bytes in length. Binary Coded Decimal (BCD) arithmetic is made possible through use of a special Decimal Adjust Register (DAR) instruction.

The 2650 microprocessor is manufactured using an N-channel silicon-gate process technology. N-channel configuration provides high carrier mobility for high speed, and allows the use of a single 5V power supply. The silicon-gate process contributes to improved speed and better transistor density. Standard 40-pin dual in-line packages are used.

The microprocessor contains seven general-purpose registers, each eight bits long. They may be used as sources or destinations for arithmetic operations, as index registers, or for I/O transfers. The processor can address up to 32,768 bytes of memory in four pages of 8,192 bytes each. Processor instructions are one, two or three bytes long, depending on the instruction. Variable-length instructions tend to conserve memory space, since a one- or two-byte instruction may be used rather than a three-byte instruction. The first byte of each instruction always specifies the operation to be performed and the addressing mode to be used. Most instructions use six of the first eight bits for this purpose, with the remaining two bits making up the register field. Some instructions use the full eight bits as an operation code.

The most complex direct instruction is three bytes long and requires 9.6 μs to execute. This figure assumes that the processor is operating at its maximum clock rate and has an associated memory with cycle and access times of less than one microsecond. The fastest instruction executes in 4.8 μs. The clock input to the processor is a single-phase pulse train and uses only one interface pin. It requires a normal TTL voltage swing, and no special clock driver is required.

The Data Bus and Address signals are tri-state to provide convenience in system design. Memory and I/O interface signals are asynchronous so that Direct Memory Access (DMA) and multiprocessor operations are easy to implement.

The 2650 microprocessor has a versatile set of addressing modes used to locate operands for operations. The interrupt mechanism is implemented as a single level, address-vectoring type. Address vectoring means that an interrupting device can force the processor to execute code at a device-determined level in memory.

Absolute Maximum Ratings [1]

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input, Output and Supply Voltages with Respect to Ground (Note 2)	−0.5V to +6V
Power Dissipation	1.6W

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

Capacitance

	SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST COND.
1	C_{IN}	Input Capacitance		10	pF	V_{IN}=0V, T_A=0°C to 70°C
2	C_{OUT}	Output Capacitance		10		V_{OUT}=0V, T_A=0°C to +70°C

Order Information

CLOCK PERIOD	PACKAGE TYPE	ORDER CODE
800ns	Ceramic DIP	2650-11-6G

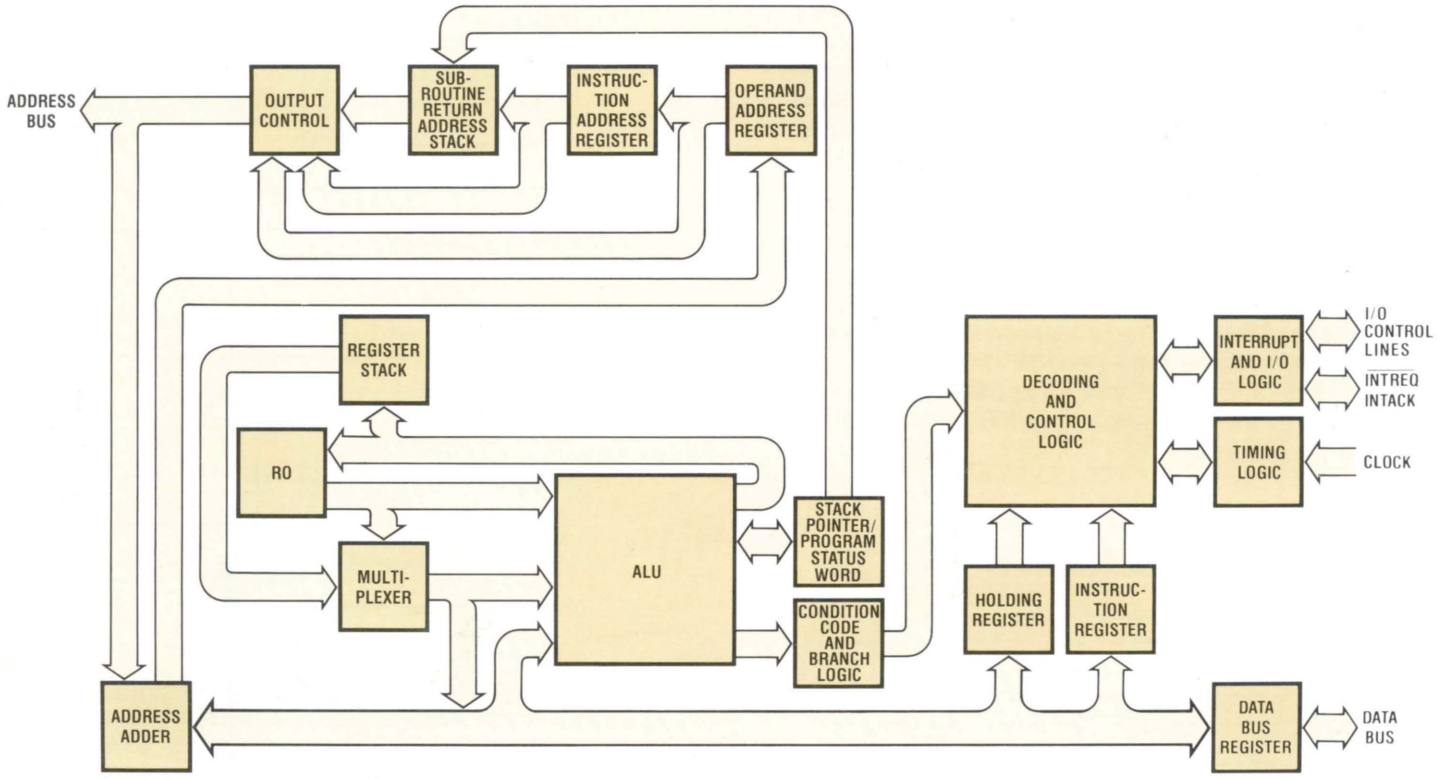
SUNNYVALE
PHONE: (408) 734-4330
TWX: (910) 339-9369

BOSTON
PHONE: (617) 259-0050
TWX: (710) 390-1768

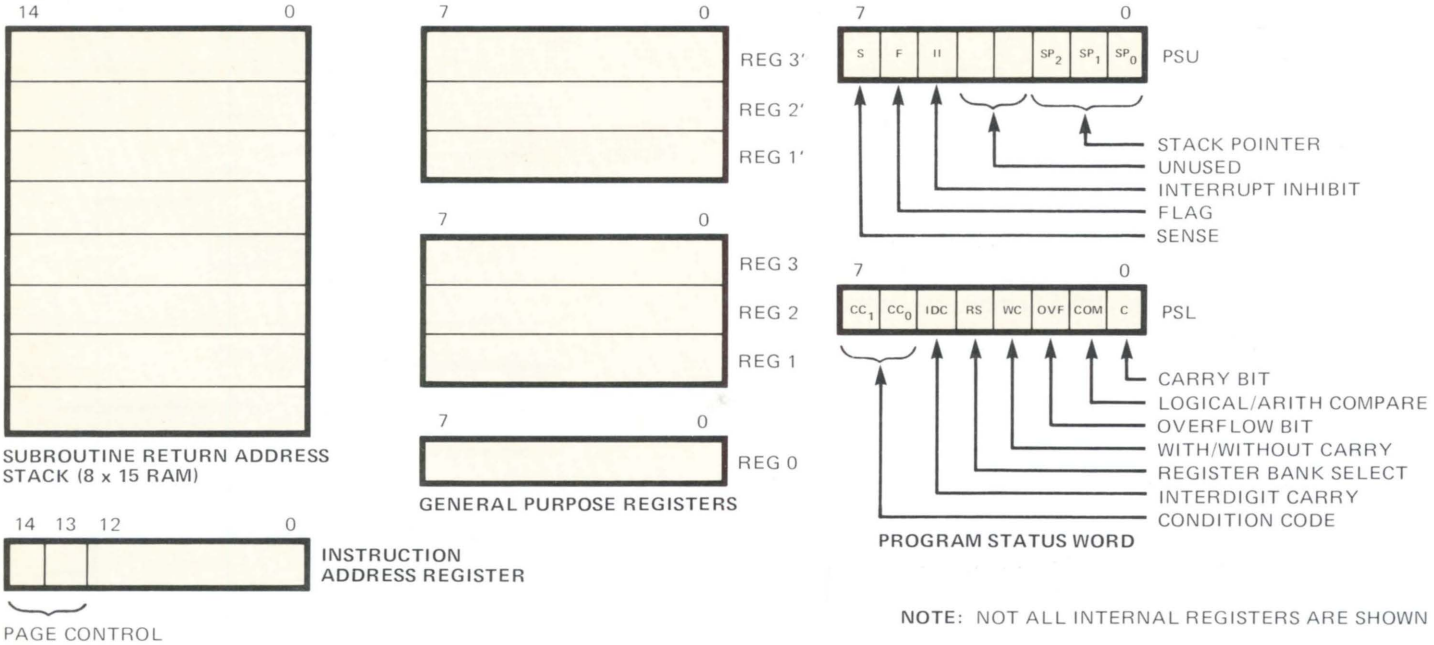
CHICAGO
PHONE: (312) 529-1474
TWX: (910) 291-3825

LONDON
PHONE: 01-542-4690
TELEX: 851 928139
CANFOR G

Functional Block Diagram



Major 2650 Registers

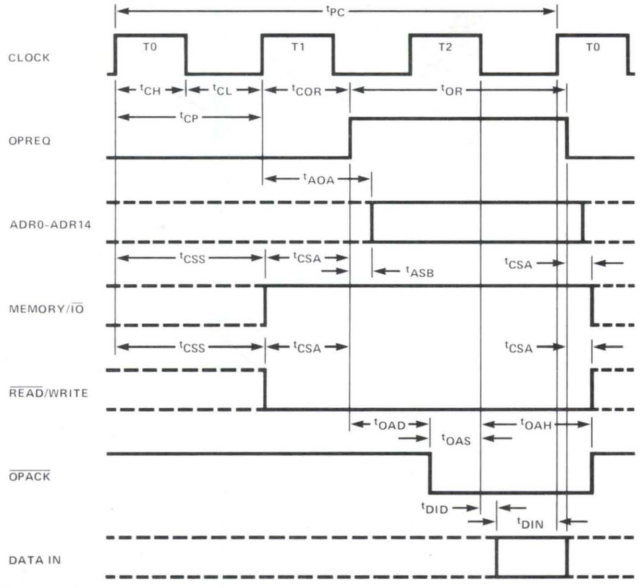


NOTE: NOT ALL INTERNAL REGISTERS ARE SHOWN

Timing Diagrams

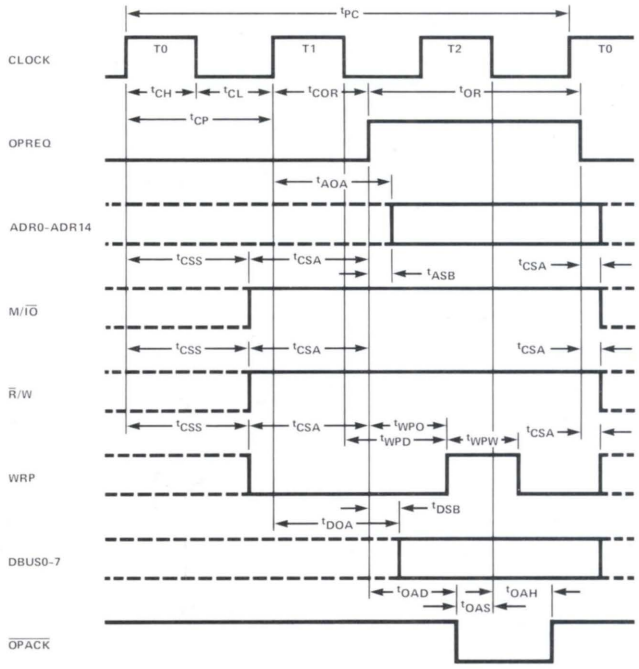
The clock input to the 2650 microprocessor provides the basic timing information which the device uses for all internal and external operations. The clock rate determines the instruction execution time, except when limited by external memories and associated devices. The maximum clock rate of the 2650 is 1.25 MHz (one clock period is 80 ns minimum). A unique feature of the microprocessor is that the clock frequency may be slowed to 0Hz, allowing complete timing flexibility for interfacing. This feature permits the clock to be single-stepped to simplify system checkout. It also provides an easy means of stopping the processor. Each 2650 cycle is composed of three clock periods. Direct instructions require either 2, 3 or 4 processor cycles for execution, and therefore will vary from 4.8 to 9.6 μs in duration.

Memory Read Sequence



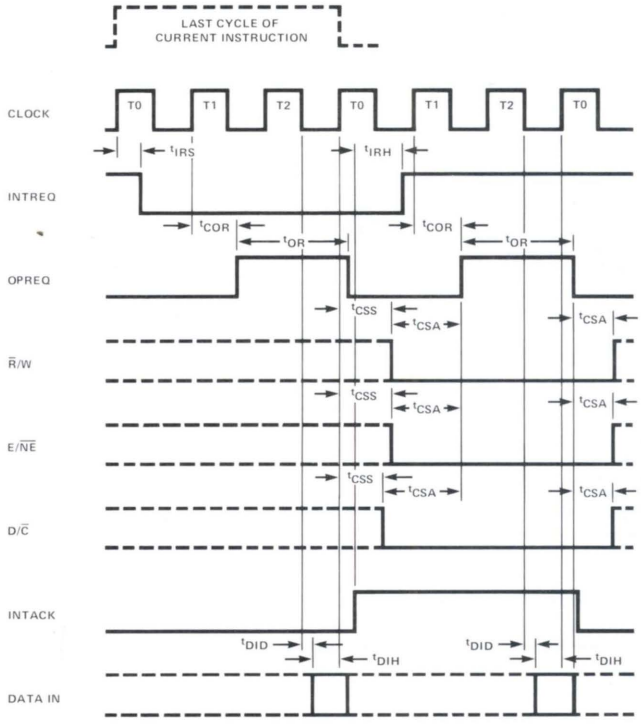
Note that in the timing diagram for a Memory Read cycle, OPREQ (Operation Request) is the master control signal which coordinates all operations external to the processor. When true, OPREQ indicates that other output signals are valid. During a Memory Read cycle, M/IO is in the M (memory) state, and R/W is in the R (read) state. The address and control lines become valid when OPREQ rises. The data to be read may be returned any time after OPREQ becomes valid. An $\overline{\text{OPACK}}$ (Operation Acknowledge) should accompany the read data from the memory. The data and $\overline{\text{OPACK}}$ signals should remain valid for 50 ns after OPREQ falls. If the $\overline{\text{OPACK}}$ signal is delayed by the memory device, the processor will wait until this signal is received. OPREQ is lowered only after receipt of $\overline{\text{OPACK}}$. The memory device will raise $\overline{\text{OPACK}}$ after OPREQ falls.

Memory Write Sequence

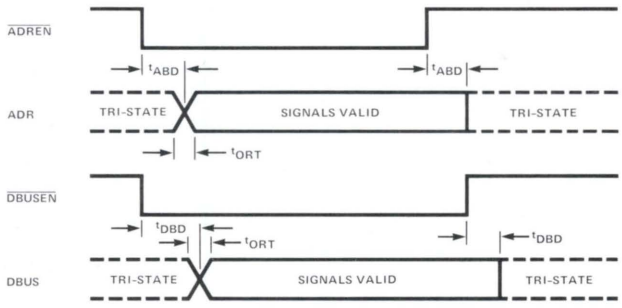


The signals involved with the processor's Memory Write sequence are similar to those used in the Memory/Read cycle, with the following exceptions: (1) the R/W signal is in the W state and (2) the WRP signal provides a positive-going pulse during the write sequence, which may be used as a chip enable command, write pulse, etc.

Interrupt Timing



Tri-State Bus Timing



Input/Output Timing

The signal exchanges for input/output timing with external devices is very similar to the Memory Read/Write sequences.

AC Characteristics 1, 2, 3, 7

TEST CONDITIONS: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

	SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
1	t_{CH}	Clock High Phase Time	400	10,000	ns	
2	t_{CL}	Clock Low Phase Time	400	∞		
3	t_{CP}	Clock Period Time	800	∞		
4	t_{PC}	Processor Cycle Time	2,400	DC		See Note 5
5	t_{OR}	OPREQ Pulse Width	$2t_{CH} + t_{CL} - 100$	∞		
6	t_{COR}	Clock to OPREQ Time	100	500		
7	t_{AOA}	Address Out Available Time	—	700		
8	t_{DOA}	Data Out Available Time	—	900		See Note 6
9	t_{CSA}	Control Signal Available Time	50	—		
10	t_{CSS}	Control Signal Stable Time	—	1,200		
11	t_{ASB}	Address Stable Time	—	230		See Note 7
12	t_{DSB}	Data Stable Time	—	420		
13	t_{OAS}	$\overline{\text{OPACK}}$ Setup Time	60	—		
14	t_{OAD}	$\overline{\text{OPACK}}$ Delay Time	0	10,000		
15	t_{OAH}	$\overline{\text{OPACK}}$ Hold Time	60	—		See Note 6
16	t_{DID}	Data In Delay Time	—	150		See Note 6
17	t_{DIH}	Data In Hold Time	250	—		
18	t_{WPD}	Write Pulse Delay Time	300	500		See Note 6
19	t_{WPW}	Write Pulse Width	$t_{CL} - 100$	t_{CL}		
20	t_{WPD}	Write Pulse From OPREQ	$t_{CH} - 200$	$t_{CH} + 400$		
21	t_{IRG}	$\overline{\text{INTREQ}}$ Setup Time	—	100		See Note 6
22	t_{IRH}	$\overline{\text{INTREQ}}$ Hold Time	0	—		
23	t_{ABD}	Address Bus Delay Time	—	220		
24	t_{DBD}	Data Bus Delay Time	—	120		
25	t_{ORT}	Output Buffer Rise Time	—	150		See Note 4

NOTES:

1. Input levels swing between 0.80 and 2.2 volts.
2. Input signal transition times are 20ns.
3. Timing reference level is 1.5 volts.
4. Load is -100 μA and 100 pf.
5. Processor cycle time consists of three clock periods.
6. Parameter definition change.
7. In order to avoid slowing the processor down, input data must be returned to the processor in 650ns or less time from the OPREQ edge, at a cycle time of 2.4 μs.

DC Characteristics

TEST CONDITIONS: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

	SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
1	I_{LI}	Input Load Current	—	10	μA	V_{IN} = 0 to 5.25V
2	I_{LOH}	Output Leakage Current, High	—	+10		ADREN, DBUSEN = 2.2V, V_{OUT} = 4V
3	I_{LOL}	Output Leakage Current, Low	—	−10		ADREN, DBUSEN = 2.2V, V_{OUT} = 0.45V
4	I_{CC}	Power Supply Current	—	150	mA	V_{CC} =5.25V, T_A = 0°C
5	V_{IL}	Input Voltage Low	−0.5	0.8	V	
6	V_{IH}	Input Voltage High	2.2	V_{CC}		
7	V_{OL}	Output Voltage Low	0	.45		I_{OL} =1.6 mA
8	V_{OH}	Output Voltage High	2.4	V_{CC}−.5		I_{OH} = −100 μA

Instruction Set

The 2650 microprocessor instruction set is powerful, easily understood, and typical of larger computers. Numerous addressing modes provide for one-, two- and three-byte instructions. A complete list of instructions is shown in the following table.

Automatic incrementing or decrementing of an index register is available in the arithmetic indexed instructions. All of the branch instructions except for indexed branching are conditional. Register-to-register instructions are one byte; register-to-storage instructions are two or three bytes long. The two-byte register-to-memory instructions are either immediate or relative addressing types.

Instruction Set Table

	MNEMONIC		DESCRIPTION OF OPERATION	AFFECTS	CYCLES
LOAD/STORE	LOD	Z	Load Register Zero		2
		I	Load Immediate		2
		R	Load Relative		3
		A	Load Absolute	CC (Note 1)	4
	STR	Z	Store Register Zero (r ≠ 0)		2
		R	Store Relative	—	3
		A	Store Absolute	—	4
ARITHMETIC	ADD	Z	Add to Register Zero w/wo Carry		2
		I	Add Immediate w/wo Carry		2
		R	Add Relative w/wo Carry		3
		A	Add Absolute w/wo Carry	C, CC (Note 1), IDC, OVF	4
	SUB	Z	Subtract from Register Zero w/wo Borrow		2
		I	Subtract Immediate w/wo Borrow		2
		R	Subtract Relative w/wo Borrow		3
		A	Subtract Absolute w/wo Borrow		4
	DAR		Decimal Adjust Register	CC (Note 2)	3
LOGICAL	AND	Z	AND to Register Zero (r ≠ 0)		2
		I	AND Immediate		2
		R	AND Relative		3
		A	AND Absolute		4
	IOR	Z	Inclusive OR to Register Zero		2
		I	Inclusive OR Immediate	CC (Note 1)	2
		R	Inclusive OR Relative		3
		A	Inclusive OR Absolute		4
	EOR	Z	Exclusive OR to Register Zero		2
		I	Exclusive OR Immediate		2
		R	Exclusive OR Relative		3
		A	Exclusive OR Absolute		4
COMPARE	COM	Z	Compare to Register Zero Arithmetic/Logical	CC (Note 3)	2
		I	Compare Immediate Arithmetic/Logical		2
		R	Compare Relative Arithmetic/Logical	CC (Note 4)	3
		A	Compare Absolute Arithmetic/Logical		4
ROTATE	RRR		Rotate Register Right w/wo Carry	C, CC, IDC, OVF	2
	RRL		Rotate Register Left w/wo Carry		2

Instruction Set Table (cont.)

	MNEMONIC		DESCRIPTION OF OPERATION	AFFECTS	CYCLES
BRANCH	BCT	R	Branch on Condition True Relative		3
		A	Branch on Condition True Absolute		3
	BCF	R	Branch on Condition False Relative		3
		A	Branch on Condition False Absolute		3
	BRN	R	Branch on Register Non-Zero Relative		3
		A	Branch on Register Non-Zero Absolute		3
	BIR	R	Branch on Incrementing Register Relative		3
		A	Branch on Incrementing Register Absolute		3
	BDR	R	Branch on Decrementing Register Relative		3
		A	Branch on Decrementing Register Absolute		3
	ZBRR		Zero Branch Relative, Unconditional		3
	BXA		Branch Indexed Absolute, Unconditional (Note 5)		3
SUBROUTINE BRANCH/RET.	BST	R	Branch to Subroutine on Condition True, Relative		3
		A	Branch to Subroutine on Condition True, Absolute		3
	BSF	R	Branch to Subroutine on Condition False, Relative		3
		A	Branch to Subroutine on Condition False, Absolute		3
	BSN	R	Branch to Subroutine on Non-Zero Register, Relative	SP	3
		A	Branch to Subroutine on Non-Zero Register, Absolute		3
	ZBSR		Zero Branch to Subroutine Relative, Unconditional		3
	BSXA		Branch to Subroutine, Indexed, Absolute, Unconditional (Note 5)		3
	RET	C	Return from Subroutine, Conditional		3
		E	Return from Subroutine and Enable Interrupt, Conditional	SP, II	3
I/O	WRTD		Write Data	—	2
	REDD		Read Data	CC (Note 1)	2
	WRTC		Write Control	—	2
	REDC		Read Control	CC (Note 1)	2
	WRTE		Write Extended	—	3
	REDE		Read Extended	CC (Note 1)	3
MISC.	HALT		Halt, Enter Wait State	—	2
	NOP		No Operation	—	2
	TMI		Test Under Mask Immediate	CC (Note 6)	3
PROGRAM STATUS	LPS	U	Load Program Status, Upper	F, IJ, SP	2
		L	Load Program Status, Lower	CC, IDC, RS, WC, OVF, COM, C	2
	SPS	U	Store Program Status, Upper	CC (Note 1)	2
		L	Store Program Status, Lower	CC (Note 1)	2
	CPS	U	Clear Program Status, Upper, Masked	F, II, SP	3
		L	Clear Program Status, Lower, Masked	CC, IDC, RS, WC, OVF, COM, C	3
	PPS	U	Preset Program Status, Upper, Masked	F, II, SP	3
		L	Preset Program Status, Lower, Masked	CC, IDC, RS, WC, OVF, COM, C	3
	TPS	U	Test Program Status, Upper, Masked	CC (Note 6)	3
		L	Test Program Status, Lower, Masked	CC (Note 6)	3

NOTES:

1. Condition code (CC1, CC0): 01 if postive, 00 if zero, 10 if negative.
2. Condition code is set to a meaningless value.
3. Condition code (CC1, CC0): 01 if R0 > r, 00 if R0 = r, 10 if R0 < r.
4. Condition code (CC1, CC0): 01 if r > V, 00 if r = V, 10 if r < V.
5. Index register must be register 3 or 3'.
6. Condition code (CC1, CC0): 00 if all selected bits are 1s, 10 if **not** all the selected bits are 1s.

Program Status Word

PSU

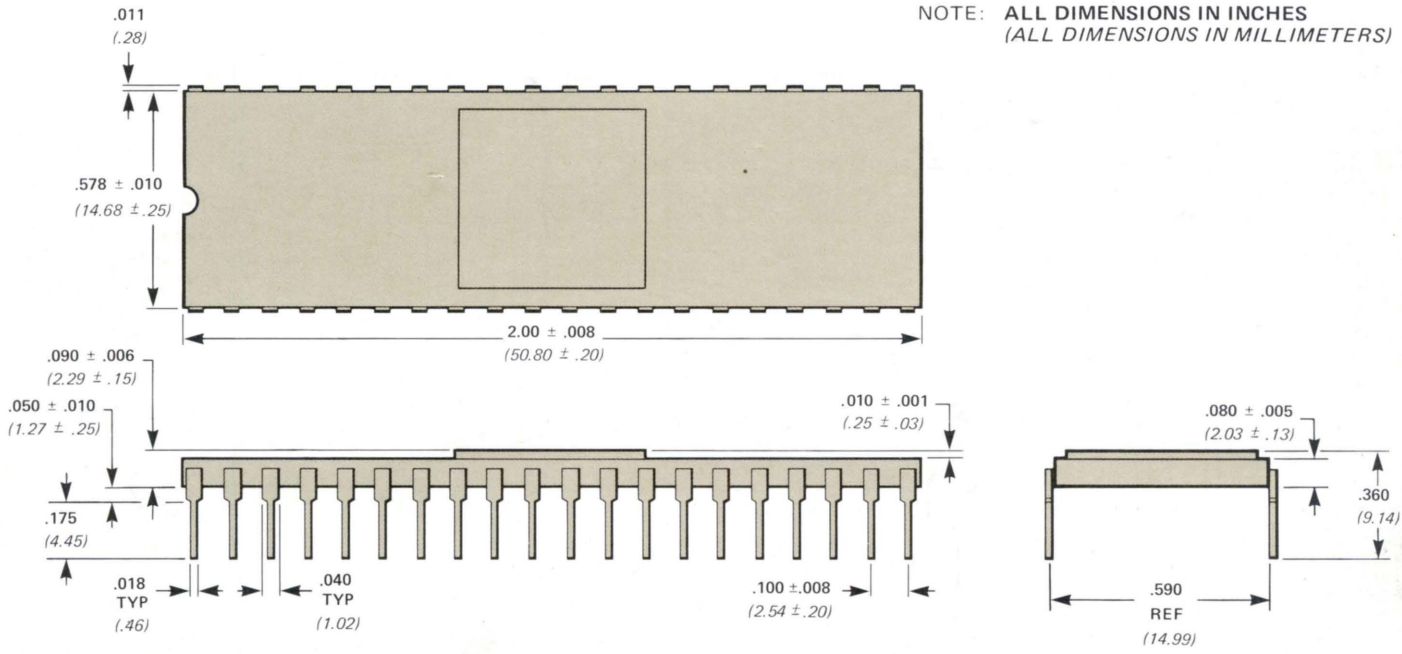
7	6	5	4	3	2	1	0
S	F	II	Not Used	Not Used	SP2	SP1	SP0

PSL

7	6	5	4	3	2	1	0
CC1	CC0	IDC	RS	WC	OVF	COM	C

S	Sense (Pin 1)
F	Flag (Pin 40)
II	Interrupt Inhibit
SP2	Stack Pointer Two
SP1	Stack Pointer One
SP0	Stack Pointer Zero
CC1	Condition Code One
CC0	Condition Code Zero
IDC	Interdigit Cary
RS	Register Bank Select
WC	With/Without Carry
OVF	Overflow
COM	Logical/Arith. Compare
C	Carry/Borrow Bit

Package Dimensions



NOTE: **ALL DIMENSIONS IN INCHES**
(ALL DIMENSIONS IN MILLIMETERS)

Interface Signals

TYPE	PIN	ABBREVIATION	FUNCTION	SIGNAL SENSE
GND	21	GND	Ground	GND = 0
PWR	39	V_{CC}	+5 Volts ± 5%	V_{CC} = 1
INPUT	16	RESET	Chip Reset	RESET = 1 (pulse), causes reset
INPUT	38	CLOCK	Chip Clock	ACTIVE = 1 (10μs max.)
INPUT	37	$\overline{\text{PAUSE}}$	Temp. Halt execution	$\overline{\text{PAUSE}}$ = 0, temporarily halts execution
INPUT	17	$\overline{\text{INTREQ}}$	Interrupt Request	$\overline{\text{INTREQ}}$ = 0, requests interrupt
INPUT	36	$\overline{\text{OPACK}}$	Operation Acknowledge	$\overline{\text{OPACK}}$ = 0, acknowledges operation
INPUT	1	SENSE	Sense	SENSE = 0 (low) or SENSE = 1 (high)
INPUT	15	$\overline{\text{ADREN}}$	Address Enable	$\overline{\text{ADREN}}$ = 1 drives into third state
INPUT	25	$\overline{\text{DBUSEN}}$	Data Bus Enable	$\overline{\text{DBUSEN}}$ = 1 drives into third state
IN/OUT	26-33	DBUS0–DBUS7	Data Bus	DBUSn = 0 (low), DBUSn = 1 (high)
OUTPUT	2-14	ADR0–ADR 12	Address 0 through 12	ADRn = 0 (low), ADRn = 1 (high)
OUTPUT	19	ADR13 or E/$\overline{\text{NE}}$	Address 13 or Extended/Non-Extended	$\overline{\text{Non-Extended}}$ = 0, Extended = 1
OUTPUT	18	ADR14 or D/$\overline{\text{C}}$	Address 14 or Data Control	$\overline{\text{Control}}$ = 0, Data 1
OUTPUT	24	OPREQ	Operation Request	OPREQ = 1, requests operation
OUTPUT	20	M/$\overline{\text{IO}}$	Memory, IO	$\overline{\text{IO}}$ = 0, M = 1
OUTPUT	23	$\overline{\text{R}}$/W	Read/Write	$\overline{\text{R}}$ = 0, W = 1
OUTPUT	40	FLAG	Flag Output	FLAG = 1 (high), FLAG = 0 (low)
OUTPUT	34	INTACK	Interrupt Acknowledge	INTACK = 1, acknowledges interrupt
OUTPUT	35	RUN/$\overline{\text{WAIT}}$	Run/Wait Indicator	RUN = 1, $\overline{\text{WAIT}}$ = 0
OUTPUT	22	WRP	Write Pulse	WRP = 1 (pulse), causes writing

For order information, see page 2.

Printed in U.S.A.

1275 Hammerwood Avenue ☐ Sunnyvale ☐ California 94086 ☐ Phone: (408) 734-4330 ☐ TWX: 910-339-9369