DATA SET 205C TYPE TRANSMITTER-RECEIVER USED ON PRIVATE SERVICE SYSTEMS SWITCHING SYSTEM NO. 307 SUPPLEMENTAL INFORMATION

1. GENERAL

1.01 This section covers the detailed description and operation of the data sets, as well as testing of the individual circuit cards. The Data Set 205C type replaces Data Set 205A type which is rated manufacture discontinued. The 205C can directly replace the 205A if interface pins 11 and 12 are not used.

1.02 The circuit description and schematic drawings are CD- and SD-1D087-01, and SD-1D060-01.

1.03 Data Set 205C type uses synchronous 4-phase modulation techniques for transmission of serial binary data at 2400 bps (full-speed) or 1200 bps (half-speed).

1.04 Transmission is over voice frequency circuits using an 1800-cps carrier frequency. The line signal spectrum is essentially confined in the band extending from 750 to 2850 cps.

1.05 Data set clock signals supplied to the customer are synchronous with transmit and receive data. These clocks are selected by the customer and, through an external connection, are at the data rate or twice the data rate.

1.06 Two Data Set 205C type units may be interconnected to form a 4-wire regenerative repeater. Timing and data signals are exchanged between the two sets through customer connector B.

2. DATA SET TRANSMITTER

2.01 Incoming serial data bits are delivered to the transmitter through the send data (SD) circuit, the data transitions being synchronous with positive-going transitions of the transmitter clock (SCT). These are examined in pairs (dibits) and used to control the 4-phase modulation of the carrier.

CARRIER CONTROL

A. Four-Wire Operation

Continuous Carrier

2.02 In 4-wire operation, carrier may be placed continuously on by strapping terminals 1 and 2 on card 019. When in a continuous carrier mode, confirm (CON) is placed off by the customer. A continuous clear-to-send (CS) on signal is given by the data set. No 1000 quad-bit SYNC code is generated.

2.03 The continuous carrier mode provides customer operation without waiting for clear-to-send on before each transmission. In return, the customer must provide a minimum number of crossings per second of send data (SD) for receiver synchronization whether transmitting data or not.

Carrier Controlled by Request-to-Send

2.04 Carrier may be turned on and off with request-to-send. In this mode, the strap from terminal 1 to 2 on card 019 must be disconnected.

2.05 A 1000 quad-bit synchronizing code is now transmitted for a period not less than 638.33 msec whenever request-to-send is placed on. After the waiting period, which may be controlled by the confirm circuit, a clear-to-send on signal is given. This indicates that the remote receiver has had sufficient time to synchronize and that data may now be transmitted.

2.06 The customer must provide a minimum number of crossings per second of send data, for receiver synchronization, while clear-to-send is on.

TRANSMITTER TIMING

Note: When the data set clocks have been selected to be at the data rate, transmitter timing may be derived from either the internal crystal oscillator or a customer-supplied external source (2400-cps square wave or send data). With double-speed clocks, external timing is not provided. When the data set is used as a regenerator, external timing is supplied by another data set.

A. Data Set Supplied

2.07 Internal timing may be used with both normal and double-speed clocks. In this mode, a strap must be connected from terminal 3 to 4 on card 019. This strap grounds the external clock (SCTE) input to prevent false timing corrections due to noise.

B. Customer Supplied

2.08 External timing may be used only with normal speed clocks. In this mode, the strap from terminal 3 to 4 on card 019 is disconnected. A square-wave clock or send data is then applied to the external timing (SCTE) input and used to generate discrete phase corrections of the transmitter clock.

C. Regenerator Timing

2.09 Two data sets are required to form a regenerative repeater. In this case, each data set transmitter derives external timing from the receiver of the opposite data set. A square-wave clock from the SCR output of each receiver is applied to the external timing (SCTE) lead of the opposite transmitter. In this mode, the strap from terminal 3 to 4 on card 019 is disconnected.

3. DATA SET RECEIVER

3.01 The data set receiver demodulates the received line signal to deliver serial data (RD) and a synchronous clock (SCR) to the connecting data equipment or another data set in case of regeneration.

3.02 The input to the receiver is an AGC circuit with a 30-db dynamic range and an input sensitivity of —39 (±1) dbm. In the event the received signal is sufficiently greater than the basic receiver sensitivity, loss pads of 5, 10, or 15 db may be set to reduce sensitivity of the receiver to noise or speech interference.

4. INTERFACE AND LINE CIRCUIT CONNECTORS

4.01 Four multiple-pin connectors provide for all interface and line circuit connections for the data set. All connectors are mounted on the front of the data set.

Note: Lightning protection is ***not*** provided on any interface circuit. Therefore, cables carrying these circuits may not be used out-of-doors.

CONNECTOR FUNCTION

4.02 CUSTOMER A connector carries the data and clock interface circuits, the clock rate (SCX2) circuit, the data set ready (DSR-DSRX2) circuit, frame ground, and signal ground. The DSR-DSRX2 circuits are strapped by the mating customer-supplied connector.

4.03 CUSTOMER A connector is specifically for use with government equipment. The data and clock interface circuits are capable of operation over twisted-pair cables several hundred feet long providing resistance and ground potential requirements are met.

4.04 CUSTOMER B connector carries the control interface circuits, the data and clock interface circuits, the clock rate selection circuit, frame ground, and signal ground. It is for use with cable lengths up to 50 feet. It is also used for testing purposes.

4.05 The 2-WIRE connector carries the single transmit and receive pair for use in 2-wire operation. The strap connections in the mating connector on the 4A1 cord connect the data set for 2-wire operation.

4.06 The 4-WIRE connector carries the transmit and receive line pairs for 4-wire operation. The same strap connections in the mating connector on the 4A1 cord connect the data set for 4-wire operation.

5. DATA SET CONTROL INTERFACE

5.01 Control interface signals are accepted or delivered to the data set through the CUSTOMER B connector.

5.02 In addition, +18 and −18 volts, each in series with 681 ohms, are supplied by the data set at CUSTOMER B connector for external use in generating control signals.

5.03 All drivers and terminators used in the control interface conform to EIA Standard RS-232A and are designed to work with cables up to 50 feet in length.

5.04 In the event of a power failure on either side of the interface, all control interface signals will be considered in the off condition at zero volts. The source impedance of all driving circuits is greater than 300 ohms to signal ground with power off.

CIRCUIT AND SIGNAL DEFINITIONS FOR THE CONTROL INTERFACE

A. Control Drivers

5.05 When the data set is the signal source, the interface circuit is a driver. Control drivers will deliver a +6.8 (±1.2) volt ON signal, or a −6.2 (±1.2) volt OFF signal to a 3000-ohm (or higher) resistive load.

B. Control Terminators

5.06 When the data set is the signal acceptor, the interface circuit is a terminator. Control terminators recognize +3 to +25 volts as an ON signal and −3 to −25 volts as an OFF signal without regard to rise or fall time of transitions.

5.07 Shunt capacity to signal ground on all control terminators, measured at the interface and including up to 50 feet of cable, shall not exceed 2500 uuf.

5.08 Input resistance to all control terminators is greater than 3000 ohms. For reasons given below, the input resistance for the SCTE terminator is greater than 30,000 ohms.

(a) A high input resistance on SCTE allows up to 10 externally-timed data sets to be driven from the SCT output of one internally-timed data set.

(b) When using send data as the external-timing source (by strapping SD to SCTE), a high SCTE input resistance prevents loading the MIL. STD 188B terminator used for send data.

DESCRIPTION OF CONTROL SIGNALS

A. Request-to-Send (RS) — Terminator

Continuous Carrier Operation (4-Wire Mode Only)

5.09 When the data set has been strapped for continuous carrier, the RS circuit is disabled.

Carrier Controlled by Request-to-Send (4-Wire or 2-Wire Mode)

5.10 When the data set is not strapped for continuous carrier, carrier is turned ON and OFF with request-to-send.

(a) ***Four Wire Operation:*** In this mode, an RS ON signal turns on carrier and initiates the RS-CS period during which the synchronizing code is transmitted. At the end of this period, a CS ON is given by the data set to indicate that data may be transmitted. RS must be held ON for the full duration of the message and for the entire interval of the last bit to be transmitted.

(b) ***Two-Wire Operation:*** In the 2-wire mode, placing RS ON connects the transmitter to the line, turns on carrier and initiates the RC-CS period, during which the synchronizing code is transmitted. At the same time, the data set receiver is connected to provide local copy on the receive data circuit. RS must be held on for the full duration of the message and for the entire interval of the last bit to be transmitted. When RS is turned off the data set turns off the carrier, disconnects the transmitter, and connects the receiver to the telephone line.

B. Clear-to-Send (CS) — Driver

5.11 A CS ON signal indicates that transmission of the synchronizing pattern has ended and that the data set will accept and transmit data. CS goes OFF when RS is turned off.

5.12 The RS-CS time period depends on the state of the confirm circuit as described below:

Case 1 — Confirm OFF

5.13 With confirm OFF, an RS on signal initiates a 640 $\binom{+0.00}{-1.67}$ msec timing period that ends with CS ON being given. This interval is adequate for a receiver to acquire synchronization.

Case 2 — Confirm ON

5.14 With confirm ON, an RS on signal is prevented from initiating the 640 $\binom{+0.00}{-1.67}$ msec timing period until the receiver has detected a synchronizing pattern from a remote data set. This indicates that a remote receiver is connected to the line.

C. Confirm (CON) — Terminator

5.15 The function of the confirm circuit has been described in B. Clear-to-Send (CS) — Driver. The confirm circuit is for use in a 4-wire mode only. When operating 2-wire, confirm must be placed OFF by the customer.

D. Data Carrier Detector (COO) — Driver

5.16 An ON condition of C00 indicates that telephone line power is being detected in the receiver. Excessive line noise or speech, as well as carrier, can operate this circuit. An OFF condition indicates that line power is not being detected. When C00 is in the OFF condition the receive data (***RD***) lead is held at the negative voltage level. Sensitivity of the C00 circuit is —39 dbm (±1 db) with random signal input.

E. Data Speed Select (SS) — Terminator

5.17 The bit-per-second speed of the data set is controlled by SS. An SS ON signal causes the data set to operate at 2400 bps, while an OFF signal causes the data set to operate at 1200 bps. The latter speed reduces the bandwidth of the line signal and gives increased probability of successful transmission over other facilities than those normally used.

5.18 SS with RGRN OFF also controls the rate of the clocks (SCT and SCR) supplied to the connecting data equipment in accordance with the bit rate. These clocks can run either at the data rate or at twice the data rate.

5.19 It is necessary that both the local and remote data sets be set for the same bit rate.

F. Data Set Ready (DSR) — Driver

5.20 An ON condition of DSR indicates that the data set is not in a test mode and that power is ON in the data set. DSR is OFF when the data set is in a test mode, and is at zero voltage whenever power is off in the data set. The output impedance is not less than 300 ohms for any condition.

5.21 The DSR circuit is to be used only when data and clock signals are accepted or delivered through CUSTOMER B connector. When CUSTOMER A connector is used for data and clock signals, the ***DSRX2*** lead is to be used in place of ***DSR*** (see section below, concerning the DSRX2 circuit).

G. Data Set Ready X2 DSRX2) — Driver

5.22 The DSRX2 circuit description is identical to that given above for DSR, except that DSR passes through a strap provided by the customer in the plug connected to CUSTOMER A connector before appearing in CUSTOMER B connector as DSRX2. Thus, if the plug is out, the data set ready signal cannot be delivered.

5.23 DSRX2 is for use only when data and clock signals are being provided through CUSTOMER A connector.

H. Remote Test (RMT) — Terminator

5.24 The RMT circuit permits a data set to be tested from a 904E Data Test Center when the data set is in the 4-wire mode. The data set is placed in this mode by the customer upon request of the test center. When RMT is ON the data set will:

- Disconnect all data and timing interface circuits.
- Disconnect all control interface circuits except RMT, DSR (DSRX2), SIG GND, and DT1.
- Give a DSR (DSRX2) OFF indication to the control interface.
- Set up the local data set for remote testing.

5.25 With the data set in the remote test mode, the remote test center may check the following:

- The function of the ***CON*** lead.
- The RS-CS time interval.
- Data performance at 2400 and 1200 bps.
- Local oscillator accuracy.
- Effectiveness of the receiver synchronization recovery circuits.

5.26 An OFF condition applied to RMT removes the data set from the remote test mode and restores all circuits.

5.27 When operating the data set in a 2-wire mode, the remote test feature is not provided and the ***RMT*** lead will not accept any signal.

I. External Timing (SCTE) — Terminator

> *Note:* External timing may not be used when the data set clocks, SCT and SCR, are at twice bit rate. If external timing is not used, an internal strap connection must be made from terminal 3 to 4 on card 019. When external timing is used, the strap must be disconnected.

5.28 The data set may be synchronized with an external source by using the SCTE circuit. The input may be either a square wave at the bit rate or send data (SD) itself. (To use SD as the input to SCTE, the customer must supply a strap between pins 2 and 24 on CUSTOMER B connector.) In either case, the required minimum frequency accuracy of the external source is ±0.01 percent.

5.29 The transmitter is initially synchronized with SCTE by application of the square-wave source or a send data dotting code (alternate 0 — 1) for at least 40 msec before RS is turned ON. Once the 40-msec period has elapsed and RS has been turned ON, it is necessary to ensure at least 13 positive transitions of SCTE per second to keep the transmitter in synchronization.

5.30 The maximum synchronization dropout time depends on both the transmitter and receiver clock frequency tolerances. However, since the receiver clock frequency tolerance is fixed at ±0.0005 percent, the maximum dropout time will then vary primarily with the transmitter clock frequency tolerance. The maximum dropout time of 6.0 seconds for a transmitter timing tolerance of ±0.0005 percent decreases linearly to 0.57 seconds for a tolerance of ±0.01 percent.

J. Regeneration (RGRN) — Terminator

> *Note:* The RGRN interface lead on pin 11 of CUSTOMER B connector must be connected to a negative voltage (−3 to −25 volts) unless the data set is to be used as a regenerative repeater. If the data set is used as a regenerator, then SS and RGRN must be connected to a positive voltage (+3 to +25 volts).

5.31 The RGRN circuit permits the data set to be operated as a regenerator. Two data sets are required for each 4-wire regenerative repeater. Interconnections between the two data sets are established through the CUSTOMER B connectors. Fig. 1 and 2 show typical regenerative repeater connections. Both RGRN and the SS interface leads must be turned ON when the data set is used as a regenerator. The frequency of the receiver clock signal appearing at SCR is 1200 cps (receiver dibit clock). Received data (RD) is connected to the send data (SD) input of a transmitter. SCR is connected to the external timing input (SCTE) of a transmitter to keep the transmitter dibit clock "in phase" with the receiver dibit clock. This maintains the identity of the A and B data bits and guarantees that the repeated line signal is identical to the received line signal at a regenerative repeater.

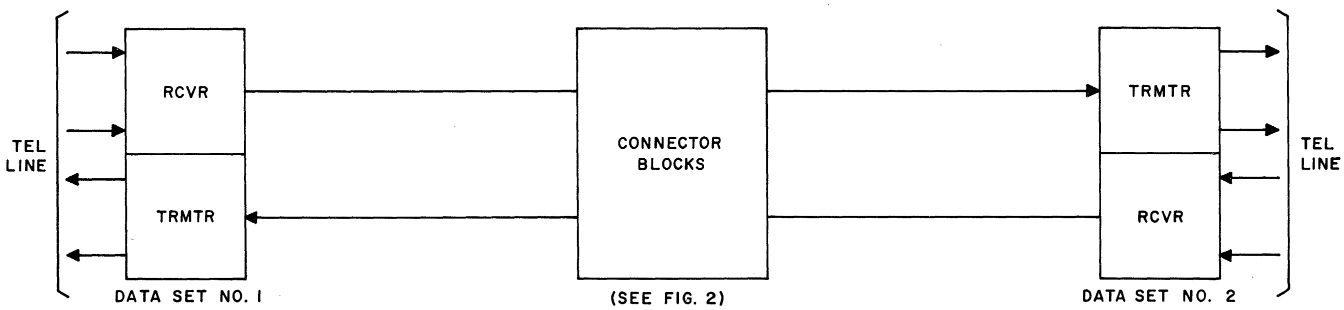

Fig. 1 — Regeneration Connections, Block Diagram

5.32 When RGRN is OFF, (for normal clocks) the frequency of the receiver clock (SCR) is the bit rate frequency; either 2400 cps or 1200 cps as determined by the condition of SS.

5.33 The following table summarizes the clock rates appearing on the SCR and SCT leads as a function of the control leads RGRN, SS, and SCX2.

TABLE

CLOCK RATES

SS	RGRN	SCX2 STRAPPED TO TERM. 7	CLOCK FREQ. (CPS)	
			SCT	SCR
ON	OFF	NO	2400	2400
ON	OFF	YES	4800	4800
OFF	OFF	NO	1200	1200
OFF	OFF	YES	2400	2400
ON	ON	NO	2400	1200

K. Prepare Receiver (PR) — Driver

Note: The PR circuit is provided by printed circuit boards located at positions 049 and 050.

5.34 The PR circuit is used to provide an indication to the control equipment after the synchronizing code has been detected and completed and the received data is continuously positive for at least 85 milliseconds. The customer must supply the positive send data at the transmitting end. PR is turned OFF when a negative voltage occurs in the received data or C00 is in the OFF condition. PR remains OFF until C00 is in the ON condition and the received data is continuously positive for at least 85 milliseconds.

6. DATA AND CLOCK INTERFACE

6.01 Four interface circuits are provided through both customer connectors for the data and clock signals. These signals are accepted or delivered by the data set through cable drivers and cable terminators designed to meet MIL. STD 188B.

6.02 Twisted-pair lengths up to several hundred feet may be used. The primary factor restricting the cable length is the maximum resistance of the four parallel ***SIG GND*** leads that may safely exist between the data set signal ground and the ac power ground.

CABLE DRIVER AND CABLE TERMINATOR

A. Cable Driver

6.03 The cable driver delivers an open circuit output voltage of 6.1 volts (±5 percent), positive and negative, through less than 100 ohms source impedance.

6.04 The rise and fall times of the output wave shape are specified by MIL. STD 188B to be within 5 to 6 percent of the duration of the unit interval at the applicable modulation rate. In this case, the rise and fall times have been fixed by constant resistance RLC circuits to be approximately 11 usec. This value is approximately 5.5 percent of the half-period of a 2400-cps square wave.

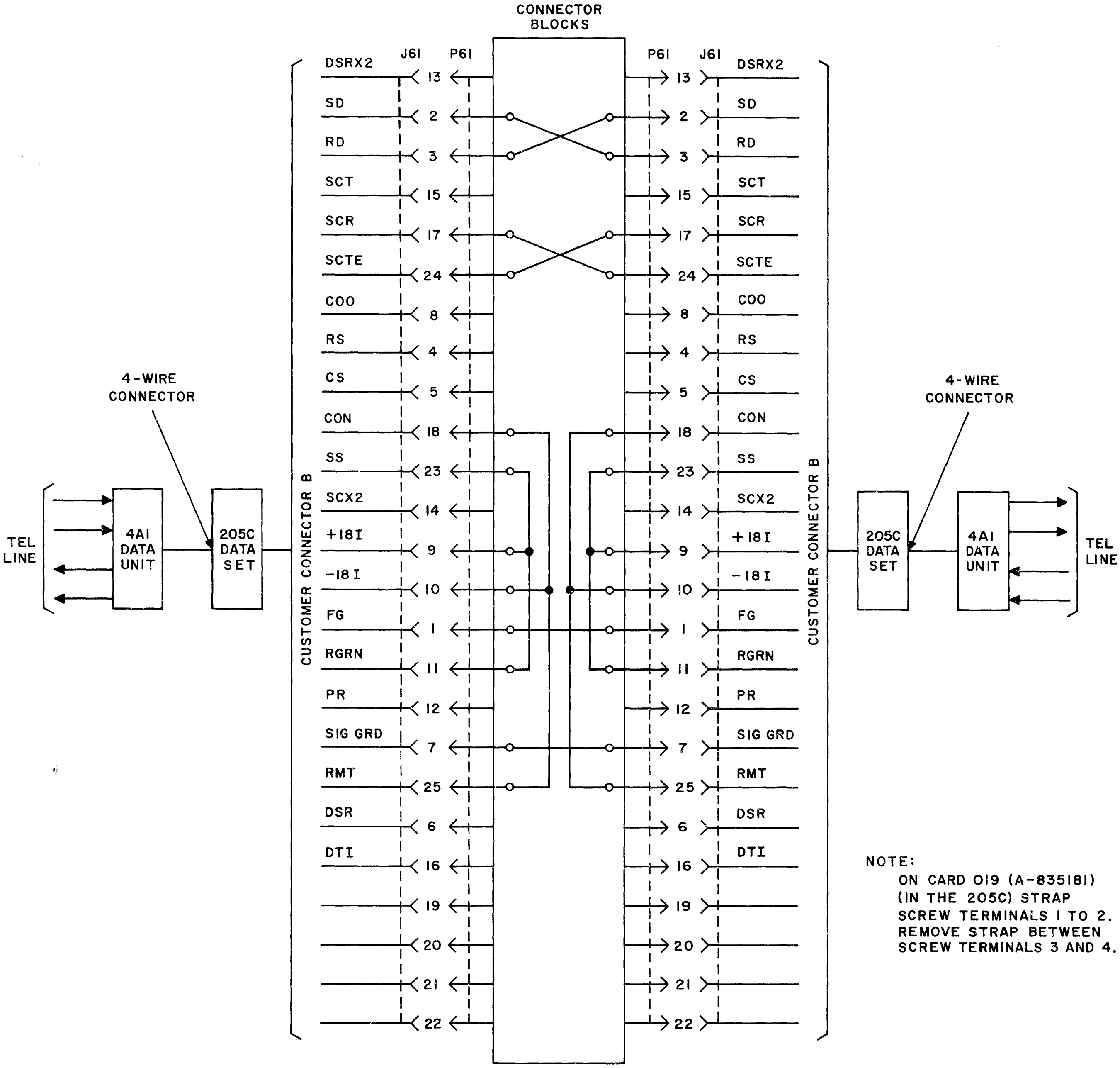

Fig. 2 — Regeneration Connections At Connector Blocks

B. Cable Terminator

6.05 The cable terminator is a bipolar detector with a potentiometer that is factory set to meet the balance requirement of MIL. STD. 188B.

6.06 The cable terminator has a minimum input resistance in excess of 5000 ohms. The input capacitance is that due to wiring and is less than 100-uuf shunt capacity to signal ground.

CLOCK SIGNALS

6.07 The data set provides two square-wave clocks (SCR and SCT) to the connecting data equipment for use in synchronizing the connecting equipment with the data set. The rate of these clocks is dependent on the data rate selected and the clock rate selected.

A. Clock Rate Selection

6.08 SCR and SCT may be chosen to be at the data rate (2400/1200 cps) or at twice the data rate (4800/2400 cps) by a strap connection on either of the customer connectors. To select double rate clocks (4800-2400 cps), pins 7 (SIG GRD) and 14 (SCX2) are strapped on either customer connector. For normal rate clocks (2400/1200 cps) no strap connection is made.

6.09 The rate is used with government equipment, commercial business machines, and during data set testing.

6.10 For regeneration, SCR is at 1200 cps and SCT is at 2400 cps.

B. Serial Clock Transmit (SCT) — Driver

6.11 SCT is a square-wave clock provided by the data set at the data rate (or twice the data rate) for use by the customer in synchronizing send data with the transmitter timing.

6.12 When external transmitter timing is used, jitter will be present in the SCT signal due to discrete phase corrections made in the transmitter timing circuit.

6.13 Each correction advances or delays a positive transition of SCT by approximately 8.7 usec (1/48 of a 2400-cps period). Once initial phase synchronization has been obtained, the correction rate is determined by the frequencies of the internal oscillator and the external timing source.

6.14 The maximum correction rates for maintenance of synchronization (exclusive of noise induced corrections) to be expected after initial phase synchronization has been obtained are given below. These rates are given as a function of the external timing accuracy and assume:

(a) an internal clock of 2400 ±0.0005 cps,

(b) an external clock at 2400 cps, and

(c) a positive transition rate of SCTE that is at least equal to the maximum correction rate given.

EXTERNAL CLOCK ACCURACY	MAXIMUM CORRECTIONS PER SECOND
PERCENT	
±0.01	12.2
±0.001	1.7
±0.0005	1.2

C. Serial Clock Receive (SCR) — Driver

6.15 SCR is a square-wave clock provided by the data set at the data rate (or twice the data rate). Positive transitions of SCR are coincident with transitions of receive data.

6.16 Jitter will be present in the SCR signal due to discrete phase corrections made in the receiver timing circuit. Corrections never occur more often than one every 11.7 msec (every 28 cycles of a 2400-cps clock) and are such that each correction advances or delays a positive transition of SCR by approximately 17.4 usec (1/24 of a 2400-cps clock period). After initial phase synchronization is obtained, additional corrections will be necessary only when the SCR signal drifts out of phase due to local oscillator drift, corrections generated by noise, or a change in the line delay. Consequently, corrections of SCR should occur considerably less often than one every 11.7 msec during normal operation. For example, corrections due to oscillator drift will occur at a rate of approximately 6 per second if the transmitter clock variation is ±0.01 percent.

DATA SIGNALS

A. Send Data (SD) — Terminator

6.17 Serial data to be transmitted is to be presented to the data set on the SD circuit synchronous with SCT. With SCT at twice the data rate, transitions of SD must occur within ±80 usec of every other positive transition of SCT. When SCT is at the data rate, transitions of SD must occur within ±160 usec of each positive transition of SCT (all measurements taken at CUSTOMER B connector) when used for transmitter timing.

6.18 The rise and fall times of the send data input should be no greater than 11 usec.

6.19 A negative voltage level is defined as the binary 1 or mark state.

Receiver Clock Recovery

6.20 The data set uses a zero-crossing clock recovery system that requires the number of crossings per second of send data to be greater than some minimum value in order to keep the receiver in synchronization in the presence of clock variation and noise, and to restore the receiver clock after a dropout. The definition of a crossing depends on the bit rate of the data set.

(a) For a 2400-bps rate, a crossing is defined as a change in a bit state with respect to the state of the second previous bit. Thus a dot pattern (-101010-) contains no data crossings and may not be used. Quad-bit codes such as 1000, 1100, 1011, etc, are necessary to provide crossings.

(b) For a 1200-bps rate, a crossing is defined as a change in the bit state with respect to the previous bit. Therefore, only the steady 0000 or 1111 codes are prohibited.

Data Crossing Rates

6.21 Due to the transmitter clock variation and noise, a minimum number of crossings per second must be provided to hold the receiver clock; after a dropout a higher crossing rate should be used.

(a) ***Minimum Crossing Rate:*** The minimum crossing rate per second necessary to hold the receiver clock in synchronization depends primarily on the accuracy of the transmitter timing source (the receiver clock accuracy is fixed at ±0.0005 percent by the internal crystal oscillator).

TRANSMITTER TIMING ACCURACY	MINIMUM CROSSING RATE PER SECOND
PERCENT	
±0.0005	10
±0.0010	14
±0.0050	46
±0.0100	90

(b) ***Crossing Rate Versus Restoral Time:*** After a dropout period, the receiver clock restoral time will depend primarily on the crossing rate of the received data. Therefore, to ensure remote receiver clock restoral after dropout, the local customer shall provide a send data crossing rate that exceeds the minimum values given above. The figures given assume a worst-case transmitter clock variation, i.e., ±0.01 percent.

CROSSINGS PER SECOND	MINIMUM RESTORAL TIME
	SECONDS
150	1.75
300	0.53
600	0.22

B. Receive Data (RD) — Driver

6.22 Serial data obtained from demodulating the received line signal is delivered to the interface on the RD circuit. Transitions of RD are coincident with positive transitions of SCR. The ***RD*** lead is clamped at the negative voltage level (binary 1 or mark state) whenever the received input power is below the padded receiver sensitivity.

C. Grounding

6.23 The data set frame ground (FG) and the ac power third-wire ground are connected in the data set. However, data set signal ground (SG) is connected to FG and the ac power ground through a wire strap mounted on the connector mounting plate. This strap must be cut and removed only when the data set is to be connected through CUSTOMER A connector. In all other cases such as testing or when data and clock signals are taken through CUSTOMER A connector, a strap must be present so that SG is connected to FG and ac power ground.

7. POWER, TEMPERATURE, AND HUMIDITY REQUIREMENTS

7.01 AC input: 117 volts ±10 percent, 50 watts, 60 ±0.45 cps.

7.02 Ambient temperature: 50° to 104 F.

7.03 Relative humidity range: 20 to 95 percent.

8. VOICEBAND TRANSMISSION REQUIREMENTS

8.01 Suppressed carrier frequency: 1800 cps.

8.02 Transmitter:

(a) Output power: —9, —6, —3, or 0 dbm.

(b) Output impedance; 600 ohms for 4-wire, 900 ohms for 2-wire.

8.03 ***Receiver:***

(a) Input impedance; 600 ohms for 4-wire, 900 ohms for 2-wire.

(b) Input Power;

PAD LOSS (DB)	MINIMUM INPUT POWER (DBM)	MAXIMUM INPUT POWER (DBM)
0	—38	—10
5	—33	—5
10	—28	0
15	—23	+5

(c) Automatic gain control range; 30 db.

(d) Derived clock lock-in time; 0.6 second maximum following request-to-send, when using the transmitter internally generated 1000 quadbit code.

(e) Minimum data crossing per second; 10, when the transmitter furnishes all timing or when external clock accuracy is ±0.0005 percent.

8.04 ***Impairment Tolerances:***

(a) Delay distortion; 4 db SNR impairment for band limited random noise. This means that the SNR of a back-to-back connection would be degraded by 4 db when the following amounts of delay distortion are inserted in the circuit. The same amount of band limited random noise is present under both conditions.

FREQ. RESPONSE	LOSS (DB)
300 to 500 cps	—2 to +6
501 to 2800 cps	—1 to +3
2801 to 3000 cps	—2 to +6

(b) Attenuation distortion; 10 db maximum 600 to 3000 cps.

(c) Sudden net loss variation; ±4 db.

(d) Circuit net loss; adjusted so that the padded receiver input is between —39 dbm (±1 db) and —10 dbm.

(e) Frequency translation error;

- 10 cps causes 1 db SNR impairment.
- 25 cps causes 3 db SNR impairment.

(f) Signal-to-noise ratio; 20 db minimum.

(g) Near-end crosstalk; 30 db below received signal.

9. PACKAGING

9.01 The Data Set 205C is designed to mount in a 23-inch relay rack. Its over-all dimensions are 22.93 inches wide by 17.97 inches high by 8.32 inches deep.

10. INDIVIDUAL CPS CHECKS NOR GATE TEST

A. Testing Equipment

1\. — NOR gate test set such as shown in Fig. 3.

1 — Oscilloscope, Tektronix 535A with type 53/54C plug-in unit (or equivalent).

2 — Probes, Tektronix P410 (10X) (or equivalent).

1 — Square-Wave generator, Hewlett-Packard 211A (or equivalent).

1 — Mercury relay, WECo 291A (or equivalent).

1 — DC voltmeter, 20,000 ohm/volt, ±3 percent.

1 — DC milliammeter, ±5 percent.

3 — Switches:

1 — DPDT.

1 — 5-wafer, 10-position, rotary.

1 — 4-wafer, 5-position, rotary.

4 — Resistors:

1 — 100 ohms, (±1 percent), 1 watt, WECo 144E (or equivalent).

1 — 316 ohms, ±1 percent), 0.5 watt, WECo 145A (or equivalent).

1 — 121 ohms, (±1 percent), 1 watt, WECo 144E (or equivalent).

1 — 2150 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

B. Power Requirements

+18.0 (±0.5) volts dc — 200 ma

+2.5 (±0.1) volts dc — 40 ma

+6.0 (±0.3) volts dc — 20 ma

C. Testing Procedure

10.01 ***Diode Short Test:***

(a) This test is to be made before the card to be tested is inserted into the test set.

(b) Ground pin 1 and apply +6.0 (±0.3) volts dc to test point 8 of the card; current drawn should be less than 3.0 ma dc.

10.02 ***Zener Voltage Test:***

(a) Insert the card into the test set and connect +18.0 (±0.5) volts dc to J10.

(b) The voltage between test point 7 and ground, when measured with the voltmeter, should be +6.2 (±0.6) volts dc.

10.03 ***Turn-On Time:***

(1) Connect the test circuit as shown in Fig. 3.

Note: Consult Table A to determine which gate and corresponding input resistance are under test.

(2) Set the frequency of the square-wave generator between 40 and 50 cps.

(3) Set the DPDT switch to position 1.

(4) Set the GATE and TEST FUNCTION selector to position 1.

(5) Set the EXT SYNC TRIGGER to the (+) positive position.

(6) Rotate the GATE selector through positions 1 to 10. At each position the input and output step shall be as specified in Fig. 4.

(7) Set the TEST FUNCTION selector to position 2. Rotate the GATE selector through positions 1 to 8. Observe output as in (6). Time base measurements need not be made.

(8) Set the TEST FUNCTION selector to position 3. Rotate the GATE selector through positions 1 to 6. Observe output as in (6). Time base measurements need not be made.

(9) Set the TEST FUNCTION selector to position 4. Rotate the GATE selector through positions 1 to 2. Observe output as in (6).

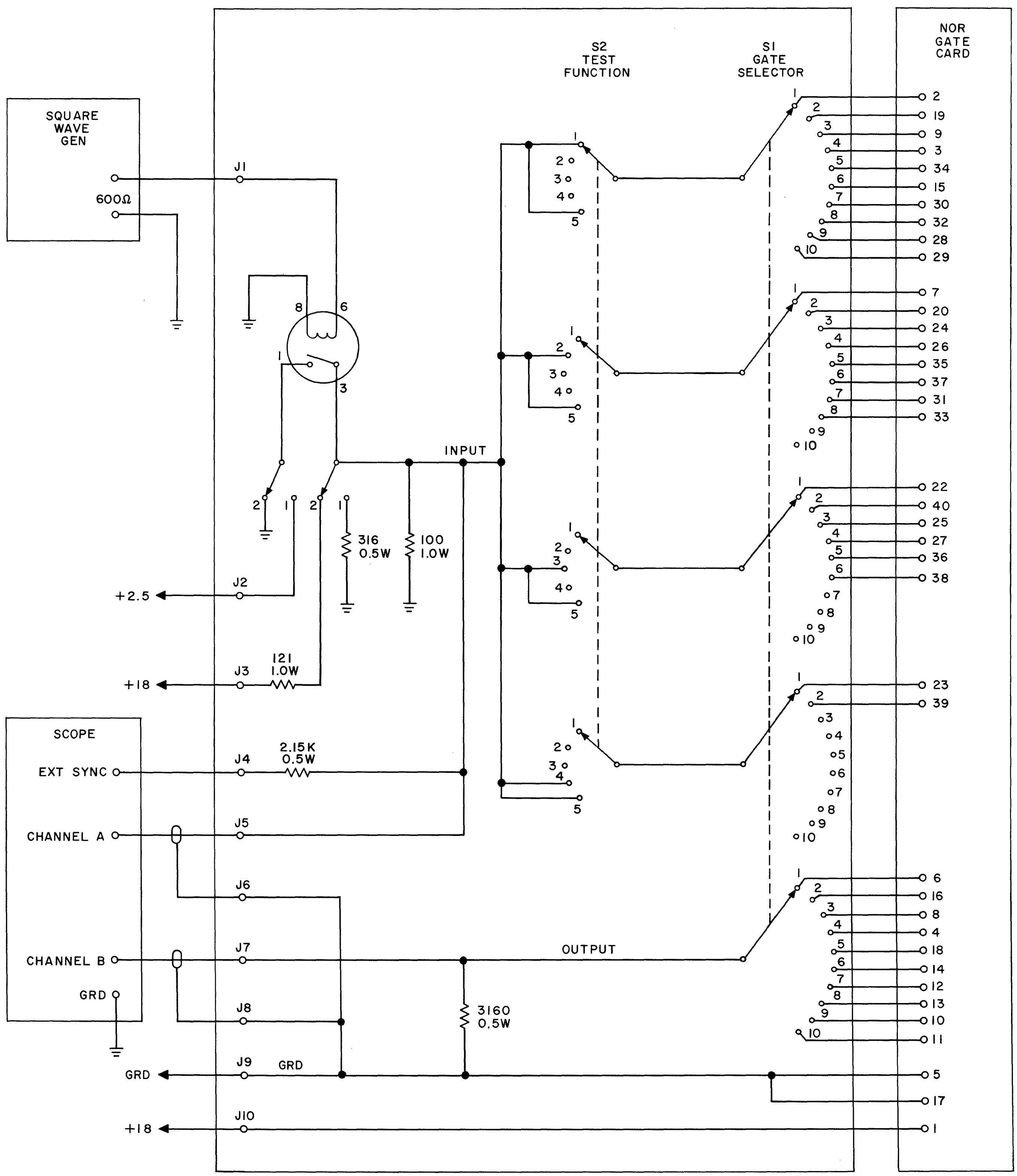

Fig. 3 — NOR Gate Test Set

TABLE A

KEY TO COMPONENTS UNDER TEST AT EACH POSITION OF TEST SET SWITCHES

TEST FUNCTION POSITION	GATE SELECTOR POSITION	INPUT TERMINAL	INPUT RESISTOR	TRANSISTOR	OUTPUT TERMINAL
1	1	2	R1	Q1	6
	2	19	R23	Q10	16
	3	9	R5	Q2	8
	4	3	R8	Q3	4
	5	34	R17	Q8	18
	6	15	R20	Q9	14
	7	30	R13	Q6	12
	8	32	R15	Q7	13
	9	28	R11	Q4	10
	10	29	R12	Q5	11
2	1	7	R2	Q1	6
	2	20	R24	Q10	16
	3	24	R6	Q2	8
	4	26	R9	Q3	4
	5	35	R18	Q8	18
	6	37	R21	Q9	14
	7	31	R14	Q6	12
	8	33	R16	Q7	13
3	1	22	R3	Q1	6
	2	40	R25	Q10	16
	3	25	R7	Q2	8
	4	27	R10	Q3	4
	5	36	R19	Q8	18
	6	38	R22	Q9	14
4	1	23	R4	Q1	6
	2	39	R26	Q10	16
5	1	2, 7, 22, 23	R1, R2, R3, R4	Q1	6
	2	19, 20, 40, 39	R23, R24, R25, R26	Q10	16
	3	9, 24, 25	R5, R6, R7	Q2	8
	4	3, 26, 27	R8, R9, R10	Q3	4
	5	34, 35, 36	R17, R18, R19	Q8	18
	6	15, 37, 38	R20, R21, R22	Q9	14
	7	30, 31	R13, R14	Q6	12
	8	32, 33	R15, R16	Q7	13
	9	28	R11	Q4	10
	10	29	R12	Q5	11

10.04 ***Gate Turn-Off Time:***

(1) Set the DPDT switch to position 2.

(2) Set the EXT SYNC TRIGGER to (−) negative.

(3) Rotate the GATE selector through positions 1 to 10. The input and output steps shall be as specified in Fig. 5 at each position.

COMPLEMENTARY FLIP-FLOP TEST

A. Testing Equipment

1 — OFF test set such as shown in Fig. 6.

1 — Oscilloscope, Tektronix 535A with plug-in unit-type 53/54C or C-A (or equivalent).

2 — Probes, Tektronix P410 (10X) (or equivalent).

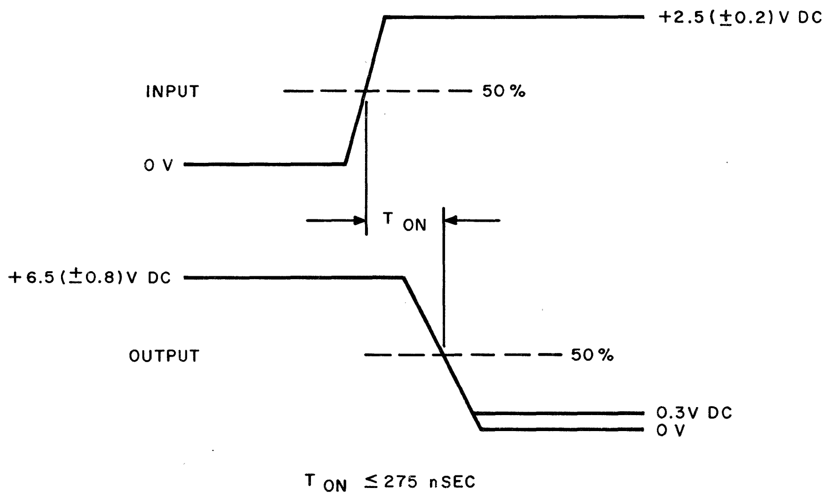

Fig. 4 — NOR Gate Test

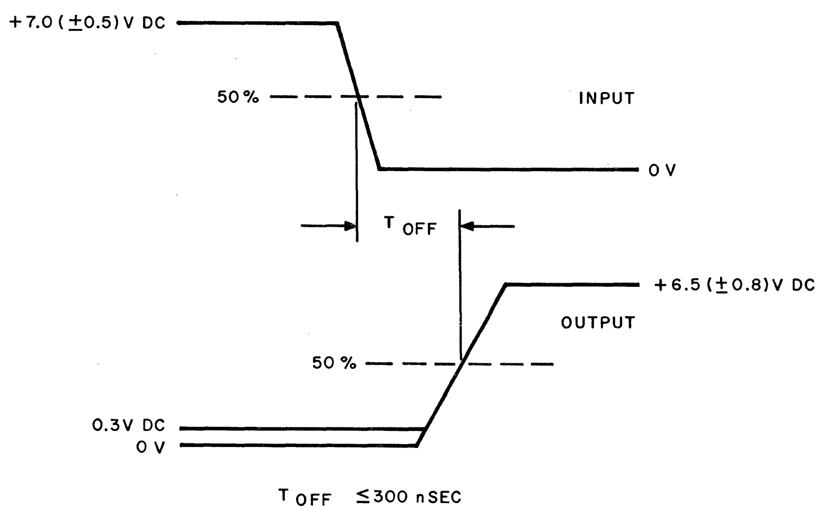

Fig. 5 — NOR Gate Test

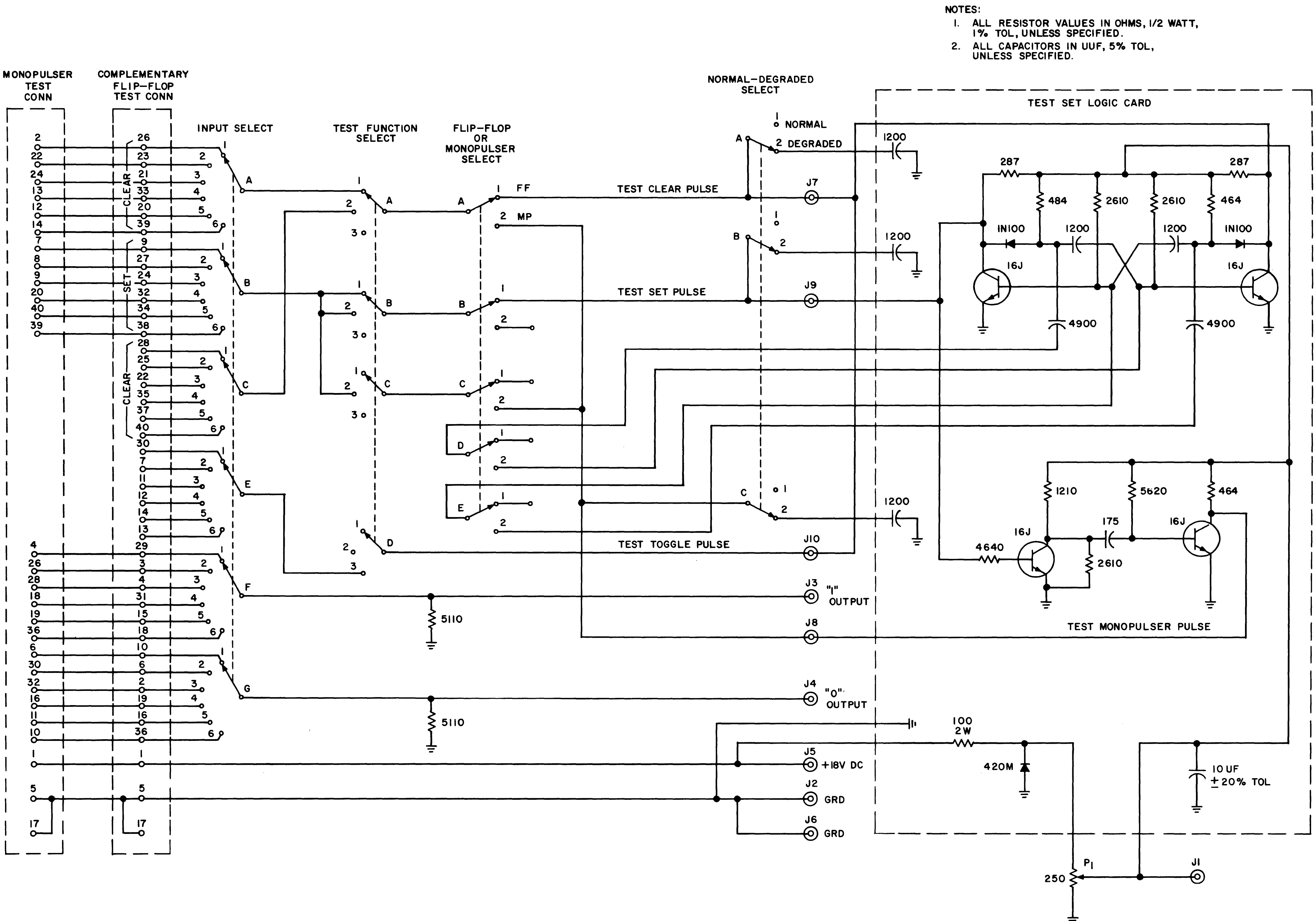

Fig. 6 — Complementary Flip-Flop Test

1 — DC voltmeter, 20,000 ohm/volt, ± 3 percent.

1 — 0 to 50 microammeter, ±3 percent.

2 — Resistors:

1 — 0.121 meg, (±5 percent), 1/2 watt, WECo 145A (or equivalent).

1 — 2150 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

B. Power Requirements

+18 (±0.5) volts dc — 200 ma

+6 (±0.3) volts dc — 0.1 ma

C. Preliminary Procedure

10.05 Set up the test circuit as shown in Fig. 7. The scope EXT SYNC TRIGGER selector should be set to the (+) positive position.

10.06 Make the following settings on the test set:

(1) INPUT selector to position 1.

(2) TEST FUNCTION selector to position 1.

(3) FLIP-FLOP — MONOPULSER selector to FLIP-FLOP.

(4) NORMAL — DEGRADED selector to NORMAL.

(5) Adjust the potentiometer until the voltage between J1 and ground of the test set is 6.0 (±0.2) volts dc.

D. Testing Procedure

10.07 ***Diode Leakage Test:***

(a) This test is to be made before the card is inserted into the test set.

(b) Ground pin 1 and apply +6 (±0.3) volts dc in series with a 0.121-meg resistor to test point 8 of the card to be tested.

(c) The total current drawn shall be less than 35 ua dc.

(d) Remove connections made in (b).

10.08 ***Zener Voltage Test:***

(a) Insert the card to be tested into the test set flip-flop test connector.

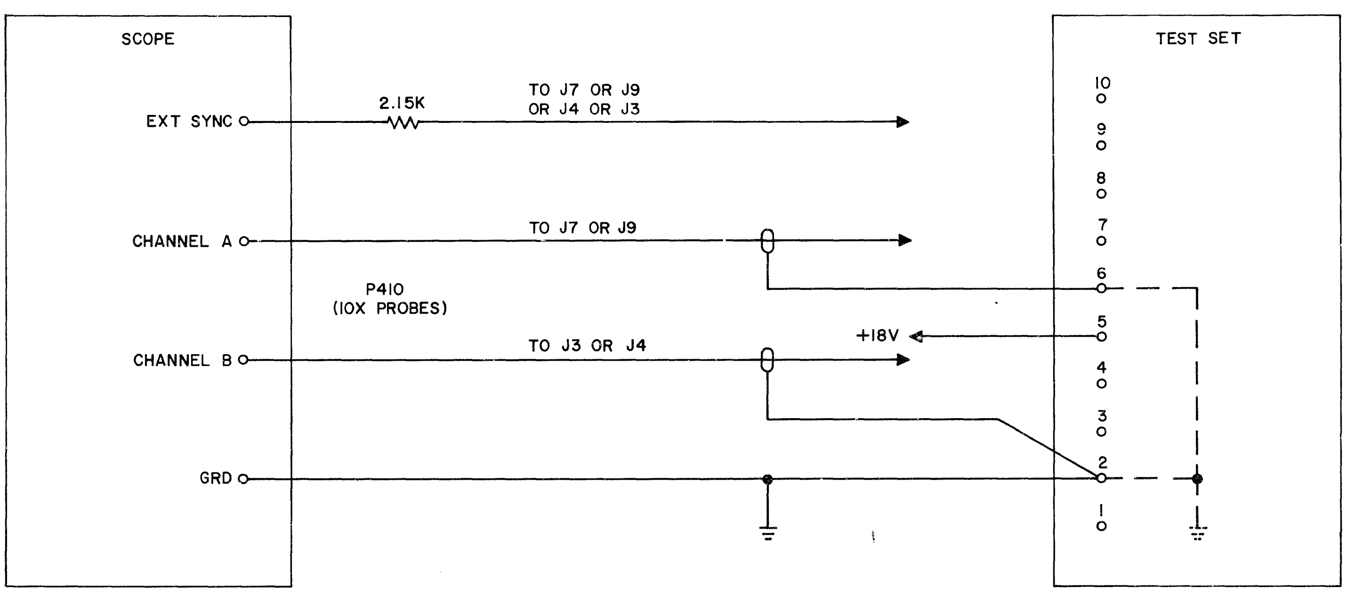

Fig. 7 — Complementary Flip-Flop Test

(b) The voltage between test point 8 and ground, when measured with the voltmeter, shall be +6.2 (±0.6) volts dc.

10.09 ***Pulse Test — Normal Input:***

(a) Consult Table B to determine which flip-flop circuit and corresponding input resistor or capacitor is under test.

10.10 ***Clear Test:***

(1) Connect the EXT SYNC lead to J7 on the test set.

(2) Connect the CHAN A probe to J7 on the test set.

(3) Connect the CHAN B probe to J4 on the test set.

(4) The input test pulse on J7 shall be as specified in Fig. 8.

(5) Rotate the INPUT selector through positions 1 to 6.

(6) The output pulse on J4 of the test set shall be as specified on Fig. 9 at each position.

(7) Rotate the TEST FUNCTION selector to position 2.

(8) Repeat as in (5) and (6).

10.11 ***Set Test:***

(1) Connect the EXT SYNC lead to J9 of the test set.

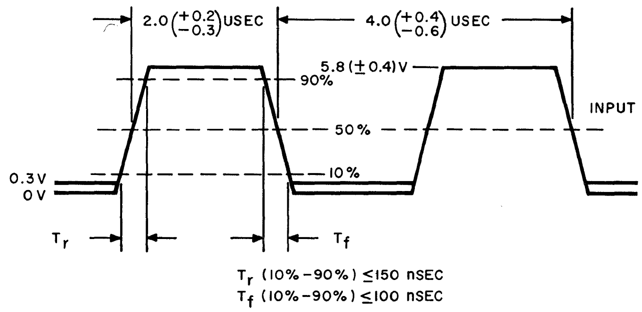

Fig. 8 — Complementary Flip-Flop Test

TABLE B

KEY TO COMPONENTS UNDER TEST AT EACH POSITION OF TEST SET SWITCHES

TEST FUNCTION POSITION	INPUT SELECTOR POSITION	INPUT TERMINAL	INPUT RESISTOR CAPACITOR	TRANSISTOR	OUTPUT TERMINAL
1	1	26, 9	R9.0, R7.0	Q1.0, Q2.0	29, 10
	2	23, 27	R9.1, R7.1	Q1.1, Q2.1	3, 6
	3	21, 24	R9.2, R7.2	Q1.2, Q2.2	4, 2
	4	33, 32	R8.3, R7.3	Q1.3, Q2.3	31, 19
	5	20, 34	R8.4, R7.4	Q1.4, Q2.4	15, 16
	6	39, 38	R9.5, R7.5	Q1.5, Q2.4	18, 36
2	1	28, 9	R8.0, R7.0	Q1.0, Q2.0	29, 10
	2	25, 27	R8.1, R7.1	Q1.1, Q2.1	3, 6
	3	22, 24	R8.2, R7.2	Q1.2, Q2.2	4, 2
	4	35, 32	R9.3, R7.3	Q1.3, Q2.3	31, 19
	5	37, 34	R9.4, R7.4	Q1.4, Q2.4	15, 16
	6	40, 38	R8.5, R7.5	Q1.5, Q2.5	18, 36
3	1	30	C1.0, C2.0	Q1.0, Q2.0	29, 10
	2	7	C1.1, C2.1	Q1.1, Q2.1	3, 6
	3	11	C1.2, C2.2	Q1.2, Q2.2	4, 2
	4	12	C1.3, C2.3	Q1.3, Q2.3	31, 19
	5	14	C1.4, C2.4	Q1.4, Q2.4	15, 16
	6	13	C1.5, C1.5	Q1.5, Q2.5	18, 36

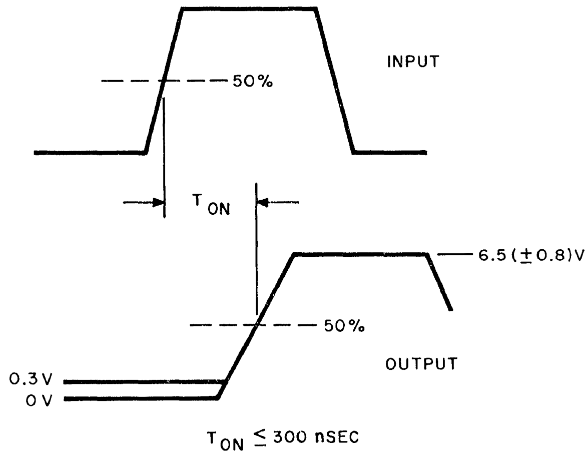

Fig. 9 — Complementary Flip-Flop Test

(2) Connect the CHAN A probe to J9 of the test set.

(3) Connect the CHAN B probe to J3 of the test set.

(4) Rotate the TEST FUNCTION selector to position 2.

(5) Rotate the INPUT selector through positions 1 to 6.

(6) The output pulse on J3 shall be as specified in Fig. 9.

10.12 ***Toggle Test:***

(1) Rotate the SCOPE TRIGGER SLOPE selector to the (—) negative position.

(2) Rotate the TEST FUNCTION selector to position 3.

(3) Connect the EXT SYNC lead to J4 on the test set.

(4) Connect the CHAN A probe to J7 on the test set.

(5) Connect the CHAN B probe to J3 on the test set.

(6) Rotate the INPUT selector through positions 1 to 6.

(7) The output pulse on J3 of the test set shall be as specified in Fig. 10.

(8) Connect the EXT SYNC lead to J3 on the test set.

(9) Connect the CHAN B probe to J4 on the test set.

(10) Repeat (6). The output pulse on J4 shall be as shown in Fig. 10.

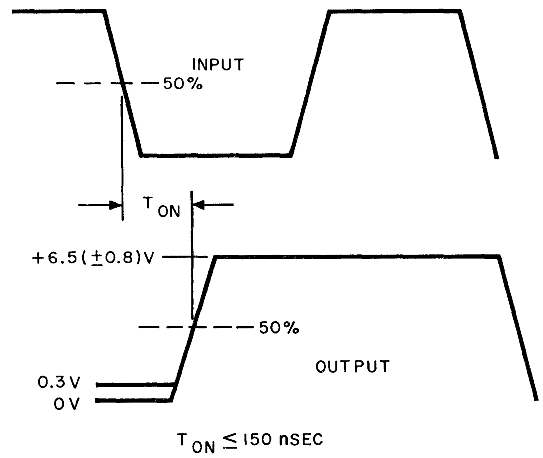

Fig. 10 — Complementary Flip-Flop Test

10.13 ***Pulse Test — Degraded Input:***

(1) Set the NORMAL — DEGRADED selector to DEGRADED. Adjust the voltage between J1 and ground to +3.0 (±0.2) volts dc.

(2) With the input pulse as shown in Fig. 11, repeat 10.10, 10.11, and 10.12; however, time base measurements need not be made. Output waveforms shall appear as in Fig. 9 and 10.

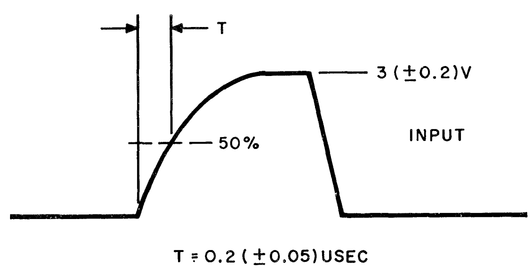

Fig. 11 — Complementary Flip-Flop Test

SINGLE FREQUENCY DETECTOR TEST

A. Testing Equipment

1 — Oscilloscope, Tektronix 535A with plug-in unit 53/54C (or equivalent).

2 — Probes, Tektronix P410 (10X) (or equivalent).

1 — Sine-Wave generator, Hewlett-Packard model 200CD (or equivalent).

1 — Square-Wave generator, Hewlett-Packard model 211A (or equivalent).

1 — DC voltmeter; 20,000 ohms/volt, ±3 percent.

1 — AC voltmeter, Hewlett-Packard model 400L (or equivalent).

1 — Mercury relay, WECo 291A (or equivalent).

3 — Resistors:

1 — 75 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

2 — 316 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

2 — Capacitors:

1 — 100 uf, (±20 percent), WECo 602B (or equivalent).

1 — 40 uf, (±20 percent), WECo 602A (or equivalent).

1 — Transformer, WECo Rep 120C (or equivalent).

1 — Switching diode; KS-16986, L2 (or equivalent).

B. Power Requirements

+18.0 (±0.5) volts dc — 100 ma

−18.0 (±0.5) volts dc — 75 ma

C. Test Procedure

10.14 ***Zener Voltage Test:***

(a) Connect +18.0 (±0.5) volts dc to terminal 1 and ground to terminals 5 and 17.

(b) The voltage between test point 14 and ground shall be +6.2 (±0.6) volts dc.

10.15 ***Threshold Test:***

(1) Connect the card as in the suggested test circuit shown in Fig. 12. Connect +18.0 (±0.5) volts dc to terminal 1, −18.0 (±0.5) volts dc to terminal 20, and ground to terminals 5 and 17. For this section of the test, place a short between pins 1 and 3 of the mercury relay.

(2) Set the frequency of the sin-wave generator to 600 cps (±5 percent).

(3) Set the amplitude of the input sine wave at the primary of the transformer to 1.2 (±0.1) volts rms.

(4) The voltage between terminal 14 and ground shall be +6.5 (±0.8) volts dc.

(5) Increase the amplitude of the input sine wave to 2.0 (±0.1) volts rms.

(6) The voltage between terminal 14 and ground shall be less than or equal to +0.3 volt dc.

(7) Reduce the amplitude of the input sine wave until the output on terminal 14 switches to +6.5 (±0.8) volts dc. The amplitude of the input sine wave at the point of switching shall be 1.6 (±0.2) volts rms.

10.16 ***Transient Test:***

(1) Connect the card in the suggested test circuit shown in Fig. 12.

(2) Set the frequency of the sine-wave generator to 600 cps (±5 percent).

(3) Temporarily short pin 1 to pin 3 of the mercury relay. Set the amplitude of the input sine wave at the primary of the transformer to 3.5 (±0.05) volts rms. Remove the short between pins 1 and 3 of the relay.

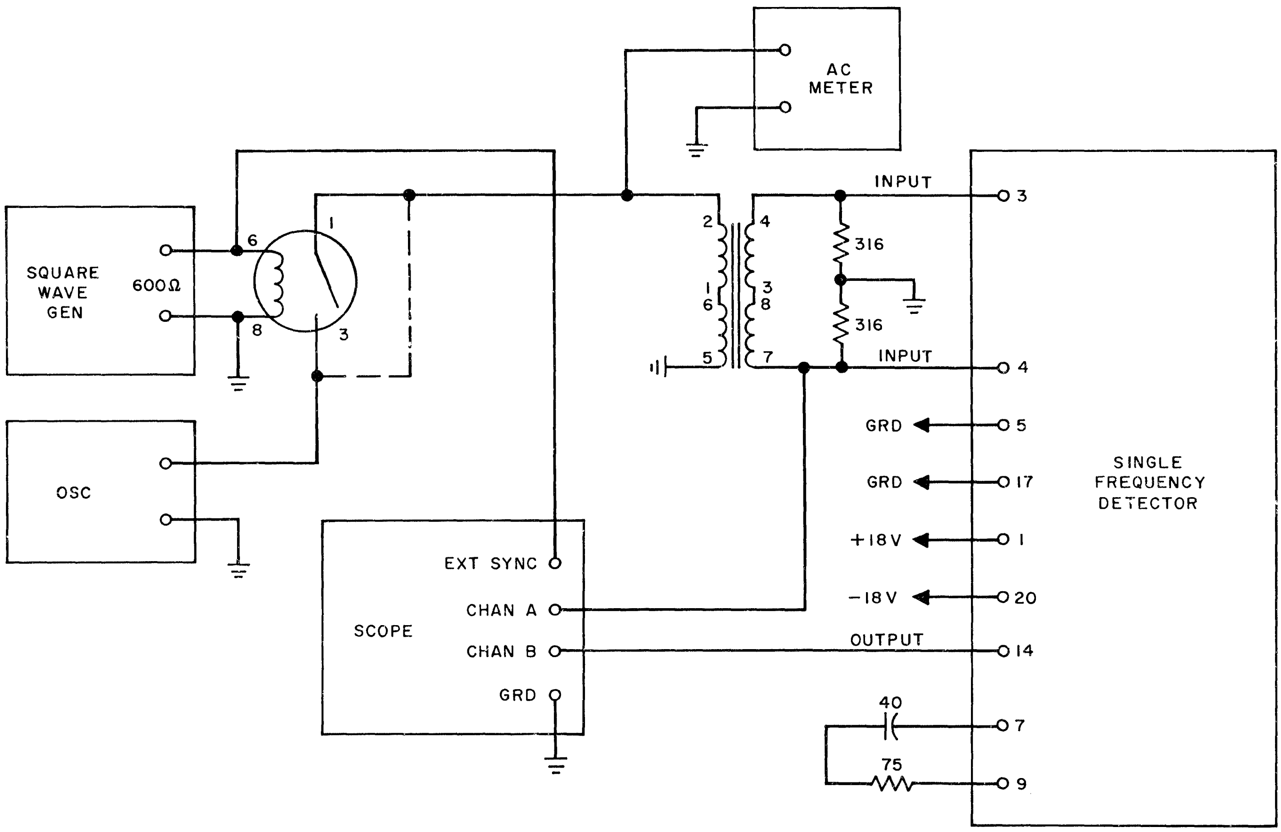

Fig. 12 — Single Frequency Detector Test

(4) Set the frequency of the square-wave generator to 2.0 cps. Set the amplitude of the square-wave generator high enough to operate the mercury relay.

(5) Set the scope EXT SYNC TRIGGER to the (—) negative position. The output waveform at terminal 14 shall be as specified in Fig. 13.

(6) Set the scope EXT SYNC TRIGGER to the (+) position. The output waveform at terminal 14 shall be as specified in Fig. 14.

10.17 ***Integrator-Slicer Test:***

(1) Connect the circuit as in the suggested test circuit shown in Fig. 15. Connect +18.0 (±0.5) volts dc to terminal 1, —18.0 (±0.5) volts dc to terminal 20, and ground to terminals 5 and 17.

(2) Set the frequency of the square-wave generator to 5 (±0.5 cps.

(3) The input waveform shall be as specified in Fig. 16.

(4) Set the scope EXT SYNC TRIGGER to the (—) negative position. The output waveform shall be as specified in Fig. 16.

(5) Set the scope EXT SYNC TRIGGER to the (+) positive position. T_3 shall be as specified in Fig. 16.

AUTOMATIC GAIN CONTROL 1 TEST

10.18 The automatic gain control 1 card, SD-1D060-01 Sheet J4, must be tested in conjunction with an automatic gain control 2 card, SD-1D060-01 Sheet J5, or its equivalent. Therefore, an automatic gain control 2 card shall be

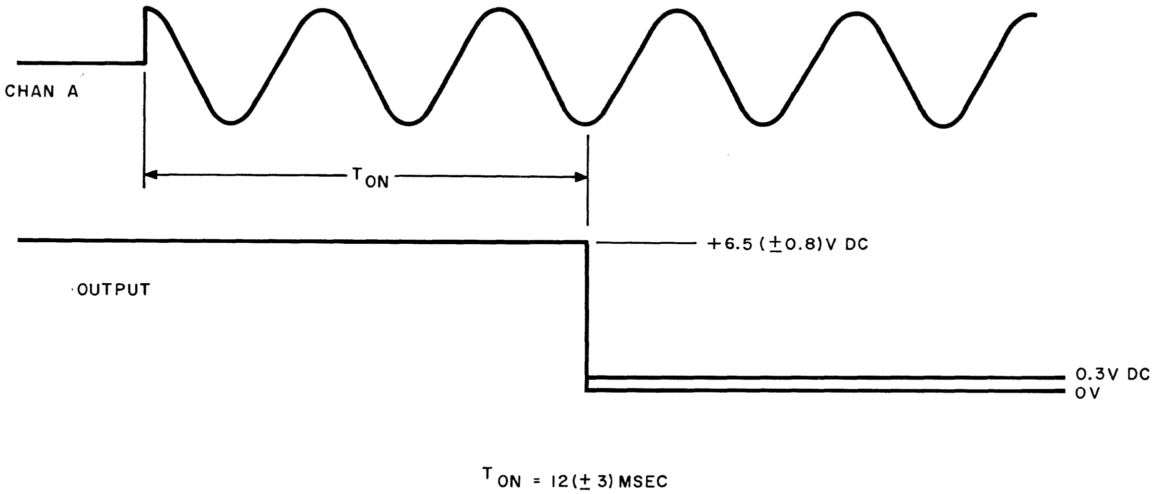

Fig. 13 — Single Frequency Detector Test

contained in the test facility for the automatic gain control 1 card.

A. Testing Equipment

1 — Automatic gain control 2 card, SD-1D060-01 Sheet J5 (or equivalent).

1 — Oscilloscope, Tektronix 535A with plug-in unit 53/54C (or equivalent).

2 — Probes, Tektronix P410 (10X) (or equivalent).

1 — DC volt-ohmmeter, Hewlett-Packard 412A (or equivalent). DC accuracy ±1 percent, ohmmeter ±5 percent.

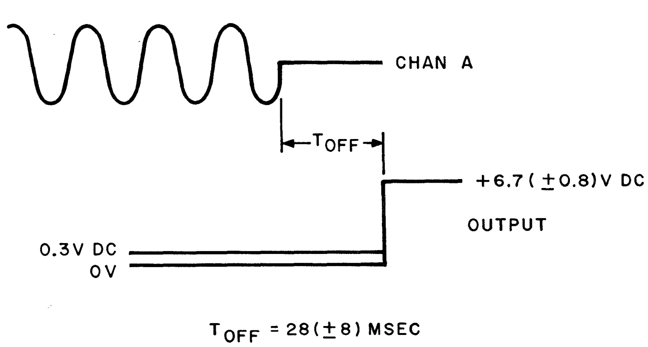

Fig. 14 — Single Frequency Detector Test

1 — AC vacuum tube voltmeter, Hewlett-Packard 400L (or equivalent).

1 — Square-Wave generator, Hewlett-Packard 211A (or equivalent).

1 — Sine-Wave generator, harmonic distortion less than 0.5 percent, Hewlett-Packard 200CD (or equivalent).

1 — Mercury relay, WECo 291A (or equivalent).

1 — Wave analyzer, Hewlett-Packard 302A (or equivalent).

2 — Capacitors:

1 — 2.0 uf, (±10 percent), WECo 579A (or equivalent).

1 — 5.0 uf, (±20 percent), WECo 600B (or equivalent).

3 — Resistors:

1 — 562 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent)

1 — 31.6 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent)

1 — 1000 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

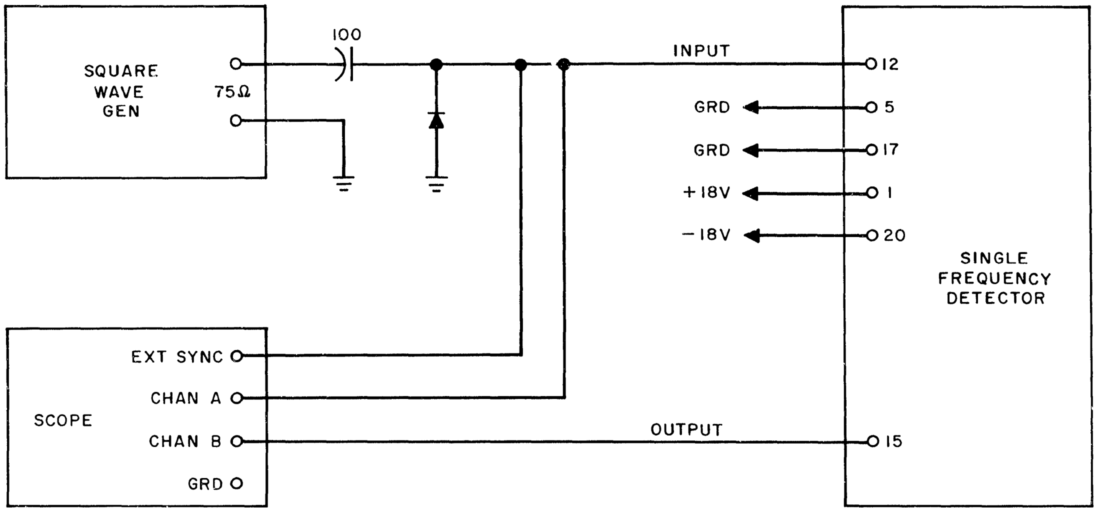

Fig. 15 — Single Frequency Detector Test

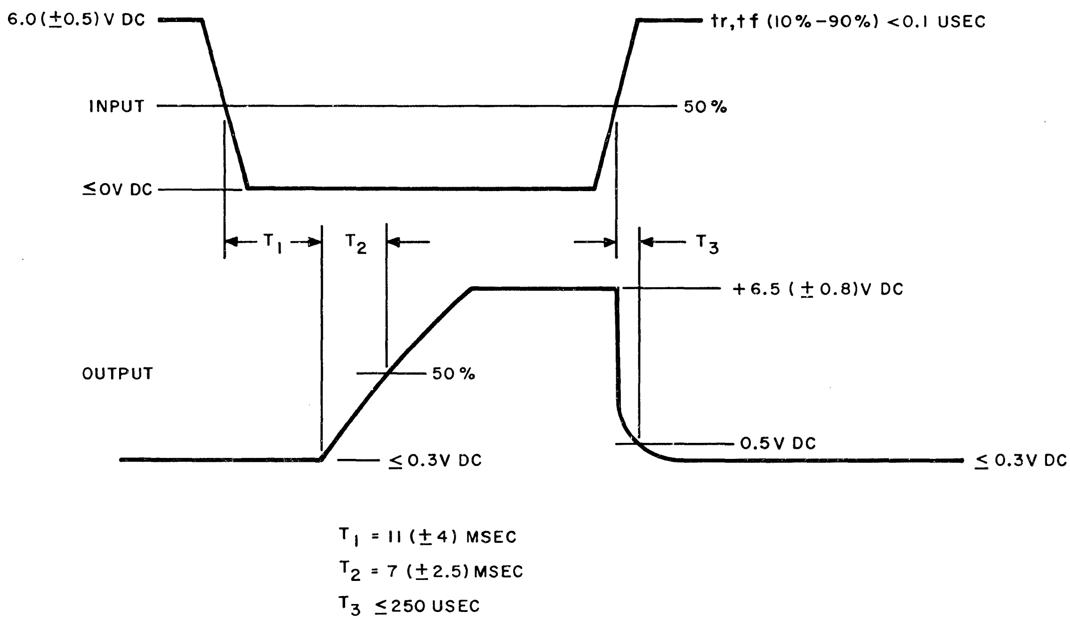

Fig. 16 — Single Frequency Detector Test

B. Power Requirements

+18.0 (±0.5) volts dc — 100 ma

—18.0 (±0.5) volts dc — 50 ma

C. Testing Procedure

10.19 ***Resistance Test:***

(a) Located on the AGC1 card are five slotted machine screw terminals. The resistance between the screw terminals shall be as follows:

BETWEEN SCREW TERMINALS	RESISTANCE VALUE OHMS
1 and 2	866 (±5%)
2 and 3	487 (±5%)
3 and 4	287 (±5%)
4 and test point 8	365 (±5%)

(b) Insert a strap between screw terminals 1 and 5.

10.20 ***Zenner Voltage Test (AGC1 Card):***

(a) Apply ground to terminals 5 and 17, +18.0 (±0.5) volts dc to terminal 1, and —18.0 (±0.5) volts dc to terminal 20.

(b) The voltage between terminal 14 and ground shall be +12 (±1.5) volts dc.

(c) The voltage between test point 14 and ground shall be +6.2 (±0.45) volts dc.

10.21 ***Gain Control Test:***

(1) The gain control test of the AGC1 card is made in conjunction with an AGC2 card. Connect the cards, as in the suggested test circuit shown in Fig. 17, with the scope connected to terminal 10 of the AGC2 card. Connect power to both cards as specified in 10.20 (a).

(2) Connect the sine-wave generator in series with a 2-uf capacitor to terminal 8 of the AGC1 card. Set the frequency of the generator to 1800 cps (±5 percent). Set the output level of the generator to 0.

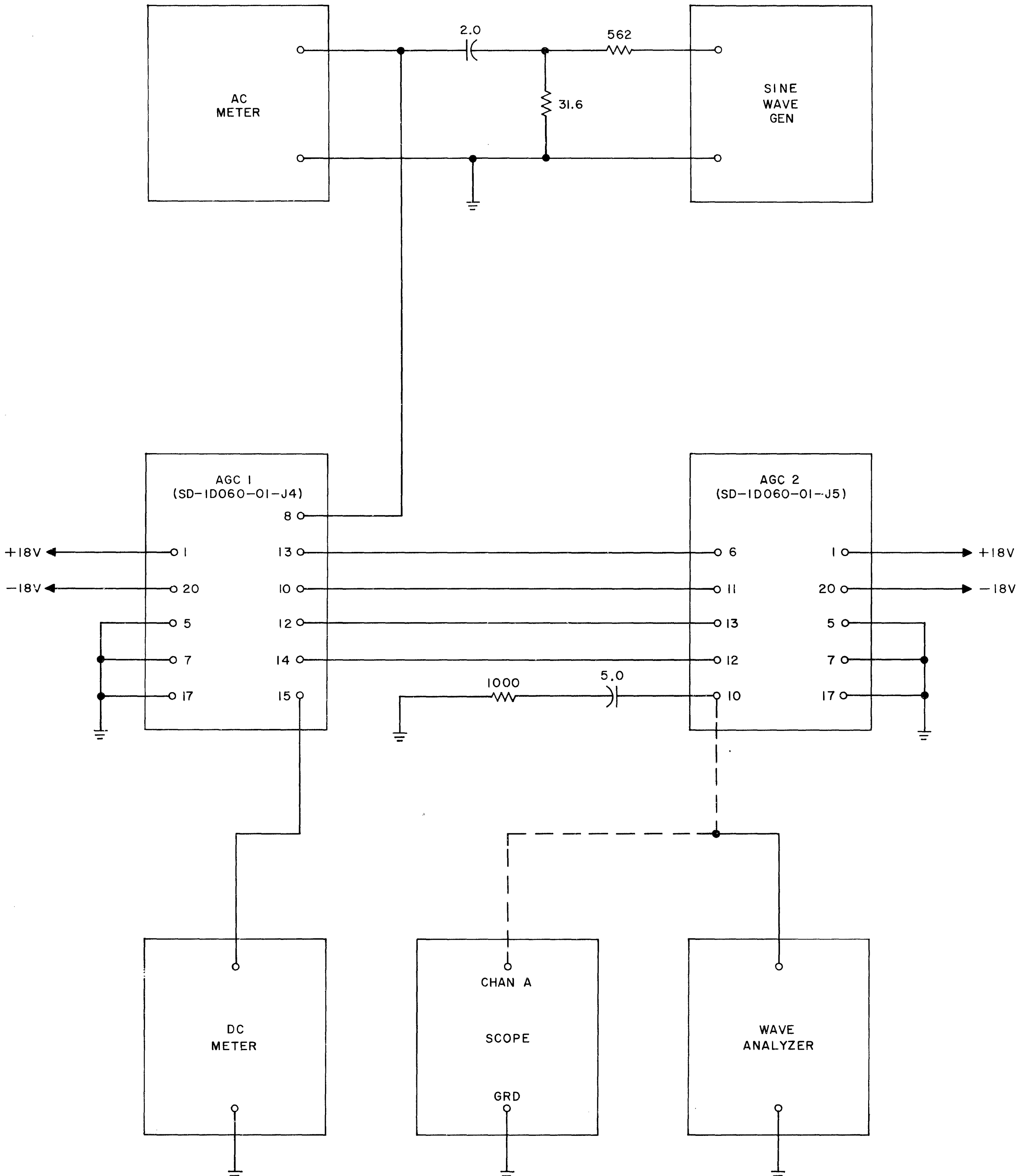

Fig. 17 — Automatic Gain Control 1 Test

(3) Slowly increase the output level of the generator until the carrier detector voltage on terminal 15 of the AGC1 card switches to +6.5 (±0.8) volts dc. The input voltage between terminal 8 and ground of the AGC1 card shall be 13.5 $\left(\begin{smallmatrix}+0.9\\-0.8\end{smallmatrix}\right)$ mv rms. Record the input level.

(4) The output waveform on terminal 10 of the AGC2 card shall be a sine wave of amplitude 2.5 (±0.3) volts peak-to-peak.

(5) Increase the input signal level between terminal 8 and ground of the AGC1 card to 78 (±1) mv rms. The output level on terminal 10 of the AGC2 card shall be a sine wave of amplitude 2.5 $\left(\begin{smallmatrix}+0.35\\-0.30\end{smallmatrix}\right)$ volts peak-to-peak. The voltage on terminal 15 of the AGC1 card shall be +6.6 (±0.8) volts dc.

(6) Increase the input signal level between terminal 8 and ground of the AGC1 card to 450 (±5) mv rms. The voltage on terminal 10 shall be 10, 2.5 $\left(\begin{smallmatrix}+0.45\\-0.30\end{smallmatrix}\right)$ volts peak-to-peak; and terminal 15 shall measure +6.5 (±0.8) volts dc.

10.22 ***Distortion Measurement:***

(1) The distortion measurement of the AGC1 card is made in conjunction with the AGC2 card. Connect the cards, as in the suggested test circuit shown in Fig. 17, with the wave analyzer connected to terminal 10 of the AGC2 card. Apply power to both cards as in 10.20 (a).

(2) With the wave analyzer connected to terminal 10 of the AGC2 card, apply a 78 (±1) mv rms signal at 600 cps (±5 percent) to input terminal 8 of the AGC1 card. Tune the wave analyzer to obtain a peak reading on the meter at the fundamental frequency of 600 cps. Set the meter indication to 0 db by adjusting the wave analyzer reference adjustment.

(3) Tune the wave analyzer for a peak meter reading in the vicinity of the second harmonic frequency of 1200 cps. The meter should indicate —30 db or lower at the second harmonic frequency.

10.23 ***Carrier Detector Response Time:***

(1) The carrier detector response test of the AGC1 card is made in conjunction with the AGC2 card. Connect the cards as in the suggested test circuit shown in Fig. 18. Apply power to both cards as in 10.20 (a).

(2) Set the frequency of the square-wave generator to approximately 1 cps. Set the symmetry control to its center position and the 600-ohm output amplitude control to 0.

(3) Set the frequency of the sine-wave generator to 1800 cps (±5 percent). Adjust the generator amplitude control until the input level at terminal 8 of the AGC1 card is 2 db higher than the level recorded in 10.21 (3). Set the 600-ohm output amplitude control of the square-wave generator to its center position.

(4) Set the scope EXT SYNC TRIGGER selector to the positive (+) position. The input waveform on terminal 8 of the AGC1 card and the output waveform on terminal 15 of the AGC1 card shall be as specified in Fig. 19.

(5) Set the scope EXT SYNC TRIGGER selector to the negative (—) position. The input and output waveforms shall be as specified in Fig. 20.

AUTOMATIC GAIN CONTROL 2 TEST

10.24 The automatic gain control 2 card, SD-1D060-01, Sheet J5, must be tested in conjunction with an automatic gain control 1 card, SD-1D060-01 Sheet J4, or its equivalent. Therefore, an automatic gain control 1 card shall be contained in the test facility for the automatic gain control 2 card.

A. Testing Equipment

1 — Automatic gain control 1 card SD-1D060-01 Sheet J4 (or equivalent). (This card or its equivalent must have met requirments specified in previous test.)

1 — Oscilloscope, Tektronix 535A with plug-in unit 53/54C (or equivalent).

2 — Probe, Tektronix P410 (10X) (or equivalent).

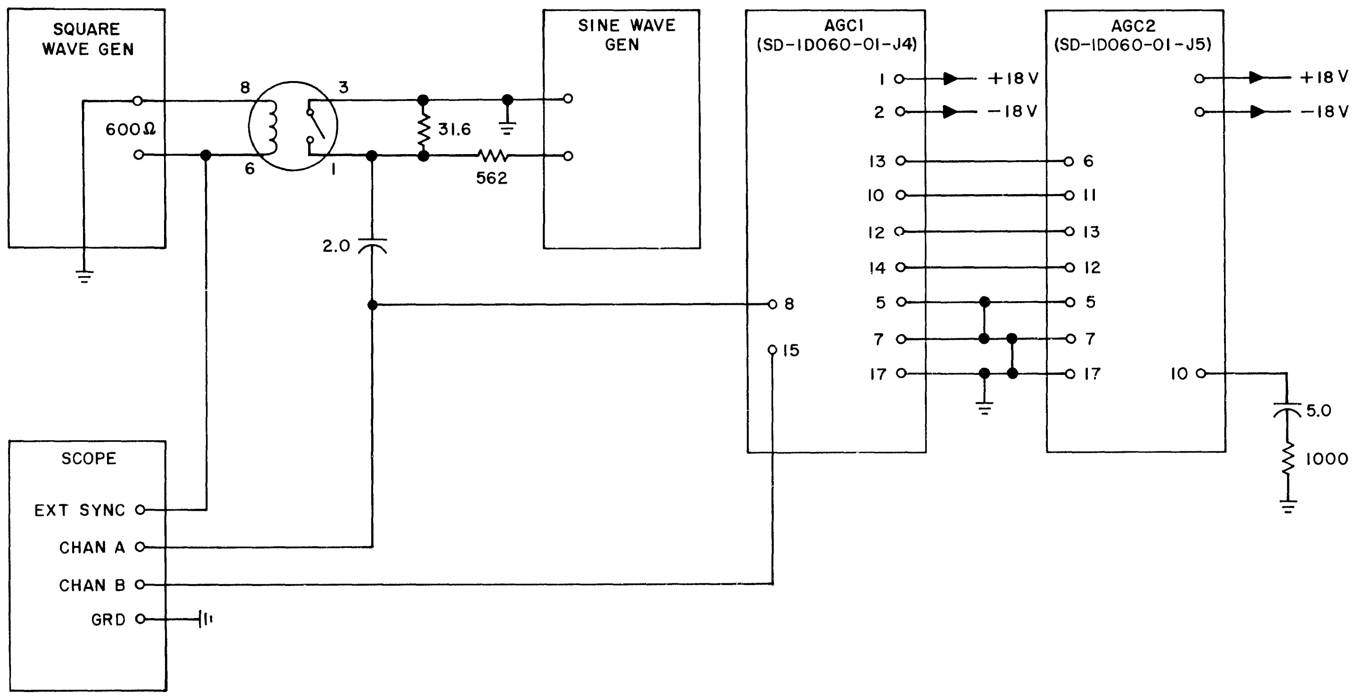

Fig. 18 — Automatic Gain Control 1 Test

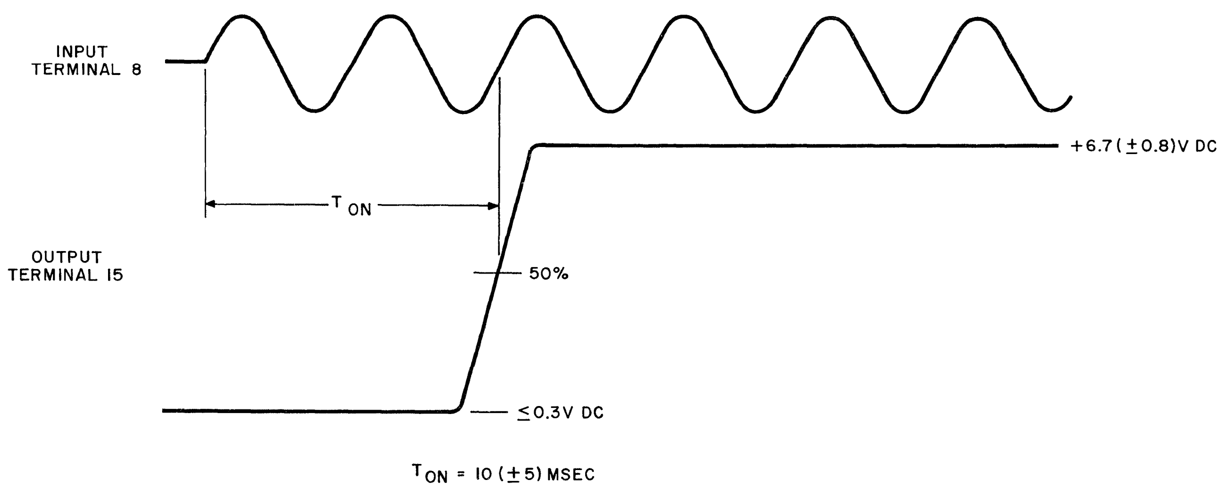

Fig. 19 — Automatic Gain Control 1 Test

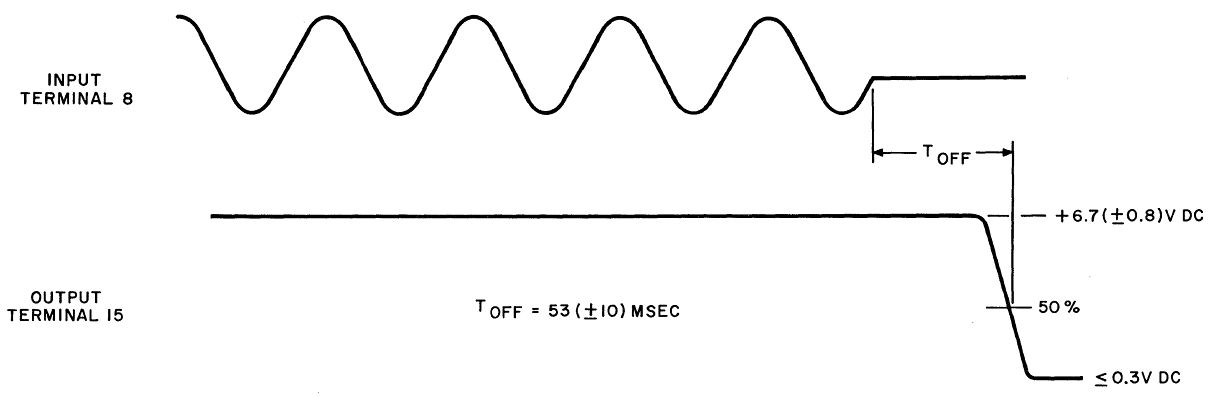

Fig. 20 — Automatic Gain Control 1 Test

1 — DC volt-ohmmeter, Hewlett-Packard 412A (or equivalent).

1 — AC voltmeter, Hewlett-Packard 400L (or equivalent).

1 — Square-Wave generator, Hewlett-Packard 211A (or equivalent).

1 — Sine-Wave generator, harmonic distortion less than 0.5 percent, Hewlett-Packard 200CD (or equivalent).

1 — Mercury relay, WECo 291A (or equivalent).

1 — Wave analyzer, Hewlett-Packard 302A (or equivalent).

2 — Capacitors:

2.0 uf, (±10 percent), WECo 579A (or equivalent).

5.0 uf, (±20 percent), WECo 600B (or equivalent).

3 — Resistors:

1 — 1000 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

1 — 562 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

1 — 31.6 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

1 — Test set such as shown in Fig. 3.

B. Power Requirements

+18.0 (±0.5) volts dc — 100 ma

—18.0 (±0.5) volts dc — 50 ma

C. Testing Procedure

10.25 ***Zener Voltage Test:***

(a) Apply ground to terminals 5 and 17, +18.0 (±0.5) volts dc to terminal 1, and —18.0 (±0.5) volts dc to terminal 20. The voltage between test point 10 and ground shall be —12.0 (±1.5) volts dc.

10.26 ***Gain Adjustment:***

(1) The gain adjustment of the AGC2 card is made in conjunction with the AGC1 card. Connect the cards as in the suggested test circuit shown in Fig. 21. Connect power to both cards as specified in 10.25 (a).

(2) Located on the AGC2 card are five numbered strapping pins. This section of the test will determine which pins, if any, are to be strapped. Connect the test set shown in Fig. 22 to the five strapping pins located on the AGC2 card. Set both switches to position 1.

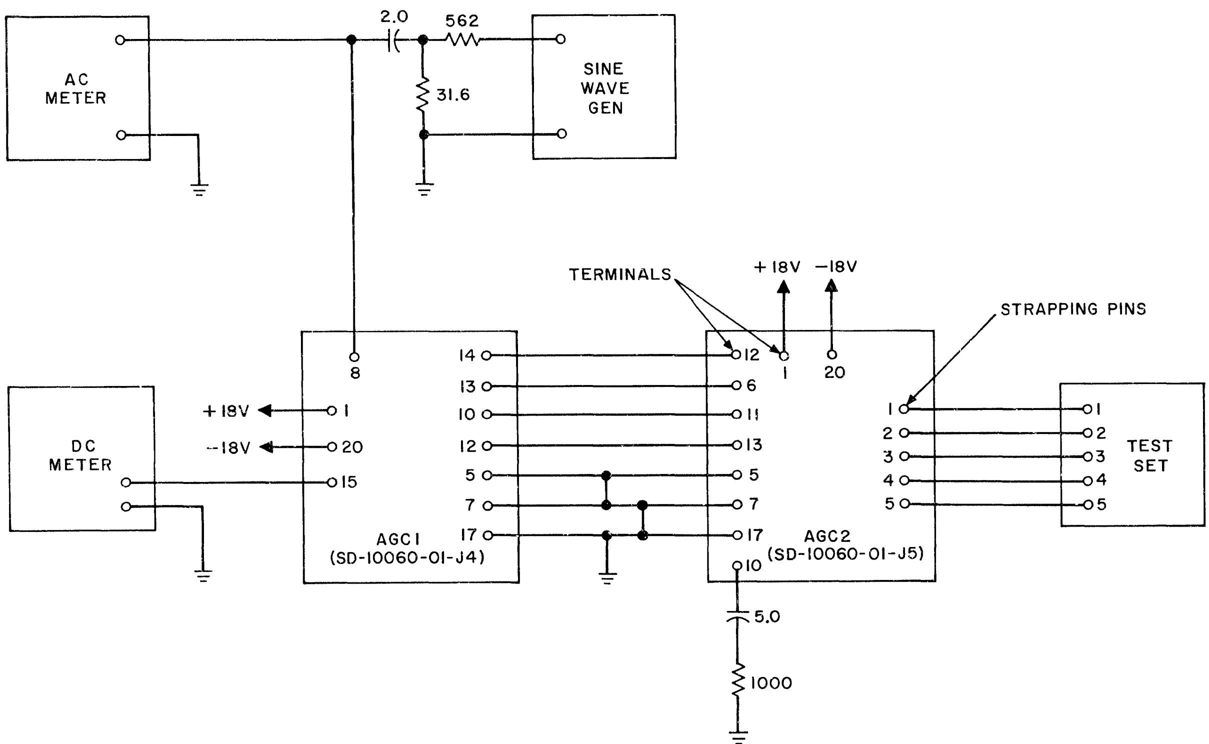

Fig. 21 — Automatic Gain Control 2 Test

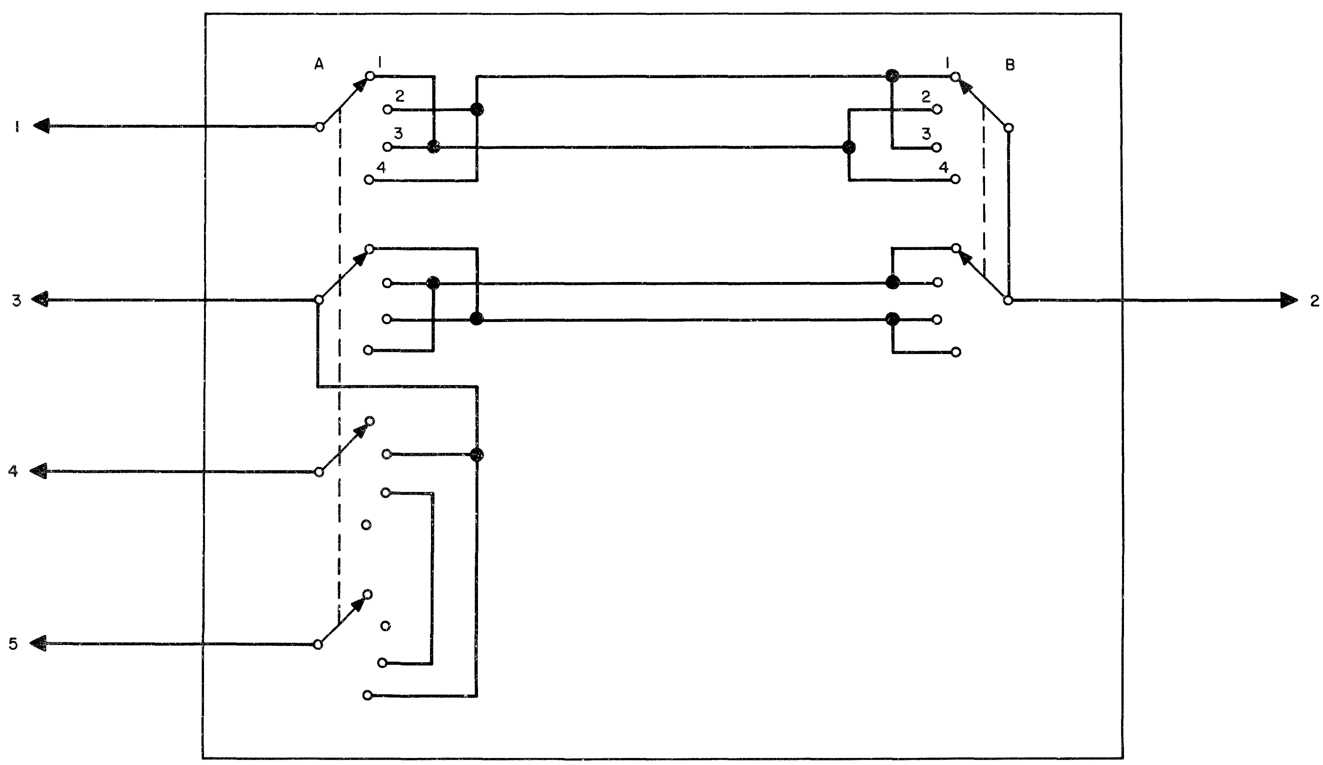

Fig. 22 — Automatic Gain Control 2 Test

(3) Connect the sine-wave generator in series with a 2-uf capacitor to terminal 8 of the AGC1 card as shown in Fig. 21. Set the frequency of the generator to 1800 cps (±5 percent) and adjust the amplitude to obtain a 13.1 (±0.05) mv rms signal between terminal 8 and ground of the AGC1 card. The voltage between terminal 15 and ground shall be +6.5 (±0.8) volts dc.

(4) Rotate switches A and B on the test set, beginning with both switches at position 1, according to the sequence given in Table C, until the voltage between terminal 15 and ground on the AGC1 card switches to less than +0.3 volt dc. Note the position of the test set switches.

(5) Using the test set switch positions obtained in (4) consult Table C to determine which pins should be strapped.

(6) Remove the card from the test circuit and strap the appropriate pins according to the instructions given in A-A of AGC2 card assembly drawing A-835179.

Note: Subsequent strap changes may be required only if components are replaced.

10.27 ***Gain Control Test:***

(1) The gain control test of the AGC2 card is made in conjunction with an AGC1 card. Connect the cards as in the suggested test cir-

TABLE C

STRAPPING FOR PIN POSITION

TEST SET (STEP 4) SWITCH POSITIONS		CHECK INDICATES PINS TO BE STRAPPED				TOTAL RESISTANCE BETWEEN PINS 1 AND 5
SWITCH A	SWITCH B	1 TO 2	2 TO 3	3 TO 4	4 TO 5	OHMS
1	1					2307
1	2	√				2145
1	3		√			1991
1	4	√	√			1829
2	4			√		1688
2	3	√		√		1526
2	2		√	√		1372
2	1	√	√	√		1210
3	1				√	1079
3	2	√			√	935
3	3		√		√	781
3	4	√	√		√	619
4	4			√	√	478
4	3	√		√	√	316
4	2		√	√	√	162
4	1	√	√	√	√	Less than 1

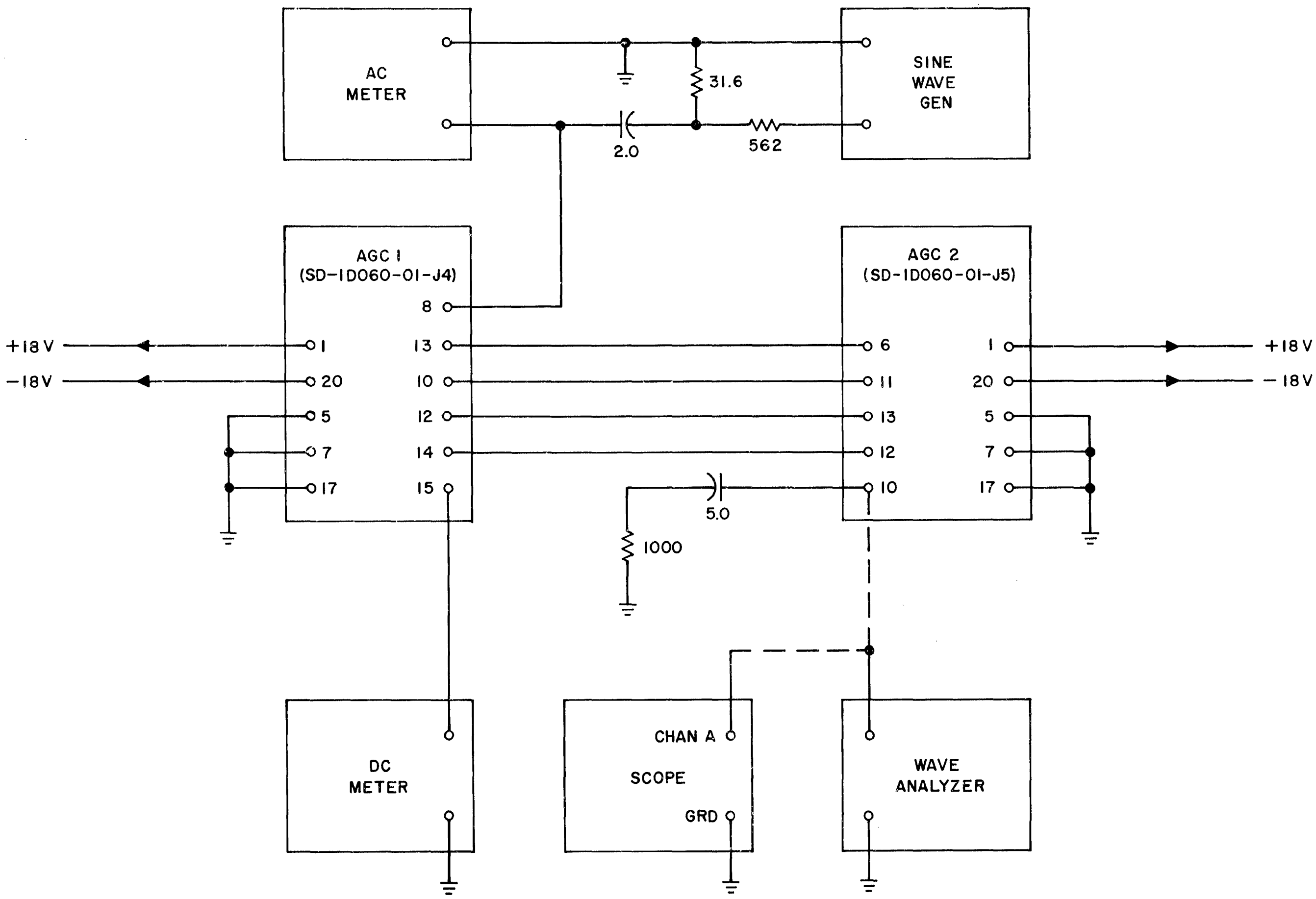

Fig. 23 — Automatic Gain Control 2 Test

cuit shown in Fig. 23 with the scope connected terminal 10 of the AGC2 card. Apply power to both cards as specified in 10.25 (a).

(2) Set the frequency of the sine-wave generator to 1800 cps (±5 percent). Set the output level of the generator to 0.

(3) Slowly increase the output level of the generator until the carrier detector voltage on terminal 15 of the AGC1 card switches to +6.5 (±0.8) volts dc. The input level between terminal 8 and ground of the AGC1 card shall be 13.5 (±0.4) mv rms. Record the input level.

Note: After the initial gain adjustment and upon subsequent testing of the AGC2 card, the input level requirement when the carrier detector voltage switches to +6.5 (±0.8) volts dc shall be $13.5\binom{+0.9}{-0.8}$ mv rms.

(4) The output waveform on terminal 10 of the AGC2 card shall be a sine wave of amplitude 2.5 (±0.3) volts peak-to-peak.

(5) Increase the input signal level between terminal 8 and ground of the AGC1 card to 78 (±1) mv rms. The output level on terminal 10 of the AGC2 card shall be a sine wave of amplitude $2.5\binom{+0.35}{-0.30}$ volts dc. The voltage on terminal 15 of the AGC1 card shall be +6.5 (±0.8) volts dc.

(6) Increase the input signal level between terminal 8 and ground of the AGC1 card to 450 (±5) mv rms. The voltage on terminal 10 shall be $2.8\binom{+0.45}{-0.30}$ volts dc; and terminal 15 shall measure +6.5 (±0.8) volts dc.

10.28 ***Distortion Measurement:***

(1) The distortion measurement of the AGC2 card is made in conjunction with the AGC1 card. Connect the cards as in the suggested test circuit shown in Fig. 23, with the wave analyzer connected to terminal 10 of the AGC2 card. Apply power to both cards as in 10.25 (a).

(2) With the wave analyzer connected to terminal 10 of the AGC2 card, apply a 78 (±1) mv rms signal at 600 cps (±5 percent) to input terminal 8 of the AGC1 card. Tune the wave analyzer to obtain a peak reading on the meter at the fundamental frequency of 600 cps. Set the meter indication to 0 db by adjusting the wave analyzer reference adjustment.

(3) Tune the wave analyzer for a peak meter reading in the vicinity of the second harmonic frequency of 1200 cps. The meter should indicate —30 db or lower at the second harmonic frequency.

10.29 ***Carrier Detector Response Time:***

(1) The carrier detector response test of the AGC2 card is made in conjunction with the AGC1 card. Connect the cards as in the suggested test circuit shown in Fig. 24. Apply power to both cards as in 10.25 (a).

(2) Set the frequency of the square-wave generator to 1 cps. Set the symmetry control to its center position and the 600-ohm output amplitude control to 0.

(3) Set the frequency of the sine-wave generator to 1800 cps (±5 percent). Adjust the generator amplitude control until the input level at terminal 8 of the AGC1 card is 2 db higher than the level recorded in 10.27 (3). Set the 600-ohm output amplitude control of the square-wave generator to its center position.

(4) Set the scope EXT SYNC TRIGGER selector to the (+) positive position. The input waveform on terminal 8 of the AGC1 card and the output waveform on terminal 15 of the AGC1 card shall be as specified in Fig. 25.

(5) Set the scope EXT SYNC TRIGGER selector to the (—) negative position. The input and output waveforms shall be as specified in Fig. 26.

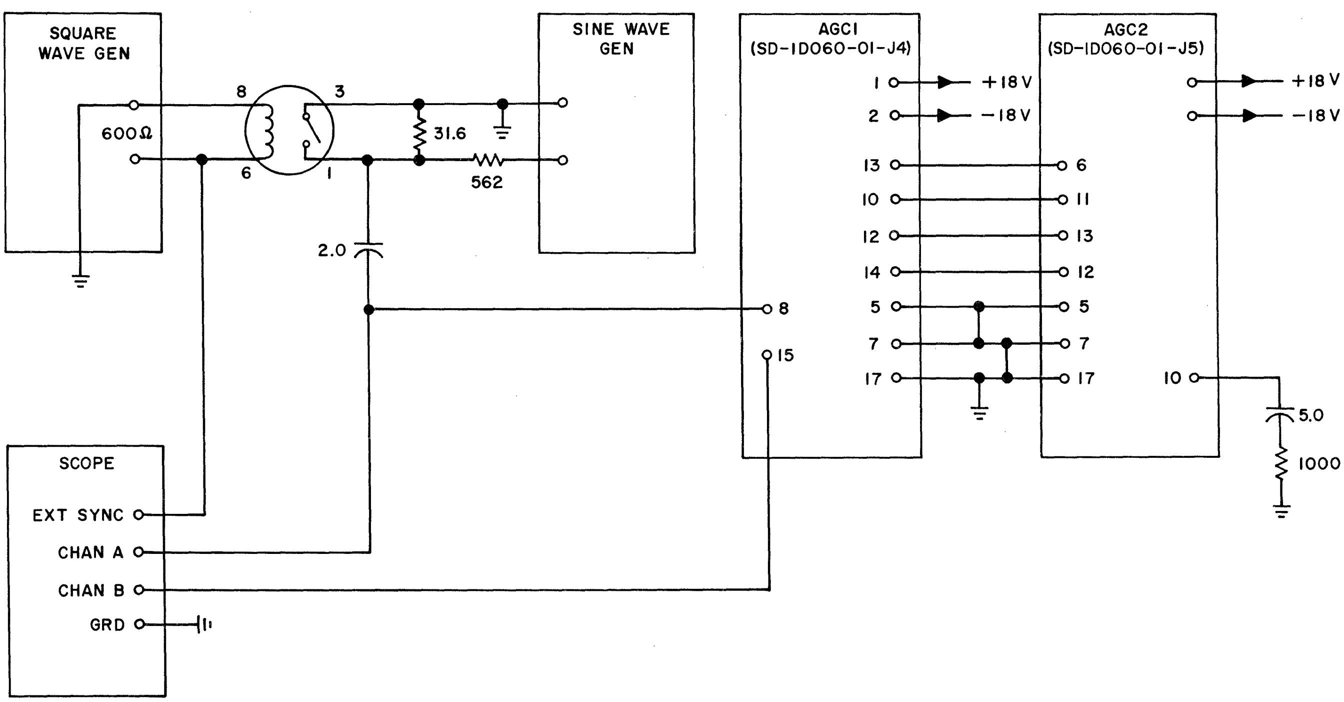

Fig. 24 — Automatic Gain Control 2 Test

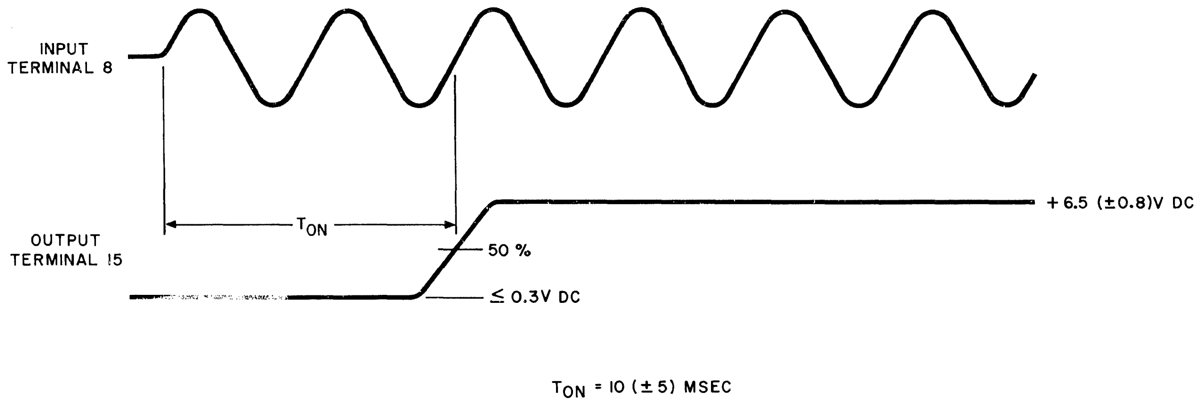

Fig. 25 — Automatic Gain Control 2 Test

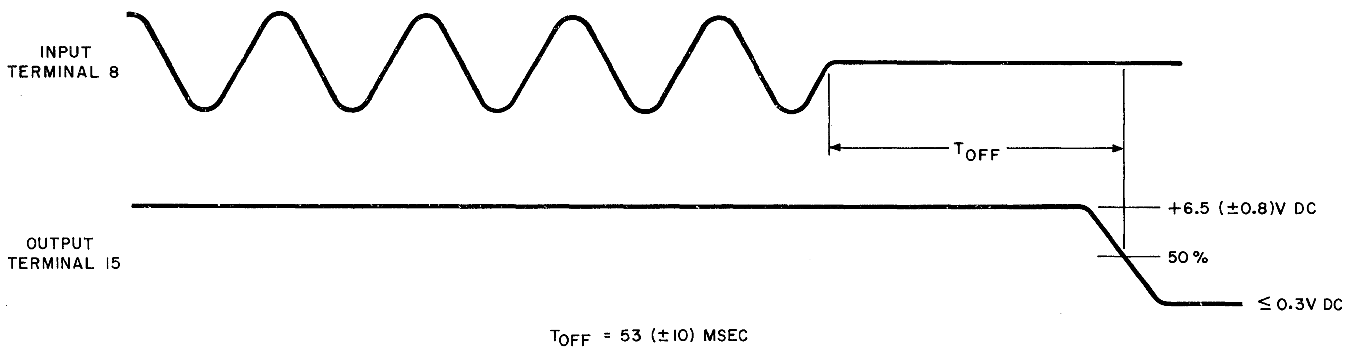

Fig. 26 — Automatic Gain Control 2 Test

TRANSMITTER OUTPUT TEST

A. Power Requirements

+18.0 (±0.5) volts dc — 50 ma

−18.0 (±0.5) volts dc — 25 ma

B. Testing Equipment

1 — Oscilloscope, Tektronix 535A with plug-in unit C-A or 53/54C (or equivalent).

2 — Probes, Tektronix P410 (10X) (or equivalent).

1 — Oscillator, Hewlett-Packard 200CD (or equivalent).

1 — 0- to 10-volt dc voltmeter, 20,000 ohm/volt, calibrated to 0.5 percent full scale accuracy.

1 — Square-Wave generator, Hewlett-Packard 211A (or equivalent).

1 — Ohmmeter, Hewlett-Packard 412A (or equivalent).

1 — 0 to 10 ua dc meter, ±3 percent, Hewlett-Packard 412A (or equivalent).

1 — Transformer, WECo Rep 120C (or equivalent).

1 — AC voltmeter, Hewlett-Packard 400L (or equivalent).

2 — DPDT switches.

1 — Inductor, 0.115h, (±2 percent), WECo 1592A (or equivalent).

3 — Capacitors:

1 — 40 uf, (±20 percent), WECo 602A (or equivalent).

2 — 0.0392 uf, (±2 percent), WECo 570K (or equivalent).

1 — Switching diode, KS-16986, L2 (or equivalent).

7 — Resistors:

2 — 316 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

2 — 5.620k ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

1 — 5.11k ohms, (±1 percent), 1/2 watt, WECo 221A (or equivalent).

1 — 1.78 meg, (±1 percent), 1/2 watt, WECo 221A (or equivalent).

1 — 600 ohms, (±1 percent), 1/2 watt, WECo 221A (or equivalent).

C. Testing Procedure

10.30 ***Resistance Measurement:***

(a) Located on the card are four numbered slotted machine screw strapping terminals. The resistance between the terminals shall be as follows.

BETWEEN SCREW TERMINALS	RESISTANCE VALUE
	OHMS
1 and 2	220 (±5%)
2 and 3	150 (±5%)
3 and 4	100 (±5%)

(b) The resistance between screw terminal 4 and card plug terminal 20 shall be 2940 ohms (±5 percent).

(c) Insert a strap between terminals 1 and 4.

10.31 ***Diode Leakage Test:***

(a) Connect ground to terminals 5 and 17. Connect +18.0 (±0.5) volts dc in series with 1.78-meg resistor to terminals 15, 16, 13, and 14 as shown in Fig. 27. The current drawn from the +18 volt supply shall be less than 0.2 ua dc.

10.32 ***Zener Voltage Test:***

(a) Connect ground to terminals 4, 5, 6, and 17, and +18.0 (±0.5) volts dc to terminal 1. The voltage between test point 1 and ground shall be +8.2 (±0.45) volts dc when measured with a voltmeter calibrated to 0.5 percent accuracy.

10.33 ***Square-Wave Driver Test:***

(1) Connect ground to terminals 5 and 17 and +18.0 (±0.5) volts to terminal 1.

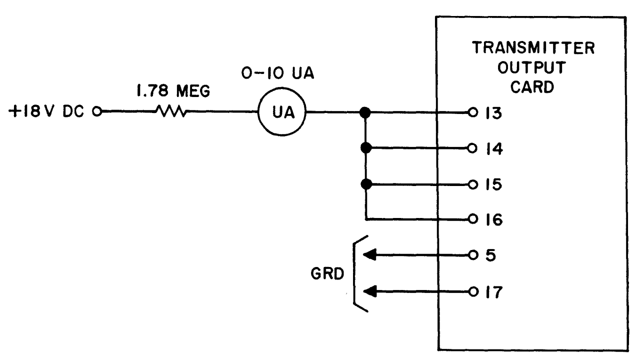

Fig. 27 — Transmitter Output Test

(2) Connect the card as in the suggested test circuit shown in Fig. 28 using the output of the square-wave generator. Set the symmetry control to the center position.

(3) The input waveforms on terminals 3 and 10 and the output waveforms on terminals 4 and 6 shall be as specified in Fig. 29.

10.34 *Line Amplifier Test:*

(1) Connect the card as in the suggested test circuit shown in Fig. 30. Frequency of oscillator shall be 1800 cps (±5%).

(2) With both switches set to position 1, adjust the oscillator to produce a 1 ±0.05 volt rms signal between input terminal 13 and ground and between input terminal 14 and ground. The output voltage between terminals 7 and 9 shall be 1.7 (±0.25) volts rms.

(3) With both switches set to position 2, adjust the oscillator to produce a 1.0 (±0.05) volt rms signal between input terminal 15 and ground and between input terminal 16 and ground. The output voltage between terminals 7 and 9 shall be 1.7 (±0.25) volts rms.

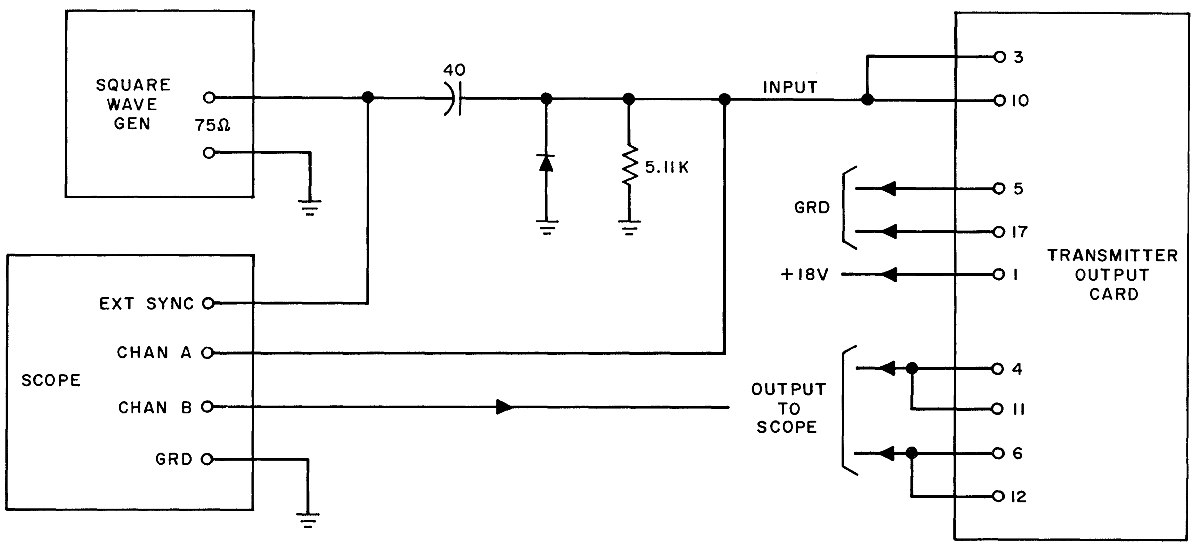

Fig. 28 — Transmitter Output Test

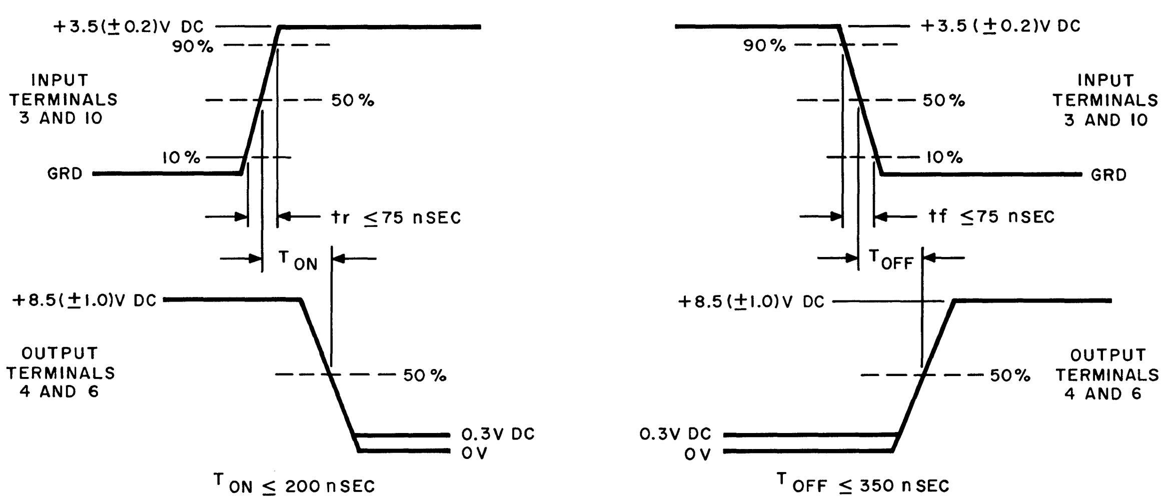

Fig. 29 — Transmitter Output Test

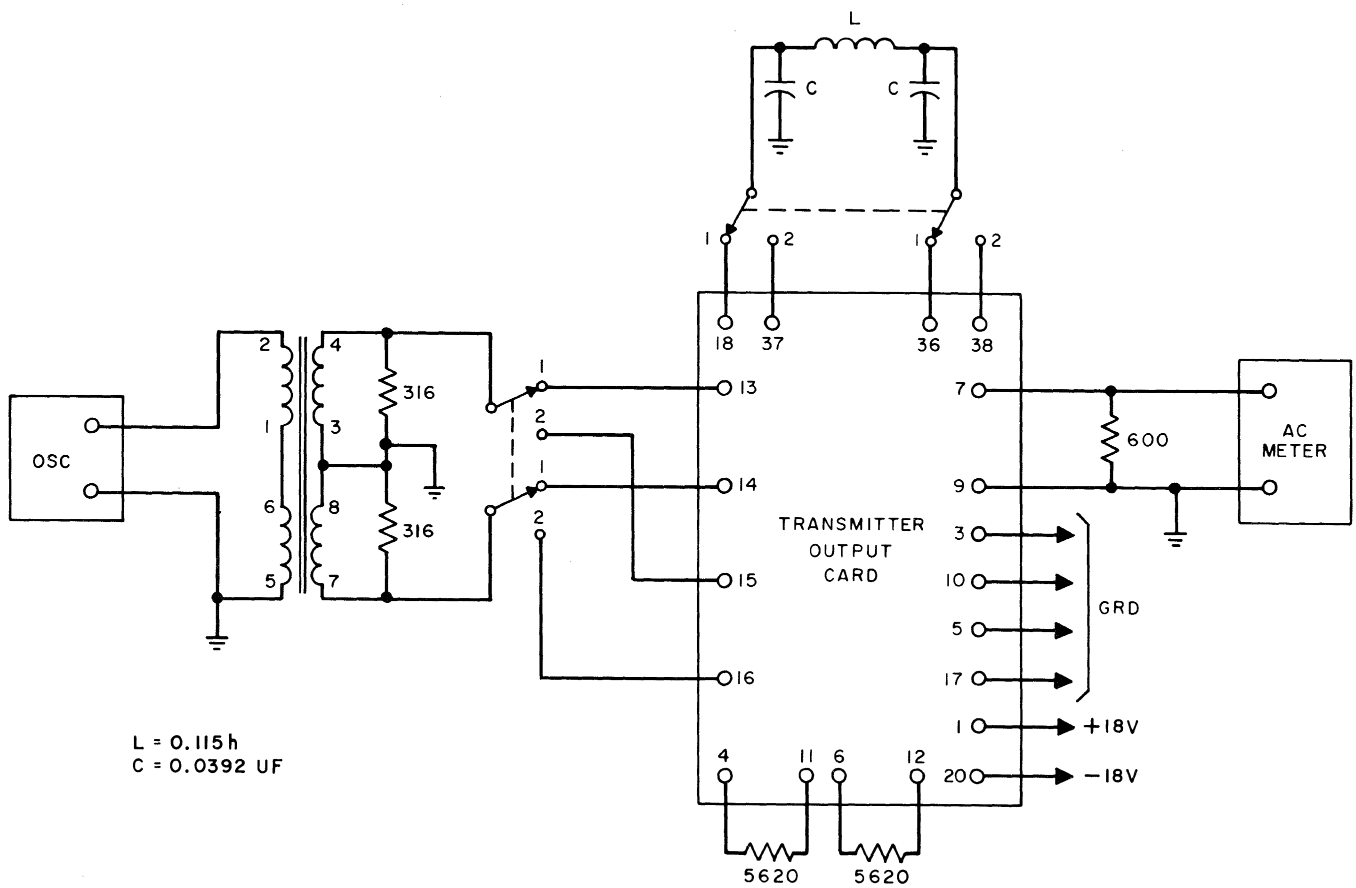

Fig. 30 — Transmitter Output Test

MONOPULSER CARD TEST

A. Testing Equipment

1 — Monopulser test set such as shown in Fig. 6.

1 — Oscilloscope, Tektronix 53A with plug-in unit-type 53/54C or C-A (or equivalent).

2 — Probes, P410 (10X) (or equivalent).

1 — DC voltmeter, 20,000 ohm/volt, ±3 percent.

1 — DC milliammeter, ±5 percent.

B. Power Requirements

+18 (±0.5) volts dc — 200 ma

+6 (±0.3) volts dc — 20 ma

C. Preliminary Procedure

(1) Set up the test circuit as shown in Fig. 31. The scope EXT SYNC TRIGGER selector should be set to the (+) positive position.

(2) Make the following settings on the test set:

(a) INPUT selector to position 1.

(b) TEST FUNCTION selector to position 2.

(c) FLIP-FLOP-MONOPULSER selector to MONOPULSER.

D. Testing Procedure

10.35 ***Diode Short Test:***

(a) This test is to be made before the card is inserted into the test set.

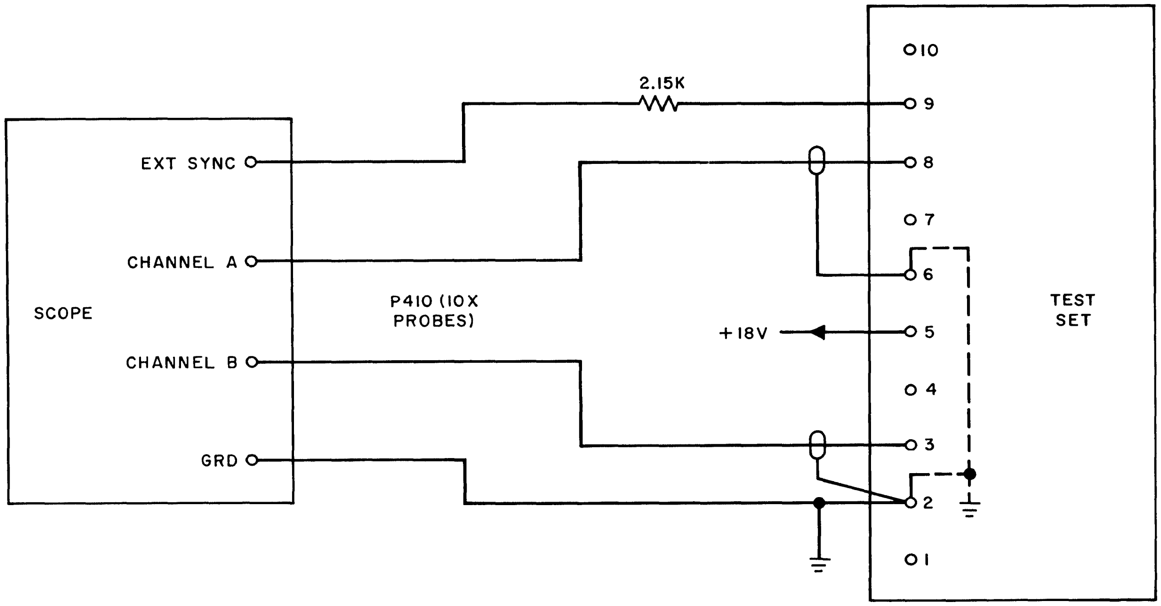

Fig. 31 — Monopulser Card Test

(b) Ground pin 1 and apply +6 (±0.3) volts dc to test point 8 of the card to be tested.

(c) The total current drawn shall be less than 3.0 ma dc.

10.36 ***Zener Voltage Test:***

(1) Insert the card to be tested into the test set monopulser test connector.

(2) The voltage between test point 8 and ground when measured with the voltmeter should be +6.2 (±0.6) volts dc.

10.37 ***Pulse Test — Normal Input:***

(1) Consult Table D to determine which monopulser and corresponding input resistor are under test.

TABLE D

KEY TO COMPONENTS UNDER TEST AT EACH POSITION OF TEST SET SWITCHES

TEST FUNCTION POSITION	INPUT SELECTOR POSITION	INPUT TERMINAL	INPUT RESISTOR	TRANSISTOR	OUTPUT TERMINAL
1	1	2	R1	Q1, Q2	6, 4
	2	22	R7	Q3, Q4	30, 36
	3	24	R13	Q5, Q6	32, 28
	4	13	R19	Q7, Q8	16, 18
	5	12	R25	Q9, Q10	11, 19
	6	14	R31	Q11, Q12	10, 36
2	1	7	R2	Q1, Q2	6, 4
	2	8	R8	Q3, Q4	30, 36
	3	9	R14	Q5, Q6	32, 28
	4	20	R20	Q7, Q8	16, 18
	5	40	R26	Q9, Q10	11, 19
	6	39	R32	Q11, Q12	10, 36

(2) Set the NORMAL-DEGRADED selector to NORMAL.

(3) Adjust potentiometer P1 until the voltage between J1 and ground measures +6.0 (±0.2) volts dc with the voltmeter.

(4) The input test pulse on J8 should be as specified in Fig. 32.

(5) Rotate the INPUT selector through positions 1 to 6. The output pulse on J3 should be as specified in Fig. 32 at each position.

(6) With the TEST FUNCTION selector in position 2, repeat as in (5).

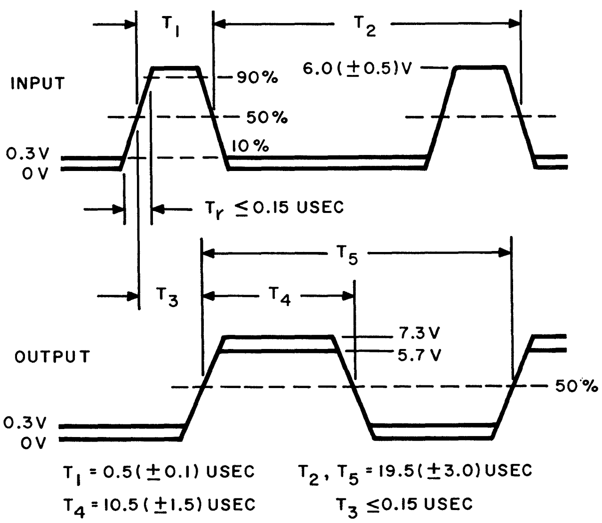

Fig. 32 — Monopulser Card Test

10.38 *Pulse Test — Degraded:*

(1) Set the NORMAL-DEGRADED selector to DEGRADED.

(2) Adjust potentiometer P1 until the amplitude of the input test pulse on J8 is 3.0 (±0.2) volts on the oscilloscope. The input test pulse should appear as in Fig. 31.

(3) Rotate the INPUT selector through positions 1 to 6. The output pulse on J3 should appear as in Fig. 33. Time base measurements need not be made on the output waveform.

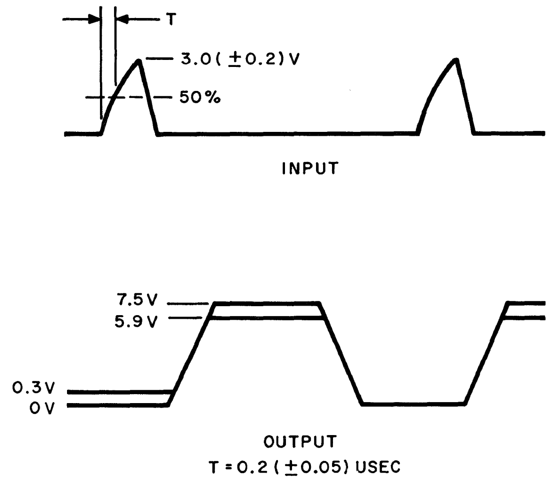

Fig. 33 — Monopulser Card Test

EIA INTERFACE TEST

A. Testing Equipment

1 — Oscilloscope, Tektronix 535A with plug-in unit-type 53/54C or C-A (or equivalent).

2 — Probes, Tektronix P410 (10X) (or equivalent).

1 — DC meter, 0 to 20 volts, 20,000 ohm/volt, ±3 percent.

1 — DC meter, 0 to 10 ma, ±3 percent.

4 — Resistors:

1 — 75 ohms, (±1 percent), 1 watt, WECo 144E (or equivalent).

1 — 147 ohms, (±1 percent), 2 watts, WECo 147D (or equivalent).

1 — 600 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

1 — 2.15k ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

1 — Mercury relay, WECo 291A (or equivalent).

1 — Square-Wave generator Hewlett-Packard model 211A (or equivalent).

1 — 2-section, 10-position rotary wafer switch.

B. Power Requirements

+18.0 (±0.5) volts dc — 200 ma

—18.0 (±0.5) volts dc — 100 ma

+6.0 (±0.3) volts dc — 10 ma

C. Test Procedure

10.39 ***+6.8 Volts DC Regulator Diode Test:***

(a) Connect ground to terminals 5 and 17 and apply +18 (±0.5) volts dc to terminal 1. The voltage between test point 8 and ground should be +6.8 (±0.9) volts dc.

10.40 ***—6.8 Volts DC Regulator Diode Test:***

(a) With terminals 5 and 17 connected to ground, apply —18 (±0.5) volts dc to terminal 20. The voltage between test point 12 and ground shall be —6.8 (±0.9) volts dc.

10.41 ***Output Clipping Diode Short Test:***

(a) With the card connected as in the suggested test circuit shown in Fig. 34, connect +6.0 (±0.3) volts dc to test point 8 of the card.

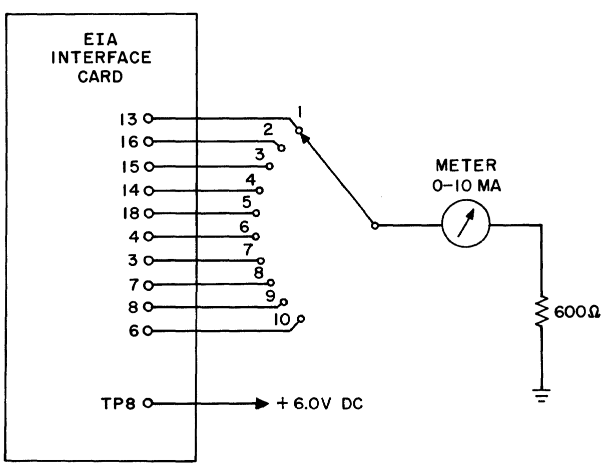

Fig. 34 — EIA Interface Test

Measure the current drawn at each output terminal by rotating the switch through positions 1 to 10. At each position of the switch the current drawn should be less than 1.5 ma dc.

10.42 ***Input Regulator Diode Test:***

(a) With the card connected as in the suggested test circuit shown in Fig. 35, connect ground to terminals 5 and 17, +18 (±0.5) volts dc to terminal 1, and —18 (±0.5) volts dc to terminal 20. Measure the voltage between the input and test point 12 of each of the five driver inverters by rotating the switch through positions 1 to 5. This voltage should be +9.3 (±1.0) volts dc.

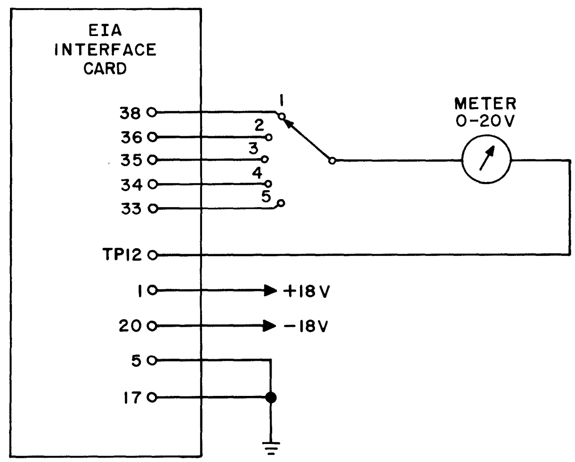

Fig. 35 — EIA Interface Test

10.43 ***Pulse Tests:***

(a) With the card connected as in the suggested test circuit shown in Fig. 36, connect ground to terminals 5 and 17, +18 (±0.5) volts dc to terminal 1, and —18 (±0.5) volts dc to terminal 20. Temporarily short terminal 1 to terminal 3 of the mercury relay. The voltage between point A and ground should measure +6.0 (±0.3) volts dc with the voltmeter. Remove the short on the mercury relay and set the frequency of the square-wave generator between 40 and 50 cps. Set the EXT SYNC TRIGGER on the scope to (+) positive.

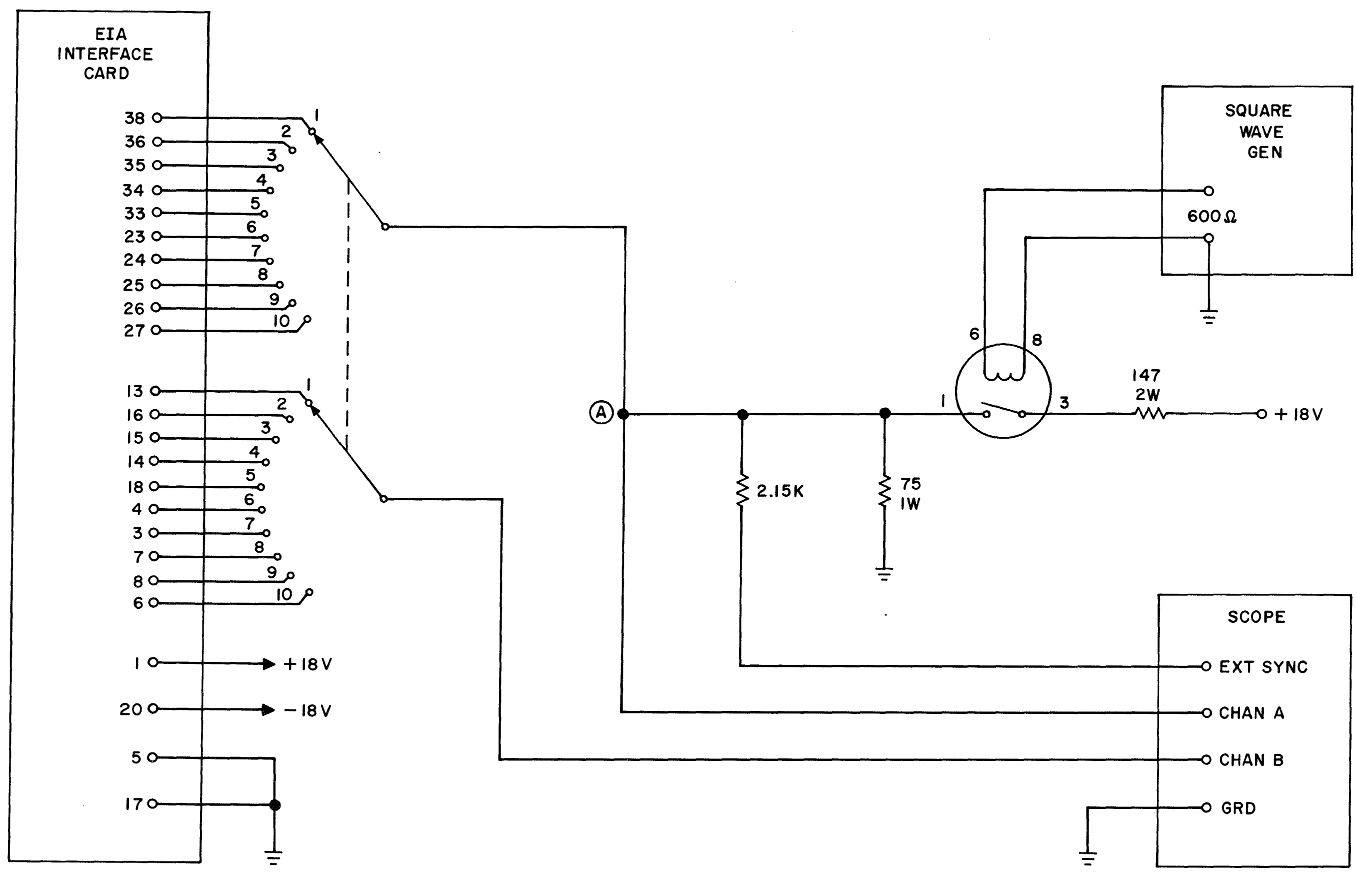

Fig. 36 — EIA Interface Test

10.44 *Turn-On Time:*

(1) Rotate the switch through positions 1 to 5. The input-output waveforms shall be as specified in Fig. 37.

(2) Rotate the switch through positions 6 to 9. The input-output waveforms shall be as specified in Fig. 38.

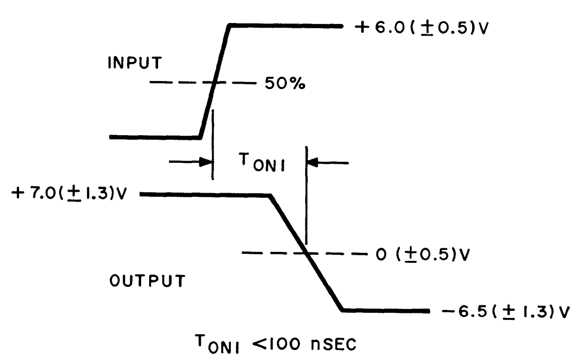

Fig. 37 — EIA Interface Test

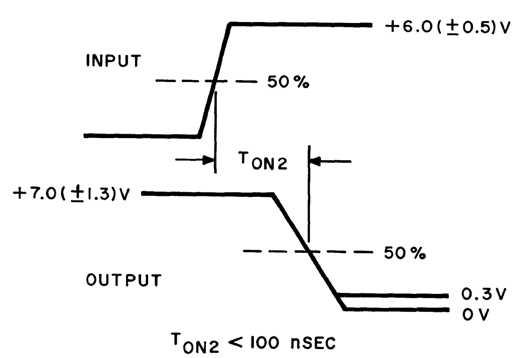

Fig. 38 — EIA Interface Test

(3) Rotate the switch to position 10. The input-output waveforms shall be as specified in Fig. 39.

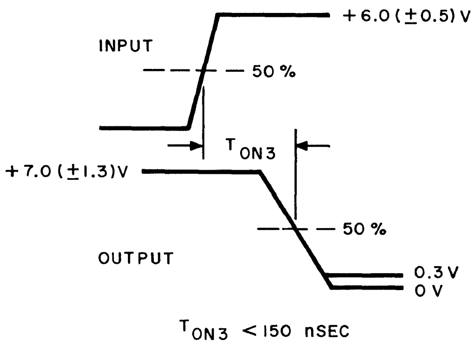

Fig. 39 — EIA Interface Test

10.45 ***Turn-Off Time:***

(1) Set the EXT SYNC TRIGGER to (—) negative.

(2) Repeat 10.44 (1), (2), and (3). Input-output waveforms shall be as specified in Fig. 40, 41, and 42, respectively.

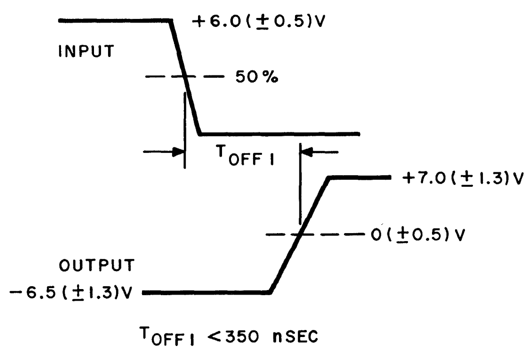

Fig. 40 — EIA Interface Test

REMOTE TEST CIRCUIT CARD

A. Testing Equipment

1 — Oscilloscope, Tektronix 535 or 535A with plug-in unit-type 53/54C or C-A (or equivalent).

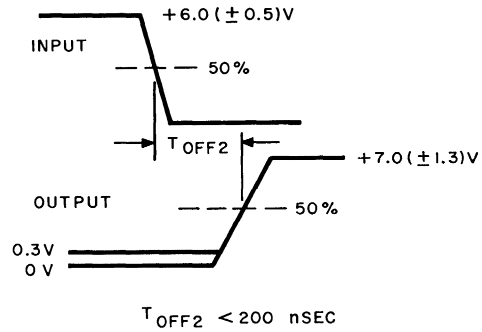

Fig. 41 — EIA Interface Test

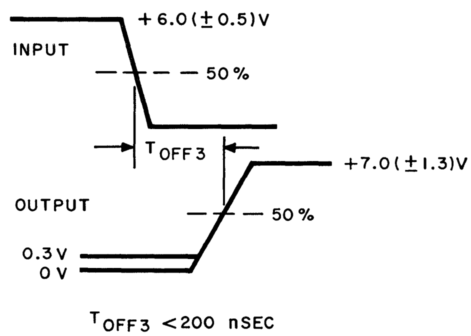

Fig. 42 — EIA Interface Test

2 — Probes, Tektronix P410 (10X) (or equivalent).

2 — Square-Wave generators, Hewlett-Packard model 211A (or equivalent).

1 — DC voltmeter, 20,000 ohm/volt, ±3 percent.

1 — Ohmmeter, ±5 percent.

1 — Capacitor, 40 uf, (±20 percent), WECo 602A (or equivalent).

5 — Resistors:

1 — 5.11k ohms, (±1 percent), 1/2 watt, WECo 221A (or equivalent).

1 — 2.15k ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

1 — 19.6k ohms, (±1 percent), 1/2 watt, WECo 221A (or equivalent).

1 — 215 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

1 — 1.78 meg, (±1 percent), 1/2 watt, WECo 221A (or equivalent).

1 — Switching diode, KS-16986, L2 (or equivalent).

B. Power Requirements

+18.0 (±0.5) volts dc — 50 ma

−18.0 (±0.5) volts dc — 5 ma

C. Test Procedure

10.46 ***Resistance Test:***

(a) The resistance between terminals 6 and 8 shall be 3160 ohms (±5 percent).

(b) The resistance between terminals 1 and 2, terminal 1 and test point 10, and between terminal 20 and test point 11 shall be 1960 ohms (±5 percent).

(c) The resistance between terminals 19 and 20 shall be 681 ohms (±5 percent).

(d) The resistance between terminals 1 and 4 shall be 681 ohms (±5 percent).

(e) The resistance between terminals 1 and 3 shall be 11,000 ohms (±5 percent).

10.47 ***Diode Leakage Test:***

(1) Connect terminals 5 and 17 to ground. Connect +18.0 (±0.5) volts dc in series with a 1.78 ±1 percent meg resistor to terminal 6. The current drawn from the +18.0 volt dc supply shall be less than 7.0 ua.

(2) Repeat (1) for terminal 7.

10.48 ***Strap Test:***

(1) Using the ohmmeter, the resistance measured between the following terminals shall be less than 1 ohm.

FROM	TO
Terminal 22	Terminal 23
Terminal 24	Terminal 25
Terminal 26	Terminal 27
Terminal 28	Terminal 29
Terminal 30	Terminal 31
Terminal 32	Terminal 33
Terminal 34	Terminal 35
Terminal 36	Terminal 37
Terminal 38	Terminal 39

10.49 ***Zener Voltage Test:***

(a) With ground connected to terminals 5 and 17, apply +18.0 (±0.6) volts dc to terminal 1.

(b) The voltage between test point 2 and ground shall be +6.2 (±0.5) volts dc.

10.50 ***Pulse Forming Network Dynamic Test:***

(1) With ground connected to terminals 5 and 17 and +18.0 (±0.5) volts dc connected to terminal 1, connect the card as in the suggested test circuit shown in Fig. 43. Set the frequency of the square-wave generator to 2.5 kcps (±10 percent).

(2) Set the scope EXT SYNC TRIGGER SLOPE to (+) positive.

(3) The input waveform at terminal 7 shall be as specified in Fig. 44.

(4) The output waveform at terminal 12 shall be as specified in Fig. 44.

(5) Connect the card as in the suggested test circuit shown in Fig. 45.

(6) The input waveforms at terminals 7 and 11 shall be as specified in Fig. 46. The relative phase of the input waveforms is immaterial.

(7) The voltage at test point 5, when measured with the voltmeter, should be +10.0 (±1.5) volts dc.

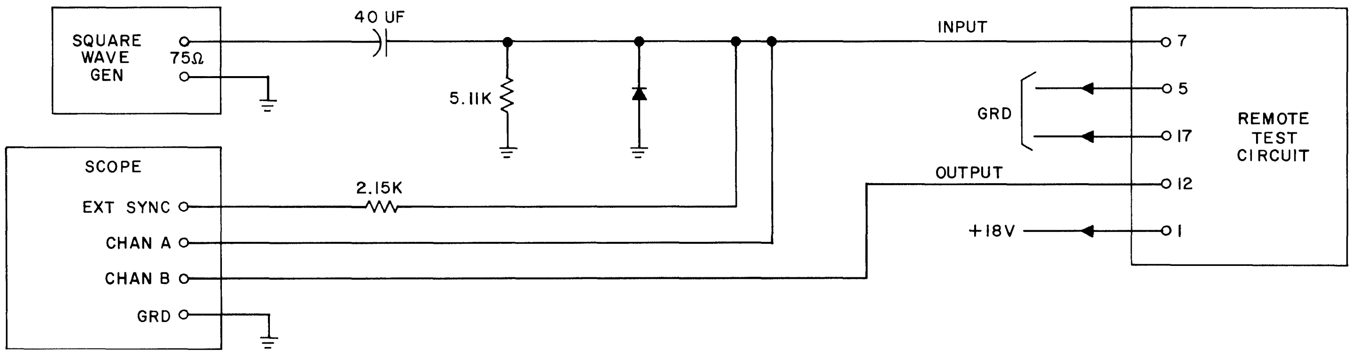

Fig. 43 — Remote Circuit Card Test

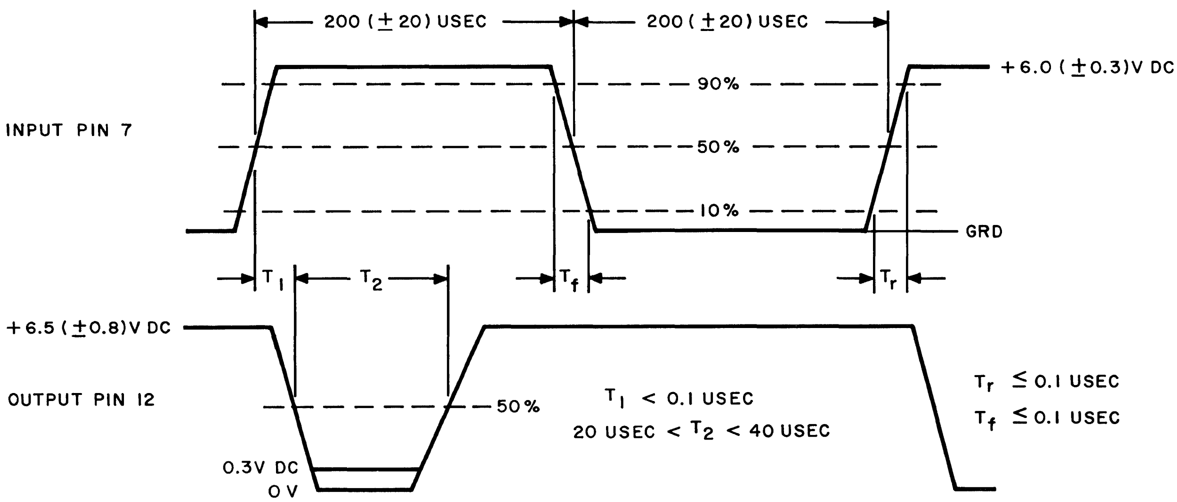

Fig. 44 — Remote Circuit Card Test

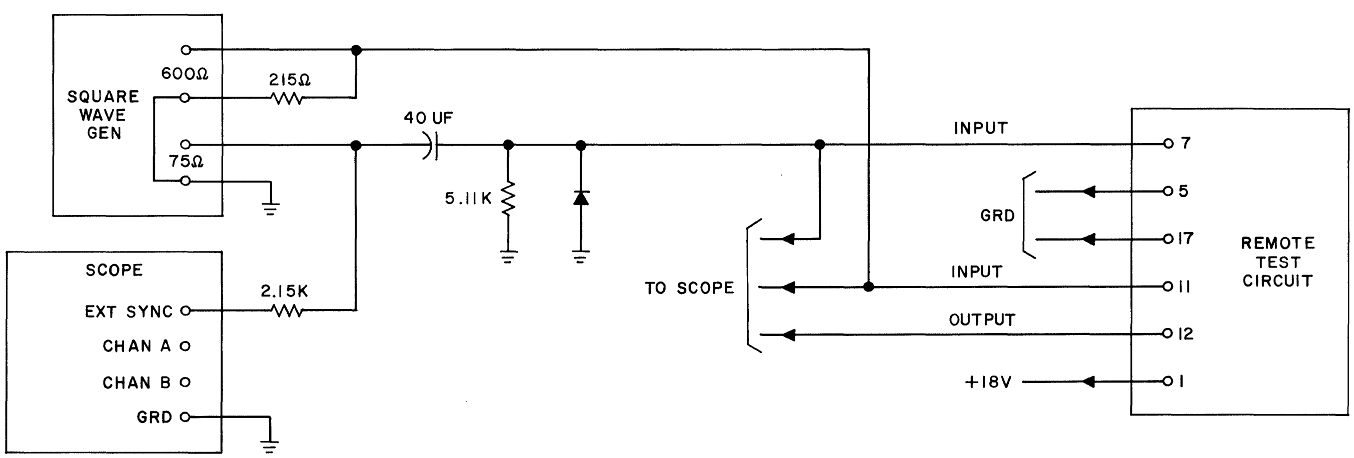

Fig. 45 — Remote Circuit Card Test

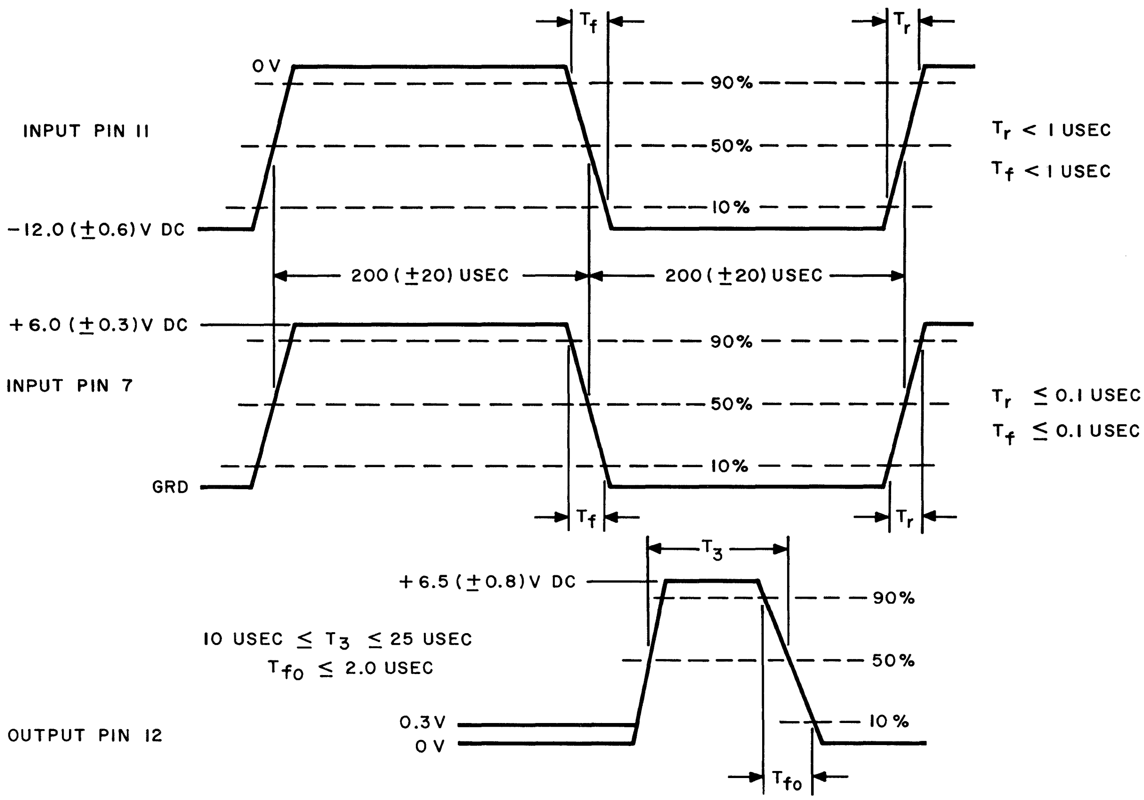

Fig. 46 — Remote Circuit Card Test

(8) Set the scope EXT SYNC TRIGGER SLOPE to the (—) negative position.

(9) The output waveform shall be as specified in Fig. 46.

10.51 ***Relay and Relay Driver Test:***

(1) Connect ground to terminals 5 and 17, +18.0 (±0.5) volts dc to terminal 1, and —18.0 (±0.5) volts dc to terminal 20.

(2) With test point 8 connected to test point 13, and test point 7 connected to ground, measure the resistance between terminal 15 and ground. The resistance shall be less than 1 ohm.

Caution: Do not use 1X range on ohmmeter.

(3) Remove the connection between test point 7 and ground. The ohmmeter should indicate an open circuit between terminal 15 and ground. Remove the connection between test point 13 and test point 8.

(4) Connect the card as in the suggested test circuit shown in Fig. 47. Set the frequency of the square-wave generator to 10 cps (±10 percent).

(5) The input waveform at terminal 14 and the output waveform at terminal 15 shall be as specified in Fig. 48. No time base measurements need to be made.

MIL. STD 188 INTERFACE TEST

A. Testing Equipment

1 — Oscilloscope, Tektronix 535A with plug-in unit-type 53/54C (or equivalent).

2 — Probes, Tektronix P410 (10X) (or equivalent).

1 — DC voltmeter, 0 to 10 volts dc, 20,000 ohm/volt calibrated to 0.5 percent full scale accuracy.

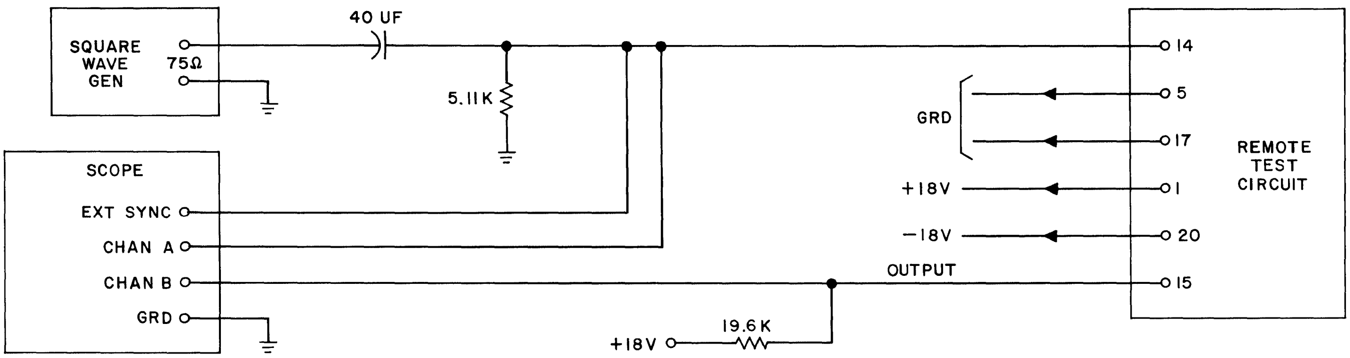

Fig. 47 — Remote Circuit Card Test

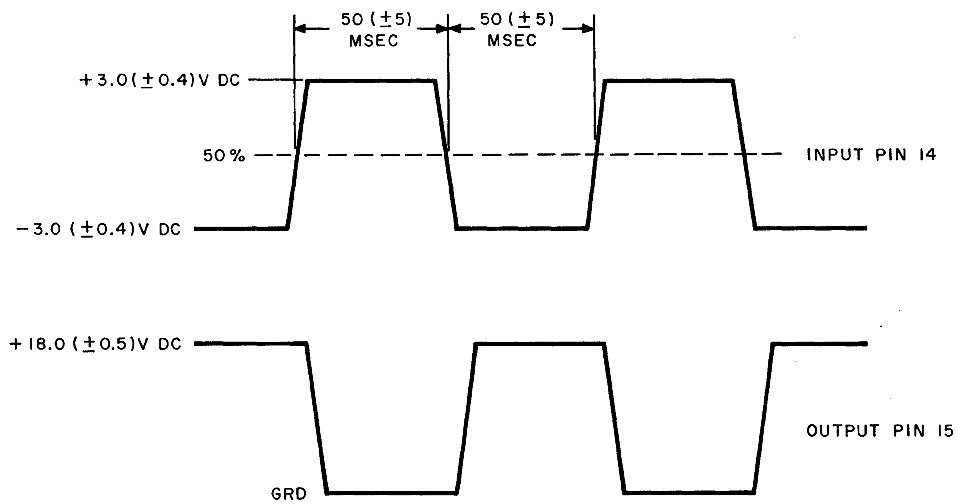

Fig. 48 — Remote Circuit Card Test

1 — Square-Wave generator, Hewlett-Packard 211A (or equivalent).

1 — Sine-Wave generator, Hewlett-Packard 200 CD (or equivalent).

1 — AC voltmeter, Hewlett-Packard 400L (or equivalent).

1 — Transformer, WECo Rep 120C (or equivalent).

1 — Capacitor, 40 uf, (±20 percent), WECo 602A (or equivalent).

4 — Resistors:

1 — 5110 ohms, (±1 percent), 1/2 watt, WECo 221A (or equivalent).

1 — 2150 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

1 — 511 ohms, (±1 percent), 1/2 watt, WECo 221A (or equivalent).

1 — 100 ohms, (±1 percent), 1/2 watt, WECo 221A (or equivalent).

B. Power Requirements

+18 (±0.5) volts dc — 50 ma

−18 (±0.5) volts dc — 50 ma

C. Test Procedure and Requirements

10.52 ***Zenner Voltage Test:***

(1) With ground connected to terminals 5 and 17 and +18.0 (±0.5) volts dc applied to terminal 1, measure the voltage between test point 3 and ground with the calibrated voltmeter. The voltage should be between +5.8 and +6.6 volts dc.

(2) Apply −18.0 (±0.5) volts dc to terminal 20. Measure the voltage between test point 6 and ground with the calibrated voltmeter. The voltage should be between −5.8 and −6.6 volts dc.

10.53 ***Driver Pulse Test:***

(1) With the card connected as in the suggested test circuit shown in Fig. 49, connect +18.0 (±0.5) volts dc to terminal 1, −18.0 (±0.5) volts dc to terminal 20, and ground to terminals 5 and 17.

(2) Set the frequency of the square-wave generator to about 5000 cps with a duty cycle of 50 percent.

(3) Set the scope EXT TRIGGER SLOPE to the (+) positive position.

(4) The input waveform should be as specified in Fig. 50.

(5) Observe the output of each of the three interface drivers by rotating the switch through positions 1 to 3. At each position the output shall be as specified in Fig. 50.

(6) Set the scope EXT TRIGGER SLOPE to the (−) negative position. Rotate the switch through positions 1 to 3. The output waveform at each position shall be as specified in Fig. 50.

10.54 ***Terminator Balance Adjustment:***

(1) With the card connected as in the suggested test circuit as shown in Fig. 51, connect +18.0 (±0.5) volts dc to terminal 1, −18.0 (±0.5) volts dc to terminal 20, and ground to terminals 5, 13, and 17.

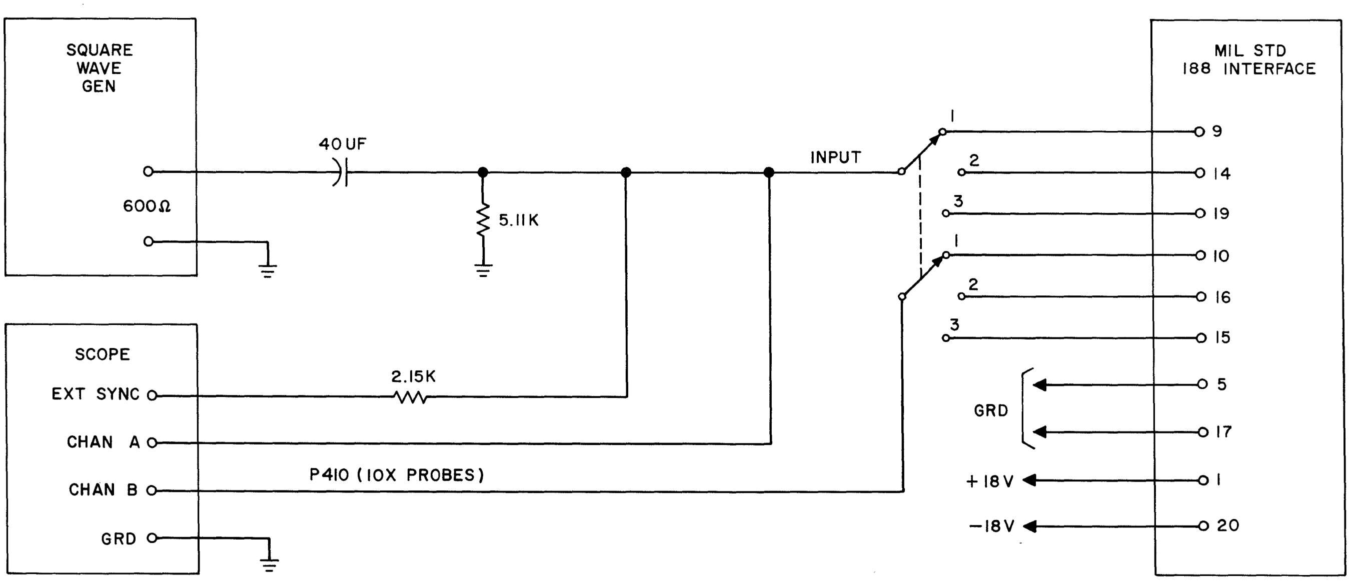

Fig. 49 — MIL. STD 188 Interface Test

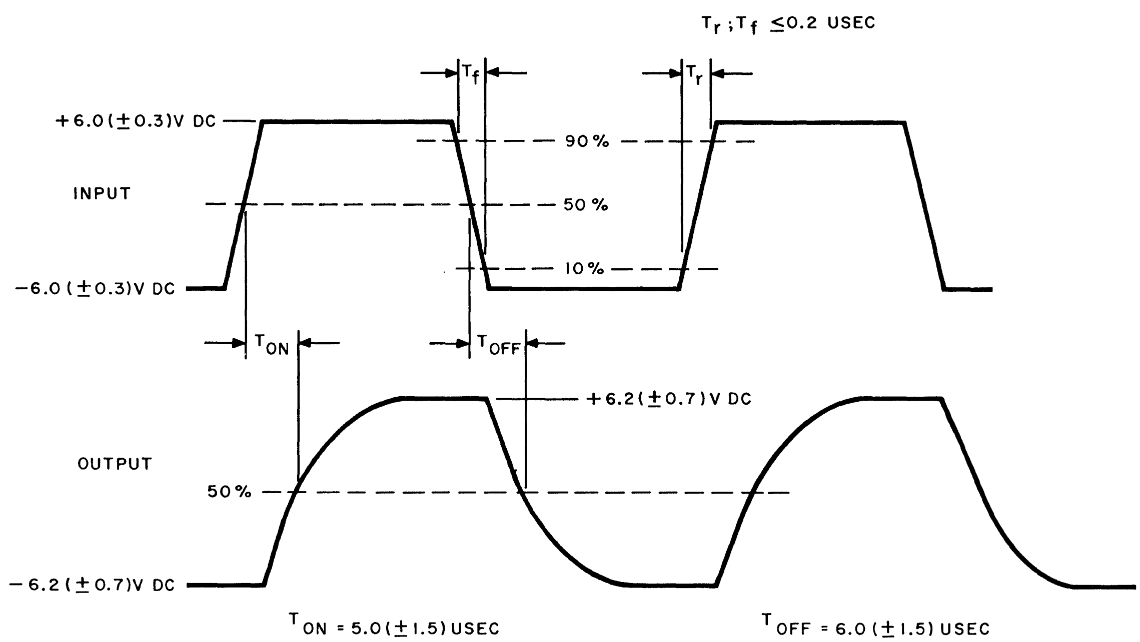

Fig. 50 — MIL. STD 188 Interface Test

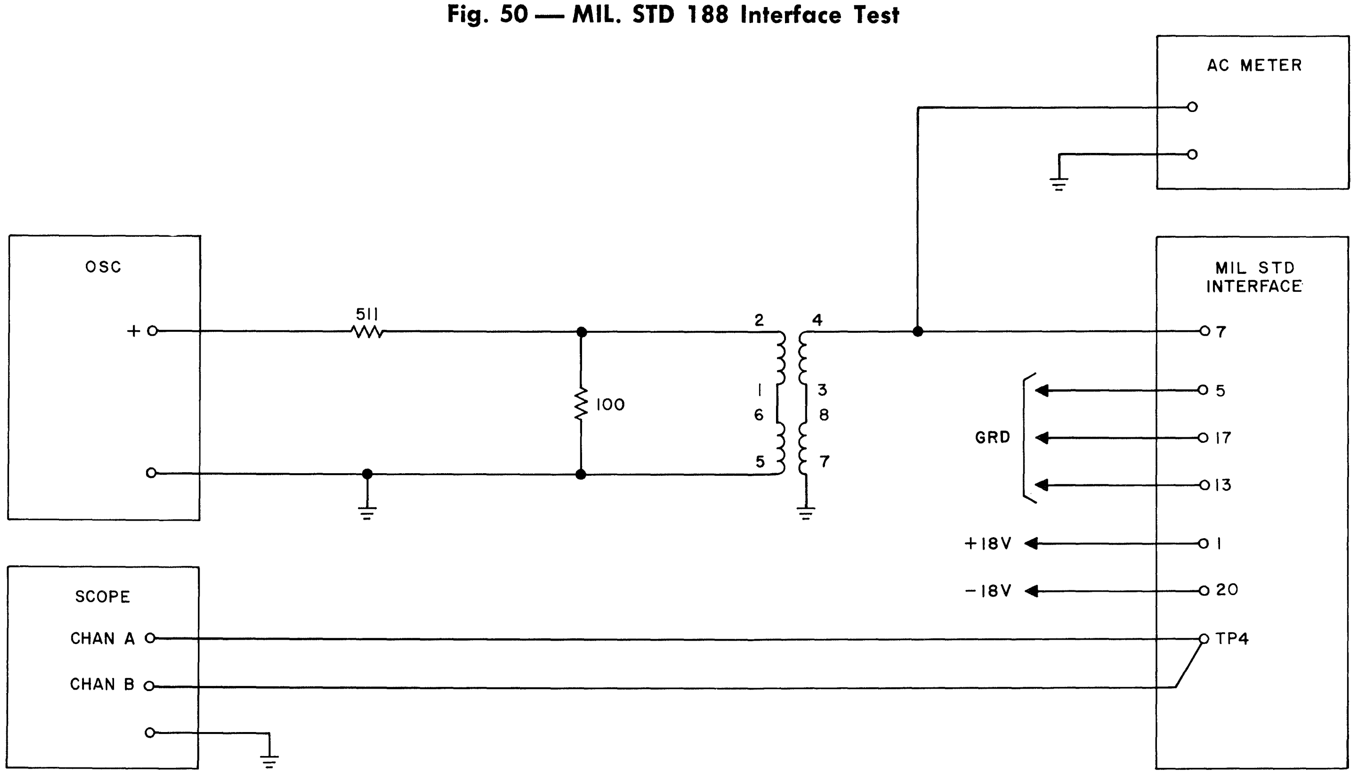

Fig. 51 — MIL. STD 188 Interface Test

(2) Set the controls on the oscillator so that the input sine wave to terminal 7 is about 1.5 volts rms with a period of 200 (±10.0) usec (5000 cps).

(3) Make the following settings and connections on the scope.

(a) Connect the vertical signal output to the TIME BASE B TRIGGER input.

(b) Rotate the TIME BASE A TRIGGER stability control fully clockwise.

(c) Set the MODE selector on the dual trace amplifier to ALTERNATE.

(d) On the dual trace amplifier set the CHAN A polarity switch to the (+) positive position and the CHAN B polarity switch to the (−) negative position.

(e) Set the TIME BASE B TRIGGER mode to the dc position and the trigger slope to the (+) EXT position.

(f) Set the TIME BASE B TIME/CM selector to 20 usec.

(g) Set HORIZONTAL DISPLAY to B.

(4) Adjust the TIME BASE B STABILITY and TRIGGERING LEVEL controls to obtain a display of the waveform on test point 4. Overlay the CHAN A and CHAN B waveforms, as shown in Fig. 52, by adjusting the AMPLIFIER VERTICAL POSITION controls. The TRIGGERING LEVEL control should be set in a region where a slight counterclockwise or clockwise movement does not cause TD to vary.

(5) Adjust potentiometer R10 until the negative transition of the A sweep precedes the negative transition of the B sweep by approximately 20 usec.

(6) Reduce the amplitude of input sine wave to 0.35 (±0.01) volt rms.

(7) Rotate potentiometer R10 clockwise until the negative transition of the A sweep precedes the negative transition of the B sweep by approximately 4 usec (i.e., T_D approximately 4 usec, see Fig. 52).

(8) Set the HORIZONTAL DISPLAY selector to the B-INTENSIFIED-BY-A position. Set the TIME BASE A TIME/CM selector to 1 usec.

(9) Adjust the delay time multiplier until the intensified portion of the sweep overlays the negative transitions of the displayed waveforms.

(10) Rotate the HORIZONTAL DISPLAY selector to the A-DELAYED-BY-B position.

(11) Rotate R10 clockwise until T_D is less than 0.5 usec. Because of backlash, it is important that the final setting be made in the clockwise direction. If T_D is made greater than 0.5 usec by excessive clockwise rotation of R10, back off in the counterclockwise direction until T_D is approximately equal to 10 usec, then reduce T_D to less 0.5 usec by rotating R10 in the clockwise direction.

(12) Set the HORIZONTAL DISPLAY selector to the B position. Set the AMPLIFIER MODE switch to the A ONLY position. Reduce

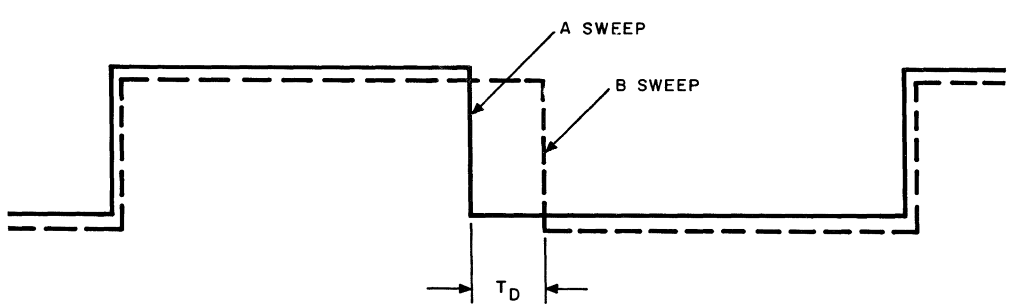

Fig. 52 — MIL. STD 188 Interface Test

the amplitude of input sine wave on terminal 7 to 0.1 (±0.005) volt rms. A square wave, with arbitrary duty cycle, should be observed at test point 4. No time base measurements need be taken.

(13) After initial adjustment of R10 and upon subsequent tests of the MIL. STD 188 interface card it shall not be required to adjust R10 if T_D is less than 4 usec.

10.55 ***Terminator Pulse Test:***

(1) Connect the card as in the suggested test circuit shown in Fig. 53.

(2) Set the frequency of the square-wave generator to 5000 cps (±5 percent) with a duty cycle of 50 percent. Set the amplitude of the input pulse on terminal 7 (test point 8) to 12.0 (±0.6) volts dc.

(3) The input pulse on the test point 8 should be as specified in Fig. 52.

(4) Set the scope EXT SYNC TRIGGER SLOPE to the (+) positive position. The output pulse on terminal 12 should be as specified in Fig. 54 (1). Measure T17. Set the EXT SYNC TRIGGER SLOPE to the (—) negative position and measure T27.

(5) The output pulse on terminal 11 should be as specified in Fig. 54 (2). With the EXT SYNC TRIGGER SLOPE set at the (+) positive position, measure T14. Set the trigger slope to the (—) negative position and measure T24.

TRANSMIT-RECEIVE SWITCH TEST

Note: Located on the card are four slotted machine screw terminals numbered from 1 to 4. A strap should be inserted between screws 3 and 4. There should not be a strap between screws 1 and 2.

A. Testing Equipment

1 — DC vacuum tube volt-ohmmeter, Hewlett-Packard 412A (or equivalent).

3 — Resistors:

1 — 1000 ohms, (±1 percent), 1/2 watt, WECo 145A (or equivalent).

1 — 1.78 meg, (±1 percent), 1/2 watt, WECo 221A (or equivalent).

1 — 2370 ohms, (±5 percent), 1/2 watt, WECo 221A (or equivalent).

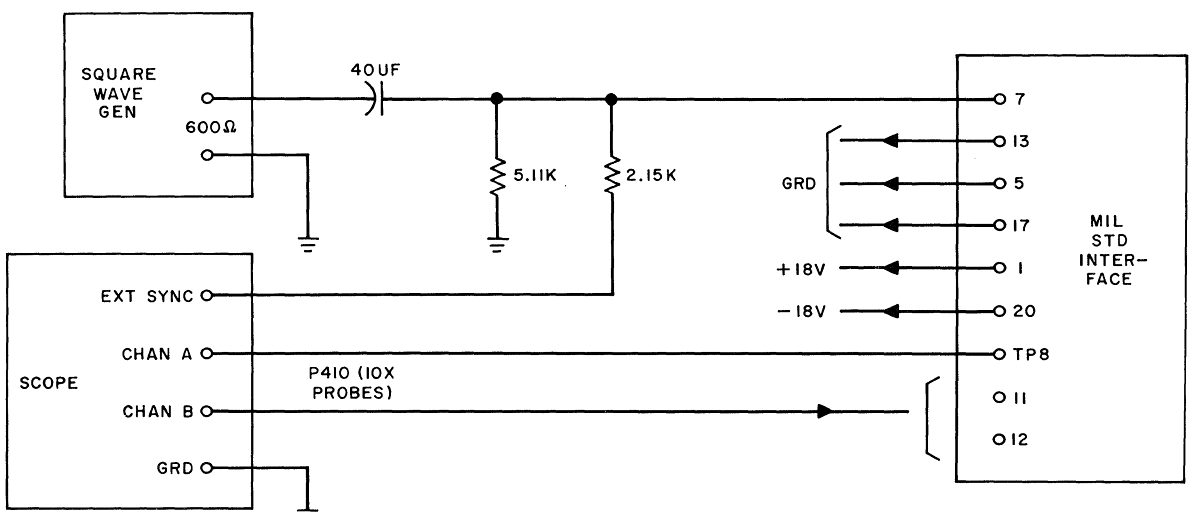

Fig. 53 — MIL. STD 188 Interface Test

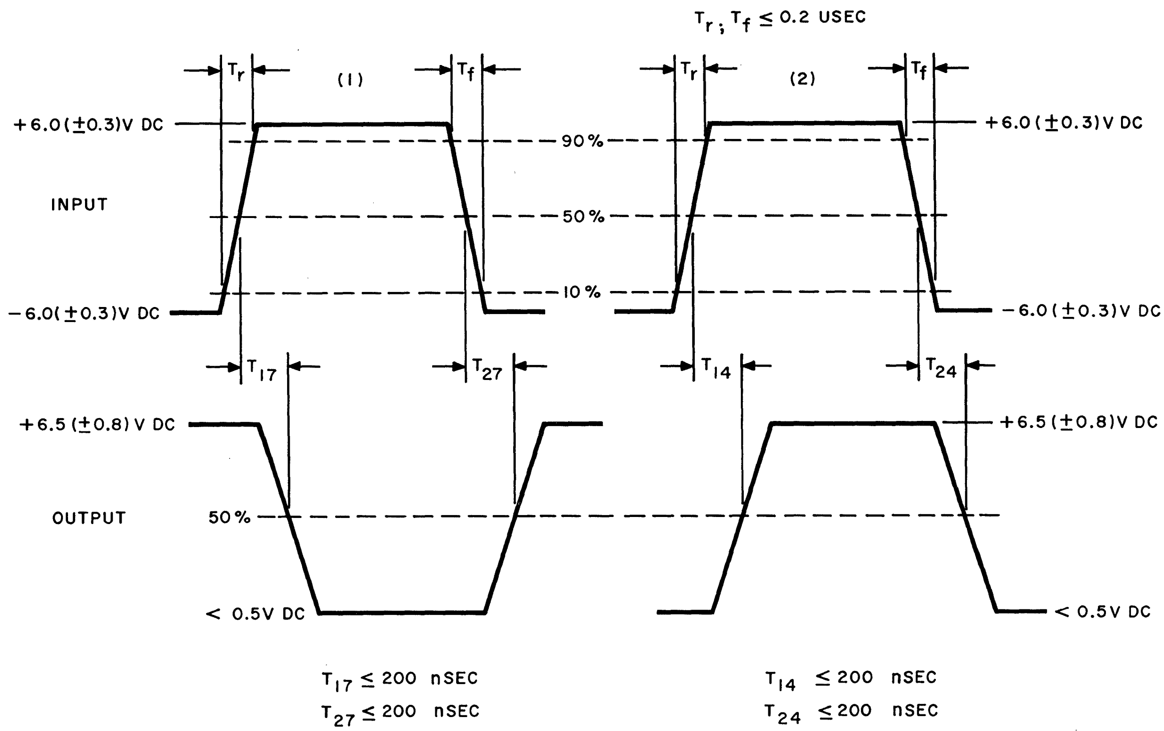

Fig. 54 — MIL. STD 188 Interface Test

B. Power Requirements

+18.0 (±0.5) volts dc — 75 ma

+30.0 (±1.5) volts dc — 50 ma

C. Test Procedures

10.56 ***Resistance Tests:***

(a) The following resistance tests are to be made before voltage is applied to the card. Connect ground to terminals 5 and 17.

(b) The resistance between the following terminals shall be as indicated.

TERMINALS	RESISTANCE VALUE OHMS
13 to 14	20 (±20%)
13 to 18	521 (±10%)
19 to 38	68 (±20%)
3 to 8	348 (±5%)
9 to 22	348 (±5%)
11 to 10	316 (±5%)
12 to 31	316 (±5%)

TERMINALS	RESISTANCE VALUE OHMS
4 to GRD	Less than 1
6 to GRD	Less than 1
15 to GRD	Less than 1
16 to GRD	Less than 1
40 to GRD	Less than 1
Screw No. 1 to 23	Less than 1
Screw No. 2 to GRD	Less than 1
Screw No. 3 to GRD	Less than 1
Screw No. 3 to 40	Less than 1

(c) The following resistance tests result in values that depend on the direction of current flow from the test instrument. In Table E the resistance values indicated correspond to current flow from terminal A to terminal B as listed. In the Hewlett-Packard model 412A, test current flows from the MA/OHM probe when the TEST FUNCTION selector is in the ohms position, therefore the MA/OHM probe should be applied to the terminal listed as FROM, and the common probe to the terminal listed as TO.

10.57 ***Diode Leakage Test:***

(a) Remove ground from terminals 5 and 17.

(1) Connect +18.0 (±0.5) volts dc in series with a 1.78 (±1 percent) meg resistor to terminal 11. Apply ground to terminal 9. The current drawn from the +18.0 volt dc supply shall be less than 7.0 ua dc.

(2) Repeat (1) for terminal 12 with ground connected to terminal 8.

(3) Repeat (1) for terminal 9 with ground connected to terminal 8.

(4) Repeat (1) for terminal 8 with ground connected to terminal 9.

10.58 ***Zener Voltage Test:***

(1) With ground connected to terminals 5 and 17, connect +18.0 (±0.5) volts dc to terminal 1.

(2) The voltage between terminal 37 and ground shall be +6.8 (±0.8) volts dc.

(3) The voltage between test point 6 and ground shall be +12.0 (±1.7) volts dc.

(4) Apply +30.0 (±1.5) volts dc in series with a 1000-ohm (±1 percent) resistor to terminal 29. The voltage between terminal 29 and ground shall be +18.0 (±2.3) volts dc.

(5) Repeat (4) for terminals 39, 11, and 12.

10.59 ***Bias Voltage Test:***

(a) With ground connected to terminals 5 and 17 and +18.0 (±0.5) volts dc connected to terminal 1, the voltage between terminal 8 and ground, between terminal 9 and ground, between terminal 11 and ground, and between terminal 12 and ground shall be 3.0 (±0.3) volts dc.

10.60 ***T-R Switch Driver Test:***

(a) Make the following connection on the card under test:

(1) Connect ground to terminals 5 and 17.

(2) Connect +18.0 (±0.5) volts dc to terminal 1.

(3) Connect terminal 11 to terminal 37.

(4) Connect a 2370-ohm (±1 percent) resistor between terminals 37 and 2.

(5) Connect terminal 9 to terminal 33.

(b) The voltage between terminal 27 and ground shall be less than 1 volt dc.

(c) Remove the connection between terminals 37 and 2. Connect ground to terminal 2.

(d) The voltage between terminal 27 and ground shall be +11.8 (±1.6) volts dc.

TABLE E

CURRENT FLOW RESISTANCE VALUES

TERMINALS		REMARKS	RESISTANCE
FROM	TO		OHMS
27	33		196 (±5%)
33	27	RANGE Selector on 100X	Less than 100
11	7	RANGE Selector on 100X	Less than 100
7	11		1210 (±5%)
12	30	RANGE Selector on 100X	Less than 100
30	12		1210 (±5%)

DEMODULATOR CARD TEST

A. Power Requirements

+18.0 (±0.5) volts dc — 25 ma

−18.0 (±0.5) volts dc — 100 ma

B. Testing Equipment

1 — Oscilloscope, Tektronix 535A with type D high-gain dc differential plug-in amplifier (or equivalent).

2 — Oscillators, Hewlett-Packard 200CD (or equivalent).

1 — DC voltmeter, 20,000 ohm/volt, ±3 percent, Hewlett-Packard 412A (or equivalent).

1 — AC voltmeter, ±3 percent, Hewlett-Packard 400L (or equivalent).

2 — Capacitors, 2 uf (±5 percent), WECo 542F (or equivalent).

C. Test Procedure

10.61 ***Zener Voltage Test:***

(a) Connect ground to terminals 5 and 17, +18.0 (±0.5) volts dc to terminal 1, and −18.0 (±0.5) volts dc to terminal 20.

(b) The voltage between test point 3 and ground shall be −8.2 (±1.1) volts dc.

(c) The voltage between test point 6 and ground shall be +6.2 (±0.6) volts dc.

(d) The voltage between test point 4 and terminal 20 shall be +12 (±2.0) volts dc.

10.62 ***Demodulator Test:***

(1) Connect the card as in the suggested test circuit shown in Fig. 55.

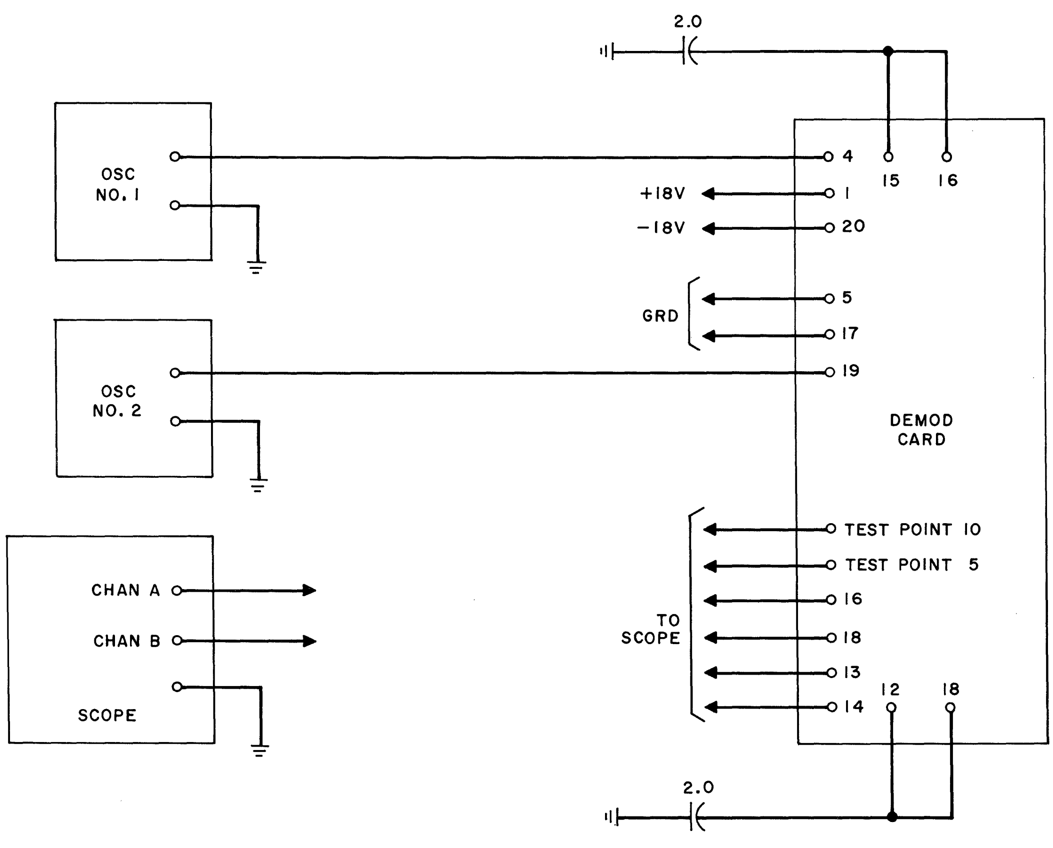

Fig. 55 — Demodulator Card Test

(2) With the amplitude control of oscillator No. 2 set to 0, temporarily connect ground to input terminal 19.

(3) Set the controls of oscillator No. 1 to produce a 0.2 (±0.005) volt rms signal at 1800 cps between input terminal 4 and ground. The waveform between test point 5 and ground shall be a sine wave of 0.68 (±0.15) volts peak-to-peak.

(4) Remove the ground connection from input terminal 19. With the amplitude control of oscillator No. 1 set to 0, temporarily connect ground to terminal 4.

(5) Set the controls of oscillator No. 2 to produce a 0.5 (±0.005) volt rms signal at 1800 cps between input terminal 19 and ground. The waveform between test point 10 and ground shall be a sine wave of 0.68 (±0.15) volt peak-to-peak. Remove the ground connection from terminal 4.

(6) Set the controls of oscillator No. 1 to produce a 0.32 (±0.005) volt rms signal at 1800 cps between input terminal 4 and ground.

(7) Set the controls of oscillator No. 2 to produce a 0.80 (±0.005) volt rms signal at 1800 cps between input terminal 19 and ground.

(8) Connect the scope, using the differential mode of operation, to terminals 16 and 18. Satisfactory synchronization may be obtained by connecting EXT SYNC to VERTICAL SIGNAL OUT on the scope. The output waveform shall be a sine wave. Trace the frequency of oscillator No. 2 in the vicinity of 1800 cps until the frequency of the output sine wave is approximately 2 cps. The output sine wave shall be 12.5 (±2.5) volts peak-to-peak.

(9) With the controls of the oscillators set as in (8), connect the scope, using the differential mode, to terminals 13 and 14. The output waveform shall be a square wave of approximately 2 cps with amplitude 12.4 (±1.2) volts peak-to-peak.

(10) Increase the frequency of oscillator No. 2 to approximately 2700 cps. With the EXT SYNC TRIGGER SLOPE set to the positive (+) position, expand the TIME/CM selector until an overlay of positive transitions is displayed on the scope as shown in Fig. 56. The rise time of the first transition shall be as specified in Fig. 56.

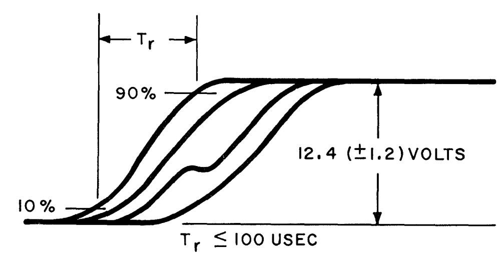

Fig. 56 — Demodulator Card Test

(11) Momentarily turn off oscillator No. 1. The differential voltage between terminals 13 and 14 shall be less than 150 mv peak-to-peak. Turn on oscillator No. 1. Momentarily turn off oscillator No. 2. The differential voltage between terminals 13 and 14 shall be less than 150 mv peak-to-peak.